Low-inductance decoupling capacitor for the thermal conduction modules of the IBM Enterprise System/9000 processors

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Multilayer ceramic decoupling capacitors fabricated using a barium titanate-based dielectric are used with the glass-ceramic/copper/polyimide substrates of the thermal conduction modules (TCMs) of the IBM Enterprise System/9000™ processors to suppress the voltage noise generated by the logic circuits of the semiconductor chips used in the processors. Use is made of thick-film multilayer ceramic fabrication processes and thin-film termination processes to achieve substrate-mounted capabilities which, when combined with the low-inductance design of the capacitors, minimize the inductance of the decoupling paths to their adjacent chips. When mounted on the glass-ceramic/copper/polyimide substrate of a water-cooled TCM, the capacitors suppress approximately 50% of the voltage noise, thereby enhancing the performance of the TCMs.

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Introduction

Because of current flow during the simultaneous switching of the circuits of digital systems, voltage fluctuations are generated across power supply buses. The magnitude of these fluctuations depends on the amount of current, its rise time, and the effective chip and package inductances. This noise can couple through a quiet logic circuit driver and appear as a spurious voltage signal on the input terminals of a logic receiver circuit, sometimes causing switching [1, 2].

Although improved system performance usually requires a decrease in rise time and an increase in circuit density, these trends exacerbate this "simultaneous switching" problem to the point that it can become a serious limitation to the system performance.

One way of managing this noise problem is to use decoupling capacitors to supply the current needed by the switching circuits and decouple it from the package inductance [2, 3]. This approach is used with both the alumina/molybdenum/polyimide and glass-ceramic/copper/polyimide substrates used in the IBM Enterprise System/9000™ (ES/9000™) mainframe processors. Overviews of the substrates and associated first-level packaging aspects of those processors may be found in [4, 5]. Ceramic decoupling capacitors are mounted directly onto the substrate at the corner of each chip site to lower the inductance of the current supply circuits to the chip. The substrate can accommodate up to 144 capacitors arranged in this fashion.

This paper covers aspects of the design, structure, fabrication, reliability, and performance of the decoupling capacitors.

Design considerations

The effectiveness of a decoupling capacitor is determined by the magnitude of the voltage drop developed across its terminals and its proximity to the switching circuit. For a unit current flow, the smaller the voltage drop developed, the more effective the decoupling capacitor will be. Four components contribute to the voltage drop V:

$$V = V_c + V_{ci} + V_l + V_r. \quad (1)$$

The component V_c is the voltage drop expected from the change in the charge content of an ideal capacitor. The component V_{ci} is an additional voltage drop caused by any rolloff of the dielectric constant at high frequencies. The voltage drops V_l and V_r are related to the internal inductance and the internal resistance of the capacitor electrodes.

These voltage drops can be related to conventional capacitor parameters by the equation

$$V = Q/C + V_{ci} + Ldi/dt + Ri, \quad (2)$$

where

Q = charge on the capacitor,
C = equivalent series capacitance (ESC) for an equivalent capacitor having an ideal dielectric,
L = capacitor equivalent series inductance (ESL),
R = capacitor equivalent series resistance (ESR).

In designing a capacitor, one must first determine the total voltage drop V allowed for a given current flow. This voltage drop is then partitioned into the various components given in Equation (1). From Equation (2) it can be seen that V_c is determined by the capacitance of the capacitor and the change of the charge content in the capacitor due to the current flow. The voltage drop V_{ci} results from the rolloff of the dielectric constant with an increasing rate of change of the charge content. It can be maintained to less than 10% of V_c by properly selecting a material whose dielectric constant does not roll off appreciably below the cutoff frequency of 1 GHz. The voltage drop V_r is determined by the resistivity of the internal electrodes of the capacitor. The inductive voltage drop V_l is related to the geometry of the capacitor, as discussed below.

- *Design of a capacitor having low internal inductance*

For high-speed circuits, such as those used in the ES/9000 processors, the inductive voltage drop becomes the dominant component among the last three terms of Equation (2). Therefore, minimization of the internal inductance of a decoupling capacitor becomes a key element in its design. This is achieved by using short current flow paths and reducing the magnetic flux between adjacent current flow paths.

Short current flow paths can be achieved by connecting many small capacitors in parallel to form one structure, and utilizing a plurality of termination points. The multiple termination points permit current to be injected into and extracted from the capacitor through an array of closely spaced contacts, thereby enabling current flow in many short paths. This is in contrast to the larger, single pair of series connections typical of standard decoupling capacitors [6]. Reduction of magnetic coupling between current flow paths is achieved by ensuring the flow of opposing currents in adjacent electrodes. The prototype low-internal-inductance decoupling capacitor structure depicted in **Figure 1** was proposed [7, 8] on the basis of these concepts. Its unit cell consists of three parallel, vertical electrodes. The space between the electrodes is filled with a high-dielectric-constant material. Each electrode contains tabs that are connected by rectangular shorting bars, as shown in the figure. The complete capacitor is formed by repeating six of the unit cells, which are electrically connected in parallel.

• *Comparison with experiment*
Experimental capacitors similar in design to the prototype structure were fabricated [9] and their input impedance determined. Their parallel plate capacitance was calculated in a conventional manner, and their inductance and resistance were calculated by the modeling technique described in [10].

The experimental units contained a barium titanate-based dielectric and internal electrodes of Pt. The shorting bars were a trilayer structure consisting of Al sandwiched between levels of Ti-W alloy.

The input impedance of the experimental capacitors was determined from reflection coefficient measurements using a high-frequency wave analyzer. Typical measured values of the real and imaginary parts of the input impedance for each of three experimental capacitors are shown in **Figure 2**. The correlation between the average of the measured values is within 10% of those calculated from the model.

These input impedance measurements could then be related to equivalent capacitor parameters. The equivalent series resistance (ESR) could be obtained from the real part of the input impedance at low frequency. The equivalent series capacitance (ESC) could be determined from the imaginary part of the input impedance at low frequency. Finally, the equivalent series inductance (ESL) could be obtained from the imaginary part of the input impedance at high frequency.

Decoupling capacitor for the ES/9000 processors

On the basis of the results of the electrical modeling and measurements on the experimental capacitors, a modified decoupling capacitor [11] was designed for use with the substrates of the ES/9000 processors. The capacitor, depicted in **Figure 3**, is also fabricated using a barium titanate-based ceramic having a high dielectric constant, making it possible to achieve a large capacitance/size ratio. It retains the tabbed vertical plate feature of the prototype design to lower its internal inductance. Modifications such as a reduction in the number of tabs per plate and the use of shorting lands instead of shorting bars have been used to facilitate the manufacture of the capacitor and enhance its reliability.

• *Capacitor structure*
The body of the decoupling capacitor measures nominally 0.875 mm by 1.60 mm by 1.85 mm. It is composed of groupings of vertical internal electrodes separated by layers of dielectric. Use is made of two types of electrodes, each having two small tabs. The electrodes are alternately arranged in groups of eight—four of each type—in a manner that allows the tabs to exit the terminating surface. On the terminating surface, tabs of similar alignment are interconnected by shorting lands.

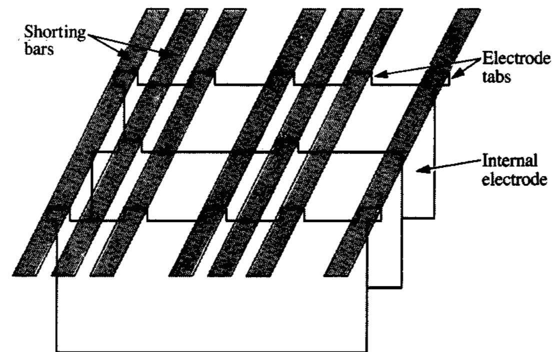

Figure 1

Unit cell of prototype low-internal-inductance capacitor. The complete capacitor is formed by a parallel array of six cells.

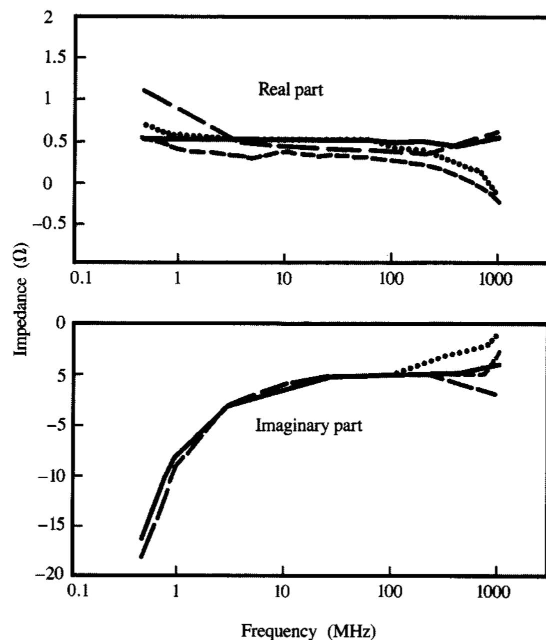

Figure 2

Calculated (solid lines) and measured input impedances of three experimental capacitors.

Thus, for each grouping of eight internal electrodes, there are four shorting lands alternately addressing each electrode type. The capacitor is composed of four of these

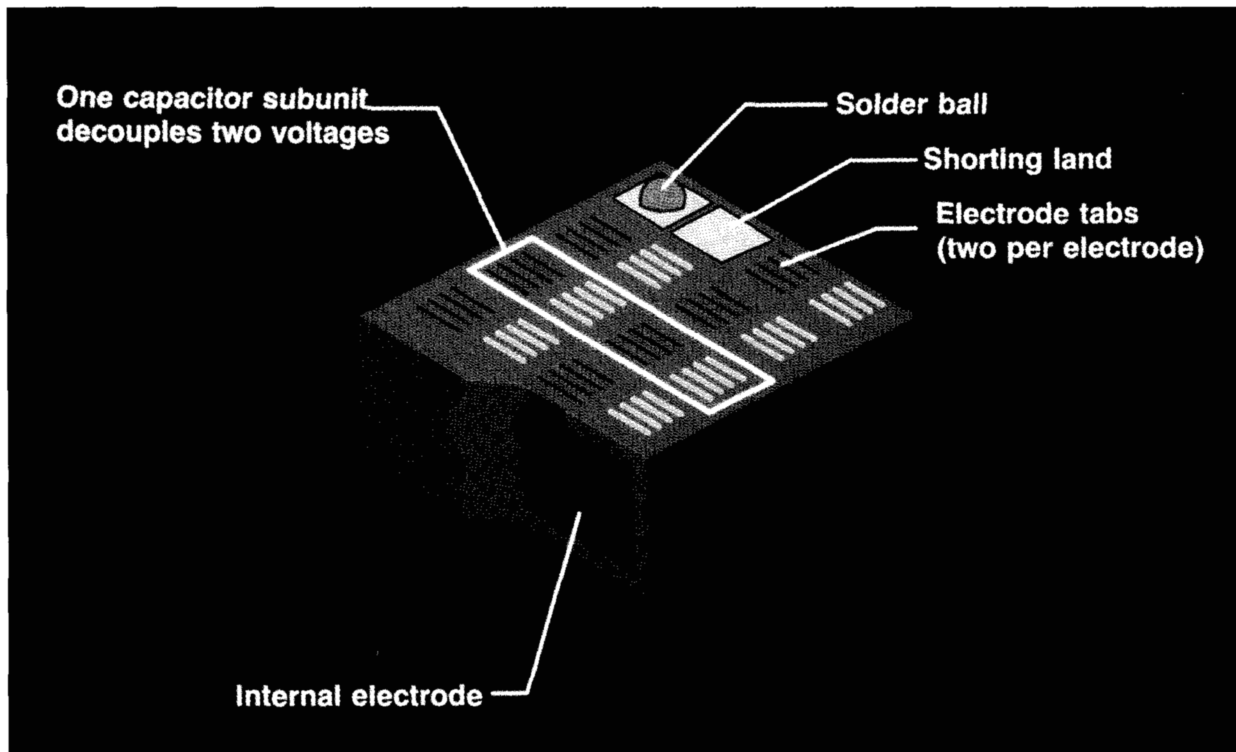

Figure 3

Decoupling capacitor structure; its nominal dimensions are 0.875 mm × 1.60 mm × 1.85 mm.

electrode groups—in essence, four individual capacitors, or subunits—and 16 accompanying shorting lands. The shorting lands measure 0.3 mm by 0.4 mm, somewhat larger than the groupings of tabs they are used to connect. This land size is also large enough to allow for the alignment of the solder balls that are deposited onto them and used to connect the capacitor to a substrate.

- *Capacitor requirements*

Since each decoupling capacitor consists of four capacitor subunits, it can be deployed in a variety of ways determined by the voltages of the substrate lands to which it is connected. On one extreme, eight separate voltages can be decoupled. In that case, each capacitor subunit operates independently of the others. The other extreme involves the decoupling of only two voltages; in that case, all four capacitor subunits are connected in parallel. That capability makes the capacitor quite versatile, but it renders its electrical characteristics application-dependent. In this paper, to eliminate confusion, the electrical requirements for the capacitor are indicated for each of its subunits.

The electrical requirements for each subunit of the capacitor are ESL ≤ 135 pH, ESR ≤ 100 mΩ, and capacitance ≥ 6 nF. The capacitor must also be able to function at a temperature of 60°C, at frequencies up to 1 GHz, and at voltages ≤ 5 V. Since the capacitors are designed to be attached to the surface of glass-ceramic/copper/polyimide substrates, minimal changes should occur in their electrical parameters as the capacitors undergo the various thermal excursions (to 365°C) needed to join them to the substrates, or during chip replacement.

- *Capacitor body materials*

The capacitor body is fabricated from a high-dielectric-constant barium titanate-based ceramic. The high dielectric constant permits the interelectrode ceramic layers to be relatively thick (~30 μm). Such a dielectric thickness, in turn, increases the reliability of the capacitor by inhibiting interelectrode shorting.

The barium titanate-based ceramic has additional benefits. It has long been used to fabricate conventional capacitors, giving it a strong history of manufacturability. The material has also been found to resist chemical reduction [9], making it compatible with reducing atmospheres that may be needed in solder joining. Finally, the material has been found to be capable of retaining a high dielectric constant at the temperature

and frequency (60°C, 1 GHz) up to which it is required to function.*

The internal electrodes used in the capacitor body are platinum. The sintering temperature of the metal paste used to form the electrodes is compatible with that of the dielectric, and the resulting electrodes are chemically stable and inert. As a result, the capacitor can withstand reducing atmospheres [9], and is resistant to corrosion and metal migration, thereby promoting good reliability.

- *Capacitor body fabrication*

The processes used to fabricate the capacitor body are similar to conventional multilayer ceramic processes [6], as indicated in **Figure 4**. Ceramic powders are mixed with organic binders to form a slurry that is cast into greensheets. The greensheets are blanked and mounted onto metal frames to increase their stability during screening. Metal paste electrode patterns are screened onto the individual sheets using conventional thick-film techniques. The capacitor bodies are formed, and the organic binders are carefully removed in a lengthy baking process. The ceramic and metal electrode patterns are densified during sintering. The sintered capacitors are then subjected to a tumbling operation to remove sharp edges.

The equipment used to form the capacitor bodies is essentially a sophisticated punch and die cavity apparatus. Prior to the forming process, metal paste electrodes are screened in rows and columns onto a greensheet. In this pattern, all of the electrodes needed for an individual capacitor are contained in one column. The number of these columns of electrodes specifies the number of capacitors that will be formed. The greensheet is indexed over the die cavities, and the first electrode/dielectric layer of each capacitor is punched and stacked in the cavity. The entire sheet then advances to the second row of electrodes, where the second electrode/dielectric layers are punched and stacked. This procedure is repeated until the entire capacitor configuration has been stacked within the cavity. The final stroke of the punch is used to laminate the individual layers. By using this technique, it is possible to fabricate up to 50 layers while maintaining the alignment required for the electrode tabs.

- *Capacitor termination*

As indicated in **Figure 5**, capacitor termination is achieved through the use of shorting lands, ball-limiting metallization (BLM), and solder balls. The shorting lands are Cr pads that are electrically conducting while providing the necessary adhesion to the ceramic surface. The BLM and solder balls are essentially the same as the ones used in forming the C4s (controlled collapse chip connections) in chip fabrication [12]. The BLM consists of layers of Cr, Cu, and Au. It provides a wettable surface for the solder and restricts it from spreading over the shorting land surface. The solder consists of a Pb-Sn alloy.

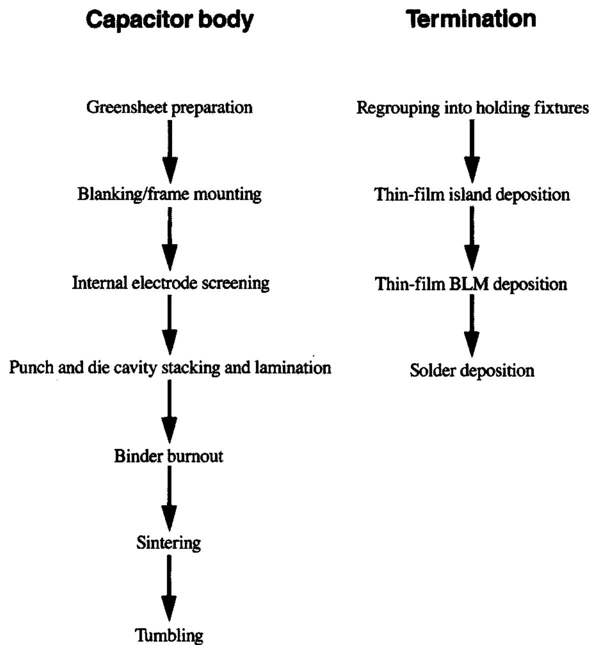

Figure 4

Processes for fabrication of body and terminals of decoupling capacitor.

Termination is achieved by using the thin-film processes indicated in Figure 4. To achieve alignment of the terminal metals to the tabs, the capacitors are precisely fitted into the orifices of a fixture. A mask having the shorting land patterns is then aligned to this fixture. After deposition of the shorting lands, the fixture is used with a mask for depositing the BLM and solder configurations. The use of large shorting lands eases the alignment tolerances required for the BLM and solder. Melting of the solder to form the completed C4 configuration constitutes the final step in capacitor fabrication.

- *Capacitor reliability*

The reliability objectives of the low-inductance decoupling capacitor were that no field fails should occur. Frequently reliability is ensured through burn-in stressing of capacitors at elevated temperatures and/or voltages to screen defective components prior to use. The reliability of the decoupling capacitor, however, is favored by its design.

*J. A. Weiss and T. Y. F. Tsang, Dept. of Physics, Worcester Polytechnic Institute, Worcester, MA, unpublished results.

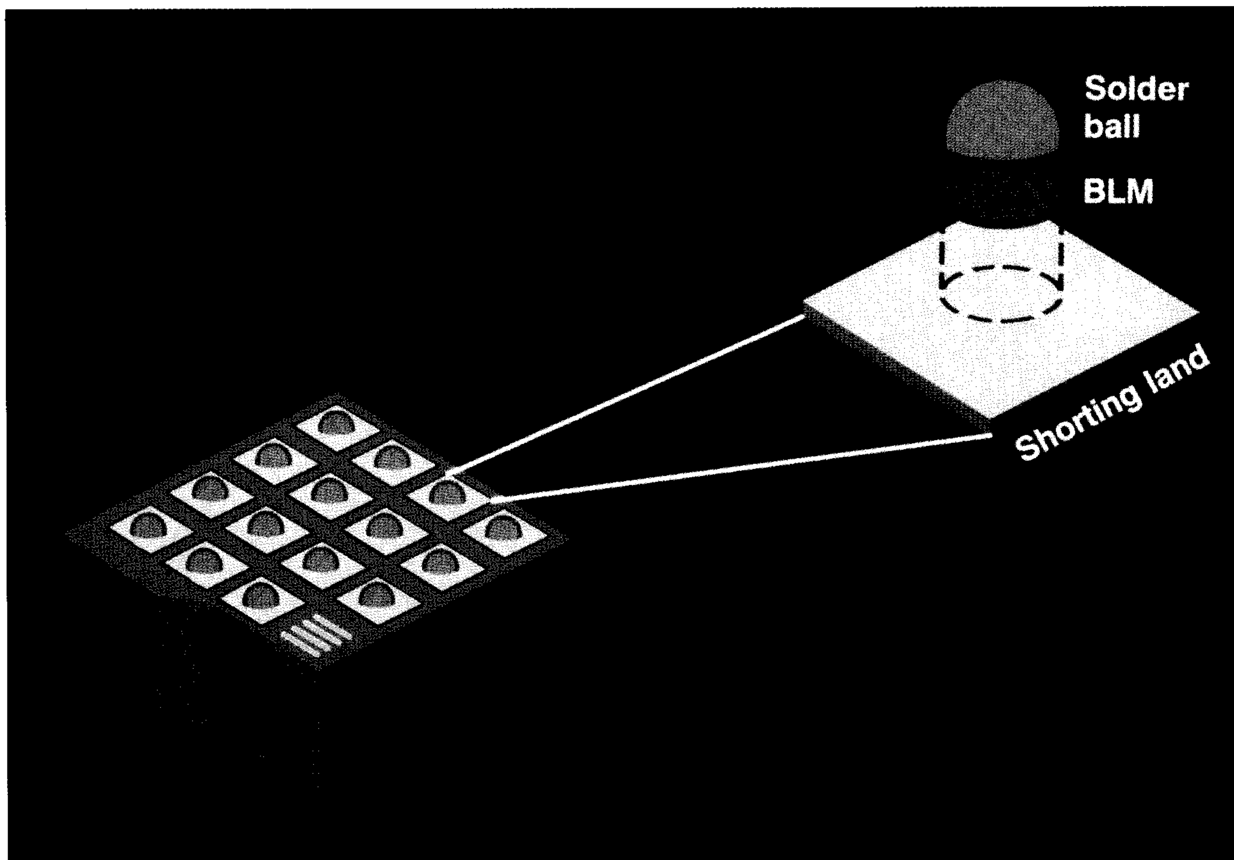

Figure 5

Capacitor termination.

For example, most conventional SMT (surface mount technology) multilayer ceramic capacitors have Ag-Pd internal electrodes; their attachment to printed circuit boards can cause cracking of the ceramic dielectric, providing a path for the deleterious migration of silver.

With the decoupling capacitor, the use of the C4 mounting technique provides multiple attachment points to the substrate, minimizing stress on the capacitor and thereby essentially eliminating cracking. Additionally, the Pt internal electrodes provide no migrating species.

A battery of highly accelerated stress tests were chosen to assess the reliability of the decoupling capacitor. Capacitors were stressed, both individually and after being attached to substrates. The stress tests used in the assessment are summarized in **Table 1.** Included were tests at elevated temperatures, voltages, and humidity levels as well as aggressive cycling conditions.

Nominal operating conditions for the decoupling capacitor are 60°C, 5 V, and 8% relative humidity. Using models to relate the accelerated test conditions to the nominal operating conditions, the tests performed stressed the capacitors far beyond an equipment operating life of 100 000 hours and/or 2500 on-off cycles. While the actual models used are confidential, they are derived from published models. The humidity model is based on that of Brunaer, Emmett, and Teller [13]. An Arrhenius relationship is used to model the effect of temperature. The effects of voltage are derived from a voltage law relationship [14], and cyclic fatigue effects originate from Coffin–Manson relationships [15].

Key parameters monitored during the stress tests included insulation resistance, capacitance, resistance changes, and evidence of corrosion or cracking. Despite the high stress conditions, the decoupling capacitor showed no failures, although some due to silver migration were observed in several conventional SMT multilayer capacitors that were subjected to similar stress conditions.

- *Capacitor performance*

Measurements at room temperature of the inductance, metal resistance, capacitance, and insulation resistance, summarized in **Table 2,** indicated that design objectives

Table 1 Stress tests used to assess reliability of decoupling capacitors.

Test	*Conditions*	*Potential failure modes*
Temperature/voltage	125°C/15 V 125°C/50 V	Metal migration, intra/interlevel shorts
Temperature/humidity/voltage	85°C/81% R.H./6 V 85°C/81% R.H./0 V	Corrosion, intra/interlevel shorts
Voltage cycling	0 to 15 V, 72 cycles per day	Leakage, capacitance degradation
Temperature cycling	0 to 100°C, 72 cycles per day −55 to 125°C, 8 cycles per day 25 to 365°C, up to 18 cycles −40 to 60°C, 10 cycles	Resistance, capacitance degradation, leakage, solder joint integrity, cracking
Impact shock	300 G of force	Mechanical integrity
Vibration	5 to 500 Hz	Mechanical integrity

were met or exceeded. For example, when the capacitors were mounted on glass-ceramic/copper/polyimide substrates of water-cooled TCMs to be used in an ES/9000 processor, the presence of the decoupling capacitors resulted in a ~50% suppression of the noise resulting from the simultaneous switching of circuits. A further increase in noise suppression would require the capacitors to be mounted even closer to the chips (to further reduce the inductance of the total decoupling circuit).

Summary

The barium titanate-based decoupling capacitor described here represents an enhancement to the conventional multilayer ceramic capacitor. It is based on design features that minimize its internal inductance, and is fabricated using a combination of thick-film multilayer ceramic processes and thin-film termination processes. The capacitor has exceeded its low-inductance design objectives, and it has passed a series of stringent reliability tests. Finally, it has proved capable of significantly suppressing voltage noise, thereby enhancing the performance of a TCM.

Acknowledgments

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Table 2 Electrical design objectives compared to measured values for capacitor subunits. Measurements were carried out at room temperature.

Parameter	*Objective*	*Measured values*
Inductance	≤135 pH	45 to 60 pH
Resistance	≤0.1 Ω	0.07 Ω
Capacitance	≥6 nF	8 to 10 nF
Insulation resistance	>1 GΩ	5 GΩ

References

1. E. E. Davidson, "Electrical Design of a High Speed Computer Package," *IBM J. Res. Develop.* **26**, No. 3, 349–361 (1982).
2. C. W. Ho, D. A. Chance, C. H. Bajorek, and R. E. Acosta, "The Thin-Film Module as a High-Performance Semiconductor Package," *IBM J. Res. Develop.* **26**, No. 3, 286–296 (1982).
3. D. Akihiro, W. Toshihiko, and N. Hideki, "Packaging Technology for the NEC SX-3/SX-X Supercomputer," *Proceedings of the 40th Electronic Components and Technology Conference*, IEEE, 1990, pp. 525–533.
4. J. U. Knickerbocker, G. B. Leung, W. R. Miller, S. P. Young, S. A. Sands, and R. F. Indyk, "IBM System/390 Air-Cooled Alumina Thermal Conduction Module," *IBM J. Res. Develop.* **35**, No. 3, 330–341 (1991).
5. R. R. Tummala, H. R. Potts, and Shakil Ahmed, "Packaging Technology for IBM's Latest Mainframe Computers (S/390/ES9000)," *Proceedings of the 41st Electronic Components and Technology Conference*, IEEE, 1991, pp. 682–688.
6. J. Adair, D. Anderson, G. Dayton, and T. Shrout, "A Review of the Processing of Electronic Ceramics with an Emphasis on Multilayer Capacitor Fabrication," *J. Mater. Educ.* **9**, Nos. 1 & 2, 71–118 (1987).
7. I. Feinberg and L. L. Wu, "Thick Film Capacitor Having Very Low Inductance," U.S. Patent 4,274,124, June 16, 1981.
8. C. H. Bajorek, D. A. Chance, C. W. Ho, and D. A. Thompson, "Multiple Layer, Ceramic Carrier for High Switching Speed VLSI Chips," U.S. Patent 4,328,530, May 4, 1982.

9. J. M. Oberschmidt and J. N. Humenik, "A Low Inductance Capacitor Technology," *Proceedings of the 40th Electronic Components and Technology Conference*, IEEE, 1990, pp. 284–288.
10. A. E. Ruehli, "Inductance Calculations in a Complex Integrated Circuit Environment," *IBM J. Res. Develop.* **16**, No. 5, 470–480 (1972).
11. A. Arnold, M. Bariether, S. U. Chiang, H. Dalal, R. A. Miller, F. A. Montegari, J. Oberschmidt, and D. T. Shen, "Multilayer Capacitor," U.S. Patent 4,831,494, May 16, 1989.
12. L. F. Miller, "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Develop.* **13**, No. 3, 239–250 (1969).
13. A. W. Adamson, *Physical Chemistry of Surfaces*, 2nd ed., Interscience Publishers (John Wiley & Sons), New York, 1967, pp. 584–594.
14. M. Shatzkes and M. Av-Ron, "Determination of Breakdown Rates and Defect Densities in SiO_2," *Thin Solid Films* **91**, 217–230 (1982).
15. K. C. Norris and A. H. Landzberg, "Reliability of Controlled Collapse Interconnections," *IBM J. Res. Develop.* **13**, No. 3, 266–271 (1969).

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