GENERAL ELECTRIC

70A111154

PRINT DIST.	SENSE LINE MODULE INSTALLATION SPECIFICATION	CONT. ON 1 SH. NO. 0
K7-20		(02-062A20)

GENERAL NOTES

F.C.F.
FMF: GE-PAC 30

APPROVED BY: E. A. Lita DATE: January 23, 70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
B	REV SHTS 01 PER ANI-035	J LIMA 8-11-71			

REISSUED
A Dodds
B AUG 14 '97

Made By	Issue Date	PROCESS	Dwg. No.	Sh. No.
W. WONG Jan 22, '70	Jan 23, 1970	COMPUTER PHOENIX, ARIZ.	Cont. on 1	70A111154 0

GE 20A 7-62

1. UNPACKING

When this module is shipped with a Processor, there is no special unpacking procedure. However, if the module is shipped as an expansion unit, unpack it carefully and check for breakage and damage to components.

2. PHYSICAL CHARACTERISTICS

This module consists of a standard 9-3/4 inch by 10-1/2 inch mother-board and two cables.

3. LOCATION

This mother-board connects to any I/O slot in the Processor or expansion card file.

4. SAFEGUARDS

To prevent damage to personnel or equipment, make sure the AC power is off while installing the module.

5. CABLES

The cable connectors are inserted into locations 40 and 41 of the mother-board. See Table 1 for cable terminations and designations.

The device address of this module is X'11'. This address can be changed by rearranging the position of the wires located at position 20 of the mother-board as shown in Figure 1 and Table 2.

Verify that the strap lead between 214-0 and 114-0 (RACK/TACK jumper) is removed from the wiring side of the Processor or expansion card file on the slot chosen for the module. This allows the necessary Interrupt Receive and Acknowledge signals from the Processor to enter the module.

6. INSTALLATION CHECK

Run Test Program 70A112464 to determine if the sense Line Module is installed correctly and operating properly.

NOTE: If the device address is changed, the test program must also change.

TITLE SENSE LINE MODULE
INSTALLATION SPECIFICATION

FIRST MADE FOR GE-PAC 30 (02-062A20)

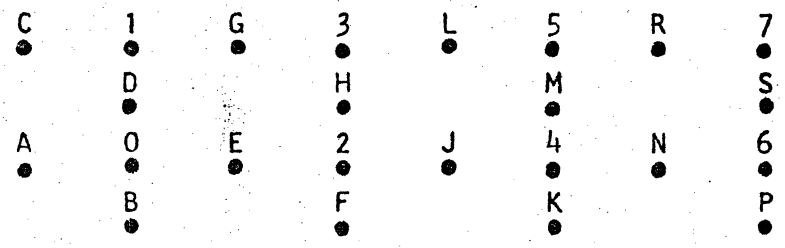
REVISIONS

TABLE 1
CABLE CONNECTION AND DESIGNATION

TERMINAL	DESIGNATION	TERMINAL	DESIGNATION
70-40	S001	51-40	S091
60-40	S011	41-40	S101
50-40	S021	31-40	S111
40-40	S031	21-40	S121
30-40	S041	11-40	S131
20-40	S051	70-41	S141
10-40	S061	71-41	S151
71-40	S071	60-41	EXT INTERRUPT LINE
61-40	S081	61-41	EXT BUSY LINE

Interface Specification

Logical ZERO - 0V ± 0.5V at 1.2 ma
Logical ONE - 5V ± 2V at 0 ma



1. The numbered pins, 0-7, are connected directly to the inputs of the Address NAND gate.

2. The lettered pins denote the level of the signal going to the numbered pins as shown in Table 2.

Figure 1. Physical layout of Address Field on I/O mother-board

PRINTS TO

TABLE 2
DEVICE ADDRESSING

NUMBERED PINS	LETTERED PINS	LEVEL	HEXADECIMAL WEIGHT	EXAMPLES OF DEVICE ADDRESSING	
				X'4C'	X'2B'
0	A B	1 0	8	0 To B	0 To B
1	C D	1 0	4	1 To C	1 To D
2	E F	1 0	2	2 To F	2 To E
3	G H	1 0	1	3 To H	3 To H
4	J K	1 0	8	4 To J	4 To J
5	L M	1 0	4	5 To L	5 To M
6	N P	1 0	2	6 To P	6 To N
7	R S	1 0	1	7 To S	7 To R

0 0 0 1 0 0 0 1

GENERAL ELECTRIC

70A111241

PRINT DIST. K7-21

SENSE LINE MODULE
MAINTENANCE SPECIFICATION

CONT. ON 1 SH. NO. 0
(02-062A21)

GENERAL NOTES

F.C.F.
FMF: GE-PAC 30

APPROVED BY: E. A. [illegible] DATE: Jan. 23, 70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				

REISSUED
A Issue

Made By
W. WONG JAN. 8, 1970

Issue Date
Jan 28, 1970

PROCESS
COMPUTER
PHOENIX, ARIZ.

Dwg. No. 70A111241
Cont. on 1 Sh. No. 0

PCE 20A 7-62

1. INTRODUCTION

The Sense Line Module, Part Number 02-062, provides the means for detecting the status of sixteen sense inputs from external equipment. The data on the sense lines is read into the Processor by two consecutive Read Data Instructions. Each instruction inputs one byte of data from the sense lines.

Provisions are made for user initiated Processor interrupt. The Processor can arm or disarm the interrupt under program control.

2. BLOCK DIAGRAM

The block diagram for the Sense Line Module is shown on FS32, Sheet 5. As shown on the diagram, the user provides sixteen status lines from an external source to the input of the module. Two Read Instructions gate the sense data, one byte at a time, to the Processor via the Data Request Lines, DRL,000 through DRL,070.

3. FUNCTIONAL DIAGRAM ANALYSIS

The functional logic for the Sense Line Module is shown in FS32.

3.1 Addressing Input

When the Processor gates the correct address to the input of this module, it is strapped to present all highs at the input to the Address NAND gate on 1L3 when the desired combination of bits are received on the DAL lines. The gate is enabled and its low output is inverted to present a high B pulse at the S input to the Address flip-flop on 1P2.

ADRS,0 from the Processor is inverted to product ADRS,1. The combination of ADRS,1 and the high B pulse enables the NAND gate on 3E1. The output from the gate causes SYN,0 to be sent to the Processor. ADRS,1 sets the Address flip-flop to produce AD,1.

3.2 Sense Data

The Processor sends DAL,031 to one input of the NAND gate on 4E8. A CMD,0 from the Processor is inverted. The high output from the inverter is ANDed with AD,1 to produce a CMG,0 pulse. This pulse is inverted to place CMG,1 at the other input to the NAND gate on 4E8. The gate is enabled to produce SCLR,0A. This pulse clears the flip-flop on 4F7.

The Processor sends two consecutive Read Data Instructions in

the form of DR,0 pulses. The first DR,0 pulse is inverted and applied to one input of the NAND gate on 3E4. This high is ANDed with AD,1 to product DRG,0. DRG,0 is inverted and a DRG,1 pulse sets the flip-flop on 4F7. Since it is the lagging edge of the pulse that sets the flip-flop, a high is present on one input to the NAND gate at the same time as the high from the 0-side is at the other input. The NAND gate is enabled and the resultant low is inverted to produce GHIGH,1.

The user presents a byte of sense data on Sense Lines, S,001 through S,071. The lines are connected to one input of the NAND gates located on 4A3 through 4G3. GHIGH,1 is applied to the other input to these NAND gates and the data is gated to the Processor via Data Request Lines, FRL,00A through DRL,070A.

When the second Read Instruction is sent from the Processor, DRG,0 is inverted and resets the flip-flop on 4E7. Since the output from the 1-side of the flip-flop is high at the same time DRG,1 is high, the NAND gate on 4H6 is enabled. The resultant low is inverted to produce GLOW,1.

The user presents a second byte of sense data on Sense Lines S,081 through S,151. The lines are connected to one input to the NAND gates on 4G3 through 4H3. GLOW,1 is applied to the other input and the data is gated to the Processor via Data Request Lines. DRL,00A through DRL,070A.

3.3. Busy

A Sense Status Instruction (SS) interrogates the modules busy line. It sends a Status Request (SR,0) pulse to the input of the inverter on 4D3. The high output from the inverter is ANDed with the AD,1 high to produce a SRG,0 pulse. The SRG,0 pulse is inverted and applies SRG,1 at the input to the NAND gate on 4N5. If the module is busy, the user sends a BSY,1 to the other input. The gate is enabled and a low signal is sent to the Processor via Data Request Line, DRL,040A.

3.4 Interrupt

The interrupt is armed by a combination of DAL,011 pulse from the Processor and a CMG,1 pulse. This enables the NAND gate on 4K8 to produce a low EBL,0. This sets the flip-flop on 3P2. Under these conditions, an interrupt pulse from the user on the BASTN,1 input to the NAND gate on 4R8, enables the gate to set the Interrupt Queue flip-flop on 4N7. The ATN,1 level from the flip-flop is inverted to send ATN,0 to

the Processor.

The Processor returns RACK,0 to the module. This pulse is inverted to place a high at the input to the NAND gate on 4H8. Since the other input is high, the gate is enabled to produce ATSYN,0. This pulse is inverted and the resultant ATSYN,1 resets the Interrupt Queue flip-flop.

When the Processor sends a DAL,001 to one input to the NAND gate on 4K9, CMG,1 on the other input enables the gate to produce a low EBL,1. This resets the flip-flop configuration on 4P2, causing a high output. The high is inverted and keeps ATN,1 at ground potential. This inhibits the output of the Interrupt Queue flip-flop. When the Processor sends RACK,0 to the module, it returns TACK,0 as part of the daisy-chain procedure.

3.5 Initialize

When the INITIALIZE pushbutton is depressed, a System Clear (SCLR,0) pulse is applied to the input of the module. The pulse is buffered and is used to clear the Address flip-flop and the flip-flop on 4F7.

4. MNEMONICS LIST

This section provides an alphabetical list of the mnemonics used in the Sense Line Module. A brief description of the mnemonics and a reference to its source on Schematics FS32 are also provided.

MNEMONIC	MEANING	LOCATION
AD,1	Signal from the 1-side of Address flip-flop	1R2
ADRS,0	Address Pulse from Processor	3A1
ATN,0	Attention to the Processor	3A7
ATSYN,0	Attention Synchronization	3K5
B	Signal at S Input to Address flip-flop	1R1
BSATN,1	A High going pulse from the User that Sets the Interrupt Queue flip-flop.	3R4
CMD,0	Command Pulse from Processor	3A2
CMG,0	Command Gated with Device Address	3H2

MNEMONIC	MEANING	LOCATION
DAL,000 through DRL,070	Data Available Lines	1A1 through 1A7
DR,0	Read Instruction From the Processor (RD)	3A4
DRG,0	DR,0 Gated with the Device Address	3H4
DRL,000 through DRL,070	Data Request Lines	2C2 through 2C7
EBL,0	Enables the Interrupt When Low	3P1
GHIGH,1	Gate High Byte to Processor	4M7
GLOW,1	Gate Low Byte to Processor	4M6
RACK,0	Receive Acknowledge	3A8
SCLR,0	System Clear Signal	1A8
SR,0	Status Request from Processor	3A3
SRG,0	Status Request Gated with Device Address	3H3
SYN,0	Synchronization to Processor	3A5
TACK,0	Transmit Acknowledge	3A9

GENERAL ELECTRIC

70A110426

PRINT DIST.		CONT. ON	SH. NO.
K7-12	SENSE LINE MODULE	1 (32-070A12)	0

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: E. A. White DATE: Oct 6, 69

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				

REISSUED

M	A	Issue E									

Made By E. WHITE | Issue Date Oct 14, 1969 | PROCESS COMPUTER PHOENIX, ARIZ. | Dwg. No. 70A110426 Cont. on 1 Sh. No. 0

PCE 20A 7-62

SENSE LINE MODULE

REVISIONS

1.0 General

This module provides a means of detecting the status of 16 external sense line inputs such as switch positions, relay contacts or digital logic levels.

2.0 Operation

The status of the 16 lines are read into a memory location by executing two 'Read Data' instructions to two consecutive bytes of memory. The module contains the steering gates and control to automatically read in the two bytes of the Sense Lines. A signle 'Output Command' instruction resets the control logic.

The module also provides an external interrupt line. An interrupt is generated by an external device which, when acknowledged, will request the program to read in the status of the sense lines. This mode of operation is useful when it is required only to read in the sense lines when there is a change in status.

3.0 Programming Considerations

A strap option provides for any device # between X'00' & X'FF'.
The following instructions will read in the two bytes from the sense lines and store them in a memory location. Assume R1 has been previously loaded with the device number of the module.

```
RD    R1, LOC       GATES EVEN BYTE TO LOC.
RD    R1, LOC + 1   GATES ODD BYTE TO LOC.
```

4.0 Command & Status Structure

Output Command X'80'	Disables interrupt
Output Command X'40'	Enables interrupt
Output Command X'10'	Resets the byte steering logic

If desired, the EXT Busy line may be used to inform the program when the lines are ready to be monitored. Execution of a Sense Status instruction puts the condition of EXT Busy in the Busy bit of the condition code.

5.0 Mechanical Considerations

The Sense Line Module consists of one Mother Board and 2 (DB) cable connectors. The cable connectors are inserted into locations 40 and 41 of the Mother Board. The module may be plugged into any I/O slot in the expansion card file. The strap lead from 21A-0 to 11A-0 should be removed from the wiring side of the slot chosen.

See Table 1 for cable terminations and designations.

PRINTS TO

TABLE 1

TERMINAL	DESIGNATION
70-40	S001
60-40	S011
50-40	S021
40-40	S031
30-40	S041
20-40	S051
10-40	S061
71-40	S071
61-40	S081
51-40	S091
41-40	S101
31-40	S111
21-40	S121
11-40	S131
70-41	S141
71-41	S151
60-41	EXT. INTERRUPT LINE
61-41	EXT. BUSY LINE

Interface Specification

Logical Zero - 0V ± 0.5V at 1.2ma
Logical One - 5V ± 2V at 0ma

GENERAL ELECTRIC

70A110446

PRINT DIST.	PROGRAMMING SPECIFICATION	CONT. ON 1	SH. NO. 0
K7-15	SENSE LINE MODULE		

GENERAL NOTES

F.C.F.
FMF:

APPROVED BY: Lucas A. Pelaez DATE: 12-10-71

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	Issue				

REISSUED

A	Issued										

Made By	Issue Date	PROCESS	Dwg. No.	70A110446
J. Lima/LAP	DEC 16 1971	COMPUTER PHOENIX, ARIZ.	Cont. on 1	Sh. No. 0

PCE 20A 7-62

TITLE PROGRAMMING SPECIFICATION
SENSE LINE MODULE

FIRST MADE FOR GE-PAC 30

REVISIONS

1. INTRODUCTION

The Sense Line module is an interface designed to allow GE-PAC 30 processors to read two bytes of information from a user's external equipment. The meaning of this data depends upon the user's equipment.

Device number X'11' is normally assigned to this device.

2. STATUS AND COMMAND BYTES

Table 1 describes the status and command byte coding for this device.

3. INITIALIZATION

Depressing INITIALIZE on the processor clears a pending interrupt, disables interrupts, and resets the Steering as in Command bit 3.

4. PROGRAMMING CONSIDERATIONS

Two Read Data instructions are used to read the 16 bits of data. The upper 8 bits are read first, then the lower 8 bits..

K7-15

PRINTS TO

Table 1.

Sense Line Module
Status and Command Byte Data

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY*			
COMMAND BYTE	DISABLE	ENABLE		RESET				

*Optional

DISABLE — This command disables the device interrupt (but leaves it armed), thus allowing queuing of interrupts.

ENABLE — This command enables the device to interrupt the Processor.

RESET — This command resets the steering unconditionally so that the next Read samples the upper eight status lines.

BSY — This Status bit may be used to indicate that the external device is ready to have its sense lines read. The use of this status bit is left up to the user. This line is separate from the external interrupt line.

Other bits in the Status and Command bytes are ignored.

GENERAL ELECTRIC

70A110860

PRINT DIST.	SENSE LINE MODULE PRODUCT SPECIFICATION	CONT. ON 1 SH. NO. 0 (02-062 A19)
K7-19	GENERAL NOTES	F.C.F. FMF: GE-PAC 30

APPROVED BY: E. A. White DATE: Sept 19, 69

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
B	REV. SHTS. 1 & 2 PER	P. MILLER			
ENG	AN 6WDW-44-015	JAN 2, '70			
C	REV SHS 1 & 2 PER	P. Russudes			
	A1-095	JULY 27, 1971			

REISSUED
A ISSUE
B Jan 8, 1970
C JUL 20, 1971

Made By E. WHITE | Issue Date Sept 24 1969 | PROCESS COMPUTER PHOENIX, ARIZ. | Dwg. No. 704110860 Cont. on 1 | Sh. No. 0

1. DOCUMENTATION

1.1 Shipped with Product

1 each 70A111241	Maintenance Spec.
1 each 70A111154	Installation Spec.
1 each 70A112464	Test Program.
1 each 70B113242 (FS-32)	Logic Schematic

2. PARTS LIST

Part Number 70A104048 G.70 (02-062) consists of the following:

1 each 32-070	Sense Line Module (MB)
2 each 17-069F04	GP I/O Cables

3. DIMENSIONS

9.75" x 10.5" standard card
Cable Length 12 ft. (open end)

4. WEIGHT

Three pounds including cable

5. POWER

Interface board: +5 volts ± 10% @ .75 amps

6. ENVIRONMENTAL DATA

6.1 Temperature: 0° to 50° C

6.2 Humidity: Equals or exceeds processor

6.3 Vibration: Equals or exceeds processor

7. DESCRIPTION

7.1 The 70A110860 Sense Line Module provides sixteen input sense lines and an externally controlled interrupt line. With the device interrupts enabled a pulse in the external interrupt line will cause a computer interrupt which may be used to initiate the proper subroutine for read in of sense lines, checking, etc.

7.2 The Sense Line Module mother-board may be plugged into any I/O slot.

7.3 The Input Sense Lines are not stored in the interface board. They are gated directly through to the Processor Memory.

8. ACCEPTANCE TEST

The 02-062 Sense Line Module must successfully perform its designated test program 70A112464 in order to be considered operational. The program should run under the prescribed system environmental variations.

GENERAL ELECTRIC
PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
SENSE LINE MODULE

DRAWING NUMBER 70B113242 | CONT OA | PAGE 0
FIRST MADE FOR GE-PAC 30
(FS32)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
D	ISSUED				
E	REV SH OA & 4 PER	J. Morales			
[illegible]	AN 6WDW-44-012	12-2-69			
E1	REV SH 4 PER	C. Ellsworth			
[illegible]	ANGWOW-44-013	DEC. 11, '69			

REISSUED

D	ISSUED
E	Dec. 10, 1969
E1	Dec. 15, 1969

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME

REISSUED

(FS32)

MADE BY J. Cigrand 8 SEPT 69
ISSUED September 11, 1969
APPROVAL E. G. White Sept 9, 69
REV. D

DWG. NO. 70B113242 | CONT. OA | PAGE 0
PRINTS TO: K7-08

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
SENSE LINE MODULE
GE-PAC 30

DWG NO 70B113242
CONT ON SHEET 1 REV NO OA

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	CA	-	2	3	4																
FUNCTIONAL SCHEMATIC	1	1	2	2	2																
	2	1	2	2	2																
	3	1	2	2	2																
	4	1	1	3	4																
BACK PANEL MAP		-	2	2	2																
BLOCK DIAGRAM		1	1	1	1																
ISSUE DATE		4-23-68	12-5-68	3-14-69	8-14-69																

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD SENSE LINE MODULE	32-070

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.
3. IN THE EVENT THAT THE REVISION LEVEL STAMPED ON THE PWB DOES NOT CORRESPOND TO THAT IN THE SUPPORTING INFORMATION TABLE, PLEASE REQUEST SCHEMATIC OF THE CORRECT REVISION LEVEL FROM "GENERAL ELECTRIC CO., 40 FEDERAL STREET, WEST LYNN, MASSACHUSETTS 01905".

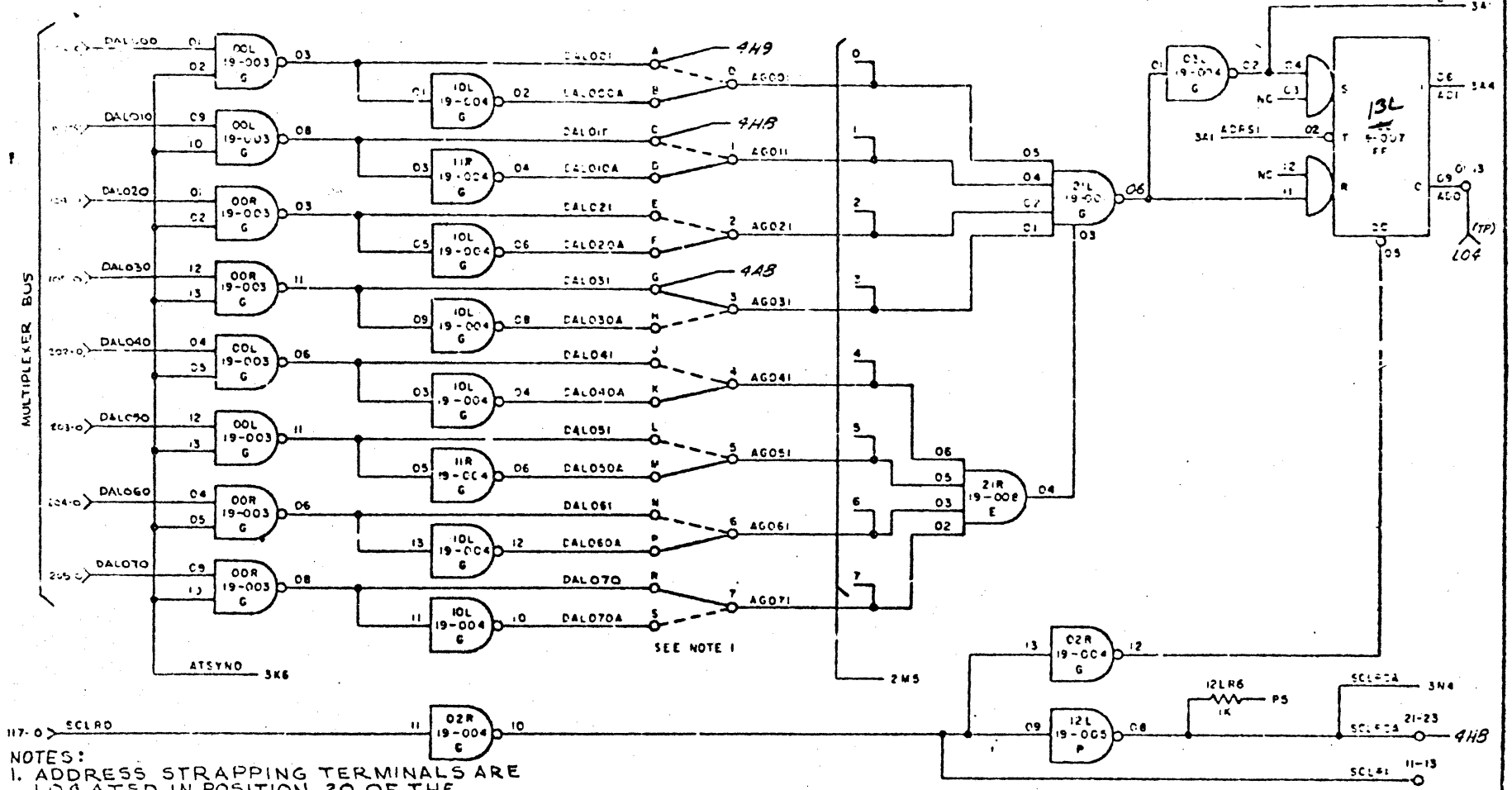
MADE BY [illegible] Sept 11, 1969
APPROVAL [illegible] Sept 9, 69
DES
CHKR
REV. J ISSUED
E

DWG NO (FS 32) 70B113242
CONT ON SHEET 1 REV NO OA

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
SENSE LINE MODULE
FOR GE-PAC 30

70B 3242



NOTES:
1. ADDRESS STRAPPING TERMINALS ARE LOCATED IN POSITION 20 OF THE MOTHER BOARD.

MADE BY	APPROVAL	DES	REV				ENG NO (FS 32)
L.C. Kirby & Sons	E.A. White	CHAR	D	ISSUED			70B 3242
DATED Sept 4, 1969	Sept 4, 69						CONT SHEET 2 SH NO 1

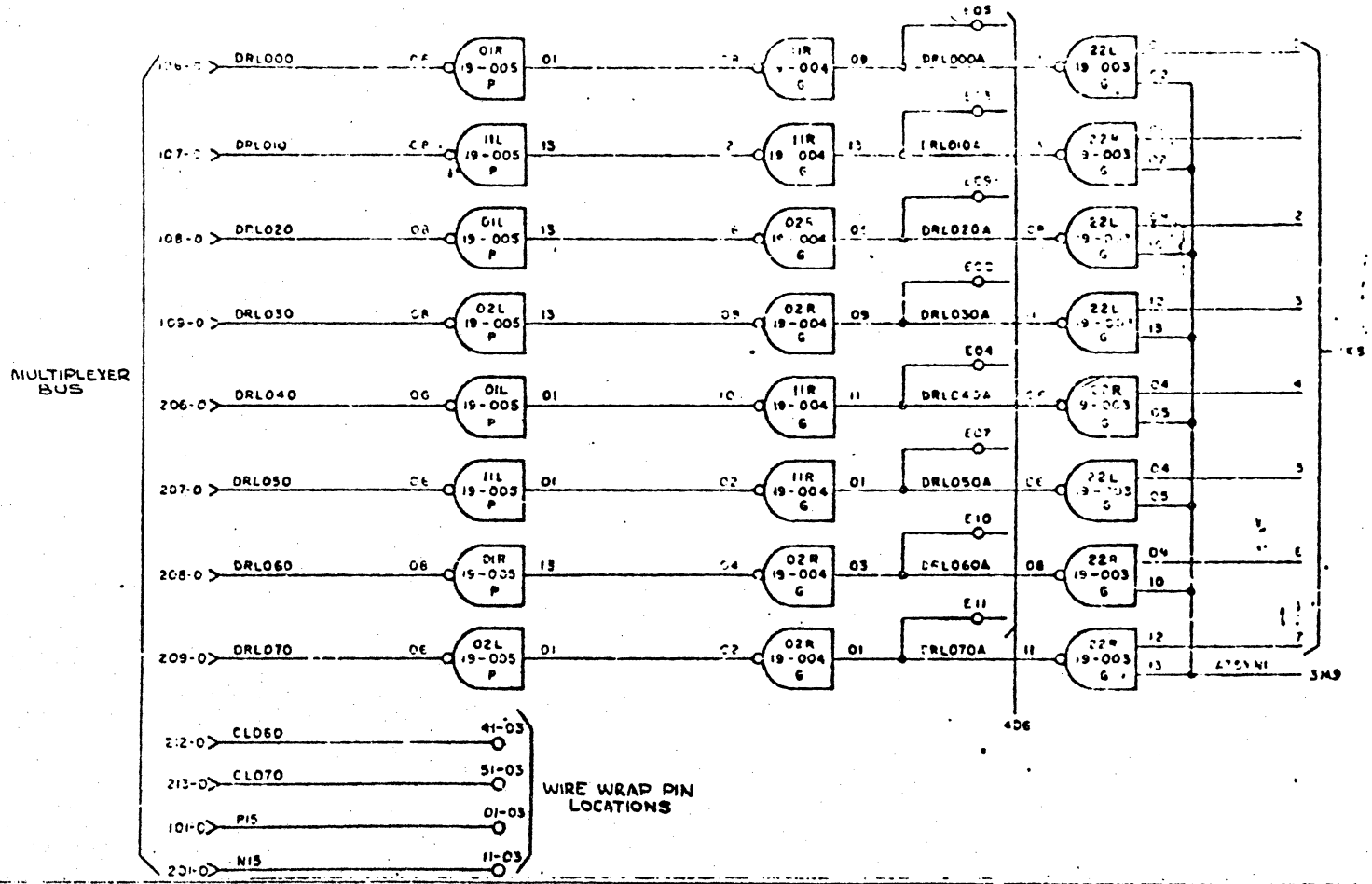
GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
SENSE LINE MODULE
GE-PAC 30

DRG NO (PS 32) 70B113242
SHEET 2 OF 3 REV NO 2

NOTES:

1. CL070 USED FOR POWER FAIL DETECTION OPTION.
   CL060 NOT NORMALLY USED.



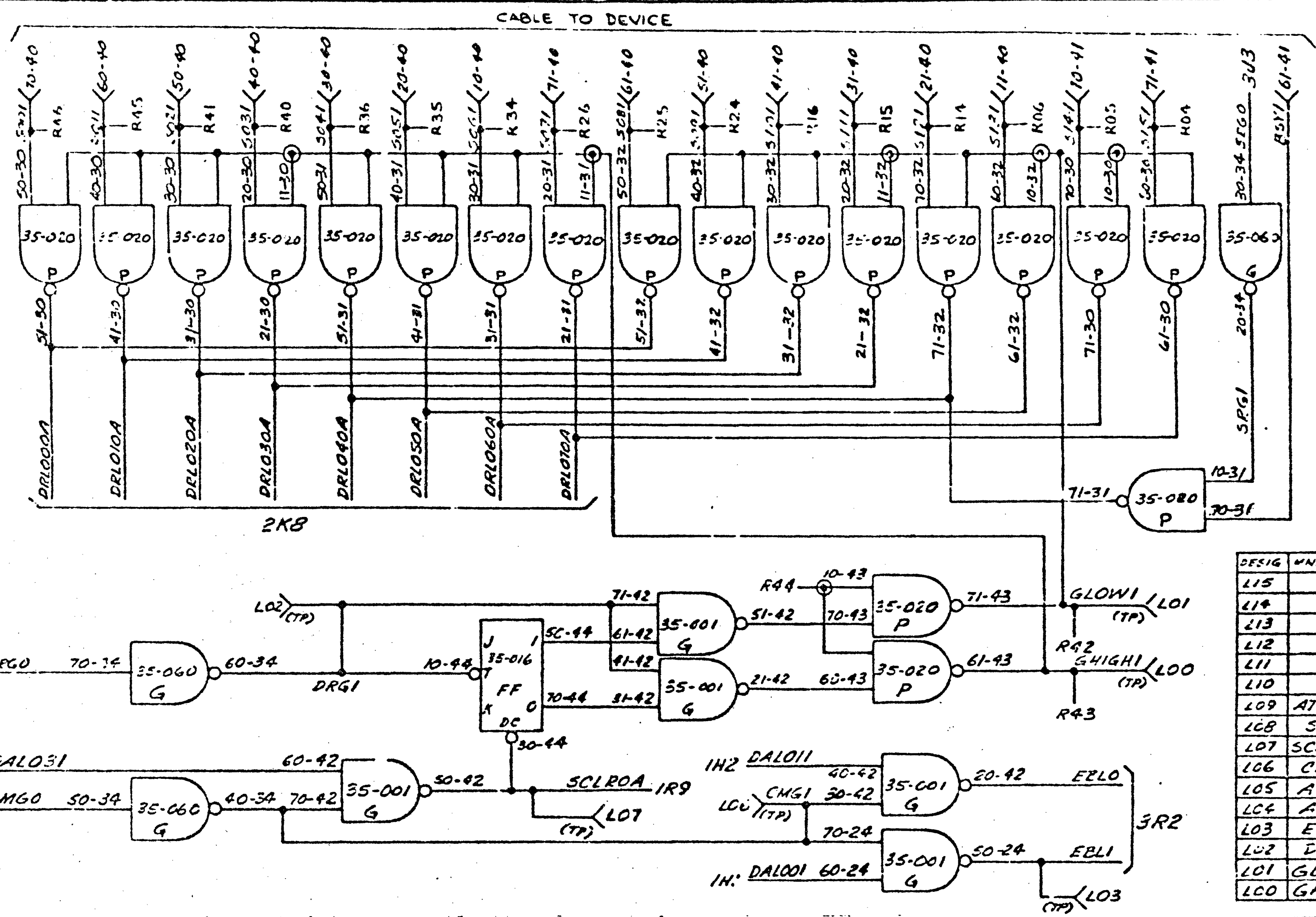
MADE BY	APPROVAL	DES.		REV		ISSUED				DRG NO (PS 32) 70B113242
		CHKR			D					SHEET 3 REV NO 2
DATE Sept 11/1969										

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

FUNCTIONAL SCHEMATIC
SENSE LINE MODULE
GE-PAC 30

DWG NO (FS 32) 70B113242
CONT ON SHEET 5 SH NO 4



DESIG	MNEMONIC	SHT NO.
L15		
L14		
L13		
L12		
L11		
L10		
L09	ATSYN1	3
L08	SRGO	3
L07	SCLROA	4
L06	CMG1	4
L05	ATN1	3
L04	ADO	1
L03	EBL1	4
L02	DRG1	4
L01	GLOW1	4
L00	GHIGH1	4

MADE BY [signature] 4 Sept 1969
ISSUED Sept 11, 1969
APPROVAL [signature]

REV.	
D	ISSUED
E	E1

DWG NO (FS 32) 70B113242
CONT ON SHEET 5 SH NO 4

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING — APPLIED PRACTICES — SURFACES √ — TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS ± — DECIMALS ± — ANGLES ±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE: FUNCTIONAL SCHEMATIC
SENSE LINE MODULE

1ST MADE FOR: GE-PAC 30

DWG NO (FS 32) 7C B113242 — CONT ON SHEET 6 — SH NO 5

BACK PANEL MAP

CONN POS	VERT POS	SENSE LINE MODULE HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1	2	HORIZ POS 0	1
1	22																	
	21																	
	20																	
	19																	
	18																	
	17																	
	16																	
	15																	
	14																	
	13																	
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	09																	
	08																	
	07																	
	06																	
	05																	
	04																	
	03																	
	02																	
	01																	
	00																	
0	22		PS	GND														
	21																	
	20																	
	19																	
	18																	
	17		SCLRO															
	16																	
	15		SYNO	ATNO														
	14		RACKO	TACKO														
	13		SRO	CL070														
	12		DRO	CL060														
	11		DAO															
	10		ADRSO	CMDO														
	09		DRL030	DRL070														
	08		DRL020	DRL060														
	07		DRL010	DRL050														
	06		DRL000	DRL040														
	05		DAL030	DAL070														
	04		DAL020	DAL060														
	03		DAL010	DAL050														
	02		DAL000	DAL040														
	01		FIS	NIS														
	00		PS	GND														

MADE BY: Hal Kirby 4 SEPT 1969 — ISSUED: Sept 11, 1969 — APPROVAL: E. White, Sept 9, 69 — DES. — CHKR

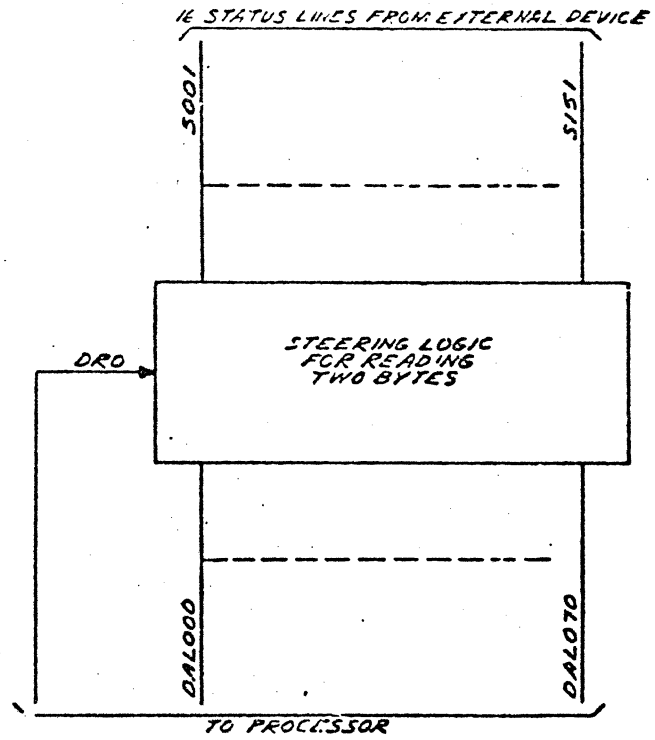
REV. D ISSUED

DWG NO (FS 32) 7C B113242 — CONT ON SHEET 6 — SH NO 5

DIST.	UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING — APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED ELEMENTS: FRACTIONS	DECIMALS	ANGLES	GENERAL ELECTRIC PROCESS COMPUTER PHOENIX	TITLE FUNCTIONAL SCHEMATIC SENSE LINE MODULE FOR GE-PAC 30 1 PCV	DWG NO (FS 32) 70B113242 CONT ON SHEET F SH NO 6
		√	±	±	±			

A B C D E F G H J K L M N P R

1 2 3 4 5 6 7 8 9



MADE BY	APPROVAL			REV.								DWG NO (FS 32) 70B113242
ISSUE Sept 11 1969	E.G. White 9/11/69	DES.			D	ISSUE						CONT ON SHEET F SH NO 6
		CHKR.										

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
SENSE LINE MODULE

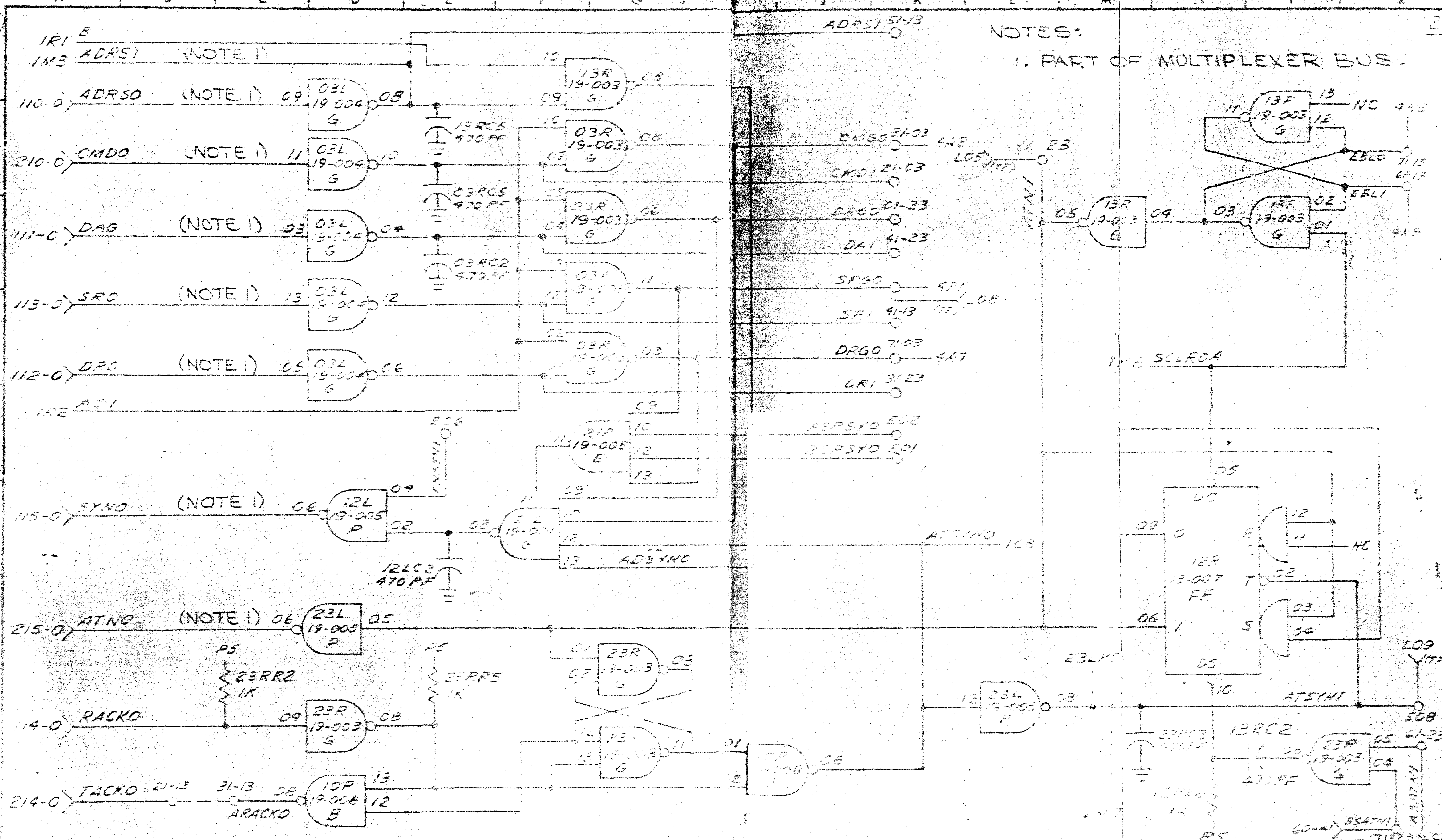
DWG NO (FS 32)
70B113242

FIRST MADE FOR GE-PAC 30

CONT ON SHEET 4

NOTES:

1. PART OF MULTIPLEXER BUS.



DWG NO (FS 32)
70B113242
CONT ON SHEET 4 SH NO 3

APPROVAL
Sept 11, 1969