MSV11-P User Guide

Prepared by Education Services of Digital Equipment Corporation
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1.1 INTRODUCTION
This manual describes the MSV11-P family of memory modules. The MSV11-P memory modules are metal oxide semiconductors (MOS), random access memory (RAM). They are designed to be used with the LSI-11 bus. The MSV11-P provides storage for 18-bit words (16 data bits and 2 parity bits) and also contains parity control circuitry and a control and status register (CSR). There are three versions of the MSV11-P memory modules as shown in Table 1-1.

<table>
<thead>
<tr>
<th>Option Designation</th>
<th>Module Designation</th>
<th>Storage Capacity</th>
<th>MOS Chips</th>
<th>Module Population</th>
<th>Number of Rows</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSV11-PL</td>
<td>M8067-LA</td>
<td>256K words by 18 bit</td>
<td>64K</td>
<td>Full</td>
<td>8</td>
</tr>
<tr>
<td>MSV11-PK</td>
<td>M8067-KA</td>
<td>128K words by 18 bit</td>
<td>64K</td>
<td>Half</td>
<td>4</td>
</tr>
<tr>
<td>MSV11-PF</td>
<td>M8067-FA</td>
<td>64K words by 18 bit</td>
<td>16K</td>
<td>Full</td>
<td>8</td>
</tr>
</tbody>
</table>

1.2 GENERAL DESCRIPTION
The MSV11-P memory module consists of a single, quad-height module (M8067) that contains the LSI-11 bus interface, timing and control logic, refresh circuitry, and a MOS storage array. The module also contains circuitry to generate and check parity, and a control and status register.

The memory module’s starting address can be set on any 8K boundary within the 2048K LSI-11 address space or 128K LSI-11 address space. The MSV11-P allows the top 4K of the LSI-11 address space to be reserved for the I/O peripheral page. Note that there is no address interleaving with the MSV11-P.

The memory storage elements are 16,384 by 1 bit, MOS dynamic RAM devices or 65,536 by 1 bit MOS dynamic RAM devices. The MOS storage array contains 18 of these devices for every 16K rows of memory or 64K rows of memory. Unlike core memory, the read operation for MOS storage devices is nondestructive; consequently the write-after-read operation associated with core memory is eliminated. The MOS storage devices must be refreshed every 14.5 μs so that the data remains valid.
The MSV11-PF memory uses +5 V, +12 V and −5 V. The positive voltages are received from the backplane and the negative voltage is generated from a charge pump circuit on the board. The MSV11-PL and MSV11-PK require +5 V, which is received from the backplane.

There is a green LED on the module that stays on as long as +5 V power is supplied to the logic required for memory refresh, read/write request, arbitration, and row and column addressing.

The control and status register in the MSV11-P contains bits that are used to store the parity error address bits. By setting a bit in the CSR you can force wrong parity. This is a useful diagnostic tool for checking out the parity logic. The CSR has its own address in the top 4K of memory. Bus masters can read or write to the CSR.

The parity control circuitry in the MSV11-P generates parity bits based on data being written into memory during a DATO or DATOB bus cycle. One parity bit is assigned to each data byte and is stored with the data in the MOS storage array. When data is retrieved from memory during DATI or DATIO bus cycles, the parity of the data is determined. If parity is good, the data is assumed correct. If the parity bits do not correspond, the data is assumed unreliable and memory initiates the following action.

1. A red LED on the module lights. This provides a visual indication of a parity error and sets CSR bit 15.

2. If bit 0 in the CSR is set, the memory asserts BDAL 16 and 17. This warns the processor that a parity error has occurred.

3. Part of the address of the faulty data is recorded in the CSR.

1.3 SPECIFICATIONS
This section of the manual gives functional, electrical, and environmental specifications and backplane pin utilization information.

1.3.1 Functional Specifications
Table 1-2 provides MSV11-P functional specifications.

1.3.2 Electrical Specifications
The electrical specifications state the voltage and power requirements for the MSV11-P.

No adjustment or maintenance is required. Two LEDs are used to indicate board status. A green LED indicates that +5 V GR is present on the board. This is useful on battery backed up systems where the boards could be removed from the backplane with only +5 V shut off. A red LED indicates the detection of a parity error.
Table 1-2  Access and Cycle Times*

<table>
<thead>
<tr>
<th>Bus Cycles</th>
<th>Access Time†</th>
<th>Cycle Time‡</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATI</td>
<td>240</td>
<td>650</td>
</tr>
<tr>
<td>DATO(B)</td>
<td>90</td>
<td>610</td>
</tr>
<tr>
<td>DATIO(B)</td>
<td>660</td>
<td>1175</td>
</tr>
<tr>
<td>REFRESH</td>
<td>640</td>
<td>690</td>
</tr>
</tbody>
</table>

* Parity – CSR configurations, refer to notes 1, 8, and 9.
† Tacc (ns)
‡ Tcyc (ns)

NOTE 1:  Assuming memory not busy and no arbitration.

NOTE 2:  SYNCH to RPLYH with minimum times (25/50 ns) from SYNCH to (DINH/DOUTH). The DATO(B) access and cycle times assume a minimum 50 ns from SYNCH to DOUTH inside memory receivers. For actual LSI-11 bus measurements, a constant (K=200 ns) should be added to DATO(B) times, i.e., Tacc (Typical) = 90 + (200 - 50) = 240 ns.

NOTE 3:  SYNCH to RPLYH [DATO(B)] with minimum time (25 ns) from SYNCH to DINH and minimum (350 ns) from RPLYH (DATI) asserted to DOUT asserted.

NOTE 4:  SYNCH to TIM250H negated.

NOTE 5:  SYNCH to TIM250H negated with minimum time (50 ns) from SYNCH to DOUTH.

NOTE 6:  SYNCH to TIM250H [DATO(B)] with minimum times (25 ns) from SYNCH to DINH and minimum (350 ns) from RPLYH (DATI) asserted to DOUT asserted.

NOTE 7:  REF REQ L to TIM250H negated.

NOTE 8:  REFRESH arbitration adds (90 ns) typical and (110 ns) maximum to access.

NOTE 9:  REFRESH conflict adds (640 ns) typical and (690 ns) maximum to access and cycle times.

1.3.2.1 Voltages – The MSV11-PF memory modules require +5 V, +12 V, and −5 V for the multivoltage MOS RAMs. The −5 V is generated from the memory module. Single voltage MOS RAMs (MSV11-PK/PL) require only +5 V. Voltage margins for the +5 V and +12 V are ±5 percent (Table 1-3).

NOTE:  Latest MSI available and in use at DIGITAL will be used for control.

1.3.2.2 Power Requirements – Power requirements are provided in Table 1-4.

1.3.3 Environmental Specifications
Environmental specifications cover storage and operating temperature, relative humidity, altitude, and air flow specifications.
Table 1-3  Multi/Single Voltage MOS RAM

Multivoltage MOS RAMs (MSV11-PF)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Pins</th>
<th>Service</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non Battery Backed Up</td>
<td>+5 V</td>
<td>AA2, BA2, BV1, CA2</td>
</tr>
<tr>
<td></td>
<td>+12 V</td>
<td>AD2, BD2</td>
</tr>
<tr>
<td></td>
<td>+5 V</td>
<td>AA2, BA2, BV1, CA2</td>
</tr>
<tr>
<td>Battery</td>
<td>+5 V BBU</td>
<td>AV1, AE1</td>
</tr>
<tr>
<td>Backed Up</td>
<td>+12 V BBU</td>
<td>AS1</td>
</tr>
</tbody>
</table>

Single Voltage MOS RAMs (MSV11-PK/PL)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Pins</th>
<th>Service</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non Battery Backed Up</td>
<td>+5 V</td>
<td>AA2, BA2, BV1, CA2</td>
</tr>
<tr>
<td></td>
<td>+5 V (VDD)</td>
<td>DA2</td>
</tr>
<tr>
<td>Battery</td>
<td>+5 V</td>
<td>AA2, BA2, BV1, CA2</td>
</tr>
<tr>
<td>Backed Up</td>
<td>+5 V</td>
<td>AV1, AE1</td>
</tr>
</tbody>
</table>

* For systems without +5 V on DA2, +5 V can be supplied from AA2, BA2, BV1, and CA2.

1.3.3.1 Temperature – Temperature is separated into the following two groups.

1. Operating Temperature Range – The operating temperature range is +5 °C to +60 °C. Lower the maximum operating temperature by 1 °C for every 1000 feet of altitude above 8000 feet.

2. Storage Temperature Range – The storage temperature range is −40 °C to +66 °C. Do not operate a module that has been stored outside the operating temperature range. Bring the module to an environment within the operating range and allow at least five minutes for the module to stabilize.

1.3.3.2 Relative Humidity – The relative humidity for the MSV11-P memory modules must be 10 percent to 90 percent noncondensing for storage or operating conditions.

1.3.3.3 Operating Airflow – Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module to 5 °C when the inlet temperature is +60 °C. For operation below +55 °C, airflow must be provided to limit the inlet to outlet temperature rise across the module to 10 °C maximum.
### Table 1-4 MSV11-P Power

**MSV11-PF (Multivoltage MOS RAMs)**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Standby Current (A)</th>
<th>Active Current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Meas Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+5 V Noncritical</td>
<td>1.40</td>
<td>2.21</td>
</tr>
<tr>
<td>+5 V BBU</td>
<td>1.15</td>
<td>1.55</td>
</tr>
<tr>
<td>Total +5 V</td>
<td>2.55</td>
<td>3.76</td>
</tr>
<tr>
<td>+12 V</td>
<td>0.10</td>
<td>0.12</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Standby Power (W)</th>
<th>Active Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Meas Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+5 V Noncritical</td>
<td>7.00</td>
<td>11.60</td>
</tr>
<tr>
<td>+5 V BBU</td>
<td>5.75</td>
<td>8.14</td>
</tr>
<tr>
<td>Total +5 V</td>
<td>12.75</td>
<td>19.74</td>
</tr>
<tr>
<td>+12 V</td>
<td>1.20</td>
<td>1.51</td>
</tr>
<tr>
<td>Total Power</td>
<td>13.95</td>
<td>21.25</td>
</tr>
</tbody>
</table>

**MSV11-PK (Single Voltage, Half Populated)**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Standby Current (A)</th>
<th>Active Current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Meas Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+5 V Noncritical</td>
<td>1.65</td>
<td>2.10</td>
</tr>
<tr>
<td>+5 V BBU</td>
<td>1.35</td>
<td>1.80</td>
</tr>
<tr>
<td>Total +5 V</td>
<td>3.00</td>
<td>3.90</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Standby Power (W)</th>
<th>Active Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Meas Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+5 V Noncritical</td>
<td>8.25</td>
<td>11.00</td>
</tr>
<tr>
<td>+5 V BBU</td>
<td>6.75</td>
<td>9.45</td>
</tr>
<tr>
<td>Total Power</td>
<td>15.0</td>
<td>20.45</td>
</tr>
</tbody>
</table>

**MSV11-PL (Single Voltage, Fully Populated)**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Standby Current (A)</th>
<th>Active Current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Meas Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+5 V Noncritical</td>
<td>1.65</td>
<td>2.10</td>
</tr>
<tr>
<td>+5 V BBU</td>
<td>1.45</td>
<td>1.90</td>
</tr>
<tr>
<td>Total +5 V</td>
<td>3.10</td>
<td>4.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Standby Power (W)</th>
<th>Standby Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Meas Typ</td>
<td>Max</td>
</tr>
<tr>
<td>+5 V Noncritical</td>
<td>8.25</td>
<td>11.0</td>
</tr>
<tr>
<td>+5 V BBU</td>
<td>7.25</td>
<td>10.0</td>
</tr>
<tr>
<td>Total +5 V</td>
<td>15.5</td>
<td>21.0</td>
</tr>
</tbody>
</table>

**NOTE:** Typical power calculations are done at nominal voltages. Maximum power calculations are done with maximum currents at the highest voltage (nominal +5 percent).
1.3.3.4 Altitude – The module resists mechanical or electrical damage at altitudes up to 50,000 feet (90 MM mercury) under storage or operating conditions.

*NOTE:* Lower the maximum operating temperature by $1^\circ$ C for every 1000 feet of altitude above 8000 feet.

1.3.4 Refresh
The MSV11-P memory module uses a self-contained refresh rate that is typically 650 ns every 14,500 ns. The refresh overhead maximum is 685 ns/13,500 ns or about 5 percent.

1.3.5 Diagnostics
The diagnostics are CVMSAA (22-bit system) and CZKMAA (18-bit system).

1.3.6 Backplane Pin Utilization
MSV11-P backplane pin utilization is shown in Table 1-5. Blank spaces indicate pins not used.

<table>
<thead>
<tr>
<th>Table 1-5 Backplane Pin Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A Connector</strong></td>
</tr>
<tr>
<td><strong>Pin</strong></td>
</tr>
<tr>
<td>A</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>D</td>
</tr>
<tr>
<td>E</td>
</tr>
<tr>
<td>F</td>
</tr>
<tr>
<td>H</td>
</tr>
<tr>
<td>J</td>
</tr>
<tr>
<td>K</td>
</tr>
<tr>
<td>L</td>
</tr>
<tr>
<td>M</td>
</tr>
<tr>
<td>N</td>
</tr>
<tr>
<td>P</td>
</tr>
<tr>
<td>R</td>
</tr>
<tr>
<td>S</td>
</tr>
<tr>
<td>T</td>
</tr>
<tr>
<td>U</td>
</tr>
<tr>
<td>V</td>
</tr>
</tbody>
</table>

* Must be hardwired on backplane or damage to MOS devices may result.
† Hardwired via etch on module.
‡ Jumpered on module.
§ When SA16K (starting address 16K) jumper is removed, there is no connection to this pin (used in memory test only).
1.4 RELATED DOCUMENTS
Refer to the following documents for more information.

- Field Maintenance Printset (MP01239)
- Microcomputer and Memory Handbook (EB-18451-20)
- Microcomputer Interface Handbook (EB-20175-20)
- LSI-11 System Service Manual (EK-LSI-FS-SV)*

These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

ATTN: Communications Services (NR2/M15)
Customer Services Section

*Field Service Use Only
2.1 GENERAL
This chapter contains information for configuring and installing the MSV11-P family of memory modules. This includes the M8067-LA, M8067-KA, and M8067-FA.

The fully populated module, M8067-LA, has 512K bytes. The half populated module, M8067-KA, has 256K bytes. Both modules use 64K bit chips. The M8067-FA module has 128K bytes of memory. This is a fully populated module using 16K bit chips.

Installation includes the following procedures.

- Wire wrap guidelines
- Jumpers configuration

CAUTION
1. You must remove dc power from the backplane during module insertion or removal.

2. You must install memories in sequential slots following the CPU.

3. Be careful when replacing the memory module. Make sure that the component side of the module faces in the same direction as the other modules in the LSI-11 system. The memory module, backplane, or both can be damaged if the module is installed backwards.

2.2 WIRE WRAP GUIDELINES
A pin can have no more than two wire wraps. The starting address and control and status register (CSR) address pins may require two wire wraps. Always follow this procedure to wire wrap these pins.

1. Find out how many pins must be wrapped.

2. Each wrap must be daisy chained to its own ground.

3. Always put lower wraps on the pins first and then the upper wraps.
2.3 CONFIGURING THE MSV11-P

The jumpers on the MSV11-P memory module are divided into the following five groups.

- Starting Address Jumpers
- CSR Address Jumpers
- Power Jumpers
- Bus Grant Continuity Jumpers
- General Jumpers

Figure 2-1 shows the location of the five jumper groups, four of which are enclosed in solid boxes and labeled. The remaining jumpers are classified as general jumpers. The general jumpers are enclosed in dotted boxes. Table 2-1 shows all the jumpers and their function.

2.3.1 Configuring the Module Starting Address

Each MSV11-P memory module installed in a system is jumpered for its own starting address. To configure the starting address, perform the following steps.

1. Determine the starting address.
2. Determine the pins to be jumpered for the starting address.
3. Wire wrap the pins for the starting address.

2.3.1.1 Determining Starting Address – The memory module starting address can be found if you know how much memory the system has before the replacement module. Change the byte value (how much memory the system has) to a word value. This word value is the module starting address (MSA).

2.3.1.2 Determining Pins to be Jumpered – Module starting address jumpers consist of the following two groups:

1. First Address of the Range (FAR) – Selects the first 256K word range address that the starting address falls in (Table 2-2, Part 1).
2. Partial Starting Address (PSA) – Selects which 8K boundary within a specific multiple of 256K words the starting address falls in (Table 2-2, Part 2).

At this point you know your module starting address (MSA) and you must find the FAR and PSA values. This is done in the following way.

1. Find the FAR value – This is done by looking at Table 2-2, Part 1 and locating the address range the MSA falls in. The FAR value is the first address of the selected address range. Associated with the FAR value is a specific configuration of jumper pins (X, W, and V) that use jumper pin Y (a ground pin).
2. Find the PSA value - This is done by inserting the MSA and FAR values into the equation \( PSA = MSA - FAR \). After you do the subtraction, find Table 2-2, Part 2 and locate the PSA value. Associated with the PSA is a specific configuration of jumper pins (P, N, M, L, and T) that use jumper pin R (a ground pin). Examples 1 and 2 show how to use the equation to jumper a module.
## Table 2-1  MSV11-P Jumper Check List

<table>
<thead>
<tr>
<th>Jumper Name or Pin to Pin</th>
<th>Jumper In</th>
<th>Jumper Out</th>
<th>Wire Wrap</th>
<th>Solder</th>
<th>Check</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 to 7</td>
<td>X</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>In – write wrong parity</td>
</tr>
<tr>
<td>8 to 7</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>In – disables wrong parity</td>
</tr>
<tr>
<td>2 to Y</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>2 to Y out – 22 bit machine 2 to Y in – 18 bit machine</td>
</tr>
<tr>
<td>43 to 44</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Single voltage MOS RAM access time (150 ns device)</td>
</tr>
<tr>
<td>45 to 44</td>
<td>X</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Multiple voltage MOS RAM access time (200 ns device)</td>
</tr>
<tr>
<td>22 to 23</td>
<td>X</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Not used</td>
</tr>
<tr>
<td>21 to 23</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Not used</td>
</tr>
<tr>
<td>F to H</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>F to H in – connected to force starting address to 16K F to H out – disables force function</td>
</tr>
<tr>
<td>3 to 9</td>
<td>X</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>3 to 9 in – connected on 16K and 64K MOS chip</td>
</tr>
<tr>
<td>13 to 15</td>
<td>X</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Connected on 16K and 64K MOS chip</td>
</tr>
<tr>
<td>4 to 10</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Connected only on 64K MOS chip</td>
</tr>
<tr>
<td>14 to 16</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Connected only on 64K MOS chip</td>
</tr>
<tr>
<td>W3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>Power for 16K chips, jumpers are in</td>
</tr>
<tr>
<td>W11</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>Power for 64K chips, jumpers are in</td>
</tr>
<tr>
<td>W13</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>W4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>Power for 64K chips, jumpers are in</td>
</tr>
<tr>
<td>W5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>W9</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>W13</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>W15</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>W1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>Bus grant continuity</td>
</tr>
<tr>
<td>W2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>CSR address</td>
</tr>
<tr>
<td>B</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td>Starting address</td>
</tr>
<tr>
<td>W</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>V</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>-</td>
<td>-</td>
<td>X</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>
**Table 2-2 Starting Address Configurations (Part 1)**

<table>
<thead>
<tr>
<th>First Address Ranges (FAR)</th>
<th>Jumpers to Ground (Pin Y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decimal K Words</td>
<td>Octal K Words</td>
</tr>
<tr>
<td>000 - 248</td>
<td>0000 0000 - 0174 0000</td>
</tr>
<tr>
<td>256 - 504</td>
<td>0200 0000 - 0374 0000</td>
</tr>
<tr>
<td>512 - 760</td>
<td>0400 0000 - 0574 0000</td>
</tr>
<tr>
<td>768 - 1016</td>
<td>0600 0000 - 0774 0000</td>
</tr>
<tr>
<td>1024 - 1272</td>
<td>1000 0000 - 1174 0000</td>
</tr>
<tr>
<td>1280 - 1528</td>
<td>1200 0000 - 1374 0000</td>
</tr>
<tr>
<td>1526 - 1784</td>
<td>1400 0000 - 1574 0000</td>
</tr>
<tr>
<td>1742 - 2040</td>
<td>1600 0000 - 1774 0000</td>
</tr>
</tbody>
</table>

**Table 2-2 Starting Address Configurations (Part 2)**

<table>
<thead>
<tr>
<th>Partial Starting Address (PSA)</th>
<th>Jumpers to Ground (Pin R)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000 0000</td>
</tr>
<tr>
<td>8</td>
<td>0004 0000</td>
</tr>
<tr>
<td>16</td>
<td>0010 0000</td>
</tr>
<tr>
<td>24</td>
<td>0014 0000</td>
</tr>
<tr>
<td>32</td>
<td>0020 0000</td>
</tr>
<tr>
<td>40</td>
<td>0024 0000</td>
</tr>
<tr>
<td>48</td>
<td>0030 0000</td>
</tr>
<tr>
<td>56</td>
<td>0034 0000</td>
</tr>
<tr>
<td>64</td>
<td>0040 0000</td>
</tr>
<tr>
<td>72</td>
<td>0044 0000</td>
</tr>
<tr>
<td>80</td>
<td>0050 0000</td>
</tr>
<tr>
<td>88</td>
<td>0054 0000</td>
</tr>
<tr>
<td>96</td>
<td>0060 0000</td>
</tr>
<tr>
<td>104</td>
<td>0064 0000</td>
</tr>
<tr>
<td>112</td>
<td>0070 0000</td>
</tr>
<tr>
<td>120</td>
<td>0074 0000</td>
</tr>
<tr>
<td>128</td>
<td>0100 0000</td>
</tr>
<tr>
<td>136</td>
<td>0104 0000</td>
</tr>
<tr>
<td>144</td>
<td>0110 0000</td>
</tr>
<tr>
<td>156</td>
<td>0114 0000</td>
</tr>
<tr>
<td>160</td>
<td>0120 0000</td>
</tr>
<tr>
<td>168</td>
<td>0124 0000</td>
</tr>
<tr>
<td>176</td>
<td>0130 0000</td>
</tr>
<tr>
<td>184</td>
<td>0134 0000</td>
</tr>
<tr>
<td>192</td>
<td>0140 0000</td>
</tr>
<tr>
<td>200</td>
<td>0144 0000</td>
</tr>
<tr>
<td>208</td>
<td>0150 0000</td>
</tr>
<tr>
<td>216</td>
<td>0154 0000</td>
</tr>
<tr>
<td>224</td>
<td>0160 0000</td>
</tr>
<tr>
<td>232</td>
<td>0164 0000</td>
</tr>
<tr>
<td>240</td>
<td>0170 0000</td>
</tr>
<tr>
<td>248</td>
<td>0174 0000</td>
</tr>
</tbody>
</table>
Example 1

The system has 512K bytes of memory. To jumper the memory module, change this byte value (512K) to a word value (256K). This word value is called the MSA.

Insert this value into the equation.

\[
\text{PSA} = \text{MSA} - \text{FAR} \\
\text{PSA} = 256K - \text{FAR}
\]

To find the value of FAR use Table 2-2, Part 1 to locate the address range that the MSA value falls in. Take the first address of the address range and insert it into the equation.

\[
\text{PSA} = \text{MSA} - \text{FAR} \\
\text{PSA} = 256K - 256K \\
\text{PSA} = 0
\]

Use Table 2-2, Part 1 - The FAR value equals 256K, this means wire wrap pins V to Y.

Use Table 2-2, Part 2 - The PSA value equals 0K, this means no wire wraps on pins P, N, M, L, and T.

Example 2

The system has 672K bytes of memory. To jumper the memory module, change this byte value (672K) to a word value (336K). This word value is called the MSA.

Insert this value into the equation.

\[
\text{PSA} = \text{MSA} - \text{FAR} \\
\text{PSA} = 336K - \text{FAR} \\
\text{PSA} = 336K - 256K \\
\text{PSA} = 80K
\]

Use Table 2-2, Part 1 - The FAR value equals 256K, this means wire wrap pins V to Y.

Use Table 2-2, Part 2 - The PSA value equals 80K, this means wire wrap pins L to N and N to R.

2.3.1.3 Wire Wrap Pins for the Starting Address - Wire wrap the pins according to the wire wrap procedures in Paragraph 2.2.

2.3.2 Control and Status Register (CSR) Jumpers
Each MSV 11-P memory module has a control and status register. The bus master can read or write the CSR via the LSI-11 bus. The CSR is a 16-bit register whose address falls in the top 4K of system address space.
Each MSV11-P CSR is assigned to one of the 16 addresses shown in Table 2-3. CSR addresses are assigned as follows.

1. Find out how many memory modules in your system have CSR registers.

2. List the memory modules sequential postion from the CPU.

3. The memory modules closest to the CPU have the lower module starting address (MSA).

4. The memory module with the lowest MSA is assigned to the lowest CSR address and jumpered according to Table 2-3.

5. The next sequential CSR memory module is assigned the next higher CSR address.

Each memory module has four CSR jumper pins (A, B, C, and D) which can be daisy chained to pin E (the ground pin). The jumpers allow logic to detect a specific CSR address that has been assigned to a CSR memory module.

For example, assume the system has two memory modules with CSR registers. You are installing the third CSR memory. Refer to Table 2-3 and find the column labeled module number three. The CSR jumper pin configuration is pin B wire wrapped to pin E. The memory module’s CSR address is 17772104 for large systems or 772104 for small systems.

Table 2-3 CSR Address Selection

<table>
<thead>
<tr>
<th>Module Number</th>
<th>Large System LSI-11 Bus Address</th>
<th>Small System LSI-11 Bus Address</th>
<th>Jumper to Ground (Pin E)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1777 2100</td>
<td>7721 00</td>
<td>out out out out</td>
</tr>
<tr>
<td>2</td>
<td>1777 2102</td>
<td>7721 02</td>
<td>out out out in</td>
</tr>
<tr>
<td>3</td>
<td>1777 2104</td>
<td>7721 04</td>
<td>out out in out</td>
</tr>
<tr>
<td>4</td>
<td>1777 2106</td>
<td>7721 06</td>
<td>out in out in</td>
</tr>
<tr>
<td>5</td>
<td>1777 2110</td>
<td>7721 10</td>
<td>out in out out</td>
</tr>
<tr>
<td>6</td>
<td>1777 2112</td>
<td>7721 12</td>
<td>out in in out</td>
</tr>
<tr>
<td>7</td>
<td>1777 2114</td>
<td>7721 14</td>
<td>out in in out</td>
</tr>
<tr>
<td>8</td>
<td>1777 2116</td>
<td>7721 16</td>
<td>out in in in</td>
</tr>
<tr>
<td>9</td>
<td>1777 2120</td>
<td>7721 20</td>
<td>in out out out</td>
</tr>
<tr>
<td>10</td>
<td>1777 2122</td>
<td>7721 22</td>
<td>in out out in</td>
</tr>
<tr>
<td>11</td>
<td>1777 2124</td>
<td>7721 24</td>
<td>in out in out</td>
</tr>
<tr>
<td>12</td>
<td>1777 2126</td>
<td>7721 26</td>
<td>in out in in</td>
</tr>
<tr>
<td>13</td>
<td>1777 2130</td>
<td>7721 30</td>
<td>in in out out</td>
</tr>
<tr>
<td>14</td>
<td>1777 2132</td>
<td>7721 32</td>
<td>in in out in</td>
</tr>
<tr>
<td>15</td>
<td>1777 2134</td>
<td>7721 34</td>
<td>in in in out</td>
</tr>
<tr>
<td>16</td>
<td>1777 2136</td>
<td>7721 36</td>
<td>in in in in</td>
</tr>
</tbody>
</table>
2.3.3 Power Jumpers (Table 2-4)
The power jumpers are divided into the following two groups.

1. 16K multiple voltage devices (M8067-FA) with or without battery backup

2. 64K single voltage devices (M8067-LA and M8067-KA) with or without battery backup

NOTE: DIGITAL does not support battery backup.

Figure 2-1 shows all the possible power configurations. Figures 2-2 through 2-5 show the jumper conditions for 16K/64K devices (MOS memory chips), and the dual functions of pin 9, address or data.

2.3.4 Bus Grant Continuity Jumpers
To install W1 and W2 in your system, identify the backplane and refer to Table 2-5 for the W1 and W2 configuration.

2.3.5 General Jumpers
The general jumper group is the catchall section. All jumpers and their functions that have not yet been covered are described in Table 2-6.

Table 2-4 Power Jumpers

<table>
<thead>
<tr>
<th>16K Multiple Voltage Devices</th>
<th>Non-bat Backup</th>
<th>Bat Backup</th>
<th>Voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>W3</td>
<td>W11</td>
<td>W13</td>
</tr>
<tr>
<td>Non-bat Backup</td>
<td>W3</td>
<td>W10</td>
<td>W12</td>
</tr>
<tr>
<td>Bat Backup</td>
<td>W4</td>
<td>W5</td>
<td>W9</td>
</tr>
<tr>
<td>Voltages</td>
<td>-5</td>
<td>+12 VDD</td>
<td>+5 CR</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>64K Single Voltage Devices</th>
<th>Non-bat Backup</th>
<th>Bat Backup</th>
<th>Voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>W4</td>
<td>W5</td>
<td>W9</td>
</tr>
<tr>
<td></td>
<td>W13/W15</td>
<td>W14</td>
<td>+5 VDD</td>
</tr>
</tbody>
</table>
Figure 2-2  Triple Voltage MOS RAM without Battery Backup

Figure 2-3  Triple Voltage MOS RAM with Battery Backup
Figure 2-4  Single Voltage MOS RAM without Battery Backup

Figure 2-5  Single Voltage MOS RAM with Battery Backup
Table 2-5  Bus Grant Continuity

<table>
<thead>
<tr>
<th>Backplane</th>
<th>Machine Type</th>
<th>W1</th>
<th>W2</th>
</tr>
</thead>
<tbody>
<tr>
<td>H9270 (4 slot backplane)</td>
<td>Q/Q</td>
<td>in</td>
<td>in</td>
</tr>
<tr>
<td>H9275 (9 slot backplane)</td>
<td>Q22/Q22</td>
<td>in</td>
<td>in</td>
</tr>
<tr>
<td>H9273 (4 slot backplane)</td>
<td>Q/CD</td>
<td>out</td>
<td>out</td>
</tr>
<tr>
<td>H9276 (9 slot backplane)</td>
<td>Q22/CD</td>
<td>out</td>
<td>out</td>
</tr>
</tbody>
</table>

Table 2-6  General Jumpers

<table>
<thead>
<tr>
<th>Pin Numbers</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 to 7</td>
<td>In – write wrong parity</td>
</tr>
<tr>
<td>8 to 7</td>
<td>In – disables wrong parity</td>
</tr>
<tr>
<td>2 to Y</td>
<td>2 to Y out – 22 bit machine</td>
</tr>
<tr>
<td></td>
<td>2 to Y in – 18 bit machine</td>
</tr>
<tr>
<td>43 to 44</td>
<td>In – single voltage MOS RAM access time (150 ns device)</td>
</tr>
<tr>
<td>45 to 44</td>
<td>In – multiple voltage MOS RAM access time (200 ns device)</td>
</tr>
<tr>
<td>22 to 23</td>
<td>Not used</td>
</tr>
<tr>
<td>21 to 23</td>
<td>Not used</td>
</tr>
<tr>
<td>F to H</td>
<td>F to H in – connected to force starting address to 16K</td>
</tr>
<tr>
<td></td>
<td>F to H out – disables force function</td>
</tr>
<tr>
<td>3 to 9</td>
<td>3 to 9 in – connected on 16K and 64K MOS chip</td>
</tr>
<tr>
<td>13 to 15</td>
<td>Connected on 16K and 64K MOS chip</td>
</tr>
<tr>
<td>4 to 10</td>
<td>Connected only on 64K MOS chip</td>
</tr>
<tr>
<td>14 to 16</td>
<td>Connected only on 64K MOS chip</td>
</tr>
</tbody>
</table>
3.1 INTRODUCTION
The MSV11-P memory modules interface with the LSI-11 bus. The CPU and DMA devices can become bus master of the LSI-11 bus to transfer or obtain data from memory. The memory is always a slave to whatever device becomes bus master. Figure 3-1 shows the CPU and DMA devices connected to memory via the LSI-11 bus.

Devices that are ready to use the LSI-11 bus must gain control of the bus through the arbitration that takes place in the CPU. The device that wins the arbitration is able to use the bus as soon as bus signals BSYNC and BRPLY are negated. This device is now bus master and can initiate a bus cycle. The types of bus cycles that can be performed are shown in Table 3-1.

![Figure 3-1 Typical System](image)

Table 3-1 Summary of Bus Cycles

<table>
<thead>
<tr>
<th>Bus Cycle Mnemonics</th>
<th>Description</th>
<th>Function with Respect to Bus Master</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATI</td>
<td>Data word input</td>
<td>Read word</td>
</tr>
<tr>
<td>DATO</td>
<td>Data word output</td>
<td>Write word</td>
</tr>
<tr>
<td>DATOB</td>
<td>Data byte output</td>
<td>Write byte</td>
</tr>
<tr>
<td>DATIO</td>
<td>Data word input/output</td>
<td>Read word, modify, write word</td>
</tr>
<tr>
<td>DATIOB</td>
<td>Data word input/byte output</td>
<td>Read word, modify, write byte</td>
</tr>
</tbody>
</table>
All bus cycles are divided into three sequential events.

- Address cycle
- Data cycle
- Bus cycle termination

3.2 LSI-11 BUS SIGNALS AND DEFINITIONS

In order for the bus master to transfer data, it must generate the signals shown in Figure 3-2. The slave device (memory) receives the signals and initiates BRPLY. This starts a chain reaction to terminate the bus cycle. Table 3-2 gives the signal names and definitions of the bus signals. Appendix A contains the flow diagram and signal sequences for DATO(B), DATI, and DATIO(B).

![Figure 3-2 MSV11-P Memory Interface](image)

**Table 3-2 LSI-11 Bus Signals and Definitions**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Cycle</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Data Address Lines (BDAL 21-00 L)</td>
<td>Address</td>
<td>BDAL 21–00 L is received and decoded as an address by the slave (memory).</td>
</tr>
<tr>
<td></td>
<td>Data write</td>
<td>When the bus master does a memory write, DATO(B) or DATIO(B), the data is transferred on BDAL 15–00 L.</td>
</tr>
<tr>
<td></td>
<td>Data read</td>
<td>The bus master receives data on BDAL 15–00 L. The validity of the data is noted by the condition of BDAL 16 and 17. If BDAL 16 and 17 are active then the data on BDAL 15–00 L is bad. If BDAL 16 and 17 are not active, then the data on BDAL 15–00 L is good.</td>
</tr>
</tbody>
</table>
### Table 3-2 LSI-11 Bus Signals and Definitions (Cont)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Cycle</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Write/Byte (BWTBTL)</td>
<td>Address</td>
<td>When BWTBT is active, a write operation is enabled. When BWTBT is negated a read operation is enabled.</td>
</tr>
<tr>
<td></td>
<td>Data</td>
<td>If BWTBT is active during the data cycle, the write operation that is performed is write byte. Address bit 0 tells the logic what byte will be modified.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If BWTBT is negated during the data cycle, the write operation that is performed is write word.</td>
</tr>
<tr>
<td>Bus Bank 7 Select (BBS7 L)</td>
<td>Address</td>
<td>The bus master generates BBS7 during the address cycle and removes the signal at the end of the address cycle. The memory, on receiving the signal changes the name to BSEL 7 H. BSEL H (BBS7 L) implies the address on the LSI-11 bus is an I/O address. If address bits 5-12 are correct for CSR, BSEL H enables the CSR address decode logic and inhibits the memory address decode from the PROMs.</td>
</tr>
<tr>
<td></td>
<td>Data</td>
<td>BSEL L (BBS7 H) implies the address on the LSI-11 bus is a memory address. This allows the memory address decode from the PROMs and inhibits CSR address decode.</td>
</tr>
<tr>
<td>Bus Synchronize (B SYNC L)</td>
<td>Address</td>
<td>B SYNC L is asserted by the bus master to indicate that it has placed an address on the LSI-11 bus.</td>
</tr>
<tr>
<td></td>
<td>Data</td>
<td>The transfer is in progress until B SYNC L is negated. When memory receives B SYNC L it does the following.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Latches address bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Latches row address bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Latches column address bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sets read or WT request flip-flop.</td>
</tr>
<tr>
<td>Bus Data Input (BDIN L)</td>
<td>Data</td>
<td>When asserted during B SYNC L time, BDIN L implies an input transfer with respect to the current bus master and requires a response (BRPLY) from the addressed slave (memory). When the memory receives BDIN L it enables the memory transmitters. This allows the data to be sent out on the LSI-11 bus.</td>
</tr>
</tbody>
</table>
Table 3-2  LSI-11 Bus Signals and Definitions (Cont)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Cycle</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Data Output (BDOUT L)</td>
<td>Data</td>
<td>BDOUT, when asserted, implies that valid data is available on BDAL 15-00 L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the LSI-11 bus. On receiving BDOUT L the memory generates write REQ L and if permitted, starts the memory timing. Arbitration with refresh always takes place with write or read request.</td>
</tr>
<tr>
<td>Bus Reply (BRPLY L)</td>
<td></td>
<td>The slave (memory) asserts BRPLY in response to BDIN L or BDOUT L. BRPLY L is generated by a slave device to indicate that it will place its data on the BDAL lines or that it will accept data from the BDAL lines according to proper protocol.</td>
</tr>
<tr>
<td>Termination</td>
<td></td>
<td>When the bus master receives BRPLY L, it starts a chain of events that terminates the transfer.</td>
</tr>
</tbody>
</table>

3.2.1  LSI-11 Bus Dialogues
The MSV11-P memory module responds to the following dialogues: DATI, DATO(B) and DATIO(B). Table 3-3 explains which figure and table to use with each dialogue.

Table 3-3  Dialogues to Perform Memory Data Transfers

<table>
<thead>
<tr>
<th>Dialogue</th>
<th>Figure</th>
<th>Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATO(B)</td>
<td>3-3</td>
<td>3-4</td>
</tr>
<tr>
<td>DATI</td>
<td>3-4</td>
<td>3-5</td>
</tr>
<tr>
<td>DATIO(B)</td>
<td>3-5</td>
<td>3-6</td>
</tr>
</tbody>
</table>
Figure 3-3  Dialogue DATO(B)

Table 3-4  Dialogue DATO(B) Cycle

<table>
<thead>
<tr>
<th>Bus Master</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Address Cycle</strong></td>
<td></td>
</tr>
<tr>
<td>(BDAL) 21–00 L</td>
<td>Memory receives the address and accepts or rejects it according to how the board was jumpered. The memory board that accepts the address generates MSEL provided BSEL 7 H is negated.</td>
</tr>
<tr>
<td>(BBS7)L</td>
<td>BSEL 7 H negated enables the address decode logic to generate MSEL.</td>
</tr>
<tr>
<td>(BWTBT)L</td>
<td>Memory sets up to do a write cycle by preventing the setting of the read request flip-flop.</td>
</tr>
<tr>
<td>(BSYNC)L</td>
<td>(BSYNC)L latches the following.</td>
</tr>
<tr>
<td></td>
<td>Address</td>
</tr>
<tr>
<td></td>
<td>Row address</td>
</tr>
<tr>
<td></td>
<td>Column address</td>
</tr>
<tr>
<td></td>
<td>Set write request flip-flop.</td>
</tr>
<tr>
<td><strong>Data Cycle</strong></td>
<td></td>
</tr>
<tr>
<td>Bus master takes the address and BBS7 L off-line.</td>
<td></td>
</tr>
<tr>
<td>(BSYNC)L</td>
<td>(BSYNC)L is still active.</td>
</tr>
<tr>
<td>(BWTBT)L</td>
<td>If BWTBT is active, it writes a byte.</td>
</tr>
<tr>
<td></td>
<td>If BWTBT is negated, it writes a word.</td>
</tr>
</tbody>
</table>
Table 3-4 Dialogue DATO(B) Cycle (Cont)

<table>
<thead>
<tr>
<th>Bus Master</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Cycle</strong></td>
<td></td>
</tr>
<tr>
<td>(BDAL) 21–00 L</td>
<td>Data is received from BDAL 15–00 L and two parity bits are generated. The 18 bits, 16 bits data and 2 bits parity, are inputs to the MOS chips.</td>
</tr>
<tr>
<td>(BDOU{T})L</td>
<td>Memory receives (BDOU{T})L and generates write request. Write request goes to the arbitration logic; if there is no refresh request or refresh cycle in progress, write request initializes the memory timing. The effects of timing enable the memory module to write the data into the MOS chips and generate (BRPLY)L.</td>
</tr>
</tbody>
</table>

**Termination of Bus Cycle**

<table>
<thead>
<tr>
<th>Bus master receives (BRPLY)L and removes data and (BDOU{T})L from the LSI-11 bus.</th>
<th>(BRPLY)L</th>
</tr>
</thead>
<tbody>
<tr>
<td>(BDOU{T})L negated</td>
<td>Memory receives BDOU{T} negated and negates (BRPLY)L.</td>
</tr>
<tr>
<td>Bus master receives (BRPLY)L negated and negates (BSYNC)L which terminates the transfer.</td>
<td>(BRPLY)L is negated.</td>
</tr>
</tbody>
</table>

**Figure 3-4 Dialogue DATI**
Table 3-5  Dialogue DATI Cycle

<table>
<thead>
<tr>
<th>Bus Master</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Cycle</td>
<td></td>
</tr>
<tr>
<td>(BDAL) 21–00 L</td>
<td>Memory receives the address and accepts or rejects it, according to how the board was jumpered. The memory module that accepts the address generates MSEL, provided BSEL 7 H is negated.</td>
</tr>
<tr>
<td>(BBS7)L negated</td>
<td>BSEL 7 H negated enables the address decode logic to generate MSEL.</td>
</tr>
<tr>
<td>(BWTBT)L negated</td>
<td>Memory sets up to set the read request flip-flop.</td>
</tr>
<tr>
<td>(BSYNC)L</td>
<td>(BSYNC)L latches address and row and column address bits, and sets the read request flip-flop. The read request goes to the arbitration logic. If there is no refresh request or refresh cycle in progress, the read request initializes the memory timing.</td>
</tr>
<tr>
<td>Data Cycle</td>
<td></td>
</tr>
<tr>
<td>(BSYNC)L</td>
<td>(BSYNC)L is still active.</td>
</tr>
<tr>
<td>(BDIN)L</td>
<td>When memory receives (BDIN)L it enables the memory transmitters, for DAL 15–00, as soon as TRPLY is active. Then the read data can be sent out on the LSI-11 bus.</td>
</tr>
<tr>
<td>Bus master receives (BRPLY)L indicating memory will place its data on the BDAL lines.</td>
<td>The memory generates (BRPLY)L as a result of receiving BDIN L and TRPLY L.</td>
</tr>
<tr>
<td>Bus master receives the data.</td>
<td>Data read from memory goes to parity checking logic and is latched and sent out through transceivers DAL 15–00. DAL 16 and 17 are 0s if no parity error was detected, or 1s if a parity error was detected.</td>
</tr>
<tr>
<td>Termination Cycle</td>
<td></td>
</tr>
<tr>
<td>(BDIN)L negated when bus master receives BDIN L this causes (BDIN)L to be negated.</td>
<td>The signal (BDIN)L negated causes memory to negate (BRPLY)L, which in turn prevents the transceivers from placing data on BDAL 15–00.</td>
</tr>
<tr>
<td>Bus master receives (BRPLY)L negated which terminates bus cycle.</td>
<td>(BRPLY)L is negated.</td>
</tr>
</tbody>
</table>


Figure 3-5  Dialogue DATIO(B)

Table 3-6  Dialogue DATIO(B) Cycle

<table>
<thead>
<tr>
<th>Bus Master</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Address Cycle</strong></td>
<td></td>
</tr>
<tr>
<td>(BDAL) 21-00 L</td>
<td>Memory receives the address and accepts or rejects it according to how the board was jumpered. The memory board that accepts the address generates MSEL, provided BSEL 7 H is negated.</td>
</tr>
<tr>
<td>(BBS7)L</td>
<td>BSEL 7 H negated enables the address decode logic to generate MSEL.</td>
</tr>
<tr>
<td>(BWTBT) L negated</td>
<td>Memory sets up to set the read request flip-flop.</td>
</tr>
<tr>
<td>(BSYNC)L</td>
<td>(BSYNC)L latches address and row and column address bits, and sets the read request flip-flop. The read request goes to arbitration logic. If there is no refresh or refresh cycle in progress, the read request starts the memory timing.</td>
</tr>
</tbody>
</table>
### Table 3-6  Dialogue DATIO(B) Cycle (Cont)

<table>
<thead>
<tr>
<th>Bus Master</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Data Cycle (Read)</strong></td>
<td></td>
</tr>
<tr>
<td>(BSYNC)L</td>
<td>(BSYNC)L is still active.</td>
</tr>
<tr>
<td>(BDIN)L</td>
<td>When memory receives (BDIN)L it enables the memory transmitter, for DAL 15–00, as soon as TRPLY is active. Then the read data can be sent out on the LSI-11 bus.</td>
</tr>
<tr>
<td>Bus master receives (BRPLY)L indicating memory will place its data on BDAL 15–00 L and negates (BDIN)L.</td>
<td>The memory generates (BRPLY)L as a result of receiving BDIN L and TRPLY.</td>
</tr>
<tr>
<td>Bus master receives the data.</td>
<td>Data read from memory goes to parity checking logic and is latched and sent out through the transceivers DAL 15–00. DAL 16 is 0s if no parity error was detected, or 1s if a parity error was detected.</td>
</tr>
<tr>
<td>(BDIN)L negated</td>
<td>Complete input transfer – remove data from BDAL 15–00 negate (BRPLY)L.</td>
</tr>
<tr>
<td>Bus master receives (BRPLY)L negated and gets ready to output data.</td>
<td>(BRPLY)L is negated.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Pause</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>(BDIN)L negated</td>
</tr>
<tr>
<td>Bus master receives (BRPLY)L negated and gets ready to output data.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Data Cycle (Write)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>(BSYNC)L</td>
</tr>
<tr>
<td>(BWTBT)L</td>
</tr>
<tr>
<td>(BWTBT)L active means write byte. (BWTBT)L negated means write word.</td>
</tr>
<tr>
<td>Data output BDAL 21–00 L</td>
</tr>
<tr>
<td>(BDOU[T]L</td>
</tr>
</tbody>
</table>
3.3 FUNCTIONAL DESCRIPTION OF MEMORY MODULE

All MSV11-P memory modules have the logic functions shown in Figure 3-6. The charge pump circuit is used only with the M8067-FA module (16K chips). The functions shown in Figure 3-6 are discussed in detail in the following paragraphs.

3.3.1 Xcvers (Transmit-Receives)
The Xcvers allow memory to transmit or receive: address, data, and control, via the LSI-11 bus. The LSI-11 bus signals are defined in Table 3-2.

3.3.2 Address Logic

1. The modules are jumpered for a starting address and a CSR address.

2. MSV11-P memory modules receive all addresses from the LSI-11 bus.

3. The address decode logic on each memory module checks to see if the board is selected (memory select) or the CSR is selected.

3.3.2.1 Board Selection Decode Logic – This consists of two PROMs that monitor BDAL 21-14 and compare the address received against the starting address jumpers. The PROMs are programmed to enable the logic to generate memory select (MSEL) and row enables (NA 16/18 and NA 15/17). Table 3-7 shows the output of the PROMs programmed for module M8067-LA with a starting address of zero. There are three different types of PROMs.

1. M8067-LA PROMs programmed for 256K addresses per module
2. M8067-KA PROMs programmed for 128K addresses per module
3. M8067-FA PROMs programmed for 64K addresses per module
Figure 3-6  Logic Functions

Table 3-7  PROM Output for M8067-LA (Starting Address Zero)

<table>
<thead>
<tr>
<th>Octal Addresses</th>
<th>NA 18</th>
<th>NA 17</th>
<th>Row Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0177 7776</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>0140 0000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0137 7776</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Generates MSEL L</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>0100 0000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0077 7776</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0040 0000</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0037 7776</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000 0000</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
The address range of the two PROMs begins with the starting address (jumper-selectable). The top limit of the memory module is then determined by what type of PROMs are being used (e.g., 256K from starting address).

3.3.2.2 MOS Memory Address Logic – Jumper consideration must be taken for 16K or 64K MOS memories when loading the row and column latches with the MOS RAM address. The logic also has a row latch used for refresh addresses.

The MSV11-P family of memory modules perform three basic operations.

- CSR read/write transfers
- Memory read/write transfers
- Refresh cycles

When CSR transfers take place, the row select signals (RAS 0-3) and column select signals (CAS 0-3) are inhibited (Figure 3-7).

When read/write cycles take place, the PROM sends the row enable signals (RAS 0-3) to the MOS memory array in order to select the proper row. All columns (CAS 0-3) are always selected (Figure 3-7). First the row address, then the column address is loaded into internal registers in the MOS RAM chips. One 18 bit location in memory is now selected.

When refresh cycles take place, the column select logic is inhibited. All rows are selected (RAS 0-3). The refresh row address is loaded into an internal register in the MOS RAM chips (Figure 3-7), and that address is refreshed.

3.3.2.3 CSR Address Logic – Memory receives a CSR address and compares (XOR) DAL1-DAL4 with the CSR jumpers. If there is a match, CSR selected (CSR) is generated. CSR generates MSEL, which enables a read/write request to start the memory timing. RAS and CAS are inhibited; therefore, no memory addressing occurs.

3.3.3 CSR Write (Figure 3-8)
CSR address and signals BBS7 and BWTBT are received by the memory. If the CSR address matches the CSR jumpers, CSR SEL and MSEL are generated. When BSYNC is received, the address and CSR SEL are latched, and the WT REQ flip-flop is set. During the data cycle the memory receives the data to be stored in the CSR register. Then, BDOU is received and write request starts memory timing. The signal LAT CSR SEL selects the received data to be passed through the multiplexed inputs to the CSR register. The CSR clock logic generates the CSR clock pulse which, in turn, loads the CSR register.
Figure 3-7  Overview of Memory Logic
3.3.4 CSR Read (Figure 3-9)
CSR address, BBS7, and BWTBT negated are received by the memory. If the CSR address matches the CSR jumpers, CSR SEL and MSEL are generated. When BSYNC is received, the address and CSR SEL are latched, and the RD REQ flip-flop is set, starting the memory timing. As soon as TRPLY is generated, the contents of the CSR is latched. Memory receives BDIN L, which enables the memory to transmit the latched CSR data onto the LSI-11 bus.

3.3.5 Memory Array
The MSV11-P family of memory modules uses early writes. Early writes are achieved by a write going low prior to CAS going active. Data in is strobed into the MOS chips by CAS going active.

The following MOS RAM chips are used in the MSV11-P memory modules.

M8067-LA  (64K chips) - A fully populated module that consists of four rows of MOS RAM chips (512K bytes)
M8067-KA  (64K chips) - A half populated module that consists of two rows of MOS RAM chips (256K bytes)

M8067-FA  (16K chips) - A fully populated module that consists of four rows of MOS RAM chips (128K bytes)

The MOS RAM chips used in the M8067-LA and M8067-KA memory modules are dynamic random access memory circuits organized as a 65,536 by 1 bit (Figure 3-10). The MOS chips used in the M8067-FA memories are dynamic random access memory circuits organized as a 16,384 by 1 bit (Figure 3-11).

3.3.6 Timing and Control Logic

The memory responds to the asynchronous read/write commands or the synchronous refresh cycle that takes place every 14.5 μs. All requests go to the memory timing lockout gate. When timing lockout is negated, the request goes to arbitration and the winner gains control of the memory timing (Figure 3-12).
### PIN OUT

<table>
<thead>
<tr>
<th>PIN</th>
<th>PIN FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CAS</td>
</tr>
<tr>
<td>2</td>
<td>DATA IN</td>
</tr>
<tr>
<td>3</td>
<td>DATA OUT</td>
</tr>
<tr>
<td>4</td>
<td>RAS</td>
</tr>
<tr>
<td>5</td>
<td>A0</td>
</tr>
<tr>
<td>6</td>
<td>A1</td>
</tr>
<tr>
<td>7</td>
<td>A2</td>
</tr>
<tr>
<td>8</td>
<td>A3</td>
</tr>
<tr>
<td>9</td>
<td>A4</td>
</tr>
<tr>
<td>10</td>
<td>A5</td>
</tr>
<tr>
<td>11</td>
<td>A6</td>
</tr>
<tr>
<td>12</td>
<td>A7</td>
</tr>
<tr>
<td>13</td>
<td>A8</td>
</tr>
<tr>
<td>14</td>
<td>A9</td>
</tr>
<tr>
<td>15</td>
<td>A10</td>
</tr>
<tr>
<td>16</td>
<td>A11</td>
</tr>
</tbody>
</table>

**Figure 3-10** 64K MOS RAM Chip

### PIN CONNECTIONS

<table>
<thead>
<tr>
<th>PIN</th>
<th>PIN FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VBB</td>
</tr>
<tr>
<td>2</td>
<td>DIN</td>
</tr>
<tr>
<td>3</td>
<td>WRITE</td>
</tr>
<tr>
<td>4</td>
<td>RAS</td>
</tr>
<tr>
<td>5</td>
<td>A0</td>
</tr>
<tr>
<td>6</td>
<td>A1</td>
</tr>
<tr>
<td>7</td>
<td>A2</td>
</tr>
<tr>
<td>8</td>
<td>A3</td>
</tr>
<tr>
<td>9</td>
<td>A4</td>
</tr>
<tr>
<td>10</td>
<td>A5</td>
</tr>
<tr>
<td>11</td>
<td>A6</td>
</tr>
<tr>
<td>12</td>
<td>A7</td>
</tr>
<tr>
<td>13</td>
<td>A8</td>
</tr>
<tr>
<td>14</td>
<td>A9</td>
</tr>
<tr>
<td>15</td>
<td>A10</td>
</tr>
<tr>
<td>16</td>
<td>VSS</td>
</tr>
</tbody>
</table>

**Figure 3-11** 16K MOS Chip

### PIN NAMES

- **VBB**: POWER (-5V)
- **VCC**: POWER (+5V)
- **VDD**: POWER (+12V)
- **VSS**: GROUND
- **A0-A6**: ADDRESS INPUTS
- **CAS**: COLUMN ADDRESS STROBE
- **DIN**: DATA IN
- **DOUT**: DATA OUT
- **RAS**: ROW ADDRESS STROBE
- **WRITE**: READ/WRITE INPUT
- **NOT USED**:
3.3.7 Parity Logic

The parity logic performs the following two functions.

1. Parity generation - when the bus master is doing a DATO(B)

2. Parity checking - when the bus master is doing a DATI

3.3.7.1 Parity Generation – The data received from the bus master on the LSI-11 bus (DAL00-15) goes to the parity generators (Figure 3-13).

The low byte parity generator generates odd parity (PDI 16 H). The high byte parity generator generates even parity (PDI 17 H).

CSR02 enables the diagnostic to force wrong parity. This enables the diagnostic to check out the parity logic.
3.3.7.2 Parity Checker – The MSV11-P memory modules detect parity errors, report parity errors, and save the address of the parity error in the CSR register. Parity detection logic always expects byte 0 to have an even number of one bits and byte 1 to have an odd number of one bits. If this does not happen, T PAR ERR L is generated (Figure 3-14).

Parity reporting is done if the program has set CSR bit 0, the parity error enable bit, T PAR ERR L, and RDIN negated. This allows BDAL 16 and BDAL 17 to be sent out on the LSI-11 bus to flag a parity error.

Parity address is saved in the following way.

- After the data is read from memory, it goes to the parity checkers and a holding register.
- When the data is latched, the signal CSR CLK is generated if there is a parity error (Figure 3-14).
- CSR CLK latches the address in the CSR register.

CSR cycles or refresh cycles inhibit the parity logic.

3.3.8 Refresh
The MSV11-P memory modules are MOS RAM chips which are refreshed every 2 ms. The logic refreshes a row at a time; 128 rows are refreshed in a 2 ms period.

Figure 3-15 shows that a refresh timer generates a pulse every 14.5 μs. This pulse, called REF CLK, does the following.

- Generates a refresh request
- Increments the refresh address CTR

The address counter produces row address bits A1 through A7 for 16K chips, and A1 through A8 for 64K chips.
Figure 3-14 Parity Checkers

Figure 3-15 Refresh Logic and Charge Pump Circuit
3.3.9 Charge Pump Circuit
The purpose of the charge pump circuit is to generate a filtered regulated 
−5 V. The M8067-LA and M8067-KA modules, which use 64K chips, do 
not require −5 V. If W3 is removed (Figure 3-15), then the memory mod­
ules mentioned above will not receive −5 V. The M8067-FA modules, 
which use 16K chips, require −5 V; therefore, W3 must be installed.

The −5 V is generated in the following manner (Figure 3-16). The output 
of the timer is a +12 V pulse that occurs every 14.5 μs. The +12 V pulse 
goes to a rectifier whose output is −11 V. A three terminal regulator 
takes the −11 V and produces a regulated −5 V. The −5 V regulator 
output goes to module pin connection BK1, which is connected to BL1 on 
the backplane. Filter capacitors receive the −5 V and pass the filtered 
−5 V to the output, if W3 is installed.

3.4 CONTROL AND STATUS REGISTER (CSR) BIT ASSIGNMENT
The control and status register (CSR) in the MSV 11-P allows program 
control of certain parity functions, and contains diagnostic information if a 
parity error has occurred. The CSR is assigned an address and can be 
accessed by a bus master via the LSI-11 bus. Some CSR bits are cleared 
by assertion of BUS INIT L. This signal is asserted for a short time by the 
processor after system power has come up, or in response to a reset in­
struction. The CSR bit assignments are shown in Figure 3-17 and are de­
scribed as follows.

Bits 1, 3, 4, 12, and 13 These bits are not used and are always 
read as logical zeros. Writing into these 
bits has no affect on the CSR.

Bit 0 Parity Error Enable - If a parity error 
occurs on a DATI or DATIO(B) cycle to 
memory, and bit 0 is set = 1, then BDAL 
16 L and BDAL 17 L are asserted on the 
bus simultaneously with data. This is a 
read/write bit reset to zero on power up 
or BUS INIT.

Figure 3-16 CSR Bit Allocation
Bit 2
Write Wrong Parity - If this bit is set = 1 and a DATO or DATOB cycle to memory occurs, wrong parity data is written into the parity MOS RAMs. This bit can be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable.

- With bit 2 set, writes entire memory with any pattern.
- Read first location in memory, if bit 0 of the CSR is set, then a parity error indication is detected on the LSI-11 bus, and the failed address (location 0) is stored in the CSR.
- Reads the CSR and obtains the failed address, CSR bit 14 = 0 implies A11-A17 on CSR bits 5-11. CSR bit 14 = 1 implies A18-A21 on CSR bits 5-8. Bit 2 is a read/write bit reset to zero on power up or BUS INIT.

Bits 05-11
Error Address Bits - If a parity error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 5-11 and bits A18-A21 are latched. The 128K word machines (18-bit address) require only one read of the CSR register to obtain the failed address bits. CSR bit 14 = 0 allows the logic to pass A11-A17 to the LSI-11 bus. A 2048K word machine (22-bit address) requires two reads. The first read CSR bit 14 = 0 sends contents of CSR bits 5-11. Then the program must set CSR bit 14 = 1. This enables A18-A21 to be read from CSR bits 05-08.

The parity error addresses locate the parity error to a 1K segment of memory. These are read/write bits and are not reset to zero via power up or BUS INIT. If a second parity error is encountered, the new failed address is stored in the CSR.

Bit 14
Extended CSR Read Enable - The use of this bit was explained in the error address description.
Bit 14 = 0, always for 128K word machine

Bit 14 = 0, first read on 2048K word machine

Bit 14 = 1, second read on 2048K word machine

Bit 15

Parity Error - This bit set indicates that a parity error has occurred. The bit then turns on a red LED on the module. This provides visual indication of a parity error.

Bit 15 is a read/write bit. It is reset to zero via power up or BUS INIT and remains set unless rewritten or initialized.
CHAPTER 4
MAINTENANCE

4.1 GENERAL
The maintenance procedures in this chapter apply to both versions of the MSV11-P memory module. To perform corrective maintenance on this product, the user must understand basic operation of the MSV11-P memory module as described in the previous chapters. This knowledge, together with diagnostic testing knowledge, should help the user isolate MSV11-L malfunctions.

CAUTION: ALL power must be off before installing or removing modules. Always be sure the component side of the memory faces in the same direction as the other modules within the LSI system.

4.2 PREVENTIVE MAINTENANCE
Preventive maintenance pertains to specific tasks, performed at intervals, to detect conditions that may lead to performance deterioration or malfunction. The following tasks can be performed along with other scheduled preventive maintenance procedures for the LSI computer system.

1. Visual inspection
2. Voltage measurements
3. Diagnostic testing

4.2.1 Visual Inspection
Inspect the modules and backplane for broken wires, connectors, or other obvious defects.

4.2.2 Power Voltage Check
Once primary power has been turned on, check the dc power voltage at the backplane (Table 4-1).
# MAINTENANCE

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Backplane Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>AA2, BA2, BV1, CA2, and DA2</td>
</tr>
<tr>
<td>+5V BBU</td>
<td>AV1 and AE1* or AV1 and AS1*</td>
</tr>
<tr>
<td>+5V</td>
<td>AA2, BA2, BV1, and CA2</td>
</tr>
<tr>
<td>+12V</td>
<td>AD2 and BD2</td>
</tr>
<tr>
<td>+5V BBU</td>
<td>AV1 and AE1</td>
</tr>
<tr>
<td>+12V BBU</td>
<td>AS1</td>
</tr>
</tbody>
</table>

*Check backplane voltages to ensure proper configurations.

## 4.2.3 Diagnostic Testing

Memory diagnostic programs are available from DIGITAL for testing the MSV11-PF/PK/PL memory modules.

For fault isolation in 22-bit systems and 18-bit systems use the following diagnostics.

- MAINDEC-11 CVMSA (22-bit system)
- MAINDEC-11 CZKMA (18-bit system)

In most cases a bad memory module can be detected by using the error printout and program listing.

Detailed operating instructions and program listings are included with each diagnostic software kit.

## 4.3 DIGITAL'S SERVICES

Maintenance services can be performed by the user or by DIGITAL. DIGITAL's maintenance and on-site services are described in Chapter 1 of the *Microcomputer Processor Handbook* (EB-18451-20).
Figures A-1, A-2, A-3, and A-4 provide the flow diagram and signal sequences for DATO(B), DATI, and DATIO(B).
Figure A-1  Memory Operation Cycle
Figure A-2  DATO(B) Signal Sequence

Figure A-3  DATI Signal Sequence
Figure A-4  DATIO(B) Signal Sequence