DN11
automatic calling unit
interface manual
CONTENTS

CHAPTER 1 INTRODUCTION

CHAPTER 2 GENERAL DESCRIPTION

2.1 Introduction 2-1
2.2 Functional Description 2-1
2.2.1 System Configuration 2-1
2.2.2 DN11 Automatic Calling Unit Interface 2-2
2.2.3 DN11 Control Module M7226 2-2
2.2.4 Overall Operation 2-3
2.3 Physical Description 2-4
2.3.1 Configuration 2-4
2.3.2 Interface Cabling 2-5
2.3.3 Power and Bus Loading Requirements 2-5
2.3.4 Address Assignments 2-6
2.3.5 M7820 and M7821 Interrupt Modules 2-8

CHAPTER 3 DETAILED DESCRIPTION

3.1 Introduction 3-1
3.2 Bell 801 Automatic Calling Unit 3-1
3.3 M7226 DN11 Control Module 3-2
3.3.1 Introduction 3-2
3.3.2 Control and Status Register 3-2
3.3.3 Gating Logic 3-4
3.3.4 Interrupt Control Logic 3-6
3.4 Automatic Call Sequence 3-10
3.4.1 Introduction 3-10
3.4.2 Dialing 3-10
3.4.3 Answering 3-11
3.4.4 Abandon Call and Retry 3-11
3.4.5 Call Termination 3-12
3.5 Maintenance Mode 3-12
3.6 Bus Data Transfer Operations 3-13
3.6.1 Introduction 3-13
3.6.2 DATI Operation 3-13
3.6.3 DATO Operation 3-14
3.6.4 DATOB Operation 3-14
3.7 Interrupt Transaction 3-14
3.7.1 Introduction 3-14
3.7.2 Interrupt Operational Sequence 3-15

CHAPTER 4 PROGRAMMING INFORMATION

CHAPTER 5 MAINTENANCE

5.1 Introduction 5-1
CONTENTS (Cont)

5.2 DNII Diagnostic Program MAINDEC-11-D9JA .......................... 5-1

APPENDIX A INTEGRATED CIRCUIT DESCRIPTION

7474 Dual D-Type Edge-Triggered Flip-Flops A-2
8266 2-Input 4-Bit Digital Multiplexer A-3

APPENDIX B LOGIC SYMBOLOGY

B.1 Introduction .............................................................. B-1
B.2 Unibus Signal Levels .................................................. B-1
B.3 Equivalent Gate Symbols ............................................. B-1
B.4 Physical Representation of D-Type Flip-Flops ..................... B-2
B.5 2-Output Terminal Flip-Flop Symbology ............................ B-3
B.6 Redefined 4-Output Terminal Flip-Flops ............................ B-3

ILLUSTRATIONS

<table>
<thead>
<tr>
<th>Figure No.</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1</td>
<td>Typical DNII System Application, Simplified Block Diagram</td>
<td>2-1</td>
</tr>
<tr>
<td>2-2</td>
<td>DNII Automatic Calling Unit Interface, Simplified Block Diagram</td>
<td>2-2</td>
</tr>
<tr>
<td>2-3</td>
<td>DNII System Unit Layout</td>
<td>2-5</td>
</tr>
<tr>
<td>2-4</td>
<td>801 Interface Pin Assignments</td>
<td>2-6</td>
</tr>
<tr>
<td>3-1</td>
<td>Typical Status Register Read/Write Bit (D02), Simplified Logic Diagram</td>
<td>3-4</td>
</tr>
<tr>
<td>3-2</td>
<td>Gating Logic Diagram</td>
<td>3-5</td>
</tr>
<tr>
<td>3-3</td>
<td>Address Word for Line 1</td>
<td>3-5</td>
</tr>
<tr>
<td>3-4</td>
<td>Interrupt Control Circuit, Simplified Logic Diagram</td>
<td>3-7</td>
</tr>
<tr>
<td>3-5</td>
<td>One Bit (PND) of 8266 2-Input 4-Bit Multiplexer, Logic Diagram</td>
<td>3-8</td>
</tr>
<tr>
<td>3-6</td>
<td>Typical Negative-Edge Triggered One-Shot (Pulser), Schematic and Timing Diagram</td>
<td>3-9</td>
</tr>
<tr>
<td>B-1</td>
<td>Logically Equivalent Gates</td>
<td>B-2</td>
</tr>
<tr>
<td>B-2</td>
<td>7474/74H74 Pin Designations and Truth Table</td>
<td>B-2</td>
</tr>
<tr>
<td>B-3</td>
<td>Flip-Flop Logic Symbology</td>
<td>B-3</td>
</tr>
<tr>
<td>B-4</td>
<td>Electrical Connections to Outputs of 2-Terminal and 4-Terminal Flip-Flops</td>
<td>B-4</td>
</tr>
<tr>
<td>B-5</td>
<td>Standard and Redefined 4-Terminal Flip-Flops</td>
<td>B-4</td>
</tr>
</tbody>
</table>

TABLES

<table>
<thead>
<tr>
<th>Table No.</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1</td>
<td>Control and Status Register Bits</td>
<td>2-3</td>
</tr>
<tr>
<td>3-1</td>
<td>Control and Status Register Bit Assignments</td>
<td>3-2</td>
</tr>
<tr>
<td>3-2</td>
<td>Gating Logic Signal Selection</td>
<td>3-5</td>
</tr>
<tr>
<td>Table No.</td>
<td>Title</td>
<td>Page</td>
</tr>
<tr>
<td>----------</td>
<td>---------------------------------------------------------</td>
<td>--------</td>
</tr>
<tr>
<td>3-3</td>
<td>Select Signals</td>
<td>3-6</td>
</tr>
<tr>
<td>3-4</td>
<td>Response Signal Representation by Digit Flip-Flops</td>
<td>3-12</td>
</tr>
</tbody>
</table>
CHAPTER 1
INTRODUCTION

The DN11 Automatic Calling Unit Interface controls a Bell 801 Automatic Calling Unit (or equivalent) to dial any telephone number in the U.S. Direct Distance Dialing Network. It is used in a system with a modem and associated serial line interface (DC11, DP11, DJ11, DQ11, or DM11) to establish a data link between the PDP-11 and a remote terminal.

Although signals are transferred between the DN11 and the Unibus, this manual does not describe the operation of the Unibus. A detailed description of the Unibus is presented in the PDP-11 Peripherals and Interfacing Handbook. The PDP-11 computer is described in a set of PDP-11/20 manuals, DEC-11-HR1A-D through DEC-11-HR7A-D.

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the DN11 Automatic Calling Unit Interface. The level of discussion assumes that the reader is familiar with basic digital computer theory.

This manual is organized into five chapters: Introduction, General Description, Detailed Description, Programming Information, and Maintenance. A separate set of engineering drawings is provided with each DN11. They are listed below.

<table>
<thead>
<tr>
<th>Drawing No.</th>
<th>Title</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-CS-M7226-0-1</td>
<td>Control (DN11)</td>
<td>Sheet 1 is component placement and parts reference. Sheets 2 and 3 are logic diagrams.</td>
</tr>
<tr>
<td>C-CS-M105-0-1</td>
<td>Address Selector M105</td>
<td>Logic diagram</td>
</tr>
<tr>
<td>D-CS-M7821-0-1</td>
<td>Interrupt Control M7821</td>
<td>Logic diagram</td>
</tr>
<tr>
<td>D-BD-DN11-0-01</td>
<td>Block Diagram (DN11)</td>
<td>Detailed block diagram of DN11 Interface</td>
</tr>
<tr>
<td>B-CS-M117-0-1</td>
<td>Six 4-Input NAND Gates M117</td>
<td>Long diagram</td>
</tr>
<tr>
<td>B-CS-M002-0-1</td>
<td>Logic High Source</td>
<td>Circuit diagram</td>
</tr>
<tr>
<td>D-JC-DN11-0-02</td>
<td>Unibus Connectors (DN11)</td>
<td>Circuit diagram</td>
</tr>
<tr>
<td>B-CS-G8000-0-1</td>
<td>Filter Network G8000</td>
<td>Circuit diagram</td>
</tr>
<tr>
<td>D-AD-7008513-0-0</td>
<td>Wired Assembly</td>
<td>Circuit diagram and wiring table</td>
</tr>
<tr>
<td>D-UA-BC01R-0-0</td>
<td>Cable Card Assembly (BC01R)</td>
<td>Circuit diagram and wiring table</td>
</tr>
<tr>
<td>C-CS-M920-0-1</td>
<td>M920 Internal Bus Connector</td>
<td>Circuit diagram</td>
</tr>
<tr>
<td>D-MU-DN11-0-03</td>
<td>Module Utilization</td>
<td>Block diagram</td>
</tr>
<tr>
<td>K-WL-DN11-0-4</td>
<td>DN11 Wire List</td>
<td>Printed list</td>
</tr>
</tbody>
</table>
CHAPTER 2
GENERAL DESCRIPTION

2.1 INTRODUCTION

This chapter presents an overview of the operation of the DN11 Automatic Calling Unit Interface. It contains a functional description that is keyed to the block diagram level and a physical description that defines the DN11 configuration and general specifications.

2.2 FUNCTIONAL DESCRIPTION

2.2.1 System Configuration

The DN11, under programmed instructions from a PDP-11, controls a Bell 801 Automatic Calling Unit (801 ACU) to dial any telephone number in the Direct Distance Dialing Network. The objective is to establish a data link between the PDP-11 and a remote terminal. In a typical application (Figure 2-1) a local modem is required to handle the data transfer between sites. A serial-type controller, such as a DC11 Asynchronous Line Interface, is required to control the modem.

![Diagram of DN11 System Application](image)

Figure 2-1 Typical DN11 System Application, Simplified Block Diagram
2.2.2 DNII Automatic Calling Unit Interface

A single DNII-AA Interface (Figure 2-2) with four DNII-DA Module Sets installed can control four 801 units. The DNII-DA Module Set consists of an M7226 Control Module and a BC01R-00 Cable Card Assembly: one set is required for each 801. Each DNII control module has one addressable control and status register, so one M105 Address Selector Module is used to decode the addresses and provide the required gating signals for up to four DNII control modules. One M7821 Interrupt Control Module is used because each DNII Interface has one assigned vector address although any one of four DNII control modules can initiate the interrupt. One 4-input NAND gate on an M117 module is used in the interrupt initiating circuitry. One M002 Logic Source Module is used to provide +3V for any unused NAND gate inputs on the M117 module so that each unused input, which corresponds to a non-installed DNII-DA, is gated off.

Figure 2-2 DNII Automatic Calling Unit Interface, Simplified Block Diagram

2.2.3 DNII Control Module M7226

The major functional units of the M7226 module include a 15-bit control and status register, interrupt control, gating logic, Unibus drivers and receivers, and level converter/drivers and receivers (Figure 2-2). The functional units are briefly described in the following paragraphs.

The 15-bit control and status register provides various control and status signals. Five bits are read-only and ten are read/write. Table 2-1 describes the bits.

The interrupt control accepts four input signals from the 801, multiplexes them, and provides one output that sets the DONE flip-flop to initiate the interrupt sequence. The four input signals are Data Set Status (DSS), Abandon Call and Retry (ACR), Power Indicator (PWI), and Present Next Digit (PND). The interrupt control circuit is initiated only by transitions of these signals.

Gating logic decodes control signals from the M105 Address Selector Module to generate enabling signals for control and status register and Unibus drivers.
### Table 2-1
Control and Status Register Bits

<table>
<thead>
<tr>
<th>Bit</th>
<th>Type</th>
<th>Signal *</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Read/Write</td>
<td>Call Request (FCRQ)</td>
<td>Requests 801 to initiate automatic calling sequence.</td>
</tr>
<tr>
<td>01</td>
<td>Read/Write</td>
<td>Data Present (FDPR)</td>
<td>Informs 801 that digit presented to it is legitimate.</td>
</tr>
<tr>
<td>02</td>
<td>Read/Write</td>
<td>Master Interrupt Enable (MINAB)</td>
<td>Allows program to disable and then reenable all four DN11 Interface interrupts.</td>
</tr>
<tr>
<td>03</td>
<td>Read/Write</td>
<td>Maintenance (MAINT)</td>
<td>Allows checking of the DN11 Interface without an 801 connected.</td>
</tr>
<tr>
<td>04</td>
<td>Read Only</td>
<td>Present Next Digit (FPND)</td>
<td>Request from 801 to present the next digit to be dialed.</td>
</tr>
<tr>
<td>05</td>
<td>Read Only</td>
<td>Data Set Status (FDSS)</td>
<td>Signal from 801 indicating that called party has answered and associated modem has control of the telephone line.</td>
</tr>
<tr>
<td>06</td>
<td>Read/Write</td>
<td>Interrupt Enable (INTENB)</td>
<td>Signal from DNII control module to qualify interrupt circuitry.</td>
</tr>
<tr>
<td>07</td>
<td>Read/Write</td>
<td>Done (DONE)</td>
<td>Requests data from program by initiating an interrupt.</td>
</tr>
<tr>
<td>08 – 11</td>
<td>Read/Write</td>
<td>Digit Bits (NB01, NB02, NB04, and NB08)</td>
<td>4-bit BCD form of digit to be dialed. Also used as test signals during maintenance mode.</td>
</tr>
<tr>
<td>12</td>
<td>Read Only</td>
<td>Data Line Occupied (FDLO)</td>
<td>Signal from 801 to indicate that it is using the telephone line.</td>
</tr>
<tr>
<td>13</td>
<td>Not Used</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Read Only</td>
<td>Abandon Call and Retry (FACR)</td>
<td>Signal from 801 when its internal timer has timed out. Indicates wrong number, busy, etc.</td>
</tr>
<tr>
<td>15</td>
<td>Read Only</td>
<td>Power Off Indicator (FPWOF)</td>
<td>Signal from 801 when its power is switched off.</td>
</tr>
</tbody>
</table>

*Signals identified as FXXX are buffered Unibus signals corresponding to the function line signals XXX between the DN11 and ACU.

Unibus drivers and receivers buffer data between the Unibus and the control and status register.

The converter drivers and receivers buffer signals between the DN11 and the 801. They also provide bidirectional conversion of the DN11 logic levels (logic 1 = +3V and logic 0 = 0V) and the 801 logic levels (-15V and +8 to +15V).

#### 2.2.4 Overall Operation

The program first tests the Power Off Indicator (FPWOOF) bit and the Data Line Occupied (FDLO) bit to see if power is applied to the 801 and that it has satisfactorily completed the previous call. The Call Request (FCRQ) bit is asserted by the program and the DN11 sends a CRQ signal to the 801 which initiates the automatic dialing sequence. The 801 seizes the line and signals the telephone central office that a call is waiting. When the central office is ready for the call, it signals the 801 to proceed. The 801 holds the line by asserting the Data Line
Occupied (DLO) signal which indicates that the line is in use. It now requests the first digit of the number to be dialed by asserting the Present Next Digit (FPND) signal to the DN11. The program responds by loading the first digit and the Data Present (DPR) signal which informs the 801 that the digit is legitimate.

The telephone number is presented a digit at a time in 4-bit BCD form. After the digit is dialed, the 801 negates PND and the DN11 negates DPR. The DN11 awaits the next PND signal from the 801 which is a request for the next digit to be dialed. This process is repeated until all digits have been dialed whereupon the network completes the call. When the destination answers, the 801 switches the telephone line back to the modem and the data is transferred between sites. Switching the line from the 801 to the modem is accomplished by a tone signal from the destination modem to the 801; or by sending an end-of-number code (EON = 1210) to the 801 as the last digit presented to the DN11. In both cases the 801 responds with a Data Set Status (DSS) signal to the DN11 which can be read to indicate that the destination has answered and the local modem is in the data mode.

Two options are available for terminating a call. The CRQ control option terminates the call locally by clearing the CRQ signal from the DN11 to the 801 after data transmission is complete. The data set control option allows the DN11 to clear CRQ after DSS is asserted without terminating the call. The modem terminates the call in the manner prescribed for the particular model used (for example, clearing the modem Data Terminal Ready signal). In both options DLO is cleared when the call is dropped to ensure the availability of the 801 and the modem for the next call.

The 801 contains an Abandon Call and Retry (ACR) timing circuit to help prevent long delays due to a wrong number, busy number, or any condition resulting in an incomplete call. The timer is set whenever PND is cleared; the timeout interval can be set for 7, 10, 15, 25, or 40 seconds. If the DN11, telephone network, or 801 takes more time than the preset interval from the last PND Clear, the Abandon Call and Retry (ACR) signal is sent from the 801 to the DN11 which sets the FACR bit. The program reads this bit and takes the appropriate action.

A cleared Power Indication (PWI) signal from the 801 indicates that it is inoperative because of a power loss. When PWI is cleared, it sets the Power Off Indicator (FPWOF) bit in the DN11. This bit is read by the program to indicate an error condition if power is lost during a call, or to prevent a call request if power is off at the start of a call sequence.

2.3 PHYSICAL DESCRIPTION

2.3.1 Configuration

One DN11 Automatic Calling Unit Interface occupies one system unit within a system mounting box. A DN11 Interface consists of two assemblies: DN11-AA and DN11-DA. The DN11-AA assembly comprises the following parts:

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Nomenclature</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>7008513</td>
<td>Wired System Unit</td>
<td>1</td>
</tr>
<tr>
<td>M920</td>
<td>Unibus Jumper Module</td>
<td>1</td>
</tr>
<tr>
<td>G8000</td>
<td>Filter Network (+15V Supply)</td>
<td>1</td>
</tr>
<tr>
<td>M002</td>
<td>Logic/Source Module</td>
<td>1</td>
</tr>
<tr>
<td>M117</td>
<td>4-Input NAND Gate Module</td>
<td>1</td>
</tr>
<tr>
<td>M7820</td>
<td>Interrupt Control Module</td>
<td>1</td>
</tr>
<tr>
<td>M105</td>
<td>Address Selector Module</td>
<td>1</td>
</tr>
<tr>
<td>H850</td>
<td>Module Extender</td>
<td>2</td>
</tr>
</tbody>
</table>

The DN11-DA assembly is a module set consisting of a DN11 Control Module M7226 and Cable Card Assembly BC01R-00. The cable is available in lengths of 25 feet (BC01R-25) and 50 feet (BC01R-50). One set is installed in the DN11-AA for each Bell 801 ACU connected to the DN11 Interface with a maximum of four 801 ACUs allowed. A DN11 Interface consists of one DN11-AA and up to four DN11-DA module sets. The module layout
for a DN11 Interface is shown in Figure 2-3. If only one 801 is to be interfaced, the M7226 Control Module must be installed in location E01/F01 because Master Enable (MINAB) bit D02 is connected in this location only. The associated BC01R-25 cable must be installed in location C01.

The M920 Unibus Jumper Module connects the Unibus from one system unit to the next. In Figure 2-3 the lower M920 module connects A04/B04 of the preceding system unit to A01/B01 of the DN11 system unit: the upper M920 module connects A04/B04 of the DN11 system unit to A01/B01 of the succeeding system unit. If the succeeding system unit is located in a different mounting box, the BC11A Unibus Cable is used. If the DN11 is the last system unit connected to the Unibus, the M930 Unibus Terminating Module must be used in place of the M920 Unibus Jumper Module.

2.3.2 Interface Cabling

The BC01R-00 Cable Card Assembly (drawing D-UA-BC01R-25-0 REV B and up) is used to interconnect the DN11 control module and the Bell ACU. One end of the cable is connected to an M970 card that plugs into the system unit and the other end terminates in a 25-pin male connector that mates with the interface connector on the rear of the 801 unit. A Cinch DB-25P connector is used with RS-232A compatible pin assignments (Figure 2-4). The M970 card is a universal connector used in other communications devices. It contains eight jumpers and the configuration varies with the application. For the DN11 Interface, all but four jumpers should be cut; the exceptions are the two EIA jumpers and the two 301 jumpers.

2.3.3 Power and Bus Loading Requirements

One line controller represents one unit load to the PDP-11 Unibus: a maximum of 20 unit loads is allowed. For more than 20 unit loads, a Unibus repeater option (DB11-A) must be used.

A DN11-AA Interface, with one line control unit installed, requires 1.4A of +5V power. Each additional line control requires 0.4A of +5V power.

In planning the system configuration, allow four unit loads and 2.6A of +5V power for each DN11-AA Interface, even if all the line control units are not installed. Planning for the maximum bus loading and power requirements allows for the easy installation of additional line control units in the field.
2.3.4 Address Assignments

Each M7226 Control Module contains one register that requires a 16-bit address. Four M7226 modules can be plugged into a DN11-AA Interface. The four associated addresses must be assigned consecutively starting with line 1 (control unit 0). If only one M7226 Control Module is used in a system, it must be installed in row 1 and assigned address 775200. Address space has been assigned for 64 lines as follows.
Each DNII Interface, whether it contains one or four controllers, requires only one interrupt vector address. The addresses are assigned in order from 300 through 777 according to a specific convention that ranks the types of communications devices in a system. The first vector address (300) is assigned to the first DCII Serial Asynchronous Line Interface in the system, the next DCII (if used) is assigned vector address 310, etc. Vector addresses are assigned consecutively to each unit of the second-ranked device in accordance with the following list.

<table>
<thead>
<tr>
<th>Rank</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DCII Asynchronous Line Interface</td>
</tr>
<tr>
<td>2</td>
<td>KLII Teletype Control</td>
</tr>
<tr>
<td>3</td>
<td>DP11 Synchronous Serial Modem Interface</td>
</tr>
<tr>
<td>4</td>
<td>DM11 Asynchronous Serial Line Multiplexer</td>
</tr>
<tr>
<td>5</td>
<td>DN11 Automatic Calling Unit</td>
</tr>
<tr>
<td>6</td>
<td>DM11-BB Modem Control</td>
</tr>
<tr>
<td>7</td>
<td>DR11-A Device Register</td>
</tr>
<tr>
<td>8</td>
<td>DR11-C General Purpose Device Interface</td>
</tr>
<tr>
<td>9</td>
<td>PA611 Reader</td>
</tr>
<tr>
<td>10</td>
<td>PA611 Punch</td>
</tr>
<tr>
<td>11</td>
<td>DT11 Bus Switch</td>
</tr>
<tr>
<td>12</td>
<td>DX11 IBM 360 Interface</td>
</tr>
<tr>
<td>13</td>
<td>DL11-C, D or E Asynchronous Line Interface</td>
</tr>
</tbody>
</table>

If any of the above devices are not included in the system, the vector address assignments move up to fill the vacancies. If a device is added to an existing system, its vector address must be inserted at the normal position and all other addresses must be moved accordingly. DEC software cannot test the system if the procedure is not followed.

A system containing a large number of communications devices will require vector addresses beyond 400; therefore, all communications devices, including the DN11, are supplied with Interrupt Control Module M7821 which contains seven bits in the vector address.
2.3.5 M7820 and M7821 Interrupt Modules

Early DN11 shipments included the M7820 Interrupt Module rather than the newer M7821 Interrupt Module that is included with later DN11 shipments.

The M7821 is a replacement for the M7820 that improves PDP-11 system performance. In almost all cases, it can be used directly in place of the M7820, without alteration of system hardware or software.

The significance of the jumpers that select the vector address differs between the two modules. In the M7821, a jumper must be cut out to generate a 0 and left in to generate a 1. This is the reverse of the M7820.

The M7821 module has a jumper in the line for bit 02. This has some significance with respect to module interchangeability depending on how the module is used.

A DN11 that uses the M7821 is wired as shown in the DN11 Block Diagram, drawing D-BD-DN11-0-0 Revision A. It is similar to the M7820 interconnection except that Unibus signal BUS NPR is connected to M7821 pin J1. Two additional conditions must be met which are not shown in the block diagram. The jumper associated with pin J1 on the M7821 module must be left in; and the bit 02 jumper must be left in. Under these conditions, the M7821 module operates like the M7820 module; that is, only one vector address is generated. For example, assume that vector address 400 is assigned to the first DN11 in the system. Each interrupt vector requires two words (four bytes) and vector addresses are constrained to even-word boundaries; that is, each vector must end in 4 or 0. In this example, vector 400 takes four bytes, 400, 401, 402 and 403, which is two words. The DN11 system configuration as described above, cannot generate vector 404 because bit 02, which controls the least significant bit of the octal address, cannot become a 1. If another DN11 is added to the system, the next available vector is 410. Multiple DN11s in a system must be assigned consecutive vectors that start on a modulo 10² boundary.

In a system with multiple DN11s, the M7821 modules can be used to generate XX4 vectors as well as XX0 vectors. This allows the same number of vectors in one half the memory locations required for the previously discussed configuration.

The connection between M7821 module pins N1 and D2 is removed and D2 is connected to +3V. On the M7821 module associated with the first DN11, remove the bit 02 jumper. This makes bit 02 a 0 and generates vector XX0. On the M7821 module, associated with the next DN11, leave the bit 02 jumper in place. This makes bit 02 a 1 and generates vector XX4. In this way, the otherwise unavailable XX4 vectors can be used. Refer to the PDP-11 Peripherals and Interfacing Handbook for more details concerning the M7820 and M7821 modules.
CHAPTER 3

DETAILED DESCRIPTION

3.1 INTRODUCTION

This chapter provides a detailed description of the operation of the DN11-AA Interface. A typical automatic calling sequence is described in detail (request, dial, answer and terminate). Signals are traced through the M7226 DN11 Control Module in detail, and through the M105 Address Selector Module and M7821 Interrupt Control Module in just enough detail to provide proper understanding of overall system operation.

A separate discussion is provided to explain the interrupt initiating logic and other circuits in the M7226 DN11 Control Module. A detailed bit assignment for the control and status register is included.

Basic descriptions of data in (DATI), data out (DATa), data out byte (DATOB), and interrupt bus transactions are also provided.

The various types of Bell 801 Automatic Calling Units and options are also discussed.

The text refers to the set of engineering drawings that is supplied separately. A drawing list is given in Chapter 1. Simplified logic diagrams are also used to support specific areas of discussion. The flip-flops used in the logic diagrams are shown logically as four output terminal devices. This symbology is used by DEC to allow direct reading of logic functions in detailed logic diagrams that show explicit electrical connections between the flip-flop outputs and other logic elements. Refer to Appendix B for an explanation of this concept.

3.2 BELL 801 AUTOMATIC CALLING UNIT

Two basic 801 ACUs are available: the 801A for use in dial pulse telephone networks (finger wheel dialing), and the 801C for use in TOUCH TONE® telephone networks (pushbutton dialing). Each model is described in a Bell System Data Communications document: Interface Specification—Data Auxiliary Set 801A and Interface Specification—Data Auxiliary Set 801C. These documents should be referenced for any information pertaining to the 801 ACUs. The purpose of this paragraph is to briefly describe the models and options as related to the detailed discussions which follow.

The DN11 unit will drive only those 801 ACUs that have an EIA Standard RS-232A voltage interface: this includes 801A5, 801A6, 801C1, and 801C2. Models 801A5 and 801C1 must receive the end-of-number (EON) code from the DN11 in order to switch the telephone line to the modem after dialing is complete. Models 801A6 and 801C2 contain an answer signal detection circuit that responds to the answer tone sent out by the called station to switch in the modem. Options are available for the answer detect models to allow the ACU to respond to the start or end of either a 2025-Hz signal or a 2225-Hz signal. Selection of these options is dictated by the choice of modem used in the system (see Bell 801 Interface Specification documents).

TOUCH TONE is a registered trademark of AT&T Company.
Normally, the 801 terminates the call after the modem is in the data mode when the program drops the Call Request (CRQ) signal. An option is available that allows the call to be terminated via the modem after it is in the data mode. In this case, dropping CRQ does not terminate the call, although it must be dropped sometime to release the 801 for the next call request.

Normally, the Abandon Call and Retry (ACR) timer in the 801 stops when the modem enters the data mode. An option is available that allows the timer to continue running. It will timeout and enable the ACR signal during data transmission, which is a convenience when the 801 is used in the end-of-number (EON) mode.

The effects of these options on the operation of the DN11 Interface are discussed in subsequent paragraphs.

3.3 M7226 DN11 CONTROL MODULE

3.3.1 Introduction

The M7226 is a double-height module that plugs into DN11 system unit locations E/F01, E/F02, E/F03, and E/F04. The major functional units of the module are:

a. control and status register
b. gating logic
c. interrupt control logic
d. receivers and drivers

3.3.2 Control and Status Register

The control and status register (CSR) is a 15-bit register that provides various control and status signals related to the operation of the DN11 Interface. Ten bits are read/write and five are read-only. Table 3-1 lists the bit assignments for the CSR.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Designation*</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Call Request (FCRQ)</td>
<td>Control lead to the 801. Set by the program to start the automatic calling sequence. Cleared by the program or INIT. Read/write.</td>
</tr>
<tr>
<td>01</td>
<td>Digit Present (FDPR)</td>
<td>Control lead to the 801. Must be set by the program after it loads the next digit in response to a PND from 801. It informs the 801 to continue dialing. It is automatically cleared by the DN11 logic when the 801 clears PND to indicate acceptance of the digit. Read/write.</td>
</tr>
<tr>
<td>02</td>
<td>Master Enable (MINAB)</td>
<td>Cleared by the program to disable and then set to reenable all four DN11 interrupts. This action is required to condition the M7820 interrupt control circuits to prevent multiple interrupts. This bit is connected only in line 1 of the DN11 Interface. Cleared by the program or INIT. Read/write.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table 3-1 (Cont)
#### Control and Status Register Bit Assignments

<table>
<thead>
<tr>
<th>Bit</th>
<th>Designation *</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>03</td>
<td>Maintenance (MAINT)</td>
<td>Set by the program to check out the DN11 during maintenance without an 801 connected. It uses the outputs of the digit flip-flops to represent the 801 response lines (PND, DSS, PWI, and ACR) for testing purposes. It also clears the CRQ signal to the 801 and asserts FDLO (bit D12). Cleared by the program and INIT. Read/write.</td>
</tr>
<tr>
<td>04</td>
<td>Present Next Digit (FPND)</td>
<td>Control lead from the 801. It requests the program to load another digit during dialing. It sets DONE to initiate an interrupt. It is cleared by the 801 when the digit is accepted (after DPR is set) and remains cleared for a short interval before being set for the next request. Read-only.</td>
</tr>
<tr>
<td>05</td>
<td>Data Set Status (FDSS)</td>
<td>Control lead from the 801. It indicates that the called party has answered and the associated data line now has control of the line. It sets DONE to initiate an interrupt. It remains set until the call is terminated or the Data Terminal Ready signal is cleared. Read-only.</td>
</tr>
<tr>
<td>06</td>
<td>Interrupt Enable (INTENB)</td>
<td>Set by the program to allow an interrupt to be initiated when DONE is set by PND, DSS, PWI, or ACR provided the Master Enable bit is set. Cleared by the program and INIT. Read/write.</td>
</tr>
</tbody>
</table>
| 07  | DONE | Set by the DN11 logic to initiate an interrupt, providing the Interrupt Enable and Master Enable bits are set. The following conditions from the 801 set DONE:

   a. Positive transition of PND after CRQ is set or previous DPR is set.
   b. Positive transition of DSS after last DPR or EON.
   c. Positive transition of ACR at any time.
   d. Negative transition of PWI if a call is in progress (CRQ = 1).

Cleared by the program or INIT. Read/write. |
| 08–11 | Digits (NB01, NB02, NB04, and NB08) | Control leads to the 801. Set by the program to represent the digit to be dialed in 4-bit BCD format. Use data line bits 8 through 11 which are the low-order bits of the high byte. In Maintenance mode, these bits are switched to the 801 response lines (PND, DSS, PWI, and ACR, respectively) for testing purposes. Cleared by the program or INIT. Read/write. |
| 12  | Data Line Occupied (FDLO) | Control lead from the 801. Set by the 801 when it is using the telephone line. Allows the program to check for termination of a call before initiating another call request. Read-only. |
| 13  | Not used | |

(continued on next page)
### Table 3-1 (Cont)

Control and Status Register Bit Assignments

<table>
<thead>
<tr>
<th>Bit</th>
<th>Designation *</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>Abandon Call and Retry (FACR)</td>
<td>Control lead from the 801, set at timeout of the 801 internal timer which is reset when PND is set. It is used to detect wrong numbers and busy lines. Sets DONE to initiate an interrupt. Normally inhibited by DSS, except when 801 contains option to allow timer to run during data transmission. Read-only.</td>
</tr>
<tr>
<td>15</td>
<td>Power Off (FPWOF)</td>
<td>Control lead from the 801. Set by the 801 when it loses power (PWI goes low). Sets DONE to initiate an interrupt if FCRQ = 1. Read-only.</td>
</tr>
</tbody>
</table>

*Signals identified as FXXX are buffered Unibus signals corresponding to the function line signals XXX between the DN11 and ACU.

Each read-only bit uses one 8881 two-input Unibus driver. One input is the data and the other is the enabling signal that is generated during a data input transaction (DATI). When enabled, the driver places its input information on the Unibus data line. The DATI is a read operation, and in this case, the PDP-11 processor is reading the contents of the control and status register.

Each read/write bit uses one 7474 D-type flip-flop, one 380 Unibus receiver, and one 8881 Unibus driver. A typical read/write bit is shown in Figure 3-1. The read operation is the same as that described above. Enabling signal IN SEL H is asserted and the output of flip-flop E18 is placed on the Unibus data line D02L. During a write operation (DATO), the program asserts Unibus data line D02L which is sent to the D-input of flip-flop E18 via Unibus receiver E17. Signal LO SEL H is generated during the DATO operation and clocks the data at the flip-flop input to its outputs. The flip-flop is cleared by INIT L which is generated during the power-up sequence of the PDP-11 processor. Refer to drawing D-CS-M7226-0-1 (sheets 2 and 3) for the complete configuration of the control and status register.

![Figure 3-1 Typical Status Register Read/Write Bit (D02), Simplified Logic Diagram](image)

### 3.3.3 Gating Logic

The gating logic (Figure 3-2) generates signals that are used to enable the control and status register (CSR) Unibus drivers and clock the CSR flip-flops. Selection is controlled by the input signals which come from the M105...
Address Selector Module. The selection signal (SEL H) is asserted when the address of the DN11 control module (M7226) is decoded on the M105 Address Selector. The other three signals are asserted with respect to the type of data transfer bus transaction being performed. Signal selection is shown in Table 3-2.

Figure 3-2 Gating Logic Diagram

Table 3-2
Gating Logic Signal Selection

<table>
<thead>
<tr>
<th>Bus Transaction</th>
<th>Function</th>
<th>Input Signal</th>
<th>Control Signal Asserted</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATI</td>
<td>Reads all bits of CSR</td>
<td>IN H</td>
<td>IN SEL H</td>
<td>Enables all CSR drivers</td>
<td></td>
</tr>
<tr>
<td>DATO</td>
<td>Writes word into CSR</td>
<td>LO OUT H</td>
<td>LO SEL H</td>
<td>Clocks all 10 CSR flip-flops</td>
<td></td>
</tr>
<tr>
<td>DATOB</td>
<td>Writes high byte into CSR. Actually affects four lower bits (8–11) of high byte only.</td>
<td>HI OUT H</td>
<td>HI SEL H</td>
<td>Clocks four CSR digit flip-flops only</td>
<td></td>
</tr>
</tbody>
</table>

The selection signal (SEL H) from the M105 Address Selector is actually one of four select signals generated by decoding a particular address. The DN11 addresses start at 775200: this address is used as an example in Figure 3-3.

Figure 3-3 Address Word for Line 1
The first five digits of the address (77520) indicate that the DN11-AA Interface has been selected. Bits 1 and 2 of the last digit determine which line (or M7226 module) has been selected. Assume that all four lines are used in this example. The addresses must be assigned in order starting at 775200 for line 1; therefore, the respective addresses for lines 2, 3, and 4 are 775202, 775204, and 775206. The binary representation of the last digit (0, 2, 4, and 6) always ends with a 0: only bits 1 and 2 change. Therefore, address lines A01 and A02 determine which line (or M7226 module) is addressed. Address line A00 is controlled by the program to select a byte (8 bits) instead of a word (16 bits).

Address lines A (17:13) must be all 1s to conform to the address bounds for device registers. Decoding of lines (12:03) is determined by jumpers on the M105 Address Selector (drawing C-CS-M105-0-1). If a line contains a jumper, the M105 searches for a 0 on that line. If there is no jumper, the M105 searches for a 1. In this example, jumpers would be installed in bit positions 10, 8, 6, 5, 4, and 3. Table 3-3 shows the correlation between the select signals and the DN11 control lines.

<table>
<thead>
<tr>
<th>Device Address</th>
<th>Lines A (02:01)</th>
<th>Select Signal True (+3V)</th>
<th>DN11 Control Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>775200</td>
<td>00</td>
<td>SELECT 0</td>
<td>Line 1</td>
</tr>
<tr>
<td>775202</td>
<td>01</td>
<td>SELECT 2</td>
<td>Line 2</td>
</tr>
<tr>
<td>775204</td>
<td>10</td>
<td>SELECT 4</td>
<td>Line 3</td>
</tr>
<tr>
<td>775206</td>
<td>11</td>
<td>SELECT 6</td>
<td>Line 4</td>
</tr>
</tbody>
</table>

Address line A00 and control lines C01 and C00 determine the type of bus data transfer to be implemented by the program.

<table>
<thead>
<tr>
<th>Mode Control C (01:00)</th>
<th>Byte Control A00</th>
<th>Bus Data Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>X</td>
<td>DATI</td>
</tr>
<tr>
<td>10</td>
<td>X</td>
<td>DATO</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>DATOB (High Byte)</td>
</tr>
</tbody>
</table>

3.3.4 Interrupt Control Logic

The interrupt control logic (drawing D-CS-M7226-0-1, sheet 3) allows one of four 801 response signals to set the DONE flip-flop (drawing D-CS-M7226-0-1, sheet 2) and initiate an interrupt provided the Master Enable (MINAB) bit and Interrupt Enable (INTENB) bit are set.

A simplified diagram of the logic is shown in Figure 3-4. The response signals from the 801 (DSS, ACR, PWI, and PND) are sent to type 1489 converter-receivers which convert the 801 logic levels to TTL levels. A high at the 1489 input is +15V and is converted to 0V (low) at the output; a low is -15V and is converted to +3V (high). The four response signals from the converters are one set of inputs to the 6266 two-input 4-bit multiplexer. The other set consists of the four digit flip-flop outputs FNB02 (1) H, FNB08 (1) H, FNB04 (0) H, and FNB01 (1) H. The control signal for the multiplexer is MAINT (1) H which is an output of the maintenance flip-flop. During normal operation, this flip-flop is cleared and MAINT (1) H is low. In this state, the response signals are passed through. The logic level of the response signal at the converter-receiver input appears at the associated multiplexer output. For example, if DSS is high at pin 10 of the converter-receiver E9, multiplexer output pin 13
Figure 3-4 Interrupt Control Circuit, Simplified Logic Diagram
is high also. In the maintenance mode, MAINT (1) H is high and the digit flip-flop outputs are passed through. The logic levels of these signals at the multiplexer inputs (pins 14, 11, 5, and 2) appear at the corresponding multiplexer outputs (pins 13, 12, 4, and 3). Figure 3-5 shows one bit (PND) of the multiplexer with the associated truth table.

Each multiplexer output is sent to a negative-edge triggered one-shot or pulser. Each pulser consists of a 7404 inverter, a discrete RCD network, and a 7402 NOR gate. Two pulsers share a single 2-input NOR gate. A positive-to-negative transition (negative edge) at the input of the pulser produces a short negative pulse at the output. A negative-to-positive transition (positive edge) at the input has no effect. During steady state conditions, the pulser output is high, regardless of the input level. A pulser and timing diagram are shown in Figure 3-6.

The inputs to three pulsers (DSS, ACR, and PND) are buffered by an inverter to provide the proper signal transition polarity. It is desired to trigger a pulser when DSS, ACR, or PND go high or when PWI goes low. When any one of the four pulsers is triggered, the output (pin 3) of gate E4 is driven high. This signal is ANDed with FCRQ H, which is high when a call is in process, to generate SET DONE L which sets the DONE flip-flop via its preset input.
In summary, a response event from the 801 is traced through the logic (drawing D-CS-M7226-0-1, sheet 3). Assume that a call is in process, which means that the CRQ flip-flop is set and FCRQ (1) H is asserted. This qualifying signal is sent to pin 5 of NAND gate E4; however, the other input of this gate (pin 4) is low, which disables SET DONE L. This input (pin 4) is low because the pulser outputs (E5 pin 4 and E5 pin 1) are both high, which produces a low on pin 3 of negated-input OR gate E4. At this point, DSS, ACR, and PND are low and PWI is high. The input to each pulser is high. Assume that the 801 requests another digit to be dialed by asserting PND H. This signal is reflected at the output of the multiplexer (E10 pin 3) as a high. It is inverted by E11 and appears as a low (FPND L) at the input of the pulser, which triggers it. The pulser output (E5 pin 1) is pulsed low and generates SET DONE L via the two E4 gates as described previously.
3.4 AUTOMATIC CALL SEQUENCE

3.4.1 Introduction

The automatic call sequence is described in four sections: dialing, answering, retry if busy, and termination. The signals are traced through the DN11 control module logic (drawings D-CS-M7226-0-1, sheets 2 and 3) but the details of the gating logic and interrupt control logic are not repeated.

3.4.2 Dialing

Prior to issuing a call request, the program reads the control and status register to determine if FDLO L (bit D 12) and FPWOF L (bit D15) are asserted. If FDLO L is asserted, the telephone line is busy and the call request cannot be honored. If FPWOF L is asserted, power is off to the 801 and it is inoperative.

If the telephone line is in use, the 801 asserts DLO H. It enters the DN11 control module at pin AM2 (sheet 3) which is the input (pin 10) of converter-receiver E13. This signal is converted and inverted by E13 and sent as a low to pin 9 of negated-input OR gate E14. The other input of this gate is MAINT (1) L and it is high because the maintenance flip-flop is cleared. The output of E14 (pin 8) is high and is sent to pin 3 of Unibus driver E15. The output of this gate is FDLO L and is asserted as bus data bit D12 when the driver is enabled by IN SEL H during a read operation (DATI).

If power is off to the 801, PWI is low. It enters at pin AN2 and appears at multiplexer output pin 4 as a low. It is inverted by E17 (pin 4) and sent to pin 12 of Unibus driver E15. The output of this gate is FPWOF L and is asserted as bus data bit D15 during a read operation.

If both FDLO L and FPWOF L are not asserted, the program sets CRQ which is the call request bit D00. Bits D02 (MINAB) and D06 (INTENB) are also set to allow an interrupt to be generated when the DONE flip-flop is set. These bits are set during a write operation (DATO) that generates LO SEL H. This signal clocks the flip-flop associated with these bits. The program sets CRQ by asserting it on the bus (D00 L). It is sent to the D-input of the flip-flop E19 (FCRQ) via Unibus receiver E17 pin 13 (sheet 2). When the FCRQ flip-flop is clocked, output FCRQ (1) H is high. This signal is sent to pin 13 of NAND gate E14 to be ANDed with MAINT (0) H, which is high because the maintenance flip-flop (E19 MAINT) is cleared. The low output of E14 is inverted by converter-driver E12 and its output is the asserted signal CRQ H converted to 801 logic (high = logic 1 = +15V).

The 801 receives the CRQ H signal, seizes the telephone line, and asserts DLO H to the DN11 to indicate that the line is busy. The 801 also asserts PND H which tells the DN11 that it is ready to receive the first digit for dialing. The DN11 receives the PND H signal at pin AK2 (sheet 3). It is multiplexed and triggers a pulser to generate SET DONE L which sets the DONE flip-flop E22 (sheet 2).

The 1-output of the DONE flip-flop and the 1-output of the INTENB flip-flop are ANDed at NAND gate E24. Both of these signals are high, so the output of E24 is low and is called ID L. This signal is sent to NAND gate module M117 and is inverted and ANDed with MINAB H in the M7820 Interrupt Control Module to initiate an interrupt to the PDP-11 processor (drawing D-BD-DN11-0-01).

The processor responds to the interrupt by loading a 4-bit BCD digit in bits D08 through D11. A DATOB operation is used to load these four low-order bits of the high byte. These bits are sent, via Unibus receiver E6, to the D-inputs of four flip-flops: E7 (FNBO1), E7 (FNBO2), E2 (FNBO4), and E2 (FNBO8). The DATOB operation generates HI SEL L which is inverted by E20 and clocks all four flip-flops (sheet 3). The outputs of these flip-flops, identified as FNB01 (1), FNB02 (1), FNB04 (0), and FNB08 (1), are sent to 1488L converter-driver E1 (sheet 2). The signals are inverted and converted to 801 logic levels. They are sent to the 801 as a 4-bit BCD digit NB01, NB02, NB04 and NB08, with NB08 as the most significant bit. After the digit flip-flops are loaded,
the program sets the Digit Present (DPR) bit D01. This bit is loaded via Unibus receiver E17 pin 2 to the D-input of the FDPR flip-flop. The flip-flop is clocked by LO SEL H and output FDPR (1) L is sent to 1488L converter-driver E12. This signal is low because the flip-flop is set. It is inverted to 801 logic levels and sent to the 801 as DPR H. This signal tells the 801 that the digit is now legitimate and to continue dialing.

After the 801 dials the digit, it clears PND. At the DN11 control module, multiplexer output E10 pin 3 (FPND H) is now low (sheet 3). This signal is sent to the clear input (pin 1) of the FDPR flip-flop which clears it and drops the Digit Present (DPR H) signal to the 801. PND remains cleared for a short interval before being asserted for the next request. With each PND H assertion, the sequence is repeated and it continues until all digits have been dialed.

3.4.3 Answering

After the last digit has been dialed, the 801 asserts PND H again. The program responds in one of two ways, depending on the type of answer detecting option incorporated in the 801.

If the 801 contains the answer detection circuitry, the program ignores the last PND H signal and holds DPR cleared. The called modem answers the 801 with a tone signal which the 801 recognizes as a legitimate answer. The 801 gives the telephone line back to the associated modem and asserts DSS H to the DN11 to indicate that the modem is in the data mode. DSS H is sent to the DN11 at pin AK1 (sheet 3). It is multiplexed and triggers a pulser to generate SET DONE L which sets the DONE flip-flop and initiates an interrupt. The program reads bit D05 (DSS) to indicate that the modem is in the data mode.

If the 801 does not contain the answer detection circuitry, the program responds to PND H by sending the digit 1210 and DPR H to the 801. This digit is recognized by the 801 as the end-of-number (EON) code and it immediately gives the telephone line back to the modem. The 801 drops PND H which clears DPR H in the DNII. It also asserts DSS H which has the same effect in this case as described above. In the EON mode, an additional option is available that allows the ACR timer in the 801 to run, rather than reset, when PND H is dropped. If allowed to run, the timer times out and asserts ACR H during data transmission. The ACR H signal is sent to the DN11 where it generates SET DONE L which initiates an interrupt. This interrupt occurs when an answer should have been received. The program can read this indication at bit D14 (FACR). The EON option is normally used with modems that provide their own “hand-shaking” routine so it is not necessary for the 801 to detect the answer signal.

3.4.4 Abandon Call and Retry

The 801 contains Abandon Call and Retry (ACR) timing circuitry to help prevent long delays due to a wrong number, busy number, or any condition resulting in an incomplete call. The ACR timer starts when CRQ is asserted. The timeout period is normally set for 25 seconds. When the timer is running, it resets to 0 and starts over every time the 801 clears PND H. During a call, if the preset time from the last cleared PND H is exceeded, the Abandon Call and Retry (ACR H) signal is asserted by the 801.

ACR H is sent to the DN11 and initiates an interrupt which indicates an error during the call sequence. The program reads this indication at bit D14 (FACR) and abandons the call by clearing CRQ H to the 801. This action drops ACR H. The program retries the call by asserting FCRQ after first checking that FDLO and FPWOF are not asserted.
3.4.5 Call Termination

The call request (FCRQ) must be asserted to originate the call and must remain on until the call is to be terminated. If FCRQ is cleared at any time during dialing or data transmission, the 801 will go on-hook, thus terminating the call. Therefore, after data transmission, the program terminates the call locally by clearing FCRQ (bit D00). The FCRQ flip-flop is cleared and output FCRQ (1) H is low, which clears CRQ H to the 801 via gates E14 pin 11 and E12 pin 8 (sheet 2).

An option is provided to allow call termination via modem control. When the 801 asserts DSS H, the modem is in control and clearing FCRQ H has no effect on the operation. After data transmission, the modem terminates the call in the manner prescribed for the particular model used (such as clearing the modem Data Terminal Ready signal). FCRQ H must be cleared by the program sometime between assertion of DSS H and the modem hanging up to release the 801 for the next call when DLO H is cleared.

3.5 MAINTENANCE MODE

The Maintenance bit (D03) can be set by the program to check out most circuits in the DNII control module without an 801 connected.

When set, it clears CRQ H to the 801 and asserts bit D12 (FDLO L). It also allows the outputs of the four digit flip-flops to be multiplexed in place of the response signals.

To initiate the maintenance mode, the program sets the maintenance bit (D03). The maintenance flip-flop (E19 MAINT) is set and its output can be read at the output (pin 4) of Unibus driver E16. Output MAINT (0) H of the MAINT flip-flop is sent to pin 12 of NAND gate E14 which disables the gate regardless of the state of the other input [FCRQ (1) H]. The high output of this gate drives the output (pin 8) of E12 low, which is the disabled state of CRQ to the 801 (sheet 2). The CRQ bit can still be set by the program but it does not generate a CRQ H signal to the 801. Output MAINT (1) L of the MAINT flip-flop is sent to pin 10 of negated-input OR gate E14 (sheet 3). This signal is low because the MAINT flip-flop is set and it enables the gate (pin 8 is high). The gate output is MAINT (1) H which is sent to Unibus driver E15 to be read on bus data bit D12 as FDLO L. This bit is asserted just as it is when the actual DLO H signal is sent from the 801.

Output MAINT (1) H of the MAINT flip-flop is sent to the control input (pin 9) of the multiplexer (sheet 3). This signal is high because the MAINT flip-flop is set and it allows the digit flip-flop to be multiplexed. The rest of the interrupt circuitry responds to these signals just as if they were the actual response signals from the 801. Each digit flip-flop output corresponds to a particular response signal. The program can set a digit flip-flop to initiate an interrupt just as if the associated response signal had been asserted. Table 3-4 shows the relationship between the response signals and the digit flip-flops.

<table>
<thead>
<tr>
<th>Write Bit</th>
<th>Digit Flip-Flop Output</th>
<th>Response Signal Represented</th>
<th>Read Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>D08</td>
<td>FNB01 (1) H</td>
<td>PND H</td>
<td>D08 (FPND L)</td>
</tr>
<tr>
<td>D09</td>
<td>FNB02 (1) H</td>
<td>DSS H</td>
<td>D05 (FDSS L)</td>
</tr>
<tr>
<td>D10</td>
<td>FNB04 (0) H</td>
<td>PWI L</td>
<td>D15 (FPWOF L)</td>
</tr>
<tr>
<td>D11</td>
<td>FNB08 (1) H</td>
<td>ACR H</td>
<td>D14 (FACR L)</td>
</tr>
</tbody>
</table>

Table 3-4 Response Signal Representation by Digit Flip-Flops
For example, assume that it is desired to check out the circuitry associated with the Present Next Digit (PND) response signal. The program sets bit D08 (NB01) which allows digit flip-flop E7 (FNBO1) to represent response signal PND H. The program can also set bit D00 (CRQ) to check the generation of SET DONE L. With bit D08 (NB01) set, the FNB01 flip-flop is clocked to the reset state. Output FNB01 (1) H is high and is sent to input pin 2 of the multiplexer. It appears at the multiplexer output (E10 pin 3) as FPND H. It is inverted by E11 and triggers the pulser which asserts SET DONE L, provided the CRQ bit is set to give FCRQ (1) H = 1 at pin 5 of gate E4.

3.6 BUS DATA TRANSFER OPERATIONS

3.6.1 Introduction

To assist in understanding the overall system operation, the three bus data transfer operations used with the DN11-AA Interface are described. They are: data in (DATI), data out (DATO), and data out byte (DATOB). Except when the DN11 is generating an interrupt, it operates as a slave device with the PDP-11 processor as master.

The text references the following drawings:

a. DN11 Block Diagram D-BD-DN11-0-01; hereafter referred to as DN11-BD.

b. DN11 Control D-CS-M7226-0-1; hereafter referred to as M7226, sheets 2 and 3.

c. M105 Address Selector C-CS-M105-0-1; hereafter referred to as M105.

3.6.2 DATI Operation

As an example of a DATI operation, assume that the processor desires to read the contents of the control and status register (CSR) associated with the DN11 control module installed in line 1.

a. The processor places the address of the CSR (775200) on address lines A(17:00) and asserts C01 = C00 = 0. These signals are sent to the M105 Address Selector (DN11-BD and M105). The control lines (C01 and C00) and address line A00 are decoded and IN H is asserted (M105). IN H is sent from the M105 Address Selector to the gating logic in each DN11 control module (M7226, sheet 2). Address lines (17:01) have also been decoded but no select signals are generated because the processor has not yet asserted Master Sync (MSYN L).

b. If the bus is free, Slave Sync (SSYN L) is clear and the processor asserts MSYN L to the address selector module. This signal, along with decoded lines A (17:01), enables SELECT 0 H to the DN11 control module in line 1. This signal is ANDed with IN H to generate IN SEL H which strobes the CSR data to bus data lines D (15:00) (M7226, sheets 2 and 3). MSYN L also asserts SSYN L from the address selector module.

c. The processor receives the data and SSYN L. It clears MSYN L and then clears the A and C lines.

d. The address selector module receives the cleared MSYN L which clears its SSYN L and, along with the cleared A and C lines, clears IN H and SELECT 0 H which in turn clear the D lines. The bus is now clear for other use.

e. The processor receives the cleared SSYN L which signifies the end of the current bus transaction.
3.6.3 DATO Operation

As an example of a DATO operation, assume that the processor desires to write information into several bits of the CSR to instruct the DN11 to perform a particular operation.

a. The processor places the address of the CSR (775200) on address lines A (17:00); the data on the data lines D (15:00); and asserts C01 = 1, C00 = 0. The A and C lines go to the address selector module and the D lines go to the DN11 control module installed in line 1. The address selector module decodes the control lines and address line A00 which asserts OUT LO H and OUT HI H (M105). These two signals are sent from the address selector module to the gating logic in each DN11 control module (M7226, sheet 2). Address lines A (17:01) have also been decoded but no select signals are generated because the processor has not yet asserted MSYN L.

b. If the bus is free, SSYN L is clear and the processor asserts MSYN L to the address selector module. This signal, along with decoded lines A (17:01), enables SELECT 0 to the DN11 control module in line 1. This signal is ANDed with OUT LO H and OUT HI H to generate HI SEL L and LO SEL H which clock all the flip-flops in the CSR. The D-inputs of these flip-flops contain the information on data lines D (15:00) (M7226, sheets 2 and 3). MSYN L also asserts SSYN L from the address selector module.

c. The processor receives SSYN L and clears MSYN L. It also clears the A, C, and D lines.

d. The address selector module receives the cleared MSYN L which clears its SSYN L and, along with the cleared A and C lines, clears OUT LO H, OUT HI H, and SELECT 0 H. The bus is now clear for other use.

e. The processor receives the cleared SSYN L which signifies the end of the current bus transaction.

3.6.4 DATOB Operation

The DATOB operation is similar to the DATO operation described in Paragraph 3.6.3 except that the DN11 accepts a single byte instead of a complete word. This operation is used when the digit flip-flops are loaded. The processor asserts C01 = C00 = 1 to select the DATOB operation. The state of address line A00 determines which byte is used. In this case, the high byte D (15:8) is always used (A00 = 1). Actually, only the four low-order bits D (11:8) are used; the four high-order bits are read-only, so their value is irrelevant. During the decoding process, the address selector module asserts SELECT 0 H and OUT HI H which allows only the four digit flip-flops to be clocked.

The above examples are simplified in that they do not describe the built-in delays that are required to compensate for data deskewing, decoding, etc. Refer to the PDP-11 Peripherals and Interfacing Handbook for timing details.

3.7 INTERRUPT TRANSACTION

3.7.1 Introduction

The interrupt control circuitry on the DN11 control module allows one of four response signals (DSS, ACR, PWI, or PND) to set the DONE flip-flop. This is only one step in qualifying the M7821 Interrupt Control Module to conduct the interrupt transaction. The program must also set Interrupt Enable (INTENB) bit D06 and Master Interrupt Enable (MINAB) bit D02 to activate the M7821 module. When the INTENB flip-flop is set, its 1-output is ANDed with the 1-output of the DONE flip-flop to assert ID L (M7226, sheet 2). The ID L signal from the DN11 control module that is requesting the interrupt is sent to the M117 NAND gate module.
The signal is inverted and sent to connector pin U1 of the M7821 Interrupt Control Module. This pin is one input of a NAND gate and the other input (connector pin V1) is MINAB H. The interrupt sequence is initiated when both signals are high (DN11-BD).

Each DN11 control module generates an ID signal but only line 1 contains a Master Interrupt Enable (MINAB) signal. A control module must be plugged into line 1 and programmed in order to operate any line. MINAB is used to clear all the interrupts on all four lines at once to allow the M7821 Interrupt Control Module to respond to new interrupts.

The M7821 Interrupt Control Module permits the DN11 Interface to gain control of the bus (become bus master) and perform an interrupt transaction. The M7821 sends a vector address to the processor via the bus data lines. At the end of the interrupt transaction, the processor goes into the interrupt service routine at the specified vector address. Most interrupts are generated by PND which requests a digit to be dialed. The interrupts generated by DSS, ACR, and PWI are to inform the processor of certain conditions or errors. DSS indicates that the modem is in the data mode; ACR indicates that the 801 ACR timer has timed out (usually an error during dialing); and PWI indicates that the 801 has lost power and is inoperative.

3.7.2 Interrupt Operational Sequence

In this example, assume that the DN11 control module in line 1 is requesting an interrupt in response to PND H from the 801.

a. MINAB and INTENB have been asserted by the program. A call is in process and the DONE flip-flop has been set by PND H from the 801. Signal ID L has been generated, inverted by the M117 NAND gate module and sent to pin U1 of the M7821 Interrupt Control Module. Signal MINAB H has been sent to pin V1 of the M7821. Pins U1 and V1 are inputs to the A master control section of the M7821. The B master control section of the M7821 is not used.

b. Signals ID H and MINAB H are both high which asserts BUS A BR L. This is the bus request signal and is a level 4 (BR4) for the DN11. It is sent to the processor as a request for bus mastership.

c. The processor examines the bus request (BUS A BR L) and, if it has the highest priority, Bus Grant signal BUS A BG IN H is asserted provided BUS SACK L is cleared.

d. BUS A BG IN H enters the M7821 and is blocked in the A master control logic; that is, BUS A BG OUT H is driven low. This prevents the asserted BG signal from reaching any following devices on the Unibus. Asserting BUS A BG IN H, causes BUS A BR L to be cleared and BUS SACK L to be asserted which acknowledges the grant.

e. The processor receives BUS SACK L and clears BUS A BG IN which prevents the issuance of further grants from the processor during this interrupt transaction.

f. When the current bus master completes its transaction, it clears BUS BBSY L and BUS SSYN L. In response to this action, the M7821 asserts BUS BBSY L and BUS SSYN L which clears BUS SACK L. Signal A MASTER L is also asserted which enables the interrupt signal BUS INTR L and places the vector address on the Unibus data lines BUS D02 L – BUS D08 L. This is accomplished in the DN11 by connecting pin N1 (A MASTER L) to pin R2 (A START INTR L) and pin D2 (VECTOR BIT 02 H) on the M7821 module. Pin P2 (B START INTR L) is held high because the B master control logic is not used.

g. The processor receives BUS INTR L, reads the vector address, and responds by asserting BUS SSYN L.

(continued on next page)
h. In response to BUS SSYN L, the M7821 asserts A INTR DONE H (pin L2) which is connected to A MASTER CLEAR H (pin R1) to clear BUS BBSY L, A MASTER L, BUS INTR L, and the vector address. This constitutes active release of the bus to the processor which clears BUS SSYN L when it receives the cleared BUS INTR L signal. The processor goes to the interrupt service routine at the specified vector address.

i. At this point, MINAB H, INTENB H, and DONE H are still set but further grants are inhibited because the gate in the M7821 module that asserts BUS A BR L is disabled. In order to make another request, the program must clear MINAB H to remove the disabling signal. Reasserting MINAB H qualifies the M7821 module to process another interrupt request.
The software package that is available for controlling the DN11 Interface is COMTEX-11 DN11 ISR/TAP. COMTEX-11 (Communications Oriented Multi-Task Executive) is a communications software package for the PDP-11 family of computers.

This chapter provides a sample program for control of a DN11. It is similar but not identical to COMTEX-11 DN11 ISR/TAP. Prerequisites for operation include a PDP-11/20 computer and 4K of core memory (8K to assemble the program). The terminal used in the system must supply a Terminal Ready signal. An explanation of the program parameters, completion flags, and line table is shown below. This is followed by a program listing.

Initialization Parameters
- Line number (byte)
- Null (byte)
- Address for line table (word)
- Initialization error indicator (word)

Dialing Parameters
- Line number (byte)
- Hand-shaking/EON code indicator (byte)
  -1: Hand-shaking
  0: End-of-number code
- Address of telephone number (word)
- Length of telephone number (byte)
- Null (byte)
- Address in which to place completion message (word)

Completion Message Parameters
- Line number (byte)
- 204 (byte)
- Address of telephone number (word)
- Completion flags (word)

(continued on next page)
Completion Flags

Bit 0
  0: No Y-option (no second completion entry)
  1: Y-option (ACR interrupt after DSS interrupt; address of telephone number is zeroed)

Bit 1
  0: EON code ended dialing
  1: Hand-shaking mode assumed

Bit 2
  0: No ACR timeout
  1: ACR timed out

Bit 3
  0: No power failure
  1: Power failed

Line Table

Word 0: Null
Word 1: Address of hardware register
Word 2: Address of next digit to send
Word 3:
  Low Byte: Count of digits yet to send
  High Byte:
    0,1: EON code
    -1, -2: Hand-shaking
Word 4: Low Byte
  1: Y-option
  High Byte
  1: Z-option
Word 5: Address of first digit
THE DN11 AUTOMATIC DIALER
VERSION 000X
COPYRIGHT 1971, 1972, DIGITAL EQUIPMENT CORPORATION
1146 MAIN STREET, MAYNARD, MASS. 01754

*TITLE DN11

000010 R0%0
000001 R1%1
000002 R2%2
000003 R3%3
000004 R4%4
000005 R5%5
000006 SP%6
000007 PC%7

177776 PS=177776
00240 NUF=240

000254 CLZB=254
000255 CLZC=255
000274 SEZB=274
000271 SEZC=271

175200 DNSW=175200

ADDRESS OF THE FIRST
DN11 STATUS/DATA REGISTER

NUMBER OF DIGITS ALLOWED
PER TELEPHONE NUMBER.
IF Z=OPTION INDICATORS ARE SET AT ASSEMBLY TIME
BY CHANGING THE BYTE IN THE ISR TABLE IMMEDIATELY
AFTER THE ASSOCIATED LINE NUMBER.

000204 C,NCPL=200+4

000214...#140

C,NTRY MOV R4,=(SP) JSAVE
MOV R5,=(SP) JTHREE OTHER
MOV R2,=(SP) JREGISTERS

000214 MOV #4,R2 JFOUR LINES TO TEST.
000214 MOV (R5)+,R4

000242 #02714 C,NTRY1 BIT #200,#R4 JRestart ON THIS LINE?
000230 010546 MOV R4,=(SP) JSAVE
MOV R5,=(SP) JTHREE OTHER
MOV R2,=(SP) JREGISTERS

000242 MOV #4,R5 JUPDATE FOR NEXT LINE.
000242 MOV #2,R4

000242 DEC R2 JALL LINES TESTED?
000242 BNE C,NTRY1 JNO, GO TEST NEXT.

000242 BR C,NRET JYES, FALSE INTERRUPT.
000066 016D02 C_NSET1 MOV 2(R5),R2  ; STORE LINE TABLE ADDRESS.
000072 011403 MOV $R4,R3  ; SAVE REGISTER CONTENTS.
000074 42714 BIC $7600, R4  ; CLEAR THE INTERRUPT & DIGIT.
000100 032703 BIT $C.NALL,R3  ; SPECIAL INTERRUPT?
000104 001030 BNE C_NCMP  ; YES, TEST FOR A COMPLETED CALL, ETC.
000106 105762 TSTB C_NCNT(R2)  ; NUMBER DIALED?
000112 001412 BEQ C_NEND  ; YES.
000114 105352 DEC R C_NCNT(R2)  ; UPDATE COUNTER (IN ADVANCE).
000120 117254 MOV R $C.NADD(R2),1(R4)  ; TRANSMIT NEXT DIGIT.
000126 052502 INC C_NADV(R2)  ; UPDATE POINTER
000132 052702 BIS $C.NUPR,$R4  ; SET DIGIT=PRESENT BIT
000136 005511 BR C_NRET  ; IGO EXIT.
000140 105762 C_NEND1 TSTB C_NEUN(RR)  ; SEND "EON" CODE?
000144 001156 BNE C_NRET  ; NO, 1) ALREADY SENT FOR 2) UNNECESSARY.
000146 032714 BIT $C.NMAI,$R4  ; IN MAINTENANCE MODE?
000152 001153 BNE C_NRET  ; YES, NO NEED TO SEND EON.
000154 112764 MOV $R14,1(R4)  ; SEND "END-OF-NUMBER" INDICATOR
000158 105762 INC C_NEUN(R2)  ; SET "EON SENT" FLAG.
000166 052703 BIS $C.NUPR,$R4  ; SET DIGIT=PRESENT BIT.
000172 004731 BR C_NRET  ; IGO EXIT.
000174 012746 C_NPWRI MOV $C.NPOR,(SP)  ; STORE "POWER FAILURE" INDICATOR
000203 001153 BR C_NMEES  ; IGO FREE LINE AND SEND MESSAGE.
000202 100774 C_NCMPI BHI C_NPKR  ; POWER FAILURE.
000204 032703 BIT $C.NACR,R3  ; ABANDON CALL & RETRY BIT SET?
000212 001403 BNE C_NDUN  ; NO, DATA=SET STATUS
000212 012746 C_NGUPI MOV $C.NBAD,(SP)  ; STORE "ACR TIMER INTERRUPT" IN
000220 000001 BR +4  ; STORE CONDITIONAL INDICATORS, AND SEND MESSAGE.
000222 005846 C_NDONI CLR -(SP)  ; CLEAR FOR BIT INDICATORS.
000222 105762 TSTB C_NEUN(R2)  ; HANDSHAKING MODE?
000226 000002 BPL C_NDMO  ; NO

---

This is a computer assembly code with instructions for controlling various operations based on specific conditions. The code is designed to handle different scenarios such as line status, register management, and error handling. Each line represents a specific operation, and the comments provide context on the purpose of each instruction.
000230 052716 BIS #C, NMND,(SP) YES, STORE BIT
000234 105762 C,NDN01 TSTB C, NYUP(R2) YES-OPTION ON 801?
000240 001472 BEG C,NDN1 BIS #C, NTIC,(SP) NO, STORE BIT
000242 052715 BIS C,NDN1 NO
000246 105762 C,NDN1: TSTB C, NZUP(R2) IDDES CLEARING CALL=
000252 001413 BEG C,NDN2 TSTB C, NYUP(R2) REQUEST END THE CALL?
000254 105762 600016 C,NDN2 TSTB C, NYUP(R2) YES,SECOND INTERRUPT POSSIBLE?
000260 001426 BEG C, NMES TSTB C, NEUN(R2) NO, CLEAR BIT.
000262 105762 600007 C, NMES TSTB C, NEUN(R2) YES, SECOND INTERRUPT POSSIBLE?
000266 003403 BLE C, NMES DECB C, NEUN(R2) NO, INQ, DO NOT CLEAR CCR BIT.
000270 105362 600007 C, NMES DECB C, NEUN(R2) YES, SECOND INTERRUPT POSSIBLE?
000274 000402 BR C, NMES JAIIAT SECOND INTERRUPT
000276 642714 C, NMES1 BIC #C, NCRQ,R4 YES, FREE DN11 FROM LINE.
000302 005662 C,NDN21 CLR C, NAUD(R2) IDFREE FOR NEXT CALL.
000306 142762 #1, C, NEUN(R2) IRESET END-OF-NUMBER CODE,
000314 016246 MOV C, NBAS(R2),(SP) ISTORE BUFFER START
000320 605662 CLR C, NBAS(R2) IZERO BUFFER START (SO
000324 011546 MOV #R5,(SP) IZERO BUFFER START (SO
000326 112765 MOV8 #C, NCPL1,(SP) THAT IT WILL NOT BE REUSED)
000334 012765 MOV #3,R5 ISTORE COUNTER OF 3,
000340 012072 C,NDN3 MOV (SP)+,#C, NANS(R2) ISTORE MESSAGE IN USER-
000344 002762 ADD #2, C, NANS(R2) IRESET BUFFER.
000348 600002 DEC R5 IDEFINED BUFFER.
000352 005305 BNE C,NDN3 ISTORE COMPLETE?
000354 001371 INC C,FLAG IDEFINED BUFFER.
000356 005267 INCB C,FLAG ISET DATA-PRESENT FLAG.
000362 012002 C,NRET1 MOV (SP)+,R2 IRESTORE REGISTERS,
000364 012003 MOV (SP)+,R3
000366 012004 MOV (SP)+,R4
000370 012005 MOV (SP)+,R5
000372 000002 RTI
000374 012700 C,NINTI MOV $C,NTR0,R0  #STORE START OF 1ST ISR TABLE.
000400 002700 C,NINT1 ADD $6,R0  #GET ADDRESS OF 1ST LINE NUMBER
000404 016005 MOV $2(R0),R0  #SAVE REGISTER ADDRESS.
000410 012704 MOV $4,R4  #STORE COUNTER FOR 4 LINES.
000414 121110 C,NINT1 CMPB $R1,$R0  #LINE NUMBER MATCHES?
000416 001416 BEQ C,NINT3  #YES
000420 062705 ADD $2,R5  #NO, GET NEXT REGISTER ADDRESS.
000424 062700 ADD $4,R5  #GET NEXT LINE NUMBER ADDRESS
000430 005004 DEC R4  #ALL 4 TESTED?
000432 001370 BNE C,NINT1  #NO.
000434 022027 CMP R0,$C,NTHY  #YES. ALL LINES TESTED?
000440 001357 BNE C,NINT  #NO.
000442 052761 BIS #10,4(R1)  #YES. SET "NO MATCH" BIT.
000450 062700 C,NINT1 SEN  #MAKE ERROR
000452 002707 RTS PC  #EXIT.
000454 016112 C,NINT1 MOV 2(R1),R2  #GET LINE TABLE ADDRESS,
000460 010582 MOV R5,$C,NREG(R2)  #STORE REGISTER ADDRESS
000464 010580 MOV R2,2(R0)  #STORE ADDRESS OF LINE
000470 052702 ADD $C,NADD,R2  #TABLE START IN ISR TABLE
000472 002704 JTABL1E:  #GET ADDRESS MIDWAY
000474 050522 CLR (R2)+  #THROUGH LINE TABLE,
000476 050522 CLR (R2)+  #ZERO NUMBER ADDRESS,
000478 050512 CLR #R2  #LENGTH AND MODE WORDS,
000480 155012 BISB 1(R0),#R2  #STORE Y AND Z
000482 005204 ASL (R2)+  #INDICATORS AS FLAGS
000484 005202 CLR (R2)+  #IN THE LINE TABLE.
000486 005254 CLZNC  #ZERO LAST WORD IN TABLE.
000488 002702 RTS PC  #EXIT.
000490 016203 C,INPUTI MOV $C,NREG(R2),R3  #GET ADDRESS REGISTER,
000492 000002  #C,NREG(R2),R3  #TRANSMIT ENABLED?
000494 032713 BIT $C,NLEN,#R3  #NO
000496 001200  #C,NPWO,#R3  #POWER FAILURE?
000498 032713 BIT $C,NLDO,#R3  #YES
000500 001661 BNE $C,NXT2  #DATA LINE OCCUPIED?
000502 032713 BIT $C,NPPT0  #NO.
000504 010000  #C,MAI,#R3  #MAINT MODE PRESENT?
000506 001403 BEQ $C,NXT2  #NO.
000508 032713 BEQ $C,NXT2  #NO.
@00552 005762 C, NPT01 TST C, NAOUR(R2) JNUMBER BEING DIALED?
@00556 001046 BNE C, N X T3 JYES
@00558 011610 MOV 4(R1), R0 JGET COUNT OF DIGITS.
@00564 011437 BEQ C, N X T4 JERROR, NO DIGITS.
@00566 120427 CMPB R0, #C, NMAX JERROR, NUMBER EXCEED MAXIMUM?
@00572 101034 BMI C, N X T4 JYES, EXIT.
@00574 011662 MOV R0, C, NCNT(R2) JSTORE DIGIT COUNT
@00580 011612 MOV 2(R1), C, NADD(R2) JSTORE ADDRESS OF NUMBER
@00586 111612 MOV 6(R1), C, NEON(R2) JSTORE HANDSHAKING/EON
@00590 111162 MOV 6(R1), C, NANS(R2) JSTORE ANSWER ADDRESS.
@00596 011612 MOV 2(R1), C, NBAS(R2) JSTORE BUFFER START.
@00602 011613 BIS #C, NCRQ, R3 JSET CALL REQUEST IN REGISTER.
@00604 013271 BIT #C, NMAI, R3 JMAINTENANCE MODE?
@00606 011467 BLO C, NPT2 JNO.
@00612 101562 DECB C, NCNT(R2) JUPDATE COUNTER (IN ADVANCE).
@00618 111723 MOV B #C, NADD(R2), 1(R3) JSEND FIRST DIGIT.
@00624 005262 INC C, NAOUR(R2) JUPDATE POINTER.
@00630 005256 C, NPT21 CLZNC RTS PC JEXIT
@00632 005262 C, NXT41 CLR C, NAOUR(R2) JFREE LINE FOR A NEW CALL.
@00638 005271 SECN RTS PC JERROR EXIT.
@00642 005271 RTS PC JERROR EXIT.
@00644 005262 C, NXT21 SEZ N RTS PC JERROR EXIT.
@00646 005270 C, NXT11 SEN RTS PC JERROR EXIT.
@00648 005267 C, NPT01 RTS PC JERROR EXIT.
@00654 005262 INC C, NAOUR(R2) JUPDATE POINTER.
@00660 005256 C, NPT21 CLZNC RTS PC JEXIT
@00662 005262 C, NXT41 CLR C, NAOUR(R2) JFREE LINE FOR A NEW CALL.
@00668 005271 SECN RTS PC JERROR EXIT.
@00672 005262 C, NPT01 RTS PC JERROR EXIT.
@00674 005270 C, NXT21 SEN RTS PC JERROR EXIT.
@00676 005267 C, NPT01 RTS PC JERROR EXIT.
@00678 005262 C, NPT21 RTS PC JERROR EXIT.

;PROGRAM TO UTILIZE THE ABOVE CODE FOR ONE LINE
@00706 012767 C, U S T R I MOV #40, PS JSTORE PRIORITY LEVEL.
@00710 177776
@00714 012706 MOV #1000, SP JSTORE STACK POINTER.
@00718 001000

;ASSERT "TERMINAL READY" FOR THE DATASET WHICH WILL RECEIVE CONTROL FROM THE 103.
000720 012721 MOV #C,UINT,R1 ；INITIALIZE LINE TABLE.
000724 004757 JSR PC,C,UINT ；(AND GET REGISTER ADDRESS.)
000730 177444 BMI C,UEMR ；FATAL ERROR
000732 016700 MOV C,ULIN+2,R0 ；GET HARDWARE REGISTER ADDRESS.
000736 052710 BIS #C,NLEN,C,NMEN,R0 ；SET LINE AND MASTER ENABLE
000742 012702 MOV #C,ULIN,R2 ；STORE LINE TABLE ADDRESS.
000746 012701 MOV #C,UPUT,R1 ；AND PARAMETER TABLE.
000752 004757 JSR PC,C,INPUT ；BEGIN DIALING.
000756 177444 BMI ； IMF POSSIBLE TO DIAL.
000760 085767 C,UTSTI TST C,FLAG ；DIALING COMPLETE?
000764 001715 BEQ C,UTST ；NO.
000766 032767 BIT #14,C,UMES+4 ；POWER FAIL OR ACR TIME-OUT?
000774 001600 BNE C,UEMR ；YES.
  ；CONTINUE
000775 000000 C,UEMR ；HALT
01000 000000 C,FLAGI ；WORD 0
01002 001 C,UINTI ；BYTE C,NLN0,0
01003 000 ；WORD C,ULIN
01004 001636 ；WORD C,ULIN
01006 000000 ；WORD 0
01010 001 C,UPUTI ；BYTE C,NLN0,=1
01011 377 ；WORD C,NUM
01012 001620 ；WORD 7
01014 000000 ；WORD C,UMES
01016 001301 ；WORD 10,7,11,5,1,1,1
01020 010 C,UNUMI ；BYTE 0,0,0
01021 007 ；WORD C,UMESI ；WORD 0,0,0
01022 011 ；WORD C,ULIN
01023 005 ；WORD 0
01024 001 ；WORD 0
01025 001 ；WORD 0
01026 001 ；WORD 0
01030 000000 ；EVEN
01032 000000 ；END
CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

Maintenance is performed on the DN11 Interface by using the diagnostic program supplied with the unit. The diagnostic program for the DN11 is MAINDEC-11-D9JA and consists of a tape and printout that contains an annotated program listing. Although it is well documented, the efficient use of the diagnostic program requires that the user understand the normal operation of the DN11 (Chapter 3).

Consideration must be given to the fact that the system containing a DN11 is connected to telephone lines and requires the services of some electro-mechanical components in the central office. Statistically, an electro-mechanical component malfunction is more probable than a solid state device malfunction. When a malfunction is observed in the system, repeat the operation several times before subjecting the DN11 to a diagnostic test.

Experience with several telephone exchanges has uncovered three problems that are caused frequently by telephone equipment.

a. The 801 fails to seize the line and return a PND request to the DN11 because of faulty ground-start contacts in the local office.

b. The ACR times out because the called party does not answer (possibly due to an incomplete call or wrong number).

c. The local office does not hang up for as long as 30 seconds after CRQ is cleared. This condition complicates matters because it is sometimes possible for DLO to be cleared even though the line has not been released.

If it appears that the DN11 is at fault, check it out by running the DN11 diagnostic program.

5.2 DN11 DIAGNOSTIC PROGRAM MAINDEC-11-D9JA

The printout of the DN11 diagnostic program contains instructions on how to use the program. This paragraph briefly describes the program and points out its relationship to the maintenance function that is built into the DN11.

The program consists of two parts. The first part is a series of incremental tests that check out the DN11 statically, using the maintenance mode. This mode allows most of the DN11 logic to be checked out with or without an 801 connected. When set by the program, the MAINT flip-flop allows the outputs of the four digit flip-flops to represent the 801 response lines (PND, DSS, PWI, and ACR). The interrupt logic responds to these signals just as if they were the actual response signals from the 801. It also clears the CRQ signal to the 801 to prevent the automatic calling unit from interfacing with the tests by asserting its control lines. The FDLO bit is set to prevent the line from being used by other active programs.
The second part of the program is the on-line exerciser that allows the user to dial a number in his dialing range. Upon completion, the program terminates the call and tries again.

The program contains an oscilloscope loop that allows the user to set the DN11 status bits in both the maintenance and dynamic modes.
APPENDIX A
INTEGRATED CIRCUIT DESCRIPTION

This appendix provides a description, pin designation diagram, logic diagram, and truth table for two of the more complex integrated circuits (ICs) used in the DN11. They are the 7474 Dual D-Type Edge-Triggered Flip-Flops and the 8266 2-Input 4-Bit Digital Multiplexer.
7474 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

These 7474 D-type flip-flops are triggered by the positive edge of the clock pulse. They feature direct-clear and preset inputs and complementary Q and Q outputs.

**TRUTH TABLE (Each Flip-Flop)**

<table>
<thead>
<tr>
<th>$t_n$</th>
<th>$t_{n+1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>Output Q</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Notes: 1. $t_n$ = bit time before clock pulse.  
2. $t_{n+1}$ = bit time after clock pulse.
The 8266 multiplexer is able to choose from two different input sources, each containing 4 bits: \( A = (A_0, A_1, A_2, A_3) \) and \( B = (B_0, B_1, B_2, B_3) \). The selection is controlled by inputs \( S_0 \) and \( S_1 \) as shown in the truth table.

### TRUTH TABLE

<table>
<thead>
<tr>
<th>Select Lines</th>
<th>Output ( f_n (0,1,2,3) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_0 )</td>
<td>( S_1 )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

A diagram illustrating the internal connections of the multiplexer is also provided.
APPENDIX B
LOGIC SYMBOLOGY

B.1 INTRODUCTION

The logic symbology used in the PDP-11 manuals and engineering logic diagrams is generally consistent with MIL-STD-806B Graphic Symbols for Logic Diagrams. Certain symbols are modified by DEC to allow direct reading of logic functions in detailed logic diagrams that show explicit electrical connections between logic elements. The modifications and other conventions are explained in the following paragraphs.

B.2 UNIBUS SIGNAL LEVELS

The Unibus has 56 dedicated signal lines. Negative logic is used for 51 lines and the remaining 5 (BG (7:4) and NPG) use positive logic.

The definitions of positive and negative logic are:

**Positive Logic**
- Signal Asserted: High = Logical 1 = +3V
- Signal at Rest: Low = Logical 0 = 0V

**Negative Logic**
- Signal Asserted: Low = Logical 1 = 0V
- Signal at Rest: High = Logical 0 = +3V

In the logic diagrams, the signal name mnemonic is followed by an H or L to indicate the asserted state (logical 1) of the signal to be high (+3V) or low (ground or 0V). Using this convention, a grant line is called BUS BG2 H and a data line is called BUS D12 L.

B.3 EQUIVALENT GATE SYMBOLS

In the detailed logic diagrams, the gate symbols show the active state of the gate output. A small circle at the output shows that the active state is low (L). Absence of a small circle at the output shows that the active state is high (H).

A large number of NAND and NOR gates are used in DEC logic. The symbols for the NAND and NOR gates show an active low output. Frequently, an active high output is required from a NAND or NOR gate. In this case, a logically equivalent symbol is used to retain the concept of direct reading of logic functions.

For the NAND gate, the logically equivalent negated-input OR gate is used to show the active high output.

For the NOR gate, the logically equivalent negated-input AND gate is used to show the active high output. These gate symbols and associated truth tables are shown in Figure B-1.
B.4 PHYSICAL REPRESENTATION OF D-TYPE FLIP-FLOPS

Type 7474 and 74H74 dual D-type flip-flops are commonly used in DEC logic. The pin assignment diagram and truth table for these flip-flops are shown in Figure B-2. These flip-flops differ only in operating speeds: 74H74 is the faster.

Information at the D-input is transferred to the 1 and 0 outputs on the positive edge of the clock pulse. Triggering occurs at a voltage level on the positive edge of the clock pulse and is not related to the transition time of the edge. After the clock pulse threshold voltage is exceeded, the D-input signal has no effect.
The preset and clear inputs are independent of the clock: low input to PRESET drives OUTPUT 1 high; low input to CLEAR drives OUTPUT 1 low.

B.5 2-OUTPUT TERMINAL FLIP-FLOP SYMBOLOGY

The 7474 and 74H74 flip-flops in the engineering logic diagrams are shown as 4-output terminal devices. Most other users (and the IC manufacturers) show them as 2-output terminal devices, which represents only the physical output connections. Both the 4-output symbol and the 2-output symbol are shown in Figure B-3.

![Flip-Flop Logic Symbology](image)

The flip-flop is a 2-state device with two complementary outputs. Both outputs are asserted (one high and one low) when the flip-flop is asserted (set, D-input is high, true, etc.) and neither is asserted when the flip-flop is not asserted (reset, D-input is low, false, etc.). With the 4-terminal designation, the flip-flop state and polarities of the complemented outputs in both states are read directly.

In the 4-output symbol (Figure B-3), the flip-flop name is NRA and the output signal designations contain the name, state (asserted or not asserted), and polarity (high or low). The state is either 1 for asserted (set) or 0 for non-asserted (reset). The polarity is either H (high or logical 1) or L (low or logical 0); i.e., assuming positive logic conventions in which \( H = 1 = +3V \) and \( L = 0 = 0V \). Usually, the PRESET input is placed near the 1-output because it directly sets the flip-flop; the CLEAR input is placed near the 0-output because it directly resets the flip-flop. Physically, nothing has changed: flip-flop operation is still the same and there are two electrical outputs (pin 9 for the 1-output and pin 8 for the 0-output).

The 4-terminal symbol and signal designators allow direct reading of logic functions in detailed logic diagrams that show explicit electrical connections between the flip-flop outputs and other logic elements. The correct output polarity, pin number, and flip-flop state are read at a glance. This is not possible with the 2-terminal symbol without mental translations. A comparative example is shown in Figure B-4.

B.6 REDEFINED 4-OUTPUT TERMINAL FLIP-FLOPS

Logically speaking, a redefined flip-flop is asserted (set) when clocked with a low signal on its D-input. Graphically, this is accomplished by reversing the output pin assignments and placing a circle on the D-input. The PRESET and CLEAR input pin designations are interchanged because their logical functions are reversed: PRESET directly resets the flip-flop, and CLEAR directly sets the flip-flop. Physically, the flip-flop operation is still the same. Redefinition is used to retain consistency in graphically representing the asserted state of a flip-flop in a detailed logic diagram; specifically, to produce the asserted state with a low signal on the D-input.
Pin designations and outputs for a standard 4-output terminal flip-flop and a redefined 4-output terminal flip-flop are shown in Figure B-5.

Figure B-4 Electrical Connections to Outputs of 2-Terminal and 4-Terminal Flip-Flops

Figure B-5 Standard and Redefined 4-Terminal Flip-Flops
For the redefined flip-flop, when D = 0 the flip-flop is actually reset (pin 9 = 0 and pin 8 = 1); however, the output pins are reversed and the asserted state outputs (NRA (1) H and NRA (1) L) are enabled. The logical definitions assigned to the 4-output terminal flip-flop indicate that the flip-flop is set in this case when its D-input is low.
READER'S COMMENTS

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use?

What features are most useful?

What faults do you find with the manual?

Does this manual satisfy the need you think it was intended to satisfy?

Does it satisfy your needs? Why?

Would you please indicate any factual errors you have found.

Please describe your position.

Name ___________________________ Organization _______________________

Street ___________________________ Department _______________________

City ___________________________ State ___________________________ Zip or Country _______________________