HP 81810S IC Design Verification System
HP 8180 Data Generator
HP 8181 Data Generator Extender
HP 8182 Data Analyzer

Service Information
HP 81810S IC Design Verification System

HP 8180 Data Generator
HP 8181 Data Generator Extender
HP 8182 Data Analyzer
Service Information
CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of the other International Standard's Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in material and workmanship for a period of 90 days from the date of installation. During the warranty period, HP will, at its option, either repair or replace products which prove to be defective.

Warranty services of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, HP service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to buyer. Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted and error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer supplied software or interfacing, unauthorized modifications or misuse, operation outside of the environmental specifications for the products, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES, HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office, addresses are provided at the back of this manual.

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LIST OF EFFECTIVE PAGES

The list of effective pages gives the date of the current edition, and lists the dates of all pages of that edition and all updates. Within this manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. Changes are marked with a vertical bar in the margin. If an update is incorporated when an edition is reprinted, these bars and dates remain. No information is incorporated into a reprint unless it appears as a prior update.

Issue 1.0  December 1987
Effective Pages  Date
  ALL  December 1987
PRINTING HISTORY

Printed Dec 1987
PREFACE

PURPOSE OF THIS MANUAL

The purpose of this manual is to provide the necessary information to troubleshoot and repair faults on the HP 8180A/B Data Generator, HP 8181A/B Data Generator Extender and HP 8182A/B Data Analyzer, which are part of the HP 81810S IC Design Verification System.

AUDIENCE

This manual is aimed at Service Personnel involved in the repair of the above mentioned instruments.

HOW TO USE THIS MANUAL

This manual should be used as a guide when troubleshooting the individual instruments. Section 1 gives information on how to begin the fault-finding process.

RELATED PUBLICATIONS

This section contains a list of all publications related to installation, operation and maintenance of the HP 81810S IC Design Verification System. The publications can be ordered by quoting the relevant part number.

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6-2 Test Setup for the Clock and Data Skew Test
6-3 Test Setup for the Clock 1 and Clock 2 Delay Test
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</tr>
</tbody>
</table>
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<tr>
<td>7-2</td>
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<tr>
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<td>Threshold Level Accuracy and Linearity Test - Both Attenuators and 50 Ω Feedthrough Removed</td>
</tr>
</tbody>
</table>
Chapter 1
General Information

1-1 Introduction

This chapter contains information on safe working practices, recommended test equipment and using the test procedures described in the following chapters.

1-2 Safe Working Practices

The Models 8180A/B, 8181A/B and 8182A/B are Safety Class I instruments (instruments with an exposed metal chassis that is directly connected to earth via the power supply cable).

Before operation, the instruments and manual, including the red safety page, should be reviewed for safety markings and instructions. These must then be followed to ensure safe operation and to maintain the instruments in a safe condition.

**CAUTION**

The HP 8180A/B, HP 8181A/B and HP 8182A/B contain assemblies and components that are sensitive to electrostatic discharge. Ensure that your working area conforms to Corporate Standard 741.080.

Carefully observe precautions and recommended procedures outlined below to avoid compromising the instrument's reliability because of component damage from static electricity.

- Treat all assemblies, components and connections as static sensitive.
- When unpacking new boards, keep them in their conductive plastic bags until you are ready to install them.
- Before removing the top cover from the instrument, select a work area where potential static sources are minimized. If possible, use a controlled-static workstation (HP 9300-0933 or equivalent) that includes personnel grounding provisions.
- Avoid touching any metal parts on the boards. When you are ready to install an upgrade board, remove it from its protective bag and lay it on top of the bag while keeping your free hand in contact with the bag.

1-3 Recommended Equipment

Test Equipment

The test equipment required for the adjustment and performance verification procedures is listed below. Critical specifications of substituted test instrument must meet or exceed the standards given with the equipment list.
**Introduction**

<table>
<thead>
<tr>
<th>Instrument</th>
<th>Type</th>
<th>Critical Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscilloscope</td>
<td>HP54100D</td>
<td>Resolution 100ps/DIV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Time base acc. &lt;=100 ps</td>
</tr>
<tr>
<td>Probe</td>
<td>HP54001A</td>
<td>Bandwidth &gt;=700MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transition time &lt;450 ps</td>
</tr>
<tr>
<td>Probe</td>
<td>HP54002A</td>
<td>50 Ohm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transition time &lt;=350 ps</td>
</tr>
<tr>
<td>Counter</td>
<td>HP5370B</td>
<td>Frequency range &gt;50 MHz</td>
</tr>
<tr>
<td>DVM</td>
<td>HP3456A</td>
<td>Range 10V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Resolution 100 uV</td>
</tr>
<tr>
<td>Signature Analyzer</td>
<td>HP5005A</td>
<td>f max &gt;20 MHz</td>
</tr>
<tr>
<td>Pulse Generator:</td>
<td></td>
<td>A pulse generator capable of meeting all requirements is not available. The critical specifications are given in each test/adjustment procedure. You need to select a pulse generator from the HP range that fits the particular application.</td>
</tr>
<tr>
<td>Power Supply:</td>
<td>HP6002A</td>
<td>Voltage range &gt;20V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Resolution 1 mV</td>
</tr>
<tr>
<td>Data Generator:</td>
<td>HP8018A</td>
<td>Vector depth 1kBit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit rate &gt;50 MHz</td>
</tr>
</tbody>
</table>

**Accessories**

**Cables**
- Strobe/Clock: 15422A
- DATA Cable: 15423A
- Clock Probe: 15406A
- DATA Cable: 15407A
- Interface Cable: 08181-61604
- Interface Cable: 08181-61603

**Adapters**
- Grabbers: 15408A
- BNC Adaptor: 15409A
- Miniprobe Adaptor: 15415A
- Solder in receptacles: 15426A

**Connectors**
- 50 OHM Feedthrough: 10100C
- BNC Attenuator 20dB/20W: Texscan HFP 50/20
- BNC TEE Connector: 1250-0781
- BNC female/female: 1250-0080
- Scope Probe Adapter: 1250-1454
- BNC/Dual Banana: 1251-2277

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Using the Test Procedures

**Delay Lines**

<table>
<thead>
<tr>
<th>Delay Line</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>90.5 ns (A-version)</td>
<td>08180-61636</td>
</tr>
<tr>
<td>90.5 ns (B-version)</td>
<td>08180-61696</td>
</tr>
<tr>
<td>34 ns</td>
<td>08182-61622</td>
</tr>
<tr>
<td>3 ns</td>
<td>08182-61621</td>
</tr>
</tbody>
</table>

**Extender Boards**

<table>
<thead>
<tr>
<th>Extender Board</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD AY Extender</td>
<td>08180-66557</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66556</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66555</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66554</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66553</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66552</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66551</td>
</tr>
<tr>
<td>BD AY Extender</td>
<td>08180-66550</td>
</tr>
</tbody>
</table>

**Adjustment Cover**

<table>
<thead>
<tr>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>08180-04103</td>
</tr>
</tbody>
</table>

**1-4 Using the Test Procedures**

**General**

1. Before adjusting an 8180A/B, 8181A/B or 8182A/B allow the instrument to warm up for 30 minutes.

2. Power supply adjustments must be done with all boards inserted.

3. The adjustment procedures can be used for the A- as well as the B-version. Any differences in the adjustment procedures for the two versions are notified in text.

4. Timing adjustments must be performed with the adjustment cover in place. For the A-version all adjustment holes in the adjustment cover must be blocked with adhesive tape. During adjustment, the tape should only be removed for a few seconds. Each adjustment hole should be closed immediately after the adjustment has been performed.

5. If a B instrument needs to be adjusted, the adjustment cover should be prepared as follows: block the circular hole with adhesive tape, block the two holes which are located above the A8 board with adhesive tape.

6. If only a sub procedure is to be performed, always carry out the whole adjustment procedure starting with step 1.

7. Trigger delay of the channel used as reference, as well as interchannel delay of the 54100D scope must be calibrated before timing measurements can be performed.
Parts Lists

Chapter 2
Exploded Diagrams, Parts Lists

2-1 Introduction

This chapter gives the exploded diagrams and associated parts lists, and exchange boards lists for the HP 8180B generator, the HP 8181B extender and the HP 8182B analyzer. The A-versions are fully documented in the service part of the existing Operating and Service Manual.

2-2 Parts Lists for the HP 8180B

Module Parts List

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRAME</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A61</td>
<td>08180-66561</td>
<td>BD AY U-PRCP</td>
</tr>
<tr>
<td>A62</td>
<td>08180-66562</td>
<td>BD AY INTERF</td>
</tr>
<tr>
<td>A63</td>
<td>08180-66563</td>
<td>BD AY ADDRESS</td>
</tr>
<tr>
<td>A64</td>
<td>08180-66564</td>
<td>BD AY SYNC</td>
</tr>
<tr>
<td>A65</td>
<td>08180-66565</td>
<td>BD AY TIMING</td>
</tr>
<tr>
<td>A66</td>
<td>08180-66566</td>
<td>BD AY MODULE</td>
</tr>
<tr>
<td>A68</td>
<td>08180-66568</td>
<td>BD AY ADDR. CTRL. II</td>
</tr>
<tr>
<td>A72</td>
<td>08180-66572</td>
<td>BD AY MOTHER</td>
</tr>
<tr>
<td>A76</td>
<td>08180-66576</td>
<td>BD AY TEMP CTRL</td>
</tr>
<tr>
<td>A661</td>
<td>08180-62661</td>
<td>MDL AY PWR SPLY</td>
</tr>
<tr>
<td>A672</td>
<td>08180-62672</td>
<td>MDL AY DISP</td>
</tr>
<tr>
<td>A663</td>
<td>08180-62663</td>
<td>PNL AY REAR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>3160-0510</td>
<td>DC MOTOR FAN</td>
</tr>
<tr>
<td>B2</td>
<td>3160-0510</td>
<td>DC MOTOR FAN</td>
</tr>
<tr>
<td>F1A</td>
<td>2110-0051</td>
<td>FUSE 10A 115V</td>
</tr>
<tr>
<td>F1E</td>
<td>2110-0010</td>
<td>FUSE 5A 250V</td>
</tr>
<tr>
<td>FL1</td>
<td>9135-0192</td>
<td>FILTER LINE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MP0</td>
<td>1250-0083</td>
<td>CONN BNC BLKHD</td>
</tr>
<tr>
<td>MP1</td>
<td>08180-00262</td>
<td>PANEL REAR</td>
</tr>
<tr>
<td>MP4</td>
<td>08180-01205</td>
<td>BRACKET FAN</td>
</tr>
<tr>
<td>MP5</td>
<td>08180-00204</td>
<td>PANEL REAR PS</td>
</tr>
<tr>
<td>MP6</td>
<td>08180-04111</td>
<td>COVER TOP PS</td>
</tr>
<tr>
<td>MP7</td>
<td>08180-04102</td>
<td>PANEL SIDE PS</td>
</tr>
<tr>
<td>MP8</td>
<td>08180-01202</td>
<td>BRACKET PERF.</td>
</tr>
<tr>
<td>MP9</td>
<td>01830-23201</td>
<td>COUPLER SW 10-24</td>
</tr>
<tr>
<td>MP10</td>
<td>0403-0374</td>
<td>BUMPER FOOT</td>
</tr>
<tr>
<td>MP11</td>
<td>5040-1148</td>
<td>SHAFT SHORT/GRAY</td>
</tr>
</tbody>
</table>

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## Parts Lists

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<th>Description</th>
</tr>
</thead>
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<tr>
<td>MP12</td>
<td>5040-1149</td>
<td>SHAFT LONG/GRAY</td>
</tr>
<tr>
<td>MP13</td>
<td>08180-04101</td>
<td>PANEL SIDE PS</td>
</tr>
<tr>
<td>MP14</td>
<td>08180-01206</td>
<td>BRKT PS</td>
</tr>
<tr>
<td>MP15</td>
<td>08180-04110</td>
<td>COVER TOP CRT MOD</td>
</tr>
<tr>
<td>MP16</td>
<td>08180-64701</td>
<td>MODULE CRT</td>
</tr>
<tr>
<td>MP17</td>
<td>08180-01203</td>
<td>CLAMP CRT</td>
</tr>
<tr>
<td>MP18</td>
<td>5021-0508</td>
<td>PANEL FRONT</td>
</tr>
<tr>
<td>MP19</td>
<td>08180-00201</td>
<td>PANEL KEYBD</td>
</tr>
<tr>
<td>MP20</td>
<td>4040-2097</td>
<td>FACEPLATE SAFETY</td>
</tr>
<tr>
<td>MP21</td>
<td>1400-0678</td>
<td>CLAMP</td>
</tr>
<tr>
<td>MP22</td>
<td>08180-04115</td>
<td>PLATE SAFETY</td>
</tr>
<tr>
<td>MP23</td>
<td>08180-04155</td>
<td>COVER TOP</td>
</tr>
<tr>
<td>MP25</td>
<td>5041-6820</td>
<td>CAP, HANDLE REAR</td>
</tr>
<tr>
<td>MP26</td>
<td>5060-9804</td>
<td>STRAP HDL 18IN</td>
</tr>
<tr>
<td>MP28</td>
<td>5041-6819</td>
<td>CAP, HANDLE FRONT</td>
</tr>
<tr>
<td>MP30</td>
<td>5021-0519</td>
<td>FRM FRNT 7SPCL</td>
</tr>
<tr>
<td>MP31</td>
<td>1460-1345</td>
<td>TILT STAND</td>
</tr>
<tr>
<td>MP32</td>
<td>5040-7201</td>
<td>FOOT</td>
</tr>
<tr>
<td>MP33</td>
<td>5061-9447</td>
<td>COVER BOTTOM</td>
</tr>
<tr>
<td>MP34</td>
<td>08160-04101</td>
<td>COVER SIDE PERF.</td>
</tr>
<tr>
<td>MP35</td>
<td>5060-9884</td>
<td>COVER SIDE</td>
</tr>
<tr>
<td>MP36</td>
<td>5001-8233</td>
<td>SIDE GUSSET</td>
</tr>
<tr>
<td>MP37</td>
<td>08180-05001</td>
<td>CATCH</td>
</tr>
<tr>
<td>MP38</td>
<td>08180-02301</td>
<td>HOLDER DISTANCE</td>
</tr>
<tr>
<td>MP39</td>
<td>08180-00102</td>
<td>CAGE CARD</td>
</tr>
<tr>
<td>MP40</td>
<td>5021-5837</td>
<td>CORNER STRUT</td>
</tr>
<tr>
<td>MP41</td>
<td>5021-5806</td>
<td>FRAME REAR 7IN</td>
</tr>
<tr>
<td>MP42</td>
<td>5040-7221</td>
<td>FOOT REAR</td>
</tr>
<tr>
<td>MP43</td>
<td>5040-9319</td>
<td>SHAFT PWR SWITCH</td>
</tr>
<tr>
<td>MP44</td>
<td>5040-9320</td>
<td>STOP PWR SWITCH</td>
</tr>
<tr>
<td>MP45</td>
<td>08160-0438</td>
<td>RFI STRIP FINGER</td>
</tr>
<tr>
<td>MP46</td>
<td>0363-0125</td>
<td>CONTACT FINGER</td>
</tr>
<tr>
<td>MP47</td>
<td>5040-7202</td>
<td>TRIM STRIP TOP</td>
</tr>
<tr>
<td>MP48</td>
<td>5001-0440</td>
<td>TRIM STRIP SIDE</td>
</tr>
<tr>
<td>MP50</td>
<td>9140-0726</td>
<td>WIRE AY YOKE</td>
</tr>
<tr>
<td>MP52</td>
<td>08180-03101</td>
<td>GUIDE POWER SHAFT</td>
</tr>
<tr>
<td>MP53</td>
<td>2140-0352</td>
<td>LAMP INDC TI 18V</td>
</tr>
<tr>
<td>MP54</td>
<td>08180-47401</td>
<td>KEY CUP</td>
</tr>
<tr>
<td>MP135</td>
<td>1251-0218</td>
<td>POST CON</td>
</tr>
<tr>
<td>MP136</td>
<td>08180-01282</td>
<td>STRAP TOP</td>
</tr>
<tr>
<td>V1</td>
<td>2090-0706</td>
<td>CRT</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>W7</td>
<td>08180-61681</td>
<td>CBL AY SHLD STROBE</td>
</tr>
<tr>
<td>W8/9</td>
<td>08180-61609</td>
<td>CBL AY PAIR</td>
</tr>
<tr>
<td>W10</td>
<td>08180-61670</td>
<td>CBL AY MASTER</td>
</tr>
<tr>
<td>W11</td>
<td>08180-61616</td>
<td>CBL AY REAR #2</td>
</tr>
<tr>
<td>W12</td>
<td>08180-61688</td>
<td>CBL AY SHLD SET</td>
</tr>
<tr>
<td>W16</td>
<td>08180-61661</td>
<td>CBL AY RBN TW 8P</td>
</tr>
<tr>
<td>W17</td>
<td>08180-61662</td>
<td>CBL AY RBN TW 7P</td>
</tr>
<tr>
<td>W18</td>
<td>5180-2418</td>
<td>CBL AY RBW 230 MM</td>
</tr>
<tr>
<td>W20</td>
<td>08180-61607</td>
<td>CBL AY VIDEO</td>
</tr>
<tr>
<td>W21</td>
<td>08180-61639</td>
<td>CBL AY CRT</td>
</tr>
<tr>
<td>W30</td>
<td>5180-2413</td>
<td>CBL RBN 230 MM</td>
</tr>
</tbody>
</table>
## Power Supply Parts List 8180B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A661</td>
<td>08180-62661</td>
<td>MDL PWR SUPPLY</td>
<td></td>
</tr>
<tr>
<td>A24</td>
<td>08180-66524</td>
<td>BD AY FILTER</td>
<td></td>
</tr>
<tr>
<td>A26</td>
<td>08180-66526</td>
<td>BD AY REG +15, -7V</td>
<td></td>
</tr>
<tr>
<td>A28</td>
<td>08180-66528</td>
<td>BD AY CAPACITOR</td>
<td></td>
</tr>
<tr>
<td>A81</td>
<td>08180-66581</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>A82</td>
<td>08180-66582</td>
<td>BD AY RECTIFIER</td>
<td></td>
</tr>
<tr>
<td>A83</td>
<td>08180-66583</td>
<td>BD AY SWITCHING</td>
<td></td>
</tr>
<tr>
<td>A85</td>
<td>08180-66585</td>
<td>BD AY +5V -5V</td>
<td></td>
</tr>
<tr>
<td>A87</td>
<td>08180-66587</td>
<td>BD AY +23V</td>
<td></td>
</tr>
<tr>
<td>F101</td>
<td>2112-0002</td>
<td>FUSE 2A 250V NT</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>1251-0472</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J2</td>
<td>1251-2035</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J3</td>
<td>1251-2035</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J5</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J6</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J7</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J8</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>S1</td>
<td>3101-2624</td>
<td>SWITCH PWR</td>
<td>A81</td>
</tr>
<tr>
<td>T1</td>
<td>08180-61105</td>
<td>XFMR AY</td>
<td>A81</td>
</tr>
<tr>
<td>F201</td>
<td>2110-0456</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F202</td>
<td>2110-0456</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F203</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F204</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F205</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F206</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F207</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F208</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F209</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F210</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F211</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F212</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F213</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F214</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F215</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0750</td>
<td>BD EXTR RED</td>
<td>A82</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>BD EXTR POLY</td>
<td>A82</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0751</td>
<td>BD EXTR ORN</td>
<td>A83</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0753</td>
<td>BD EXTR GRN</td>
<td>A85</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0755</td>
<td>BD EXTR VIO</td>
<td>A87</td>
</tr>
</tbody>
</table>

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Figure 2-2. A661 Power Supply Module
# Parts Lists

## Display Module Assembly Parts List 8180B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A15</td>
<td>08180-66515</td>
<td>BD AY KEY</td>
<td></td>
</tr>
<tr>
<td>A30</td>
<td>08180-66530</td>
<td>BD AY CNTL</td>
<td></td>
</tr>
<tr>
<td>A32</td>
<td>08180-66532</td>
<td>BD AY DFL VRT</td>
<td></td>
</tr>
<tr>
<td>AA34</td>
<td>08180-66534</td>
<td>BD AY DFL HORZ</td>
<td></td>
</tr>
<tr>
<td>MP15</td>
<td>08180-04110</td>
<td>COVER TOP CRT</td>
<td></td>
</tr>
<tr>
<td>MP16</td>
<td>08180-64701</td>
<td>MODULE CRT</td>
<td></td>
</tr>
<tr>
<td>MP17</td>
<td>08180-01203</td>
<td>CLAMP CRT</td>
<td></td>
</tr>
<tr>
<td>MP18</td>
<td>5021-0508</td>
<td>PANEL FRONT</td>
<td></td>
</tr>
<tr>
<td>MP19</td>
<td>08180-00201</td>
<td>PANEL KEYBD</td>
<td></td>
</tr>
<tr>
<td>MP20</td>
<td>4040-2097</td>
<td>FACEPLATE SAFET</td>
<td></td>
</tr>
<tr>
<td>MP21</td>
<td>1400-0678</td>
<td>CLAMP CRT</td>
<td></td>
</tr>
<tr>
<td>MP30</td>
<td>5021-0519</td>
<td>FRM FRNT</td>
<td></td>
</tr>
<tr>
<td>MP47</td>
<td>5040-7202</td>
<td>TRIM STRIP TOP</td>
<td></td>
</tr>
<tr>
<td>MP48</td>
<td>5001-0440</td>
<td>TRIM STRIP SIDE</td>
<td></td>
</tr>
<tr>
<td>MP50</td>
<td>9140-0726</td>
<td>DEFLECTION YOKE</td>
<td></td>
</tr>
<tr>
<td>MP53</td>
<td>2140-0352</td>
<td>LAMP INCD T118V</td>
<td></td>
</tr>
<tr>
<td>V1</td>
<td>2090-0706</td>
<td>CRT</td>
<td></td>
</tr>
<tr>
<td>W21</td>
<td>08180-61639</td>
<td>CBL AY CRT</td>
<td></td>
</tr>
</tbody>
</table>

## Keyboard Assembly Parts List

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A15</td>
<td>08180-66515</td>
<td>BD AY KEY</td>
<td></td>
</tr>
<tr>
<td>MP70</td>
<td>5041-0846</td>
<td>KNOB NOM 0</td>
<td></td>
</tr>
<tr>
<td>MP71</td>
<td>5041-0847</td>
<td>KNOB NOM 1</td>
<td></td>
</tr>
<tr>
<td>MP72</td>
<td>5041-0848</td>
<td>KNOB NOM 2</td>
<td></td>
</tr>
<tr>
<td>MP73</td>
<td>5041-0849</td>
<td>KNOB NOM 3</td>
<td></td>
</tr>
<tr>
<td>MP74</td>
<td>5041-0850</td>
<td>KNOB NOM 4</td>
<td></td>
</tr>
<tr>
<td>MP75</td>
<td>5041-0851</td>
<td>KNOB NOM 5</td>
<td></td>
</tr>
<tr>
<td>MP76</td>
<td>5041-0852</td>
<td>KNOB NOM 6</td>
<td></td>
</tr>
<tr>
<td>MP77</td>
<td>5041-0853</td>
<td>KNOB NOM 7</td>
<td></td>
</tr>
<tr>
<td>MP78</td>
<td>5041-0854</td>
<td>KNOB NOM 8</td>
<td></td>
</tr>
<tr>
<td>MP79</td>
<td>5041-0855</td>
<td>KNOB NOM 9</td>
<td></td>
</tr>
<tr>
<td>MP80</td>
<td>5041-2756</td>
<td>KNOB A</td>
<td></td>
</tr>
<tr>
<td>MP81</td>
<td>5041-2757</td>
<td>KNOB B</td>
<td></td>
</tr>
<tr>
<td>MP82</td>
<td>5041-2758</td>
<td>KNOB C</td>
<td></td>
</tr>
<tr>
<td>MP83</td>
<td>5041-2759</td>
<td>KNOB D</td>
<td></td>
</tr>
<tr>
<td>MP84</td>
<td>5041-2760</td>
<td>KNOB E</td>
<td></td>
</tr>
<tr>
<td>MP85</td>
<td>5041-2761</td>
<td>KNOB F</td>
<td></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Part Number</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP86</td>
<td>5041-2763</td>
<td>KNOB +/-</td>
</tr>
<tr>
<td>MP87</td>
<td>5041-0841</td>
<td>KEY CUP</td>
</tr>
<tr>
<td>MP88</td>
<td>5041-0409</td>
<td>KNOB NOM BLK</td>
</tr>
<tr>
<td>MP89</td>
<td>5041-2765</td>
<td>KNOB RUN</td>
</tr>
<tr>
<td>MP90</td>
<td>5041-2755</td>
<td>KNOB STOP</td>
</tr>
<tr>
<td>MP91</td>
<td>5041-2766</td>
<td>KNOB BREAK</td>
</tr>
<tr>
<td>MP92</td>
<td>5041-2767</td>
<td>KNOB BACK</td>
</tr>
<tr>
<td>MP93</td>
<td>5041-2764</td>
<td>KNOB FWD</td>
</tr>
<tr>
<td>S1/34</td>
<td>5060-9436</td>
<td>SW P-BTN SINGLE</td>
</tr>
<tr>
<td>W21</td>
<td>5180-2421</td>
<td>CBL RBN</td>
</tr>
</tbody>
</table>
Figure 2-3. A672 Display Module
## Rear Panel Assembly Parts List 8180B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A663</td>
<td>08180-62663</td>
<td>PNL AY REAR</td>
<td></td>
</tr>
<tr>
<td>A40</td>
<td>08180-66540</td>
<td>BD AY HP-IB</td>
<td></td>
</tr>
<tr>
<td>Bl</td>
<td>3160-0510</td>
<td>FAN - DC</td>
<td></td>
</tr>
<tr>
<td>MP0</td>
<td>1250-0083</td>
<td>CONN BNC BLKHD</td>
<td></td>
</tr>
<tr>
<td>MP1</td>
<td>08180-00262</td>
<td>PANEL REAR</td>
<td></td>
</tr>
<tr>
<td>MP4</td>
<td>08180-01205</td>
<td>BRACKET FAN</td>
<td></td>
</tr>
<tr>
<td>W11</td>
<td>08180-61616</td>
<td>CBL AY REAR #2</td>
<td></td>
</tr>
<tr>
<td>W20</td>
<td>08180-61607</td>
<td>CBL AY VIDEO</td>
<td></td>
</tr>
<tr>
<td>W8/9</td>
<td>08180-61609</td>
<td>CBL AY PAIR</td>
<td></td>
</tr>
</tbody>
</table>
Figure 2-4, Rear Panel Assembly
<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A61</td>
<td>08182-66561</td>
<td>BD AY U PRCR</td>
<td>A61</td>
</tr>
<tr>
<td>BT100</td>
<td>1420-0251</td>
<td>BATTERY NICAD</td>
<td>A61</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0749</td>
<td>PC EXTR BD BRN</td>
<td>A61</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A61</td>
</tr>
<tr>
<td>A62</td>
<td>08182-66562</td>
<td>BD AY INTERFC</td>
<td>A62</td>
</tr>
<tr>
<td>BT1</td>
<td>1420-0251</td>
<td>BATTERY NICAD</td>
<td>A62</td>
</tr>
<tr>
<td>J3</td>
<td>1251-4267</td>
<td>CONNECTOR POST</td>
<td>A62</td>
</tr>
<tr>
<td>J3A</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A62</td>
</tr>
<tr>
<td>MP3</td>
<td>4040-0750</td>
<td>PC EXTR BD RED</td>
<td>A62</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A62</td>
</tr>
<tr>
<td>A63</td>
<td>08182-66563</td>
<td>BD AY ADDRESS</td>
<td>A63</td>
</tr>
<tr>
<td>DL110</td>
<td>1810-0616</td>
<td>DEL LINE 14 P</td>
<td>A63</td>
</tr>
<tr>
<td>DL111</td>
<td>1810-0616</td>
<td>DEL LINE 14 P</td>
<td>A63</td>
</tr>
<tr>
<td>J3/4</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A63</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0751</td>
<td>PC EXTR BD ORN</td>
<td>A63</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A63</td>
</tr>
<tr>
<td>A64</td>
<td>08182-66564</td>
<td>BD AY CNTL</td>
<td>A64</td>
</tr>
<tr>
<td>DL101</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A64</td>
</tr>
<tr>
<td>DL103</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A64</td>
</tr>
<tr>
<td>DL104</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A64</td>
</tr>
<tr>
<td>DL201</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A64</td>
</tr>
<tr>
<td>J4/J8</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A64</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0752</td>
<td>PC EXTR BD YEL</td>
<td>A64</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A64</td>
</tr>
<tr>
<td>A65</td>
<td>08182-66565</td>
<td>BD AY DATA</td>
<td>A65</td>
</tr>
<tr>
<td>DL107</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A65</td>
</tr>
<tr>
<td>DL207</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A65</td>
</tr>
<tr>
<td>DL307</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A65</td>
</tr>
<tr>
<td>DL407</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A65</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0754</td>
<td>PC EXTR BD BL</td>
<td>A66</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A66</td>
</tr>
<tr>
<td>W1</td>
<td>08180-61601</td>
<td>CBL AY MDL</td>
<td>A66</td>
</tr>
</tbody>
</table>
# Parts Lists

This is a replaceable parts list on a sub-assembly level.

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A68</td>
<td>08180-66568</td>
<td>BD AY ADR CTL 2</td>
<td></td>
</tr>
<tr>
<td>DL1/DL7</td>
<td>1810-0616</td>
<td>DELAY LINE 14 P</td>
<td>A68</td>
</tr>
<tr>
<td>DL8</td>
<td>1810-0893</td>
<td>DELAY LINE 10 NS</td>
<td>A68</td>
</tr>
<tr>
<td>J3/J5</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A68</td>
</tr>
<tr>
<td>J6</td>
<td>1200-0588</td>
<td>SOCKET IC 16 CON</td>
<td>A68</td>
</tr>
<tr>
<td>J8/J11</td>
<td>1200-0548</td>
<td>SOCKET IC 14 CON</td>
<td>A68</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0747</td>
<td>PC EXTR BD GRA</td>
<td>A68</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A68</td>
</tr>
<tr>
<td>A72</td>
<td>08180-66572</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J2</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J3</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J4</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J5</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J6</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J7</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J8</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J9</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J10</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J11</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J12</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J13</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J14</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J15</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J16</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J17</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J18</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J19</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J20</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J21</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J22</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J23</td>
<td>1200-0607</td>
<td>SKT IC 16 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J24</td>
<td>1251-3004</td>
<td>CONN POST</td>
<td>A72</td>
</tr>
<tr>
<td>J25</td>
<td>1251-0541</td>
<td>CONN 34 PIN</td>
<td>A72</td>
</tr>
</tbody>
</table>
Figure 2-5. A12 Motherboard
## Parts Lists

### 2-3 Parts Lists for the HP 8181B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A61</td>
<td>08181-66561</td>
<td>BD AY MULTIPLEX</td>
<td></td>
</tr>
<tr>
<td>A62</td>
<td>08180-66562</td>
<td>BD AY GEN MDL</td>
<td></td>
</tr>
<tr>
<td>A66</td>
<td>08181-66566</td>
<td>BD AY MODULE</td>
<td></td>
</tr>
<tr>
<td>A68</td>
<td>08181-66568</td>
<td>BD AY ADR CNTL2</td>
<td></td>
</tr>
<tr>
<td>A72</td>
<td>08181-66572</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>A76</td>
<td>08180-66576</td>
<td>BD BD AY Fan Filter</td>
<td></td>
</tr>
<tr>
<td>A661</td>
<td>08180-62661</td>
<td>MDL AY PWR SPLY</td>
<td></td>
</tr>
<tr>
<td>A663</td>
<td>08181-62663</td>
<td>PNL AY REAR</td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>3160-0510</td>
<td>DC MOTOR FAN</td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>3160-0510</td>
<td>DC MOTOR FAN</td>
<td></td>
</tr>
<tr>
<td>F1A</td>
<td>2110-0051</td>
<td>FUSE 10A 115V</td>
<td></td>
</tr>
<tr>
<td>F1E</td>
<td>2110-0010</td>
<td>FUSE 5A 250V</td>
<td></td>
</tr>
<tr>
<td>FL1</td>
<td>9135-0192</td>
<td>FILTER LINE</td>
<td></td>
</tr>
<tr>
<td>MP1</td>
<td>08181-00264</td>
<td>PANEL REAR</td>
<td></td>
</tr>
<tr>
<td>MP4</td>
<td>08180-01205</td>
<td>BRACKET FAN</td>
<td></td>
</tr>
<tr>
<td>MP5</td>
<td>08180-00204</td>
<td>PANEL REAR PS</td>
<td></td>
</tr>
<tr>
<td>MP6</td>
<td>08180-04111</td>
<td>COVER TOP PS</td>
<td></td>
</tr>
<tr>
<td>MP7</td>
<td>08180-04102</td>
<td>PANEL SIDE PS</td>
<td></td>
</tr>
<tr>
<td>MP8</td>
<td>08180-01202</td>
<td>BRACKET PERF.</td>
<td></td>
</tr>
<tr>
<td>MP9</td>
<td>01830-23201</td>
<td>COUPLER SW 10-24</td>
<td></td>
</tr>
<tr>
<td>MP10</td>
<td>0403-0374</td>
<td>BUMPER FOOT</td>
<td></td>
</tr>
<tr>
<td>MP11</td>
<td>5040-1148</td>
<td>SHAFT SHORT/GRAY</td>
<td></td>
</tr>
<tr>
<td>MP12</td>
<td>5040-1149</td>
<td>SHAFT LONG/GRAY</td>
<td></td>
</tr>
<tr>
<td>MP13</td>
<td>08180-04101</td>
<td>PANEL SIDE PS</td>
<td></td>
</tr>
<tr>
<td>MP14</td>
<td>08180-01206</td>
<td>BRKT PS</td>
<td></td>
</tr>
<tr>
<td>MP18</td>
<td>08181-00262</td>
<td>PANEL FRONT</td>
<td></td>
</tr>
<tr>
<td>MP23</td>
<td>08181-04155</td>
<td>COVER TOP</td>
<td></td>
</tr>
<tr>
<td>MP25</td>
<td>5041-6820</td>
<td>CAP, HANDLE REAR</td>
<td></td>
</tr>
<tr>
<td>MP26</td>
<td>5060-9804</td>
<td>STRAP HDL 18IN</td>
<td></td>
</tr>
<tr>
<td>MP28</td>
<td>5041-6819</td>
<td>CAP, HANDLE FRONT</td>
<td></td>
</tr>
<tr>
<td>MP30</td>
<td>5021-0519</td>
<td>FRM FRNT 7SPCL</td>
<td></td>
</tr>
<tr>
<td>MP32</td>
<td>5040-7201</td>
<td>FOOT</td>
<td></td>
</tr>
<tr>
<td>MP33</td>
<td>5061-9447</td>
<td>COVER BOTTOM</td>
<td></td>
</tr>
<tr>
<td>MP34</td>
<td>08160-04101</td>
<td>COVER SIDE PERF.</td>
<td></td>
</tr>
<tr>
<td>MP34</td>
<td>08160-04101</td>
<td>COVER SIDE</td>
<td></td>
</tr>
<tr>
<td>MP35</td>
<td>5001-8233</td>
<td>SIDE GUSSET</td>
<td></td>
</tr>
</tbody>
</table>

Revision 1.0, Dec. 1987
<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP36</td>
<td>08180-05001</td>
<td>CATCH</td>
<td></td>
</tr>
<tr>
<td>MP37</td>
<td>08180-02301</td>
<td>HOLDER DISTANCE</td>
<td></td>
</tr>
<tr>
<td>MP38</td>
<td>08181-00102</td>
<td>CAGE CARD</td>
<td></td>
</tr>
<tr>
<td>MP39</td>
<td>5021-5837</td>
<td>CORNER STRUT</td>
<td></td>
</tr>
<tr>
<td>MP40</td>
<td>5021-5806</td>
<td>FRAME REAR 71IN</td>
<td></td>
</tr>
<tr>
<td>MP41</td>
<td>5040-7221</td>
<td>FOOT REAR</td>
<td></td>
</tr>
<tr>
<td>MP42</td>
<td>5040-9319</td>
<td>SHAFT PWR SWITCH</td>
<td></td>
</tr>
<tr>
<td>MP43</td>
<td>5040-9320</td>
<td>STOP PWR SWITCH</td>
<td></td>
</tr>
<tr>
<td>MP44</td>
<td>08160-0438</td>
<td>RFI STRIP FINGER</td>
<td></td>
</tr>
<tr>
<td>MP45</td>
<td>0363-0125</td>
<td>CONTACT FINGER</td>
<td></td>
</tr>
<tr>
<td>MP46</td>
<td>8160-0428</td>
<td>RFI ROUND STRIP</td>
<td></td>
</tr>
<tr>
<td>MP52</td>
<td>08180-03101</td>
<td>GUIDE POWER SHAFT</td>
<td></td>
</tr>
<tr>
<td>MP53</td>
<td>2140-0352</td>
<td>LAMP INDC TI 18V</td>
<td></td>
</tr>
<tr>
<td>MP54</td>
<td>08180-47401</td>
<td>KEY CUP</td>
<td></td>
</tr>
<tr>
<td>MP135</td>
<td>1251-0218</td>
<td>POST CON</td>
<td></td>
</tr>
<tr>
<td>MP136</td>
<td>08181-1282</td>
<td>STRAP TOP</td>
<td></td>
</tr>
<tr>
<td>W7</td>
<td>08180-61609</td>
<td>CBL AY PAIR</td>
<td></td>
</tr>
<tr>
<td>W8</td>
<td>08181-61601</td>
<td>CBL AY BUS</td>
<td></td>
</tr>
</tbody>
</table>
Figure 2-6. 8181B Chassis Parts
<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A661</td>
<td>08180-62661</td>
<td>MDL PWR SUPPLY</td>
<td></td>
</tr>
<tr>
<td>A24</td>
<td>08180-66524</td>
<td>BD AY FILTER</td>
<td></td>
</tr>
<tr>
<td>A26</td>
<td>08180-66526</td>
<td>BD AY REG +15V, -7V</td>
<td></td>
</tr>
<tr>
<td>A28</td>
<td>08180-66528</td>
<td>BD AY CAPACITOR</td>
<td></td>
</tr>
<tr>
<td>A81</td>
<td>08180-66581</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>A82</td>
<td>08180-66582</td>
<td>BD AY RECTIFIER</td>
<td></td>
</tr>
<tr>
<td>A83</td>
<td>08180-66583</td>
<td>BD AY SWITCHING</td>
<td></td>
</tr>
<tr>
<td>A85</td>
<td>08180-66585</td>
<td>BD AY +5V -5V</td>
<td></td>
</tr>
<tr>
<td>A87</td>
<td>08180-66587</td>
<td>BD AY +23V</td>
<td></td>
</tr>
<tr>
<td>F101</td>
<td>2112-0002</td>
<td>FUSE 2A 250V NT</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>1251-0472</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J2</td>
<td>1251-2035</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J3</td>
<td>1251-2035</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J5</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J6</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J7</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J8</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>S1</td>
<td>3101-2624</td>
<td>SWITCH PWR</td>
<td>A81</td>
</tr>
<tr>
<td>T1</td>
<td>08180-61105</td>
<td>XFMR AY</td>
<td>A81</td>
</tr>
<tr>
<td>F201</td>
<td>2110-0456</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F202</td>
<td>2110-0456</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F203</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F204</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F205</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F206</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F207</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F208</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F209</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F210</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F211</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F212</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F213</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F214</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>F215</td>
<td>2110-0456</td>
<td>FUSE 10A</td>
<td>A82</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0750</td>
<td>BD EXTR RED</td>
<td>A82</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>BD EXTR POLY</td>
<td>A82</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0751</td>
<td>BD EXTR ORN</td>
<td>A83</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0753</td>
<td>BD EXTR GRN</td>
<td>A85</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0755</td>
<td>BD EXTR VIO</td>
<td>A87</td>
</tr>
</tbody>
</table>
Figure 2-7. A661 Power Supply Module
## Parts Lists

### Rear Panel Assembly Parts List for the 8181B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A663</td>
<td>08181-62663</td>
<td>PNL AY REAR</td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>3160-0510</td>
<td>FAN - DC</td>
<td></td>
</tr>
<tr>
<td>MP1</td>
<td>08181-00264</td>
<td>PANEL REAR</td>
<td></td>
</tr>
<tr>
<td>MP4</td>
<td>08180-01205</td>
<td>BRACKET FAN</td>
<td></td>
</tr>
<tr>
<td>W7</td>
<td>08180-61609</td>
<td>CBL AY PAIR</td>
<td></td>
</tr>
<tr>
<td>W8</td>
<td>08181-61601</td>
<td>CBL AY BUS</td>
<td></td>
</tr>
</tbody>
</table>
Figure 2-8. A663 Rear Panel Assembly
### Parts Lists

This is a replaceable parts list on a sub-assembly level.

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A61</td>
<td>08181-66561</td>
<td>BD AY MULTIPLEXER</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>1251-3782</td>
<td>CONN</td>
<td>A61</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0749</td>
<td>PC EXTR BD BRN</td>
<td>A61</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A61</td>
</tr>
<tr>
<td>A62</td>
<td>08180-66562</td>
<td>BD AY GEN MDL</td>
<td></td>
</tr>
<tr>
<td>BT1</td>
<td>1420-0251</td>
<td>BATTERY NICAD</td>
<td>A62</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0750</td>
<td>PC EXTR BD RED</td>
<td>A62</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A62</td>
</tr>
<tr>
<td>A66</td>
<td>08180-66566</td>
<td>BD AY MODULE</td>
<td></td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0754</td>
<td>PC EXTR BD BL</td>
<td>A66</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A66</td>
</tr>
<tr>
<td>W1</td>
<td>08180-61601</td>
<td>CBL AY MDL</td>
<td>A66</td>
</tr>
<tr>
<td>A68</td>
<td>08181-66568</td>
<td>BD AY ADR CTL 3</td>
<td></td>
</tr>
<tr>
<td>DL1</td>
<td>08181-61665</td>
<td>CBL AY DELAY LINE</td>
<td>A68</td>
</tr>
<tr>
<td>DL3</td>
<td>1810-0893</td>
<td>DELAY LINE 10 NS</td>
<td>A68</td>
</tr>
<tr>
<td>A72</td>
<td>08181-66572</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J2</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J3</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J4</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J5</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J6</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J7</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J8</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J9</td>
<td>1251-2026</td>
<td>CONN PC 36 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J10</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J11</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J12</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J13</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J14</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J15</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J16</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J17</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>J18</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A72</td>
</tr>
<tr>
<td>A76</td>
<td>08180-66576</td>
<td>BD AY TEMP CTRL</td>
<td></td>
</tr>
</tbody>
</table>
# Module Parts List

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRAME</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A61</td>
<td>08182-66561</td>
<td>BD AY U-PRCP</td>
<td></td>
</tr>
<tr>
<td>A62</td>
<td>08182-66562</td>
<td>BD AY INTERF</td>
<td></td>
</tr>
<tr>
<td>A63</td>
<td>08182-66563</td>
<td>BD AY ADDRESS</td>
<td></td>
</tr>
<tr>
<td>A64</td>
<td>08182-66564</td>
<td>BD AY CNTL</td>
<td></td>
</tr>
<tr>
<td>A65</td>
<td>08182-66565</td>
<td>BD AY DATA</td>
<td></td>
</tr>
<tr>
<td>A66</td>
<td>08182-66506</td>
<td>BD AY CLOCK</td>
<td></td>
</tr>
<tr>
<td>A67</td>
<td>08182-66508</td>
<td>BD AY HP-IB</td>
<td></td>
</tr>
<tr>
<td>A672</td>
<td>08182-62661</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>A663</td>
<td>08182-62662</td>
<td>BD AY PWR SPLY</td>
<td></td>
</tr>
<tr>
<td>A664</td>
<td>08182-62663</td>
<td>BD AY DISP</td>
<td></td>
</tr>
<tr>
<td>A665</td>
<td>08182-62667</td>
<td>PNL AY REAR</td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>3160-0510</td>
<td>DC MOTOR FAN</td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>3160-0510</td>
<td>DC MOTOR FAN</td>
<td></td>
</tr>
<tr>
<td>F1A</td>
<td>2110-0249</td>
<td>FUSE 12A 115V</td>
<td></td>
</tr>
<tr>
<td>F1E</td>
<td>2110-0056</td>
<td>FUSE 6A 250V</td>
<td></td>
</tr>
<tr>
<td>FL1</td>
<td>9135-0192</td>
<td>FILTER LINE</td>
<td></td>
</tr>
<tr>
<td>MP1</td>
<td>08182-00265</td>
<td>PANEL REAR</td>
<td></td>
</tr>
<tr>
<td>MP4</td>
<td>08180-01205</td>
<td>BRACKET FAN</td>
<td></td>
</tr>
<tr>
<td>MP5</td>
<td>08182-00204</td>
<td>PANEL REAR PS</td>
<td></td>
</tr>
<tr>
<td>MP6</td>
<td>08180-04111</td>
<td>COVER TOP PS</td>
<td></td>
</tr>
<tr>
<td>MP7</td>
<td>08180-04102</td>
<td>PANEL SIDE PS</td>
<td></td>
</tr>
<tr>
<td>MP8</td>
<td>08180-01202</td>
<td>BRACKET PERF.</td>
<td></td>
</tr>
<tr>
<td>MP9</td>
<td>01830-23201</td>
<td>COUPLER SW 10-24</td>
<td></td>
</tr>
<tr>
<td>MP10</td>
<td>0403-0374</td>
<td>BUMPER FOOT</td>
<td></td>
</tr>
<tr>
<td>MP11</td>
<td>5040-1148</td>
<td>SHAFT SHORT/GRAY</td>
<td></td>
</tr>
<tr>
<td>MP12</td>
<td>5040-1149</td>
<td>SHAFT LONG/GRAY</td>
<td></td>
</tr>
<tr>
<td>MP13</td>
<td>08180-04101</td>
<td>PANEL SIDE PS</td>
<td></td>
</tr>
<tr>
<td>MP14</td>
<td>08182-01206</td>
<td>BRKT PS</td>
<td></td>
</tr>
<tr>
<td>MP15</td>
<td>08180-04110</td>
<td>COVER TOP CRT MOD</td>
<td></td>
</tr>
<tr>
<td>MP16</td>
<td>08180-64701</td>
<td>MODULE CRT</td>
<td></td>
</tr>
<tr>
<td>MP17</td>
<td>08180-01203</td>
<td>CLAMP CRT</td>
<td></td>
</tr>
<tr>
<td>MP18</td>
<td>5021-0508</td>
<td>PANEL FRONT</td>
<td></td>
</tr>
<tr>
<td>MP19</td>
<td>08182-00201</td>
<td>PANEL KEYBD</td>
<td></td>
</tr>
<tr>
<td>MP20</td>
<td>4040-2097</td>
<td>FACEPLATE SAFETY</td>
<td></td>
</tr>
<tr>
<td>MP21</td>
<td>1400-0678</td>
<td>CLAMP</td>
<td></td>
</tr>
<tr>
<td>MP22</td>
<td>08180-04115</td>
<td>PLATE SAFETY</td>
<td></td>
</tr>
<tr>
<td>Reference Designator</td>
<td>HP Part Number</td>
<td>Description</td>
<td>BD NO.</td>
</tr>
<tr>
<td>----------------------</td>
<td>----------------</td>
<td>---------------------------</td>
<td>--------</td>
</tr>
<tr>
<td>MP23</td>
<td>08182-04155</td>
<td>COVER TOP</td>
<td></td>
</tr>
<tr>
<td>MP25</td>
<td>5041-6820</td>
<td>CAP, HANDLE REAR</td>
<td></td>
</tr>
<tr>
<td>MP26</td>
<td>5060-9804</td>
<td>STRAP HDL 18IN</td>
<td></td>
</tr>
<tr>
<td>MP28</td>
<td>5041-6819</td>
<td>CAP, HANDLE FRONT</td>
<td></td>
</tr>
<tr>
<td>MP30</td>
<td>5021-0519</td>
<td>FRM FRNT 7SPCL</td>
<td></td>
</tr>
<tr>
<td>MP31</td>
<td>1460-1345</td>
<td>TILT STAND</td>
<td></td>
</tr>
<tr>
<td>MP32</td>
<td>5040-7201</td>
<td>FOOT</td>
<td></td>
</tr>
<tr>
<td>MP33</td>
<td>5061-9447</td>
<td>COVER BOTTOM</td>
<td></td>
</tr>
<tr>
<td>MP34</td>
<td>08160-04101</td>
<td>COVER SIDE PERF.</td>
<td></td>
</tr>
<tr>
<td>MP35</td>
<td>5060-9884</td>
<td>COVER SIDE</td>
<td></td>
</tr>
<tr>
<td>MP36</td>
<td>5001-8233</td>
<td>SIDE GUSSET</td>
<td></td>
</tr>
<tr>
<td>MP36</td>
<td>08180-05001</td>
<td>CATCH</td>
<td></td>
</tr>
<tr>
<td>MP37</td>
<td>08182-02301</td>
<td>HOLDER DISTANCE</td>
<td></td>
</tr>
<tr>
<td>MP38</td>
<td>08182-00101</td>
<td>CAGE CARD</td>
<td></td>
</tr>
<tr>
<td>MP39</td>
<td>5021-5837</td>
<td>CORNER STRUT</td>
<td></td>
</tr>
<tr>
<td>MP40</td>
<td>5021-5806</td>
<td>FRAME REAR 7IN</td>
<td></td>
</tr>
<tr>
<td>MP41</td>
<td>5040-7221</td>
<td>FOOT REAR</td>
<td></td>
</tr>
<tr>
<td>MP42</td>
<td>5040-9319</td>
<td>SHAFT PWR SWITCH</td>
<td></td>
</tr>
<tr>
<td>MP43</td>
<td>5040-9320</td>
<td>STOP PWR SWITCH</td>
<td></td>
</tr>
<tr>
<td>MP44</td>
<td>08160-0438</td>
<td>RFI STRIP FINGER</td>
<td></td>
</tr>
<tr>
<td>MP45</td>
<td>0363-0125</td>
<td>CONTACT FINGER</td>
<td></td>
</tr>
<tr>
<td>MP46</td>
<td>8160-0428</td>
<td>RFI ROUND STRIP</td>
<td></td>
</tr>
<tr>
<td>MP47</td>
<td>5040-7202</td>
<td>TRIM STRIP TOP</td>
<td></td>
</tr>
<tr>
<td>MP48</td>
<td>5001-0440</td>
<td>TRIM STRIP SIDE</td>
<td></td>
</tr>
<tr>
<td>MP50</td>
<td>9140-0726</td>
<td>WIRE AY YOKE</td>
<td></td>
</tr>
<tr>
<td>MP52</td>
<td>08180-03101</td>
<td>GUIDE POWER SHAFT</td>
<td></td>
</tr>
<tr>
<td>MP53</td>
<td>2140-0352</td>
<td>LAMP INDC TI 18V</td>
<td></td>
</tr>
<tr>
<td>MP54</td>
<td>08180-47401</td>
<td>KEY CUP</td>
<td></td>
</tr>
<tr>
<td>MP56</td>
<td>08182-01282</td>
<td>STRAP TOP</td>
<td></td>
</tr>
<tr>
<td>V1</td>
<td>2090-0706</td>
<td>CRT</td>
<td></td>
</tr>
<tr>
<td>W1</td>
<td>08182-61610</td>
<td>CBL AY CLOCK QUAL</td>
<td></td>
</tr>
<tr>
<td>W2</td>
<td>08182-61671</td>
<td>CBL AY TRG ARM</td>
<td></td>
</tr>
<tr>
<td>W3</td>
<td>08182-61672</td>
<td>CBL AY TRG QUAL</td>
<td></td>
</tr>
<tr>
<td>W4</td>
<td>08182-61673</td>
<td>CBL AY STOP</td>
<td></td>
</tr>
<tr>
<td>W5</td>
<td>08182-61614</td>
<td>CBL AY CLOCK OUT</td>
<td></td>
</tr>
<tr>
<td>W6</td>
<td>08182-61675</td>
<td>CBL AY ACTIVE OUT</td>
<td></td>
</tr>
<tr>
<td>W7</td>
<td>08182-61676</td>
<td>CBL AY TRG OUT</td>
<td></td>
</tr>
<tr>
<td>W8</td>
<td>08182-61677</td>
<td>CBL AY PULSED ERROR</td>
<td></td>
</tr>
<tr>
<td>W9</td>
<td>08182-61678</td>
<td>CBL AY LATCHED ERROR</td>
<td></td>
</tr>
<tr>
<td>W10</td>
<td>08182-61619</td>
<td>CBL AY SHLD VID</td>
<td></td>
</tr>
<tr>
<td>W11</td>
<td>08182-61605</td>
<td>CBL AY CLOCK</td>
<td></td>
</tr>
<tr>
<td>W12</td>
<td>08182-61601</td>
<td>CBL AY TWIN</td>
<td></td>
</tr>
<tr>
<td>W14</td>
<td>08182-61606</td>
<td>CBL AY DATA</td>
<td></td>
</tr>
<tr>
<td>W19</td>
<td>5180-2421</td>
<td>CBL AY HP-IB</td>
<td></td>
</tr>
<tr>
<td>W21</td>
<td>08180-61639</td>
<td>CBL AY CRT</td>
<td></td>
</tr>
</tbody>
</table>
Figure 2-10 8182 Chassis Parts
## Parts Lists

### Power Supply Module Parts List of the 8182B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A661</td>
<td>08182-62661</td>
<td>MDL PWR SUPPLY</td>
<td></td>
</tr>
<tr>
<td>A24</td>
<td>08182-66524</td>
<td>BD AY POST REG</td>
<td></td>
</tr>
<tr>
<td>A25</td>
<td>08182-66526</td>
<td>BD AY INDUCTOR</td>
<td></td>
</tr>
<tr>
<td>A26</td>
<td>08182-66526</td>
<td>BD AY REG +15, -10V</td>
<td></td>
</tr>
<tr>
<td>A28</td>
<td>08180-66528</td>
<td>BD AY CAPACITOR</td>
<td></td>
</tr>
<tr>
<td>A81</td>
<td>08182-66581</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>A82</td>
<td>08182-66582</td>
<td>BD AY RECTIFIER</td>
<td></td>
</tr>
<tr>
<td>A83</td>
<td>08182-66583</td>
<td>BD AY SWITCHING</td>
<td></td>
</tr>
<tr>
<td>F101</td>
<td>2112-0002</td>
<td>FUSE 2A 250V NT</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>1251-0472</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J2</td>
<td>1251-5160</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J6</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>J7</td>
<td>1251-2034</td>
<td>CONN PC</td>
<td>A81</td>
</tr>
<tr>
<td>S1</td>
<td>3101-2624</td>
<td>SWITCH PWR</td>
<td>A81</td>
</tr>
<tr>
<td>T1</td>
<td>08182-61105</td>
<td>XFMR AY</td>
<td>A81</td>
</tr>
<tr>
<td>F201</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F202</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F203</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F204</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F205</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F206</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F207</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F208</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F209</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F210</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F211</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F212</td>
<td>2110-0653</td>
<td>FUSE MINI 15A</td>
<td>A82</td>
</tr>
<tr>
<td>F213</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>F214</td>
<td>2110-0446</td>
<td>FUSE 10A 125V</td>
<td>A82</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0750</td>
<td>BD EXTR RED</td>
<td>A82</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>BD EXTR POLY</td>
<td>A82</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0751</td>
<td>BD EXTR ORN</td>
<td>A83</td>
</tr>
</tbody>
</table>

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Figure 2-11. A661 Power Supply
## Parts Lists

**Display Module Assembly Parts List of the HP8182B**

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A672</td>
<td>08182-62672</td>
<td>MDL AY DISPLY</td>
<td></td>
</tr>
<tr>
<td>A17</td>
<td>08180-66517</td>
<td>BD AY KEY</td>
<td></td>
</tr>
<tr>
<td>A30</td>
<td>08180-66530</td>
<td>BD AY CNTL</td>
<td></td>
</tr>
<tr>
<td>A32</td>
<td>08180-66532</td>
<td>BD AY DFL VRT</td>
<td></td>
</tr>
<tr>
<td>A34</td>
<td>08180-66534</td>
<td>BD AY DFL HORZ</td>
<td></td>
</tr>
<tr>
<td>MP15</td>
<td>08180-04110</td>
<td>COVER TOP CRT</td>
<td></td>
</tr>
<tr>
<td>MP16</td>
<td>08180-64701</td>
<td>MODULE CRT</td>
<td></td>
</tr>
<tr>
<td>MP17</td>
<td>08180-01203</td>
<td>CLAMP CRT</td>
<td></td>
</tr>
<tr>
<td>MP18</td>
<td>5021-0508</td>
<td>PANEL FRONT</td>
<td></td>
</tr>
<tr>
<td>MP19</td>
<td>08182-00201</td>
<td>PANEL KEYBD</td>
<td></td>
</tr>
<tr>
<td>MP20</td>
<td>4040-2097</td>
<td>FACEPLATE SAFET</td>
<td></td>
</tr>
<tr>
<td>MP21</td>
<td>1400-0678</td>
<td>CLAMP</td>
<td></td>
</tr>
<tr>
<td>MP30</td>
<td>5021-0519</td>
<td>FRM FRNT</td>
<td></td>
</tr>
<tr>
<td>MP47</td>
<td>5040-7202</td>
<td>TRIM STRIP TOP</td>
<td></td>
</tr>
<tr>
<td>MP48</td>
<td>5001-0440</td>
<td>TRIM STRIP SIDE</td>
<td></td>
</tr>
<tr>
<td>MP50</td>
<td>9140-0726</td>
<td>DEFLECTION YOKE</td>
<td></td>
</tr>
<tr>
<td>MP53</td>
<td>2140-0352</td>
<td>LAMP INCD TI18V</td>
<td></td>
</tr>
<tr>
<td>MP54</td>
<td>08180-47401</td>
<td>KEY CUP</td>
<td></td>
</tr>
<tr>
<td>V1</td>
<td>2090-0706</td>
<td>CRT</td>
<td></td>
</tr>
<tr>
<td>W21</td>
<td>08180-61639</td>
<td>CBL AY CRT</td>
<td></td>
</tr>
<tr>
<td>W30</td>
<td>5180-2413</td>
<td>CBL RBN 230 MM</td>
<td></td>
</tr>
<tr>
<td>Reference Designator</td>
<td>HP Part Number</td>
<td>Description</td>
<td>BD NO.</td>
</tr>
<tr>
<td>---------------------</td>
<td>----------------</td>
<td>----------------------</td>
<td>--------</td>
</tr>
<tr>
<td>A17</td>
<td>08180-66517</td>
<td>BD AY KEY</td>
<td></td>
</tr>
<tr>
<td>MP70</td>
<td>5041-0846</td>
<td>KNOB NOM 0</td>
<td></td>
</tr>
<tr>
<td>MP71</td>
<td>5041-0847</td>
<td>KNOB NOM 1</td>
<td></td>
</tr>
<tr>
<td>MP72</td>
<td>5041-0848</td>
<td>KNOB NOM 2</td>
<td></td>
</tr>
<tr>
<td>MP73</td>
<td>5041-0849</td>
<td>KNOB NOM 3</td>
<td></td>
</tr>
<tr>
<td>MP74</td>
<td>5041-0850</td>
<td>KNOB NOM 4</td>
<td></td>
</tr>
<tr>
<td>MP75</td>
<td>5041-0851</td>
<td>KNOB NOM 5</td>
<td></td>
</tr>
<tr>
<td>MP76</td>
<td>5041-0852</td>
<td>KNOB NOM 6</td>
<td></td>
</tr>
<tr>
<td>MP77</td>
<td>5041-0853</td>
<td>KNOB NOM 7</td>
<td></td>
</tr>
<tr>
<td>MP78</td>
<td>5041-0854</td>
<td>KNOB NOM 8</td>
<td></td>
</tr>
<tr>
<td>MP79</td>
<td>5041-0855</td>
<td>KNOB NOM 9</td>
<td></td>
</tr>
<tr>
<td>MP80</td>
<td>5041-2756</td>
<td>KNOB A</td>
<td></td>
</tr>
<tr>
<td>MP81</td>
<td>5041-2757</td>
<td>KNOB B</td>
<td></td>
</tr>
<tr>
<td>MP82</td>
<td>5041-2758</td>
<td>KNOB C</td>
<td></td>
</tr>
<tr>
<td>MP83</td>
<td>5041-2759</td>
<td>KNOB D</td>
<td></td>
</tr>
<tr>
<td>MP84</td>
<td>5041-2760</td>
<td>KNOB E</td>
<td></td>
</tr>
<tr>
<td>MP85</td>
<td>5041-2761</td>
<td>KNOB F</td>
<td></td>
</tr>
<tr>
<td>MP86</td>
<td>5041-2763</td>
<td>KNOB +/-</td>
<td></td>
</tr>
<tr>
<td>MP87</td>
<td>5041-0841</td>
<td>KEY CUP</td>
<td></td>
</tr>
<tr>
<td>MP88</td>
<td>5041-0409</td>
<td>KNOB NOM BLK</td>
<td></td>
</tr>
<tr>
<td>MP89</td>
<td>5041-2765</td>
<td>KNOB RUN</td>
<td></td>
</tr>
<tr>
<td>MP90</td>
<td>5041-2755</td>
<td>KNOB STOP</td>
<td></td>
</tr>
<tr>
<td>MP91</td>
<td>5041-2762</td>
<td>KNOB X</td>
<td></td>
</tr>
<tr>
<td>MP92</td>
<td>5041-2768</td>
<td>KNOB SAMPLE</td>
<td></td>
</tr>
<tr>
<td>S1/33</td>
<td>5060-9436</td>
<td>SW P-BTN SINGLE</td>
<td></td>
</tr>
</tbody>
</table>
Figure 2-12. A672 Display Module
## Parts Lists

### Rear Panel Assembly Parts List of the HP8182B

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A663</td>
<td>08182-62663</td>
<td>PNL AY REAR</td>
<td></td>
</tr>
<tr>
<td>A8</td>
<td>08182-66508</td>
<td>BD AY HP-IB</td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>3160-0510</td>
<td>FAN - DC</td>
<td></td>
</tr>
<tr>
<td>MP1</td>
<td>08182-00265</td>
<td>PANEL REAR</td>
<td></td>
</tr>
<tr>
<td>MP4</td>
<td>08180-01205</td>
<td>BRACKET FAN</td>
<td></td>
</tr>
<tr>
<td>MP135</td>
<td>1251-0218</td>
<td>CONN DS POST</td>
<td></td>
</tr>
<tr>
<td>W10</td>
<td>08182-61619</td>
<td>CBL AY SHLD VID</td>
<td></td>
</tr>
<tr>
<td>W11</td>
<td>08182-61605</td>
<td>CBL AY CLOCK</td>
<td></td>
</tr>
<tr>
<td>W12</td>
<td>08182-61601</td>
<td>CBL AY TWIN</td>
<td></td>
</tr>
<tr>
<td>W14</td>
<td>08182-61606</td>
<td>CBL AY DATA</td>
<td></td>
</tr>
</tbody>
</table>
Figure 2-13. Rear Panel Assy
## Parts Lists

This is a replaceable parts list on a sub-assembly level

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A61</td>
<td>08182-66561</td>
<td>BD AY U PRCR</td>
<td></td>
</tr>
<tr>
<td>BT100</td>
<td>1420-0251</td>
<td>BATTERY NICAD</td>
<td>A61</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0749</td>
<td>PC EXTR BD BRN</td>
<td>A61</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A61</td>
</tr>
<tr>
<td>A62</td>
<td>08182-66562</td>
<td>BD AY INTFC</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>1251-4267</td>
<td>CONNECTOR POST</td>
<td>A62</td>
</tr>
<tr>
<td>J3A</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A62</td>
</tr>
<tr>
<td>MP3</td>
<td>4040-0750</td>
<td>PC EXTR BD RED</td>
<td>A62</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A62</td>
</tr>
<tr>
<td>A63</td>
<td>08182-66563</td>
<td>BD AY ADDRESS</td>
<td></td>
</tr>
<tr>
<td>DL110</td>
<td>1810-0616</td>
<td>DEL LINE 14 PI</td>
<td>A63</td>
</tr>
<tr>
<td>DL111</td>
<td>1810-0616</td>
<td>DEL LINE 14 PI</td>
<td>A63</td>
</tr>
<tr>
<td>J3/4</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A63</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0751</td>
<td>PC EXTR BD ORN</td>
<td>A63</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A63</td>
</tr>
<tr>
<td>A64</td>
<td>08182-66564</td>
<td>BD AY CNTL</td>
<td></td>
</tr>
<tr>
<td>DL101</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A64</td>
</tr>
<tr>
<td>DL103</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A64</td>
</tr>
<tr>
<td>DL104</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A64</td>
</tr>
<tr>
<td>DL201</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A64</td>
</tr>
<tr>
<td>J3/J8</td>
<td>1250-1737</td>
<td>CC AXIAL TEST P</td>
<td>A64</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0752</td>
<td>PC EXTR BD YEL</td>
<td>A64</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A64</td>
</tr>
<tr>
<td>A65</td>
<td>08182-66565</td>
<td>BD AY DATA</td>
<td></td>
</tr>
<tr>
<td>DL107</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A65</td>
</tr>
<tr>
<td>DL207</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A65</td>
</tr>
<tr>
<td>DL307</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A65</td>
</tr>
<tr>
<td>DL407</td>
<td>1810-0616</td>
<td>DELAY LINE 14 PI</td>
<td>A65</td>
</tr>
</tbody>
</table>
## Parts Lists

This is a replaceable parts list on a sub-assembly level

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>HP Part Number</th>
<th>Description</th>
<th>BD NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1</td>
<td>4040-0753</td>
<td>PC EXTR BD GRN</td>
<td>A65</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A65</td>
</tr>
<tr>
<td>A6</td>
<td>08182-66506</td>
<td>BD AY CLOCK</td>
<td></td>
</tr>
<tr>
<td>J301</td>
<td>1251-4267</td>
<td>CONNECTOR POST</td>
<td>A6</td>
</tr>
<tr>
<td>J601</td>
<td>1251-4267</td>
<td>CONNECTOR POST</td>
<td>A6</td>
</tr>
<tr>
<td>MP1</td>
<td>4040-0754</td>
<td>PC EXTR BD BLA</td>
<td>A6</td>
</tr>
<tr>
<td>MP2</td>
<td>4040-0748</td>
<td>PC EXTR BD POLY</td>
<td>A6</td>
</tr>
<tr>
<td>A67</td>
<td>08182-66567</td>
<td>BD AY MOTHER</td>
<td></td>
</tr>
<tr>
<td>J1/J26</td>
<td>1251-1365</td>
<td>CONN PC 44 CONT</td>
<td>A67</td>
</tr>
<tr>
<td>J27</td>
<td>1251-8828</td>
<td>CONN POST 40CON</td>
<td>A67</td>
</tr>
<tr>
<td>J29</td>
<td>1251-8980</td>
<td>CONN POST TP HD</td>
<td>A67</td>
</tr>
<tr>
<td>J30/J43</td>
<td>1251-7871</td>
<td>CONN ICONT R AN</td>
<td>A67</td>
</tr>
</tbody>
</table>
Figure 2-14. A67 Motherboard
## Exchange Boards for the HP 8180B

<table>
<thead>
<tr>
<th>EXCHANGE PART NO.</th>
<th>PARENT PART NO.</th>
<th>DESCRIPTION</th>
<th>CAN ALSO BE USED IN THE 8180A</th>
</tr>
</thead>
<tbody>
<tr>
<td>08180-69561</td>
<td>08180-66561</td>
<td>BD AY U PROC</td>
<td>NO</td>
</tr>
<tr>
<td>08180-69562</td>
<td>08180-66562</td>
<td>BD AY GEN MDL</td>
<td>NO</td>
</tr>
<tr>
<td>08180-69563</td>
<td>08180-66563</td>
<td>BD AY ADDRESS</td>
<td>NO</td>
</tr>
<tr>
<td>08180-69564</td>
<td>08180-66564</td>
<td>BD AY SYNC</td>
<td>YES</td>
</tr>
<tr>
<td>08180-69565</td>
<td>08180-66565</td>
<td>BD AY TIMING</td>
<td>YES</td>
</tr>
<tr>
<td>08180-69566</td>
<td>08180-66566</td>
<td>BD AY MODULE</td>
<td>NO</td>
</tr>
<tr>
<td>08180-69568</td>
<td>08180-66568</td>
<td>BD AY ADR CTL II</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td>08180-66515</td>
<td>BD AY KEY</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66524</td>
<td>BD AY FILTER</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66526</td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66528</td>
<td>BD AY CAPACITOR</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66530</td>
<td>BD AY CNTL</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66532</td>
<td>BD AY DEFL VERT</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66534</td>
<td>BD AY DEFL HORIZ</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66540</td>
<td>BD AY HP-IB</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66572</td>
<td>BD AY MOTHER</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td>08180-66576</td>
<td>BD AY TEMP CTRL</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66581</td>
<td>BD AY MOTHER PS</td>
<td>YES</td>
</tr>
<tr>
<td>08180-69582</td>
<td>08180-66582</td>
<td>BD AY RECT</td>
<td>YES</td>
</tr>
<tr>
<td>08180-69583</td>
<td>08180-66583</td>
<td>BD AY SWITCH</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66585</td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66587</td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
</tbody>
</table>
# Parts Lists

## Exchange Boards for the HP 8181B

<table>
<thead>
<tr>
<th>EXCHANGE PART NO.</th>
<th>PARENT PART NO.</th>
<th>DESCRIPTION</th>
<th>CAN ALSO BE USED IN THE 8181A</th>
</tr>
</thead>
<tbody>
<tr>
<td>08180-69562</td>
<td>08181-66561</td>
<td>BD AY MULTIPL.</td>
<td>NO</td>
</tr>
<tr>
<td>08180-69566</td>
<td>08180-66562</td>
<td>BD AY GEN MDL</td>
<td>NO</td>
</tr>
<tr>
<td>08181-69568</td>
<td>08180-66566</td>
<td>BD AY MODULE</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td>08181-66568</td>
<td>BD AY ADR CTL.3</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td>08180-66524</td>
<td>BD AY FILTER</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66526</td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66528</td>
<td>BD AY CAPACITOR</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08181-66572</td>
<td>BD AY MOTHER</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td>08180-66576</td>
<td>BD AY TEMP CTRL</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66581</td>
<td>BD AY MOTHER PS</td>
<td>YES</td>
</tr>
<tr>
<td>08180-69582</td>
<td>08180-66582</td>
<td>BD AY RECT</td>
<td>YES</td>
</tr>
<tr>
<td>08180-69583</td>
<td>08180-66583</td>
<td>BD AY SWITCH</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66585</td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08180-66587</td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
</tbody>
</table>

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## Parts Lists

### Exchange Boards for the HP 8182B

<table>
<thead>
<tr>
<th>EXCHANGE PART NO.</th>
<th>PARENT PART NO.</th>
<th>DESCRIPTION</th>
<th>CAN ALSO BE USED IN THE 8182A</th>
</tr>
</thead>
<tbody>
<tr>
<td>08182-69561</td>
<td>08182-66561</td>
<td>BD AY U PROC</td>
<td>NO</td>
</tr>
<tr>
<td>08182-69562</td>
<td>08182-66562</td>
<td>BD AY INTFC</td>
<td>NO</td>
</tr>
<tr>
<td>08182-69563</td>
<td>08182-66563</td>
<td>BD AY ADDRESS</td>
<td>NO</td>
</tr>
<tr>
<td>08182-69564</td>
<td>08182-66564</td>
<td>BD AY CNTL</td>
<td>NO</td>
</tr>
<tr>
<td>08182-69565</td>
<td>08182-66565</td>
<td>BD AY DATA</td>
<td>NO</td>
</tr>
<tr>
<td>08182-69506</td>
<td>08182-66506</td>
<td>BD AY CLOCK</td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td>08182-66508</td>
<td>BD AY HP-IB</td>
<td>YES</td>
</tr>
<tr>
<td>08182-66517</td>
<td></td>
<td>BD AY KEY</td>
<td>YES</td>
</tr>
<tr>
<td>08180-66524</td>
<td></td>
<td>BD AY FILTER</td>
<td>YES</td>
</tr>
<tr>
<td>08182-66524</td>
<td></td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
<tr>
<td>08182-66525</td>
<td></td>
<td>BD AY INDUCT.</td>
<td>YES</td>
</tr>
<tr>
<td>08182-66526</td>
<td></td>
<td>BD AY REG</td>
<td>YES</td>
</tr>
<tr>
<td>08180-66528</td>
<td></td>
<td>BD AY CAPACITOR</td>
<td>YES</td>
</tr>
<tr>
<td>08180-66530</td>
<td></td>
<td>BD AY CNTL</td>
<td>YES</td>
</tr>
<tr>
<td>08180-66532</td>
<td></td>
<td>BD AY DEFL VERT</td>
<td>YES</td>
</tr>
<tr>
<td>08180-66534</td>
<td></td>
<td>BD AY DEFL HORIZ</td>
<td>YES</td>
</tr>
<tr>
<td>08182-66567</td>
<td></td>
<td>BD AY MOTHER</td>
<td>NO</td>
</tr>
<tr>
<td>08182-66581</td>
<td></td>
<td>BD AY MOTHER PS</td>
<td>YES</td>
</tr>
<tr>
<td>08182-69582</td>
<td>08182-66582</td>
<td>BD AY RECT</td>
<td>YES</td>
</tr>
<tr>
<td>08182-69583</td>
<td>08182-66583</td>
<td>BD AY SWITCH</td>
<td>YES</td>
</tr>
</tbody>
</table>
Chapter 3
8180A/B Adjustment Procedures

3-1 Introduction

This chapter covers the adjustments procedures necessary for the HP 8180A and 8180B generators.

When performing a major adjustment of the instrument, it is recommended that the adjustments are carried out in the order given.

3-2 Power Supply Adjustment 8180B

Equipment:
Digital Voltmeter, testleads HP3456A

**WARNING**
High voltage is present when performing this adjustment.

**NOTE**
These adjustments must be done with all PC-Boards inserted. When retrofitting options, first install all new boards, adjust the power supply and then continue with the other adjustments.

1. Remove cover from power supply.
2. Allow instrument to warm up for 10 minutes.
3. Connect DVM to TP4 on the A85 board and adjust A83 R323 to -6.1V reading.

**Output voltage adjustment of the -5.2V post regulator**

**NOTE**
If two timing boards are installed, remove right hand cover, connect DVM to the upper lead of A65 C520.
5. Adjust A85 R520 to -5.2V reading.

**CAUTION**

Base current and storage time adjustment of switching transistor Q304 are optimized in the factory. Therefore, never try to adjust A83 R360 and A83 R32.

Figure 3-1. A85 Post Regulator Board
Power Supply Adjustment

Figure 3-2 A83 Switching Board
Figure 3-3. A86 Postregulator Board
Power Supply Adjustment

Figure 3-4. A87 Postregulator Board
3-3 Display Control Board 08180-66530

Display Adjustment

If the display has to be completely adjusted (after a CRT change), set A34R3 clockwise and all other potentiometers to mid range. Position the deflection yoke nearest to the screen and fasten it lightly.

1. Set A1S1 to the position as shown in the following figure.

![Figure 3-5. Switch 1 Microprocessor Board A1](image)

2. Remove A32J4 (Vertical Deflection Board) and turn the instrument on.

3. If necessary slightly increase the intensity with A32R37.

   **NOTE**

   If a bright dot is not visible, set A1S1 to the position as shown in the following figure.

   ![Figure 3-5 continued](image)

4. Using the two ring magnets on the deflection yoke, position the dot approximately 3 mm (1/8 in) above the center of the screen.

   **NOTE**

   After ring magnet adjustment set A1S1 to the position as shown in the first figure on this page.

5. Turn the instrument off and reconnect A32J4, press A2S1 and select the test pattern by pressing the left upper softkey (Adjst Display).

6. Adjust A32R21 (Freq.) for a stable display.

7. Center the test pattern with A34R1 (Hor. Pos.) and adjust A34L2 (Hor. Lin.) for maximum horizontal deflection.

3-6 Revision 1.0, Dec. 1987
8. Adjust A34R3 (Hor. Sync) so that no intensified lines appear.

9. Adjust A34L4 (Hor. Amp.) for approx. 12.5 cm (4 1/2 in) horizontal deflection.

10. Re-adjust A34L2 for best horizontal linearity.

11. Re-centre the test pattern with A34R1 and repeat steps 8 to 10.

12. Adjust A32R27 (Vert. Amp.) for approx. 9 cm (3 1/2 in) vertical deflection.


14. Re-adjust and fasten the deflection yoke, and repeat steps 2 to 13 if necessary.

15. Correct any 'pin cushion' distortion by adding small correction magnets to the deflection yoke.

**Intensity and Focus Adjustment**

16. Press A1S1 and select Brightness on the Miscellaneous page: (Pages > Miscellaneous > Brightness > Increase [until maximum brightness is obtained]).

17. Adjust A32R37 (Intens.) until the line flyback is no longer visible.


19. Secure the ring magnets, deflection yoke and correction magnets using silicon compound.
Figure 3-6. High Voltage Board
Figure 3-7. A61 Microprocessor Board
3-4 GEM Interface Board 08180-66502 (8180A); 08180-66562 (8180B)

Restart Circuit Adjustment 08180-66502

Equipment:

Oscilloscope with Probe HP54100D
Digital Voltmeter, testleads HP3456A
5V Power Supply HP6624A

1. Remove the A2 Interface Board from the 8180A.
2. Set the power supply output voltage to +4.80V and connect the supply to the +5V and GND TP on the A2 board.
3. Connect the oscilloscope probe to the RES TP and GND TP and adjust A2 R4 so that the RES signal just switches from high to low.
4. Insert A2 and fit board distance holder.

D-A Converter Adjustment 08180-66502

Equipment:

Digital Voltmeter HP3456A

1. Program 8180A : Standard Set.
   (Pages > Store/Recall > Rcl Std Set > Execute).
2. Label B; Low Level -2V; High Level -1.5V: (Pages > Output > Level > Next Label [B] > Low <= High [Low] > -2 > Volt > Low <= High [High] > -1.5 > Volt)
3. Connect DVM to A2 TP5 and the nearest GND TP and adjust A2 R129 for -0.75 Volt ±2mV reading.
4. Set Label B; High Level to +5.5V (5.5 > Volt) and adjust A2 R127 for +2.75 Volt +/- 1mV reading.
5. Set Label B; High Level to 0V (0 > Volt) and readjust A2 R129 to 0.000V +/- 0.5mV reading.
6. Repeat steps 2 to 5 if necessary.
7. Program Label B; High Level +1.00V; Low Level 0.00V: (1 > Volt > Low <= High [Low] > 0 > Volt).
8. Connect DVM to A2 TP6 and adjust A2 R130 for 0.000V ±0.5mV reading.

DA-Converter Adjustment 08180-66562

Equipment:

Digital Voltmeter HP3456A

1. Program 8180B : Standard Set.
   (Pages > Store/Recall > Rcl Std Set > Execute).
2. Label B; Low Level -2V; High Level -1.5V: (Pages > Output > Level > Next Label [B] > Low <= High [Low] > -2 > Volt > Low <= High [High] > -1.5 > Volt)
GEM Interface Board 08180-66502 (8180A)

3. Connect DVM to A62 TP5 and the nearest GND TP and adjust A62 R129 for -0.75 Volt ±2mV reading.

4. Set Label B; High Level to +5.5V (5.5 > Volt) and adjust A62 R127 for +2.75 Volt +/- 1mV reading.

5. Set Label B; High Level to 0V (0 > Volt) and readjust A62 R129 to 0.000V +/- 0.5mV reading.

6. Repeat steps 2 to 5 if necessary.

7. Program Label B; High Level +1.00V; Low Level 0.00V; (1 > Volt > Low <-> High [Low] > 0 > Volt).

8. Connect DVM to A62 TP 6 and adjust A62 R130 for 0.000V ±0.5mV reading.
GEM Interface Board 08180-66502 (8180A)

Figure 3-8. A62 Interface Board
3-5 Address Control 1 Board 08180-66503 (8180A); 08180-66563 (8180B)

Equipment:

- Universal Counter: 5370B
- Adjustment Cover: 08180-04103
- Strobe/Clock Cable Set: 15422A
- BNC Adapter: 15409A

NOTE

Final adjustment must be done with the adjustment cover in place. Close adjustment holes with tape and remove tape only when adjusting. Allow instrument to warm up for 30 minutes. Refer to Section 1-4, paragraphs 4 and 5.

Measurement setup:

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)
3. Outputs On: (Pages > Output > Outp on/off > On)
4. Frequency 10 MHz: (Pages > Timing > Frequency > 10 > Megahertz)
5. Connect equipment as shown in measurement set up and press RUN.
7. Set 8180A/B to 50 MHz (50 > Megahertz), and adjust A3 (A63) R75 for 50.50 MHz.
8. Set 8180A/B to 1 MHz (1 > Megahertz), and adjust A3 (A63) R66 for 0.990 MHz.
Zero Delay of Clock 1 and Clock 2 Adjustment

Equipment:

Scope 54100D
Active Pods 54001A
Extender Board 08180-66551
Extender Board 08180-66557

NOTE

This adjustment is to be done only for the 8180B. Before installing the A3 (A63) and A8 (A68) boards on extenders fit distance holder.

Measurement setup:

1. Program 8180B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute).
2. Frequency 10 MHz: (Pages > Timing > Frequency > 10 > Megahertz).
3. Connect equipment as shown in measurement setup and press RUN.
4. Before performing the adjustment cancel out the channel to channel skew of the scope.
5. Set scope to: (Autoscale > Display > Split Screen to Off > Timebase > Sec/Div > 1ns >Trigger > Trigger Source to Chan 1 > Slope to POS).
6. Adjust A63DL3 for 0ns difference between the displayed transitions.
Figure 3-11. Zero Delay

External Inputs, D-A Converter Adjustment

Equipment:

Digital Voltmeter, testleads 3456A

1. Program 8180A/B Input Threshold -10V: (Pages > Control > Inputs > Threshold > -10 > Volt).
2. Connect the DVM to TPl and GND TP on the A3 (A63) board.
4. Set 8180A/B input threshold to +10V(10 > Volt) and adjust A3 (A63) R50 for -3.33V.
5. Set threshold to 0V and check for 0V +/- 3mV.
6. Repeat step 1 to 5 and readjust if necessary.
External Clock Amplifier Adjustment

Equipment:

Pulse Generator
Digital Voltmeter, testleads
Extender Board
Scope
Active Pods
BNC to BNC cable

NOTE

Before putting the A3 (A63) board on an extender, fit a board distance holder.

Measurement setup:

1. Program 8180A/B Input Threshold 0V; Impedance 50 Ohm: External Clock positive transition (Pages > Control > Inputs > Threshold > 0 > Volt > Exit > Impedance > 50Ohm > Ex Clock Source > External[positive slope])

2. Connect DVM to A3 (A63) TP2 and GND TP and adjust A3 (A63) R18 for -15mV ±2mV.

3. Set pulse generator to 10 microsec squarewave and 2 Volt amplitude into 50 Ohm symmetrical about 0 Volt. Transition <5ns.

4. Connect pulse generator to the 8180A/B EXT.CLOCK INPUT

5. Connect scope probe to A3 (A63) TP2 and GND TP and adjust A3 (A63) C12 for best pulse response.

Frequency Error Adjustment

6. Set pulse generator to 51.0 MHz squarewave with 2V amplitude symmetrical about 0 Volt.

7. Adjust A3 (A63) R63 so that the word Clock is flashing in the upper left corner of the 8180A/B display.
Figure 3-13. A63 ADC1 Board
External Break and Stop Amplifier Adjustment

Equipment:

- Pulse Generator
- BNC to BNC Cable
- Oscilloscope: HP 54100D
- Scope Probe: HP 54001A
- Digital Voltmeter, Testleads: HP 3456

1. Program 8180A/B: Input Threshold 0V; Impedance 50 Ohm; Break Input ON
   (PAGES > Control > Inputs > Threshold > 0 > Volt > Exit > Impedance > 50 Ohm > Exit > Break
   Input > ON ɔ > Exit > Stop Input > ON ɔ)

2. Set pulse generator to 10 μs (100 kHz) squarewave and 2 V amplitude (into 50 Ohm) symmetrical
   about 0 V. Transition time < 5 ns.

External Break Amplifier Adjustment

3. Connect DVM to A8 (A68) TP1 and GND TP and adjust A8 (A68) R131 for -15 mV ±2 mV.
4. Connect pulse generator to the 8180A/B External Break Input.
5. Connect Oscilloscope probe to A8 (A68) TP1 and GND TP and adjust A8 (A68) C31 for best pulse
   response.

External Stop Amplifier Adjustment

6. Connect DVM to A8 (A68) TP2 and GND TP and adjust A8 (A68) R112 for -15 mV ±2 mV.
7. Connect pulse generator to the 8180A/B Stop Input.
8. Connect oscilloscope probe to A8 (A68) TP2 and GND TP and adjust A8 (A68) C23 for best pulse
   response.
Strobe Reference Delay Adjustment

**Equipment:**

- Adjustment cover: 08180-04103 (8180A/B)
- Reference delay line A: 08180-61636
- Reference delay line B: 08180-61696
- Cable set: 15423A
- BNC adapter: 15409A
- BNC adapter female/female: 1250-0080
- BNC male probe adapter: 1250-1454
- 50 Ohm feedthrough: 10100C
- Scope: 54100D
- Active pods: 54001A

**Measurement setup:**

1. Adjust interchannel skew of 54100D to zero.

Connect scope inputs 1 and 2 to one signal source output via T-connector (20MHz square wave). Press scope front-panel keys in the following sequence:
   - Autoscale > More > Cal+Test > Cal Menu > Trigger delay > Trigger delay > press Expand waveform until timebase = 500ps. Turn Knob until second transition crosses the horizontal graticule line at the same place where the first trace crosses the horizontal graticule line.

2. Connect the reference delay line through the hole in the adjustment cover of the 8180A/B to A3 (A63) J4 (Reference clock connector).

3. Adjustment must be done with the adjustment cover in place. Allow the generator to warm up for 30 minutes.

4. Program 8180A/B Standard set: (Pages > Store/Recall > Rcl Std Set > Execute)

5. Set Label A to TTL level, Strobe to TTL level: (Pages > Output > Level > Next Label(A) > TTL levels > Execute > Exit Strobe Level > TTL)

---

Revision 1.0, Dec. 1987
6. Set Strobe Output to Clock; set Last Address to 00001: (Pages > Control > Strobe Output > Clock > Exit > Last Address > 1 > Enter N)

7. Address 0 all bits high; Address 1 all bits low: (Pages > DATA > 1 . I > Cursor(Address 1) > 0 . 0)

8. Outputs on: (Pages > Output > Outp On/Off > On)

9. Connect equipment as shown in the measurement set up.


11. New Scope settings: (Autoscale > More > Trigger > Trigger Mode > Trigger Mode [to Mode "Time-Dly")]

12. Set Trigger conditions to:

Figure 3-15. Strobe Ref Delay - 1

13. Center reference clock to vertical graticule line (Display > Split Screen > off > Graticule to (Grid) > Timebase to (500ps) > Channel 2 > Channel 2 Display to (Off) > Timebase > Delay) Adjust with Knob the 50% point of the reference clock transition to center graticule line.

14. Switch channel 1 display off, channel 2 display on
   (Channel 1 > Channel 1 Display > off
   Channel 2 > Channel 2 Display > on)

15. Set Timebase to 500ps (Timebase > Sec/Div > 500ps)
16. Store displayed transition to Memory 1 (More > Wfmsave > Clear Memory 1 > Memory 1 > on > Store to Memory 1).

17. Connect in turn all NRZ channels to Input 2 of 54100D. Store each displayed transition into Memory 1.

Figure 3-16. Strobe Ref Delay 2
Case 1: Data transitions appear after strobe reference clock.

18. Set Markers (More > Delta t > T Markers > on) Set with Knob the Start Marker to the first transition and the Stop Marker to the last transition of the displayed group.

Figure 3-17. Strobe Ref Delay 3
19. Read Delta t.

20. Set Stop Marker to \((\text{Delta} \ t)/2\) exactly in the middle of the displayed group of transitions. Set Start Marker to center graticule line and read Delta t.

---

**Figure 3-18 Strobe Ref Delay 4**

Detailed measurements:

- **Channel**: 500.0 mV/div
- **Timebase**: 500 ps/div
- **Delay**: 0.0000 sec
- **Offset**: 1.260 volts
- **Start**: 0.0000 sec
- **Stop**: 570 ps

Revision 1.0, Dec. 1987
21. Switch Memory 1 off: (More > Wfmsave > Memory 1 > Off)

22. Set Stop Marker to currently displayed transition; Set Start Marker to Delta t: (More > Delta t > Stop Marker > Knob > Start Marker > Knob until Delta t is displayed.)

Figure 3-19. Strobe Ref Delay 5
23. Adjust A8 (A68) R64 so that the 50% point of the displayed DATA channel transition meets the Start Marker.

Figure 3-20. Strobe Ref Delay 6
Case 2: Data transitions appear before strobe reference clock.

24. Set Markers (More > Delta t > T Markers > on) Set with Knob the Start Marker to the first transition and the Stop Marker to the last transition of the displayed group.

Figure 3-21. Strobe Ref Delay 7
25. Read Delta t.

26. Set Start Marker to (Delta T)/2 exactly in the middle of the displayed group of transitions. Set Stop Marker to center graticule line and read Delta t.

Figure 3-22. Strobe Ref Delay 8

<table>
<thead>
<tr>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volts</td>
<td>500.0 mV/div</td>
</tr>
<tr>
<td>Time</td>
<td>500 psec/div</td>
</tr>
<tr>
<td>Delta T</td>
<td>450 psec.</td>
</tr>
<tr>
<td>Start</td>
<td>-450 psec.</td>
</tr>
<tr>
<td>Offset</td>
<td>1.250 volts</td>
</tr>
<tr>
<td>Delay</td>
<td>0.00000 sec</td>
</tr>
<tr>
<td>Stop</td>
<td>0.00000 sec</td>
</tr>
</tbody>
</table>
27. Switch Memory 1 Off: (More > Wfmsave > Memory 1 > Off)

28. Set Start Marker to the 50% point of the currently displayed transition; Set Stop Marker to Delta t:
(More > Delta t > Start Marker > Knob > Stop Marker > Knob)

---

![Graph](image)

**Figure 3-23. Strobe Ref Delay 9**
29. Adjust A8 (A68) R64 so that the 50% point of the currently displayed DATA channel transition meets the Stop Marker.

---

**Figure 3-24. Strobe Ref Delay 10**

<table>
<thead>
<tr>
<th>Ch. a</th>
<th>500 mV/div</th>
<th>Offset</th>
<th>1.560 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timebase</td>
<td>500 mV/div</td>
<td>Delay</td>
<td>0.0000 s</td>
</tr>
<tr>
<td>Delta T</td>
<td>450 mV</td>
<td>Scale</td>
<td>140 mV</td>
</tr>
</tbody>
</table>
30. Check all NRZ channels. The group of transitions should be symmetrical about the reference clock.

![Graph showing waveform and measurements.]

- Ch. 2 = 500.0 mV/div
- Timebase = 500 µs/div
- Delta Y = 450 mV
- Start = -250 mV
- Offset = 1.050 V
- Delay = 0.00000 sec
- Rise = 140 mV

Figure 3-25. Strobe Ref Delay 11
31. Connect the Strobe output to scope channel 2 and adjust A8 (A68) R204 so that the 50% point of the positive going edge of the Strobe signal overlays with the 50% point of the strobe reference transition.

**NOTE**

The adjustment range of A8 (A68) R204 is approximately 1ns. If it is not possible to adjust for zero delay between Strobe and Strobe reference clock, set A8 (A68) R204 to the middle of the adjustment range and perform a pre-adjustment with A8 (A68) DL8. After the pre-adjustment, center the Strobe transition with A8 (A68) R204.
Address Control 2 Board 08180-66508 (8180A); 08180-66568 (8180B)

Figure 3-26. A68 Address Control 11
Output Amplifier High/Low Level Adjustment

Equipment:

- Digital Voltmeter: HP 3456A
- BNC adapter: 15409A
- BNC (f) dual banana plug: 1251-2277
- DATA cable set: 15423A

High Level Adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Memory Set: (Pages > Data > Edit > Clear & Set > Set Data > Execute)
3. Label A High Level 0V; Low Level -2V: (Pages > Output > Level > Next Label[to Label A] > Low<-> High[to High] > 0 > Volt > Low<-> High[to Low] > -2 > Volt)
4. Outputs On: (Pages > Output > Outp on/off > On)
5. Connect Data channel to be adjusted to DVM. Press RUN. Adjust A6 (A66) A60 R2 for 0V +/-0.5mV DVM reading.

Low Level Adjustment

6. Memory Clear: (Pages > Data > Edit > Clear&Set > Clear Data > Execute)
7. Label A High Level +2V; Low Level 0V: (Pages > Output > Level > Low<-> High[to High] > 2 > Volt > Low<-> High[to Low] > 0 > Volt)
8. Press RUN and adjust A6 (A66) A60 R1 for 0v ±0.5mV reading.

Data Flatness and Overshoot Adjustment

Equipment:

- Scope: 54100D
- Active pods: 54001A
- BNC scope probe adapter: 1250-1454
- BNC adapter female/female: 1250-0080
- BNC adapter: 15409A
- Data cable set: 15423A
- Strobe/Clock cable set: 15422A
- 50 Ohm feedthrough: 10100C

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
3. Frequency 250 Hertz: (Pages > Timing > Frequency > 250 > Hertz)
4. First Address 0; Last Address 1; Strobe Output Clock: (Pages > Control > Last Address > 1 > Enter Number > Exit > Strobe Output > Clock)

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5. FAD Data High; LAD Data Low: (Pages > Data > 1 . . . 1 [until FAD Data is high] 0 . . . 0 [until LAD Data is Low])

6. Outputs On: (Pages > Output > Output On/off > On)

7. Press RUN.

8. Connect DATA channel to be measured to scope channel no. 1

9. Set 54100D to Autoscale and Timebase to 1 ms: (Autoscale > Timebase > Sec/Div > 1 ms/msec)

10. Adjust A6 (A66) A60 R4 and A6 (A66) A60 R6 for best flatness.

---

Figure 3-27. Data Flatness Adj
11. Connect 50 Ohm feedthrough to Data channel and adjust A6 (A66) A60 R5 for best flatness.

**Overshoot Adjustment Module Board Output Amplifier 8180A**

12. Set 8180A Frequency to 10MHz (Pages > Timing > Frequency > 10 > Megahertz)
13. Label A ECL Levels: (Pages > Output > Level > ECL Levels > Execute)
14. Connect channel to be adjusted to scope input no. 1 and set scope to: (Autoscale > Delta V > Vmarkers- > on > Auto Top-Base > Timebase > 1 > nanosec)
15. Read Delta V and adjust A6 A60 R3 for < 9% of Delta V.

---

**Figure 3-28. Overshoot Adj**

---

Revision 1.0, Dec. 1987
16. Check rise and fall time for typ. 1.5ns measured from the 20% to 80% of amplitude.

Figure 3-29. Rise Time
Overshoot Adjustment Module Board Output Amplifier 8180B

17. Set 8180B Frequency to 10MHz (Pages > Timing > Frequency > 10 > Megahertz)

18. Label A ECL Levels (Pages > Output > Level > ECL Level > Execute)

19. Connect 50 Ohm feedthrough to the data cable to be adjusted.

20. Connect data channel to scope input no. 1 and adjust A66 A60 R3 for <5% overshoot.

Transition Time Adjustment

21. Adjust rise and fall time for typ. 1.5ns with A66 A60 C27 (measured between the 20% and 80% point of transition).
Figure 3-31 A66 Module Board
Timing Board 08180-66505 (8180A); 08180-66565 (8180B)

3-8 Timing Board 08180-66505 (8180A); 08180-66565 (8180B)

Timing Channels Pre-adjustment

Equipment:
- Scope 54100D
- Active pods 54001A
- 50 Ohm Feedthrough 10100C
- BNC adapter female/female 1250-0080
- BNC scope probe adapter 1250-1454
- Adjustment cover 08180-04103
- Data cable set 15423A
- Strobe/Clock cable set 15422A

NOTE

Strobe Reference Delay must have already been adjusted in Section 3-7.

Measurement setup:

Figure 3-32 Equipment Setup - Timing Channel Pre-adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Frequency 600 KHz All Channel Format RZ=50%: (Pages > Timing > Frequency > 600 > Kilohertz > Exit > Chnl Timing > All Ch Format > RZ=50%)
3. Strobe Level TTL; Label A Level TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label[to Label A] > TTL Levels > Execute)
4. Outputs On: (Pages > Output > Outp on/off > On)
5. All Data set: (high) (Pages > Data > Edit > Clear&Set > Set Data > Execute)
6. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)
7. Connect equipment as shown in the measurement set up and press RUN.

8. Program All Channel Delay 990ns: (Pages > Timing > Chnl Timing > All Ch Delay > 990 > Nanosec)

9. Program scope to: (Autoscale > Chan 1 > Chan 1 Display to off > Display > Split Screen to off > Timebase > Sec/Div > 1ns > Delay > 990ns)

10. Connect in turn all Timing Channels to scope input no. 2 and adjust each positive going transition to 990ns with these pots:
    - A5 (A65) R105 (Channel 0-0 or 1-0)
    - A5 (A65) R305 (Channel 0-1 or 1-1)
    - A5 (A65) R505 (Channel 0-2 or 1-2)
    - A5 (A65) R705 (Channel 0-3 or 1-3)

11. Set 8180A/B All Channel Delay to 90ns: (90 > Nanosec)

12. Set scope Delay to 90ns: (Timebase > Delay > 90ns)

13. Connect in turn all Timing Channels to scope input no. 2 and store each positive going transition into Memory 1 of the scope: (More > Wtmsave > Memory 1 to on > Store to Memory 1)

14. Change the tap connection on the A8 (A68) DL6 Delay Line on the Address Control 2 Board A8 (A68), so that the deviation of most of the timing channels is closest to 90ns.
Figure 3-33. A65 Timing Board
Timing Board 08180-66505 (8180A); 08180-66565 (8180B)

Delay and Width Adjustment

Equipment:

Scope: HP 54100D
Active pods: HP 54001A
50 Ohm Feedthrough: HP 10100C
BNC adapter female/female: 1250-0080
BNC scope probe adapter: 1250-1454
Adjustment cover: 08180-04103
Data cable set: HP 15423A
Strobe/Clock cable set: HP 15422A

NOTE

Final adjustment must be done with an adjustment cover in place. Close adjustment holes with tape and remove tape only when adjusting. Allow instrument to warm up for 30 minutes. Refer to notes 4 and 5 in Chapter 1.

Measurement setup:

![Diagram of measurement setup]

Figure 3-34. Timing Channel - Delay and Width Adj

Delay Adjustment

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Frequency 600 Kilohertz; All Channel Format RZ=50%: (Pages > Timing > Frequency > 600 > Kilohertz > Exit > Chnl Timing > All Ch Format > RZ=50%)
3. Strobe Level TTL; Label A Level TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label[to Label A] > TTL Levels > Execute)
4. Outputs On: (Pages > Output > Outp on/off > On)
5. All Data Set (to high): (Pages > Data > Edit > Clear&Set > Set Data > Execute)
6. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)
7. All Channel Delay 0 ns: (Pages > Timing > Chnl Timing > All Ch Delay > 0 > Nanosec)

8. Connect equipment as shown in the measurement set up and press RUN.

9. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to off > Display > Split Screen to off > Timebase > Sec/Div > 500ps)

10. Connect in turn all Timing Channels to scope input no. 2 and adjust to 0 ns delay between Strobe and Data with the following pots:

   A5 (A65) R104 (Channel 0-0 or 1-0)
   A5 (A65) R304 (Channel 0-1 or 1-1)
   A5 (A65) R504 (Channel 0-2 or 1-2)
   A5 (A65) R704 (Channel 0-3 or 1-3)

11. Recheck zero delay adjustment for all channels and readjust if necessary.

12. Set scope Timebase Delay to 89.0ns: (Timebase > Delay > 89.0ns)

13. Set 8180A/B All Channel Delay to 89.9ns. Connect in turn all Timing Channels to scope input no. 2 and adjust the positive going transition to 89.0ns with the following pots:

   A5 (A65) R101 (Channel 0-0 or 1-0)
   A5 (A65) R301 (Channel 0-1 or 1-1)
   A5 (A65) R501 (Channel 0-2 or 1-2)
   A5 (A65) R701 (Channel 0-3 or 1-3)

14. Set 8180A/B All Channel Delay to 90.0ns. Connect in turn all Timing Channels to scope input no. 2 and adjust the positive going transition to 89.1ns with the following pots:

   A5 (A65) R105 (Channel 0-0 or 1-0)
   A5 (A65) R305 (Channel 0-1 or 1-1)
   A5 (A65) R505 (Channel 0-2 or 1-2)
   A5 (A65) R705 (Channel 0-3 or 1-3)
15. Set 8180A/B All Channel Delay to 989ns. Connect in turn all Timing Channels to scope input no. 2 and adjust the positive going transition to 979.1ns with the following pots:

- A5 (A65) R103 (Channel 0-0 or 1-0)
- A5 (A65) R303 (Channel 0-1 or 1-1)
- A5 (A65) R503 (Channel 0-2 or 1-2)
- A5 (A65) R703 (Channel 0-3 or 1-3).

![Figure 3-35. Delay Setting](image-url)
Width Adjustment

16. Set 8180A/B to All Channel Format RZ, All Channel Delay 0 ns, All Channel Width 10ns: (Pages > Timing > Chnl Timing > All Ch Format > RZ > Exit > All Ch Delay > 0.0 > Nanosec > All Ch Width 10 > Nanosec)

17. Recheck zero delay between Strobe channel and Timing channel.

18. Set scope to: (Timebase > Sec/Div > 500ps > Delay > 0ns )

![Graph showing zero delay between Strobe and Timing channels](image)

**Figure 3-36 Zero Delay - Strobe/Timing Channel**
19. Set scope Timebase Delay to 10ns (Timebase > Delay > 10ns)

20. Connect in turn all Timing Channels to scope input no. 2 and adjust the negative going transition (50% point) to 10.0ns with the following pots:

- A5 (A65) R204 (Channel 0-0 or 1-0)
- A5 (A65) R404 (Channel 0-1 or 1-1)
- A5 (A65) R604 (Channel 0-2 or 1-2)
- A5 (A65) R804 (Channel 0-3 or 1-3)

Figure 3-37. Width Adj 1
21. Set 8180A/B All Channel Width to 99.9ns (99.9 > Nanosec)

22. Set scope Timebase Delay to 98.9ns (Timebase > Delay > 98.9ns)

23. Connect in turn all Timing Channels to scope input no. 2 and adjust the negative going transition to 98.9ns with the following pots:

A5 (A65) R201 (Channel 0-0 or 1-0)
A5 (A65) R401 (Channel 0-1 or 1-1)
A5 (A65) R601 (Channel 0-2 or 1-2)
A5 (A65) R801 (Channel 0-3 or 1-3)

Figure 3-38 Width Adj 2
24. Set 8180A/B All Channel Width to 100ns and adjust the negative going transition to 99.0ns with the following pots:

A5 (A65) R205 (Channel 0-0 or 1-0)
A5 (A65) R405 (Channel 0-1 or 1-1)
A5 (A65) R605 (Channel 0-2 or 1-2)
A5 (A65) R805 (Channel 0-3 or 1-3)

Figure 3-39. Width Adj 3
25. Set 8180A/B All Channel Width to 999ns.

26. Set scope Timebase Delay to 989ns: (Timebase > Delay > 989ns)

27. Adjust the negative going transition to 989 ns with the following pots:

A5 (A65) R203 (Channel 0-0 or 1-0)
A5 (A65) R403 (Channel 0-1 or 1-1)
A5 (A65) R603 (Channel 0-2 or 1-2)
A5 (A65) R803 (Channel 0-3 or 1-3)

---

Figure 3-40 Width Adj 4
Figure 3-41. Timing Board

COMPONENT SIDE 08180-66565

Revision 1.0, Dec. 1987
3-9 Sync Board 08180-66504 (8180A); 08180-66564 (8180B)

External Run Amplifier Adjustment

Equipment:

Pulse Generator
BNC to BNC cable
Scope 54100D
Active Pods 54001A
DVM 3456A

1. Program 8180A/B Input Threshold 0V; Impedance 50 Ohm RUN input On: (Pages > Control > Inputs > Threshold > 0 Volt > Exit > Impedance > 50 Ohm > Exit > Break Input > On[pos. slope] > Exit > RUN Input > On[pos slope]

2. Set pulse generator to 10 µs squarewave and 2 Volt amplitude into 50 Ohm symmetrical about 0 Volt. Transition Time < 5 ns

3. Connect DVM to A4 (A64) TPI and GND TP and adjust A4 (A64) R15 for -15mV +/-2mV

4. Connect pulse generator to the 8180A/B EXTERNAL RUN, GATED INPUT.

5. Connect scope probe to A4 (A64) TPI and GND TP and adjust A4 (A64) C3 for best pulse response.

Clock Output Amplifier High/Low Level Adjustment

Equipment:

Digital Voltmeter HP 3456A
BNC adapter 15409A
BNC (f) dual banana plug 1251-2277
Clock/Strobe cable set 15422A

High Level Adjustment

1. Program 8180A Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)

2. Clock 1 Complement; Clock 2 Complement: (Pages > Output > Clock Output > Clock 1 Polar > Complement > Exit > Clock 2 Polar > Complement)

3. Label A High Level 0V; Low Level -2V: (Pages > Output > Level > Next Label [to Label A] > Low <-> High [to High Level] > 0 > Volt > Low <-> High [to Low Level] > -2 > Volt)

4. Outputs On (Status Stop): (Pages > Output > Output On/Off > On)

5. Connect clock channel to be adjusted Adjust A4 (A64) A60 R2 for 0V ±0.5mV DVM reading.

Low Level Adjustment

6. Clock 1 Normal; Clock 2 Normal: (Pages > Output > Clock Output > Clock 1 Polar > Normal > Exit > Clock 2 Polar > Normal)

7. Label A High Level +2V; Low Level 0V: (Pages > Output > Level > Low <-> High [to High] > 2 > V > Low <-> High [to Low] > 0 > Volt)
8. Adjust A4 (A64) A60 R1 for 0V +/-0.5mV DVM reading.
Sync Board 08180-66504 (8180A); 08180-66564 (8180B)

Flatness and Overshoot Adjustment

Equipment:

Scope HP 54100D
Active pods HP 54001A
BNC adapter HP 15409A
Strobe/Clock cable set HP 15422A

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Label A TTL Levels; Strobe Level to TTL: (Pages > Output > Level > Next Label [to Label A] > TTL Levels > Execute > Exit > Strobe Level > TTL)
3. Frequency 250 Hertz: (Pages > Timing > Frequency > 250 > Hertz)
4. Strobe Output Clock: (Pages > Control > Strobe Output > Clock)
5. Clock 1 Format RZ=50%; Clock 2 Format RZ=50%; (Pages > Timing > Clock Timing > Clock 1 Format > RZ=50% > Exit > Clock 2 Format > RZ=50%)
6. Outputs On: (Pages > Output > Output on/off > on)
7. Connect Strobe Output to scope input no. 1 and clock channel to be measured to scope channel 2.
8. Set 54100D to Autoscale and Timebase to 500 µs: (Autoscale > Timebase > Sec/Div > 500 > microsec)
9. Adjust A4 (A64) A60 R4 and A4 (A64) A60 R6 for best flatness.
10. Connect 50 Ohm feedthrough to currently connected clock output and adjust A4 (A64) A60 R5 for best flatness.

Figure 3-43. Sync Board O/p Amp Flatness Adj
Sync Board 08180-66504 (8180A); 08180-66564 (8180B)

Overshoot Adjustment Sync Board Output Amplifier 8180A

11. Set 8180A Frequency to 10MHz (Pages > Timing > Frequency > 10 > Megahertz)

12. Label A ECL Levels (Pages > Output > Level > ECL Level > Execute)

13. Connect clock channel to be adjusted to the scope input no. 2 (trigger to the 8180A strobe output > scope channel no. 1) and adjust A4 A60 R3 for <9% overshoot.

Figure 3-44 Sync Board O/P Amp Overshoot
14. Check rise and fall time for typical 1.5ns measured from the 20% to 80% of amplitude.

Figure 3-45 Sync Board O/P Amp Rise Time
Overshoot Adjustment Sync Board Output Amplifier 8180B

15. Set 8180B Frequency to 10MHz (Pages > Timing > Frequency > 10 > Megahertz)

16. Label A ECL Levels (Pages > Output > Level > ECL Level > Execute)

17. Connect a 50 Ohm feedthrough to the connected clock cable.

18. Connect the clock channel to be adjusted to the scope input no. 2 (Trigger to the 8180B strobe output > scope input no. 1), and adjust A64 A60 R3 for <5% overshoot.

Transition Time Adjustment

19. Adjust rise time to 1.5ns with A64 A60 C27 (measured between the 20% and 80% point of transition).
3-10 Address Control 2 Board 08180-66508 (8180A); 08180-66568 (8180B)

Clock Channels Pre-adjustment

Equipment:

Scope 54100D
Active Pods 54001A
Adjustment Cover 08180-04103
Strobe/Clock cable set 15422A
BNC Adapter 15409A
50 Ohm Feedthrough 10100C
BNC Adapter female/female 1250-0781
BNC Scope probe Adapter 1250-1454

Measurement setup:

1. Cancel out the scope trigger delay of scope channel 1 and the interchannel delay between scope channel 1 and scope channel 2.
2. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
3. Frequency 600 kHz; Clock 1 Format RZ = 50%; Clock 2 Format RZ = 50%: (Pages > Timing > Frequency > 600 > Kilohertz > Exit > Clock Timing > Clock Format > RZ=50% > Exit > Clock 2 Format > RZ = 50%)
4. Strobe Level TTL; Label A Level TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label [to label > TTL Levels > Execute])
5. Outputs On: (Pages > Output > Output on/off > On)
6. Strobe Output to Clock and press RUN: (Pages > Control > Strobe Output > Clock > RUN)
7. Connect Strobe channel to scope input no. 1 and Clock 1 channel to scope input no. 2.
8. Program Clock 1 Delay and Clock 2 Delay to 990ns: (Pages > Timing > Clock Timing > Clock 1 Delay > 990 > Nanosec > Exit > Clock 2 Delay > 990 > Nanosec)

Fig 3-47. Clock Channels - Pre-adjustment
9. Set scope to: (Autoscale > Display > Split Screen to Off > Channel 1 > Channel 1 to Off > Delta t > T Markers to On > Start Marker to 0 ns > Stop Marker to 990ns > Timebase > Sec/Div > 5 n Delay > 990 ns)

10. Adjust A4 (A64) R101 so that the 50\% point of the positive going transition of Clock 1 meets the center graticule line.

Adjust A4 (A64) R105 so that the 50\% point of the positive going transition of Clock 2 meets the center graticule line.

11. Set 8180A/B Clock 1 and Clock 2 Delay to 90 ns (Exit > Clock 1 Delay > 90 > Nanosec > Exit > Clock 2 Delay > 90 > Nanosec)

12. Set scope to (Timebase > Delay > 90ns > Delta t > Stop Marker > 90ns)

13. Measure and note the time deviation (+/-) of clock 1 to 90ns.

14. Adjustment for the 8180A: Change the tap of delay line A8 DL4 so that the deviation of the 50\% point of the positive going transition is a minimum.

Adjustment for the 8180B: Adjust A8 (A68) DL4 so that the 50\% point of the positive going transition of clock 1 meets the center graticule line.

15. Measure and note the time deviation (+/-) of clock 2 to 90ns.

16. Adjustment for the 8180A: Change the tap of delay line A8 DL5 so that the deviation of the 50\% point of the positive going transition is a minimum.

Adjustment for the 8180B: Adjust A8 (A68) DL5 so that the 50\% point of the positive going transition of clock 2 meets the center graticule line.
3-11 Sync Board 08180-66504 (8180A); 08180-66564 (8180B)

Delay and Width Adjustment

Equipment:

- Adjustment cover: 08180-04103 (8180A/B)
- Strobe/Clock cable set: 15422A
- BNC adapter: 15409A
- 50 Ohm feedthrough: 10100C
- BNC adapter female/female: 1250-0080
- BNC scope probe adapter: 1250-1454

NOTE

On the 8180A, final adjustment must be done with the adjustment cover in place. Block adjustment holes with tape and remove tape only when adjusting. Allow instrument to warm up for 30 minutes.

On the 8180B, final adjustment must be done with the adjustment cover in place. Block the circular hole during adjustment. Allow instrument to warm up for 30 minutes.

Before starting the measurements, cancel out the following delays:

- The trigger delay of scope channel 1:
  (More > Cal&Test > Cal Menu > Trigger Delay channel 1 > Knob)
- The interchannel delay between scope channel 1 and channel 2:
  (Trigger Delay Chan 1 > Chan to Chan Skew > Knob)

![Figure 3-48. Measurement Setup - Clk Delay and Width](image)

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rcl Std Set > Execute)
2. Frequency 600kHz: (Pages > Timing > Frequency > 600 > Kilohertz)
3. Strobe Level TTL; Label A TTL: (Pages > Output > Strobe Level > TTL > Exit > Level > Next Label[to Label > TTL Levels > Execute)
4. Outputs On: (Pages > Output > Output on/off > on)

5. Clock 1 Format RZ 50%; Clock 2 Format RZ 50%; (Pages > Timing > Clock Timing > Clock 1 Format > RZ=50% > Exit > Clock 2 Format > RZ=50%)

6. Strobe output Clock: (Pages > Control > Strobe output > Clock)

7. Clock 1 Delay 0ns; Clock 2 Delay 0ns; (Pages > Timing > Clock Timing > Clock 1 Delay > 0 > Nanosec. > Exit > Clock 2 Delay > 0 > Nanosec)

8. Connect equipment as shown in the measurement set up and press RUN.

9. Connect Strobe to scope input no.1 and Clock 1 to scope input No. 2.

10. Set the 54100D to: (Autoscale).

11. Switch Chan 2 off; Split Screen off; Timebase to 500ps; Trigger on positive slope; (Chan 2 > Chan 2 Display > off > Timebase > Sec/Div > 500 > psec > Trigger > Slope > positive)

12. Check if the 50% point of the displayed Strobe transition is centered on the center graticule line. Set Start marker to 50% point of transition: (Delta T > T markers > On > Start marker > Knob)

13. Switch Channel 1 Off and Channel 2 On: (Chan 1 > Chan 1 Display > Off > Chan 2 > Chan 2 Display > On)
Zero Delay Adjustment

14. Adjust A4 (A64) R100 (Clock 1) so that the 50% point of the displayed Clock 1 transition meets the center graticule line.

Adjust A4 (A64) R104 (Clock 2) so that the 50% point of the displayed Clock 2 transition meets the center graticule line.

Figure 3-49. Zero Delay
15. Connect Clock 1 to scope.

16. Set scope Delay to 89ns: (Timebase > Delay > 89ns)

17. Set Clock 1 Delay to 89.9 nsec and adjust A4 (A64) R93 to 89.0 nsec.

18. Set Clock 1 Delay to 90.0 nsec and adjust A4 (A64) R101 to 89.1 nsec.

19. Set Clock 1 Delay to 989 nsec.

20. Set scope Timebase Delay to 979.1 nsec: (Timebase > Delay > 979.1 nsec)

21. Adjust A4 (A64) R92 so that the 50% point of the displayed Clock 1 transition meets the center graticule line.

Figure 3-50 Clk Delay

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22. Connect Clock 2 to scope channel 2 and program Clock 2 Delay: (Exit > Clock 2 Delay)

23. Set Clock 2 Delay to 89.9 nsec and adjust A4 (A64) R97 to 89 nsec. Set Clock 2 Delay to 90.0 nsec and adjust A4 (A64) R105 to 89.1 nsec. Set Clock 2 Delay to 989 nsec and adjust A4 (A64) R96 to 979.1 nsec.

**Width Adjustment Clock 1**

24. Connect Strobe to scope channel no.1 and connect Clock 1 to scope channel 2.

25. Set 8180A/B Clock 1 Format to RZ and Clock 2 Format to RZ: (Pages > Timing > Clock Timing > Clock 1 Format > RZ > Exit > Clock 2 Format > RZ)

26. Set Clock 1 Delay and Clock 2 Delay to 0.00 ns: (Clock 1 Delay > 0 > Nanosec > Exit > Clock 2 Delay > 0 > Nanosec)

27. Set Clock 1 Width and Clock 2 Width to 10ns: (Exit > Clock 1 Width > 10 > Nanosec > Exit > Clock 2 Width > 10 > Nanosec)

28. Set 54100D Timebase to 500ps/DIV and Timebase Delay to 10ns: (Timebase > SEC/DIV > 500ps > Delay > 10ns)

29. Adjust A4 (A64) R102 so that the 50% point of the negative going transition of Clock 1 meets the center graticule line.

30. Set Clock 1 Width to 99.9ns and set scope Timebase Delay to 98.9ns. Adjust A4 (A64) R94 so that the 50% point of the displayed transition meets the center graticule line.

31. Set Clock 1 Width to 100ns and set Stop marker to 99.0ns. Adjust A4 (A64) R103 so that the 50% point of the displayed transition meets the Stop marker.

32. Set Clock 1 Width to 999ns and set scope Timebase Delay to 989ns. Adjust A4 (A64) R95 so that the 50% point of the displayed transition meets the center graticule line.

**Width Adjustment Clock 2**

33. Connect Clock 2 to scope channel 2.

34. Set 54100D Timebase to 500ps/DIV and Timebase Delay to 10ns: (Timebase > SEC/DIV > 500ps > Delay > 10ns)

35. Adjust A4 (A64) R106 so that the 50% point of the negative going transition of Clock 2 meets the center graticule line.

36. Set Clock 2 Width to 99.9ns and set scope Timebase Delay to 98.9ns. Adjust A4 (A64) R98 so that the 50% point of the displayed transition meets the center graticule line.

37. Set Clock 2 Width to 100ns and set Stop marker to 99.0ns. Adjust A4 (A64) R107 so that the 50% point of the displayed transition meets the Stop marker.

38. Set Clock 2 Width to 999ns and set scope Timebase Delay to 989ns. Adjust A4 (A64) R99 so that the 50% point of the displayed transition meets the center graticule line.
Figure 3-51. Sync Board
## Adjustments - After Board Replacement

### 3-12 Adjustments to be made after Board Replacement

The following table gives the adjustments that need to be carried out whenever any of the 8180A/B boards listed are replaced.

<table>
<thead>
<tr>
<th>Board (Version)</th>
<th>Exchange Part no.</th>
<th>Check and Adjustment</th>
<th>Adj. Cover required</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1 (A)</td>
<td>08180-69501</td>
<td>None</td>
<td>No</td>
</tr>
<tr>
<td>A61 (B)</td>
<td>08180-69561</td>
<td>None</td>
<td>No</td>
</tr>
<tr>
<td>A2 (A)</td>
<td>08180-69502</td>
<td>Restart Circuit function, Output Amplifier High/Low Levels (A6), D-A Converter</td>
<td>No, No, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A62 (B)</td>
<td>08180-69562</td>
<td>Output Amplifier High/Low Levels (A6), D-A Converter</td>
<td>No, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A3 (A)</td>
<td>08180-69503</td>
<td>Internal Clock Generator, D-A Converter, Ext. Clock Amp. Thres. &amp; Pulse Resp., Frequency Error Notification, Strobe Reference Delay</td>
<td>Yes, No, No, Yes, Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A63 (B)</td>
<td>08180-69563</td>
<td>Internal Clock Generator, D-A Converter, Ext. Clock Amp. Thres. &amp; Pulse Resp., Frequency Error Notification, Strobe Reference Delay, Zero Delay Clock 1, Clock 2</td>
<td>Yes, No, No, Yes, Yes, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A4 (A)</td>
<td>08180-69504</td>
<td>Ext. RUN Amp. Thres. &amp; Pulse Response, Clock 1 &amp; 2 Output Amplifier, Clock 1 &amp; 2 Delay and Width, Clock Channels Pre-adjustment, Overshoot Clock 1 &amp; 2 Output</td>
<td>No, No, Yes, No, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A64 (B)</td>
<td>08180-69564</td>
<td>Ext. RUN Amp. Thres. &amp; Pulse Response, Clock 1 &amp; 2 Output Amplifier, Clock 1 &amp; 2 Delay and Width, Clock Channels Pre-adjustment, Overshoot Clock 1 &amp; 2 Output, Transition Time</td>
<td>No, No, Yes, No, No, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A5 (A)</td>
<td>08180-69505</td>
<td>Output Amplifier Timing Delay &amp; Width, Timing Channels Pre-adjustment</td>
<td>Yes, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A65 (B)</td>
<td>08180-69565</td>
<td>Output Amplifier Timing Delay &amp; Width, Timing Channels Pre-adjustment</td>
<td>Yes, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A6 (A)</td>
<td>08180-69506</td>
<td>Output Amplifier DC Levels, Output Amplifier Overshoot</td>
<td>Yes, No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A66 (B)</td>
<td>08180-69566</td>
<td>Output Amplifier DC Levels, Output Amplifier Overshoot, Output Amplifier Transition Time</td>
<td>Yes, No, No</td>
</tr>
</tbody>
</table>

Revision 1.0, Dec. 1987
3-13 Locating Components in the 8180A Data Generator

The following diagrams should be used when locating components/test-points in the HP 8180A Data Generator.
Figure 3-52. A1 Microprocessor Board
Figure 5-53. A2 Interface Board
Figure 3-55. A4 Sync Board
Figure 3-57. A6 Module Board
Figure 3-58. A8 Address Control II Board
Figure 3-99. A12 Motherboard

A12 MOTHERBOARD 8180A-5512

NOTE:
"J" DETAILS IN I ARE THOSE EMBEDDED ON BOARD, OTHERS REFER TO SCHEMATIC INFORMATION & PARTS LISTS.
Figure 3-60. A21 Power Supply Module
Figure 3-61. A22 Rectifier Board
Figure 3-62. A23 Switching Board
Figure 3-63. A25 Post Regulator Board
Figure 3-64. A26 Post Regulator Board
Figure 3-65. A27 Post Regulator Board
Figure 3-66. A30 Control - Board
Figure 3-67. A32 Vertical Deflection Board
Figure 3-68. A34 High Voltage Board
Chapter 4
8181A/B Adjustment Procedures

4-1 Introduction

This chapter deals with the adjustment procedures that need to be performed on the HP 8181A and HP 8181B generator extenders.

When doing a major adjustment of the instrument, it is recommended that the adjustments are carried out in the order given.

NOTE

When performing power supply adjustment please refer to Chapter 3, section 3-2.
When performing Output Amplifier Adjustment please refer to Chapter 3, section 3-8.

NOTE

When adjusting the 8181A, section 4-3 PHI 2 Adjustment must be carried out before performing section 4-2 Extender Delay Adjustment.

4-2 Extender Delay Adjustment

Equipment:

Scope
54100D Active pods          HP 54001A
Data Cable Set             HP 15423A
Strobe/Clock Cable Set     HP 15422A
BNC adapter               HP 15409A
BNC scope probe adapter    1250-1454
BNC adapter female/female 1250-0080
50 Ohm feedthrough         HP 10100C
Adjustment cover           08180-04103
Adjustment Procedure 8181A/B

NOTE

Before making any adjustments on the 8181A/B make sure that adjustments on the 8180A/B have completed. Allow instruments to warm up for 30 minutes.

Measurement setup:

![Equipment Setup Diagram]

Figure 4-1. Equipment Setup - Delay Adjustment
Adjustment Procedure 8181A/B

1. Program 8180A/B Standard Set: (Pages > Store/Recall > Rel Std Set > Execute)
2. Label A TTL Levels: (Pages > Output > Level > Next Label[to Label A] > TTL Level > Execute)
3. Strobe Level TTL: (Pages > Outout > Strobe Level > TTL)
4. Frequency 600 KHz: (Pages > Timing > Frequency > 600 > Kilohertz)
5. First Address 0; Last Address 1: (Pages > Control > Last Address > 1 > Enter Number)
6. Strobe Output to Data: (Pages > Control > Strobe Output > Data)
7. FAD Data and Strobe High; LAD Data and Strobe Low: (Pages > Data > 1 > F...[until all extender Data is set] > Cursor [to Strobe Addr. 1] > 0...[for Strobe and Data channels])
8. Connect equipment as shown in the measurement set up and press RUN.

Preadjustment

10. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split Screen to Off > Timebase > Sec/Div > 500ps > Delay > 990ns)
11. Adjust the positive going transition to 990ns with A8 R41.
12. Program extender delay to 90ns: (90 > Nanosec)
13. Set scope Timebase Delay to 90ns: (Timebase > Delay > 90ns)
14. Measure the time difference between the 50% point of the positive going transition and the center graticule line. Carry out the following steps:
   a) move tap on A8 DL3 (in 1 ns steps) so that the delay deviation is closest to 90ns (only for 8181A)
   b) adjust A8 DL3 to 90 ns (only for 8181B).

Final Adjustment

15. Set Extender Delay to | Set scope Timebase Delay to | Adjust | Set positive transition to
--- | --- | --- | ---
0.0 ns | 0 ns | A8 R42 | 0.0 ns
89.9 ns | 89.0 ns | A8 R43 | 89.0 ns
90.0 ns | 89.1 ns | A8 R41 | 89.1 ns
989 ns | 980 ns | A8 R44 | 980 ns

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Adjustment Procedure 8181A/B

Transition adjusted for 980 ns.

Ch. 2 = 500.0 mvolts/div       Offset = 1.330 volts
Timebase = 500 psec/div        Delay = 980.000 nsec

Figure 4-3. Extender Delay Adjustment
4-3 Multiplexer Board 08181-66501 (8181A)

PHI 2 Adjustment

Equipment:

Scope 54100D
Active pods 54001A

1. Connect channel A probe to A1 U4 pin 18 and channel B probe to test point PHI 2.

2. Set scope to: (Autoscale > Timebase > Sec/DIV > 50ns > Trigger > Trigger Mode to State Trigger On Negative Edge; On Chan 2; When Pattern H - XX)

3. Set Start Marker to 0ns; Stop Marker to 40ns: (Delta t > T Markers to On > Start Marker > 0ns > Stop Marker > 40ns >

4. Adjust with Al R4 so that the trailing edge of the PHI 2 signal is 40ns ahead of the trailing edge of the tristate ramp as shown below.

NOTE

There is no PHI 2 adjustment on the 8181B Multiplexer Board.

---

Figure 4-4. PHI 2 Adj

Revision 1.0, Dec. 1987
Adjustment Procedure 8181A/B

Figure 4-5. A1 Multiplexer Board
4-4 Locating Components in the 8181A Extender

The following diagrams are component/testpoint locators for the 8181A Data Extender.
Figure 4-6. A1 Multiplexer Board
Figure 4-8. A6 Module Board
Figure 4-9. A8 Address Control III
Figure 4-10. A12 Mother Board
Figure 4-11. A21 Power Supply Motherboard
Figure 4-12. A22 Rectifier Board
Figure 4-13. A23 Switching Board
Figure 4-14. Post Regulator Board
A 26 REGULATOR BD +15V, -7.5V 08180-65526

Figure 4-15. A26 Post Regulator Board
A27 23V, 15V REGULATOR BOARD 08180-66527

Figure 4-16. A27 Post Regulator Board
Chapter 5
8182A/B Adjustment Procedures

5-1 Introduction

This chapter covers the adjustment procedures necessary for the HP 8182A and HP 8182B analyzers.

When performing a major adjustment of the instrument, it is recommended that the adjustments are carried out in the order given.

5-2 Display Control Board 08182-66530 (8182A/B)

Display Adjustment

If the display has to be completely adjusted (after a CRT change), set A34R3 (on Motherboard) clockwise and all other potentiometers to mid range. Position the deflection yoke nearest to the screen and fasten it lightly.

1. Remove A32J4 (Vertical Deflection Board) and turn the instrument on.
2. If necessary, slightly increase intensity with A32R37.
3. Using the two ring magnets on the deflection yoke, position the dot approximately 3 mm (1/8 in) above the centre of the screen.
4. Turn the instrument off, reconnect A32 J4, turn it back on and press Al (A61) S2.
5. Select the test pattern: (Pages > Miscellaneous > Right upper blank softkey > enter 8182 from the Data keys > Disp Adjust).
6. Adjust A32R21 (Freq.) for a stable display.
7. Center the test pattern with A34RI (Hor. Pos.) and adjust A34L2 (Hor. Lin.) for maximum horizontal deflection.
8. Adjust A34R3 (Hor. Sync) so that no intensified lines appear.
9. Adjust A34L4 (Hor. Amp.) for approximately 12.5 cm (5 in) horizontal deflection.
10. Re-adjust A34L2 for best horizontal linearity.
11. Re-center the test pattern with A34R1 and repeat steps 8 to 10.
12. Adjust A32R27 (Vert. Amp.) for approximately 9 cm (3 1/2 in) vertical deflection.
14. Re-adjust and fasten the deflection yoke and repeat steps 2 to 13, if necessary.
15. Correct any 'pin cushion' distortion by adding small correction magnets to the deflection yoke.

Intensity and Focus Adjustment

16. Press Al (A61) S2 and select Brightness on the Miscellaneous Page: (Pages > Miscellaneous > Brightness > Increase [until maximum brightness is obtained]).
17. Adjust A32R37 (Intens.) until the line flyback is no longer visible.


19. Secure the ring magnets, deflection yoke and correction magnets with silicon compound.
Figure 5-1. A32 Vertical Deflection Board
Figure 5-2 A34 High Voltage Board
Figure 5-3. A61 Microprocessor Board
5-3 Microprocessor Board 08182-66501 (8182A)

Restart Circuit Adjustment

Equipment:

Oscilloscope with probes HP 54100D
Digital Voltmeter, testleads HP 3456A

1. Connect the DVM to VPower Down TP and GND TP.
2. Connect the oscilloscope probe to RES TP and GND TP.
3. Adjust A1 R133 for a 4.8V reading on the DVM. This simulates a decreasing supply voltage.
4. Adjust A1 R117 slowly until the RES signal toggles from high to low.
5. Recheck 4.8V and readjust A1 R133 and A1 R117 if necessary.
6. Turn A1 R133 fully clockwise and then slowly counter-clockwise until the RES signal toggles.
7. If the signal does not toggle at 4.8V ±0.002V repeat steps 3 to 6.
8. Turn A1 R133 back clockwise to get the normal supply voltage (< 5V) at the VPower Down TP.
Digital-Analog Converter Adjustment

Equipment:
Digital Voltmeter, testleads HP34S6A

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Label A +10V: (Pages > Input > Threshold > 10 > Volt)
3. Connect DVM to A5 (A65) TP22 and the nearest GND TP on one of the A5 (A65) Data Boards.
4. Adjust A2 (A62) R115 for -5.000V.
5. Program Label A -10V: (-10 > Volt).
6. Adjust A2 (A62) R111 for +5.000V.
7. Recheck the voltage at A5 (A65) TP22 with threshold Label A programmed to +10V, 0V and -10V in turn. The voltages should be -5V ±3mV, 0V ±3mV, and +5V ±3mV respectively. Repeat steps 2 to 6 if necessary.

Internal Clock Generator Adjustment

Equipment:
Oscilloscope HP54100A

1. Program Clock Source Internal: (Pages > Control > Clock > Clock Source > Internal)
2. Connect the scope probe to A2 (A62) TP14 and GND TP and adjust A2 (A62) C124 for the cleanest waveform.
Figure 5-5. A62 Interface Board
External Trigger Arm Amplifier Adjustment

Equipment:

Scope 54100D
Active Pods 54001A
Pulse Generator (Risetime <2.5 ns)
50 Ohm Feedthrough 10100C
BNC Cable
BNC Tee Connector 1250-0781
BNC scope probe Adapter 1250-1454
Extender Board 08180-66552

Measurement setup:

![Diagram of measurement setup]

Figure 5-6. External Trigger Arm Amp Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 KHz (20 microsec) squarewave and 2.5V amplitude (2.5V into 50 Ohm, min rise and fall time, offset off).
3. Connect equipment as shown in measurement set up.
4. Connect scope to TP1 and ground TP without using a ground lead (remove insulating sleeve from the probe).
5. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split screen t Off > Chan 2 > Volt/DIV > 100 mV)

Trigger Arm Amplifier Offset Adjustment

7. Disconnect equipment from the 8182A/B and terminate Trigger Arm Input with 50 Ohm.
8. Program 8182A/B Trigger Arm Pos Slope; Threshold 0.0V: (Pages > Control > Trigger > Trg Arm > Slope > Pos Slope > Exit > Threshold > 0 > Volt)
9. Connect scope probe to TP3 and adjust A3 (A63) R1 until the signal toggles.
External Stop Amplifier Adjustment

Equipment:

- Scope: 54100D
- Active Pods: 54001A
- Pulse Generator: (Risetime ≤2.5 ns)
- 50 Ohm Feedthrough: 10100C
- BNC Cable
- BNC Tee Connector: 1250-0781
- BNC scope probe Adapter: 1250-1454
- Extender Board: 08180-66552

Measurement setup:

![Diagram of equipment setup]

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 kHz (20 µs) squarewave and 2.5V amplitude (2.5 V into 50Ω, min. rise and fall time, offset to off).
3. Connect equipment as shown in the measurement setup.
4. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split screen to Off > Chan 2 > 2 Volt/DIV > 100 mV)

External Stop Amplifier Offset Adjustment

7. Disconnect equipment from the 8182A/B and terminate Stop Input with 50 Ω.
8. Program 8182A/B Stop Pos. Slope; Threshold 0.0V: (PAGES > Control > Stop > Stop Slope > Pos. Slope > Exit > Stop Thres. > 0 > Volt )
9. Connect scope probe to TP4 and adjust A3 (A63) R2 until the signal toggles.
Figure 5-8. A63 Address Board
Trigger Qualifier Adjustment

Equipment:

- Scope 54100D
- Active Pods 54001A
- Pulse Generator (Risetime ≤ 2.5 ns)
- 50 Ohm Feedthrough 10100C
- BNC Cable
- BNC Tee Connector 1250-0781
- BNC scope probe Adapter 1250-1454

Measurement setup:

- A4 TP10 +GND → 8182A/B
- 8182A/B → 10100C
- 10100C → PULSE GENER. OUTPUT
- BNC CABLE TO TRIGGER QUAL IN 1250-0781
- 1250-0781 → 1250-1454
- 1250-1454 → 54100D INPUTS

Figure 5-9. Trigger Qualifier Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 50 KHz (20 microsec) squarewave and 2.5V amplitude (2.5V into 50 Ohm, min rise and falltime, offset off).
3. Connect equipment as shown in the measurement setup.
4. Connect scope to TP10 and ground TP without using a ground lead (remove insulating sleeve from the probe).
5. Set scope to: (Autoscale > Chan 1 > Chan 1 Display to Off > Display > Split screen t Off > Chan 2 > Volt/DIV > 100 mV)
Trigger Qualifier Offset Adjustment

7. Disconnect equipment from the 8182A/B and terminate trigger qualifier input with 50 Ohm.

8. Program 8182A/B Trigger Qualifier High Level; Threshold 0.0V: (Pages > Control > Trigger > Trg. Qualifier > Level > High Level > Exit > Threshold > 0 > Volt)

9. Connect scope probe to TP11 and adjust A4 (A64) R215 until the signal toggles.

Control Output Adjustment

Equipment:

Digital Voltmeter, testleads HP 3456A

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

2. Connect DVM to A4 (A64) TP14 and next ground TP and adjust A4 (A64) R316 for 0V ±0.05V.
Control Board 08182-66504 (8182A) 08182-66564 (8182B)

Figure 5-11 A64 Control Board

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Clock Output Amplifier Offset Adjustment

Equipment:

Digital Voltmeter, testleads
BNC cable
BNC(f) dual banana plug

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

2. Connect DVM to the Clock Out connector (rear panel) and adjust A6 R616 for 0V ±0.05V. (Clock input remains open.)

Timing IC Supply Voltage Adjustment

Equipment:

Digital Voltmeter, testleads

1. Connect DVM to TP5 and TP6 (GND) and adjust A6 R474 to -5.2V ±0.05V.

Clock Amplifier Adjustment

Equipment:

Pulse Generator (f_{min}=10Hz, f_{max}=10Mhz, tr<3ns)
Scope
Active Pods
Extender Board (8182A)
Extender Board (8182B)
BNC Adapter
50 Ohm Feedthrough
Clock Probe

Measurement setup:

Figure 5-12. Clock Amplifier Adjustment
Clock Board 08182-66506 (8182A/B)

Low Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

2. Set Pulse Generator to: 10Hz, Squarewave, LOL=0V, HIL=2.5V, 2.5V into 50 Ohm.

3. Connect equipment as shown in the measurement set up.

4. Connect scope probe to TP2 and TP3 (GND). Do not use a ground lead. Remove insulating sleeve from probe.

5. Set scope to: (Autoscale).


High Frequency Response Adjustment

7. Set Pulse Generator to: 10MHz, Squarewave, LOL=0V, HIL=2.5V, 2.5V into 50 Ohm, transition <3ns.

8. Connect scope probe to TP2 and TP3 (GND). Do not use a ground lead. Remove insulating sleeve from the probe.

9. Set scope to: (Autoscale > Timebase > Sec Div > 2ns)

10. Adjust A6 C360 for best pulse response.
Clock Amplifier Offset Adjustment

Equipment:

- Pulse Generator
- Scope: HP 54100D
- Active Pods: HP 54001A
- BNC Tee connector: 1250-0781
- BNC Adapter (female/female): 1250-0080
- BNC scope probe Adapter: 1250-1454
- 50 Ohm Feedthrough: HP 10100C
- BNC Cable
- BNC Adapter: HP 15409A
- Clock Cable: HP 15406A

Measurement setup:

1. Set Pulse Generator to:
   - Period: 1ms
   - Pulse Width: 0.5ms
   - Amplitude: 200mV symmetrically to 0V
   - Transition Time: 5µs to 250 µs

2. Adjust leading edge and trailing edge for a triangular waveform. Using the offset vernier, set the signal to be symmetrical about the center graticule line.

3. Program 8182A/B to Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute Pages > Control > Operatg Mode > Trg Start Comp > Execute)

4. Set Sampling Clock Slope to Both Slopes; Clock Threshold 0.00V: (Pages > Control > Clock > Clock Slope > Both Slps > Exit > Clock Thresh 0V > Exit > Clock Width > 50 Microsec)

5. Connect equipment as shown in measurement set up.
6. Set scope to: (Autoscale > Chan 2 > Chan 2 Display Off > Display > Split Screen Off > Trigger > Trigger Src > to Trig 3)

7. Check if generator signal is symmetrical about the center graticule line. Set the Start Marker to the crossover point / positive going transition and the Stop Marker to the crossover point / negative going transition and perform Delta t measurement: (Delta t > Tmarkers on > Start Marker > Knob > Stop Marker > Knob)

8. Switch channel 1 off and channel 2 on: (Chan 1 > Chan 1 Display to off > Chan 2 > Chan 2 Display to on)

9. Adjust A6 R353 until measured time difference between the positive going edges of the displayed pulses shows the value measured in point 7.
Figure 5-15. Clock Amp Offset Adjustment - Scope Display 2

Ch. 2 = 1.000 volts/div
Offset = 2.400 volts
Timebase = 200 us/div
Delay = 0.00000 s
Start = 264.000 us
Delta T = 508.000 us
Stop = 772.000 us
Clock Board 08182-66506 (8182A/B)

Clock Qualifier Adjustment

Equipment:

- Pulse Generator (Risetime ≤ 2.5 ns)
- HP54100D
- Scope
- HP54001A
- Active Pods
- HP10100C
- 50 Ohm Feedthrough
- BNC cable

Measurement setup:

![Diagram of measurement setup]

Figure 5-16. Clock Qualifier Adjustment

Frequency Response Adjustment

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

2. Set Pulse Generator to 50 kHz, (20 microsec.) squarewave and 2.5V amplitude. (2.5 V into 50 Ohm, min. rise and fall time, offset to Off)

3. Connect equipment as shown in the measurement set up.

4. Connect scope probe to TP1 and TP4 (GND). Do not use a ground lead. Remove insulating sleeve from probe.

5. Adjust A6 C304 for best pulse response (square wave).
Clock Board 08182-66506 (8182A/B)

Figure 5-17. Frequency Response Adjustment - Scope Display
Clock Qualifier Offset Adjustment

Equipment:
 Pulse Generator                      HP 54100D
 Scope                                HP 54001A
 Active Pods                          HP 10100C
 BNC Tee connector                   1250-0781
 BNC scope probe adapter             1250-1454
 50 Ohm Feedthrough                   HP 15406A
 BNC cable                            1250-1454
 Clock cable                          HP 15408A
 Grabber                              HP 15408A

Measurement setup:

1. Set Pulse Generator to:
   - Period: 1ms
   - Pulse Width: 0.5ms
   - Amplitude: 200mV
   - Offset: On
   - Transition Time: 5µs to 250µs

2. Adjust Leading Edge and Trailing Edge for a triangular waveform. Using the Offset Vernier set
   the triangular signal to be symmetrical about 0 Volts.

3. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

4. Set the Operating Mode to Trigger Start Compare; Clock Source to External: Both Clock Slopes to
   Active; Clock Threshold to -1.2V: (Pages > Control > Operatg Mode > Trg Strt Comp > Execute >
   Exit > Clock > Clock Source External > Exit > Clock Slope > Both Slps > Exit > Clock Thres >
   -1.2V)

5. Set Clock Qualifier to Don’t Care; Threshold 0V: (Clock Qual > Level > Don’t Care > Exit >
   Threshold > 0.00V)
6. Set Clock Width to 100 microsec (Exit > Exit > Clock Width > 100 > Microsec)

7. Connect equipment as shown in measurement set up.

8. Set scope to: (Autoscale > Trigger > Trig Src to Chan 2 > Chan 2 > Chan 2 Disp to Off > Display > Split Screen to Off > Chan 1 > Offset > 0.00V)

9. Set Timebase to 100 ns and display mode to average: (Timebase > Sec/Div > 100 ns > Display Mode to Averaged > Number of Averages to 2 > Knob)

10. Set scope into magnify mode: (Chan 1 > Chan 1 Mode to Magnify > Magnify On > Volts/DIV to 20 mV using the Knob)

11. Adjust A6 R319 so that the dotted band on the screen is symmetrical about the center graticule line.
Figure 5-20. Clock Qualifier Adjustment - Scope Display 2
Figure 5-21. A66 Clock Board

5-26
Revision 1.0, Dec. 1987
Fixed Delay Adjustment

Equipment:

Scope: HP 54100D
Active Pods: HP 54001A
Pulse Generator: 08180-66552
Extender Board: 1250-0781
BNC Connector: HP 15409A
BNC Scope Probe Adapter: 1250-1454
Delay Line: 08182-61622

Measurement setup:

1. Cancel out interchannel delay and trigger delay of scope.
2. Set Pulse Generator to:
   - Period: 1 microsec
   - Pulse Width: 0.5 microsec
   - Leading Edge: < 3ns
   - HIL: 2.00 V
   - LOL: 0.00 V into 50 Ohm
3. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
4. Clock Threshold 1.00V: (Pages > Control > Clock > Clock Thres > 1 > Volt)
5. Connect equipment as shown in measurement set up.
6. Set scope to:
   - Channel 1: 200mV/DIV
   - Channel 2: 500mV/DIV; Offset 1V
   - Trigger: on Channel 2; Trigger level 1V
   - Split Screen: Off
   (Autoscale > Chan 1 > Volt/DIV > 200mV > Chan 2 > Volt/DIV > 500mV > Offset > 1V > Trigger > Trg Src to Chan 2 > Trigger Level > 1V > Display > Split Screen to Off)
7. Adjust Channel 1 Offset so that the base line of channel 1 meets the base line of channel 2. (Chan 1 > Offset > Knob)

Figure 5-23. Fixed Delay Adjustment - Scope Display I
Clock Board 08182-66506 (8182A/B)

8. Set Timebase to 500 ps. (Timebase > 500 ps)

9. Adjust A6 R215 for zero delay of both signals measured at the center graticule line.

---

Figure 5-24. Fixed Delay Adjustment - Scope Display 2
Clock Board 08182-66506 (8182A/B)

Clock Delay Adjustment

Equipment:

Scope 
Active Pods 
Pulse Generator 
BNC Tee Adapter 
50 Ohm Feedthrough 
BNC scope probe Adapter 
BNC Adapter 
Clock Probe

Measurement setup:

1. Set Pulse Generator to:
   - Period: 100 microsec
   - Pulse Width: 1.5 microsec
   - Transition Time: 2 ns
   - HIL: 2.5 V
   - LOL: 0.00V into 50 Ohm

2. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

3. Clock Threshold 1.2 V Clock Delay 0.00ns: (Pages > Control > Clock > Clock Thres > 1.2 > Volt > Exit > Clock Delay > 0 > Nanosec)

4. Connect equipment as shown in measurement set up.

5. Set scope to: (Autoscale > Trigger > Trg Src To Chan 1 > Chan 1 > Chan 1 Display to Off > Display > Split Screen to Off > Chan 2 > Volt/DIV > 500mV > Offset > 1.25V Timebase > Sec/DIV > 20 ns)

6. Set 50% point of positive going transition to center graticule line: (Delta V > V markers to Chan 2 > Auto Top Base > 50-50% > Chan 2 > Offset > Knob)

7. Move the pulse so that the 50% point of the positive going transition crosses the center horizontal and vertical graticules: (Timebase > Sec/DIV > 1ns > Delay > 38ns > Knob)
8. Set the Start Marker to 50% point of positive going transition: (Delta t > T Markers to On > Start Marker > Knob)

![Clock Board Diagram]

Ch. 2 = 500.0 mvolts/div  
Timebase = 1.00 ns/div  
Start = 37.640 ns  
Vmarker1 = 1.280 volts

Offset = 1.280 volts  
Delay = 37.640 ns  
Stop = 41.140 ns  
Vmarker2 = 1.280 volts  
Delta T = 3.500 ns  
Delta V = 0.000 volts

Figure 5-26. Clock Delay Adjustment - Scope Display 1

NOTE

The position of the start marker is used as the reference for the delay adjustment and should therefore not be moved during the following adjustments.

9. Program 8182A/B Clock Delay 5.9 ns: (Pages > Control > Clock > Clock Delay > 5.9 > Nanosec)

10. Add to the programmed delay the zero delay (position of the Start marker) and program the Stop Marker to this value.
    Example: Start marker position = 40ns, then Stop Marker = 45.9ns. Adjust Timebase Delay until the Stop Marker crosses the vertical center line.

11. Adjust A6 R213 (D1) so that the 50% point of the positive going transition crosses the center graticules (X & Y).
Clock Board 08182-66506 (8182A/B)

12. Repeat step 9 through to 11 with the following values:

<table>
<thead>
<tr>
<th>Programmed Clock Delay</th>
<th>Adjust</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 ns</td>
<td>A6 R228 (D2)</td>
</tr>
<tr>
<td>21.9 ns</td>
<td>A6 R227 (D3)</td>
</tr>
<tr>
<td>22 ns</td>
<td>A6 R266 (D4)</td>
</tr>
<tr>
<td>117 ns</td>
<td>A6 R276 (D5)</td>
</tr>
<tr>
<td>10 µs</td>
<td>A6 R268 (D6)</td>
</tr>
</tbody>
</table>

Increase Pulse Generator Period to 150 µs.

| 99.9 µs | A6 R277 (D7) |
| 118 ns  | A6 R290 (D8) |

![Scope Display 2](image)

Figure 5-27. Clock Delay Adjustment - Scope Display 2

Clock Width Adjustment

**Equipment:**

- Scope: HP 54100D
- Active Pods: HP 54001A
- Pulse Generator: HP 15406A
Clock Board 08182-66506 (8182A/B)

BNC Adapter
50 Ohm Feedthrough
Scope probe Adapter

Measurement setup:

1. Set Pulse Generator to:
   - Period: 100 µs
   - Pulse Width: 1.5 µs
   - Transition Time: 2 ns
   - HIL: 2.5 V
   - LOL: 0.0 V into 50 Ohm

2. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

3. Trigger Event Start Compare: (Pages > Control > Operating Mode > Trg Strt Comp > Execute)

4. Clock Width 10 ns: (Pages > Control > Clock > Clock Width > 10 > Nanosec)

5. Connect equipment as shown in measurement set up.

6. Cancel out trigger delay on scope channel 1.

7. Set scope to: (Autoscale > Delta V > V Markers to Chan 1 > Auto Top Base > 50-50%)
   Adjust displayed 50% level with Knob so that it crosses the center graticule: (Chan 1 > Offset > Knob)

8. Set Start Marker to 0.00 ns and check that 50% of the positive going transition crosses the center graticules (X & Y).
   If not, check trigger delay offset: (Timebase > Sec/DIV > 1 ns > Delata t > T markers to On > Start Marker > 0)
**NOTE**

The position of the start marker is used as reference for the width adjustment and should therefore not be moved during the following adjustment.

Figure 5-29. Clock Width Adjustment - Scope Display 1

9. Set Timebase Delay to 10 ns (Timebase > Delay > 10 ns)
10. Adjust A6 R244 so that the 50% point of the negative going transition crosses the center graticules.

Figure 5-30. Clock Width Adjustment - Scope Display 2

11. Repeat step 9 and 10 for the listed Clock Width values and perform the corresponding adjustment.

<table>
<thead>
<tr>
<th>8182A/B</th>
<th>Adjust</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Width</td>
<td></td>
</tr>
<tr>
<td>16.9 ns</td>
<td>A6 R242 (W1)</td>
</tr>
<tr>
<td>17.0 ns</td>
<td>A6 R254 (W2)</td>
</tr>
<tr>
<td>31.9 ns</td>
<td>A6 R253 (W3)</td>
</tr>
<tr>
<td>32.0 ns</td>
<td>A6 R272 (W4)</td>
</tr>
<tr>
<td>127 ns</td>
<td>A6 R278 (W5)</td>
</tr>
<tr>
<td>10.0 µs</td>
<td>A6 R273 (W6)</td>
</tr>
<tr>
<td>99.9 µs</td>
<td>A6 R279 (W7)</td>
</tr>
<tr>
<td>128 ns</td>
<td>A6 R291 (W8)</td>
</tr>
</tbody>
</table>

Increase Pulse Generator Period to 150 microsec.

Table 5-1 summarizes the adjustments that are to be performed on the Clock Board.
## Clock Board 08182-66506 (8182A/B)

### Table 5-1. Clock Board Adjustments

<table>
<thead>
<tr>
<th>Adjustment</th>
<th>Adjust</th>
<th>Adjust for:</th>
<th>Measured at:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Out Offset</td>
<td>R616</td>
<td>0V +/- 0.05V</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Amplifier LF</td>
<td>R341</td>
<td>best pulse response</td>
<td>TP2 TP3</td>
</tr>
<tr>
<td>Clock Amplifier HF</td>
<td>C360</td>
<td>best pulse response</td>
<td>TP2 TP3</td>
</tr>
<tr>
<td>Clock Amplifier Offset</td>
<td>R353</td>
<td>(A) both traces symm. to 0V</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Qual. Freq. Resp.</td>
<td>C304</td>
<td>best pulse response</td>
<td>TP1 TP4</td>
</tr>
<tr>
<td>Clock Qualifier Offset</td>
<td>R319</td>
<td>Less intens. pt. symm. to 0V</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Fixed Clock Delay</td>
<td>R215</td>
<td>zero delay of both signals</td>
<td>TP13 GND</td>
</tr>
<tr>
<td>Timing IC Supply</td>
<td>R474</td>
<td>-5.2V +/- 0.05V</td>
<td>TP5 TP6</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R213</td>
<td>5.90 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R228</td>
<td>6.00 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R227</td>
<td>21.9 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R266</td>
<td>22.0 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R276</td>
<td>117 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R268</td>
<td>10.0 us</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R277</td>
<td>99.9 us</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>R290</td>
<td>118 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R244</td>
<td>10.0 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R242</td>
<td>16.9 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R254</td>
<td>17.0 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R253</td>
<td>31.9 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R272</td>
<td>32.0 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R273</td>
<td>127 ns</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R279</td>
<td>10.0 us</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R291</td>
<td>99.9 us</td>
<td>Clock Out</td>
</tr>
<tr>
<td>Clock Width</td>
<td>R291</td>
<td>128 ns</td>
<td>Clock Out</td>
</tr>
</tbody>
</table>
Input Amplifier Adjustment

Equipment:

Scope HP 54100D
Active Probe HP 54001A
Pulse Generator (Fmin=10Hz; Fmax=10MHz; tr<3ns)
Extender Board 08180-66552
50 Ohm Feedthrough HP 10100C
BNC Adapter HP 15409A
DATA Probe HP 15407A

NOTE

The following procedure describes the low and high frequency adjustment for Data Board 0 Channel 0. Adjustments for the other boards and channels are listed in the adjustment summary.

If you wish to do adjustments for one connector at a time use adjustment summary at the end of this section.

If you wish to do adjustments for one board at a time use adjustment summary at the end of this section.

Measurement setup:

Figure 5-32. Input Amplifier Adjustment

Low Frequency Response Adjustment

1. Program 8182A/B Standard Set (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Set Pulse Generator to 10Hz squarewave and 2.5V amplitude into 50 Ohm
3. Connect equipment as shown in measurement set up.
4. Connect scope probe to TPI and GND TP without using a ground lead. (Remove insulating sleeve from probe.)

5. Set scope to (Autoscale > Chan 1 > Volts/Div > 100mV)


**High Frequency Response Adjustment**

7. Set Pulse Generator to 10MHz squarewave and 2.5V amplitude into 50 Ohm, risetime <3ns)

8. Connect equipment as shown in measurement set up.

9. Connect scope probe to TPI and GND TP without using a ground lead.

10. Set scope to: (Autoscale > Chan 1 > Volts/Div > 100mV)


**Data Input Amplifier Offset Adjustment**

**Equipment:**

- Scope: HP 54100D
- Active Pods: HP 54001A
- Pulse Generator
- BNC Tee Connector: 1250-0781
- BNC scope probe adapter: 1250-1454
- 50 Ohm Feedthrough: HP 10100C
- Clock Probe: HP 15406A
- DATA Probe: HP 15407A
- Grabber: HP 5408A

**Measurement setup:**

![Diagram of measurement setup](image)

Figure 5-33. Data Input Amplifier Offset Adjustment

1. Set Pulse Generator to:
   - Period: 1 ms
   - Pulse Width: 0.5 ms
2. Adjust Leading Edge and Trailing Edge for a triangular waveform. Using the offset vernier, set the triangular signal to be symmetrical about the center graticule line.

Figure 5-34. Data Input Amplifier Offset Adjustment - Scope Display 1

3. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

4. Clock Slope Both; Clock Threshold -1.3 V: (Pages > Control > Clock > Clock Slope > Both Slopes > Exit > Clock Thres > -1.3V)

5. Label A Single Threshold 0V: (Pages > Input > Threshold > 0 > Volt)

6. Connect equipment as shown in measurement set up.

7. Connect Clock Probe to AS (A65) TP5.
8. Set scope to: (Autoscale > Trigger > Trigger source to Chan 2 > Chan 2 > Chan 2 Display to Off > Display > Split Screen to Off > Number of Averages to 2 > Timebase > 100ns > Chan 1 > Chan 1 Mode to Magnify > Magnify to On > Volts/Div > 10mV)  

10. Adjust A5 (A65) R1 until the displayed band of dots is symmetrical to the center graticule line. Adjustments for all other data channels are listed in the Adjustment Summary.

---

**Figure 5-35 Data Input Amplifier Offset Adjustment - Scope Display 2**

**Dual Threshold Adjustment**

**Equipment:**

BNC Adapter (15409A) with 50 Ohm Feedthrough (10100C)
Solder in receptacles wired to short probe inputs
15407 Data Probe Assembly

1. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)
2. Clock Source Internal; Clock Period 1ms: (Pages > Control > Clock > Clock Source > Internal > Exit > Clock Period > Fast Increase [1ms])
3. Auto Arming Delay 0s: (Pages > Control > Autoarming > Delay 0s)
4. Stop Delay 40: (Pages > Control > Stop > Stop Delay > 40 > Enter Number)
Data Board 08182-66505 (8182A) 08182-66565 (8182B)

5. Glitch Detect On: (Pages > Control > Glitch Detect > On)

6. Lower Level -0.10V; Upper Level 0.00V: (for Label A) (Pages > Input > Threshold > Sing/upp/low [to lower] > 0.1 > Volt > Sing/upp/low [to upper] > 0 > Volt)

7. Dual Threshold for all available connectors: (Pages > Input > Connector > 0 and 1 > Dual Thres > Execute > Exit > [2 and 3] > Dual Threshold > Execute > Exit)

8. Timing Diagram: (Pages > Timing Diagr)

9. Press RUN.

Adjustment Channels 0 to 3 Connector 0

10. Connect 15407A Data Probe Assembly to Connector 0.

11. Terminate probe of channel to be adjusted (0) with 50 Ohm or short all probe inputs by using wired 15426A solder in receptacles.

12. Adjust A5 (A65) R9 for channel 0 on Data Board 0 until the timing display for Connector 0 Channel 0 toggles and maximum glitches are displayed.

13. Adjust R10 for channel 1 connector 0 on Data Board 0.

14. Adjust R9 for channel 2 connector 0 on Data Board 1.

15. Adjust R10 for channel 3 connector 0 on Data Board 1.

Adjustments for all channels are listed in the Adjustment Summary at the end of this section.

NOTE

When adjusting data channels on connector 6, move the Timing Diagrams Page display upwards until the required channel is displayed. With Timing Diagram selected press: (Select Displ > Vert Window).
Figure 5-36. A65 Data Board
5-10 Sampling Point Adjustment

Equipment:

- Pulse Generator
- Delay Line 3 ns
- BNC Adapter
- BNC Adapter (female/female)
- BNC Tee Adapter
- Clock Probe
- Data Probe

NOTE

The offset adjustment for line drivers A65 U108, A65 U208, A65 U308 and A65 U408 on the Data Board 08182-66565 can only be performed at the factory. Therefore never try to adjust A65 R11, A65 R12, A65 R13 and A65 R14.

Measurement setup:

1. Set Pulse generator to:
   - Period 1 µs
   - Pulse Width 0.5 µs
   - Leading Edge < 3 ns
   - Trailing Edge < 3 ns
   - HIL 2 V
   - LOL 0 V into 50 Ohm

2. Program 8182A/B Standard Set: (Pages > Miscellaneous > Recall > Standard Set > Execute)

3. Clock Threshold to +1 V: (Pages > Control > Clock > Clock Thres > 1 > Volt)

4. Label A Single Threshold to +1 V: ((Pages > Input > Threshold > Sing/Upp/Low[to Single Thres] > 1 > Volt)
5. Stop Delay to 40: (Pages > Control > Stop > Stop Delay > 40 > Enter Number)

6. Autoarming Delay 0s: (Pages > Control > Autoarming > Delay 0s)

7. Select Timing Diagrams: (Pages > Timing Diagram > Select Displ > Vert Window > <- or -> [until the required channel is displayed])

8. Using a mixed display, set Clock Delay to 3 ns: (Softkeys > Control > Clock > Clock Delay > 3 > Nanosec)

9. Connect equipment as shown in measurement set up and press RUN.

10. Using the Increment Softkey check first for a toggling action from low to high and note reading. If the signal does not toggle between 2 ns and 4 ns, perform Sampling Point Pre-adjustment.

11. Program Clock Slope Neg and select the Clock Delay softkey again: (Exit > Clock > Clock Slope > Neg Slope > Exit > Clock Delay)

12. Vary clock delay between 1 ns and 5 ns by pressing decrement and increment softkeys and note the delay when signal toggles from high to low.

13. Calculate delta between delay noted in step 10 (Clock Pos) and delay noted in step 12 (Clock Neg).

14. With negative Clock Slope selected set Clock Delay to 3 ns plus half of the delta delay calculated in step 13.

   Example:

   With Clock Slope Pos, signal switches from low to high at 1.8 ns. With Clock slope Neg, signal switches from high to low at 2.4 ns, Delta is 600 ps. Set Clock Delay to 3 ns plus 300ps = 3.3 ns.

15. Adjust A5 (A65) C5 until the signal toggles from high to low.

16. Reselect Clock Slope Pos: (Exit > Clock Slope > Pos Slope > Exit > Clock Delay)

17. Check that signal toggles between 2 ns and 4 ns. If signal does not toggle repeat the procedure from step 10.

**NOTE**

If the sampling point specifications cannot be reached by adjusting C5 it might be necessary to readjust the internal clock delay on the A6 clock board or to change the taps of delay line DL107 to DL407 on the Data Board.

**Sampling Point Pre-adjustment (DL107, DL207, DL307 and DL407)**

1. First check the sampling point of channels on the boards that have not been exchanged. If these channels are not in specifications refer to A6 Fixed Delay Adjustment.

2. If the other channels meet specifications, delayline DL107 [DL207, DL307, DL407] on the Data Board must be pre-adjusted.

3. Use the test set up and equipment settings as described under sampling point adjustment with the addition of a scope (54100D).

4. Trigger the scope with the pulse generator and connect the channel 1 probe to TP 5 on the DATA Board 0 (connector 0, channel 0)
5. Adjust A5 (A65) C5 for minimum delay as observed on scope.

6. Increment the clock delay from 0 ns onwards in 0.1 ns steps until the timing signal toggles, and note the delay difference to 3 ns.

7. The time difference between 3 ns and the noted delay setting is the required change in the setting of delayline DL107. Delay between two taps of the delay line is 1 ns; the delay range of A5 (A65) C5 is 0-1 ns.

Examples:

1. Minimum clock delay setting where the timing display can be forced to toggle is 1.3 ns. Time difference between 1.3 ns and 3 ns is 1.7 ns. Required action: Add 1 ns delay (1 tap) at DL107 and adjust A5 (A65) C5 to 0.7 ns.

2. Minimum clock delay setting where the timing display can be forced to toggle is 5.3 ns. Time difference between 5.3 ns and 3 ns is 2.3 ns. A5 (A65). Required action: Advance data by 3 ns (-3 taps) at DL107 and adjust C5 to +0.7 ns.
Table 5-2. 8182A/B Adjustments necessary after Board Change/Repair

<table>
<thead>
<tr>
<th>BOARD</th>
<th>EXCH. P/N</th>
<th>ADJUSTMENT (CHECK)</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display</td>
<td></td>
<td>Display Adjustment</td>
<td>5-1</td>
</tr>
<tr>
<td>A1 MPU Board</td>
<td>08182-69501</td>
<td>Restart Circuit</td>
<td>5-6</td>
</tr>
<tr>
<td>A2 Interface Bd.</td>
<td>08182-69502</td>
<td>D-A Converter</td>
<td>5-9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal Clock Generator</td>
<td>5-8</td>
</tr>
<tr>
<td>A3 Address Bd.</td>
<td>08182-69503</td>
<td>Trigger Arm Amplifier</td>
<td>5-10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Freq. Response/Offset</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Stop Amplifier</td>
<td>5-11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Freq. Response/Offset</td>
<td></td>
</tr>
<tr>
<td>A4 Control Board</td>
<td>08182-69504</td>
<td>Trigger Qualifier Amp.</td>
<td>5-13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Freq. Response/Offset</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Control Outputs</td>
<td>5-13</td>
</tr>
<tr>
<td>A5 Data Board</td>
<td>08182-69506</td>
<td>Input Amplifier Adjustment</td>
<td>5-38</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LF Response/HF Response/Offset</td>
<td>5-41</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Dual Threshold</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sampling Point</td>
<td>5-44</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Delay Line Preadjustment</td>
<td>5-45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Check Fixed Delay)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adjustments Summary</td>
<td>5-47</td>
</tr>
<tr>
<td>A6 Clock Board</td>
<td>08182-69506</td>
<td>Offset of Clock Output Circuit</td>
<td>5-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timing IC Supply</td>
<td>5-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock Amplifier</td>
<td>5-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LF Response/HF Response</td>
<td>5-16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock Amp. Offset Adjustment</td>
<td>5-18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock Qual. Frequency Response</td>
<td>5-21</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock Qual. Offset Adjustment</td>
<td>5-23</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fixed Delay</td>
<td>5-27</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock Delay</td>
<td>5-30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock Width</td>
<td>5-32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adjustment Summary</td>
<td>5-36</td>
</tr>
</tbody>
</table>

(*) Version A only.
**Table 5-3. 8182A/B Data Board Adjustments Summary**

<table>
<thead>
<tr>
<th>CONN. PROBE</th>
<th>CHANNEL PROBE</th>
<th>DATA BOARD</th>
<th>LF(10Hz) TEST PT.</th>
<th>ADJ. LF</th>
<th>HF(10MHz) TEST PT.</th>
<th>ADJ. HF</th>
<th>OFFSET ADJUST</th>
<th>DUAL THRESH.</th>
<th>DELAY LINE</th>
<th>DELAY ADJ.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>TP1</td>
<td>R2</td>
<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>TP3</td>
<td>R6</td>
<td>TP3</td>
<td>C3</td>
<td>R5</td>
<td>R10</td>
<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>1</td>
<td>TP1</td>
<td>R2</td>
<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>1</td>
<td>TP3</td>
<td>R6</td>
<td>TP3</td>
<td>C3</td>
<td>R5</td>
<td>R10</td>
<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>TP2</td>
<td>R4</td>
<td>TP2</td>
<td>C2</td>
<td>R3</td>
<td>DL207</td>
<td>TP6</td>
<td>CB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>TP4</td>
<td>R8</td>
<td>TP4</td>
<td>C4</td>
<td>R7</td>
<td>DL407</td>
<td>TP8</td>
<td>CB</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>1</td>
<td>TP2</td>
<td>R4</td>
<td>TP2</td>
<td>C2</td>
<td>R3</td>
<td>DL207</td>
<td>TP6</td>
<td>CB</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>1</td>
<td>TP4</td>
<td>R8</td>
<td>TP4</td>
<td>C4</td>
<td>R7</td>
<td>DL407</td>
<td>TP8</td>
<td>CB</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>2</td>
<td>TP1</td>
<td>R2</td>
<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2</td>
<td>TP3</td>
<td>R6</td>
<td>TP3</td>
<td>C3</td>
<td>R5</td>
<td>R10</td>
<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>3</td>
<td>TP1</td>
<td>R2</td>
<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>3</td>
<td>TP3</td>
<td>R6</td>
<td>TP3</td>
<td>C3</td>
<td>R5</td>
<td>R10</td>
<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>2</td>
<td>TP2</td>
<td>R4</td>
<td>TP2</td>
<td>C2</td>
<td>R3</td>
<td>DL207</td>
<td>TP6</td>
<td>CB</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>TP4</td>
<td>R8</td>
<td>TP4</td>
<td>C4</td>
<td>R7</td>
<td>DL407</td>
<td>TP8</td>
<td>CB</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>3</td>
<td>TP2</td>
<td>R4</td>
<td>TP2</td>
<td>C2</td>
<td>R3</td>
<td>DL207</td>
<td>TP6</td>
<td>CB</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>TP4</td>
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<td>TP8</td>
<td>CB</td>
</tr>
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<td>4</td>
<td>0</td>
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<td>TP1</td>
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<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>4</td>
<td>TP3</td>
<td>R6</td>
<td>TP3</td>
<td>C3</td>
<td>R5</td>
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<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>5</td>
<td>TP1</td>
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<td>TP6</td>
<td>DL107</td>
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<tr>
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<td>R10</td>
<td>TP8</td>
<td>DL107</td>
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<td>5</td>
<td>0</td>
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<td>TP2</td>
<td>R4</td>
<td>TP2</td>
<td>C2</td>
<td>R3</td>
<td>DL207</td>
<td>TP6</td>
<td>CB</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>4</td>
<td>TP4</td>
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<td>TP4</td>
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<td>DL407</td>
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<td>CB</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>5</td>
<td>TP2</td>
<td>R4</td>
<td>TP2</td>
<td>C2</td>
<td>R3</td>
<td>DL207</td>
<td>TP6</td>
<td>CB</td>
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<tr>
<td>5</td>
<td>3</td>
<td>5</td>
<td>TP4</td>
<td>R8</td>
<td>TP4</td>
<td>C4</td>
<td>R7</td>
<td>DL407</td>
<td>TP8</td>
<td>CB</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>6</td>
<td>TP1</td>
<td>R2</td>
<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>6</td>
<td>TP3</td>
<td>R6</td>
<td>TP3</td>
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<td>R5</td>
<td>R10</td>
<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>7</td>
<td>TP1</td>
<td>R2</td>
<td>TP1</td>
<td>C1</td>
<td>R1</td>
<td>R9</td>
<td>TP6</td>
<td>DL107</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>7</td>
<td>TP3</td>
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<td>R5</td>
<td>R10</td>
<td>TP8</td>
<td>DL107</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>6</td>
<td>TP2</td>
<td>R4</td>
<td>TP2</td>
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<td>TP6</td>
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</tr>
<tr>
<td>7</td>
<td>1</td>
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<td>TP4</td>
<td>R8</td>
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<td>C4</td>
<td>R7</td>
<td>DL407</td>
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<td>7</td>
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<td>7</td>
<td>TP4</td>
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<td>R7</td>
<td>DL407</td>
<td>TP8</td>
<td>CB</td>
</tr>
</tbody>
</table>

Note that the testpoints in column "DELAY ADJ." are also to be used for "OFFSET ADJUST."
Table 5-4. 8182A/B Data Connector Adjustments Summary

<table>
<thead>
<tr>
<th>DATA BOARD</th>
<th>CONN-</th>
<th>PROBE,</th>
<th>TEST</th>
<th>LF ADJUST 10 Hz</th>
<th>HF ADJUST 10MHz</th>
<th>OFFSET ADJUST</th>
<th>DUAL THRESH HOLD ADJUST</th>
<th>DELAY ADJUST</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>TP1</td>
<td>R2</td>
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<td>0</td>
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<td>0</td>
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<td></td>
<td>TP6 C7</td>
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<tr>
<td>1</td>
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<td>TP4</td>
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<td>TP8</td>
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<td></td>
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<td>6</td>
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<td>7</td>
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<td>TP8 C8</td>
<td></td>
</tr>
</tbody>
</table>

Note that the testpoints in column "DELAY ADJ." are also to be used for "OFFSET ADJUST".
5-11 Locating components in the 8182A Data Analyzer

The following diagrams should be used when locating components/testpoints in the HP 8182A Data Generator.
Figure 5-39. A2 Interface Board
Figure 5-43. A7 Mother Board
Figure 5-44. A24 Post Regulator Board
Figure 5-45. A26 Post Regulator Board
Figure 5-46. A21 Power Supply Mother Board
Figure 5-47. A22 Rectifier Board
Figure 5-48 A23 Switching Board
Figure 5-49. A30 Control Board
Figure 5-50. A32 Vertical Deflection Board
Figure 5-51. A34 Horizontal Deflection Board
Chapter 6
HP 8180A/B Performance Verification

6-1 Introduction

The test procedures described in this chapter are designed to verify the published performance specifications for the HP 8180A/B Data Generator and the HP 8181A/B Data Generator Extender given in Chapter 1 of this manual.

NOTE

The tested instrument must be given a 30 minute warm-up time before starting any of the performance tests. During any performance test, all shields, covers and connecting hardware must be in place. The tests must be performed in the order given.

Equipment Required

The equipment necessary to perform each performance test is listed at the beginning of each test. Alternative test equipment may be substituted for the recommended models, provided that it satisfies the critical specifications given.

Test Record

When carrying out the performance tests, you should keep a tabulated test record, listing the test results and the acceptable performance limits. The results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

6-2 Cycle Modes / Run / Stop / Break / Forward / Back Tests

For testing the different cycle modes, a low frequency (10Hz) is used in order to be able to follow the address changes on the 8180A/B display. The external gate signal is simulated by changing the threshold level of the RUN/GATED input. First and last address detection at maximum speed is tested separately.

1. Program 8180A/B Standard Set.
   (PAGES, WIND10, WIND20, WIND30, WIND40 )

2. Clock Frequency 10 Hz.
   (PAGES, WIND10, WIND20, WIND30, 10, WIND40 )

3. Last Address 100.
   (PAGES, WIND10, WIND20, WIND30, 100, WIND40 )

Auto Cycle Test

4. Press RUN and check that the 8180A/B starts with address 00000 (upper right hand corner of the display), counts up to address 00100 and continues with address 00000.

Break; Forward; Back; Stop Test

5. Press BREAK. The 8180A/B should switch to BREAK.

6. Increment and decrement addresses by pressing FWD and BACK. Note that addresses can be decremented down to the First Address.

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Cycle Modes / Run / Stop / Break / Forward / Back Test

7. Press RUN. The 8180A/B should start one address after the Break Address.

8. Press STOP and RUN. The 8180A/B should start with the First Address.

Single Cycle Test

9. Program the 8180A/B to Single Cycle.
   (PAGES, CONTROL, Cycle Mode, SINGLE)

10. Press RUN and check that the 8180A/B starts at address 00000 and stops at address 00100.

Gated Cycle Test

11. Program the following: Gated Cycle; Run (Gate) Input ON; Threshold +5V.
    (PAGES, CONTROL, Cycle Mode, Gated, Threshold, 5, Volts)

12. Set threshold voltage to -5V (-, 5, Volts). The 8180A/B should run between address 00000 and 00100 as in Auto Cycle.

13. Set the threshold voltage back to +5V. The 8180A/B should complete the last cycle and stop at address 00100.

Init+Gated Cycle Test

    (PAGES, CONTROL, Cycle Mode, INIT+GATED)

15. First Address 30.
    (PAGES, CONTROL, First Address, 30, ENTER NUMBER)

16. Input Threshold +5V.
    (PAGES, CONTROL, Inputs, Threshold, 5, Volts)

17. Program the threshold voltage to -5V (-, 5, Volts) and check that the 8180A/B starts with address 00000, runs up to address 00100 and continues cycling between address 00030 and 00100.

18. Set the threshold voltage back to +5V. The 8180A/B should complete the last cycle and stop at address 00100.

Init+Auto Cycle Test

19. Program Init+Auto.
    (PAGES, CONTROL, Cycle Mode, INIT+Auto)

20. Run Input OFF.
    (PAGES, CONTROL, Inputs, Run Input, OFF)

21. Press RUN and check that the 8180A/B starts at address 00000, runs up to address 00100 and continues cycling between address 00030 and 00100.

To repeat the whole sequence press STOP and RUN again.
6-3 Last Address (Address Difference Counter) Test

This test ensures correct programmability of the address difference counters and proper operation up to 50 MHz.

1. Program 8180A/B Standard Set.
   (PAGES, STORE/SAVE, RELICSEEK, EXECUTE)

2. Clock 2 Delay to 0ns, Clock 1 Width to 10ns.
   (PAGES, TIMING, CLOCK TIMING, CLOCK 2 DELAY, 0, NANOSecs, EXIT, CLOCK 1 WIDTH, 10, NANOSecs)

3. Clock Frequency 50 MHz.
   (PAGES, TIMING, FREQ, 50, MEGAHertz)

   (PAGES, CONTROL, CYCLE MODE, SINGLE)

5. Last Address 00001.
   (PAGES, CONTROL, LAST ADDRESS, 1, ENTER NUMBER)

6. Press RUN and check that the 8180A/B stops at address 00001.

7. Change Last Address to 2 (ENTER NUMBER) press RUN and check cycle length.

8. Repeat Single Cycle test with the following Last Address settings:
   8; 16; 32; 128; 256; 512; 1024; 2048; 4096; 8192. On the 8180A go up to 512.
Strobe Break (Strobe Difference Counter) Test

6-4 Strobe Break (Strobe Difference Counter) Test

Correct programmability and proper strobe difference counter function at 50 MHz is verified with this test. After setting the Strobe Breaks, the instrument is stepped from Break to Break.

1. Program 8180A/B Standard Set.  
   (PAGES, [STORE/RECALL], [REL. SET], [EXECUTE])
2. Clock 2 Delay to 0ns, Clock 1 Width to 10ns.  
   (PAGES, [TIMING], [Clock Timing], [clock 2 Delay], 0, [NANOSEG], [EXIT], [Clock 1 Width], 10, [NANOSEG])
3. Clock Frequency 50 MHz.  
   (PAGES, [Timing], [Frequency], 50, [MEGAHERTZ])
   (PAGES, [DATA], [Edit], [Clear & Set], [Clear Strobe], [EXECUTE])
5. Strobe Breaks ON.  
   (PAGES, [CONTROL], [break control], [Strobe Breaks], [ON])
   (PAGES, [DATA], [Edit], [Entry Mode], [VERTICAL], [EXIT])
7. Top Address 00000; Strobe Bit to 1.  
   (Top Address, 0, [ENTER NUMBER], [EXIT], 1)
8. Using the Cursor softkey move cursor to address 00001 and set strobe bit high by pressing the 1 key on the data entry keypad.
9. Set strobe bits to high in following addresses as described in step 8:  
   1; 2; 4; 8; 16; 32; 64; 128; 256; 512; 1024; 2048; 4096; 8192. On the 8180A go up to 512.
10. Press STOP and RUN. The 8180A/B should be in BREAK at address 00000.
11. Press RUN again and the 8180A/B should break at address 00001.
12. Check that the 8180A/B breaks at addresses 2; 4; 8; 16; 32; 64; 128; 256, 512, 1024, 2048, 4096, 8192 and 0 each time after pressing RUN again. On the 8180A check up to 512.
Internal Clock Frequency Test

6-5 Internal Clock Frequency Test

Specification

Accuracy: ±5% of programmed value.

Description

The Strobe output signal programmed as clock is used to measure the internal clock generator accuracy. Clock timing errors flagged up on the screen with Standard Set and 50 MHz programmed have no influence on the Strobe output.

Equipment

Universal Counter: HP 5370B
Plug-on BNC Adapter: HP 15409A
Clock and Strobe Cable Set: HP 15422A

Procedure

1. Set counter as follows.
   Trig Level: +1.2V
   FUNCTION: FREQUENCY
   GATE: 0.01s
   STOP IMP: 50 Ohm
   START COM switch: SEParate

2. Program 8180A/B Standard Set
   (PAGES , STORE/RECALL , STORE/STOR , EXECUTE )

3. Strobe Level TTL
   (PAGES , OUTPUT , STROBELEVEL , EXECUTE )

4. Strobe Output Clock; Outputs ON
   (PAGES , OUTPUT , STROBE/OUT , EXECUTE , 50 , EXECUTE )

5. Frequency 50 MHz
   (PAGES , EXECUTE , FREQUENCY , 50 , EXECUTE )

6. Connect equipment as shown in Figure 6-1 and press RUN.

Figure 6-1. Test Setup for the Internal Clock Frequency Test

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Internal Clock Frequency Test

7. Check 8180A/B internal clock generator at the set frequencies as detailed in Table 6-1.

Table 6-1. Internal Clock Frequency Test Values - Tested Frequencies

<table>
<thead>
<tr>
<th>Set Frequency</th>
<th>Min. Frequency</th>
<th>Max. Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>50.00 MHz</td>
<td>47.50 MHz</td>
<td>52.50 MHz</td>
</tr>
<tr>
<td>25.00 MHz</td>
<td>23.75 MHz</td>
<td>26.25 MHz</td>
</tr>
<tr>
<td>10.00 MHz</td>
<td>9.50 MHz</td>
<td>10.50 MHz</td>
</tr>
<tr>
<td>9.99 MHz</td>
<td>9.49 MHz</td>
<td>10.49 MHz</td>
</tr>
<tr>
<td>3.00 MHz</td>
<td>2.85 MHz</td>
<td>3.15 MHz</td>
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<tr>
<td>1.00 MHz</td>
<td>0.95 MHz</td>
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<td>1.05 Hz</td>
<td>1.00 Hz</td>
<td>1.10 Hz</td>
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</tbody>
</table>
6-6 Clock and Data Skew Test

Specification

Skew: ≤ 1.6 ns for Clock and Data channels.

Description

A Square Wave pattern is used to test the Clock channels and all installed Data channels. The Strobe clock signal is used as a reference, the maximum deviation from positive going Strobe transition should be ≤ ±0.8 ns. TTL levels are used for all outputs, the test is valid also for the 8181A/B NRZ Data channels.

Figure 6-2. Test Setup for the Clock and Data Skew Test

Equipment

Scope HP 54100D
Active Pods HP 54001A
Scope Probe Adapter 1250-1454
BNC Adapter female/female 1250-0080
BNC Adapter HP 15409A
50 Ohm Feedthrough HP 10100C
Strobe/Clock Cable Assy HP 15422A
Data Cable HP 15423A

Procedure

1. Program 8180A/B Standard Set.
   (PAGES , , , )

2. Label A TTL, Strobe TTL, Strobe to Clock.
   (PAGES , , , )

3. Clock 1 Format RZ=50%; Clock 2 Format RZ=50%; Clock 1 Delay 0 ns; Clock 2 Delay 0 ns.
   (PAGES , , , )

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Clock and Data Skew Test

1. First address 00000; Last Address 00001.
2. Set Data.
3. Connect the equipment as shown in Figure 6-2. Switch outputs ON and start the generator.
4. Press RUN.
5. Cancel out interchannel delay between scope channel 1 and scope channel 2.
6. Set scope as follows:
7. Connect in turn all Clock and Data channels to scope input 2 and store each displayed transition to Memory 1.
8. Set Start Marker to the 50% point of the displayed strobe transition and measure with the Stop Marker the maximum ± deviation of the stored channel transitions.
9. The maximum deviation should be ±0.8 ns (B-version); ±1 ns (A-version).
Clock 1, Clock 2 Delay Test

6-7 Clock 1, Clock 2 Delay Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

The clock delays are referenced to the Strobe clock output signal. Delays longer than 300ns are measured with a time interval counter.

![Diagram of test setup](image)

Figure 6-3. Test Setup for the Clock 1 and Clock 2 Delay Test

Equipment

Scope HP 54100D
Active Pods HP 54001A
Clock, Strobe Cable Assembly HP 15422A
BNC Adapter HP 15409A
50 Ohm Feedthrough HP 10100C
BNC Adapter female/female 1250-0080
Scope Probe Adapter 1250-1454
Counter HP 5370B

1. Program 8180A/B Standard Set.
   (PAGES, STORE/RECALL, REL. Std. Sets, EXECUTE)

2. Period 1 µs.
   (PAGES, PROGRAM, REL. Period, 1, EXECUTE)

3. Label A TTL; Strobe TTL; Strobe output to Clock.
   (PAGES, OUTPUT, LEVEL, DIFF. levels, EXECUTE, 
   SOURCE levels, COUNT. 
   PAGES, CONTROL, STROBE OUTPUT, EXECUTE)

4. Clock 1 and Clock 2 Format RZ = 50%; Clock 1 and Clock 2 Delay = 0.00 ns.
   (PAGES, PROGRAM, CLEAR, PROGRAM, COUNT. 
   PAGES, CONTROL, EXECUTE)
Clock 1, Clock 2 Delay Test

5. Outputs ON.

6. Clock 1 (2) Delay in Softkey Area and start the generator.

Connect the equipment as shown in Figure 6-3 and start the generator (press RUN).

Cancel out scope trigger delay of channel 2 and interchannel delay between scope channel 1 and channel 2.

7. Connect equipment as shown in the measurement setup and set the scope as follows:

(Autoscale > Trigger > Trig Src to Chan2 > Slope to pos > Timebase > 1ns > Display > Split Screen to OFF > Delta > T Markers to ON > Start Marker to 0.00ns (50% point of the positive going transition of the Strobe clock signal))

Note: The position of the start marker is used as reference for this test and should therefore not be moved during the measurement.

8. Set clock delay to 30 ns (30, 6127 6181, 6150, 6151).

9. Set the scope as follows:

(Timebase > Delay > 30ns > Delta t > Stop Marker > 30ns > Knob)

10. Position the Stop Marker at the 50% point of the displayed transition and read Delta t. Delta t must be in the following range:

- Delta t minimum = 27.5 ns
- Delta t maximum = 32.5 ns

11. Check also the clock delay for the settings detailed in Table 6-2.

<table>
<thead>
<tr>
<th>Set Delay</th>
<th>Min. Delay</th>
<th>Max. Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>89.9 ns</td>
<td>84.4 ns</td>
<td>95.4 ns</td>
</tr>
<tr>
<td>90.0 ns</td>
<td>84.5 ns</td>
<td>95.5 ns</td>
</tr>
<tr>
<td>300 ns</td>
<td>284 ns</td>
<td>316 ns</td>
</tr>
</tbody>
</table>

12. Disconnect the Strobe and Clock connections from the scope (between 15409A and 10100C) and connect Strobe cable to Start Input of the counter and the Clock 1 (2) cable to the Stop Input of the counter.

13. Set the counter as follows:

- Function: Time Interval
- Sample Size: 1
- Start/Stop input: Both Channels to 1.2 V
- Start/Stop slopes: $\uparrow$
- Start/Stop input impedance: 50 Ohm
- AC/DC switches to: AC
- Start COM/SEP switch: SEP
Clock 1, Clock 2 Delay Test

14. Change 8180A/B Clock Period to 200 ms and check delay at Clock 1 and 2 at settings given in Table 6-3:

(PAGES, TIMING, Period, 200, MILLISEC, EXIT, 4,
Clock Timing, Clock1 Delay [Clock2 Delay])

Table 6-3. Clock 1, Clock 2 Delay Test Values - Clock Delay at 200 ms Period

<table>
<thead>
<tr>
<th>Set Delay</th>
<th>Min. Delay</th>
<th>Max. Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>989 ns</td>
<td>938.5 ns</td>
<td>1039.5 ns</td>
</tr>
<tr>
<td>100 ms</td>
<td>95.0 ms</td>
<td>105.0 ms</td>
</tr>
</tbody>
</table>
Clock 1, Clock 2 Width Test

6-8 Clock 1, Clock 2 Width Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

The clock width is measured at 50% amplitude. Width ranges greater than 300 ns are measured with the counter.

![Test Setup for the Clock 1 and Clock 2 Width Test](image-url)

Figure 6-4. Test Setup for the Clock 1 and Clock 2 Width Test

Equipment

<table>
<thead>
<tr>
<th>Item</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scope</td>
<td>HP 54100D</td>
</tr>
<tr>
<td>Active Pods</td>
<td>HP 54001A</td>
</tr>
<tr>
<td>Clock, Strobe Cable Assembly</td>
<td>HP 15422A</td>
</tr>
<tr>
<td>BNC Adapter</td>
<td>HP 15409A</td>
</tr>
<tr>
<td>50 Ohm Feedthrough</td>
<td>HP 10100C</td>
</tr>
<tr>
<td>Scope Probe Adapter</td>
<td>1250-1454</td>
</tr>
<tr>
<td>Counter</td>
<td>HP 5370B</td>
</tr>
<tr>
<td>BNC Adapter female/female</td>
<td>1250-0080</td>
</tr>
</tbody>
</table>

Procedure

1. Program 8180A/B Standard Set (PAGES, STORE/RECALL, EXT Std Set, [EXECUTE])
2. Clock Period 1 µs (PAGES, EXT TIMING, EXT Period, 1, [MICROSEC])
3. Label A TTL (PAGES, EXT OUTPUT, TTL Level, TTL Level, [EXECUTE])
4. Outputs ON (PAGES, EXT OUTPUT, OUT on/off, OUT on)
5. Connect the equipment as shown in Figure 6-4 and press RUN.
6. Set the scope as follows: (Autoscale > Timebase > Sec/DIV > 500 ps)
Clock 1, Clock 2 Width Test

7. Set the Start Marker to the 50% point of the displayed positive going transition.
   (Delta t > T Markers to ON > Start Marker > Knob)

8. Set Clock 1 Width to 10 ns.
   (PAGES, "TIMING", Clock Timing, Clock 1 Width, 10, NANOSEC, EXIT.)

9. Set the scope as follows:
   (Timebase > Delay > 10 ns > Delta t > Stop Marker > Knob)

10. Adjust the Stop Marker to the 50% point of the negative going transition of the Clock 1 signal and read Delta t.  
    Delta t minimum = 8.5 ns  
    Delta t maximum = 11.5 ns

   Note: The position of the Start Marker is used as reference for the following measurements and should therefore not be moved.

11. Check step linearity when incrementing the width in 100 ps steps up to 20 ns.

12. Check clock width using the procedure described in steps 8 to 10 for the width settings given in Table 6-4.

13. Disconnect the clock connection between the 10100C and 1250-0080 and connect the 10100C to the Start Input of the counter.

14. Set the counter as follows:
    Function: Time Interval
    Sample Size: 1
    Start/Stop Input Levels: Preset
    Start slope to: S
    Stop slope to: I
    Start & Stop Input Imp: 1 MΩ
    AC/DC switches to: AC
    START COM/SEP switch: START COM
    Divider: divide by 10

15. Change 8180A/B Clock Period to 200 ms and check Clock 1 width at the settings given in Table 6-5.
   (PAGES, "TIMING", Clock Timing, Clock 1 Width, 10, NANOSEC, EXIT.)

Table 6-4. Clock 1, Clock 2 Width Test Values - Clock Width at 1 µs Period

<table>
<thead>
<tr>
<th>Set Width</th>
<th>Min. Width</th>
<th>Max. Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.0 ns</td>
<td>27.5 ns</td>
<td>32.5 ns</td>
</tr>
<tr>
<td>99.0 ns</td>
<td>93.0 ns</td>
<td>105.0 ns</td>
</tr>
<tr>
<td>100.0 ns</td>
<td>94.0 ns</td>
<td>106.0 ns</td>
</tr>
<tr>
<td>300.0 ns</td>
<td>284.0 ns</td>
<td>316.0 ns</td>
</tr>
</tbody>
</table>

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Clock 1, Clock 2 Width Test

Table 6-5. Clock 1, Clock 2 Width Test Values - Clock Width at 200 ms Period

<table>
<thead>
<tr>
<th>Set Width</th>
<th>Min. Width</th>
<th>Max. Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>999 ns</td>
<td>948 ns</td>
<td>1050 ns</td>
</tr>
<tr>
<td>100 ms</td>
<td>95.0 ms</td>
<td>105 ms</td>
</tr>
</tbody>
</table>

16. Perform the above procedures for Clock 2.
Timing Channel Delay Test

6-9 Option 002 Timing Channel Delay Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

Data channel delays are referenced to the Strobe Clock output signal. Delays greater than 300 ns are measured with a time interval counter.

![Test Setup for the Timing Channel Delay Test](image)

Figure 6-5. Test Setup for the Timing Channel Delay Test

Equipment

<table>
<thead>
<tr>
<th>Item</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scope</td>
<td>HP 54100D</td>
</tr>
<tr>
<td>Active Pads</td>
<td>HP 54001A</td>
</tr>
<tr>
<td>Counter</td>
<td>HP 5370B</td>
</tr>
<tr>
<td>Clock, Strobe Cable Assembly</td>
<td>HP 15422A</td>
</tr>
<tr>
<td>Data Cable set</td>
<td>HP 15423A</td>
</tr>
<tr>
<td>BNC Adapter</td>
<td>HP 15409A</td>
</tr>
<tr>
<td>50 Ohm Feedthrough</td>
<td>HP 10100C</td>
</tr>
<tr>
<td>BNC Adapter female/female</td>
<td>1250-0080</td>
</tr>
<tr>
<td>Scope Probe Adapter</td>
<td>1250-1454</td>
</tr>
</tbody>
</table>

Procedure

1. Program 8180A/B Standard Set.

2. Set Clock Period to 1 µs.

3. Label A TTL; Strobe TTL; Strobe Output to Clock.

4. Outputs ON.
Timing Channel Delay Test

5. Set Data.
(PAGES, PAGES, PAGES, PAGES, PAGES, PAGES, PAGES)

6. Connect the equipment as shown in Figure 6-5 and press RUN.

NRZ Function Test

7. Check all installed RZ channels listed on the Timing Page for a static TTL high level (greater than +2V).

8. Set All Channel Format to RZ.
(PAGES, PAGES, PAGES, PAGES)

Cancel out interchannel skew between scope channel 1 and channel 2 and the trigger delay of channel 2.

9. Set the scope as follows:
(Autoscale > Timebase > Sec/DIV > 500 ps > Trigger > Trg Src to Channel 2 > slope to Pos > Delta t > T Markers to ON > Start Marker > Knob)

10. Position the Start Marker to the 50% point of the positive going Strobe transition (0.00 ns).

   Note: The position of the Start Marker is used as reference for this test and should therefore not be moved during the measurement.

Delay Test

11. Set All Channel Delay to 10 ns.
(PAGES, PAGES, PAGES, PAGES, PAGES)

12. Set the scope as follows:
(Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF > Timebase > Delay > 10 ns > Delta t > Stop Marker > 10 ns > Knob)

13. Place the Stop Marker at the 50% point of the displayed positive going transition and read Delta t.
Delta t minimum = 8.5 ns
Delta t maximum = 11.5 ns

14. Check in turn all RZ Data channels.

15. Repeat steps 11 to 14 for the settings given in Table 6-6.

Table 6-6. Timing Channel Delay Test Values - Clock Period at 1 µs

<table>
<thead>
<tr>
<th>Set Delay</th>
<th>Min. Delay</th>
<th>Max. Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0 ns</td>
<td>8.5 ns</td>
<td>11.5 ns</td>
</tr>
<tr>
<td>30.0 ns</td>
<td>27.5 ns</td>
<td>32.5 ns</td>
</tr>
<tr>
<td>89.9 ns</td>
<td>84.4 ns</td>
<td>95.4 ns</td>
</tr>
<tr>
<td>90.0 ns</td>
<td>84.5 ns</td>
<td>95.5 ns</td>
</tr>
<tr>
<td>300 ns</td>
<td>284 ns</td>
<td>316 ns</td>
</tr>
</tbody>
</table>

16. Change the Clock Period to 200 ms.
(PAGES, PAGES, PAGES, PAGES, PAGES, PAGES, PAGES)

17. Disconnect the Strobe and Data cable from the scope (between 15409A and 10100C) and connect the cables to the counter inputs as shown in the measurement setup.

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Timing Channel Delay Test

18. Set the counter as follows:
   Function: Time Interval
   Sample size: 1
   Start/Stop levels: Both Channels to 1.2 V
   Start/Stop slope: $f$
   Input impedances: 50 $\Omega$
   AC/DC switches: AC
   Start CAM/SEP switch: SEP
   Input Divider: divide by 1

19. Check in turn all RZ Data channels for the delay settings given in Table 6-7.

Table 6-7. Timing Channel Delay Test Values - Clock Period at 200 ms

<table>
<thead>
<tr>
<th>Set Delay</th>
<th>Min. Delay</th>
<th>Max. Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>989.0 ns</td>
<td>938.5 ns</td>
<td>1039.5 ns</td>
</tr>
<tr>
<td>100.0 ms</td>
<td>95.0 ms</td>
<td>105.0 ms</td>
</tr>
</tbody>
</table>

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Option 002 Timing Channel Width Test

6-10 Option 002 Timing Channel Width Test

Specification

Accuracy: ±5% of programmed value ±1 ns

Description

The Data channel width is measured at 50% of amplitude. Width ranges greater than 300 ns are checked with the counter.

![Figure 6-6. Test Setup for the Timing Channel Width Test](image)

Equipment

Scope
Active Pods
Counter
Data cable set
BNC Adapter
50 Ω Feedthrough
BNC Adapter female/female
Scope Probe Adapter

HP 54100D
HP 54001A
HP 5370B
HP 15423A
HP 15409A
HP 10100C
1250-0080
1250-1454

Procedure

1. Program 8180A/B Standard Set.
   (PAGES, Store/Recall, Recall Set, EXECUTE)

2. Period 1 μs (PAGES, Timing, Period, 1, MICROSEC)

3. Label A TTL; Outputs ON.
   (PAGES, Output, Level, TTL, Level, EXECUTE, EXTEND, Scope on/off, ON)

4. Set Data.
   (PAGES, DATA, Set, Clear, Data, EXECUTE)

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Option 002 Timing Channel Width Test

5. All Channel Width 10 ns.
   (PAGES, 5, TIMING, ALL CH., ALL CH. Format, RZ, EXIT)

6. Connect the equipment as shown in Figure 6-6 and press RUN.
   Cancel out the trigger delay of scope channel 1.

7. Set the scope as follows:
   (Autoscale > Timebase > Sec/Div > 500 ps > Trigger > Trigger Src to Chan 1 > Slope to Pos > Delta t > T Markers to ON > Start Marker > Knob)

8. Position the Start Marker at the 50% point of the positive going Data transition.
   Note: The position of the Start Marker is used as reference and should therefore not be moved during the measurements.

9. Set the scope as follows:
   (Timebase > Delay >10 ns > Delta t > Stop Marker > 10 ns > Knob)

10. Position the Stop Marker at the 50% point of the negative going transition of the Data pulse and read Delta t.
    delta t min. = 8.5 ns
    delta t max. = 11.5 ns

11. Check in turn all RZ Data channels for the width settings given in Table 6-8.

    Table 6-8. Timing Channel Width Test Values - Clock Period at 1 µs

    | Set Width | Min. Width | Max. Width |
    |-----------|-----------|-----------|
    | 10.0 ns   | 8.5 ns    | 11.5 ns   |
    | 30.0 ns   | 27.5 ns   | 32.5 ns   |
    | 99.0 ns   | 93.0 ns   | 105.0 ns  |
    | 100.0 ns  | 94.0 ns   | 106.0 ns  |
    | 300.0 ns  | 284.0 ns  | 316.0 ns  |

12. Change 8180A/B clock period to 200 ms.
    (PAGES, 6, TIMING, PERIOD, 200, MILLISEC, EXIT)

13. Disconnect the Data probe from the scope (between 10100C and 1250-0080) and connect the open end of the 10100C to the counter Start input.

14. Set the counter as follows:
    Function:      Time Interval
    Sample size:   1
    Start/Stop input levels: Preset
    Start slope:   0
    Stop slope:    1
    Input impedances: 1 MΩ
    AC/DC switches: AC
    Start COM/SEP switch: Start COM
    Input Divider: divide by 10
Option 002 Timing Channel Width Test

15. Check in turn all RZ Data channels for the delay settings given in Table 6-9.

Table 6-9. Timing Channel Width Test Values - Clock Period at 200 ms

<table>
<thead>
<tr>
<th>Set Width</th>
<th>Min. Width</th>
<th>Max. Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>999.0 ns</td>
<td>948.0 ns</td>
<td>1050.0 ns</td>
</tr>
<tr>
<td>100.0 ms</td>
<td>95.0 ms</td>
<td>105.0 ms</td>
</tr>
</tbody>
</table>
6-11 Data High / Low Level Accuracy Test

Specification

Level accuracy: ±0.5% of level ±60mV (add ±60mV for amplitudes smaller than 1.5V); only valid with standard cable length of 1.5m.

Description

High and low level accuracy is measured with a digital voltmeter. All data channels are set to the NRZ format. To measure the high level all data is set to high. Low level is measured with data cleared (low).

![Figure 6-7. Test Setup for the Level Accuracy Test](image)

**Equipment**

- Digital Voltmeter: HP 3456A
- BNC (f) to dual banana Plug: 1251-2277
- Plug-on BNC Adapter: HP 15409A
- Data Cable Set: HP 15423A

**High Level Accuracy Test**

1. Program 8180A/B Standard Set.
   (PAGES, STORE/RECALL, SELECT SET, EXECUTE)

2. Set Data.
   (PAGES, STORE/RUN, EXECUTE, CLEAR/SPC, EXECUTE, EXECUTE)

3. Load Impedance to Open.
   (PAGES, CLEAR/ON, EXECUTE, CLEAR/ON, EXECUTE)

4. Outputs ON.
   (PAGES, CLEAR/ON, CLEAR/ON, EXECUTE)

5. Label A Low Level to -2V, High Level to -1V.
   (PAGES, CLEAR/TRIP, CLEAR/LEVEL, CLEAR/LEVEL [to low], 2, CLEAR/LEVEL, CLEAR/LEVEL [to high], 1, CLEAR/LEVEL)

6. Connect the equipment as shown in Figure 6-7 and press RUN.

7. Measure the output voltage at the high level settings given in Table 6-10.
Data High / Low Level Accuracy Test

Table 6-10. Data High Level Accuracy Test Values

<table>
<thead>
<tr>
<th>Set Level</th>
<th>Min. Level</th>
<th>Max. Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00 V</td>
<td>-0.875 V</td>
<td>-1.125 V</td>
</tr>
<tr>
<td>0.00 V</td>
<td>-0.060 V</td>
<td>+0.060 V</td>
</tr>
<tr>
<td>+1.00 V</td>
<td>+0.935 V</td>
<td>+1.065 V</td>
</tr>
<tr>
<td>+5.00 V</td>
<td>+4.915 V</td>
<td>+5.085 V</td>
</tr>
<tr>
<td>+17.00 V</td>
<td>+16.860 V</td>
<td>+17.150 V</td>
</tr>
</tbody>
</table>

8. Repeat step 7 for all Data channels.

Low Level Accuracy Test


10. Set Label A High Level to +17 V, Low Level to -2 V.

11. Measure the output voltage at the low level settings given in Table 6-11.

Table 6-11. Data Low Level Accuracy Test Values

<table>
<thead>
<tr>
<th>Set Level</th>
<th>Min. Level</th>
<th>Max. Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2.00 V</td>
<td>-1.930 V</td>
<td>-2.070 V</td>
</tr>
<tr>
<td>-1.00 V</td>
<td>-0.935 V</td>
<td>+1.065 V</td>
</tr>
<tr>
<td>0.00 V</td>
<td>+0.060 V</td>
<td>+0.060 V</td>
</tr>
<tr>
<td>+1.00 V</td>
<td>+0.935 V</td>
<td>+1.065 V</td>
</tr>
<tr>
<td>+16.00 V</td>
<td>+15.800 V</td>
<td>+16.200 V</td>
</tr>
</tbody>
</table>

12. Repeat step 11 for all data channels.
20 MHz Memory Test

6-12 20 MHz Memory Test

Description

The 8180A/B memory can be tested with a Signature Multimeter up to 20 MHz. Start/Stop conditions for the Signature Multimeter are established with a high bit in the strobe channel. A pseudo-random binary sequence which can be generated on all channels is used as the test pattern.

![Diagram of test setup](image)

Figure 6-8. Test Setup for the 20 MHz Memory Test

Equipment

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signature Multimeter</td>
<td>HP 5005A</td>
</tr>
<tr>
<td>Data Cable Set</td>
<td>HP 15423A</td>
</tr>
<tr>
<td>Clock Strobe Cable Set</td>
<td>HP 15422A</td>
</tr>
<tr>
<td>Solder-in Receptacle</td>
<td>HP 15412A</td>
</tr>
</tbody>
</table>

1. Program 8180A/B Standard Set.
   (PAGES, STORE/RECALLS, RESTORE SETS, EXECUTE)

2. Clock 1 Format to RZ 50%; Clock 1 Delay to 25 ns; Clock 2 Delay to 0 ns.
   (PAGES, TIMING, CLOCK 1, CLOCK 2, CLOCK 1 DLY, 50%, CLOCK 1 DLY, 25, CLOCK 2 DLY, 0)

3. Clock Period to 50 ns.
   (PAGES, TIMING, CLOCK PERIOD, 50, MICROSECONDS)

4. Load Impedance Open; Label A TTL.
   (PAGES, OUTPUT, LOAD, OUTPUT, LOAD, TTL, LOAD, TTL, TTL, EXCEPT)

5. Strobe Level TTL; Outputs ON.
   (PAGES, OUTPUT, LOAD, OUTPUT, LOAD, TTL, OUTPUT, ON/OFF, ON)

   (PAGES, OUTPUT, LOAD, OUTPUT, LOAD, TTL, OUTPUT, ON/OFF, CLEAR)

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7. PRBS on Channel 0-0.
   (PAGES, Top Address, Enter Number, Exit Address, Enter Number, Exit Address)
   [until PRBS channel 00 is displayed].

8. Copy Channel.
   Press Copy Channel and using the softkey in the right hand half of the display
   move the inverse video cursor until Copy Channel 0-0 to 0-0 is displayed.

9. Copy Channel 0-0 to all other channels.
   Press alternately (on the right hand half of the display) and until all Data channels contain the pattern in channel 0-0.

10. Set the Strobe Bit to High at address 00000.
   (PAGES, Top Address, 0, Enter Number, Exit Address, 1)

11. Connect the equipment as shown in Figure 6-8 and press RUN.

12. Check all data channels for the following signature:
    On the 8180A - 46F9
    On the 8180B - H150
Ext. Clock; RUN; BREAK; and Stop Hysteresis/Threshold Test

6-13 Ext. Clock; RUN; BREAK and STOP Hysteresis/Threshold Test

Specification

Threshold Accuracy: ±3% of programmed value ±50 mV

Description

A low frequency triangular wave signal is used to stimulate the 8180A/B external inputs. When the current threshold level of the 8180A/B inputs is reached, the 8180A/B starts or stops generating a signal at its Clock 1 output. Both signals, the triangular wave signal and the Clock 1 output signal are displayed on the scope. The level of the triangular wave signal where Clock 1 generation commences or stops is the actual input threshold.

Figure 6-9. Test Setup for the External Input Test

Equipment

- Pulse/Function Generator: HP 8007B/HP8116A
- Scope: HP 54100D
- Active Pods: HP 54001A
- 50 Ohm Pod: HP 54002A
- 50 Ohm Feedthrough: HP 10100C
- BNC Tee Adapter: 1250-0781
- BNC female/female: 1250-0080
- Scope Probe Adapter: 1250-1454
- BNC Adapter: HP 15409A
- Clock/Strobe cable set: HP 15422A
- BNC Cable

Procedure

1. Program 8180A/B Standard Set.
   (PAGES, STORE/RECALL, ARPAST SET, ., EXECUTE )

2. Clock 1 Width 20 ns; Clock 2 Delay 0 ns.
   (PAGES, STORE/RECALL, ARPAST SET, CLOCKS, 0, 20, ., EXECUTE )

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3. Label A TTL; Outputs ON.  
(PAGES, CONTROL, INPUTS, CLOCK SOURCE, INTERNAL).

4. Input Impedance 100 KΩ  
(PAGES, CONTROL, INPUTS, IMPEDANCE, 100KΩ).

5. Clock Source External Positive Edge  
(PAGES, CONTROL, CLOCK SOURCE, EXTERNAL).

6. Set the Pulse Generator as follows:  
   Period approx. 1 ms  
   Width 0.5 ms  
   Transition 5 µs to 250 µs  
   Amplitude 250 mVpp (into open)  
   Offset ON

7. Adjust leading edge and trailing edge for a triangle waveform on the scope.

**External Clock Test**

8. Connect the equipment as shown in Figure 6-9 and press RUN. (BNC Cable A connected to External Clock Input.)

9. Adjust the triangular waveform such that it is symmetrical about 0V using the pulse generator's offset vernier.

10. Set the scope as follows:  
    (Autoscale > Ch 2 > Volts/Div > 1 Volt > Trigger > Trig Src to Ch 2 > Trigger Level > 1 Volt > Ch 1 > Chan 1 Mode to Magnify > Magnify to ON > Volts/Div > 20mV/Div > Offset > 0V > Timebase > Sec/Div > 50 µs)

11. The displayed transition should cross the vertical graticule line between ± 50 mV.

12. Change External Clock Slope (active edge) to negative. (EXTERNAL)

13. The displayed transition should cross the vertical graticule line between ± 50 mV.

**External RUN and BREAK Test**

14. Connect cable A to the Break Input (cable B to the Run Input).

15. Set the 8180A/B to Clock Source INTERNAL; RUN Input to ON, active edge positive; BREAK Input to ON, active edge negative.  
    (PAGES, CONTROL, INPUTS, CLOCK SOURCE, INTERNAL).

16. Set the scope as follows:  
    (Autoscale > Timebase > Sec/Div > 200 microsec/Div > Trigger > Trigger Source to Channel 3 > Trigger Level > 1 Volt > Delta t > T Markers to ON > Start Marker > Knob > Stop Marker > Knob)  
    Set the Start Marker to the positive going edge of displayed pulse on channel 2. Set the Stop Marker to the negative going edge of displayed pulse on channel 2.
17. Set the scope as follows:
   (Timebase > Delay > Knob)
   Adjust Start Marker to the vertical center graticule line.

18. Set the scope as follows:
   Timebase to 50 µs; Chan 2 to OFF; Split Screen to OFF
   (Sec/Div > 50 µs > Chan 2 > Chan 2 Display to OFF > Display > Split Screen to OFF > Channel 1 >
   Channel 1 Mode to Magnify > Magnify ON > Volts/Div > 20 mV/Div.

19. The displayed transition should cross the vertical graticule line within the limits of ±50mV.

20. Repeat the measurement at the position where the Stop Marker is located. The displayed transition
    should cross the vertical graticule line within the limits of ±50mV.

21. Set the Run Input to ON, active edge negative; Break Input to ON, active edge positive.
    (Magnify OFF, Magnify ON, Volts/Div 20 mV/Div)

22. Repeat step 15 through 20 with reversed slopes for Run and Break Inputs. Threshold Limit is
    ±50mV.

**External STOP Test**

23. Connect cable A to the Stop Input (cable B to the Run Input).

24. Check threshold levels of the Stop Input for both slopes as described above for the Break Input.

25. Check Clock, Run, Break and Stop inputs at +2 Volt and -2 Volt threshold settings.
   (PAGES 2 [-2]).

   For this test set the pulse generator to triangular waveform with an amplitude of 8V pp symmetrical about 0V.

   **Limits:**
   - Voltage Threshold minimum = 1.85 V
   - Voltage Threshold maximum = 2.15 V

   Check inputs only at one slope setting.
6-14 Transition Time / Overshoot Test

Specification

Transition Time: less than 3.0 ns + |amplitude| x 0.2 ns.
Preshoot, Overshoot, Ringing: less than ±10% of amplitude.
Specifications are valid for a cable length of 1.5 m.

Figure 6-10. Test Setup for the Transition Time / Overshoot Test

Equipment

Scope
Active Pod
Data Cable
BNC Adapter
50 Ohm Feedthrough
BNC female/female
BNC scope probe adapter

HP 54001A
HP 15423A
HP 15409A
HP 10100C
1250-0080
1250-1454

Procedure

1. Program 8180A/B Standard Set.

2. Set all bits at address 00000 High; Set all bits at address 00001 Low.

3. Last Address 00001.

4. Outputs ON.

5. Set Label A High Level to -1 V; Low Level -2 V.

6. Connect the equipment as shown in Figure 6-10 and press RUN.

7. Set the scope as follows:
(Autoscale > Delta V > Vmarkers to ON > Marker 1 Position > Knob [set Marker 1 to 0% of pulse]
Transition Time / Overshoot Test

> Marker 2 Position > Knob [set Marker 2 to 100% of pulse] > 10-90% > Timebase > Sec/Div > 500 ps > Delta t > T Markers to ON > Start Marker > Knob [set the Start Marker to the crossing point at the 10% Level and displayed transition] > Stop Marker > Knob [Set the Stop Marker to the crossing point at the 90% Level and displayed transition].

8. Measure the transition time (Delta t) from 10% to 90% of amplitude for all data channels.
   Specification: Transition Time = less than 3 ns.

9. Change Label A High Level to +2 V; Low Level to 0 V.
   (PAGES , [OUTPUT], [Level], [Low ↔ High] [to High], 2, [VOLT], [Low ↔ High] [to Low], 0, [VOLT])

10. Measure preshoot, overshoot and ringing at all data channels.
    Specification: less than ±10% of amplitude.
Chapter 7
HP 8182A/B Performance Verification

7-1 Introduction

The test procedures described in this chapter are designed to verify the published performance specifications of the HP 8182A/B Data Analyzer given in Chapter 1 of this manual.

NOTE

The tested instrument must be given a 30 minute warm-up time before starting any of the performance tests. During any performance test, all shields, covers and connecting hardware must be in place.

Equipment Required

The equipment necessary to perform each performance test is listed at the beginning of each test. Alternative test equipment may be substituted for the recommended models, provided that it satisfies the critical specifications given.

Test Record

When carrying out the performance tests, you should keep a tabulated test record, listing the test results and the acceptable performance limits. The results recorded at incoming inspection will provide a reference for periodic calibration, troubleshooting and after-repair testing.

7-2 Trigger Word and Operating Modes Tests

Description

The Data Generator HP-Model 8018A is used to generate the Trigger Word (bit) for two 8182A/B data channels. The error display indicates the Trigger Word position. Because of the cleared memory, the Trigger Word appears as an error. When selecting Trigger Event Start Compare Mode, the Trigger Delay is set to 00001. This causes the Trigger Word to be displayed in address 1023/16383.

Figure 7-1. Test Setup for the Trigger Word and Operating Mode Test
Equipment Required

Data generator
Plug-on BNC Adapter (3 off)
Clock Probe Assembly
Data Probe Assembly

HP 8018A
HP 15409A
HP 15406A
HP 15407A

Procedure

Set the 8018A as follows:

<table>
<thead>
<tr>
<th>Bit Rate</th>
<th>Clock Mode</th>
<th>Cycle Mode</th>
<th>Row Address</th>
<th>Data Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 MHz</td>
<td>Int.Clock</td>
<td>Auto</td>
<td>1-16</td>
<td>Zs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Clear both 8018A Data Channels by selecting the channel and pressing the toggle switch to Channel Clear.

2. Select Word Address 01 and load bit 1 to high in channel A and channel B.


5. Clock Delay 5 ns.

6. Autoarming Delay 1s.

7. Error Map; Trigger Word in Softkey Area.

8. Connect the equipment as shown in Figure 7-1 and press RUN.

Trigger Start Analysis Test

With Trigger Word set to X (don’t care) a single sporadic error should be displayed on the Error Map.

9. Set the Trigger Word for both connected data channels to 1.
   The Error Map should display only the Trigger Word in address 00000 as an error.

10. Set Trigger Word for one data channel to 0.
    The 8182A/B should switch to ARMED (no trigger recognition).

11. Set the Trigger Word back to 1 and the 8182A/B should trigger again.

12. Set the Trigger Word for the second channel to 0 and 1 and check Trigger Word recognition as described in steps 8 to 10.
Trigger Stop Analysis Test

13. Program 8182A/B to Trigger Stop Analysis.
   (PAGES, CONTROL, Operatg Mode, Trg Stop Anal)

   (PAGES, Error Map, SOFTKEYS, CONTROL, Trigger Word)

With Trigger Word 1 for both connected data channels, the error display should stop always at address -00000 (the Trigger Word at address -00000 is indicated as error).

15. Set the Trigger Word for one connected channel to 0.
    The 8182A/B should stay in ACTIVE (no trigger).

16. Set the Trigger Word back to 1.
    The 8182A/B should trigger again.

17. Set the Trigger Word for the second connected data channel to 0 and 1 and check Trigger Word recognition as described in steps 14 to 16.

Trigger Event Start Compare Test

18. Program 8182A/B to Trigger Event Start Compare.
    (PAGES, CONTROL, Operatg Mode, Trg Strt Comp, EXECUTE)

19. Select Error Map.
    (PAGES, Error Map)

The error display should show the Trigger Word indicated as error at address 1023 (caused by Trigger Delay 00001) and errors in the channel marking display for both connected data channels.

20. Program Trigger Start Analysis and Trigger Delay 0.
    (PAGES, CONTROL, Operatg Mode, Trg Strt Anal, EXIT, Trg Delay, 0, ENTER NUMBER)

21. Repeat the procedure starting with step 5 for the remaining data channel pairs.
Trigger Delay and Stop Delay Tests

Description

This test is to be performed with any one of the available channels to check the Trigger Delay and Stop Delay Functions. A data generator is used to generate the Trigger Word. The Trigger Word for unused data channels must be set to don't care (X).

Equipment

- Data Generator: HP 8018A
- Plug-on BNC Adapter (2 off): HP 15409A
- Clock Probe Assembly: HP 15406A
- Data Probe Assembly: HP 15407A

Procedure

Set the 8018A as follows:

<table>
<thead>
<tr>
<th>Bit Rate</th>
<th>50 MHz</th>
<th>Data Stream Length</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Mode</td>
<td>Int. Clock</td>
<td>Amplitude (A)</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Cycle Mode</td>
<td>Auto</td>
<td>Serializer</td>
<td>2x 1024</td>
</tr>
<tr>
<td>Row Address</td>
<td>1-16</td>
<td>Format</td>
<td>NRZ</td>
</tr>
<tr>
<td>Data Mode</td>
<td>Zs</td>
<td>Zs</td>
<td>50 Ohm</td>
</tr>
</tbody>
</table>

1. Clear 8018A channel A data by selecting channel A and pressing the toggle switch to Channel Clear position.

2. Select Word Address 01 and load bit 1 to high.

   (PAGES, MISCELLANEOUS, RECALL, STANDARD SET, EXECUTE)

   (PAGES, EXPOSED DATA, CLEAR DATA, CLEAR A SET, CLOCK CONTROL, EXECUTE, CLEAR DATA, CLEAR CONTROL)

5. Set Clock Delay to 5ns.
   (PAGES, CLOCK CONTROL, CLOCK, CLOCK DELAY, 5, CLEAR CONTROL)
Trigger Delay and Stop Delay Tests

6. Set Autoarming Delay to 1s, Set Stop Delay to 1023
   (PAGES, \textit{Autoarming}, \textit{Delay 1 s})
   (PAGES, \textit{Stop Delay}, 1023)

7. Connect the equipment as shown in Figure 7-2 and press \textbf{RUN}.

8. Set the Trigger Word to 1 for the connected data probe (all other channels to X, don't care)
   (PAGES, \textit{CONTROL}, \textit{Trigger Word}, 1)

9. Error Map; Trigger Delay in Softkey Area.
   (PAGES, \textit{Error Map}, \textit{Trigger Delay})

**Trigger Delay Test**

10. Increase Trigger Delay by pressing \textit{INCREMENT}, and check that the displayed error moves backwards from address 1023 (for Trg Delay 1) with increasing delay setting.

11. Set Trigger Delay back to 00000.

**Stop Delay Test**

12. Select Stop Delay in the Softkey Area and set Stop Delay to 1023/16383.
    (SOFTKEYS, \textit{Stop Delay}, 16383)

13. Check that the Stored Words displayed in the upper right hand corner of the 8182A/B display indicates 1024/16384. Vary the Stop Delay and check that the Stop Delay setting + 1 is displayed as Stored Words in the upper right hand corner of the 8182A/B display.
Sampling Point Accuracy and Skew Tests

7-4 Sampling Point Accuracy and Skew Tests

Specification

Sampling point accuracy: \( \pm 5\% \) of set Clock Delay \( \pm 1\) ns.
Channel skew: \( \leq 2\) ns.

Description

The test setup uses a pulse generator as clock and data source for the 8182A/B Data Analyzer. The data is delayed by a fixed 3 ns delay line. Setting the 8182A/B Clock Delay to 3 ns then corresponds to zero delay between clock and data. The clock can now be advanced by 3 ns and delayed with respect to the data to check when the incoming data signal is recognized as a high or a low level.

![Diagram of test setup](image)

Figure 7-3. Test Setup for the Sampling Point Accuracy and Skew Test

Equipment

- Pulse Generator: HP 8007B
- BNC Tee: 1250-0781
- Plug-on BNC Adapter (2 off): HP 15409A
- Clock Probe Assembly: HP 15406A
- Data Probe Assembly: HP 15407A
- Delay Line (including 50 \( \Omega \)) 3 ns: 08182-61621

Procedure

1. Set Pulse Generator as follows:
   - Period: 1 \( \mu \)s
   - Pulse Width: 0.5 \( \mu \)s
   - Leading Edge: \( < 3\) ns
   - Trailing Edge: \( < 3\) ns
   - Amplitude High Level: +2V into 50 \( \Omega \)
   - Low Level: 0V

   (PAGES, [Miscellaneous], [Recall], [Standard set], [Picture])

3. Set Clock Threshold to +1V.
   (PAGES, [Clock set], [Clock times], [1, [1, 5], Volts])

4. Set Threshold Label A to +1 V.
   (PAGES, [Input], [Threshold], [1, +1 Volt])

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Sampling Point Accuracy and Skew Tests

5. Set Stop Delay to 40.
   (PAGES, SETCONTROL, Stop, Stop Delay, 40, ENTER NUMBER)

6. Set Autoarming Delay to 0 s.
   (PAGES, SETCONTROL, Autoarming, Display Off)

7. Select the Timing Diagrams Page.
   (PAGES, TIMING DIAG)

8. Press SOFTKEYS, SETCONTROL, Clock, Clock Delay, 3, NANOS)  

9. Connect the equipment as shown in Figure 7-3 and press RUN. (Start with Connector 0 Channel 0.)

10. Using INC, check that the displayed timing signal switches from low to high within 2 to 4 ns of the Clock Delay setting.

11. Set the Clock Slope to Negative.
    (PAGES, SETCONTROL, Clock, Clock Slope, NEG SLOPE, EXIT, Clock Delay)

12. Increment the Clock Delay starting from 2 ns and check that the timing signal switches from high to low within 2 to 4 ns of the Clock Delay setting.

13. Repeat the Skew Test for Positive Clock Slope and Negative Clock Slope for the remaining channels as described in steps 10 to 12.
    When checking skew from connector 3 channel 0 upwards, move the vertical display window.
    (PAGES, TIMING DIAG, Select Display, Vertical Window, [until the required channels are displayed])
7-5 Clock Delay Test

Specification

±5% of set Clock Delay ±1ns.

Description

The test setup uses a pulse generator as an external clock source. The Clock Delay is measured at the 8182A/B clock output referenced to 0.00ns programmed Clock Delay.

![Figure 7-4. Test Setup for the Clock Delay Test]

Equipment

- Pulse Generator: HP 8007B
- Scope: HP 54100D
- Active scope Pods: HP 54001A
- BNC Tee Adapter: 1250-0781
- 50 Ohm Feedthrough: HP 10100C
- BNC scope Probe Adapter: 1250-1454
- BNC Adapter: HP 15409A
- Clock Probe: HP 15406A

Procedure

1. Cancel out channel to channel skew and the Trigger Delay of channel 2.
   Set the Pulse Generator as follows:
   - Period: 110 µs
   - Pulse Width: 1.5 µs
   - Transition Time: 2 ns
   - Amplitude LOL: 0 V
   - (into 50 Ohm) HIL: 2.5 V
   - Offset: OFF

   (PAGES, MISCELLANEOUS, RECALL, STANDARD SET, EXECUTE)

3. Set Clock Threshold to +1.2V; Set Clock Delay to 0.00ns.
   (PAGES, CONTROL, CLOCK, CLOCK TYPE, CLOCK, 1.2, VOLTS, EXECUTE, Clock Delay, 0, NAND GEC)

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Clock Delay Test

4. Connect the equipment as shown in Figure 7-4.

5. Set the scope as follows:
   (Autoscale > Trigger > Trigger Src to Chan 1 > Chan 1 > Chan 1 Display to OFF > Display > Split Screen to OFF)

6. Center the 50% point of the positive going transition of the displayed clock pulse on the center graticule.
   (Timebase > Sec/Div > Ins > Delay > Knob)

7. Set the Start Marker to the 50% point of the displayed transition.
   (Delta > Tmarkers to ON > Start Marker > Knob)

8. Using the INC button, step through the delay range of 0.00 ns to 10.00 ns in 100 ps steps and check the accuracy.

   The position of the Start Marker is the reference for the following measurements and must therefore not be moved.

9. Program 8182A/B Clock Delay as listed in Table 7-1 and check that accuracy is in the range ±5% ±1 ns.

   Example: Zero delay between scope input Channel 1 and Channel 2 = 38 ns
   Programmed Clock Delay = 21.9 ns

   Set scope Timebase delay to 60 ns and position the Stop Marker to the 50% point of the displayed transition. Perform a delta t reading; the reading should be in the following range:
   Delta t min = 19.8 ns
   Delta t max = 24.0 ns

   Table 7-1. Clock Delay Test Values

<table>
<thead>
<tr>
<th>Set Delay</th>
<th>Delta t min.</th>
<th>Delta t max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>21.9 ns</td>
<td>19.8 ns</td>
<td>24.0 ns</td>
</tr>
<tr>
<td>22.0 ns</td>
<td>19.9 ns</td>
<td>24.1 ns</td>
</tr>
<tr>
<td>70.0 ns</td>
<td>65.5 ns</td>
<td>74.5 ns</td>
</tr>
<tr>
<td>117.0 ns</td>
<td>110.2 ns</td>
<td>123.9 ns</td>
</tr>
<tr>
<td>118.0 ns</td>
<td>111.1 ns</td>
<td>124.9 ns</td>
</tr>
<tr>
<td>500.0 ns</td>
<td>474.0 ns</td>
<td>526.0 ns</td>
</tr>
<tr>
<td>1.01 us</td>
<td>0.96 us</td>
<td>1.06 us</td>
</tr>
<tr>
<td>1.02 us</td>
<td>0.97 us</td>
<td>1.07 us</td>
</tr>
<tr>
<td>5.00 us</td>
<td>4.75 us</td>
<td>5.25 us</td>
</tr>
<tr>
<td>9.99 us</td>
<td>9.49 us</td>
<td>10.49 us</td>
</tr>
<tr>
<td>10.0 us</td>
<td>9.50 us</td>
<td>10.5 us</td>
</tr>
<tr>
<td>50.0 us</td>
<td>47.5 us</td>
<td>52.5 us</td>
</tr>
<tr>
<td>99.9 us</td>
<td>94.9 us</td>
<td>104.9 us</td>
</tr>
</tbody>
</table>
7-6 Compare Window Width Test

Specification

Compare window width accuracy ±5% of set value ±1 ns.

Description

The test setup uses a pulse generator as an external clock source. Analyzer Clock Delay is measured at the 8182A/B Clock Output referenced to 0.00 ns programmed Clock Delay. Ranges up to 10 ns are measured with an oscilloscope. A time interval counter is used for higher ranges. A time offset is programmed on the counter in order to compensate for internal and cable delays, instead of adding these delays manually.

![Diagram of test setup](image)

Figure 7-5. Test Setup for the Compare Window Width Test

Equipment

Scope: HP 54100D
Active Scope Pod: HP 54001A
Pulse Generator: HP 8007B
Counter: HP 5370 B
Clock Probe Assy: HP 15406 A
BNC Adapter: HP 15409 A
50 Ohm Feedthrough: HP 10100 C
Scope Probe Adapter: 1250-1454

Procedure

Before performing this measurement cancel out the Trigger Delay of scope channel 1.

1. Set the Pulse Generator as follows:
   - Period: 1 µs
   - Pulse Width: 0.5 µs
   - Transition Time: 2 ns
   - HIL: 2.5 V
   - LOL: 0.0 V

   (PAGES, MISELLENEOUS, STANDARD, SET, EXECUTED)

3. Select Trigger Event Start Compare.
   (PAGES, MISELLENEOUS, OPERATOR, MODE, TEST, SETUP, COMPARE, EXECUTED)

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Compare Window Width Test

4. Set the Clock Width to 10ns.
   (PAGES, Clock Width 10, NANOSEC)

5. Connect the equipment as shown in Figure 7-5.

6. Set the scope as follows:
   (Autoscale > Timebase > Sec/Div > 500ps > Trigger > Trigger Src to Chan 1 > slope to pos)

7. Adjust the 50% point of the positive going transition to lie on the center horizontal graticule line.
   (Chan 1 > Offset > Knob)

8. Move the Start Marker to the 50% point of the displayed transition.
   (Delta t > Tmarkers to ON > Start Marker > Knob)
   Note: The Start Marker is the reference for the following measurements and must therefore not be moved.

9. Set the scope timebase delay to 10ns.
   (Timebase > Delay > 10ns)

10. Set the Stop Marker to the 50% point of the negative going transition and read delta t (Delta t > Stop Marker > Knob)

    Delta t must be in the following range:
    Delta t min: 8.5 ns
    Delta t max: 11.5 ns

11. Check linearity by incrementing the clock width in 100 ps steps up to 20 ns.

12. Check the Clock Width at the settings given in Table 7-2.

    Table 7-2. Clock Width Test Values - Clock Period at 1 µs

    | Set Width | Min. Width | Max. Width |
    |-----------|------------|------------|
    | 29.9 ns   | 27.4 ns    | 32.4 ns    |
    | 30.0 ns   | 27.5 ns    | 32.5 ns    |
    | 99.0 ns   | 93.0 ns    | 105.0 ns   |
    | 100.0 ns  | 94.0 ns    | 106.0 ns   |

13. Connect 8182A/B Clock Output to counter channel A instead of scope.

    Counter settings:
    Function: Time Interval
    Sample Size: 1
    Start/Stop slopes: \( \overline{5/\overline{n}} \)
    Start/Stop inp. imp: 50\( \Omega \)
    AC/DC switch to: AC
    Start COM/SEP switch: COM

    Change pulse generator period to 120 ms and repeat step 12 using the values in Table 7-3.
Compare Window Width Test

Table 7-3. Clock Width Test Values - Clock Period at 120 ms

<table>
<thead>
<tr>
<th>Set Width</th>
<th>Min. Width</th>
<th>Max. Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>300.0 ns</td>
<td>284.0 ns</td>
<td>316.0 ns</td>
</tr>
<tr>
<td>999.0 ns</td>
<td>948.0 ns</td>
<td>1050.0 ns</td>
</tr>
<tr>
<td>100.0 ms</td>
<td>95.0 ms</td>
<td>105.0 ms</td>
</tr>
</tbody>
</table>
7-7 Clock Threshold and Hysteresis Tests

Specification

Threshold accuracy: ±2% of set value ±10mV.
Hysteresis: < ±50mV.

Description

The pulse generator is adjusted to generate a triangular waveform with a period of 1 ms. This signal is fed into the CLOCK input of the 8182A/B. When the 8182A/B clock threshold is reached the 8182A/B generates a clock pulse, which is available at its Clock Output. This clock pulse triggers a trace on the oscilloscope. The vertical offset from zero volts corresponds exactly to the level where the 8182A/B recognises a clock signal.

![Test Setup for the Clock Threshold Hysteresis Test](image)

Figure 7-6. Test Setup for the Clock Threshold Hysteresis Test

Equipment

Scope
Active scope Pods
Pulse Generator
BNC Tee Adapter
Scope Probe Adapter
50 Ohm Feedthrough
Clock Probe
BNC Adapter

HP 54100D
HP 54001A
HP 8007B
1250-0781
1250-1454
HP 10100C
HP 15406A
HP 15409A

Procedure

1. Set the pulse generator as follows:

   Period: 1 ms
   Width: 0.5 ms
   Transition Time: 5µs to 250 µs
   Amplitude: 4V pp into 500
   Offset: ON

2. Adjust the leading and trailing edges for a triangle waveform on the scope.

3. Using the pulse generator offset vernier, set the waveform symmetrical to 0V graticule line.
Hysteresis Test

4. Program 8182A/B to Standard Set.
   (PAGES, MISCELLANEOUS, SET-RECALL, SET-DEFAULT, RECALL)  

5. Clock Slope Positive; Threshold 0.00V.
   (PAGES, SET-CONTROL, SET-CLOCK, SET-CLOCK-SLOPE, SET-POS-SLOPE, 
   SET-DEFAULT, SET-THRESHOLD, 0, SET-VOLTAGE)  

6. Connect the equipment as shown in Figure 7-6.  

7. Set the scope as follows:  
   (Autoscale > Trigger > Trig Src to Chan 2 > Display > Split Screen to OFF > Chan 2 > Chan 2 
   Display to OFF > Timebase > Sec/Div > 500ns > Chan 1 > Volts/DIV > 100mV > Chan 1 Mode to 
   Magnify > Magnify to ON > Volts/DIV > 20mV > Delta V > V Markers to ON > Marker 1 Position 
   > Knob)  

8. Position the Marker to the point where the transition crosses the vertical graticule line and read 
   \( V(1) \).
   \( V(1) \leq +50mV \).  

9. Change to negative Clock Slope.  
   (NEG-SLOPE)  
   Move V Marker 1 to the crossing point and read \( V(1) \).  
   \( V(1) \leq -50mV \)  

Threshold Test

10. Set the threshold to -1.4V.  
   (NEG-THRESHOLD, CLOCK, 1.4, SET-VOLTAGE)  

11. Set the scope as follows:  
   (Chan 1 > Chan 1 Mode to NORMAL > Volts/DIV > 100mV > Offset > -1.2 V > Chan 1 Mode to 
   Magnify > Magnify to ON > Volts/DIV > 20mV/DIV > Offset > -1.400V > Delta V > V markers to ON > 
   Marker 1 Position > Knob)  

12. Move Marker 1 to the crossing point where the displayed transition meets the vertical graticule line 
   and read \( V(1) \).  
   \( V(1)_{\text{min}}: -1.49V \)  
   \( V(1)_{\text{max}}: -1.31V \)  

13. Set Clock Slope to positive; Set Clock Threshold to +1.4V.
   (POS-SLOPE, CLOCK, 1.4, SET-VOLTAGE)  

14. Set the scope as follows:  
   (Chan 1 > Chan 1 Mode to NORMAL > Volts/DIV > 100mV > Offset > 1.200 V > Chan 1 Mode to 
   Magnify > Magnify to ON > Volts/DIV > 20mV/DIV > Offset > 1.400V)  

15. Move V Marker 1 to the point where the transition crosses the vertical graticule line 
   (Delta V > Vmarker to ON > Marker 1 Position > Knob)  

16. Read \( V(1) \).  \( V(1) \) must be in the range of:  
   \( V(1)_{\text{min}}: 1.31V \)  
   \( V(1)_{\text{max}}: 1.49V \)
7-8 Data Threshold Level Accuracy and Linearity Tests

Specification

Single threshold accuracy: ±2% of set value ±10 mV.
Level detection accuracy 50 ms after input signal transition: actual threshold = ±15 mV.

Description

This test is used to measure the high and low level detection voltage to determine the actual threshold voltage. The check-sequence is selected to ensure that all data lines used for level programming are working properly. To get a better resolution when adjusting the power supply, two 20 dB attenuators are used to reduce the output voltage. 20 W attenuators are recommended to avoid damage to the rest of the equipment. The capacitor across the DVM input suppresses spikes generated by the DVM.

Figure 7-7. Test Setup for the Data Threshold Level Accuracy and Linearity Test

Equipment

DC Power Supply
Digital Voltmeter
Plug-on BNC Adapter
Data Probe Assy.
BNC - Tee
BNC (f) to dual banana Plug (2 off)
50 Ohm Feedthrough
Capacitor
2 x Attenuator 20 dB (20W)
Cable Assembly BNC to BNC

Procedure

1. Program 8182A/B Standard Set.
2. Clock Source Internal.
3. Select Autoarming Delay of 0s.

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4. Set Stop Delay to 40.
   (PAGES, STOP DELAY, ENTER NUM. 40, ENTER NUMBER)

5. Set Channel Configuration to Connector 0 Channel 0.
   (PAGES, CHANNEL SELECTION, CONNECTOR 0, CHANNEL 0
   [until only connector 0 channel 0 is displayed])

   (PAGES, TIMING DIAG, SOFT KEYS, INPUT A, THRESHOLD
   [NEXT LABEL] if necessary)

7. Set Single Threshold of Label A to +0.01 V.
   (+.01, ENTER VOLTAGE)

   **CAUTION**

   Set power supply voltage to minimum. Do not overload attenuators.

8. Connect the equipment as shown in Figure 7-7 and press RUN.

9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading (Voltage a).

10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading (Voltage b).

    Level Detection Accuracy (Va - Vb) must be better than 30 mV.
    Actual Threshold (Va + Vb)/2 must be within ±2% of the set value ±10 mV.

    Example: Programmed Threshold = +0.01 V
    High Level Voltage (measured in step 9) = +0.012 V
    Low Level Voltage (measured in step 10) = +0.009 V
    Level detection accuracy = (0.012 V - 0.009 V) = 0.003 V
    Limit = ±0.03 V
    Single threshold accuracy = (0.012V + 0.009 V)/2 = 0.011 V
    Limit = 0.00 V to 0.02 V

13. Program the thresholds given in Tables 7-5, 7-6 and 7-7, and check for specifications as described in step 10.

Table 7-5. Threshold Level Accuracy and Linearity Test - All Attenuators in Place

<table>
<thead>
<tr>
<th>Set Thres.</th>
<th>Hi Level Va</th>
<th>Lo Level Vb</th>
<th>Delta V</th>
<th>Threshold Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min. Actual</td>
<td>Max.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.01 V</td>
<td>........ V</td>
<td>........ V</td>
<td>........ V</td>
<td>0.000V ........ 0.020V</td>
</tr>
<tr>
<td>0.02 V</td>
<td>........ V</td>
<td>........ V</td>
<td>........ V</td>
<td>0.010V ........ 0.030V</td>
</tr>
<tr>
<td>0.04 V</td>
<td>........ V</td>
<td>........ V</td>
<td>........ V</td>
<td>0.020V ........ 0.050V</td>
</tr>
<tr>
<td>0.08 V</td>
<td>........ V</td>
<td>........ V</td>
<td>........ V</td>
<td>0.068V ........ 0.092V</td>
</tr>
<tr>
<td>0.16 V</td>
<td>........ V</td>
<td>........ V</td>
<td>........ V</td>
<td>0.147V ........ 0.173V</td>
</tr>
</tbody>
</table>

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Data Threshold Level Accuracy and Linearity Tests

Table 7-6. Threshold Level Accuracy and Linearity Test - One 20 dB Attenuator Removed

<table>
<thead>
<tr>
<th>Set Thres.</th>
<th>Hi Level Va</th>
<th>Lo Level Vb</th>
<th>Delta V</th>
<th>Threshold Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.32 V</td>
<td>........V</td>
<td>........V</td>
<td>........V</td>
<td>0.304V 0.336V</td>
</tr>
<tr>
<td>0.64 V</td>
<td>........V</td>
<td>........V</td>
<td>........V</td>
<td>0.617V 0.663V</td>
</tr>
<tr>
<td>1.28 V</td>
<td>........V</td>
<td>........V</td>
<td>........V</td>
<td>1.244V 1.316V</td>
</tr>
<tr>
<td>2.56 V</td>
<td>........V</td>
<td>........V</td>
<td>........V</td>
<td>2.499V 2.621V</td>
</tr>
</tbody>
</table>

Table 7-7. Threshold Level Accuracy and Linearity Test - Both Attenuators and 50 Ω Feedthrough Removed

<table>
<thead>
<tr>
<th>Set Thres.</th>
<th>Hi Level Va</th>
<th>Lo Level Vb</th>
<th>Delta V</th>
<th>Threshold Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.12 V</td>
<td>........V</td>
<td>........V</td>
<td>........V</td>
<td>5.008V 5.232V</td>
</tr>
</tbody>
</table>
Data Offset and Gain Tests

7-9 Data Offset and Gain Tests

Specification

Single threshold accuracy:
Level detection accuracy 50 ms
after input signal transition:

\[ \pm 2\% \text{ of set value } \pm 10 \text{ mV.} \]

actual threshold = \( \pm 15 \text{ mV.} \)

Description

To determine the actual threshold and to check the threshold accuracy, the hysteresis between high and low level detection voltages must be measured first. The actual threshold is midway between high and low level detection voltages. This value must be within the specifications for single threshold.

![Test Setup for the Data Offset and Gain Test](image)

Figure 7-8. Test Setup for the Data Offset and Gain Test

Equipment

- DC Power Supply
- Digital Voltmeter
- Plug-on BNC Adapter
- Data Probe Assy.
- BNC - Tee
- BNC (f) to dual banana Plug (2 off)
- 50 Ohm Feedthrough
- Capacitor
- 2 x Attenuator 20 dB (20W)
- Cable Assembly BNC to BNC

HP 6002A
HP 3456A
HP 15409A
HP 15407A
1250-0781
1251-2277
HP 10100C
0.22 uF
(e.g. Texscan HFP 50/20)
HP 11170C

Positive Offset Test

1. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS, RECALL, Standard Set, EXECUTE)

2. Set Clock Source to Internal.
   (PAGES, CONTROL, CLOCK, Clock Source, INTERNAL)

3. Set Autoarming Delay to 0s.
   (PAGES, CONTROL, Autoarming, DELAY UP)

4. Set Stop Delay to 40.
   (PAGES, CONTROL, Stop, Stop Delay, 40, ENTER NUMBERS)
Data Offset and Gain Tests

5. Set Channel Configuration to Connector 0 Channel 0. (PAGES, [Input], [Chnl Config], DELTE CHNLS [until only connector 0 channel 0 is displayed])

CAUTION
Set power supply voltage to minimum. Do not overload attenuators.

6. Set Single Threshold Label A to +0.05 V. (PAGES, [Input], Threshold, Next Label [if necessary] .05, volt)

7. Select Timing Diagrams Report; Channel Configuration in Softkey Area. (PAGES, TIMING DIAG., SOFTKEYS, [Input], Chnl Config)

8. Connect the equipment as shown in Figure 7-8 and press RUN.

9. Increase power supply voltage slowly until the timing display just switches to high and note DVM reading (Voltage a).

10. Decrease power supply voltage slowly until the timing display just switches back to low and note DVM reading (Voltage b).

Level Detection Accuracy (Va - Vb) must be less than 30 mV.
Actual Threshold (Va + Vb)/2 must be within ±2% of set value ±10 mV.

Example: Programmed Threshold = 0.05 V
High Level Voltage (measured in step 9) = 0.056 V
Low Level Voltage (measured in step 10) = 0.043 V
Level detection accuracy = 0.056 V - 0.043 V = 0.013 V
Limit: < 0.03 V
Single thresh. accuracy = (0.056V + 0.043 V)/2 = 0.050 V
Limit: 0.039V to 0.061V

11. Select the connector and channel to be tested by pressing first the connector number and then the channel number on the data entry key pad. Connect in turn all data probes to the test setup and check for +50 mV ± 10 mV threshold accuracy.

Negative Offset Test

14. Change power supply polarity to negative and program the 8182A/B as follows:

15. Set Label A Single Threshold to -0.05 V. (SOFTKEYS, [Input], Threshold, -.05, volt)

16. Select Channel Configuration. (SOFTKEYS, [Input], Chnl Config)

17. Proceed as described for the Positive Offset Test and check all channels for -50 mV ±10 mV threshold accuracy.

Gain Test (Negative)

18. Remove both 40 dB attenuators and the 50 Ohm feedthrough from the test setup and set the power supply voltage to -9.00 V (reading on DVM).
   (PAGES, )

   (PAGES, SOFTKEYS, )

21. Set the threshold to -8.81 V and check that the corresponding timing display is low. (-8.81, )

22. Set the threshold to -9.19 and on pressing , the timing display should jump to high.

23. Repeat step 21 and 22 for all data channels.

Gain Test (Positive)

24. Change power supply voltage to +9.00 V.

25. Set the threshold to +8.81 V and check that the corresponding timing display is high. (8.81, )

26. Set the threshold to +9.19 and on pressing , the timing display should jump to low.

27. Repeat step 25 and 26 for all data channels.

Note: When testing channels at connectors 3 to 7, move the timing diagrams display up:
   (PAGES, SOFTKEYS, )
   or
   [until required connectors are displayed]. SOFTKEYS, , }
7-10 Qualifier Threshold and Impedance Tests

Specification

Threshold accuracy: ±3% of set value ±50mV.

Description

This test is used to measure the high and low level detection voltage (hysteresis) to determine the actual threshold voltage of the Qualifier Inputs (TTL setting). By measuring the voltage drop across the 20dB attenuator when switching the input to 50Ω, proper input impedance selection can be verified.

Figure 7-9. Test Setup for the Qualifier Threshold and Impedance Test

Equipment

- DC Power Supply
- Digital Voltmeter
- BNC - Tee
- BNC (f) to dual banana plug (2 off)
- Capacitor
- Attenuator 20 dB (20W)
- 2x Cable Assembly BNC to BNC
- HP 6002A
- HP 3456A
- 1250-0781
- HP J1170C
- 0.22 uF
- (e.g. Texscan HFP 50/20)
- 1251-2277
- HP 11170C

Clock Qualifier Threshold Accuracy Test

1. Program 8182A/B Standard Set.
   (PAGES, MISCELLANEOUS, [RECALL], STANDARD SET, [EXECUTE])

2. Set Clock Source to Internal.
   (PAGES, CONTROL, CLOCK, CLOCK SOURCE, INTERNAL)

3. Set Autoarming Delay to 0s.
   (PAGES, CONTROL, AUTOARMING, DELAY 0s)

4. Set Clock Qualifier to High Level; Set Threshold to +1.4V.
   (PAGES, CONTROL, CLOCK, CLOCK QUALIFIER, LEVEL, HIGH LEVEL, EXIT, THRESHOLD, 1.4, VOLTAGE)

5. Connect the equipment as shown in Figure 7-9 and press RUN.

6. Increase power supply voltage slowly until a clock signal is just indicated in the upper left hand corner of the display and note the DVM reading.
Qualifier Threshold and Impedance Tests

7. Decrease the power supply voltage slowly until the clock indication just disappears and note the DVM reading.
   Result: The mean value should be between +1.31V and +1.49V.

8. Change power supply polarity and set 8182A/B threshold to -1.40V.

9. Increase power supply voltage slowly until the clock indication just disappears and note the DVM reading.

10. Decrease power supply voltage slowly until a clock signal is just indicated and note the DVM reading.
    Result: The mean value should be between -1.31V and -1.49V.

50 Ohm Impedance Test

11. Set the power supply voltage for a -1.40V reading on the DVM.

12. Set the Clock Qualifier Input Impedance to 50Ω.
    The DVM should show approximately -0.7 V.
Trigger Qualifier Threshold Accuracy Tests

7-11 Trigger Qualifier Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
   (PAGES, *RECALL, Standard Set, EXECUTE)

2. Clock Source Internal.
   (PAGES, *CONTROL, Clock Source, INTERNAL)

3. Set Autoarming Delay to 0s.
   (PAGES, *CONTROL, Autoarming, DELAY 0s)

4. Trigger Qualifier High Level; Threshold +1.4V.
   (PAGES, *CONTROL, Trig Qualifier, Level, HIGH LEVEL, EXECUTE, INTERNAL)

5. Connect the equipment as shown in Figure 7-9 and press RUN.

6. Increase power supply voltage slowly until the status display in the upper right hand corner of the display jumps just from ARMED to IDLE (IDLE toggles) and note the DVM reading.

7. Decrease power supply voltage slowly until the display just jumps to ARMED and note the DVM reading.
   Result: The mean value should be between +1.31V and +1.49V

8. Change power supply polarity and set 8182A/B threshold to -1.40V.

9. Increase power supply voltage slowly until the display just jumps from IDLE to ARMED and note the DVM reading.

10. Decrease power supply voltage slowly until the display just jumps back to IDLE and note the DVM reading.
    Result: The mean value should be between -1.31V and -1.49V

50 Ohm Impedance Test

11. Set the power supply voltage for a -1.4 V reading on the DVM.

12. Program Triger Qualifier Input Impedance to 50Ω.
    (PAGES, *EXIT, *IMPEDANCE, 50 Ω)

    The DVM should show approximately -0.7V.
7-12 Trigger Arm Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
    (PAGES, CONTROL, AUTOARMS, STOP, DELAY, Impedance)

2. Set Clock Source to Internal; Set Clock Period to 1s.
    (PAGES, CONTROL, CLOCK, Source, INTERNAL, Period, Internal, Stop, Delay, Increase [until 1 s is displayed])

3. Set Stop Delay (Internal) to 0.
    (PAGES, CONTROL, STOP, DELAY, 0)

4. Set Autoarming Delay to 0s.
    (PAGES, CONTROL, AUTOARMS, DELAY, 0)

5. Set Trigger Arm Slope to Positive (Threshold is +1.40).
    (PAGES, CONTROL, TRIGGER, ARM, POS, SLOPE)

6. Connect the equipment as shown in Figure 7-9 and press RUN.

7. Increase power supply voltage slowly until the 8182A/B switches from ARMED to ACTIVE (upper right hand corner of display).

    **NOTE**
    Continuous toggling may be caused by noise when the threshold level has just been reached.

    The DVM reading should be between +1.31 V and +1.49 V.

8. Set Trigger Arm Slope to Negative; Set Threshold to -1.4 V.
    (POS, SLOPE, EXT, THRESH, Threshold, -1.4, V, VOLT)

9. Change power supply polarity, press RUN and increase power supply voltage slowly again until the 8182A/B switches from ARMED to ACTIVE. (See Note above.)

    The DVM reading should be between -1.31 V and -1.49 V.

50 Ohm Impedance Test

10. Set power supply voltage for a -1.40 V reading on the DVM.

11. Set Trigger Arm Input Impedance to 50Ω.
    (EXT, THRESH, IMPEDANCE, 50, Ω)

    The DVM should show approximately -0.7 V.
7-13 External Stop Threshold Accuracy Tests

1. Program 8182A/B Standard Set.
   (PAGES, [EXECUTE])

2. Set Clock Source to Internal; Set Clock Period to 100ms.
   (PAGES, [INTERNAL], [CLOCK], [PERIOD], [100MS], [INCREASE])

3. Set Stop Delay (Internal) to 0.
   (PAGES, [STOP DELAY], [0], [ENTER NUMBER])

4. Set Autoarming Delay to 1s.
   (PAGES, [AUTO ARM], [DELAY], [1SEC])

5. Set External Stop to Positive Slope (Threshold is +1.40).
   (PAGES, [POS SLOPE], [STOP], [THRESH], [1.4], [VOLT])

6. Connect the equipment as shown in Figure 7-9 and press RUN.

7. Increase power supply voltage slowly until the 8182A/B switches from ACTIVE to IDLE (upper right hand corner of display).

   **NOTE**

   Continuous toggling may be caused by noise when the threshold level has just been reached.

   The DVM reading should be between +1.31V and 1.49V.

8. Program Negative Slope; Threshold -1.4 V.
   (NEG SLOPE, [STOP], [THRESH], [-1.4], [VOLT])

9. Change power supply polarity, press RUN and increase power supply voltage again until the 8182A/B switches from ACTIVE to IDLE. (See the Note above.)

   The DVM reading should be between -1.31V and 1.49 V.

50 Ohm Impedance Test

10. Set power supply voltage for a -1.40V reading on the DVM.

11. Set External Stop Input Impedance to 50Ω.
    ([STOP], [INPUT], [IMPEDANCE], [50])

    The DVM should show approximately -0.7V.
Retrofit Procedures

Chapter 8
Retrofit Procedures for HP Models 8180A/B, 8181A/B, 8182A/B

8-1 Introduction

This chapter describes the procedures when retrofitting (upgrading) the HP 8181A/B generator, the HP 8181A/B extender and the HP 8182A/B analyzer.

8-2 81801A/B Retrofit Procedure for 8180A/B (4 additional NRZ channels)

1. Remove top and bottom cover.

   When removing the holding screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the top cover, and gently levering the cover off the rear frame as the holding screw is removed.

2. Remove the blank connector of the next available connector (e.g. connector 3 if 0, 1 and 2 are already fitted).

3. Remove board spacer.

4. Ensure that the PC-edge connectors of the Module Board are clean.

5. Insert the Module Board A6 (A66) in the next available slot (e.g. Module 3 if Module 0, 1 and 2 are already installed).

6. Install data connector on the rear panel.

7. Install board spacer and readjust the Power Supply.

8. Perform Output Amplifier High/Low Level Adjustment for the retrofitted NRZ channels.

9. With top and bottom cover fitted, allow instrument to warm up for 30 minutes and check the skew of all NRZ channels for ±1ns (A-version) and ±0.8ns (B-version), referenced to the strobe clock signal (Performance test). If the skew of the NRZ channels is out of specification, readjust Strobe Reference Delay.

8-3 81801 A/B Retrofit Procedure for 8181 A/B (4 additional NRZ channels)

1. Remove top and bottom cover. When removing the holding screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the top cover, and gently levering the cover off the rearframe as the holding screw is removed.

2. Remove the blank connector of the next available connector (e.g. connector 7 if connectors 4, 5 and 6 are already occupied).

3. Remove board spacer.

4. Ensure that the PC-edge connectors of the Module Board are clean.

5. Insert the Module Board A6 (A66) in the next available slot (e.g. Module 7 if Module 4, 5 and 6 are already installed).

6. Install data connector on the rear panel.

7. Install board spacer and readjust the Power Supply.

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Retrofit Procedures

8. Perform Output Amplifier High/Low Level Adjustment for the retrofitted NRZ channels.

9. With top and bottom cover fitted, allow instrument to warm up for 30 minutes and check skew of all NRZ channels for ±1ns (A-version) and ±0.8ns (B-version), referenced to the strobe clock signal (Performance test), of the 8180 A/B. If the skew of the NRZ channels is out of specification, readjust Extender 0 Delay slightly.

8-4 81802A/B Retrofit Procedure for 8180A/B (4 additional Timing channels)

1. Remove top and bottom cover. When removing the retaining screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the top cover, and gently levering the cover off the rear frame as the retaining screw is removed.

2. Remove the blank connector of the next available connector (e.g. connector3 if 0, 1 and 2 are already fitted).

3. Remove the board spacer.

4. Ensure that the PC-edge connectors of the Module Board and timing board are clean.

5. Insert the Module Board A6 (A66) in the next available location (e.g. Module 3 if Module 0, 1 and 2 are already installed).

6. Install data connector on the rear panel.

7. Insert the timing board A5 (A65) in location Timing 0 or Timing 1 if Timing 0 is already fitted.

8. Install board spacer.

9. Install bottom cover and continue with Power Supply Adjustment.

Module Board A6 (A66) Adjustment

10. Allow instrument to warm up and perform Output Amplifier High/Low Level Adjustment for retrofitted NRZ channels.

11. Check skew of all NRZ channels for ±1ns (A-version) and ±0.8ns (B-version) referred to the strobe clock signal.

NOTE
Readjust the Strobe Reference Delay only when the skew of the NRZ channels is out of specifications.

12. Check Date Flatness And Overshoot. Readjust only if necessary.

Timing Board A5 (A65) Adjustment

NOTE
Use Adjustment Cover and allow instrument to warm up for 30 minutes.

13. If this is the first time a timing board is being installed, then the Preadjustment For Timing Channels must be carried out.
Retrofit Procedures

14. Readjust Zero Delay for retrofitted Timing Channels and check Delay and Width ranges as described in Delay and Width Adjustment.

15. Check Zero Delay for both Clock Channels.

8-5 81821 A/B Retrofit Procedure for 8182 A/B (8 additional Data channels)

1. Remove top cover. When removing the holding screw, avoid damaging the threaded hole in the mainframe by inserting a second screwdriver in the corner cutout of the topcover, and gently levering the cover off the rear frame as the holding screw is removed.

2. Remove the cable cover from the rear frame.

3. Remove the blank cover from the next available connector (e.g. 4 and 5 if 0, 1, 2 and 3 are already fitted).

4. Remove the 4 screws from the connectors on the 08182-66530 board.

5. Install 08182-66530 board and fasten it with the additional 4 connector screws. (Discard the supplied washers.)

6. Ensure that the PC-edge connectors of the A5 (A65) Data boards are clean.

7. Insert the Data boards (08182-66505/66565) in the next two Data board locations (e.g. Data 4 and Data 5 if Data 0, 1, 2 and 3 are already installed).

   **NOTE**

   If more than 16 channels are installed, the -5.2V load must be removed. Disconnect the brown wire from the -5.2V connector and connect it to the GND connector (both located on the right hand side of the motherboard).

8. Connect the cables coming from the connector board 08182-66530 (installed in step 5 of this procedure) so that the connector marked with the blue dot is connected to the Data board with the even numbers (2, 4 or 6).

9. Fasten the connectors firmly to their corresponding Data boards using the supplied screws.

10. Perform adjustment as described for the A5 (A65) board in the adjustment procedure.

11. Ensure that all cables are correctly connected to their respective board.

12. Re-fit cable cover, board spacer and top cover.
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