The HP 1670-Series
Benchtop Logic Analyzers

Technical Data

Identifying the cause of problems in embedded microprocessor system designs can be difficult. The Hewlett-Packard 1670-series benchtop logic analyzers have the features to help the embedded system design team find hardware and software defects quickly.

With 64K of acquisition memory (1M optional) the HP 1670-series logic analyzers are the first benchtop logic analyzers which display processor mnemonics and verify critical hardware timing relationships over a long period of time.

With the standard Ethernet LAN interface, the software designer can now capture a real-time microprocessor trace and time-correlate it to source code in C++ or other high-level languages on a PC or workstation. For time-correlation of source code, order the HP B3740A Software Analysis package.

The combination of deep memory, large internal disk drive, and LAN make the HP 1670-series of benchtop logic analyzers especially well suited to solving your integration problems.

• Mass storage is provided by an internal hard drive which provides quick storage and retrieval of files.

• The 3.5-inch high-density flexible disk drive supports both DOS and LIF formats.

• The LAN interface enables access to the logic analyzer files via FTP or NFS. Use X11 windows to control or view the logic analyzer on a PC or workstation. The LAN interface includes both Ethertwist (10BASE-T) and ThinLan (10BASE 2) connectors.

• Store data as ASCII files and screen images in TIFF, PCX, and EPS (encapsulated PostScript™) formats.

• New graphical trigger macros make trigger setup easier.

• Centronics, RS-232, HP-IB and LAN communication ports make connecting to other devices easier than ever. All of these come standard on all models of the HP 1670-series.

• The HP 1670-series operating system includes System Performance Analysis (SPA). SPA provides state histograms, state overview, and time interval analysis.

• The HP E2450A Symbolic Download Utility is included with the HP 1670-series. This utility provides the capability to extract symbolic information from popular object module formats.

PostScript™ is a trademark of Adobe Systems Incorporated.

Get to the root cause of problems quickly

The HP 1670-Series Benchtop Logic Analyzers

Logic Analyzer Key Specifications and Characteristics

<table>
<thead>
<tr>
<th>Model Number</th>
<th>HP 1670D</th>
<th>HP 1671D</th>
<th>HP 1672D</th>
</tr>
</thead>
<tbody>
<tr>
<td>State and Timing Channels</td>
<td>136</td>
<td>102</td>
<td>68</td>
</tr>
<tr>
<td>Timing Analysis</td>
<td>Conventional: 125 MHz all channels, 250 MHz half channels</td>
<td></td>
<td></td>
</tr>
<tr>
<td>State Analysis Speed</td>
<td>100 MHz, all channels</td>
<td></td>
<td></td>
</tr>
<tr>
<td>State Clocks/Qualifiers</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory Depth per Channel</td>
<td>64K per channel, 128K in timing half-channel mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1M per channel optional memory, 2M in timing half-channel mode)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Human Interface

#### Front Panel
A knob and keypads make up the front-panel human interface. Keys include control, menu, display navigation, and alpha-numeric entry functions.

#### Mouse
A DIN mouse is shipped as standard equipment. It provides full instrument control. Knob functionality is replicated by holding down the right button and moving the mouse left or right.

#### Keyboard
The logic analyzer can also be operated using a DIN keyboard. Order the HP Logic Analyzer Keyboard Kit, model number HP E2427B.

### Input/Output, Control, and Printing

#### I/O Ports
All units ship with a Centronics parallel printer port, RS-232, and HP-IB as standard equipment.

#### LAN Interface
An Ethernet LAN interface is standard with the HP 1670-series. The LAN interface comes with both Ethertwist (10BASE-T) and ThinLan (10BASE 2) connectors. The LAN supports FTP and PC/NFS connection protocols. It also works with X11 window packages.

### Software and Analysis Capability

#### HP 1670-Series Software Analyzer
The HP B3740A Software Analyzer provides true source line referencing and symbol download capabilities. Standard object module formats are supported.

### Program-mability
Each instrument is fully programmable from a computer via HP-IB and RS-232 connections. This feature is standard on all models.

### HP Printer Support
Printers which use the HP Printer Control Language (PCL) and have a parallel Centronics, RS-232 or HP-IB interface are supported: HP Deskjet, Laserjet, Quietjet, Paintjet, and Thinkjet models.

### Alternate Printer Supported
The Epson FX80, LX80 and M X80 printers with an RS-232 or Centronics interface supported in the Epson 8-bit graphics mode.

### Hard Copy Output
Screen images can be printed in black and white from all menus using the Print field. State or timing listings can be printed in full or part (starting from center screen) using the Print All selection.

### ASCII Data Files
State or timing listings can be stored as ASCII files on a flexible disk via the display’s Print field. These files are equivalent in character width and line length to hardcopy listings printed via the Print All selection.

### Mass Storage Files and Software

#### Updating the Operating System
The operating system resides in Flash ROM and can be updated from the flexible disk drive or the hard disk drive.

### Mass Storage
Is supported by an internal hard disk drive and by a 1,44 M byte, 3.5-inch flexible disk drive. Supports DOS and LIF formats.

### Acquisition Arming

#### Initiation
Arming is started by Run or the Port In BNC.

#### Cross Arming
The analyzer machines can cross-arm each other.

### Output
An output signal is provided at the Port Out BNC.
HP 1670-series Logic Analyzer Specifications and Characteristics

Port In/Out

**PORT IN**
Port In is a standard BNC connection. The input operates at TTL logic signal levels. Rising edges are valid input signals.

**PORT OUT**
Port Out is a standard BNC connection with TTL logic signal levels. A rising edge is asserted as a valid output.

Arming Times

**PORT IN**
15 ns typical delay from signal input to a don't care logic analyzer trigger.

**PORT OUT**
120 ns typical delay from logic analyzer trigger to signal output.

Operating Environment

**Power**
115 Vac or 230 Vac, –22% to +10%, single phase, 48-66 Hz, 320 VA max

**Temperature**
Instrument, 0° to 50° C (+32° to 122° F). Disk media, 10° to 40° C (+50° to 104°F). Probes and cables, 0° to 65° C (+32° to 149° F)

**Humidity**
Instrument, up to 95%, relative humidity at +40° C (+140° F). Disk media and hard drive, 8% to 85% relative humidity.

**Altitude**
To 3,048 m (10,000 ft)

**Vibration:**

- **Operating**
  Random vibrations 5–500 Hz, 10 minute per axis, ~0.3 g (rms).
- **Non Operating**
  Random vibrations 5–500 Hz, 10 minutes per axis, ~2.41 g (rms); and swept sine resonant search, 5–500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

Physical Factors

**Weight**
28.6 lbs. (13 kg)

**Dimensions**
See figure 1

**Safety**
IEC 348/HD 401, UL 1244, and CSA Standard C22.2 No. 231 (series M-89)

EMC
Group 1 Class A
4kV CD, 8kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3V/m
IEC 801-4:1988/EN 50082-1 (1992): 1kV

Logic Analyzer Probes

**Input Resistance**
100 kΩ ±2%

**Input Capacitance**
average approx. 8 pF

**Input**
approx. 8 pF

**Capacitance**
(see figure 2)

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Figure 1

Figure 2

Weight 28.6 lb. (13 kg)

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[1] Time may vary depending upon the mode of logic analyzer operation.

* Warranted Specification
**State Analysis**

<table>
<thead>
<tr>
<th>Maximum State Speed</th>
<th>100 MHz</th>
</tr>
</thead>
</table>

| Channel Count [2] | HP 1670D 136/68 | HP 1671D 102/51 | HP 1672D 68/34 |

**Memory Depth per Channel**

<table>
<thead>
<tr>
<th>Standard</th>
<th>64K (65,536) samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Tags On</td>
<td>32K (32,768 samples)</td>
</tr>
<tr>
<td>Compare Mode On</td>
<td>32K (32,768 samples)</td>
</tr>
<tr>
<td>Compare Mode and Time Tags On</td>
<td>32K (32,768 samples)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option 030</th>
<th>1M (1,032,192 samples)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Tags On</td>
<td>500K (507,904 samples)</td>
</tr>
<tr>
<td>Compare Mode On</td>
<td>250K (245,760 samples)</td>
</tr>
<tr>
<td>Compare Mode and Time Tags On</td>
<td>120K (114,688 samples)</td>
</tr>
</tbody>
</table>

**State Clock Qualifier**

- The high or low of the clocks can be ANDed or ORed with the clock specification.

**Setup/Hold [3]**

- one clock, one edge: 3.5/0 ns to 0/3.5 ns (in 0.5 ns increments)
- one clock, both edges: 4.0/0 ns to 0/4.0 ns (in 0.5 ns increments)
- multi-clock, multi-edge: 4.5/0 ns to 0/4.5 ns (in 0.5 ns increments)

**Minimum State Clock Pulse Width [3]**

- 3.5 ns

**Minimum Master to Slave Clock Time [3]**

- 10 ns

**Minimum Slave to Slave Clock Time [3]**

- 10 ns

**Minimum Master to Master Clock Time [3]**

- 10 ns

**Clock Qualifiers**

- Maximum: 4.0 ns

**Setup/Hold [3]**

- 4.0/0 ns (fixed)

**State Tagging [4]**

- Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Max. count is $4.29 \times 10^9$.

**State Tag Count**

- 0 to $4.29 \times 10^9$

**State Tag Resolution**

- 1 count

**Time Tag Value**

- 8 ns to 34.4 seconds ± (8 ns + 0.01% of time tag value)

**Time Tag Resolution**

- 8 ns or 0.1% (whichever is greater)

**Timing Analysis**

**Conventional Timing**

- Data stored at selected sample rate across all timing channels.

<table>
<thead>
<tr>
<th>Maximum Timing Speed [2]</th>
<th>125 M Hz/250 M Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Count [2]</td>
<td>HP 1670D 136/68</td>
</tr>
<tr>
<td>Sample Period [2]</td>
<td>8 ns/4 ns minimum</td>
</tr>
</tbody>
</table>

**Memory Depth per Channel [2]**

<table>
<thead>
<tr>
<th>Standard</th>
<th>64K/128K samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Depth</td>
<td>(65,536/131,072)</td>
</tr>
</tbody>
</table>

**Time Covered by Data [2]**

- Sample period x memory depth

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[2] Full Channel /Half Channel Modes

[3] Specified for an input signal VH= – 0.9V, VL = – 1.7V, slew rate = 1V/ns, and threshold = – 1.3V

[4] Time or-state-tagging (Count Time or Count State) is available in the full-channel state mode. There is no speed penalty for tag use. Memory is halved when time or state tags are used unless a pod pair (34-channel group) remains unassigned in the Configuration menu.
### Qualifier
A user-specified term that can be any state, no state, any recognizer, (pattern, ranges or edge/glitch), any timer, or the logical combination (NOT, AND, NAND, OR, NOR, XOR, NXOR) of the recognizers and timers.

### Branching
Each sequence level has a branching qualifier. When satisfied, the analyzer will branch to the sequence level specified.

### Occurrence Counters
Sequence qualifier may be specified to occur up to 1,048,575 times before advancing to the next level. Each sequence level has its own counter.

### Storage Qualification
Each sequence level has a storage qualifier that specifies the states that are to be stored.

### Maximum Sequencer Speed
125 MHz

### Time Interval Accuracy

<table>
<thead>
<tr>
<th>Sample Period Accuracy</th>
<th>± 0.01%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel-to-Channel Skew</td>
<td>2 ns typical, 3 ns maximum</td>
</tr>
<tr>
<td>Time Interval Accuracy</td>
<td>± (Sample Period + channel-to-channel skew + 0.01% of time interval reading)</td>
</tr>
</tbody>
</table>

### Maximum Delay After Triggering

| Sample Period 4-8 ns: 8.389 ms |
| Sample Period > 8 ns: 1,048,575 × sample period |

### Trigger Specifications

| Trigger Macros | Trigger setups can be selected from a categorized list of trigger macros. Each macro is shown in graphical form and has a written description. Macros can be chained together to create a custom trigger sequence. |
| Pattern Recognizers | Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. |
| Pattern Recognizers (in channels) | 10 |
| Pattern Width (in channels) | HP 1670D 136/68 |
| HP 1671D 102/51 |
| HP 1672D 68/34 |
| Minimum Pattern and Range Recognizer Pulse Width | 125 MHz and 250 MHz |
| Timing Modes: 13 ns + channel-to-channel skew ≤ 125 MHz Timing Modes: 1 sample period + 1 ns + channel-to-channel skew + 0.01% |

### Range Recognizers
Recognize data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones).

| Range Recognizers | 2 |
| Range Width | 32 channels |

### Edge/Glitch Recognizers
Trigger on glitch or edge on any channel. Edge can be specified as rising, falling or either.

| Edge/Glitch Recognizers | 2 (in timing mode only) |
| Edge/Glitch Recovery Time | Sample Period 4-8 ns: 26 ns |
| Sample Period > 8 ns: 20 ns + sample period |

### Greater than Duration (timing only)

| Sample period > 8 ns: (1 to 220) × sample period |
| Accuracy is –2 ns + sample period – 2 ns ± 0.01% |

### Less than Duration (timing only)

| Sample period > 8 ns: (1 to 220) × sample period |
| Accuracy is 2 ns + sample period – 2 ns ± 0.01% |

### Pattern Recognizers
Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label.
Timers

- Timers may be Started, Paused, or Continued at entry into any sequence level after the first.

- **Timers**
  - **Range**: 400 ns to 500 seconds
  - **Resolution**: ± 32 ns or ± 0.1%, whichever is greater
  - **Accuracy**: ± 32 ns or ± 0.1%, whichever is greater
  - **Recovery Time**: 70 ns

**Data In**
- **110 ns typical**

**Trigger Out**
- **BNC Port**

**Acquisition, Measurement and Display Functions**

- **Arming**: Each analyzer can be armed by the Run key, the other analyzer, or the Port In.
- **Run**: Starts acquisition of data in specified trace mode.
- **Stop**: Stop halts acquisition and displays the current acquisition data.
- **Trace Mode**: Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until Stop is pressed or until pattern time interval or compare stop criteria are met.
- **Trigger**: Displayed as a vertical dashed line in the timing waveform, state waveform and X-Y chart displays and as line 0 in the state listing and state compare displays.

**Activity Indicators**
- Provided in the Configuration, State Format, and Timing Format menus for monitoring device-under-test activity while setting up the analyzer.

**Labels**
- Channels may be grouped together and given a 6-character name called a label. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label. Trigger terms may be given an 8-character name.

**Measurement Functions**

- **Markers**: Two markers (x and o) are shown as dashed lines in the display.
- **Time Intervals**: The x and o markers measure the time interval between events occurring on one or more waveforms or states. Available in state when time tagging is on.
- **Delta States**: The x and o markers measure the number of tagged states between any two states (state only).
- **Patterns**: The x or o marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The o marker can also find the nth occurrence of a pattern before or after the x marker.
- **Statistics**: x to o marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum x to o time, maximum x to o time, average x to o time, and ratio of valid runs to total runs.

**Compare Mode Functions**
- Performs post-processing bit-by-bit comparison of the acquired state data and Compare Image data.
- **Compare Image**: Created by copying a state acquisition into the compare image buffer. Allows editing of any bit in the Compare Image to a 1, X or O.
- **Compare Image Boundaries**: Each channel (column) in the compare image can be enabled or disabled via bit masks in the Compare Image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.

**Compare Mode Measurement**
- Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current Compare Image is equal or not equal.

**Compare Image Displays**
- Reference Listing display shows the Compare Image and bit masks; Difference Listing display highlights differences between the current state acquisition and the Compare Image.
### Data Entry/Display

<table>
<thead>
<tr>
<th>Display Modes</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>State Listing, State Waveforms, State Chart, State Compare Listing, Compare Difference Listing, Timing Waveforms, Timing Listing, interleaved time-correlated listing of two state analyzers (time tags on), and time-correlated State Listing with Timing Waveforms on the same display.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>State X-Y Chart Display</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plots value of a specified label (on y-axis) versus states or another label (on x-axis). Both axes can be scaled. Correlated to State Listing, State Compare, and State Waveform displays. Available as pattern, time, or statistics (with time counting) and states (with state counting on). Chart display is not erased between successive acquisitions. Displays state acquisitions in waveform format. Multiple channels can be displayed on one waveform display line. Displays timing acquisition in waveform format. 1 ns to 4.4 sec/div/1 ns to 2.2 sec/div -2.500 s to +2.500 s Waveform display is not erased between successive acquisitions. Waveform size set to large, the value represented by each waveform is displayed inside the waveform in the selected base. 1000 maximum.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Marker</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pattern Symbols</td>
<td>User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs.</td>
</tr>
<tr>
<td>Range Symbols</td>
<td>User can define a mnemonic covering a range of values. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>Pattern Symbols</td>
</tr>
<tr>
<td>Range Symbols</td>
<td>User can define a mnemonic covering a range of values. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Number of Symbols</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000 maximum.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing Waveform Display</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sec/div [2]</td>
<td>1 ns to 4.4 sec/div/1 ns to 2.2 sec/div</td>
</tr>
<tr>
<td>Delay</td>
<td>-2.500 s to +2.500 s</td>
</tr>
<tr>
<td>Accumulate</td>
<td>Waveform display is not erased between successive acquisitions.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing Waveform Display</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sec/div [2]</td>
<td>1 ns to 4.4 sec/div/1 ns to 2.2 sec/div</td>
</tr>
<tr>
<td>Delay</td>
<td>-2.500 s to +2.500 s</td>
</tr>
<tr>
<td>Accumulate</td>
<td>Waveform display is not erased between successive acquisitions.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overlay Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiple channels can be displayed on one waveform display line.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Displayed Waveforms</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>System Performance Analysis</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPA includes state histogram, state overview and time interval measurements to aid in the software optimization process. These tools provide a statistical overview of your synchronous design. For additional information, refer to HP 10390A System Performance Software technical data sheet, pub no. 5091-7850E.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bases</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary, Octal, Decimal, Hexadecimal, ASCII (display only), symbols, two's compliment.</td>
<td></td>
</tr>
</tbody>
</table>

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[2] Full Channel / Half Channel Modes
Ordering Information

HP 1670D-Series Benchtop Logic Analyzers

HP 1670D  136-Channel 100-MHz State/250-MHz Timing with 64K Memory Depth and Ethernet LAN

HP 1671D  102-Channel 100-MHz State/250-MHz Timing with 64K Memory Depth and Ethernet LAN

HP 1672D  68-Channel 100-MHz State/250-MHz Timing with 64K Memory Depth and Ethernet LAN

Additional HP 1660C/CS and 1670D-Series Product Options

Opt 030  Extended Memory depth to 1M samples/channel (ordered at the time of purchase)

Opt 0B3  Add Service Manual

Opt 1CM  Rack Mount Kit

Opt UK9  Front Panel Cover

Opt W30  3-Year extended repair service

Opt W50  5-Year extended repair service

Opt OB6  Add Programming Manual

Accessory Software

HP B3740A  Software Analyzer

Opt A4  IBM, 3.5-inch Media/Documentation

Opt AAY  HP 9000 Series 700 Media/Documentation

Opt AAU  SUN (Solaris and SUN OS) Media/Documentation

Opt UDY  IBM Single User License

Opt UBY  HP 9000 Series 700 Single User License

Opt UBK  SUN (Solaris and SUN OS) Single User License

HP 10391B  Inverse Assembler Development Package

HP 1670D-Series Upgrades

HP E2471D  Upgrade HP 1670D-Series from 64K to 1M of memory

Opt 001  Upgrades HP 1670D from 64K to 1M of acquisition memory

Opt 002  Upgrades HP 1671D from 64K to 1M of acquisition memory

Opt 003  Upgrades HP 1672D from 64K to 1M of acquisition memory

HP E2427B  Add keyboard with DIN connector (PC style)

State/Timing Analyzer Probes & Lead Sets

HP 5959-9333  5 Grey Probe Leads for HP 1670D-Series

HP 5959-9334  5 Long Ground Leads for HP 1670D-Series

HP 5959-9335  5 Long Ground Leads for All State and Timing Analyzers

HP 01650-61608  16-Channel Probe Lead Set for State and Timing Analyzers

HP 01650-63203  Termination Adapter for State and Timing Analyzers

HP 1810-1278  9-Channel IC Termination DIP

HP 1810-1588  Termination IC SIP

HP 1251-8106  2 x 10, 0.1-inch Center Header (Similar to 3M p/n 2520-6002)

HP 5090-4356  Surface-Mount Grabbers (package of 20)

HP 5959-0288  Throughhole Grabbers (package of 20)

Other Accessories for HP Logic Analyzers

HP 1180B  Testmobile for the HP 1670-Series

HP 92199B  Power Strip

HP 5041-9456  Front Cover for HP 1670-Series

HP 5062-7379  Rack Mount Kit for HP 1670-Series

For more information on Hewlett-Packard Test & Measurement products, applications or services please call your local Hewlett-Packard sales offices. A current listing is available via Web through AccessHP at http://www.hp.com. If you do not have access to the internet, please contact one of the HP centers listed below and they will direct you to your nearest HP representative.

United States:  Hewlett-Packard Company
Test and Measurement Organization
5301 Stevens Creek Blvd.
Bldg. 5L-SC
Santa Clara, CA 95052-8059
1 800 452 4844

Canada:  Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario L4W 5G1
(905) 206 4725

Europe:  Hewlett-Packard
European Marketing Centre
P.O. Box 999
1180 AZ Amstelveen
The Netherlands

Japan:  Hewlett-Packard Japan Ltd.
Measurement Assistance Center
9-1, Takakura-Cho, Hachioji-Shi,
Tokyo 192, Japan
Tel: (81-426) 56-7832
Fax: (81-426) 56-7840

Latin America:  Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive, 9th Floor
Miami, Florida 33126, U.S.A.
(305) 267 4245/4220

Australia/New Zealand:  Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
1 800 629 485

Asia Pacific:  Hewlett-Packard Asia Pacific Ltd
17-21/F Shell Tower, Times Square,
1 Matheson Street, Causeway Bay,
Hong Kong
Fax: (852) 2506 9285

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