**CodeTAP** Emulator  
for Intel i960 H-Series Processors

**Highlights**

- Real-time, in-circuit development system for software engineers
- Supports all HA, clock-doubled HD and clock-tripled HT processors with a single CodeTAP® probe and user interface at full-rated processor speed
- Powerful multi-windowed MWX-ICE C/C++ debugger interface runs on Sun4, HP 9000/700 and PC hosts  
  - Convenient access to all the information you need  
  - Complete control of CodeTAP features  
  - Visibility and control of your target application
- Common debugger interface with Applied’s companion CodeICE 960 Hx emulator
- Supports Intel, Cygnus, and MRI toolchains
- Debugger operates stand-alone or in the MRI MasterWorks environment
- Macro-extension language uses C-like statements and debugger commands to construct and save debug sequences and target regression test
- Intuitive CPU Browser interface to fully configure, visualize and change internal 960 Hx register states (DLMCON, PMCONs, ICON, MPARs, etc.)
- Real-time instruction trace captures 64K frames of execution history at full speed with caches enabled
- Convenient profiling and code coverage support for Intel’s optimizing compilers
- Optional 1 MB high speed overlay memory available
- Seamless networking support for both workstations and PCs
- Versatile run-control services target interrupts while the emulator is paused, allows user interaction with CodeTAP functions without stopping execution
- 6 hardware access, 6 hardware execution, and 50 software execution breakpoints

**Companion Products**

- CodeICE™ 960 Hx emulator complements CodeTAP 960 Hx with full-scale development support of HA, HD and HT processors using a single probe-tip and the same MWX-ICE user interface

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**How to Do More for Less**

Couldn’t you get more done if you had your own emulator? Of course you could. Now low-cost CodeTAP emulators put emulation power in the hands of more engineers. Applied invented CodeTAP emulation technology (U.S. patent no. 5,228,039) to give software engineers visibility and control for executing and debugging code at a cost that lets teams use tools wherever they’re needed. The latest in the family is CodeTAP 960 Hx, built for the speed of the 960 Hx processor, and delivering the productivity boost you need to finish on-schedule and beat the time-to-market clock.

CodeTAP 960 Hx supports all H-series variants with one probe and user interface, at full-rated processor speed. It runs in-circuit, with no intrusion on your target environment, so you get fully transparent, real-time debug capability.

**Unique “Full-Power” Emulation Features**

CodeTAP 960 Hx speeds development with 64K frames of instruction trace, hardware and software breakpoints, multi-mode run control, high-speed download and the graphical CPU Browser™ register configuration interface. All features are accessed through the powerful MWX-ICE debugger.

You can use the CodeTAP emulator with Applied’s full-featured CodeICE 960 Hx emulator to give your team a full complement of real-time debugging features at your fingertips. This means you can put just the right selection of debug speed and power into the hands of every engineer on the team.

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We also offer tools to support these Intel products:  
80960 CA/CF/Jx/Rp; 80C186/188 XL, EA, EB, EC; 80L186/188 XL, EA, EB, EC; 80286; 80386 SX/DX; 386EX
A Tool for Today’s Software Developers
CodeTAP 960 Hx, like Applied’s entire line of CodeTAP emulators, was designed with the growing legions of embedded software developers in mind. As software grows in complexity, companies are looking to arm developers with sophisticated debug tools that are easy to learn and use, and also small and affordable so they can be put on every developer’s desktop.

Non-Intrusive, No-Compromise Debugging Power
Offering true transparency, CodeTAP 960 Hx requires no code modifications and doesn’t consume target memory, I/O ports or interrupt vectors. The CodeTAP emulator provides a quick “plug-and-go” target connection, replacing the 80960 HA, HD, or HT processor on the target with a compact Target Access Probe. Using customized ASIC technology, CodeTAP 960 Hx delivers no-compromise performance—such as 75 MHz internal and 40 MHz external bus speeds—and a rich feature set that supports the entire H-series with a single CodeTAP probe and debugger.

Versatile Communications Solutions
Ethernet communications is included with CodeTAP 960 Hx for Sun and HP workstations, and is an available option for use on Windows PC hosts. The Ethernet link allows shared use of the CodeTAP on a LAN, including those which are subnetted. This connection lets you directly download large C/C++ applications from a networked file system into your target quickly, whether the target is on your desktop or in the lab across the street. For Windows PC users on a restricted budget, a High-Speed Serial card provides high-throughput point-to-point communication capability. Either Ethernet communications method combined with a PC and the CodeTAP’s small form factor makes it ideal for field debugging anywhere, anytime.

The Ease and Power of Graphical Debugging
Applied’s MWX-ICE debugger interface provides complete control and visibility of the target application, letting embedded developers quickly and easily view and control code execution in the target. MWX-ICE combines a point-and-click windowed interface, extensive macro capabilities, and a comprehensive hypertext on-line help system with specially engineered support for all the features of the CodeTAP 960 Hx. Users can access information including application code, data structures, processor registers, breakpoint information, trace capture, and issue debugging and emulation commands. MWX-ICE accepts executables from the popular tool chains, such as Intel’s i960 CTOOLS and GNU960, Cygnus C/C++, and MRI’s C/C++ compilers. The interface provides complete control of CodeTAP functions and code execution for transparent debugging, and is available in native versions for each supported host.

MWX-ICE displays include: C-source statements in the Code window; array contents in the Data window; stack contents in the Stack window; elements of data structures and their values in the Inspector window; and memory contents in the Memory window.
Real-Time, Non-Stop Execution Trace
To see what’s really going on in your target system under real-time conditions, an execution trace history is necessary. CodeTAP’s instruction trace captures 64K frames of execution history that will verify the correct performance of the software and hardware, and help pinpoint errors that may occur in the program’s execution. For targets that can’t be stopped to debug a problem, you can examine trace while the CodeTAP runs the target. You can store trace history in a file and add comments to the stored trace for later reference or future run comparison.

To debug code that makes the most of heavily cached processors, such as the Hx family, you need a means of seeing the entire execution history — even if the instruction as executed out of cache. Applied’s CodeTAP trace system not only does that, but also disassembles cached instructions. Display can be related in source-level, assembly-level or mixed levels.

Breakpoints for Every Situation
The CodeTAP emulator provides a variety of ways to set breakpoints, depending on the particular target situation. Access to the on-chip hardware execution breakpoints provide break capability on the execution of an instruction or in any medium of memory, be it RAM, ROM or Flash. The on-chip hardware access breakpoints are also available through MWX-ICE and can be set for real-time break capability on address-specific data access or write bus cycles. CodeTAP also provides over 50 software execution breakpoints for code located in RAM or CodeTAP overlay memory.

Specialized Tools for Target Visibility and Control
In many cases, tracking down real-time bugs involves continuous target operation. You simply cannot stop your target in order to debug code or else your network may stop, the machine may lose control, or you may simply lose the context of the problem if you stop emulation. CodeTAP’s flexible run-control helps support these considerations by providing the ability to interact with or update the debugger while still running the target. It can also continue to service target interrupts even when you have stopped on a breakpoint. These are processor control features that you just can’t get with a “general purpose” emulator.

Overlay Memory
High-speed overlay memory helps maximize your investment by eliminating time spent burning ROMs or programming Flash to verify a code fix. Even before your target hardware system may be ready, the CodeTAP combined with overlay memory provides a real-time execution vehicle so you can get going early. Simply map the overlay memory to mimic your target system read-only or read-write memory. 1 MB of overlay memory is available for the CodeTAP 960 Hx.

CPU Register Utility
The CPU Browser utility provides a guided, error-proof means to configure and visualize the states and meanings of all the 960 Hx registers, such as the DLMCON, PMCONS, ICON, and more. Its graphical display shows current or proposed register configuration information, with point-and-click access to all configurable bit fields. The CPU Browser includes clear descriptions of individual bit fields and checks changes for errors before they are applied.

A Family of 960 Hx Tools
CodeTAP 960 Hx joins the full-featured CodeICE 960 Hx to provide engineers and project managers a choice in both lower-cost tools for everyday software debugging and more powerful tools to root out the toughest bugs. A compatible family, both CodeTAP and CodeICE 960 Hx share a common MWX-ICE debug front-end to leverage experience and training.

To see how the new CodeTAP emulator can let you to do a lot more on your 960 Hx project for a lot less, call 1-800-426-3925 today. And get an emulator you can call your own.
CodeTAP Emulator for Intel i960 H-Series Processors

**Microprocessors Supported**
Intel 80960HA, 80960HD, 80960HT; at 75 MHz

**Packages Supported**
PGA direct; QFP with optional adapter
Adapters available for rotating pin-one orientation 90°, 180°, and 270°

**Minimum Host Requirements**
PC 386 or better
MS Windows 3.1 or higher, 16 MB RAM minimum, 20 MB suggested
(1 vacant ISA or EISA slot for High-Speed Serial)

**SunSPARC**
16 MB RAM minimum, 20 MB swap,
Sun OS 4.1.x, Solaris 2.3,
Ethernet port

**HP 9000/700**
16 MB RAM minimum, 20 MB swap,
HP/UX 9.0 or later, Ethernet port

**Communications**

**PC Environment**
Ethernet (Winsock 1.2, TCP/IP
(including Novell), IEEE 802.3)
10base2, 10base5, 10baseT
High Speed Serial

**Sun / HP Environment**
Ethernet IEEE 802.3 10base2, 10baseT

**User Interface**

**Integrated Source Level Debugger**
Multi-windowed interface (X-windows/
Motif/Open Windows on workstations,
Windows on PC)
Support for Intel, GNU and MRI C / C++ and assembly language
High-level control of all emulation subsystems
Access to all global, local stack-based and register-based symbols with full
data typing features
C-like macro facility extends commands for developing and saving initialization sequences and regression test suites
Data Inspector Window de-references pointers and allows display and modification of structures, structure elements, and unions
Common interface with Applied’s EL 3200, and CodeICE emulators

**Toolchain Compatibility**
Intel, GNU and MRI C / C++ (COFF and IEEE695 objects read directly)

**Target and CPU Awareness and Control**
Flexible run-control
Service system interrupts while execution is paused; debug code without stopping the target system with Dynamic Run feature

**CPU Browser**
Graphical interface allows display and modification of all internal memory, breakpoint, interrupt, and bus controller register values

**Performance Optimizing Tools**
Profile support for Intel’s optimizing C compilers and code coverage utilities
Big Endian support
Transparent translation of little- and big-endian information

**Advanced Testing and Set-Up Capabilities**
Construct complex macros containing C-like statements and CodeTAP control commands
Record and play back debugging sessions

**Trace System**
Trace depth 64K frames of instruction execution history
Display trace data in source, disassembled, or combined levels on-the-fly
Display execution history of cached instructions
Window scrollable forward and backwards

**Breakpoint System**
Six hardware execution breakpoints
Set on line numbers, source statements, program labels and memory addresses in RAM, ROM, or Flash
Six hardware access breakpoints
Set on read or write bus cycles
50 software execution breakpoints
Set in RAM or overlay memory on line numbers, source statements, program labels and memory addresses

**Optional 1 MB Overlay Memory**
No overlap wait states to 33 MHz (one wait state above 33 MHz)
Mappable anywhere in 128K segments
Configure as read-only or read-write to simulate ROM and RAM in the system

**Physical Specifications**
Dimensions: 7.25" x 3.18" x 0.918"
[18.41 cm x 8.07 cm x 2.33 cm]
Physical Specifications
[ L x W x H]
Weight: 7.2 oz. (201 kg.)
Operating temperature: 32-104° F
(0-40° C)

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