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Section I

INTRODUCTION

1.1 General

The inclusion of Error Correction into the HBR 3000 is a result of two factors. The need for error performance which exceeds the error rate of the data gathering and processing system in order to make the recorder transparent to the user and/or the wish to use otherwise marginal quality tape for digital recording applications.

1.2 History

The need for Error Correction was recognized several years ago by both the users and manufacturers of HDDR equipment. The question became more one of how much was needed and what system would yield the necessary performance with the minimum overhead. We originally proposed a relatively complicated system which would have necessitated major system changes but would have provided very high performance with almost any size of error. After a lot of work and some success it was suggested that we try a much simpler system which as it turns out was easier to implement, maintains compatibility with the existing format, and provides sufficient correction for most applications.

As time progressed we also were able to better define the error patterns that occur from tape and some of their typical characteristics. Also, parallel efforts in other parts of the system were able to define the source of errors not due solely to tape and many of these areas were corrected.

1.3 Description

The ECC method we have chosen involves two processes. First, we insert information into each channel of parallel data which allows us to detect, with very high reliability, if errors exist in each 480 bit block of data between sync words. A perpendicular parity is also generated and recorded on a separate track, which allows us to correct the bits in error. The limitation of this system is that if two channels have simultaneous data blocks with one or more errors we cannot correct either of them. This has not proven to be a problem as our calculations and tests have shown that simultaneous errors on two tracks are primarily due to improper handling and care of the tape.

Depending on the uncorrected error rate we are consistently achieving 2 to 4 orders of magnitude of error reduction. It is not unusual to go through an entire roll of tape (90,000 megabits of data) with no errors.

In addition to the effectiveness of the correction, we have also maintained compatibility with the "standard" HBR 3000 tape format. ECC tapes can be reproduced on existing
systems and tapes made on non-ECC systems can be reproduced on ECC systems without any modification to either the HBR system or the interface to the customer. Upgrading of an existing system to an ECC system is not quite as simple as it requires new digital process bay(s), 13 new PWA's per DPB, and a new Mode Select Panel.
2.1 General

The basic HBR system concept and layout has not been changed. The introduction of ECC affects only the Digital Process Bay (DPB) and Mode Select Panel (MSP). See Section III for a discussion of these changes. Improvements in other areas of the system have also been made which, although they do not relate directly to ECC, have improved the raw error rate substantially. ECC of course benefits from this as the Error Correction improves approximately geometrically with improvements in raw error rate. All of the improvements are included or available in the ECC system. In addition most of the improvements can be installed on existing systems to improve their performance.

2.2 Record Electronics

The record system has been improved to minimize the recorded skew and jitter due to the electronics and to minimize the Bias-Data intermodulation products.

2.2.1 Clocked Encoder PWA

PWA 1259673
Sch 1259670

The outputs of the Encoder PWA are now simultaneously clocked so that the residual jitter and timing difference between Encoder chips is eliminated.

2.2.2 13 MHz Bias System

The Bias/Head Driver system used for the 4 MHz at 240 ips system has been incorporated into the ECC system. This minimizes the intermodulation products generated by Bias-Data interaction while retaining the advantages of Bias recording in setup and equalization.

2.2.3 Non Bias Recording

Due to physical limitations in the Airborne products it is necessary to use non-Bias recording when operating at the higher bit rates (above 4 Mbits per second). While this may require some readjustment for large speed changes, this is not felt to be a limitation as the vast majority of airborne users operate at fixed rates and do not require the
flexability of a laboratory system. The system is designed to be compatible with the same reproduce amplifiers used in the bias recorded systems.

2.2.3.1 Line Driver/Filter PWA

PWA 1261763
Sch 1261760

Several versions of the Filter PWA have been created over the past years in attempts to interface with different Head Drivers. The latest version incorporates line drivers which can be jumped for Bias or Non-Bias recording and if properly terminated will match the cable and Head Driver input requirements of most systems.

The new Filter PWA also incorporates up to 4 auxiliary channels (data, either analog or digital, which is not synchronous to the parallel clock) which can be assigned by means of jumpers to channels 1, 10 to 13, 14, and 23 to 26 (corresponding to tracks 1, 12 to 15, and 25 to 28) in the system. Please remember that ECC systems require a Parity channel which is either Channel 12 or 13 and 25 or 26, be sure you don't remove the Parity channel when selecting Aux. channels.

2.3 Reproduce System

A variety of reproduce options are now available for various data rates and customer requirements.

2.3.1 Bay Assembly

The Bay assembly used for Reproduce and Bit Sync Bays is no longer identical. To improve noise rejection and system interface several changes have been necessary which resulted in making the bays different.

2.3.2 Reproduce Amplifier

Three Reproduce amplifier versions have been used in standard HBR systems. They are physically interchangeable in bays with a Speed Encoder PWA pn 1255930-04. The 6 and 7 speed electronics do not need a Low Speed Select PWA installed. The Two Speed (pn 1256153) version is being phased out in favor of the 6 speed (pn 1257253) version as the standard. Both of these PWA's are well covered in the standard HBR Manual (pn 1262016).
2.3.2.1 7 Speed

PWA 1257473
Sch 1257470

This PWA is necessary for the higher density systems. It uses active equalization techniques for the band edge equalization and has separate phase adjustments for 120ips.

2.3.3 Bit Sync-Decoder

Two Bit-Sync Decoder boards are available. They are physically interchangeable.

2.3.3.1 4 Mbit

There are several (?) versions of this around with various part numbers and different designs. Most of the variations are in the input limiter stage and DC restoration circuitry. The standard HBR manual description is fairly complete and up to date.

2.3.3.2 5 Mbit

PWA 1261253
Sch 1261250

This PWA was designed to increase the data rate capability of the 4 Mbit version. It accomplishes this by the use of faster chips, a D/A converter chip in place of the discrete version, and a slightly revised clocking scheme. In addition, the selection of BiPhase/Miller code, BiPhase polarity, and DC Restorer On/Off are by means of switches on the front edge of the PWA instead of jumpers.

2.3.4 Serial Clock Delay

PWA 1259623
Sch 1259620

To provide a delay in the serial clock which matches the parallel clock delay in the reproduce signal processing it is necessary to have this board. At a given serial rate the P/S converter can be jumpered to operate properly, but as the rate changes the phase difference of the parallel and serial clocks will change and the P/S converter will not function properly. If the serial clock is delayed the correct amount this problem is eliminated.
Section III

SYSTEM INTERCONNECT

3.1 General

The following pages show the interconnections required in the HBR 3000 ECC systems. The 14 channel system as shown in Figure 3.1, is virtually identical to the non-ECC system. The 28 channel systems shown in Figure 3.2, is also virtually identical, but if the one-channel parity option is to be used a pair of new interconnect cables, from J48 and J49 in one DPB to J49 and J48 respectively in the other DPB, is required in order to interconnect the A and B bay Error Corrector cards.

3.2 PWA location

Generally the locations of the PWA's is the same as the standard system. As shown in Figure 3.3. One new PWA (The CRC Generator) is added next to the Sync Inserter, Slave Deskews 7/8, 9/10, 11/12 have been moved one slot to the left to make room for two new cards (the Flag Detector/Delay and the Error Corrector). The Serial Clock Delay PWA has been moved between the Error Corrector and P/S Converter to locate it more logically in the signal path. The last PWA location has been reserved for future requirements.

3.3 Connector designations

3.3.1 Internal

In order to simplify the bay for construction and troubleshooting the J numbers of the PWA mating connectors have been revised. They are now J1 to J21 from left to right as you face the front of the bay, The last slot in the bay is J51. Headers which are used for either system interconnect or customer interface have retained the SAME number so there should be no confusion in cabling a system. Headers have been added for ECC interconnect (J48, J49), Monitor functions (J47), and Speed lines (J50) (for future HBR-ES systems).

3.3.2 Customer interface.

The rear panel of the DPB has been significantly revised. See Figure 3.4. The I/O functions are now clearly labeled (no more J numbers) and some optional connector
locations have been added, most notably the Monitor and Spare connectors. The functions have also been grouped in a more logical manner. The DPB assembly is now the same for HBR 3000 and AHBR with only wirewrap differences on the motherboard.

3.4 Mode Select Panel

The Mode Select Panel has been changed to include an ECC ON/OFF switch and an uncorrected error indicator as shown in Figure 3.5. Certain functions have also been removed (512/256 and SSW/NSSW select) and the location of functions has been revised to improve the functional layout. The functions removed were considered to be unnecessary on the front panel. They are still available by jumper selection on PWB's in the DPB.
Section IV

ERROR CORRECTION SYSTEM

4.1 General

The Error Correction System we have chosen is called an orthogonal or rectangular scheme. This means that we use two error detection systems which are at right angles to each other over a defined field of data. For a multi-track tape recorder this is fairly obvious as we have an error detection method used on each track along the tape and another system checking the data across the tape. At the point where these two checks intersect a single bit can be corrected, which is what we do.

4.1.1 Longitudinal Detection

The longitudinal system we use is implemented by a system called a Cyclical Redundancy Check (CRC). A block of data is manipulated by a shift register with feedback which performs a binary combination of the data with a known formula. This results in a Check Word which is not unique to the data but would be very difficult to duplicate with a data pattern which has errors in it. This system tells us if errors have occurred in any one track during the period between the Check Words.

4.1.2 Orthogonal Detection

To detect errors across the tape we use a simple Parity check which requires only that we add a single bit to tell us whether there was an odd or even number of ones or zeroes in the data when it was recorded. This has the limitation of not being able to determine more than one error, but that is a minor limitation on a tape recorder with the track widths we use.

4.2 System

The following page, Figure 4.1 shows the signal flow in the Digital Process Bay with the changes required for ECC in the dashed outlines. The following sections of this manual deal with these changes in more detail. Figure 4.2 and Figure 4.3 show an overall signal flow for the Record and Reproduce sides of the system. Figure 4.2 is applicable in an overall sense to the AHBR system as well as the HBR 3000.
Section V
SYNC INSERTER (ECC) PWA

Part No 1261623
Schematic No 1261620

5.1 Description.

The sync inserter, shown in Figure 5.1 and Figure 5.2, is basically the same as the standard sync inserter. The major differences are in the sync word format, the generation of a parity channel for use in the ECC system and the insertion of data in the Channel 15 and 16 sync words.

5.1.1 Compatibility

This assembly is compatible with the standard Sync Inserter (pn 1803074) and can be used as a replacement in standard HBR systems, future production will probably adopt this as the standard for all systems. Note that the Sync Inserter (Parity), pn 1257573, is NOT the same as the Sync Inserter (ECC) described here and it cannot be replaced by any other sync inserter if its parity function is used.

5.2 Sync Word Generation.

The sync word generation is the same as the standard HBR except that the 17th bit of the 32 bit sync word is a one instead of zero, as shown in Figure 5.3. This creates a sync word which is symmetrical about the center of the last half (ie bit positions 17 thru 32) of the sync word. Since the Deskew logic only reads the last half of the sync word (16 bits) and in fact it ignores the first bit of this pattern the new sync word is compatible with existing systems in the forward direction. Since the first half of the sync word will be used for ECC functions (see CRC GENERATOR/INSERTER) the pattern still remains compatible with existing systems. When ECC is disabled (ECC/N0ECC is low) the sync word reverts to the standard non-ECC 32 bit word with 4 zeroes in the center.

5.3 Parity Channel

The Parity channel is generated as a perpendicular (across the tape) function of the incoming data. It becomes and is treated as a data channel, for the purposes of sync insertion and data distribution, as shown in Figure 5. The Parity generated is called even parity, which means that the Parity Channel will have a one or zero in it such that
the total number of ones, including the Parity Channel, will be even (0, 2, 4, 6, 8, etc). This becomes obvious when an even number of parallel data channels is selected. If they all have the same input data (i.e., Parallel Test Mode) the Parity Channel will be all zeroes.

5.3.1 14 Track Systems.

The Parity channel is handled as if it is Data Channel 12 or 13. For up to 11 customer data channels it will normally be channel 12, if there are 12 customer data channels (or if channel 12 is selected as a data channel with less than 12 data channels) it will be channel 13.

5.3.2 28 Track Systems.

For a 28 track system there will normally be 2 parity channels, one in each DPB, each generated as if each is a separate 14 track system. The Parity channel will be channel 12 or 13 in the A bay and 25 or 26 in the B bay. Note that the channel numbers are not changed, i.e., the first channel in the B bay is still Channel 14.

If it becomes necessary, due to the need for 24 customer channels and an Aux. channel, a single parity channel is generated in the "A" DPB and it is channel 13. The single parity channel is created by taking the parity sum generated in the "B" DPB (PARITY-SI) and combining it with the parity of the "A" DPB channels. While this results in less overhead it also results in less error correction and the corrected error rate may be up to twice (2X) the corrected error rate using two parity channels. The Aux channel will be in the B bay in place of channel 26.

5.4 Parity (ECC) channel selection.

The channels used to create the parity channel (those that will be error corrected) are selected by dip switches on the front of the SYNC INSERTER PWA, as shown in Figure 5.4. Any combination of channels can be selected, except that Channel 13 can only be uncorrected data (no correction on Channel 12) or the Parity channel (Channel 12 is data to be corrected). When ECC is turned off, all 13 channels are available for Customer Data. It is also important to remember that the Filter PWA can select channels 12 and/or 13 as Aux Channels. If this is done the Parity Channel will not be recorded and no error correction can take place. The B bay follows the same convention as the A bay with channel 14 as channel 1 and channel 25 or 26 as the Parity Channel.

5.5 Auto Channel Select.

The Sync Inserter has 2 sync words generated but not normally inserted in the channel 14 and 15 slots of the Master Channel in each DPB. In order to facilitate the setup and configuration of an ECC system these are replaced with a 16 bit block of system information and a 48 bit block of optional customer information, as shown in Figure 5.5.
The first 4 bits (of the 16 bit system block) are ECC channel information, formatted as a sync bit, and then 3 channel select bits. It takes 4 blocks to complete the channel select for all 12 channels in each DPB. In addition the next four blocks contain the same information but inverted for data checking in reproduce mode. The channel select information is taken from the format select switches on this card. The next 12 bits are reserved for later expansion.

5.6 48 Bit Customer Data.

This block (one in each DPB) is provided for the customer to store (record) any information that is of a low rate or "blockable" nature. The system provides a gate signal which is 48 bits wide and parallel clock. The first bit of data is clocked into the system on the first positive parallel clock edge after the gate (M48 GATE) goes low. Thus the first bit to be recorded should be at the input before the gate goes low and subsequent data should loaded on positive parallel clock edges.

5.7 Format Compatibility.

Compatibility and tape interchangeability between ECC and non-ECC systems is as follows:

5.7.1 ECC format tapes

1. Tapes recorded with ECC format are playable with Error Correction in the forward direction only and in the reverse direction without Error Correction on ECC equipped systems.
2. Tapes recorded with ECC format are playable on standard (non-ECC) systems only in the forward direction, and of course there will be no Error Correction.
3. Non-ECC systems built with ECC type Deskews will play ECC format tapes in both forward and reverse directions, without error correction of course.

5.7.2 Non-ECC format Tapes

1. ECC systems are capable of playing non-ECC format tapes in the forward direction.
Section VI

CRC GENERATOR/INSERTER (ECC) PWA

Part No. 1261713
Schematic No. 1261710

6.1 Description.

The function of the CRC generator/inserter PWA is to generate a 16 bit binary check-word from the 480 bits of data between sync words and insert this word into the first 16 bits of the 32 bit sync word, as shown in Figure 6.1.

6.2 Gate Generation

In order to generate and insert the check word it is necessary to generate a series of gate signals which correspond to the location of the first 16 bits of the sync word in each data channel. See Figure 6.2.

The counter lines from the Sync Inserter (SI-CTR-A,-B,-C,-D) are used to generate a series of 32 bit gates corresponding to the location of the sync words, they are also used to preset a counter which generates a clock at 1/16 the parallel clock rate. This clock (C16) is used to blank the last half of the 32 bit gate in each channel. This signal, the Check Word Enable (CWE), is used to gate the check word in each channel, but leave the 16 bit sync word intact.

6.3 CRC Generation

The CRC generator is a single IC which performs a binary algebraic operation on incoming serial data. This results in, for the mode we have selected, a 16 bit check sum being generated. The operation is much like a pseudo random data generator. As long as the CWE input is held high and clock is fed into the device it continues to cycle the input data thru a shift register with feedback which controls the algebraic manipulation. When the CWE input is set low, the input data is ignored and during the next 16 clock cycles (the first half of the 32 bit sync period), the remaining states of the shift register are clocked out as a 16 bit CRC check word, as shown in Figure 6.3. At the end of the CWE, the CRC Generator is reset to start a new computation on the next 480 bit block of data. This results in a check word which is generated by and only related to the last 480 bits of data.
6.4 CRC Insertion

The input data from the Sync Inserter is continuously sent to the CRC generator and the output selector switch, as shown in Figure 6.3. When the CWE goes low, indicating a CRC checkword is being sent, the output selector is switched to allow insertion of the CRC checkword.
Section VII

MASTER DESKEW (ECC) PWA

Part No. 1261793
Schematic No. 1261790

7.1 Description.

The Master Deskew PWA is functionally equivalent to the Master Deskew presently used in the HBR system. The only differences are that the Master channel data is brought out for use in the error correction process, the CSAA, CSBA, CSCA, and CSDA lines are brought out to allow synchronization of the error correction electronics and the sync blanking and distributed data outputs are turned off in an ECC system. The counter preset logic is modified to read the ECC format sync words in both forward and reverse, however error correction is only performed in forward mode. See Figure 7.1.

7.1.1 Compatibility

This PWA may be used in place of the Master Deskew PWA (pn 1803064) by changing the E26-E27 (ECC) jumper to E27-E28 (nonECC) and removing the CS driver IC (U8).

7.2 Tape Reference Selection

The circuitry which divides the parallel clock and Master Channel Bit Sync clock to drive the transport in Tape Mode has been changed for operational simplicity and compatibility with various transports. Divide by 2 is selected with solder jumpers, however this mode is very rarely needed and is considered a special case which would probably on be used on otherwise highly modified systems. There are now a pair of DIP switches which allow selection of divide by 4, 8, 16, or 32. This allows simple selection of the frequency which the transport would most like to see. Most systems operate well at divide by 8, but at high packing densities divide by 16 might work better. Conversely at low speeds (ie. below 7 1/2 ips) divide by 4 might work better. The Airborne transports also require frequencies lower than the Lab systems, and this allows simple selection of the appropriate division ratio.

7.3 Sync Detection.

In the standard system the sync word is a 32 bit word symmetrical about the center bits. The logic is such that only the last half of the word is read and thus the logic remains the same for both forward and reverse directions. Actually only the last 15 of the 32 bits are read, thus the new 16 bit sync word with a one as the first sync bit is
compatible with standard sync detection logic. By making the first bit of the 16 bit sync word a 1 the sync word is identical in forward or reverse and sync detection identical to the standard system.

In the ECC system, however, the first half (in forward mode) of the 32 bit period is filled with CRC information, thus if reverse mode were attempted the sync word would be read but it would be 16 bits early and the system would ignore the 16 bits of data before the sync word and assume the CRC word is data. Thus it is necessary, in reverse, to add 16 to the counter preset to correct this. This is accomplished by changing the logic in the counter preset circuitry. This does prevent reading standard (32 bit sync) tapes in reverse as the Sync word would be read where the CRC information would be placed and the effect is to displace the logic 16 bits in the opposite direction to the previous discussion.
8.1 Description.

Changes to the Slave Master Deskew are identical, functionally, to the Master Deskew changes, except there is no transport reference generated on this board, thus no DIP switch.

8.2 Compatibility

The standard Slave Master Deskew (pn 1802995) may be replaced by this PWA if the jumper E9-E10 (ECC) is changed to E10-E11 (nonECC) and the CS driver IC (U20) is removed, except where standard (32 bit sync word) tapes must be read in reverse.
Section IX

SLAVE DESKEW 2 CHANNEL (ECC)

9.1 Description.

The Slave Deskew changes are the same Forward/Reverse logic changes as the Master Deskew.

9.2 Compatibility

The sync blanking and data reinsertion circuitry has a jumper added to allow either ECC or nonECC operation. In ECC position the data and sync are sent directly to the output and in nonECC position the Data Reinsertion and reclocking are connected. This PWA can then be used to replace the 2 Channel Slave Deskew (pn 1808083) in standard HBR systems, except where reverse read of a standard (32 bit sync word) tape is required. Remember this is a 2 channel device and therefore there are two jumpers to change.
Section X

512 BIT DELAY AND ERROR DETECTOR (ECC) PWA

Part No 1261633
Schematic No 1261630

10.1 Description.

As the title indicates there are two functions on this card, detection of errors and delay of the data.

10.2 512 Bit Delay.

Since an error cannot be recognized until after the data has passed, it is necessary to delay the data until after the error check occurs. While this is only 496 bits it is easier from a hardware point of view to delay it 512 bits. Figure 10.1 shows how the delay is accomplished by a pair of 256 bit RAM's in each data channel. A series of counters, synchronized to the Master Channel via the CS lines, generates consecutive addresses to the memory. During the first 80 ns. of each address a data bit is read from that address in the memory, then the Write Enable is activated and a new data bit is written into the same address. 512 clocks later the same address is accessed and thus the data will be read out with a 512 bit delay. Since the Memories only have 256 addresses, two memories are used with the most significant address used as a Chip Select. This has the effect of placing the two memories in series.

10.3 Error Detection.

Error Detection makes use of the CRC word inserted in the first 16 bits of the sync word time to detect if an error occurred within the 480 bit data block.

10.3.1 Gate and Counter Logic

The Counter is used as described in the Delay paragraph to generate the memory addresses. The Gate logic, see Figure 10.2, and Figure 10.3, generates a series of 16 bit gates similar to the CRC Generator in section VI. These gates are used to latch the error Flag and reset the CRC detector. A signal from the Error Corrector PWA called the Serial Flag is used to determine which channels are active in the ECC process, all other channels are reset continuously and do not produce any Error Flags.
10.3.2 Flag Detection

Error Flags are generated on a per channel basis as shown in Figure 10.4. There are two flag outputs, one goes to the Error Corrector PWA and the other is a monitor signal.

The data is sent thru a CRC encoder chip, as it was on the CRC Generator card, as shown in Figure 10.5. At the end of the data block the 16 bit CRC word is also allowed to enter the encoder chip. If there are no errors the shift register stages will all be zeroes and the output of the CRC encoder will be a zero as shown in Figure 10.6. If there was an error one or more of the shift register stages will not be zero and the output will be a one. The output (one or zero) is latched during the last bit of the CRC word (the only time it is valid), delayed for the 16 bits of the sync word, for a total delay of 32 bits after the last data bit and then held for 480 bits until the next CRC word begins.

Thus after a block containing error(s) is recognized a Flag is generated which is delayed by 18 bits, held for 480 data bits, and reset for 16 bits for a total of 512 bits. Since the data is delayed for 512 bits, the data and flag will occur at the same time.

10.4 M48 Gate.

The gate signal (active low) for the customer 48 bit data block in the Master channel is also generated on this card, as shown in Figure 10.7. It occurs from the middle of the Channel 14 sync time to the end of the Channel 15 sync time. It goes low slightly after the positive edge of the parallel clock, thus the negative or positive edge of the parallel clock occurring after the Gate has gone low can be used to load the M48 data from the Master Channel into registers in the customers equipment.
11.1 Description.

The Error Corrector and Data Reinsertion PWA, shown in Figure 11.1, has three main functions, to determine if one and only one track has errors on it, to correct the errors if that is true, and to recombine the data in the Master Channel with the respective data channels.

11.1.1 Channel Select

Channel selection for error correction can be selected by either the DIP switches on the front of the PWA or by the optional Auto Channel Select PWA. In the manual mode, see Figure 11.2, the data channels are selected by the DIP switches to match the recorded format. The Parity Channel is automatically determined to be channel 12 or 13 in a manner similar to the CRC Generator. If the format selected does not match the recorded format the Error Correction will probably not work and may in fact be detrimental, since the recorded Parity will be different from the Parity check done in reproduce. After blanking the CRC and Sync word (which were not used in the recorded parity calculation), each channel selected will route its data to the Parity test circuitry.

The Auto Channel Select PWA can select Auto or Manual Mode. In Auto mode the base of the select transistor is grounded which opens the DIP switches. The format read from the tape is then used to select the active channels via the Channel Select inputs.

11.1.1.1 Serial Flag

The Serial Flag (SF) is a signal which consists of a series of 32 bit long signals indicating in a serial fashion which channels are selected. Since the Parity channel was created prior to Sync Insertion, the data which was moved from each Data Channel into the Master Channel must be included in the Parity check. The Serial Flag is used to gate the Master channel data so that data blocks from channels in the ECC format will be included in the Parity check, and all other blocks will be excluded. The Serial Flag is also used by the Delay/Detector PWA to clear the Error Flag circuit on the active channels, See Section X.
11.2 Flag Arbitration Logic.

The Flag signals from the Error Detector PWA are sent to an analog comparator circuit which determines how many flags are present. Each flag has a weight of proportional to the number of flags present as shown in Figure 11.3.

A FLAG ONE is generated by the first comparator which has a reference of 0.75 units and will change state if one or more Flags are present (1.0 or more units) the ONE Parity channel system along with the FLAG ONE from the other DPB to indicate two channels in error (one in each Bay), which creates a FLAG TWO. For Two Parity channel systems this signal is not used.

A FLAG TWO signal is generated by the second comparator which has a reference of 1.25 units. If 2 or more Flags are present (1.5 units or more) the comparator changes state and the Error Correction is disabled. This signal is also sent to the other DPB for use in ONE Parity Channel systems. This is required as the system is limited to correcting one and only one channel with errors (see description of Parity checking). The TWO/ONE switch selects how many Parity Channels are in use. The A/B switch is used to program whether this card is in the A or B DPB. Since the Parity channel in a ONE Parity system is in the A Bay the B Bay parity channel must not be selected. In Two Parity channel systems the A/B switch has no effect.

11.3 Data Correction/Reinsertion

Data Correction and Reinsertion is performed on a per channel basis, as shown in Figure 11.4.

11.3.1 Error Correction

The Error Correction circuit does a parity check of all of the data channels, portions of the Master Channel and the Parity Channel. If no error exists the check is ok and no further action is taken. If an odd number of channels have an error the parity checking circuit has an error output. This signal is sent to the correction logic where a decision is made whether or not correction should take place. If only one channel has a FLAG the data in that channel is corrected by inverting its state, if two or more channels have errors the FLAG TWO signal will inhibit the correction.

11.3.2 Sync Blanking.

On the record side the Parity channel was generated before sync words or the CRC words were added to each channel and before the Master Channel was generated done. In addition the data during these periods was part of the parity, so the Master Channel (which now contains the 32 bit blocks removed from the Data Channels) must be included in the parity check (see the description of Serial Flag). If the check is done after data reinsertion, the Error Flag from the Master channel would have to be distributed as well as the data which would severely complicate the logic required.
11.3.3 Parity Checking.

The parity generation in this system is called even parity, where the parity channel contains a one or a zero such that the total number of ones in all the channels (including the parity channel) is an even number (0, 2, 4, 6, 8 etc). If an even parity check is then made of all of the channels including the parity channel, the result will always be zero. If an error exists in one channel the result will be one. However, if two channels have simultaneous errors the result will again be zero as if no error existed. The Error Detection PWA only detects error(s) somewhere in a 480 bit block thus if one channel has a block with error(s) overlapping a block with errors in another channel neither can be corrected during the time the blocks (and corresponding Flags) overlap.

In a one parity channel system, the Parity result (PAR-ERR-OUT) of each Corrector is sent to the other Corrector (PAR-ERR-IN) and a final calculation is made independently on each Error Corrector PWA. This reduces the time required to make the calculation.

11.3.4 Data Reinsertion.

Reinsertion of the data from the Master channel into the various Data channels is accomplished in a similar manner to the standard HBR system except that it is done on this PWA instead of the individual Slave Deskew cards.

11.4 Parity Retest.

After the Data channels are corrected and reinserted a parity check is again performed to verify the data. The Parity result is provided on an output pin.

11.5 M48 Data

The master channel data (DATA-CORR-M) is sent to an output connector where, along with a 48 bit gate (from the Error Detector and Delay PWA) the customer can select his data out of the Master channel with the M48-GATE and parallel clock. The M48 data cells are aligned with the negative going edges of the Parallel clock, thus the first data bit is valid at the first positive going edge of the Parallel after the the M48 GATE goes low.
Section XII

AUTO CHANNEL SELECT PWA

Part No. 1262013
Schematic No. 1262010

12.1 Description

The Auto Channel Select PWA contains a Slave Deskew for Channel 13 and the logic for decoding the channel select information inserted in the first half of the Channel 14 sync time in the Master Channel. A toggle switch on the front of the PWA selects AUTO(up) or MANUAL(down) operation. A series of LED's indicate the ECC active channels.

12.1.1 Compatibility

When the Auto Channel Select feature is not used a Slave Deskew (ECC) PWA may be inserted in this card location to perform the Channel 13 deskew function.

12.2 Auto Channel Select

The first 4 bits of the channel 14 sync period in the Master channel contain information relative to the channels active in ECC (ie. used to create the parity channel) when the tape was recorded. They are formatted in blocks as a sync bit and 3 channel select bits. Since there are a maximum of 12 customer data channels it takes 4 blocks to completely specify the format. In addition, the 4 blocks are repeated with inverted information to decrease the possibility of decoding an incorrect format. The channel select bits are a one for a selected channel when the sync bit is a zero and a zero for a selected channel when the sync bit is a one. Thus it takes 8 blocks to complete the channel select information.

The Channel 14 GATE starts a 4 bit shift register. See Figure 12.1 and Figure 12.2. The first bit (sync) polarity is detected and sets an exclusive-or gate to pass or invert the following data bits. The sync bit is also sent to a latch which detects a change in the sync bit from a one to a zero. This point is the beginning of an 8 block segment of channel select information. At this point the data from the previous 8 blocks is transferred to the output latches (if there were no errors) and the error detector is reset.

The 3 data bits are shifted into a register and the register is held until the next block. After 4 blocks the first bit will be at the end of the register. When the next block (number 5) comes in the bit at the end of the shift register is compared with the incoming bit. If they do not agree, a latch is set. This process continues for the next 12 data bits (4 blocks) and if any of the 12 bits do not agree the error latch will prevent the data from being transferred to the output latch.
The output latches drive open collector inverters which illuminate LED's on the front edge of the PWA and drive the channel select circuitry on the Error Corrector PWA. If the toggle switch is in the Manual position (down) the LED's are held off and the normal manual selection switches on the Error Corrector PWA are enabled. In the Auto position the manual selection switches are disabled and can be left in any position.
Fig. 3.1
Fig. 3.2

28 CHANNEL INTERCONNECT
## Diagram Description

### Components and Connections

- **Data S/P Converter**: Converts data from serial to parallel or vice versa.
- **SIP Converter**: Converts SIP (Source Interchange Format) to parallel or serial.
- **CRC Generator-Inserter**: Adds cyclic redundancy check (CRC) to data.
- **Error Detector-Data Delay**: Detects errors and delays data accordingly.
- **Flag Monitor**: Monitors flags in the data stream.
- **Error Corrector-Data Reinsertion**: Corrects errors and reinserts data.
- **Co Serial Clock Delay (Generator)**: Delays the clock signal for serial communication.
- **Spare**: Additional components for redundancy or future expansion.

### Key Elements

- **Aux In**: Auxiliary input for data processing.
- **DATA FILTER**: Filters data for enhanced quality.
- **DATA ENCODER**: Encodes data for transmission.
- **CRC Generator**: Generates cyclic redundancy check for error detection.
- **Encoder**: Converts data into a format suitable for transmission.

### Connections and Signals

- **40, 41, 42, 43, 44, 45**: Connections for various data signals and signals.
- **J1 to J45**: Jumper connections for signal routing.
- **3/4**: Jumper setting for signal selection.
- **5/6**: Jumper setting for signal selection.

### Specific Jumper Settings

- **J1**: Serial or Parallel Select
- **J2**: Data S/P Select
- **J3**: Data S/P Select
- **J4**: Data S/P Select
- **J5**: Data S/P Select

### Notes

- **Spare Jumper Settings**:Available for future use or redundancy.
- **Jumper Positions**: 3/4, 5/6, 11/12 for configuring data signals.
XTAL-REF/QX

EXT-REF-TO-TSPT

CLK-SER-XTAL/NRZ

TO B-BAY

234-DATA.OUT-XX J40

234-DATA.IN-XX J43

SERIAL TO PARALLEL CONVERTER J1

DATA-SPC-XX J39

DATA-PAR-IN-XX J38

SERIAL OR PARALLEL SELECT J2

DATA-SPS-XX J37

DATA-SPS-XX J34

CAL NO 1 J3

DATA-CALL-XX

SYNC INSERTER J4

DATA-SI-XX

CRC GENERATOR/INSERTER J5

DATA-CRC-XX

ENCODER NO 1 J7

DATA-ENC-XX

DATA-ENC-XX J30

DATA-ENC-CAL-XX J31

TO BIT SYNC BAY

FILTER J8

DATA-FILT-XX J29

TO TRANSPORT HEAD DRIVERS

DPB RECORD
Fig. 5.2

SYNC INSERTER TIMING
AUTOMATIC CHANNEL SELECT - M48

Fig. 5.5
CRC GENERATION AND INSERTION

Fig. 6.3
-29-
Fig. 6.3A
CRC TIMING
Fig. 10.2
ERROR FLAG LOGIC

Fig. 10.5
42
ERROR FLAG TIMING
CHANNEL SELECT LOGIC
FLAG ARBITRATION
Fig. 11.4
AUTO CHANNEL SELECT LOGIC
SEE SHEET ONE