Workstation Architecture
by R. Belleville, Mgr. Advanced Design

1. Workstation Requirements and Goals

2. Discussion of alternative approaches

3. The concept of a synchronous multi-tasking processor

4. The Dandelion Workstation

5. The Cub Workstation
Star Workstation Constraints

1. Support large format display (1024x808)
2. Support Ethernet communication
3. Support high performance rigid disks
4. Support Low Speed Electronic Printer
5. Support Mesa Emulation
6. Support a number of slow devices
Star Workstation Design Alternatives

1. Commercial LSI Microprocessors

2. Bus-Organized Distributed Systems

3. Custom LSI

4. Synchronous Multi-Tasking Microprocessors
Bus Organized Workstation Microprocessor
Conventional Processor Organization

System Bus

Bus Interface Logic
Buffering
High Speed Device Interface
Peripheral
(Rigid Disk)

Bus Interface Logic
Buffering
High Speed Device Interface
Peripheral
(Ethernet)

Bus Interface Logic
Buffering
High Speed Device Interface
Peripheral
(ETC)

Multi-Tasking Processor

Micro-Coded Device Driver
Micro-Coded Device Driver
Micro-Coded Device Driver
CPU
Main Memory

High Speed Device Interface
Peripheral
(Rigid Disk)

High Speed Device Interface
Peripheral
(Ethernet)

High Speed Device Interface
Peripheral
(ETC)
What Effect Micro-Instructions have on Microprocessors

Peripheral Input and Output Registers

Many Different Registers

Main Memory

Memory Data

Memory Address

Very High Speed Registers

Temporary Data

Source Selection Logic

Source Field

Operation Field

Destination Selection Logic

Destination Field

Next Instruction Address

Arithmetic and Logical Operations

Micro-Instruction
Micro-Instruction Sequencing In a Multi-Tasking Microprocessor

Control Store

Task 0 Micro-Instructions

... 

Task 1 Micro-Instructions

... 

Task 2 Micro-Instructions

... 

Task 3 Micro-Instructions

... 

Next Micro-Instruction Pending Table

Task Selection

0 1 3 2

Micro-Instructions Feed to Microprocessor

Micro-Sequence.sil
A Synchronous Multi-Tasking Microprocessor with 4 Clicks/Round

Is the Display Waiting for Service?
- Yes
  - Micro-Instruction #1: Display Click
  - Micro-Instruction #2: Main Memory Cycle
  - Micro-Instruction #3

Is the Ethernet Waiting for Service?
- Yes
  - Micro-Instruction #1: Xerox Wire Click
  - Micro-Instruction #2: Main Memory Cycle
  - Micro-Instruction #3

Is the Rigid Disk Waiting for Service?
- Yes
  - Micro-Instruction #1: Rigid Disk Click
  - Micro-Instruction #2: Main Memory Cycle
  - Micro-Instruction #3

Is the Low-Speed I/O System Waiting for Service?
- Yes
  - Micro-Instruction #1: Low-Speed I/O Click
  - Micro-Instruction #2: Main Memory Cycle
  - Micro-Instruction #3

On to the start of the next round
The Dandelion System

Central Processor

- Processor (2901 based)
  - Mesa Emulator
  - Ethernet II and controller
    - Rigid Disk and controller
    - LSEP controller (option)

Memory System

- Memory (128K by 22)
- Memory (64K by 22)

Input/Output Processor

- Processor (8085 based)
  - Floppy Disk
  - Keyboard
  - Pointer
  - Speaker
  - Character
  - Printer
  - Maintenance Panel
  - Time of Day Clock
  - RS-232-C (option)

Large Format Display

Display Controller

Monitor

February 26, 1980
Dandelion-Block.sil
RLB
Workstation Configuration
(Note: This drawing is subject to change.)

Power Supply → AC Power Filter → Cooling

DC Power Distribution

AC Power Distribution

Slot 0 - Storage
128K Storage (22 bits wide) (16K memory parts) necessary until 64K LSI memory parts become available

Slot 1 - Memory and Memory Control
64K Storage (22 bits wide) (16K memory parts) Single bit error correction, Double bit detection Memory Controller

Slot 2 - High Speed I/O (Type I)
System Clocks
Display Controller
SA 1000/4000/4100 series rigid disk controller
Note: Type II has controller for large rigid disks such as Hunter in place of the Shugart controller.

Slot 3 - CPU
ALU
Control Store

Slot 4 - IOP
8085 MPU, RAM, and PROM
CPU control
Writable control store interface
IBM Floppy Disk Controller
Keyboard and Pointer Controllers
Speaker
Time of day clock
RS-232C (DCE Interface) for character printer
Maintenance Panel, Reset, and Alt. Boot Buttons

Slot 5 - Options (Type I)
Raven controller
Ethernet II Local Area Network controller
Communication RS-232C (DTE Interface)
RS-366 (Auto Dial)

Shugart SA1002/4
Rigid Disk Drive

Shugart SA800 or SA850
Floppy Disk Drive

17 Inch Monitor
Connector Panel for connection to peripherals and options

SA 4XXX Disk Drive (separate cabinet)
Keyboard/Ptr/Spkr
Char. Printer
LSEP (Raven)
Ethernet Tranceiver
RS-232-C (DTE)
RS-366

Maintenance Panel

AC Input

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Logic-Configuration.Sil RLB
Dandelion Chip Count

1. Memory and Memory Control
   Ram 88, Other 70, Total 158

2. 128K Storage
   Ram 176, Other 26, Total 202

3. Central Processor
   Control store 49, Other 118, Total 167

4. Input/Output Processor
   Ram 32, Prom 4, Floppy 27, Kbd 12, Other 88, Total 163

5. High Speed I/O
   Clocks 19, Display 56, Disk 65, Total 140

6. Option Type I
   RS232 & LSEP 39, Ethernet (est) 55, Total 94
Workstation Development Environment

Logic Drawings

Source Files

Alto Mesa Based Software Tools
- 8085 Assembler/Binder
- MASS - Dandelion Central Processor MicroAssembler
- Burdock - "Front Panel"/Debugger
- Logic Analyser Interface
- Design Automation

Alto

Umbilical Connection

DandeLion Engineering Model

DandeLion Peripherals
Workstation Design's
Tasks

Bob Garner ALU Design, Emulator microcode
Don Charnley

Ron Crane Memory system, Display controller, related microcode

Dan Davies Disk Controllers, Xerox Wire Controller
Roy Ogus Xerox Wire microcode

Dick Snow Development tools environment
Don Charnley Microassembler
Jim Frandeen Micorassembler

Pat Olmstead LSEP interface microcode, printing application w/ Dandelion
Pitts Jarvis LSEP controller

Roy Ogus IOP

Neil Hansen Model building, logics
Jim Cucinitti

Jim Peterson Diagnostics and Field Service

Bob Belleville Everything else
The Dandelion Empire

TPM                           Hal Lazar/ Hans Scharmann          EL Segundo
Industrial Design            Robin Kincaid/ Claude Hutcheson      Dallas
Package                      Dick Hanson & Allen Bell              Dallas
Power Supply                  Avi Kandola                          EL Segundo
PWBA Manufacture             ED                                    EL Segundo
Component Qual               ED                                    EL Segundo
Other Engineering            ED                                    EL Segundo
Support
Manufacture                  Bill Powers                           Dallas
Field Service                Art Johnson                          EL Segundo
LSEP                          TPM                                  EL Segundo
                              John Michell                          Webster
                              Joe Hruchak et al                     Webster
Engine                       John Forester et al                  Webster

I am sure there are more I haven’t found yet.
**Workstation Design's Tasks**

<table>
<thead>
<tr>
<th>Name</th>
<th>Task</th>
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</thead>
<tbody>
<tr>
<td>Tom Chang</td>
<td>Ethernet support</td>
</tr>
<tr>
<td>Don Charnley</td>
<td>Microassembler, Design review</td>
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<tr>
<td>Jim Cucinitti</td>
<td>Memory system mechanization, Tech. Support</td>
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<tr>
<td>Ron Crane</td>
<td>Memory system, Display controller, related microcode</td>
</tr>
<tr>
<td>Dan Davies</td>
<td>Disk Controllers</td>
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<tr>
<td>Bob Garner</td>
<td>ALU Design, Emulator microcode, Ethernet controller</td>
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<tr>
<td>Neil Hansen</td>
<td>Model building, Tech. Support</td>
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<tr>
<td>Pitts Jarvis</td>
<td>Development tools (Burdock), LSEP controller</td>
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<tr>
<td>Roy Ogus</td>
<td>IOP, IOP software, Maintenance panel</td>
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<tr>
<td>Pat Olmstead</td>
<td>LSEP interface microcode, printing application w/ Dandelion</td>
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<tr>
<td>Dick Snow</td>
<td>Development tools environment</td>
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<tr>
<td>Ken Yamanaka</td>
<td>RS-232 controller</td>
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<tr>
<td>Bob Belleville</td>
<td>Everything else</td>
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</tbody>
</table>

**Kaz Mats**  

**Purchasing / Expedite**

*wd-tasks.sil
August 7, 1980*
<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Task Description</th>
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<tbody>
<tr>
<td>1978</td>
<td>4th Quarter</td>
<td>October Study</td>
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</table>
| 1979 | 1st Quarter | February Study  
Begin design |
|      | 2nd Quarter | IOP up |
|      | 3rd Quarter | CP up  
Tools up |
|      | 4th Quarter | Display up  
Microcode based example programs |
| 1980 | 1st Quarter | Disks up  
Logic design to mechanization |
|      | 2nd Quarter | Mesa up  
Some first etch under test |
|      | 3rd Quarter | Pilot up  
3 ElMs up |
|      | 4th Quarter | PPMs (6)  
Servers to field (2?) |
| 1981 | 1st Quarter | 200 machines |
|      | 2nd Quarter | |
|      | 3rd Quarter | 1000 - to 1800 machines |
|      | 4th Quarter | |
1. Minimum hardware
2. Microcode to simulate the "Alto/Orbit"
3. Use whole machine during printing
4. Very limited bandwidth to the printer

Dandelion/LSEP System Concept

- Star Document
  - Not real time
  - Mesa based programs
  - Conversion in the workstation

- OIS Print File
  - Not real time
  - Mesa based programs
  - Conversion in the printer server

- Bandlist File
  - Must be real time
  - Mesa with microcode assist
  - Conversion in the printer server

- Band Buffers
  - Must be real time
  - Microcode with Mesa based engine control
  - Conversion in the printer server

- Image on paper
All are ECL balanced pairs
Receivers are MC10125
Transmitters are MC10124

MSEP should be the same; however, a Page Sync may have to be added to insure page registration.