Test Shift Reg. (40-bit)

Note: Load: if Input Reg. with address > 4
Shift: if Input Reg. with address < 4
OMeF
LdCR
Register 0

Ed eClk2
LdStart
Register 1

TP031
ClkStart'
Registers 3, 10-13

elkCR'

Register 2

ClkSlarl'
Registers 10-13

ClkIAR'

Registers 10-13

ClkIAR'

Register 3

ClkIAR'

Register 4

ClkIAR'

Register 5

ClkIAR'

Register 6

ClkIAR'

Register 7

LdCurOCR

ClkCurOCR'

EvenLine

WriteOddBuf'

Registers 10-13

WriteEvenBuf'

Registers 10-13

LdCur1CR

ClkCur1CR'

RamCik1

CurOWE'

Register 8

Cur1WE'

Register 9

RamCik1

Diagnostic Reg. Tn-State

Terminal Diagnostic
Input Shift Mux
for Buffer 0

Output

for Buffer 2

Output

for Buffer 1

Output

for Buffer 3

Output

Note: Complement Qaddr 6,7 lines used for better load sharing
See page 17 for terminators
Note: 14-Pin crystal should be install in this 20-pin platform as follows

Crystal PLAT
Pin 1: N. C. P4
7: GND P10
8: Output P11
14: +V dc P17

ID Modifier must have even number of p

Note: These platforms are shown as 20 pin units. They are actually 16 pin r
with pin 8 of the network inserted into pin 9 of the 20-pin pattern.
They are shown as 20 pins so that ROUTE will not try to cut any traces on the
Test Clips:

- Transmit
- OMnP
- IMbP
- T1Msg
- T2Msg
- T3Msg
- Wake1
- Wake2
- Wake3
- Wake4
- SendControl
- WriteorCont'
- SendRequest
- WakeRequest

MyTask
- Switch
- Click
- ClickStart'
- ClickEnd'
- BankTerminal
- WriteOddBuf'
- WriteEvenBuf'
- GND

Switchoff
- Buffer
- Out
- GND

Bulder
- Bul2B1
- Bul2B2
- Bul2B3
- GND

Filler Caps for ECL chips:

These capacitors mount between pins 2 and 19 of a 20 pin pattern due to the offset

- GND
- VEECAP
- VEE

Spare Positions (for Multiwire):

- FPLAT
- GND

- FPLAT
- GND

- FPLAT
- GND

- FPLAT
- GND

- FPLAT
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- FPLAT
- GND
Minor changes to logic found necessary during checkout.
Re-layout to eliminate crossover of connections to I/O connectors.
Made all I/O connectors male.
Added hardware cursor to channels 1 & 2.
All logic pages changed and renumbered.

Synchronized BckGnd0 and BckGnd1 with Switch, Log. Dwg. p. 7.
Added SendControl to Background control to maintain proper polarity of Control signals.
Changed control gate for Output shift register from S10 to S02.
Log. Dwg. p. 6, 12, & 16.
Changed Blank function in Control register to Unblank so that Rest results in blanked display.

Page 05; OAddr4' Input changed to OAddr4.0MeF and S10 gate (b12c) utilized for that.
Page 07; Control Register, PPUnblank changed to PPBlank, EnOsc changed to Allow WU, S74
(c15a) deleted
Sync CR - PUnblank changed to PBlank
S00 (e18d) changed to S02 (d56). ControlPhase' Input changed to ControlPhase.
Inverter (f15f) used instead of S02 (d56). New wire EnblCurs' added.

Page 13; SendControl' changed to EnblCurs' on the input of S10 (b12e) and load inputs of
S163 (b11 and a11). Typos corrected - Output control inputs on b13 and a13
changed from Hi to GND

Page 14; SendControl' changed to EnblCurs' on the input of S10 (b12b) and load inputs of
S163 (d11 and c11). Typos corrected - Output control inputs on d13 and c13
changed from Hi to GND

Page 15; SendControl' input on S00 (c12) changed to DropClockB. SendControl, and S00
Gate added (e18d)

Page 16; NC1k gate input changed from ClkB to ClkB'. EnOsc input on S51 changed to Allow WU
DropClockB' signal added on the output of S74 (f13b). S10 gate (d4b) added to produce
CurXC1k'. Corrected typo - Out0.09 changed to Out0.15 on the input os S51

Page 17; Pullup and pulldown resistors added to the Crystal Plat (also in UTVFCSplat.sil)
Added test chip S241 in loc. c8. Its symbols are scattered on several pages. Added test points
on most pages.

Page 19; Corrected error made in adding the test points on page 9 and 10.
Changed EdgeClock2' to EdgeClock1' (Etch layout related) on p.2. Changed S166 to LS166 on page 4. Cosmetics on p.17.

Changes for revision Gb (7/18/80 - CPT)

1) Connected pin 15 of all 4 terminal connectors to ground (p 16).
2) Created latched signal MyStrobe' (pp. 3).
Note: The I/O connector area is loaded with 4 15pin MALE D-series connectors.
Note: All platforms except A have pin 8 of the platform in pin 9 of the pattern.
Note REVERSAL of all ECL Chips (MC124, MC125)

---

20pins: A
16pins: B
14pins: C
22pins: D
24 pins: E

---

Note: The short vertical lines indicate filter capacitor locations.
(103 total)

Broken vertical lines
indicate VEE filter caps
for ECL chips. These are mounted
from pin 2 or pin 19 of the 20 pin pattern.
(7 total)
Platform e1 (oscillator):

```
+---------+  +---+  +---+  +---+  +---+  +---+
|         |  |   |  |   |  |   |  |   |
|        1K|  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
|         |  |   |  |   |  |   |  |   |
```

Note: The oscillator is mounted on the platform as follows:

<table>
<thead>
<tr>
<th>Oscillator Pin number</th>
<th>Platform Pin number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td>14</td>
<td>15</td>
</tr>
</tbody>
</table>

Oscillator is Motorola K1100A series

Note: ID.08' - ID.12' are wired to Hi (pin 3) or Gnd (pin 8) depending on the oscillator frequency as follows:

<table>
<thead>
<tr>
<th>Oscillator f: 50mhz</th>
<th>20mhz</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID.08' (pin 4)</td>
<td>Hi</td>
</tr>
<tr>
<td>ID.09' (pin 6)</td>
<td>Hi</td>
</tr>
<tr>
<td>ID.10' (pin 6)</td>
<td>Hi</td>
</tr>
<tr>
<td>ID.11' (pin 11)</td>
<td>Gnd</td>
</tr>
<tr>
<td>ID.12' (pin 7)</td>
<td>Gnd</td>
</tr>
</tbody>
</table>

Platforms b1, c1, g1, h1

Xerox P/N 703W11691 (15 resistors) is acceptable
All resistors 220 ohm, 1/4 w.

Platform d1:

Xerox P/N 703W00891 (8 resistors) is acceptable substitute
All resistors 1000 ohm 1/4 or 1/8 watt, 10%