Block 0&1 bits 0-15

BlockSel1 2  LS175  2 LS175  4 LS175  6 LS175  7 LS175  8 LS175  10 LS175  12 LS175  14 LS175  16 LS175  17 LS175  18 LS175  19 LS175  20 LS175  21 LS175  22 LS175  23 LS175  24 LS175  25 LS175  26 LS175  27 LS175  28 LS175  29 LS175  30 LS175  31

Clock 3  LoadD 5  LoadW 4  v89b 6  LoadWO 9

typ of 4 25509
see page 14 for others
Loads on 2nd word of transport loads on 1st word and again on 4th word if BlockSel0 and again on 3rd word if BlockSel0.

Block Sel 0

Loads on 2nd word of transport loads on 1st word and again on 4th word if BlockSel0 and again on 3rd word if BlockSel0.

Block Sel 0

Loads on 2nd word of transport loads on 1st word and again on 4th word if BlockSel0 and again on 3rd word if BlockSel0.

Block Sel 0

Loads on 2nd word of transport loads on 1st word and again on 4th word if BlockSel0 and again on 3rd word if BlockSel0.

Block Sel 0

Loads on 2nd word of transport loads on 1st word and again on 4th word if BlockSel0 and again on 3rd word if BlockSel0.

Block Sel 0

Loads on 2nd word of transport loads on 1st word and again on 4th word if BlockSel0 and again on 3rd word if BlockSel0.
### Bit Locations

<table>
<thead>
<tr>
<th>Block</th>
<th>Bits 0-3</th>
<th>Bank</th>
<th>Bank</th>
<th>Bank</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0-3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>0-3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0-3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>255</td>
<td>32-63</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### Load and Storage

- **Load**: 6 LoadW3 9 S10 PUP3
- **Clock**: 3
- **Storage**: 182 bits 48-63

**StorE0ut**: 15
- 04: Bank1Dout.04 91
- 11: Bank1Dout.11 91
- 14: Bank1Dout.14 91
- 15: Bank1Dout.15 91

**StorEcOut**: 4
- 04: Bank2Dout.04 91
- 11: Bank2Dout.11 91
- 14: Bank2Dout.14 91
- 15: Bank2Dout.15 91

**StorEcOut**: 12
- 04: Bank2Dout.04 91
- 11: Bank2Dout.11 91
- 14: Bank2Dout.14 91
- 15: Bank2Dout.15 91

**StorEcOut**: 16
- 04: Bank2Dout.04 91
- 11: Bank2Dout.11 91
- 14: Bank2Dout.14 91
- 15: Bank2Dout.15 91

**StorEcOut**: 22
- 04: Bank2Dout.04 91
- 11: Bank2Dout.11 91
- 14: Bank2Dout.14 91
- 15: Bank2Dout.15 91

**StorEcOut**: 255
- 04: Bank2Dout.04 91
- 11: Bank2Dout.11 91
- 14: Bank2Dout.14 91
- 15: Bank2Dout.15 91

**Enable for**: Other

### Note

- Loads on 4th word of transport
- Clocked same time as last Data Word
- See page 14 for others

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**Diagrams**

- [Clock Diagram](#)
- [Load and Storage Diagram](#)
XEROX E0D
Project D0
Storage Card Bank 2, Least Significant Bits
File D0stor05.sil
Designer Rosen
Rev B Date 1/26/80 Page 05

Clock 11
LoadW'10
LoadD'0

Storage Card File Designer Rev Date Page
Bank 2, Least Significant Bits

BlockSel0a 1

Clock 11
LoadW'10
LoadD'0

S10 PUP3

Loads on 3rd word of transport typ of 4 25S09

see page 14 for others
Shown for completeness only
Not used on 96k storage card

Jumper for I/O Boards

Clock

LoadW

LoadD

Select Card, RAS, CAS

File Designer

Rev Date 9/8/78 Page 07
Part of EC input register, which is shared by banks 0 and 2.