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*Testability control to be added for etch module.*
Testability control to be added for each module.
CRC-16 $X^{16} + X^{15} + X^2 + 1$

CRC Polynomial

**FOR TESTABILITY**

ECCGenerator Polynomials:
- Write - $X^{*32} + X^{*23} + X^{*21} + X^{*11} + X^{*2} + 1$
- Read - $X^{*11} + X^{*2} + 1$; and $X^{*21} + 1$

* Testability control to be added for etch module.
Testability control to be added for etch module.
* Testability control to be added for etch module.

(Clk = ByteClk)
Testability control to be added for etch module.
* Testability control to be added for etch module.
Note: Splats A, B, and C are 16 pin platforms centered in the 20-pin pattern.
Rev A: Initial Release

Changed DevSelOK counter load control so that Dr/HdRegLo loads counter only if DrSel[0:1] is changed. Log. Dwg. p. 14.
Added Seek counter at 0 to produce seek step just when DevOpReg is loaded with Seek bit (GntDlOs). Causes SeqAdr[0:3] to be 0000 when Seek is true. Inhibits Wake-up until Seek has been generated. Log. Dwg. p. 2, 3, 4, 5, & 15.
Deleted Wake PROM and Counter; removed XferLate from IOAttn; deleted Flow Control
Counter added Data Wake up/down counter; added 3 wake count to IOAttn. Log. Dwg. p. 3 & 13.
Numerous minor changes in mechanization as a result of above. Log. Dwg. p. all.

Added RateError FF. Log. Dwg. p. 3.
Added DataReq to hold term for WakeReqF to override IOSrofe reset. Log. Dwg. p. 3.
Added term to Wake Counter enable to prevent incrementing beyond max, or decrementing below 0. Log. Dwg. p. 3.
Adds RateError to Status Parity Generator. Log. Dwg. p. 16.
Changes RateError qualifier to DataWrt. Log. Dwg. p. 3.
Moved $280 from if4 to if5. Log. Dwg. p. 15.

Deleted Abort from Wake Request logic. Log. Dwg. p. 3.
Changed data error check to look at Syndrome.00 during ECCCheck. Log. Dwg. p. 11.
Changed latch of NonComp FF to insure at least 2 DevClk times on. Log. Dwg. p. 9.
Added SectorMarkSP "and" ReadGate to Abort set term to indicate missing Sync pattern. Log. Dwg. p. 12.

Rev E: Added SeqAdrXferS' to BufSeqEnbl to insure transfer of Sequence Address even if IMEF or OMEF is true. Log. Dwg. p. 6 & 7.
Changed CRC control from DataTime to ECCShift. Log. Dwg. p. 11.
Added detection for ServiceLate to indicate Header and Label data not loaded into buffer by Header SyncFound. ServiceLate added as Idata.05 in Status word. Log. Dwg. p. 12 & 16.
Changes Reset functions from single Output function with data specified functions to specific Output functions for General Reset and Error Reset to eliminate gate noise on direct reset lines. Log. Dwg. p. 2.
Added synchronization of Abort with DevClk (AbortISD) to prevent erroneous setting of Sequencer Address Registers. Log. Dwg. p. 4 & 12.
Added RateErrorPossible to Buffer Control Sequencer to define actual time when rateerror can occur. Decreased RateError wake-up count from 3 to 2 to insure RateError detection if delay in memory pipe and only 20 words initially loaded in RDC buffer. Log. Dwg. p. 3 & 6.
REQUIRES REV B PROM!!!

Rev F: Replaced Ht in Status Word with ServiceLate' in order to maintain correct parity. Log. Dwg. p. 12 & 16.
Added PrimOData output function to MemUsesBuf to allow firmware to Prime Idata without parity error Log. Dwg. p. 2, 3, 4, & 15.
Changed AllowWake and WakeoFqF control to allow firmware control of AllowWake. Added WakeRequest to IDWord bit 12 for firmware test. This is to facilitate "booting" from the disk. Log. Dwg. p. 2, 3, 4, & 15.

Rev G: Changed AllowWake so that ODato.04 = 1 sets AllowWake to comply with unpublished convention of setting output registers to zero causing initialization of controllers. Log. Dwg. p. 4.

Rev Ga: generated from Rev G on 4/11/79 by CPT.

1) Redrew splats at d1, e1, f1 as FPLATS to avoid ROUTE trace cuts (pg 17).
2) Added spare positions at g3, h9, i9, e17, b10, c10 (pg 17).
Rev Ga: generated from Rev G on 4/11/79 by CPT.
1) Redrew splats at d1, e1, f1 as FPLATS to avoid ROUTE trace cuts (pg 17).
2) Added spare positions at g3, h9, i9, e17, b10, c10 (pg 17).

Rev Gb: 9/3/79 - CPT
This change is a manual addition to the revision Ga MultiWire board.
1) Lift the following pins:
   a15.12
   c16.9
   d10.6
   i13.10
   a13.15
2) Add an 5174 IC in position i9, and wire i9.16 to Vcc.
3) Add the following wires:
   a15.12 to i16.9 (DevSelOK, pg 2,16)
   c16.9 to a15.11 (RstAbrt/Err', pg 3,2)
   d10.6 to a15.9 (ClrDevOpS', pg 12)
   a15.8 to h13.1 (ClrOp', pg 4,7 - new signal name)
   a15.10 to a15.5 (Run, pg 2,12)
   i13.10 to 10.4 (Unnamed signal - was InhHdrAbrt, pg 4)
   h13.7 to i9.3 (Unnamed signal - was VerifyLabel, pg 4)
   i11.0 to i9.3 (OpRegClk', pg 4)
   i11.0 to i9.1 (ResetAbrt/Err', pg 4)
   i9.5 to a13.1 (InhHdrAbrt, pg 4,12)
   i9.2 to a13.15 (VerifyLabel, pg 4,12)
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Note: The short vertical lines indicate filter capacitor locations.