Note: Storage card inverts data and check bits.

Note: GenPhase0 \rightarrow GenSyn0,1,2,3,X = (pullups on page 12)
Note: Storage card inverts data and check bits

Note: Balance of checker is on pg. 6
Note: Storage card inverts data and check bits.
Type classifies references according to the types of faults they can cause:
Non-memory/Fetch/Store
References are also classified as to whether or not they use a pipe slot.

Note: ALUF[0:3] is reference type in memory references.
During PStore12, this
EdgeClock line selects data from storage or data from R. MC1 and MC2 are both active.
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Note: Pins marked with * have 470 ohm pullup resistors to +5v.

20 pins: A 16 pins: B 14 pins: C 22 pins: D 24 pins: E

Note: The short vertical lines indicate filter capacitor locations.
(143 Places)

16 pins REVERSED!!!
typical of MK4116: F
Changes from Rev E to Rev F:
1) Added the signal Disable2 (pg 20, 12) for last
2) Removed HParityErr* from the term that forms Abort* (gate at a15 now free, inverter at e1 moved).
Note: This change deletes IC a15.

Changes from Rev F to Rev G:
1) h11.1b (pg 1) - Gm X, not GmX* (this was wrong in .nl file, ok on dwg.)
2) h13.9 - CcntSyn4, h13.11 - CcntSyn6 (pg 3)

Changes from Rev G to Rev H:
1) (pg 13) Change e1.13 from HamClock to EdgeClock
2) (pg 1, 15) Changed g9 from S74 to S175. Relocated g9's functions to i10. Added MOBands as H.05 during H-Pipe operation.
3) (pg 16) Deleted S04 at a10. Replaced with S00 at a15a, and added MC1StartMC2* as input to MC1Active.
4) Added MC2PS12* by replacing f3 (S74) with S175 (pg 19). MC1PS12* is used instead of PSStore12* at a1.13 (pg 20).

Changes from Rev H to Rev I (5/9/78)
1) (pg 20) h.3.9 was MC2HoldISNE0, is now MC2StartXport after passing through the 8T09 at h6b (used as a driver).
2) Renamed signal MC2TestISNE0 to MC2HoldISNE0 (essentially, these two signals have been coalesced into one).
3) Added test points.
4) Added comments on Vee bypass and -10V supply changes to D0memplatforms.sil

Changes from Rev I to Rev J (8/12/78 - C. Thacker)
1) Renamed signal TP055 GateALUParity, and connected it to E079 (pg 10)
2) Latched signal StorAccessType in S374 at h4f (pg 15)
3) Removed MC2XM2Word and MC1XM2Word from a5.11 and a5.12. Connected a5.11 and a5.12 to a5.13 (pg 16). Note that signal MC1XM2Word is no longer used on this card, so E006 is free.
4) Removed -10V supply components on D0memplatforms.sil

Changes from Rev J to Rev K (10/8/78 - C. Thacker)
1) Changed h7.12 from MC1WriteMem to MC1WriteMemSlow (pg 13). This signal is generated at platform a16 (pg 12).
2) Changed platform a16 to 20pins to make room for MC1WriteMemSlow (pg 12).
3) Added capacitors on StorMapRSA* and StorMapWrite* (platform c5, page 12).
4) Changed a5.12 from MC1Task.3 to MC1Next.4 (pg 15).
5) Changed i7.1 from P03b to referenced (pg 15). This requires changing PROM 17 to revision E.

Changes from Rev K to rev L (11/1/78 - C. Thacker)
1) Signal clkOutputReg is now clkOutputReg* by removing S37 at h6a (now free) page 13.
2) h10.1 (pg 15) was Disableb10, is now GND. Also removed Disableb10 from SPLAT i1 (pg 12).
   There are no prom changes in this revision.

Changes from Rev L to rev M (12/9/78 - C. Thacker)
1) Changed platforms c5 and i1 - removed capacitors and changed values.
2) Changed the generation of clkOutputReg* (pg 13). This signal is now one cycle wide, rather than being a qualified EdgeClock.
3) The input to h5g (pg 13) is ProtoeAd*, not EnRlewAd*. This board requires an ALU board of rev M for proper operation.
   There are no prom changes in this revision.

Note: Rev M = Rev Ga

Changes from Rev Ga to rev Gb (7/18/80 - CPT).
1) Added 16 FICAPS for MK4116 chips (VDD and VEE)
2) Added glitch suppression capacitor adjacent to h7 (on MC1WriteMemSlow - 100pf).
3) Changed interlock logic on page 18.

Current PROM Revisions:
- a4, a3, a2, b3, b4, c2, c3, d2, d3, e3 (MC1 Sequencer): E
- g3, g1, h1, h2, i2 (MC2 Sequencer): D
- i7 (Fault): E
- b11 (Ftype, Pipe): D
- f14 (Single/Double errors) D