# Dandelion I/O Processor

## Logic Drawings

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<tr>
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I/O Control

(4 addresses each)

I/O Device selector

(I/O addresses 80H - 06FH)

Memory Control

PROM Bank Selector

(Addresses Bank 0: 00H - 7FH,
Bank 1: 800H - 0FFFH,
Bank 2: 1000H - 17FH,
Bank 3: 1800H - 1FFFH)

RAM Bank Selector

(Addresses 2000H - 3FFFH, 8K)

RAM Bank Selector

(Addresses 4000H - 5FFFH, 8K)

Note: Banks 4 and 5 reserved for Options board.
Note: Bank 5 temporarily used for DMA tests.

Single Register Block

(Bank 6, registers 8-15, addresses 0E3H - 0EFH)
Bidirectional bus-driver

CPUAD.00 2 LS245 #18 IPData.00 92
CPUAD.01 3 A7 B0 17 IPData.01 192
CPUAD.02 4 A1 B1 16 IPData.02 193
CPUAD.03 5 A2 B2 15 IPData.03 93
CPUAD.04 6 A3 B3 14 IPData.04 94
CPUAD.05 7 A4 B4 13 IPData.05 194
CPUAD.06 8 A5 B5 12 IPData.06 95
CPUAD.07 9 A6 B6 11 IPData.07 95

T CS' b12 T = 1 -> A to B

Enable IPData'

Alternate I/O Data Bus

Enable Data Bus Prom (EnDataProm)

CPUAD.00 2 LS245 #18 IPData.0 1 II #TP034
CPUAD.01 3 A0 B0 17 IPData.1 1 II #TP035
CPUAD.02 4 A1 B1 16 IPData.2 1 II #TP036
CPUAD.03 5 A2 B2 15 IPData.3 1 II #TP037
CPUAD.04 6 A3 B3 14 IPData.4 1 II #TP038
CPUAD.05 7 A4 B4 13 IPData.5 1 II #TP039
CPUAD.06 8 A5 B5 12 IPData.6 1 II #TP040
CPUAD.07 9 A6 B6 11 IPData.7 1 II #TP041

T CS' b12 T = 1 -> A to B

Enable IPData'

Note: Ch2 is used temporarily by DmaTest.
Note: Do not use DMA memory addresses in the I/O Address space.
Floppy Disk Controller Clock generator

Motorola Clock 16.000 MHz

Head Load Delay

T = 40 ms

Note: Discrates on page 27
From FD cable (page 28)

FD Pull-ups = 150 Ohms, 1/4 Watt

Backplanned for Troy controller

FD Index' 2

FD Index' 1

FD Index' 1 tl # TP073

LSO4 h5b

FDCHld 2

FDHldLoad'

118

FD Ready' 4

FDCReady

FDStep 4

FDStep'

119

FDTk00' 6

FDCtl00'

FDDirectionIn'

122

FDWrProt' 8

FDCWrProt'

1 tl # TP075

LSO4 h5c

SGWGate 8

FDWGate'

124

FDTwoSided' 17

Flipper TwoSided

FD Comp 17

FDWData'

125

FDRdData' 15

FDRaw RdData

FDCT43 11

FDWCurrent'

126

FD Disk Change' 13

Floppy Disk Change

Note 1: Active high if two sided diskette is installed on SA 850

Note 2: I/O Connector description on page 28.

Note 3: For cable documentation see SA 850 OEM manual

Note 4: TP 076 above is to be used to provide high/a signal when EnFDChr' is inactive.

FDC Index tl # TP077

Note: Schottky

FD Index tl # TP078

FDC Index tl # TP077

Note: Schottky

FDC Index tl # TP078

(Skip line)

S240

Self Troy Mode

(Pullup, page 27)

Note 1: Active high if two sided diskette is installed on SA 850

Note 2: I/O Connector description on page 28.

Note 3: For cable documentation see SA 850 OEM manual

Note 4: TP 076 above is to be used to provide high/a signal when EnFDChr' is inactive.

From FD State Register

Self Floppy Drive 2

FDSolDrive'

18

g2a

S240

Note: Schottky

Gate used by Bell

Self Floppy Drive 2

FDSolDrive'

18

g2a

S240

Note: Schottky

Gate used by Bell

Self Floppy Drive 2

FDSolDrive'

18

g2a

S240

Note: Schottky

Gate used by Bell
Raw Read Data synchronizer and pulse shaper

Pulse width = 125 ns

Inputs to WD1791:
- FD RdDataSync' Data
- FD CRCik - Data Window

Double density selection

DDen = SelDoubleDen . (SelSidoO . Track00)'

Disabled by tester.

DataSepProm

SepState State Machine

Note: Data Window is always high order state bit.

1K x 8 Prom state machine

Disabled by tester.
DMA Test Register

For testing Dma controller independently of Floppy disk.
This register uses Dma channel 2 temporarily, and SelBank5' to enable.
Can be removed later.

[Diaagram of DMA Test Register]

XEROX

Project
Dandelion

I/O Processor
DMA Test

File
DandIOP13.sil

Designer
Ogus

Rev
J

Date
2/22/80

Page
13
Interrupt Request Register

FloppyIntReg → 2 → 18 → IPData.00
   1 → c12a (FloppyIntReg')

KBintr → 4 → 18 → IPData.01
   1 → c12b (Keyboard Request')

PrinterTxRdy → 6 → 14 → IPData.02
   1 → c12c (Printer transmitter Request')

PrinterRxRdy → 8 → 12 → IPData.03
   1 → c12d (Printer receiver Request')

ReadIntReg'
   1 → LS240

165 → MiscInt → 17 → 3 → IPData.04
     1 → c12e (Misc. Interrupt')

164 → Int.5 → 15 → 5 → IPData.05
      1 → c12f (unassigned)

164 → Int.6 → 13 → 7 → IPData.06
      1 → c12g (unassigned)

164 → Int.7 → 11 → 9 → IPData.07
      1 → c12h (unassigned)

Temporary:
IOPIntReq0 - RS232C - Options
IOPIntReq1 - LSEP UART Tx - Options
IOPIntReq2 - LSEP UART Rx - Options
IOPIntReq3 - Miscellaneous interrupt
(from Timer)

Host Address Prom
(HostAddrProm)

GND → 15 → F93427
  1 → A7
  2 → A6
  3 → A5
  4 → A4
  5 → A3
  6 → A2
  7 → A1
  8 → A0
  9 → CS
  10 → Q3
  11 → Q2
  12 → Q1
  13 → Q0
  14 → CS'
  15 → CS'

Host address is 48 bits long, stored in addresses 0 - 11 of the Prom.
Address 12 should contain a 4-bit checksum of the address.
Host address Prom has the 16 I/O Bank 3 addresses.

I/O address          Host address bits
      OB0H           0-3
      OBCH
      OBDH

checksum

XEROX
Project
SDD
Dandelion
I/O Processor
Interrupt Req. req, Host address
File
DandIOP14.sil
Designer
Ogus
Rev
J
Date
4/22/80
Page
14
Keyboard Data

ReadKB' latches data from KB
ReadKBData' reads it into CPU

Pullup/pulldown resistors
16-pin package

Bell circuit on page 27.
X-coordinate

Y-coordinate

Note: Use LS191 + LS244 if not 25LS2569

MouseProm

Each transition of XA or XB (YA or YB) causes the particular counter to be incremented or decremented. The samples are made with the inverted processor clock to ensure that the counters are stable when a read or clear of the counters is done.
IOP CPU Clock generator

Motorola Clock 6.00 MHz
(5.88 MHz temp.)

Note: pulled up

CPU boot

Note: We need to pass the slowly-rising boot signal through a Schmitt-trigger before we go through the LS08.

Dip Cable to Alto-IOP interface

18 pin socket for DIP connector

External Waits can be requested from the Options card. The RS232 will require a Wait cycle.

Currently, all devices on IPAData cause a Wait cycle.

Disabled by tester.

CPU Ready

Pullups

XEROX
SDD
Project
Dandelion
I/O Processor Miscellaneous CPU control

File
DandiOP21.sil

Designer
Ogus

Rev
J
Date
5/8/80
Page
21
Printer UART

From printer cable

PTTxData 1
PTDTR 4
PTRTS 10
(none)

PTCCTS 8
N75189

PTCSR 3
N75189

IPReset 21
IOPClk 20
IPAddr.15 12
IPAddr.13 13
IPOWr 10
C/L 7
RD 8
WR 9
others

75188 Voltage Hookup
(see page 28)

75188 Ground hook-up
GND 7 d11

Note: Connector labels correspond to the Printer signals.

Baud-rate generator

IPAddr.14 20
IPAddr.15 19
SD 21
TimerRT 22
TimerWR 23
High/a 9
G0 11
G1 15
implemented

(Clock from pg. 20)

Baud-rate oscillator (1.8432 MHz)

RFout 8
BRClk a5
EnKBBell 115
i8253

KBBC 1
() #TP10S
GND 19

Note: When the bell is disabled, the signal KBBCClk should be high to turn off transistor driver. KBBClClk goes high when the bell clock is disabled.
Note: All the logic on this page is powered from the Maintenance panel + 5V supply, MVcc (see page 26)

Seconds Counter

SetClkA
1HzClk

1HzClk' From MP cable

1 usec (typ)

Clock counter Load SR

SetClkB
Time.24

SetClkB
Time.24

SetClkC
Time.16

SetClkD
Time.08

SetClk'

SetTime = 0 => 32 bit counter
SetTime = 1 => Four 8-bit counters

SetClkB'
SetClkB

SetClkB'
SetClkB

SetClkC'
SetClkC

SetClkB' 4
SetClkB

SetClkB' 4
SetClkB

SetClkB' 4
SetClkB

SetClkB' 4
SetClkB

The 8 inputs are pulled up for the power-down condition.

ReadClk'
SetClkB

ClearTime'
SetClkB

ReadTime'
SetClkB

SetTime'
SetClkB

GND 1
EN 19

XEROX SDD
Project Dandelion
I/O Processor Time-of-Day Clock - 1
File DandiOP25.sil
Designer Ogus
Rev J
Date 5/8/80
Page 25
Time Read Shift Register

Note: All the logic on this page is powered from the Maintenance panel +5V supply, MVcc

ReadTime = 0 =>
Shift register parallel loads Seconds Counter
ReadTime = 1 =>
Shift register in serial shift mode, CkReadSR' clock

Power for Time-of-day clock from Maintenance Panel

MVcc  14   a6p   LS393
      14   a7p   LS393
      14   i6p   LS393
      14   i7p   LS393
      18   a5p   LS240
      16   g5p   LS157
      14   i5p   LS08
      16   i1p   LS165
      16   i2p   LS165
      16   h1p   LS165
      16   h2p   LS165
      20   g1p   LS244

16-pin resistor pack
5.1K pullups

When the IOPPower is off, the signal EnMPSignals' is inactive (high), thus disabling those signals, which feed unpowered logic.
DISCRETE COMPONENTS

Pullups, 150 ohm, 1/4 watt
Allen-Bradley 316B161

VCC 1
RS1 2  RS0 2
RS2 3  RS02 3
RS3 4  RS03 4
RS4 5  FDIndex' 5
RS5 6  FDDReady' 6
RS6 7  FDTR00' 7
RS7 8  FDWPProt' 8
RS8 9  FDNTwoSided' 9
RS9 10  FDBDiskChange' 10
RS10 11  x1 (pseudo position)

15K 1
1' 2  FDHDC 1
10uF 2  HDLDc 1
1LFT 2  # TP114
1LFT 2  # TP115

CPU clock driver pull-ups

Miscellaneous Floppy Controller discrete components

ppClk termination

Keyboard Bell Driver

Discretes for Testability

Floppy Disk jumper

GND 1' 2  FDid
0 ohms
Jumper in: SA 850 drive
Jumper removed: SA 800 drive

Pullup for Reset line from Alto

VCC 1' 2  AltoIPReset'
10 K
(Node for when no Alto is connected)
Inputs

- 220. FDIindex'
- '20/19'.
- 222. FDReady'
- J1[22/21].
- 223. FDTok00'
- J1[42/41].
- ✓ 244. FDWrProt'
- J1[44/43].
- 243. FDTwoSided'
- J1[10/9].
- ✓ 246. FDrdData'
- J1[43/45].
- 248. FDDiskChange'
- J1[12/11].
- 213. GND

Unused signal grounds

- 223.
- 227.
- 229.
- 231.
- 247.
- 249.

Outputs

- FDlnUse'
- FD-J1[16/15].
- FDWrLoad'
- FD-J1[18/17].
- FDStep'
- J1[36/35].
- ✓ 236. FDDirectionnl'
- J1[34/33].
- ✓ 240. FDWrGate'
- J1[40/39].
- ✓ 233. FDWrData'
- J1[38/37].
- ✓ 226. FDDiskChange'
- J1[26/25].
- ✓ 214. GND

Unused signal grounds

- 223.
- 227.
- 229.
- 231.
- 247.
- 249.

Flloppy Disk Cable Connector
50-pin male connector
Xerox 713W14820
(Subtract 200 from above pin numbers to get physical pin number)

Maintenance Panel Cable Connector
14-pin male connector
Xerox 713W13320
(Subtract 400 from pin numbers to get physical pin number)

(Printer)

- 2. PTTxDATA
- PTTxDATA
- 10. PTDTTR
- PTCTS
- 4. PTTRTS
- PTDSR
- (ON when power is on)
- PTCD

GND (Frame ground)
Note: Currently NC to Frame Ground in harness

GND (Signal ground)
Note: Connector labels correspond to the Printer signals.

RS-232-C DCE port Cable Connector
10-pin male connector
Xerox 713W12220
(Above pin numbers are same as physical pin numbers)

75188 Voltage hookup

VDD 14 d1 e 1 VFF
(+ 12V)
N75188
(- 12V on PC)

XEROX
CABLES

Keyboard cable connector
40-pin male connector
Xerox 713W12720
(Subtract 50 from above pin numbers to get physical pin number)

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<td>Ogus</td>
<td>J</td>
<td>5/8/80</td>
<td>29</td>
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IOP - CP communication - Port timing

Timing Diagrams (not to scale)

CPOut
CPOutWr' (10Wr')
CPOutIntReq (Also DMA Request)
CPOutWakeReq
IOPReq (CPClk sync)

Data written by IOP
Data read by CP

CPIn
CPInWr' (IOPIData')
CPInIntReq (Also DMA Request)
CPInWakeReq
IOPReq (CPClk sync)

Data written by CP
Data read by IOP

400, 590 nsec
137
39
400, 750 nsec
ALTO-DANDELION Communication via Umbilical

Alto Operations

Output:

```
  0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

UTILOUT  (177016B)
```

- Used for logic analyzer interface
- Select Input Nibble
  - 0: High nibble
  - 1: Low nibble
- Miscellaneous control (TBD)
- Alto ACK
- Alto REQ
- Reset IOP (boot)

Sequence of Output operation:
- Output data to UTILOUT
- Alto Request (Set AltoREQ = 1) (UTILOUT[0])
- Read Dandelion ACK
  - DandelionACK = 1 means data received.
- Remove Alto Request (Set AltoREQ = 0)
- Read Dandelion ACK
  - DandelionACK = 0 means data accepted.

Input:

```
  0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

UTILIN  (177030B)
```

- Data
- Unused
- Dandelion ACK
  - 1: Data received in Dandelion buffer
  - 0: Data removed from Dandelion buffer
- Dandelion REQ'
  - 1: No data available
  - 0: Data available

Sequence of Input Operation:
- Poll Dandelion REQ (UTILIN[4])
  - DandelionREQ' = 0 means data is available.
- Set SelectInputNibble = 0 (UTILOUT[7])
- Read high data nibble (UTILIN[0:3])
- Set SelectInputNibble = 1 (UTILOUT[7])
- Read low data nibble (UTILIN[0:3])
- Alto Acknowledge (Set AltoACK = 1)
- Poll Dandelion REQ'
  - Dandelion REQ' = 1 means ACK has been received.
- Remove Alto Acknowledge (Set Alto ACK = 0)
ALTO-DANDELION Communication via Umbilical

Timing Diagrams (not to scale)

Alto to Dandelion:

Alto Output Data

AltoREQ

DandelionACK

8085 Internal Signals:

8085Read'

8085Interrupt

Dandelion to Alto:

DandelionREQ'

AltoACK

Alto Input Data

8085 Internal Signals:

8085Write'

8085Interrupt
Dandelion I/O Processor Floppy Disk Controller

WritePre-compensation Timing Circuit
(See DandIO90.sil for circuit)

FD CW rData

WDL

LateHold
EarlyHold

WDS

WDEarly

b

WDL C r (c)

′earWDL′

WDNorm

e

f

WDLate

Floppy 16MHz

Phase Jitter = +/- 31.25 ns
Precompensation = 187.5 ns +/- jitter
WriteData Pulse width = 187.5 ns
### IPData Loads

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**Backplane**

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2650 Fixed input loads

530 3450 LS245 drive, all other bl or out are tristate
3650 LS245 input

---

### IPData Loads

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100 460 LS245 drive, other LS245 tristate
100 640 LS245 drive, other LS245 input
100 660 Mos drive, one LS245 input, 1 LS245 tristate
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260 1000 8085, 2114, or 2716 drive
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60  440  IPMemRd'
340 720  IPMemWr'
240 3290  IPIORd'
200 3040  IPIOWr'
1. Filter capacitors: 1 per 3 chip positions  
   1 per 2 chip positions for 2114L, 2716  
   1 per 8085, 8257, 1793/7, 8251, 8253

2. Spare chip positions at PC locations c5, f5, g5, d4, I3  
   Unused chip positions b11, c11, d11, e11 (can be made spare)

3. CP clocks:  
   Chip S02 at PC location a11 should not be moved.  
   Resistors R8 and R9 should be as close to backplane edge-connector pin 9 as possible.  
   Clock qualifier chip is at i10 - position is acceptable.

4. FD1793/97: Either a FD1793 or an FD1797 can be plugged into stitchweld position p8.

5. Board stiffener is to be placed between PC rows 2 and 3, so that the Alto umbilical socket (PC location h2) is on the I/O connector side of the stiffener. Alto Umbilical socket is an 18-pin socket.

6. ***Important***:  
   The time-of-day clock chips (boxed at lower left side of layout) receive their  
   Vcc power from the Maintenance Panel connector. They are NOT to be powered  
   by the board Vcc. Ground pin is the same as the board ground. The signal, MVcc,  
   originating from the Maintenance Panel connector is already wired to the  
   appropriate Vcc pins of the affected chips. The affected chips are:  
   PC locations: a2, b2, c2, d2, a3, b3, c3, d3, a4, b4, c4, a5, b5.

7. The nets IPAddr.xx (16 nets), IPData.xx (8 nets), IPADData.xx (8 nets), CPUAD.xx (8 nets),  
   IPMemWr' (1 net),  
   are long nets with many nodes, and the maximum length should be minimized  
   as best as possible. If necessary, a hand layout of these busses should be done.  
   For example:  
   The RAM memory should have the busses, IPAddr.xx, CPUAD.xx, and IPMemWr' laid  
   out as follows, to  
   shorten themaximum length

   ![Diagram]

8. Voltages used by this board: +5 V, +12 V, -12V.

9. All locations to be provided with IC sockets.

10. Note the positions of the Maintenance Panel and RS-232-C DCE connectors.  
     They have been reversed in position from previous board drawings.

11. High/a, High/b, High/c, and High/d, are constant high signals, and can be  
     interchanged if necessary.
<table>
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Dandelion I/O Processor

Revision History

Rev. A to Rev. B. 
1. Signals on A and B ports of LS245 (g11) switched to account for correct sense of CpuS1 signal. (T = 1 -> A to B) (pg. 1)
2. Enable (pin 1) of LS240 connected to GND. (pg. 1)
3. From macro changed for I2716 (h12), to reverse data bus connection. (pg. 2)
4. Ports PA, PB, and data bus reversed on i8255A (I9) with macro change. (pg. 5).

Rev. B to Rev. C. 
1. DMA controller added (pg. 7).
2. Floppy Disk controller added (pgs. 8-12).
3. New bus organization (see page 006c)
4. Address space change, to allow both memory or normal I/O mapping. IPAddr.00 on e8, I8, pin 14 (pg. 1).
5. IPDataOut signal (c6b, pin 9, pg. 1).
6. CPUReady signal to insert wait state for FDC, and DMA (slave). (pg. 6)
7. Change in generation of IPMemRd', IPMemWr', IPIORd', IPIOWr'. This removes the LS257 to avoid the output glitches which occur when device goes from tristate to active. (Gary Miller, Intel, 987-8086, 6/20/79) (pg. 1).
8. New I/O address decoding (pg. 5)

Rev. C to Rev. D. 

Bug Fixes
1. Added inverters for CpuRd', CpuWr', DmaMemRd', DmaMemWr', DmaIORd', and DmaIOWr' and replaced LS253 with LS353 to fix multiplexer glitch when S2, S1 lines change. (page 1)
2. Fixed pullups for FloppyIntReq, FDCVFOen' (I8, page 6).
3. Removed boot switch backplane signal (pg. 6).
4. Buffered FDChld (page 8).
5. IPReset' now clears FloppyDataReq and FloppyEndCount (page 8).
6. Hld on shot: c2a.1 to GND (page 10).
7. inUse signal to drive removed (drive can be jumpered), FDCTG43 and DiskChange signals added (page 11).

Additions
1. CP control and control store read/write, TPC/TC read and TPC write added (page 15).
2. Backplane connections added.


Bug Fixes
1. LS353 inputs to GND instead of Vcc (page 1)
2. Pullup for FDCDataReq.

Additions/Changes
1. Reorganization of bus structure. Two I/O data busses, IPData (TTL) and IPAD (MOS). This is due to loading reasons for the MOS devices.
2. Added CP Port, keyboard, Mouse interfaces, Printer, maintenance panel, time-of-day clock Interface.
3. Increase PROM to 8K, RAM to 16K.
3. Alto module moved off IOP board.

Stitchweld Board History

S/N 001: A, B, stripped, E
S/N 002: B, C, D, scrapped
S/N 003: F
S/N 004: H

XEROX SDD

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# Dandelion I/O Processor

## Revision History - 2

### New Functions:
- Redesign of maintenance panel, incorporation of time-of-day clock in IOP (pg. 24, 25)
- Host address prom (pg. 14)
- Backplane signals for options IOP.

### General:
- All signals are named.
- Separate pages for discrete and I/O connectors, different versions for PC and SW boards.
- Backplane conforms to Backplane Rev. B.
- Keyboard interface changed (pg. 18)
- Mouse front end redesigned (pg. 19)
- CPStatus has new CSpErr, CPControl inputs (pg. 15)
- IOPdata and IOPData bus enable logic changed (pg. 6)
- SKY signals renamed to High.
- Part substitutions as recommended by CP&T made.

### Bug Fixes:
- Enable of FDCData bus changed to avoid interference with Dma controller (pg. 8)
- pWaitClik* generated and used (pg. 15-17)
- WakeMode inputs inverted on IOPReq prom (pg. 17)

#### Page 1:
- IPMemRd', IPIORD' BP changed 86, 186 to 79, 179.
- LS240: b19h changed to b17a. b17d Inverter added for IOPClik to BP 12.

#### Page 5:
- SelBank 1a - 1d', SelBank 4, 5, backplanned.
- I/O address banks renamed: 0a to 0b, 0b to 1, ..., 3a to 6, 3b to 7.
- SelDma' moved to Bank 2, SelControlStore' renamed, moved to bank 6.

#### Page 6:
- EnIPData, EnIOPData generation changed. EnDataProm (c9) added. a12a, c9a, c9b, c6a removed.
- Signal IPIORD' renamed.

#### Page 7:
- DmaCycle backplanned.
- DmaCh2Req, DmaCh3Req, DmaCh2Ack*, DmaCh3Ack* named and backplanned.
- DmaTest uses Ch2 signals. DmaTestReq'Ack' removed.

#### Page 8:
- FCVF0en LS04 moved to pg. 12.
- Bug fix for EnFDCData. Added LS00 g7d, g7c.
- FDCI meaning changed to indicate 800/850 drive.
- DmaTestReq in Floppy state renamed to DmaCh2Req.

#### Page 9:
- EY' on LS153 disconnected. LS253 replaced by LS153.

#### Page 10:
- S163 replaced by LS183.
- Discretes moved to pg. 27.

#### Page 11:
- I/O connector moved to pg. 27.
- InUse added. SelDrive1, InUse, SelSide0 3240 always enabled.
- I/O signals backplanned for Troy.

#### Page 12:
- FDCVF0en LS04 moved from pg. 8.

#### Page 13:
- DmaTestAck*, SelDmaTest renamed to DmaCh2Ack*, SelBank5'

#### Page 14:
- HostAddr prom added. Int5-7 backplanned.

#### Page 15:
- SWTAddr sense changed in CPControl = IOPKernel change.
- IOPWait, SWTAddr, SWTAddr' synced to CPControl before backplane.
- WRTPcIow' inverted before backplane.
- Control Store write addresses permuted = => IOPKernel change.
- LS240 b19 changed to b17. S00 (a19) moved to b18.
- IOPStatus permuted. PWaitClik' used instead of pClik'

#### Page 16:
- S00 a19 moved to b18. LS240 b19 moved to b17. PWaitClik' used instead of pClik'.

#### Page 17:
- Bug fix WakeMode permutation on IOPReq prom. IOPAttn backplane changed from 139 to 138 (i00isp.1).
- Extend CPPort status to include CSPErr, CPControl inputs.
- Add pWaitClik'. S02 in a19, move S00 to b18.

#### Page 18:
- Moved KB connector to pg. 27.
- Change KB Sel', KB Dblag' drivers from 74265 to 75114. FPLAT to RDV16. Connector 1000pF capacitor between 75115 pins 6, 7.

#### Page 19:
- Added new mouse front end (MouseProm). Moved MiscInput1 to pg. 20.

#### Page 20:
- MP connector moved to pg. 27. MiscInput1 moved from pg. 19. MiscControl1 LS174 replaced by LS273.
- KB Bell changed by addition of discrete amplifier.
- MiscClocks1 addition of SetClik0'. 1HzIntr' renamed 1HzClikB'.

#### Page 21:
- Floppy disc moves to pg. 27. FPLAT renamed RPULL16, PLAT18.
- CPUReady changed. IOPData always causes Wait cycle, ExtWaitReq' available form backplane.

#### Page 22:
- KB Bell clock added

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**Rev. F to Rev. G**

### Bug Fixes:
- Added Schmitt trigger to BootReset' signal path to fix power boot problems (pg. 21)
- Renamed ReadTime (e5.5, LS240) to ReadT since it is different from ReadTime (pg. 25, 26)
- Added inverter to SelClik driver to cause driver to be off when bell is disabled (pg. 20, 22).

### Changes:
- Backplanned IPDataOut (pg. 1), BRClik (pg. 22).
- Moved CSPErr and TODInstr' to MiscInputs. Added EmuWake to CPStatus (pg. 14, 17, 20)
Dandelion I/O Processor

Revision History - 3


Bug Fixes:
PTCRxD line did not exist. Incorrectly connected to PTCTxD. Printer control (page 22). Printer cable pin 20 incorrect on PC cable. Corrected to pin 25 (page p28).

Changes:
- Backplane IPALE (page 1) to pin 38 for use with State Analyzer.
- ReadK8 moved from MiscClocks to MiscControl (pg. 20).


Changes: Incorporation of testability features suggested by Fortlage memo.
Addition of miscellaneous timer for use as Interrupt by CPU.

Page 1:
- Isolation of CpuClk, CpuReset, CpuALE, DmaHoldReq with LS244 buffers under tester control.
- Tester control of LS353 Enable inputs.
- Change in IOPClk generation.

Page 6:
- Tester control of EnDataProm CS' Inputs.

Page 7:
- Isolation of CpuHoldAck, DAck0-3', DmaEndCount, DmaAEN, DmaAddrStrobe by LS244 buffers under tester control.
- DmaCycle generations changed.

Pages 8, 9, 10, 11, 12:
- Isolation of FDCDataReq, FDCWrGate, FDCWrData with LS244 buffers under tester control.
- Isolation of FDCEarly, FDCLate. Floppy 16MHz generation changed.
- Floppy cable receivers can be disabled under tester control.
- FloppyProms' isolated. Floppy proms can be disabled by tester.

Page 14:
- MiscInt fed to Bit 4 of Int Req register.

Page 17:
- IOPReq prom can be disabled by tester.

Page 19:
- MouseProm can be disabled by tester.

Page 21:
- CpuReady isolated by LS244 buffer

Page 22:
- Extra timer added from 82353.

Page 27:
- Keyboard cable moved to page 29 (PC only).
- Tester discretes added. Jumper for Floppy disk id added (PC only).


Changes: Incorporation of test pads.

Page 27:
- Addition of 10K resistor to AltoIPreset' to pull up to Vcc when Alto not connected (PC only).
Dandelion I/O Processor

Design Notes

General
Wait states forced for all devices on IPAData. External WaitReq available for RS232 Z80-SIO.

CPU
1. See notes on memory address space (pg. 70, 71.
2. Mem, I/O Rd'/Wr' decoding changed to avoid LS257 potential glitching.

Floppy Disk Controller
1. WD1791 chip used temporarily. Eventually will use 1797 or 1793-01.
   This has the following effects:
   - Inverted data bus - compensate in software.
   - No VFOE signal available (dummy one generated) for separator.
   - Side Select signal generated by Floppy Control register.
   - DMA worst case timing in DMA write: 1791 and 2114 has write setup time problem. (see page 32)
     1793-01/51 with 2114, or 1791 with 2114-3 OK.
   Current plan is to upgrade to use 1793-01 and not take advantage of the extra 1797 features.
   1797 can be plugged into same position.
2. Need 1 wait state with FDC chips and full-speed 8085A
3. Need FloppyDataReq latch when using 8257 DMA controller.
4. Floppy EndCount latch implemented to check correct DMA completion. Could be removed if not needed.
5. Floppy status register implemented to read external floppy status. FloppyIntrReq is in a common intrReq register.
6. Write compensation: Note jitter characteristics. Could use delay line or WD2143 if not tolerable.
   Currently a Disable write comp. in control register. Later,
   DisableWDComp = [DDan' or TG43')', EnableWDComp]
7. WriteCurrent signal not provided for drive (from TG43). Supplied in Rev. D

9. Select Drive 2 and Select Troy mode signals available.
10. Read Separator synchronizer has only one stage. When next reblowing Prom add a second stage (D0-Q0 of LS273).
    Feed DataSync' through LS273, Q0 to 1791 RData', Prom should expect complemen of RData.

DMA controller
1. Wait state required in slave mode.
2. Use extended write.
3. Intel 8257 chip used currently. Later could use 8237 controller.
   This provides programmable single byte transfer (see FloppyDataeq latch above).
4. Fully buffered address, control, and data buses.
5. Dma Test register added to channel 2 to allow Dma testing. The Dma Req Is temporarily taken from Floppy State Register,
   using signal SelFloppyDrive2.
6. DmaTest register temporarily uses the whole of I/O bank 5 addresses.
7. DACK0' and DACK1' are fully loaded (80 uA, 1.6 mA)

CP port
See programming description (pg. 72, 75)

TOD clock
Time-of-day clock has potential problem if IOP Is powered and maintenance panel cable is unplugged. This is because there
is some logic which is unpowered (in the TOD clock) which is driven by powered logic (in the IOP). This problem is to be
described in a memo and will be further investigated.
# Dandelion I/O Processor Address Space

## Normal memory address space

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</tr>
<tr>
<td>4</td>
<td>RAM</td>
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</tr>
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<td>5400 - 57FF (1K)</td>
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</tr>
<tr>
<td>6</td>
<td>RAM</td>
<td>5800 - 5BFF (1K)</td>
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<tr>
<td>7</td>
<td>RAM</td>
<td>5C00 - 5FF (1K)</td>
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**Dandelion I/O Processor Address Space**

### I/O Address Space

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<td>Alto PPI-C</td>
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<td>Alto PPI-Control</td>
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<td>0</td>
<td>Floppy Sector (R, W)</td>
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<td>Floppy Control reg. (Write)</td>
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<td></td>
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<td>0</td>
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<td>89</td>
<td></td>
<td>0</td>
<td>Printer Status (Read)</td>
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<td></td>
<td>0</td>
<td>Same as 80, 80</td>
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<tr>
<td>8C</td>
<td></td>
<td>0</td>
<td>Timer Counter 0 (R,W)</td>
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<tr>
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<td>0</td>
<td>Timer Counter 1 (R,W)</td>
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<td>0</td>
<td>Timer Counter 2 (R,W)</td>
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<td>0</td>
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**Dma 8257**

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<td>0A7</td>
<td></td>
</tr>
<tr>
<td>0A8</td>
<td></td>
</tr>
<tr>
<td>0A9 - 0AF</td>
<td></td>
</tr>
<tr>
<td>0B0 - 0BF</td>
<td></td>
</tr>
<tr>
<td>0D0 - 0DF</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

1. I/O Ports can be reached using:
   - IN or OUT instructions using port address:
     \[ P = 80H + p, \text{ where } 0 \leq p \leq 7FH (128) \]
   - Memory reference instructions using address:
     \[ A = 8000H + p, \text{ where } P \text{ is given above} \]

   Note that bit 8 being 1 is not required by the hardware.

2. Bank addresses (hex):

<table>
<thead>
<tr>
<th>Bank</th>
<th>Address</th>
<th>Data bus</th>
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</thead>
<tbody>
<tr>
<td>Bank 0</td>
<td>80 - 8F</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 1</td>
<td>90 - 9F</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 2</td>
<td>A0 - AF</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 3</td>
<td>80 - 8F</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 4</td>
<td>C0 - CF</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 5</td>
<td>D0 - DF</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 6</td>
<td>E0 - EF</td>
<td>IPAData</td>
</tr>
<tr>
<td>Bank 7</td>
<td>F0 - FF</td>
<td>IPAData</td>
</tr>
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3. Addresses in Banks 4 and 5 are reserved for the OPTIONS card. DmaTest temporarily uses bank 5.
### Write Registers

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Floppy Control</th>
<th>Misc. Control 1</th>
<th>Misc. Clocks 1</th>
<th>CP Control</th>
<th>TPCHigh</th>
<th>TPCLow</th>
</tr>
</thead>
<tbody>
<tr>
<td>E8</td>
<td>EF</td>
<td>E9</td>
<td>EC</td>
<td>FE</td>
<td>FF</td>
<td></td>
</tr>
<tr>
<td>Bit 0</td>
<td>Enable Wait cycles</td>
<td>(unused)</td>
<td>(unused)</td>
<td>IOPWait*</td>
<td>TPCAddr.0</td>
<td>(unused)</td>
</tr>
<tr>
<td></td>
<td>Enable Write Comp.</td>
<td>ReadKB</td>
<td>Clear MPanel</td>
<td>SwTAddr*</td>
<td>TPCAddr.1</td>
<td>TPCData.06*</td>
</tr>
<tr>
<td></td>
<td>Select Side 1</td>
<td>Enable Bell</td>
<td>Inc. MPanel</td>
<td>IOPAttn</td>
<td>TPCAddr.2</td>
<td>TPCData.08*</td>
</tr>
<tr>
<td></td>
<td>Select Troy Mode</td>
<td>Diagnose KB</td>
<td>Read Time Cnk</td>
<td>CP DmaMode</td>
<td>TPCData.00*</td>
<td>TPCData.07*</td>
</tr>
<tr>
<td></td>
<td>Select Double Den.</td>
<td>Blank MPanel</td>
<td>Set Time CnkA</td>
<td>CP Dma In</td>
<td>TPCData.01*</td>
<td>TPCData.08*</td>
</tr>
<tr>
<td></td>
<td>Enable Floppy contr.</td>
<td>Read Time</td>
<td>Set Time CnkB</td>
<td>(unused)</td>
<td>TPCData.02*</td>
<td>TPCData.09*</td>
</tr>
<tr>
<td></td>
<td>Dma Ch 2 Request *</td>
<td>Clear Time</td>
<td>Set Time CnkC</td>
<td>(unused)</td>
<td>TPCData.03*</td>
<td>TPCData.10*</td>
</tr>
<tr>
<td></td>
<td>Select Drive 1</td>
<td>Set Time</td>
<td>Set Time CnkD</td>
<td>(unused)</td>
<td>TPCData.04*</td>
<td>TPCData.11*</td>
</tr>
<tr>
<td>0 = MSB</td>
<td>* temporarily, later</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 = LSB</td>
<td>Select Drive 2</td>
<td></td>
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### Read Registers

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Floppy Ext. Status</th>
<th>Misc. Inputs 1</th>
<th>Interrupt Req.</th>
<th>CP Status</th>
<th>TPCHigh</th>
<th>TPCLow</th>
</tr>
</thead>
<tbody>
<tr>
<td>E8</td>
<td>EF</td>
<td>E9</td>
<td>EC</td>
<td>FE</td>
<td>FF</td>
<td></td>
</tr>
<tr>
<td>Bit 0</td>
<td>Disk Change</td>
<td>Alternate Boot</td>
<td>Floppy Req*</td>
<td>CP Attn**</td>
<td>TC.0</td>
<td>TPCData.04*</td>
</tr>
<tr>
<td></td>
<td>Floppy End Count</td>
<td>Serial Time</td>
<td>Keyboard Req*</td>
<td>EmuWake**</td>
<td>TC.1</td>
<td>TPCData.05*</td>
</tr>
<tr>
<td></td>
<td>Two-sided *</td>
<td>Misc. Interrupt</td>
<td>Printer Tx Req*</td>
<td>IOPAttn</td>
<td>TC.2</td>
<td>TPCData.06*</td>
</tr>
<tr>
<td></td>
<td>Floppy ID **</td>
<td>Time 1 sec Req</td>
<td>Printer Rx Req*</td>
<td>CP DmaMode*</td>
<td>TC.3</td>
<td>TPCData.07*</td>
</tr>
<tr>
<td></td>
<td>(unused)</td>
<td>CS ParError*</td>
<td>(unused) *</td>
<td>CP Dma In</td>
<td>TPCData.08*</td>
<td>TPCData.09*</td>
</tr>
<tr>
<td></td>
<td>Mouse Sw 1</td>
<td>(unused)</td>
<td>(unused)</td>
<td>CP Int. Req.</td>
<td>TPCData.01*</td>
<td>TPCData.10*</td>
</tr>
<tr>
<td></td>
<td>Mouse Sw 2</td>
<td>(LSEP UART Tx*)</td>
<td>(LSEP UART Rx*)</td>
<td>CP Out Int. Req.</td>
<td>TPCData.02*</td>
<td>TPCData.11*</td>
</tr>
<tr>
<td></td>
<td>Mouse Sw 3</td>
<td>(LSEP UART Rx*)</td>
<td>CP Dma Compl.</td>
<td>TPCData.03*</td>
<td>TPCData.11*</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. LSI devices control and status registers not shown here.
2. All numbers are decimal, except where indicated otherwise.
3. Single quote after name indicates active low value, e.g. TPCData.00'

---

XEROX SDD
Project: Dandelion
1/O Processor: 1/O Control and Status Registers
File: DandIOP72.slx
Designer: Ogus
Rev: 1
Date: 4/22/80
Page: 72
CP IOP Task Programming

IOP Control Register

IOPCTL = in any cycle

This register controls the mode of the IOP interface.
When disabled, EmuWake or IOPAttn will cause task wakeup.
Input mode, input data full will cause task wakeup.
output mode, output data empty will cause task wakeup.
always wake mode, wakeup always active.

CPAttn causes a service request to the IOP.
Emu Wake should be set by the emulator when task wakeup is required.

Note: Emu Wake should be set by the emulator in one click by a read-modify-write.

IOP Status Register

→ IOPStatus in any cycle

IOP Req
WakeMode.1'
WakeMode.0'
CP Attn'
Emu Wake'
IOP Attn
OO always
(unused)

IOPIData Register

→ IOPIData in any cycle

Input data
(unused)

IOPOData Register

IOPOData = in any cycle

Output data
(unused)

Programming Notes.

1. IOP port can be used on a polling or wakeup basis. The kernel task can use the port with the polling method.
The IOP task uses the wakeup method.

2. Polling Method.
Poll IOP Request in IOP Status to determine when to transfer data.
After writing IOP Control, IOPReq is not valid in the next cycle.
I.e. IOPCTL = k .c. {Write Control register}
Noop .c. {IOPReq NOT valid in this instruction}
R ← IOPStatus .c. {IOPReq now valid in IOPStatus}
After reading or writing data, IOPReq is not valid for 3 cycles.
I.e. IOPOData ← R .c. {Write output data}
Noop .c. {IOPReq NOT valid in this instruction}
Noop .c. {IOPReq NOT valid in this instruction}
Noop .c. {IOPReq NOT valid in this instruction}
R ← IOPStatus .c. {IOPReq now valid in IOPStatus}

3. Wakeup method.
When in input or output mode, the transfer of data will cause the task wakeup to be removed.
The wakeup will be re-asserted when the appropriate data conditions are true again (see IOPControl above)
<table>
<thead>
<tr>
<th>Item No.</th>
<th>Drawing Title</th>
<th>Drawing No.</th>
<th>No. Req.</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
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<td><strong>i8085A</strong></td>
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<td>Intel microprocessor</td>
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<td></td>
<td><strong>i8257-5</strong> (Alt: AMD 9517-4)</td>
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<td>Dma controller</td>
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<td>UART</td>
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<td><strong>i8253-5</strong></td>
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<td>Timer</td>
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<td>Western Digital Floppy Disk controller</td>
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<td><strong>i2114L</strong></td>
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<td>low power 2114, 450 nsec 1k x 4 RAM</td>
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<td>or Am25LS2569</td>
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<td>Capacitor</td>
<td>1000 pF, 25 V</td>
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<td></td>
</tr>
<tr>
<td>Capacitor</td>
<td>1.0 uF, 10 uF, 39 uF, 25V</td>
<td>1 ea.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor</td>
<td>.1 uF bypass, 25V</td>
<td>1 per 3 chip positions</td>
<td></td>
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</tr>
<tr>
<td>Capacitor</td>
<td>15 uF, 25V</td>
<td>2</td>
<td></td>
<td>VDD, VFF bypass</td>
</tr>
<tr>
<td>Resistor</td>
<td>4.7 ohm, 1/2 watt</td>
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<td>Stitchweld version only</td>
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<td>1 ea.</td>
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</tr>
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<td>1. CPU</td>
<td>DandIOP01.sil</td>
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<td>2. PROM, memory control</td>
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<td>3. 4K RAM memory Banks 0 - 3</td>
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<td>6. I/O Data Bus control</td>
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<td>8. Floppy Disk Controller</td>
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<td>13. Dma Test register</td>
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<td>15. CP control, Control store</td>
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<td>18. Keyboard Interface</td>
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<td>19. Mouse Interface</td>
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<td>22. Printer Interface</td>
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<td>24. 4K RAM memory Banks 12 - 15</td>
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# Dandelion I/O Processor

## Documentation Drawings

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<th>File</th>
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<td>DandIOP00.silx</td>
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<td>0a. Drawings - Documentation</td>
<td>DandIOP00a.silx</td>
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<td>0b. Revision History</td>
<td>DandIOP00b.silx</td>
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<td>0c. Design Notes</td>
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### Block Diagrams:

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<td>0e. IOP Control</td>
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<td>0f. Floppy Disk Controller Block Diagram</td>
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<td>30.</td>
<td>Timing: Cpu-FDC</td>
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<td>31.</td>
<td>Timing: Cpu-Mem</td>
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<td>32.</td>
<td>Timing: Dma-FDC</td>
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<td>IOP-CP Communication</td>
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<td>Alto-IOP Communication - 1</td>
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<td>FDC Write Comp. Timing</td>
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<td>Signal Loading - 2</td>
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### Addressing:

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<td>50.</td>
<td>I/O Processor Address space - Memory</td>
<td>DandIOP50.silx</td>
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<td>I/O Processor Address space - I/O</td>
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### Construction:

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<td>Keyboard Cable</td>
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<td>56.</td>
<td>Floppy Disk Signal Cable, Misc. cable</td>
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<td>61.</td>
<td>Board layout</td>
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Dandelion I/O Processor

Revision History

Rev. A to Rev. B

1. Signals on A and B ports of LS245 (g11) switched to account for correct sense of CpuS1 signal. (T = A to B) (pg. 1)
2. Enable (pin 1) of LS240 connected to GND. (pg. 1)
3. Prom macro changed for I2716 (h12), to reverse data bus connection. (pg. 2)
4. Ports PA, PB, and data bus reversed on I8255A (j9) with macro change. (pg. 5).

Rev. B to Rev. C

1. DMA controller added (pg. 7).
2. Floppy Disk controller added (pgs. 8-12).
3. New bus organization (see page 00c).
4. Address space change, to allow both memory or normal I/O mapping. IPAddr.00 on e8, f8, pin 14 (pg. 1).
5. IPDataOut signal (c6b, pin 9, pg. 1).
6. CPUReady signal to insert wait state for FDC, and DMA (slave). (pg. 6)
7. Change in generation of IPMemRd^t, IPMemWr^t, IPIORd^t, IPIOWr^t. This removes the LS257 to avoid the output glitches which occur when device goes from tristate to active. (Gary Miller, Intel, 987-8086, 6/20/79) (pg. 1).
8. New I/O address decoding (pg. 5)

Rev. C to Rev. D

Bug Fixes

1. Added inverters for CpuRd^t, CpuWr^t, DmaMemRd^t, DmaMemWr^t, DmaOHrd^t, and DmaOWr^t and replaced LS253 with LS353 to fix multiplexer glitch when S2, S1 lines change. (page 1)
2. Fixed pullups for FloppyIntReq, FDCVFOen^t (I6, page 6).
3. Removed boot switch backplane signal (pg. 6).
4. Buffered FDCHld.d (page 8).
5. IPRest^t now clears FloppyDataReq and FloppyEndCount (page 8).
6. HDLd one-shot: e2a.1 to GND (page 10).
7. InUse signal to drive removed (drive can be jumpered), FDCTG43 and DiskChange signals added (page 11).

Additions

1. CP control and control store read/write, TPC/TC read and TPC write added (page 15).
2. Backplane connections added.

Rev. D to Rev. E (10/25/79)

Bug Fixes

1. LS353 inputs to GND instead of Vcc (page 1)
2. Pullup for FDCDataReq.

Additions/Changes

1. Reorganization of bus structure. Two I/O data busses, IPData (TTL) and IPAData (MOS). This is due to loading reasons for the MOS devices.
2. Added CP Port, keyboard, Mouse interfaces, Printer, maintenance panel, time-of-day clock interface.
3. Increase Pm to 4K, RAM to 16K.
3. Alto module moved off IOP board.
Dandelion I/O Processor

Design Notes

General
1. Rev E appears to have space for RS232-C DTE.

CPU
1. See notes on memory address space.
2. Mem, I/O Rd'/Wr' decoding changed to avoid LS257 potential glitching.

Floppy Disk Controller
1. WD1791 chip used temporarily. Eventually will use 1797 or 1793-01.
   This has the following effects:
   - Inverted data bus - compensate in software.
   - No VF0E signal available (dummy one generated) for separator.
   - Side Select signal generated by Floppy Control register.
   - DMA worst case timing in DMA write: 1791 and 2114 has write setup time problem.
     1793-01/51 with 2114, or 1791 with 2114-3 OK. (see page 32)
   Current plan is to upgrade to use 1793-01 and not take advantage of the extra 179/ features.
     1797 can be plugged into same position.
2. Need 1 wait state with FDC chips and full-speed 8085A
3. Need FloppyDataReq latch when using 8257 DMA controller.
4. Floppy EndCount latch implemented to check correct DMA completion. Could be removed if not needed.
5. Floppy status register implemented to read external Floppy status. FloppyIntReq is in
   a common INTReq register.
6. Write compensation: Note jitter characteristics. Could use delay line or WD2143 if not tolerable.
   Currently a Disable write comp. in control register. Later,
   DisableWDComp' = ([DDen or TG43)' & EnableWDComp]
7. WriteCurrent signal not provided for drive (from TG43). Supplied in Rev. D
8. FD cable is wired to provide ID bit to determine presence of drive.
9. Select Drive 2 and Select Troy mode signals available.
10. Read Separator synchronizer has only one stage. When next rebloating Prom add a second stage (D0-Q0 of LS273).
   Feed DataSync' through LS273, Q0 to 1791 RDData', Prom should expect complement of RDData.

DMA controller
1. Wait state required in slave mode.
2. Use extended write.
3. Intel 8257 chip used currently. Later could use 8237 controller.
   This provides programmable single byte transfer (see FloppyDataeq latch above).
4. Fully buffered address, control, and data buses.
5. Dma Test register added to channel 2 to allow Dma testing. The Dma Req is temporarily taken from Floppy State Register,
   using signal SelFloppyDrive2.
6. DmaTest register temporarily uses the whole of I/O bank 1b addresses.
7. DAC0' and DACK1' are fully loaded (80 uA, 1.6 mA)
Address Bus Latch

CPU

Rd', Wr'

CpuAddr

CpuAD

LS373

DmaCycle'

LS245

DmaAddr

IPAddrLo

LS373

DmaData

IPAddrHI

LS04

IPMemRd'

IPMemWr'

IPIORd'

IPIOWr'

LS241

DmaCycle'

DmaMemRd'

DmaMemWr'

DmalORd'

DmalOWr'

CpuRd'

CpuWr'

MUX

Select

DmaCycle

IPAddr[0]
I/O Processor Floppy Disk Controller

Block Diagram

Controller

Write Precompensation

Drive driver/receivers

Data

CPU/Dma Control

Miscellaneous control/status

To Drive

Read Data Separator

LS245

IPData

LS273

IPData

Floppy State Register

LS241

IPData

Floppy Status (External)
Note: RST 6 is for Mouse Halt from Alto
RST 5 is for Attention from CP

CPU data bus

Note: CpuO/M' replaced by IAddr.00.
See note on Address space.
I/O Control

(Depends on Addr[0] = Addr[8], etc. for I/O. IPAddr[0] = 1 for I/O addresses.)

I/O Device selector

(Bank 0 - addresses 80H - 09FH)

I/O Control

(Bank 2a)

SelControlStore'

(Q0')

SelRegBlk'

(Q1')

Bank 3

SelICmp(34)

(SelControlStore' )

I/O Device selector

(Bank 2b)

(Q0')

SelRegBlk'

(Q1')

Bank 1b

SelDma'

(SelRegBlk' )

Note: Bank 3B is temporarily used by SelDmaTest'

I/O Device selector

(Bank 2 and Bank 3)

(Bank 2b and Bank 3)

(I/O addresses each)

(16 registers each)

SelRegBlk'

IPAdrr.12

(I/O addresses each)

IPAdrr.09

IPAdrr.08

IPAdrr.07

IPAdrr.06

IPAdrr.05

IPAdrr.04

IPAdrr.03

IPAdrr.02

IPAdrr.01

IPAdrr.00

IPAdrr.11

IPAdrr.12

IPAdrr.13

IPAdrr.09

IPAdrr.08

IPAdrr.07

IPAdrr.06

IPAdrr.05

IPAdrr.04

IPAdrr.03

IPAdrr.02

IPAdrr.01

IPAdrr.00

IPAdrr.11

IPAdrr.12

IPAdrr.13

IPAdrr.09

IPAdrr.08

IPAdrr.07

IPAdrr.06

IPAdrr.05

IPAdrr.04

IPAdrr.03

IPAdrr.02

IPAdrr.01

IPAdrr.00

LS138 111

LS138 b11

LS138 c11

LS138 d11

LS138 h11

Single Register Block

(Bank 3a, registers B-15, addresses OEH - 0EFH)

Memory Control

PROM Bank Selector

(Addresses Bank 0: 0 - 7FFH,
Bank 1: 800H - OFFFFH,
Bank 2: 1000H - 17FFFH,
Bank 3: 1800H - 1FFFFH)

RAM Bank Selector

(Addresses 2000H - 3FFFFH, 8K)

(Addresses 4000H - 5FFFFH, 8K)
Note: Do not use DMA memory addresses in the I/O Address space.
Phase Jitter = 62.5 ns (+/- 31.25 ns)
Precompensation = 187.5 ns +/- jitter
WriteData Pulse width = 187.5 ns
(See DandIOP39.silx for timing)

Note: e4 (S74), f3 (S374), g5 (S02) must be Schottky.
Floppy Disk Controller Clock generator

Motorola Clock 16.000 MHz

Head Load Delay

$T = 40 \text{ ms}$

Pullups, 150, .25W

Miscellaneous Floppy Controller discrete components
(20 pin platform)

(Note: Still need to have FDld pulld up)
Note 1: Active high if two sided diskette is installed on SA 850
Note 2: 37 pin female connector (D-series), bottom connection.
   For correct placement, add 150 to pin number.
Note 3: For cable documentation see SA 850 OEM manual
Raw Read Data synchronizer and pulse shaper

Double density selection

Separator State Machine

Note: Data Window is always high order state bit.

1K x 8 Prom state machine
DMA Test Register

For testing Dma controller independently of Floppy disk.
Can be removed later.

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<td>18</td>
<td>07</td>
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CK  OC'  LS374

DmaTestWr'  DmaTestRd'

(Dma select)
(Dma select)
(Cpu select)

DmaTestAck'

S101DmaTest'

S101DmaTest'

PIQWR'

PIQWR'

PIQWR'

LS32

a10b

6

5

4

DmaTestRd'

XEROX

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<tr>
<th>Project</th>
<th>I/O Processor</th>
<th>File</th>
<th>Designer</th>
<th>Rev</th>
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<td>DMA Test</td>
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<td>Ogus</td>
<td>E</td>
<td>10/24/79</td>
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Interrupt Request Register

FloppyIntReq → 2
   c12a (FloppyIntReq')
   IPData.00

KBItr' → 4
   c12b (Keyboard Request)
   IPData.01

PrinterTxRdy → 6
   c12c (Printer transmitter Request')
   IPData.02

PrinterRxRdy → 8
   c12d (Printer receiver Request')
   IPData.03

ReadIntReg' →
   c12i
   EN'
   LS240
   1

TODInt' → 17
   c12e (TODInterrupt)
   IPData.04

   c12f
   c12g
   c12h

This register contains the interrupt requests of various devices.
Keyboard Data

From KB connector

ReadKB' latches data from KB
ReadKBData' reads it into CPU

Pullup/pulldown resistors

Keyboard cable connector
(2 16-pin DIP connectors)
(23 signals, +5V, GND)

16-pin Plat #

1  MouseXB'
2  KBTone' (conn)
3  MouseYB'
4  GND
5  MouseSw2'
6  MouseSw1'
7  GND
8  a1

16-pin Plat #

1  FPLAT
2  P1
3  P2
4  P3
5  P4
6  P5
7  P6
8  P7
9  P8
10  P9
11  P10
12  P11
13  P12
14  P13
15  P14
16  P15
17  P16
18  P17
19  P18
20  VCC

N75115

Ref
1
E
2
Resp
3

N265

1  a2a
2  To KB Connector

13
14
15

N265

a2d
To KB Connector

KBIntr'

SKY/a

+Term

1

KBSet'

KBData.7'

KBData.6'

KBData.5'

KBData.4'

KBData.3'

KBData.2'

KBData.1'

From KB connector

KBData.0'

KBData.0"'

KBData.1"'

KBData.2"'

KBData.3"'

KBData.4"'

KBData.5"'

KBData.6"'

KBData.7"'

PLAT

1  FPLAT
2  P1
3  P2
4  P3
5  P4
6  P5
7  P6
8  P7
9  P8
10  P9
11  P10
12  P11
13  P12
14  P13
15  P14
16  P15
17  P16
18  P17
19  P18
20  VCC

MouseXA'

MouseYA'

MouseXA'

MouseYA'

MouseXA'

MouseYA'

MouseXA'

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Cable connection to Maintenance panel

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<tr>
<th>(To MP)</th>
<th>DipCable</th>
<th>16</th>
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<th>VCC</th>
<th>(To MP - Dandelion + 5V)</th>
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<td>IncMPPanel'</td>
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<td>P16</td>
<td>(From MP)</td>
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<td>(To MP)</td>
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<td>P2</td>
<td>P15</td>
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<td>P11</td>
<td>ReadClk'</td>
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<td>ReadTime'</td>
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<td>TimeData'</td>
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<td>(To MP)</td>
<td>GND</td>
<td>9</td>
<td>P8</td>
<td></td>
<td>SetCikC'</td>
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<tr>
<td>(To MP)</td>
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<td>(Dandelion signal ground)</td>
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Miscellaneous control 1

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<th>LS174</th>
<th>3</th>
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<th>Q1</th>
<th>00</th>
<th>(Latches KB data)</th>
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<td>IPEndata.04</td>
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<td>IPEndata.06</td>
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<td>IPEndata.07</td>
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<td>Q5</td>
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<tr>
<td>CK</td>
<td></td>
<td>11</td>
<td>C1</td>
<td>b1</td>
<td>19</td>
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<td>GND</td>
<td></td>
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</tbody>
</table>

Miscellaneous Clocks 1

Note: The TOD control must be inactive at Boot.
Note: We can't drive TOD inputs with LS174 or LS175 due to outputs being clamped to ground on power down.

Time-of-Day 1 second interrupt

Procedure to read time:
- Wait for TODIntr to be set
- When set, clear and wait for it to be set again
- read time
  (maximum delay = 2 seconds)

Alternative:
- clear TODIntr (If being set will not be cleared)
- wait until set
- read time
  (maximum delay = 1 second)
Note: Connector labels correspond to the Printer signals.

Note: Due to a design shortcoming, the RD' and WR' lines of the 8253-5 must be externally qualified.

Baud-rate generator

25 pin female connector located on top edge of board. Add 300 to pin number for proper placement.

Baud-rate oscillator (1.8432 MHz)
CPU - I/O Timing: Floppy Disk Controller (1 wait state)
ALTO-DANDELION Communication via Umbilical

**Alto Operations**

**Output:**

![Diagram of UTILOUT (177016B)]

- **UTILOUT (177016B)**
  - Used for logic analyzer interface
  - Select Input Nibble
    - 0: High nibble
    - 1: Low nibble
  - Miscellaneous control (TBD)
  - Alto ACK
  - Alto REQ

**Sequence of Output operation:**
- Output data to UTILOUT
- Alto Request (Set AltoREQ = 1) (UTILOUT[0])
- Read Dandelion ACK
  - DandelionACK = 1 means data received.
- Remove Alto Request (Set AltoREQ = 0)
- Read Dandelion ACK
  - DandelionACK = 0 means data accepted.

**Input:**

![Diagram of UTILIN (177030B)]

- **UTILIN (177030B)**
  - Data
  - Unused
  - Dandelion ACK
    - 1: Data received in Dandelion buffer
    - 0: Data removed from Dandelion buffer
  - Dandelion REQ'
    - 1: No data available
    - 0: Data available

**Sequence of Input Operation:**
- Poll Dandelion REQ (UTILIN[4])
  - DandelionREQ' = 0 means data is available.
- Set SelectInputNibble = 0 (UTILOUT[7])
- Read high data nibble (UTILIN[0:3])
- Set SelectInputNibble = 1 (UTILOUT[7])
- Read low data nibble (UTILIN[0:3])
- Alto Acknowledge (Set AltoACK = 1)
- Poll Dandelion REQ'
  - DandelionREQ' = 1 means ACK has been received.
- Remove Alto Acknowledge (Set AltoACK = 0)
ALTO-DANDELION Communication via Umbilical

Timing Diagrams (not to scale)

Alto to Dandelion:

- **Alto Output Data**
- **AltoREQ**
- **DandelionACK**

8085 Internal Signals:

- **8085Read’**
- **8085Interrupt**

Dandelion to Alto:

- **DandelionREQ’**
- **AltoACK**
- **Alto Input Data**

8085 Internal Signals:

- **8085Write’**
- **8085Interrupt**
Dandelion I/O Processor Floppy Disk Controller

WritePre-compensation Timing Circuit
(See DandIOP09.sil for circuit)

FDCWrData

WDL

LatchHold
EarlyHold

Synchronizer delay (jitter): +/- 31.25 ns

WDS

WDEarly

b

WDLCIr (c)

\text{earWDL'}

WDNorm

e

f

WDLate

Floppy 16MHz

Phase Jitter = +/- 31.25 ns
Precompensation = 187.5 ns +/- Jitter
WriteData Pulse width = 187.5 ns
### IPData Loads

<table>
<thead>
<tr>
<th>Page</th>
<th>Chip</th>
<th>Position</th>
<th>High (μA)</th>
<th>Low (μA) (in, trl)</th>
<th>Drive:</th>
</tr>
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<tbody>
<tr>
<td>6</td>
<td>LS245 (bi)</td>
<td>g11</td>
<td>20</td>
<td>200, 20</td>
<td>15000 24000</td>
</tr>
<tr>
<td>8</td>
<td>LS273 (in)</td>
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<tr>
<td>14</td>
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<td>16</td>
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<td>18</td>
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<tr>
<td>19</td>
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<td>20</td>
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<td>20</td>
<td>LS374 (in)</td>
<td>b5</td>
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<td>400</td>
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</tbody>
</table>

**Backplane**
- LS241 (in) 20 200
- LS241 (in) 20 200
- LS374 (in) 20 400
- LS251 (out) 20 0, 20 (trl) Drive: 2600 8000

---

**Notes:**
- Fixed input loads
- 340 2810 LS245 drive, all other bi or out are tristate
- 3010 LS245 Input

---

### IPAData Loads

<table>
<thead>
<tr>
<th>Page</th>
<th>Chip</th>
<th>Position</th>
<th>High (μA)</th>
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<td>15000 24000</td>
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<td>LS257 (bi)</td>
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<td>10</td>
<td>150 1600</td>
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<tr>
<td>7</td>
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<tr>
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<tr>
<td>22</td>
<td>LS251A (bi)</td>
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<td>10</td>
<td>400 2200</td>
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<tr>
<td>22</td>
<td>LS253-5 (bi)</td>
<td>a8</td>
<td>10</td>
<td>10</td>
<td>400 2200</td>
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</tbody>
</table>

---

**Notes:**
- 100 460 LS245 drive, other LS245 tristate
- 100 640 LS245 drive, other LS245 input
- 100 660 Mos drive, one LS245 input, 1 LS245 tristate
### IPAddr Loads

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<thead>
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<th>Chip</th>
<th>Position</th>
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<th>Drive</th>
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<tr>
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<td>3,4</td>
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<td>160</td>
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<td>(16 chips)</td>
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**Skiplane**

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<th>Low (µA) (in, trl)</th>
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### CpuAD bus loading

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<tr>
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<td>80</td>
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</tr>
<tr>
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<td>I2114 (bl)</td>
<td>a,b,c,d,e,f,g15,16</td>
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<td>80</td>
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<td>Drive: 1000 2100</td>
</tr>
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<td>IPAddr.14,15 only</td>
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<td></td>
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<td></td>
<td></td>
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<td>260 1000 8085, 2114, or 2716 drive</td>
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</tbody>
</table>

---

**XEROX SDD**

**Project**

**I/O Processor**

**Signal Loading - 2**

**File**

**DandlOP41.silx**

**Designer**

**Ogus**

**Rev**

**Date**

**Page**

**10/22/79**

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<table>
<thead>
<tr>
<th>Page</th>
<th>Chip</th>
<th>Position</th>
<th>High (uA)</th>
<th>Low (uA) (in, tri)</th>
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<tbody>
<tr>
<td>1</td>
<td>LS353 (out)</td>
<td>e9</td>
<td>--</td>
<td>--</td>
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<td>MemRd, MemWr</td>
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<tr>
<td></td>
<td>LS353 (out)</td>
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<tr>
<td></td>
<td>LS508 (in)</td>
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<td>MemRd, MemWr</td>
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<td>LS74 (in) S', R'</td>
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<td>800</td>
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<td>2</td>
<td>I2716 (in)</td>
<td>e, f, g, h12</td>
<td>40</td>
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<td>MemRd</td>
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<td>3,4</td>
<td>I2114 (in)</td>
<td>a-h, 13, 14</td>
<td>160</td>
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<td>MemWr          (16 chips)</td>
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<td>23,24</td>
<td>I2114 (in)</td>
<td>a-h, 15, 16</td>
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<td>MemWr          (16 chips)</td>
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<tr>
<td>5</td>
<td>LS138 (in)</td>
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<td>6</td>
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<td>7</td>
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<td>8</td>
<td>WD1791 (in)</td>
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<td>14</td>
<td>LS32 (in)</td>
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<td>15</td>
<td>LS138 (in)</td>
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<td>20</td>
<td>400</td>
<td></td>
<td>IOWr</td>
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<tr>
<td></td>
<td>LS32 (in)</td>
<td>h19</td>
<td>20</td>
<td>400</td>
<td></td>
<td>IORd</td>
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<td>16</td>
<td>LS32 (in)</td>
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<td>21</td>
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<td>IORd, IOWr</td>
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<td>22</td>
<td>I8251A (in)</td>
<td>j9</td>
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<td>IORd, IOWr</td>
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<tr>
<td></td>
<td>I8253-5 (in)</td>
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<td>10</td>
<td></td>
<td>IORd, IOWr</td>
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</table>

|                  |               |          | 60        | 440   | IPMemRd'      |
|                  |               |          | 340       | 720   | IPMemWr'      |
|                  |               |          | 200       | 3040  | IPIORd'       |
|                  |               |          | 200       | 3040  | IPIOWr'       |

Drive: 2600 8000
Drive: 2600 8000
Dandelion I/O Processor Address Space

Normal memory address space

<table>
<thead>
<tr>
<th>Bank</th>
<th>Type</th>
<th>Address Range (Hex)</th>
<th>Addr[1:2]</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>PROM</td>
<td>0 - 7FF (2K)</td>
<td>0</td>
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<tr>
<td>1</td>
<td>PROM</td>
<td>800 - 0FFF (2K)</td>
<td>0</td>
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<tr>
<td>2</td>
<td>PROM</td>
<td>1000 - 17FF (2K)</td>
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<td>3</td>
<td>PROM</td>
<td>1800 - 1FFF (2K)</td>
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<tr>
<td>0</td>
<td>RAM</td>
<td>2000 - 23FF (1K)</td>
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<tr>
<td>1</td>
<td>RAM</td>
<td>2400 - 27FF (1K)</td>
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</tr>
<tr>
<td>2</td>
<td>RAM</td>
<td>2800 - 2BFF (1K)</td>
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</tr>
<tr>
<td>3</td>
<td>RAM</td>
<td>2C00 - 2FFF (1K)</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>RAM</td>
<td>3000 - 33FF (1K)</td>
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<tr>
<td>5</td>
<td>RAM</td>
<td>3400 - 37FF (1K)</td>
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<td>RAM</td>
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<tr>
<td>7</td>
<td>RAM</td>
<td>3C00 - 3FFF (1K)</td>
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<tr>
<td>0</td>
<td>RAM</td>
<td>4000 - 43FF (1K)</td>
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<tr>
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<td>RAM</td>
<td>4400 - 47FF (1K)</td>
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<tr>
<td>2</td>
<td>RAM</td>
<td>4800 - 4BFF (1K)</td>
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<td>3</td>
<td>RAM</td>
<td>4C00 - 4FFF (1K)</td>
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<tr>
<td>4</td>
<td>RAM</td>
<td>5000 - 53FF (1K)</td>
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<tr>
<td>5</td>
<td>RAM</td>
<td>5400 - 57FF (1K)</td>
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<td>6</td>
<td>RAM</td>
<td>5800 - 5BFF (1K)</td>
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</tr>
<tr>
<td>7</td>
<td>RAM</td>
<td>5C00 - 5FFF (1K)</td>
<td>2</td>
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</table>
## Dandelion I/O Processor Address Space

### I/O Address Space

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Bank</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>0a</td>
</tr>
<tr>
<td>81</td>
<td>0a</td>
</tr>
<tr>
<td>82</td>
<td>0a</td>
</tr>
<tr>
<td>83</td>
<td>0a</td>
</tr>
<tr>
<td>84</td>
<td>0a</td>
</tr>
<tr>
<td>85</td>
<td>0a</td>
</tr>
<tr>
<td>86</td>
<td>0a</td>
</tr>
<tr>
<td>87</td>
<td>0a</td>
</tr>
<tr>
<td>0E8</td>
<td>3a</td>
</tr>
<tr>
<td>0E9</td>
<td>3a</td>
</tr>
<tr>
<td>88</td>
<td>0a</td>
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<tr>
<td>89</td>
<td>0a</td>
</tr>
<tr>
<td>8A, 8B</td>
<td>0a</td>
</tr>
<tr>
<td>8C</td>
<td>0a</td>
</tr>
<tr>
<td>8D</td>
<td>0a</td>
</tr>
<tr>
<td>8E</td>
<td>0a</td>
</tr>
<tr>
<td>8F</td>
<td>0a</td>
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### I/O Bank select

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Bank</th>
</tr>
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<tbody>
<tr>
<td>Dma 8257</td>
<td>1b</td>
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<tr>
<td>OB0</td>
<td>1b</td>
</tr>
<tr>
<td>OB1</td>
<td>1b</td>
</tr>
<tr>
<td>OB2</td>
<td>1b</td>
</tr>
<tr>
<td>OB3</td>
<td>1b</td>
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<tr>
<td>OB4</td>
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<tr>
<td>OB5</td>
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<tr>
<td>OB6</td>
<td>1b</td>
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<tr>
<td>OB7</td>
<td>1b</td>
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<tr>
<td>OB8</td>
<td>1b</td>
</tr>
<tr>
<td>OB9 - 0BF</td>
<td>1b</td>
</tr>
<tr>
<td>0FO</td>
<td>3b</td>
</tr>
<tr>
<td>0F1 - 0FF</td>
<td>3b</td>
</tr>
</tbody>
</table>

### Notes:
1. I/O Ports can be reached using:
   - IN or OUT instructions using port address:
     \[ P = 80H + p, \text{where } 0 \leq p \leq 7FH \leq 128 \]
   - Memory reference instructions using address:
     \[ A = 8000H + P, \text{where } P \text{ is given above.} \]
   - Note that bit 8 being 1 is not required by the hardware.

### Addresses (hex):

#### Bank 0
- Bank 0a
- Bank 0b
- Bank 1a
- Bank 1b
- Bank 2a
- Bank 2b
- Bank 3a
- Bank 3b

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Bank</th>
</tr>
</thead>
<tbody>
<tr>
<td>2a</td>
<td>(Unavailable for Read)</td>
</tr>
<tr>
<td>2a</td>
<td>TPC High (Addr, High 5 bits data) (W)</td>
</tr>
<tr>
<td>2a</td>
<td>TPC Low (Low 7 bits data) (W)</td>
</tr>
<tr>
<td>2a</td>
<td>TPC[4:1] (W)</td>
</tr>
<tr>
<td>2a</td>
<td>Control Store Byte 0 (R, W)</td>
</tr>
<tr>
<td>2a</td>
<td>Control Store Byte 1 (R, W)</td>
</tr>
<tr>
<td>2a</td>
<td>Control Store Byte 2 (R, W)</td>
</tr>
<tr>
<td>2a</td>
<td>Control Store Byte 3 (R, W)</td>
</tr>
<tr>
<td>2a</td>
<td>Control Store Byte 4 (R, W)</td>
</tr>
<tr>
<td>2a</td>
<td>Control Store Byte 5 (R, W)</td>
</tr>
<tr>
<td>3a</td>
<td>Interrupt Request register (read)</td>
</tr>
<tr>
<td>3a</td>
<td>Keyboard data (read)</td>
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<tr>
<td>3a</td>
<td>CPin (read)</td>
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<tr>
<td>3a</td>
<td>CPStatus (read)</td>
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<tr>
<td>3a</td>
<td>Mouse X (read)</td>
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<tr>
<td>3a</td>
<td>Mouse Y (read)</td>
</tr>
<tr>
<td>3a</td>
<td>Misc Inputs 1 (read)</td>
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<tr>
<td>3a</td>
<td>Clocks 1 (write)</td>
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<tr>
<td>3a</td>
<td>TOD interrupt (clear)</td>
</tr>
<tr>
<td>3a</td>
<td>COMOut (write)</td>
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<tr>
<td>3a</td>
<td>Central processor Control (write)</td>
</tr>
<tr>
<td>3a</td>
<td>Mouse XY (clear)</td>
</tr>
<tr>
<td>3a</td>
<td>CP Dma Complete (clear)</td>
</tr>
<tr>
<td>3a</td>
<td>Control 1 (write)</td>
</tr>
</tbody>
</table>
Clock i10
Crystal Clock in 14 pin package right-aligned as shown.

Motorola K1114A clock or equiv. 5.88 MHz (temp)

FPLAT i9
Miscellaneous components
16 pin platform
Left aligned as shown.
Resistors 1/4 watt, 5%

FPLAT e10
10K pullup resistors
16 pin package left-aligned as shown.
Allen-Bradley 316A 103 or equivalent
FPLAT b2
Pullup/pulldown resistors
16 pin package right aligned as shown.
Allen-Bradley 316E131211
or equivalent

R1 = 130 ohms, R2 = 210 ohms

FPLAT f2
Pullup resistors for
Floppy drive signals,
Head Load one-shot discretes
20-pin platform
Resistors 1/4 watt, 5%

Clocks I5, a5
Floppy Controller Clock
Baud Rate Generator Clock
Crystal Clock in 14 pin
package right-aligned as shown.
Motorola K1114A
16 MHz, 1.8432 MHz

FPLAT a1, b1 : Keyboard Cable
DipSocket c2: Maintenance Panel Cable
FPLAT d2: Alto Control Cable
**I/O Processor Keyboard Cable**

*Interim stitchweld board arrangement*

---

### Signal Table

<table>
<thead>
<tr>
<th>Signal</th>
<th>IOP Connector pin</th>
<th>Keyboard Connector pin</th>
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<tbody>
<tr>
<td></td>
<td>Platform a1</td>
<td>Platform b1</td>
</tr>
<tr>
<td></td>
<td>23 signals, +5V, GND</td>
<td>30-pin D-series</td>
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<tr>
<td>KBDATA.0</td>
<td>-</td>
<td>3</td>
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<tr>
<td>KBDATA.1</td>
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<td>8</td>
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<td>KBDATA.2</td>
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<tr>
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<td>+5V</td>
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<td>16</td>
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<tr>
<td>GND</td>
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<td>-</td>
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</tbody>
</table>

*No cable connection: 2, 4, 5, 12, 13, 13, 17, 18, 35, 36, 37, 38, 44*

Note: On Platform a1, connect a 390 ohm resistor between pin 3 and 14
FLOPPY CONTROLLER
COMPONENT SIDE VIEW
BOTTOM 37 PIN
FEMALE CONNECTOR

17 twisted pairs
1 jumper (2 pins)

Note: On Edge J1, even numbers are on component side of board, odd numbers on non-component side

IOP to Alto control cable

IOP - Alto control
18-wires
18-pin platform
18-pin platform

One-to-One connection between 2 18-pin platforms

IOP-Maintenance Panel cable

IOP - Maintenance Panel
18-wires
16-pin DIP connector
16-pin DIP connector

One-to-One connection between 2 16-pin DIP connectors

---

XEROX
Project
Dandelion
I/O Processor
Floppy Disk Signal Cable
Misc. cables

File
DandIOP56.silx

Designer
Ogus

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I/O Processor

Floppy Disk Cabling

Bottom connector
37 pin female D-series

16 twisted pairs, shield, jumper
37 pin male D-series

(See pin description on page 26)

P1 J1
Signal lines

P4 J4
AC Power

P4 Pins
1. 115 V AC
2. Frame Ground
3. 115 V Return

P5 J5
DC Power

P5 Pins
1. +24 V DC
2. +24 V Return
3. -12 V Return
4. -12 V DC
5. +5 V DC
6. +5 V Return

Note: configure for -7 to -16 V DC option

Note: See SA 850 OEM manual, pages 17, 18, 19, 20 for details of connectors.
Note: • indicates where capacitors have to be removed and pin inserted. Coordinate of pin 1 of large chips is indicated.

I/O Connector (25 pin female)  I/O Connector (37 pin female)