# High Speed Input/Output Board

## Logic Drawings

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## Other Documentation

This file is in:  
- [Iris] <Workstation> HSIO<Pr>SIO-R.dm  
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All logic drawings in Press format

All design Automation info about HSIO board

Wirelist for this rev of HSIO board

Disk Documentation in Sil and Bravo formats

All Disk Documentation in Press format

Disk Prom Programs

Display Documentation drawings, Timing Diagrams

All Display Logic, Timing diagrams in Press format

Display Prom Programs

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**XEROX SDD**

**Project:** Dandelion  
**Reference:** High Speed I/O Board  
**File:** sHSIO00.sil  
**Designer:** Crane, Davies  
**Rev:** R  
**Date:** 10/22/80  
**Page:** 0
Note: The prefix #% in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitch weld card. The suffix l prevents route from attempting automatic terminator assignment since DO stitch weld card has none defined. Subnet wiring order for a net is done by appending to the net name a 1 followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of l as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.
EndLine goes low once per horizontal line.
DCASDly' is DCAS delayed by 20 ns.
Read signal goes low for 20 ns before low data byte is latched by the shift register.

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DCAS' increments counters. State machine generates EndRdRead when the allotted number of accesses for the mix of page and full accesses has been reached for a given round (4 clicks out of 6). Page/Full 'goes low whenever the conditions for a full access are met.

When the word counter reaches 63, it resets to 0 and the InhibitRead signal is asserted, which prevents the Read Machine from restarting until it is reset by ClrDataFifo'.

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XEROX
Project: WS
Read Machine: Word Counter & End Conditions
File: sHSIO27.sil
Designer: Crane
Rev: R
Date: 10/22/80
Page: 27
Common gate input to this 10124 is connected to InhibitRead'.

Full is set during last tick if next access is a full access.

Full7: 11
Full6: 7
Full5: 3
Full4: 1
Full3: 0

LCAS-LCAS Counter

RAS' output changes at or before end of tick7.

PD/P Goes high during click4 cycle 3
Changes 25-45ns after 51 MHz cycle boundary at end of tick7

PD/P

EndRndRead' 7
Goes low during last access of round.

Common gate input to this 10124 is connected to InhibitRead'.

Terminators are shown on the clock page.
This is a platform of discretes used to filter the video, Hsync and Vsync signals.

The connector is a 15 pin Female D connector located on the bottom edge of the card. The pin numbers shown are the actual pin number + 750.

These RDIV16's are being used as ECL terminators, so their power connections must change to reflect ECL conventions.
Buffer X bus to reduce loading.

Video

Video'

This is used to test the video lines being sent to the monitor

Most other resistors used on HSIO62.sil
Termination Packages A, B, C, D, E above are 100 ohm termination to -2 V
Allen-Bradley part no. 316E161261
Pin 16 on each termination package is connected to GND and Pin 8 to VEE (-5.2 V). This is done on pWSD09.sil and sWSD09.sil where there is more room. This connection makes the termination compatible with normal ECL power rules.

Note: The prefix % in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweld card.
The suffix ! prevents Route from attempting automatic terminator assignment since DO stitchweld card has none defined. Subnet wiring order for a net is done by appending to the net name a ! followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.
Using an S74 instead of the LS273 speeds up WordBoundary', so it will change before the RawCRCError indicator from the 8041 CRC Checker. This allows us to latch the CRCError signal directly using WordBoundary'. The RawCRCError signal is too slow to latch into the Word Status buffer register using NRZClock'. There is then a race between WordBoundary' and RawCRCError after NRZClock rises. Using the faster S74 here ensures WordBoundary' wins.
The inputs to the encoder must be synchronized to its clock. They arrive too late for the PROM if read directly.

When ReduceW is true, pre-compensation should be enabled (inner tracks).

Although inputs D3 and D7 are never chosen, they are attached to prevent decoder glitches on switching.
DiskWriteData

SMFMWriteData

SA1000/SA4000

UWriteEnable

DiskOutputCk

HeadsSelect1

HeadsSelect2

HeadsSelect4

HeadsSelect8

HeadsSelect16

ReduceIW

DirectionIn

Step

FaultClear

DriveSelect

DWriteEnable is delayed 5 bit times to let Pre-comp shift reg clear out at end of write operation.

DWriteEnable

RawOverflow

IOPreset

BTransferEnable

UWriteEnable

The use of UWriteEnable prevents a race between WriteGate and ReadGate. If BWriteEnable were used, there would be a race between BTransferEnable and BWriteEnable when finishing a write op that could glitch ReadGate, causing a WriteFault. Since BTransferEnable is faster than UWriteEnable, there is a ~ 20 ns glitch in ReadGate at the beginning of a Write Op. This causes NRZClock to pause, but only temporarily.

XEROX SOD

Project

Dandelion

Dandelion Disk Controller

Disk Output Buffers, Drivers

File

sHSIO53.sil

Designer

Davies

Rev

R

Date

10/22/80

Page

53
This is a Beckman RPack number 886-6-R220/330.

SeekComplete'
Track00'
Index'
Ready'
WriteFault'
Sector'
RawSA1/SA4'

RDIV16
RD1 = VCC
RD2 RD14
RD3 RD13
RD4 RD12
RD5 RD11
RD6 RD10
RD7 RD9
RD8 GND

PrinterReq'
Pull this up so display request will work even if Options board is unplugged.

SeekComplete'
Track00'
Index'
Ready'
WriteFault'
Sector'

SA1SkComplete
SA00
SA1000'/SA4000'
HalfCik

HalfCik is a 25.5 MHz clock generated in the CLOCK section of the display. It is divided by three here to produce a 117 ns clock to run the disk.

DiskReadCik

Show Reference clock to PLL during Seek Operations so it cannot drift out of lock.

DiskWriteData

Note the delayed version of the input data is used. This is because it is the properly 180 degrees out of phase with the DriveFMClock. It lags inputdata by 50 ns.

DelInputData

DriveFMClock

We note that AdvExit.4 ceases to be active when TransferEnable drops. A clock is needed to start a write operation, so SA1NRZClock is set to the always active SA1WNRZClock as soon as WriteEnable goes active. To ensure the DWriteEnable shift register delay is cleared, we keep SA1NRZClock set to SA1WNRZClock until DWriteEnable goes low.
The SA4000's SeekComplete is delayed by 25 Sector pulses, to make sure of at least 28 sectors. This gives a 20 ms delay for the heads to settle.

SyncClkFlags

Index

SyncClkFlags

RetFMFClock

Test1

DiskReadClk

DiskReadClk

SA1NRZClock

SyncSA4Data

AddrMkCnt2

SA1000/SA4000'
The 50 pin cable to the SA1000 drive has been reduced 10 37 lines so the 37 pin connector on the stichewd board may be used. The connector on the stichewd board is a 37 pin female in the TOP position. Its pins are numbered 101-137. Signals not referenced on the drive's 50 pin cable are not connected to the stichewd board.

In addition, GND to pins 1, 23, 25, 27, 29, 31 and 45 of 50 conductor cable.

Breaks in consecutive numbering.

The 16 pin data cable is installed in a DIP socket.

These termination resistors are mounted in the unused holes of 20 pin sockets holding 14 pin chips. They are each 51 ohms.