High Speed Input/Output Board

Logic Drawings

HSIO Board
1. HSIO0 - this page
2. phHSIO1 - drawings of fuses
3. HSIO02.sily - Display controller parts list
4. HSIO03.sily - Display controller parts list
5. HSIO04.sily - Disk controller parts list
6. HSIO05.sily - Disk controller parts list
7. HSIO06.sily - Stichweld layout
8. HSIO07.sily - proposed PWB layout

Display Controller
1. HSIO22 - 51 MHz Clock Dividers and ECL Terminators
2. HSIO23 - Cycles, Clocks and Display counter
3. HSIO24 - Display Output Machine and Control register
4. HSIO25 - Data FIFO and Barrier Register
5. HSIO26 - Control FIFO Data Path
6. HSIO27 - Read Machine: Word Counter & End Conditions
7. HSIO28 - LCAS & LMAS: Generation
8. lplhsHSIO29 - Discretes, Connectors

Disk Controller
8. HSIO47 - Control and Write Data registers
9. HSIO48 - Status / Test Multiplexer, ReadData Register
10. HSIO49 - Service Request, Overrun and Word Status Buffer
11. HSIO50 - Serializer / DeSerializer
12. HSIO51 - Field / Word Machine
13. HSIO52 - MFM Encoding, Pre-compensation and Address Mark Gen.
14. HSIO53 - Disk Output Buffers and Drivers
15. HSIO54 - Logic for Phase Decoder
16. HSIO55 - Disk Input Buffers and Receivers
17. HSIO56 - Miscellaneous Input Clocks and Multiplexing
18. HSIO57 - Data Separator and Address Mark Detection
19. HSIO58 - Input Muxplexer
20. shHSIO59 - Disk Cables Connections for Stichweld card
21. phHSIO59 - DiskCables. Terminators for PWB card
22. shHSIO60 - Discrete Phase Decoder Oscillator. Stichweld version
23. phHSIO60 - Discrete Phase Decoder Oscillator. PWB version
24. shHSIO61 - Discrete Phase comparator. Stichweld Version
25. phHSIO61 - Discrete Phase comparator. PWB version

Other Documentation
This file is in:
[Iris]<Workstation>HSIO:HSIO-R.wi


[Iris]<Workstation>HSIO:S2D-Rev-C.ShowDm
[Iris]<Workstation>HSIO:S2D-Rev-C.Drn
[Iris]<Workstation>HSIO:S2D-Rev-C.pris
[Iris]<Workstation>HSIO:S2D-Rev-C.pris


All logic drawings in Press format
All design Information about HSIO board
Wirelist for this rev of HSIO board
Disk Documentation in Sil and Bravo formats
All Disk Documentation in Press format
Disk Prom Programs
Display Documentation drawings. Timing Diagrams
All Display Logic, Timing diagrams in Press format
Display Prom Programs
Note: The prefix % in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweald card.
The suffix ! prevents Route from attempting automatic terminator assignment since DO stitchweald card has none defined.
Subnet wiring order for a net is done by appending to the net name a ! followed by the wiring sequence number of the node in the net.
Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.
The scheduling prom on the CP looks at this signal to decide whether to give the Ethernet/Disk click to the Ethernet or to the Disk. GND > Ethernet all the time since this disk controller cannot lower its service request in time to stop two services from one service request.

Click is 51MHz + 15nS
51 MHz + 25 nS

Display PROM Counter
Counts from 46 to 255

Package Count
.75 S241
.75 S02
.33 S04
.25 LS163
DCAS' increments counters. State machine generates EndRndRead when the allotted number of accesses for the mix of page and full accesses has been reached for a given round (4 clicks out of 5). Page/Full' goes low whenever the conditions for a full access are met.

When the word counter reaches 63, it resets to 0 and the inhibitRead signal is asserted, which prevents the Read Machine from restarting until it is reset by ClrDataFifo.'
Common gate input to this 10124 is connected to InhibitRead.

Full is set during last tick if next access is a full access.

LRAS-LCAS Counter

RAS' output changes at or before end of tick 7.

PD/P Goes high during click4 cycle 3
Changes 25-45 ns after 51 MHz cycle boundary at end of tick 7

InhibitRead' 6

EndRndRead' 7

Goes low during last access of round.

Common gate input to this 10124 is connected to InhibitRead.

Terminators are shown on the clock page.
This is a platform of discretes used to filter the video, Hsync and VSync signals.

The connector is a 15 pin Female D connector located on the bottom edge of the card. The pin numbers shown are the actual pin number + 750.

These RDIV16's are being used as ECL terminators, so their power connections must change to reflect ECL conventions.
Buffer X bus to reduce loading.

This is used to test the video lines being sent to the monitor.

Most other resistors used on HSIO62.sil
Termination Packages A, B, C, D, E above are 100 ohm termination to -2V
Allen-Bradley part no. 316E161261

Pin 16 on each termination package is connected to GND and Pin 8 to VEE (-5.2 V). This is done on pWS09.sil and sWS09.sil where there is more room. This connection makes the termination compatible with normal ECL power rules.

The prefix # in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweol card.

The suffix ! prevents Route from attempting automatic terminator assignment since Q0 stitchweol card has none defined.

Subnet wiring order for a net is done by appending to the subnet name a! followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of ! as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.

Note:
Using an S74 instead of the LS273 speeds up WordBoundary’, so it will change before the RawCRCError indicator from the 9401 CRC Checker. This allows us to latch the CRCError signal directly using WordBoundary’. The RawCRCError signal is too slow to latch into the Word Status buffer register using NRZClock’. There is then a race between WordBoundary’ and RawCRCError after NRZClock rises. Using the faster S74 here ensures WordBoundary’ wins.
The inputs to the encoder must be synchronized to its clock. They arrive too late for the prom if read directly.

When Reduce1W is true, pre-compensation should be enabled (inner tracks).
The use of UWriteEnable prevents a race between WriteGate' and ReadGate'. If BWriteEnable were used, there would be a race between BTransferEnable and BWriteEnable when finishing a write op that could glitch ReadGate', causing a WriteFault. Since BTransferEnable is faster than UWriteEnable, there is a ~20 ns glitch in ReadGate at the beginning of a Write Op. This causes NDBClock to pause, but only temporarily.
This is a Beckman RPack number 698-5-R220/330.

Pull this up so display request will work even if Options board is unplugged.
Test 1

HaltCk

HaltCk is a 25.5 MHz clock generated in the CLOCKS section of the display. It is divided by three here to produce a 117 ns clock to run the disk.

DiskReadClk

Show Reference clock to PLL during Seek Operations so it cannot drift out of lock.

DiskWriteData

Note the delayed version of the Input Data is used. This is because it is the properly 180 degrees out of phase with the RefMFMclock. It lags InputData by 50 ns.

DelInputData

DriveMFMclock

Test 1

AdmCnt 4

SA1WNRZClock

BWriteEnable

DWriteEnable

while reading or verifying the SA 1000 disk the NRZClock should be derived from the data stream. While writing, it is synchronized with RefMFMclock like the rest of the controller. SA1WNRZclock is produced as part of the TimingClock divider in the Input Multiplexer.

UWriteEnable

We note that AdmCntr 4 ceases to be active when TransferEnable drops. A clock is needed to start a write operation, so SA1NRZClock is set to the always active SA1WNRZClock as soon as WriteEnable goes active. To ensure the DWriteEnable shift register delay is cleared, we keep SA1NRZClock set to SA1WNRZClock until DWriteEnable goes lo.

XEROX

SDD

Project

Dandelion

Dandelion Disk Controller

Misc. Input Clocks and Mux.

File

sHSI056.sil

Designer

Davies

Rev

R

Date

10/22/80

Page

56
The derived NRZ data is supplied on AddrMkCnt.2, the derived NRZClock on AddrMkCnt.4. The clock changes only in the middle of a data bit, not at its end. The Data and clock are not valid until AddrMkFound is.
The SA4000's SeekComplete is delayed by 29 Sector pulses, to make sure of at least 28 sectors. This gives a 20 ms delay for the heads to settle.
The 50 pin cable to the SA1000 drive has been reduced to 37 lines so the 37 pin connector on the stichweld board may be used.

The connector on the stichweld board is a 37 pin female in the TOP position. Its pins are numbered 101-137.

Signals not referenced on the drive's 50 pin cable are not connected to the stichweld board.

---

The 16 pin data cable is installed in a DIP socket.

---

In addition, GND to pins 1, 2, 3, 5, 6, 10, and 11 of the DIP socket.
Most other resistors on this pkg used on dwg HSIO20.sil

RDIV16
RD1 = VCC
RD2 = RD14
RD3 = RD13
RD4 = RD12
RD5 = RD11
RD6 = RD10
RD7 = RD9
=GND RDB98

TstSrvRqPnm’ 1
TstSrvRqPnm’

TstFidWdProm’ 3
TstFidWdProm’

TstEncodePnm’ 5
TstEncodePnm’

TstAddrMkPnm’ 9
TstAddrMkPnm’

TstMFMClock’