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1  2901 CHIPS
2  LOOKAHEAD, SHIFT ENDS, CIN
3  SU
4  RH, STACKP
5  IB
6  XBUS: LROT, RH, ZEROHIGHX
7  XBUS: IB, CONSTANTS, ERRINTSTACKP
8  MIR
9  MIR DECODING I
10 MIR DECODING II
11 DISPATCH/BRANCH
12 PNI A, PTC (BRANCHING)
13 TPC, TC, & LINK
14 SCHEDULE, SWITCH, & TASKS
15 ERROR, EMULATOR, & KERNEL PROMS
16 CLOCKS, WAIT
17 CONTROL STORE A [0-7]
18 CONTROL STORE B [8-15]
19 CONTROL STORE C [16-23]
20 CONTROL STORE D [24-31]
21 CONTROL STORE E [32-39]
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23 CS PARITY (PC) - YEK
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27 PC DISCRETES & NIA
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29 FILTER CAPACITORS
30 TEST POINT LISTING, EDGE CONNECTOR LISTING, SIGNAL LISTING
2901 Carry Lookahead

CIN-SE (48) 13 CIN 9 CIN0-3 1 ti TP001
GND 6 GIO' 11 PageCarry
G4-7' 14 P1' 10 G0' 7
P4-7' 15 P11' CY 5
G8-11' 11 P12' 4
P8-11' 2 P13' 3
G12-15' 3 P14' 2
P12-15' 4 P15' 1

R Shift Ends

CIN-SE (48) 5 X0 7 R.0 1 ti TP003
CIN-SE (48) 4 X1 6 X2 3 X3
R.15 13 Y0 10 Y1 9 Y2 8 Y3
Q.0 12 YO 11 Y1 10 Y2 9 Y3
aD.1 (20) 2 S2 1 S1
Shift' (34) 14 EX' EY'
aD.0 (20) 1 aD.0' (26)

Q Shift Ends

CIN-SE (48) 5 R.15 2 ti TP004
aD.0' (26) 1 S38 6 u57a
CIN-SE (48) 4 aD.0 (20) 1 u57b (57)
aD.1 shift'

0 0 Cout
 0 1 Cin
 1 0 Cin
 1 1 Cin

aD.0 = 0 implies right shift

Cin & Shift Ends

CIN-ps16 (39) 10 CIN-SE 1 ti TP007
ps16' (20) 9 u57c
CIN-ps16X' (34) 13 u57d
CIN-SE-wrSU' (20) 12
If the S189 must be used instead of the 29701, then place S240 between Xbus & S189 inputs.
Timing for HM7649 IBProm:

IBFront - Xbus = (x + 37, x + 36) nS

- x to IBProm-PC.0
- 1A
- SelectB1' to NB
- LS374 setup


Difference between S373 "Data to Q" and "Data to 0" = 18[2] - 13[1] = 6 nS. Data can arrive 6 nS after WriteIB goes high.

In C..
Schedule, Switch, & Tasks

<table>
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<tr>
<th>Nt</th>
<th>Ct</th>
<th>Pt</th>
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<tr>
<td>3-S</td>
<td>3-S</td>
<td>3-S</td>
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<tr>
<td>Previous</td>
<td>Current</td>
<td>Previous</td>
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</table>

**ScheduleProm·RevD**

- EORound
- Click 0 (20)
- Click 1 (20)
- Click 2 (20)
- IOPReq (22)
- EReq (22)
- KReq (22)
- KernReq (20)

- CS' CS'
- F93453 v60

**SwitchProm·RevC**

- C1.0 (30)
- C1.1 (30)
- Nt.0 (77)
- Nt.1 (77)
- Nt.2 (77)
- Cycle 2 (22)
- Wait (61)

- CS' CS'
- F93427 v67

**Tasks**

- Click 0
- Click 1
- Click 2
- Click 3

- Ethernet
- Disk
- IOP
- Ethernet/Disk
- Display/LSEP-Refresh

- LS374 (30)

When Disk = SA4000, Click 3 is Ethernet only.
When Disk = Trident, Click 3 is Ethernet on even rounds and Trident on odd rounds (i.e., 10 click round).
The Display & LSEP-Refresh tasks never both use Click.

**Schedule, Switch, & Tasks**

- Title: SCHEMATIC, CP
- Sheet: 14 of A
Clock Receivers

1. pWaitCLK' 5. AlwaysClk-a
2. v17c 6. (981, 137)
3. v17d 11. AlwaysClk-b
4. v17e 10. (981, 137)
5. AlwaysClk-c

TCWaitc1' (20)

1. WrTCQ (42)
2. S08
3. u87a
4. Cycle2 (22)
5. S00
6. u87b

Cycles

1. Cycle1' (18, 13 typ)
2. S04
3. v17a
4. Cycle2 (18, 13 typ)
5. v17b
6. S04

Qualified Clocks

pAlwaysCLK' (941, 133)

1. Cycles
2. pWaitCLK' 12. Waitc1 (53)
3. AlwaysClk-a (981, 137)
4. WriteTC' 11. S08
5. Cycle2 (22)
6. u87a

Cycle1 (21)

1. S02
2. v63a
3. v63b
4. Cycle3 (37)
5. WriteTPCLow
6. S51
7. u86a

Wait Control

1. IOPWait (34)
2. Cycle1 (22)
3. Disp-Proc' (30)
4. u86b
5. Bank0
6. S374
7. u51e
8. Waitc1' (53)
9. u51f
10. Waitc2' (20)
11. S10
12. Wait

Detects low bank for max 1024K mem.
Control Store E [12-39]
CS Parity (PC) - Yek
The Control Store can be read & written via backplane pins. Once tested, instructions (or parts of instructions), can be loaded in order to test additional features. For instance, all X-bus sources can be disabled by loading a 6 into CS bits 16-23 (controlled by CSWE.c'). Simple programs to test the 2901's can also be executed in this way.

The SU & RH registers can be loaded by controlling EnableSU, CIN-SE-wrSU, & RH~ from a microinstruction.

stackP, IB, High SU Addr, & Low SU Addr can be similarly tested.

The MIR & MIR decoding can be tested by loading instructions into the CS.

The SU & RH registers can be loaded by controlling EnableSU, CIN-SE-wrSU, & RH~ from a microinstruction. stackP, IB, High SU Addr, & Low SU Addr can be similarly tested.

The MIR & MIR decoding can be tested by loading instructions into the CS.

POT-Ybus is used to test devices attached to the Y bus.

POT-A is used to disable registers or Proms whose outputs go to a register clocked by AlwaysClk.

POT-W is similarly used for WaitClk.

POT-Clik & POT-Wait disable the outputs of AlwaysClk & WaitClk'd registers.

The following steps cause a CS byte to be written. It is assumed that the TPC has been written with the required CS address.

\[
\begin{align*}
PDT-Clik & - 1; \ Swc3 & - 1; \quad \text{(cause NIA to come from TPC)} \\
IOPWait & - 1; \\
SwTAddr' & - 0; \ SwTAddr - 1; \quad \text{(init code)} \\
IOPData & - \text{data} \\
CSWE.x' & - 0; \ CSWE.x' - 1;
\end{align*}
\]

If IOPWait is left high, the CP will not execute the instruction which has been loaded into the CS. Instead, the CP will be frozen in a state where the instruction is totally decoded, but the result will no be loaded into any register. Thus, all the microinstruction register (MIR) decoding logic can be tested without even executing an instruction.

The following steps cause the TPC to be written:

\[
\begin{align*}
IOPWait & - 1; \quad \text{(init code)} \\
SwTAddr' & - 0; \ SwTAddr - 1; \\
IOPData & - \text{data or (data rshift5)} \\
WtTPCHigh' & - 0; \ WtTPCHigh' - 1; \\
IOPData & - \text{data & 7F'x;} \\
WtTPCLow & - 0; \ WtTPCLow - 1; \quad \text{write low 7 bits}
\end{align*}
\]

Testability

Testability programs for reading & writing TPC & CS available on [Iris]<Workstation>:/HCardTest.dm
Unused Parts

AlwaysClk

Junk 374 Allocation

S374

g15 - Always Clock

b MAR-
c AllowMDR-
d KernReq'
e WaitC2
f WaitG3
g TCWait
h
i

S374

h16 - Always Clock

b EKTrap2'
c CSPar.4 PC only
d EKTrapc2
e EKErr.0'
f EKErr.1'
g Swc3
h Swc3'
i CSPar.5 PC only

LS374

h17 - Wait Clock

b iBPtr.0
c iBPtr.1
d CSParErr
e Mesalnt
f StackErr
g VirAddErrc2
h pc16'
i MemErrc3

LS374

u51l  CK OC

WaitClk

PDT-Clk

PDT-Wait

S374

u51l  CK OC

S374

u38l  CK OC

S374

u26l  CK OC

S374

u40c  CK OC

S374

u40d  CK OC

Unused parts, S374 clocks
NOTE: C1-C65, CAP., CERAM, 50V, .10UF, PART NO. 702W05218

Filter Capacitors

XEROX  PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS
TITLE  SCHEMATIC, CP
SIZE  A4
REV.  A

DWG  DWG NO. 156P11673
Sheet  29 OF A
Comments:

2) The last item on lines below, preceded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.
3) Line with no page number was a continuation of the previous line.

#TP001 .11 CIN-3 ;02 #TP052 .11 TPC.7' ;13
#TP002 .11 PageCross ;02 #TP053 .11 TPC.8' ;13
#TP003 .11 R.0 ;02 #TP054 .11 TPC.9' ;13
#TP004 .11 R.15 ;02 #TP055 .11 TPC.10' ;13
#TP005 .11 Q.0 ;02 #TP056 .11 TPC.11' ;13
#TP006 .11 Q.15 ;02 #TP057 .11 plink.0' ;13
#TP007 .11 CIN-SE ;02 #TP058 .11 plink.1' ;13
#TP008 .11 IB.0 ;06 #TP059 .11 plink.2' ;13
#TP009 .11 IB.1 ;06 #TP060 .11 plink.3' ;13
#TP010 .11 IB.2 ;06 #TP061 .11 TCY.0 ;13
#TP011 .11 IB.3 ;06 #TP062 .11 TCY.1 ;13
#TP012 .11 IB.7 ;06 #TP063 .11 TCY.2 ;13
#TP013 .11 IB.6 ;06 #TP064 .11 TCY.3 ;13
#TP014 .11 IB.5 ;06 #TP065 .11 Ct.0 ;14
#TP015 .11 IB.4 ;06 #TP066 .11 Ct.1 ;14
#TP016 .11 IBFront- ;05 #TP067 .11 Ct.2 ;14
#TP017 .11 GoodIBDisp2 ;06 #TP068 .11 Ct=Emu ;14
#TP018 .11 RefillIntc2 ;06 #TP069 .11 Pt=Emu ;14
#TP019 .11 SelectIB0' ;06 #TP070 .11 Nt.0 ;14
#TP020 .11 pIBPtr.0 ;06 #TP071 .11 Nt.1 ;14
#TP021 .11 pIBPtr.1 ;06 #TP072 .11 Nt.2 ;14
#TP022 .11 SelectIB1' ;06 #TP073 .11 Nt=Emu ;14
#TP023 .11 MAR- ;08 #TP074 .11 Swc2' ;14
#TP024 .11 DispBr.0' ;11 #TP075 .11 Swc2' ;14
#TP025 .11 DispBr.1' ;11 #TP076 .11 pCSPE ;15
#TP026 .11 DispBr.2' ;11 #TP077 .11 pMI ;15
#TP027 .11 DispBr.3A' ;11 #TP078 .11 MesaInt ;15
#TP028 .11 DispBr.3B' ;11 #TP079 .11 EKTrapc2' ;15
#TP029 .11 pNIA.0 ;12 #TP080 .11 EKTrapc2 ;15
#TP030 .11 pNIA.1 ;12 #TP081 .11 EKErr.0' ;15
#TP031 .11 pNIA.2 ;12 #TP082 .11 EKErr.1' ;15
#TP032 .11 pNIA.3 ;12 #TP083 .11 pEK' ;15
#TP033 .11 pNIA.4 ;12 #TP084 .11 pEK ;15
#TP034 .11 pNIA.5 ;12 #TP085 .11 pEK0' ;15
#TP035 .11 pNIA.6 ;12 #TP086 .11 pEK1' ;15
#TP036 .11 pNIA.7 ;12 #TP087 .11 pSE ;15
#TP037 .11 pTC.0 ;12 #TP088 .11 pVAE ;15
#TP038 .11 pNIA.8 ;12 #TP089 .11 StackErr ;15
#TP039 .11 pTC.1 ;12 #TP090 .11 VirtAddrErr ;15
#TP040 .11 pNIA.9 ;12 #TP091 .11 pKR ;16
#TP041 .11 pTC.2 ;12 #TP092 .11 pPC16' ;15
#TP042 .11 pNIA.10' ;12 #TP093 .11 KernReq' ;16
#TP043 .11 pTC.3 ;12 #TP094 .11 pc16' ;15
#TP044 .11 pNIA.11' ;12 #TP095 .11 prA.0 ;17
#TP045 .11 pNIA.12 ;13 #TP096 .11 prA.1 ;17
#TP046 .11 TPC.0 ;13 #TP097 .11 prA.2 ;17
#TP047 .11 TPC.1 ;13 #TP098 .11 prA.3 ;17
#TP048 .11 TPC.2 ;13 #TP099 .11 prB.0 ;17
#TP049 .11 TPC.3 ;13 #TP100 .11 prB.1 ;17
#TP050 .11 TPC.4 ;13 #TP101 .11 prB.2 ;17
#TP051 .11 TPC.6' ;13 #TP102 .11 prB.3 ;17
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CSParErr: u39.17i

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CSWE.f': u47.8i ;22
CSWE.f': u17.8i ;22
CSWE.f': u32.8i ;22
CSWE.f': u64.8i ;22
CSWE.f': v61.50i ;24

CSWE.a': v19.8i ;17
CSWE.a': v06.8i ;17
CSWE.a': u99.8i ;17
CSWE.a': u75.8i ;17
CSWE.a': u42.8i ;17
CSWE.a': u69.8i ;17
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CSWE.b': v20.8i ;18
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CSWE.c': v21.8i ;19
CSWE.c': v07.8i ;19
CSWE.c': u77.8i ;19
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CSWE.d': v22.8i ;20
CSWE.d': v08.8i ;20
CSWE.d': u78.8i ;20
CSWE.d': u92.8i ;20
CSWE.d': u62.8i ;20
CSWE.d': u45.8i ;20
CSWE.d': u15.8i ;20
CSWE.d': u30.8i ;20
CSWE.d': v61.12o ;24

CSWE.e': v23.8i ;21
CSWE.e': u93.8i ;21
CSWE.e': u93.8i ;21
CSWE.e': v09.8i ;21
CSWE.e': u79.8i ;21
CSWE.e': u46.8i ;21
CSWE.e': u63.8i ;21
CSWE.e': u31.8i ;21
CSWE.e': u16.8i ;21
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CSWE.f': u94.8i ;22
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<td>#TP089.1i, u55.12o</td>
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