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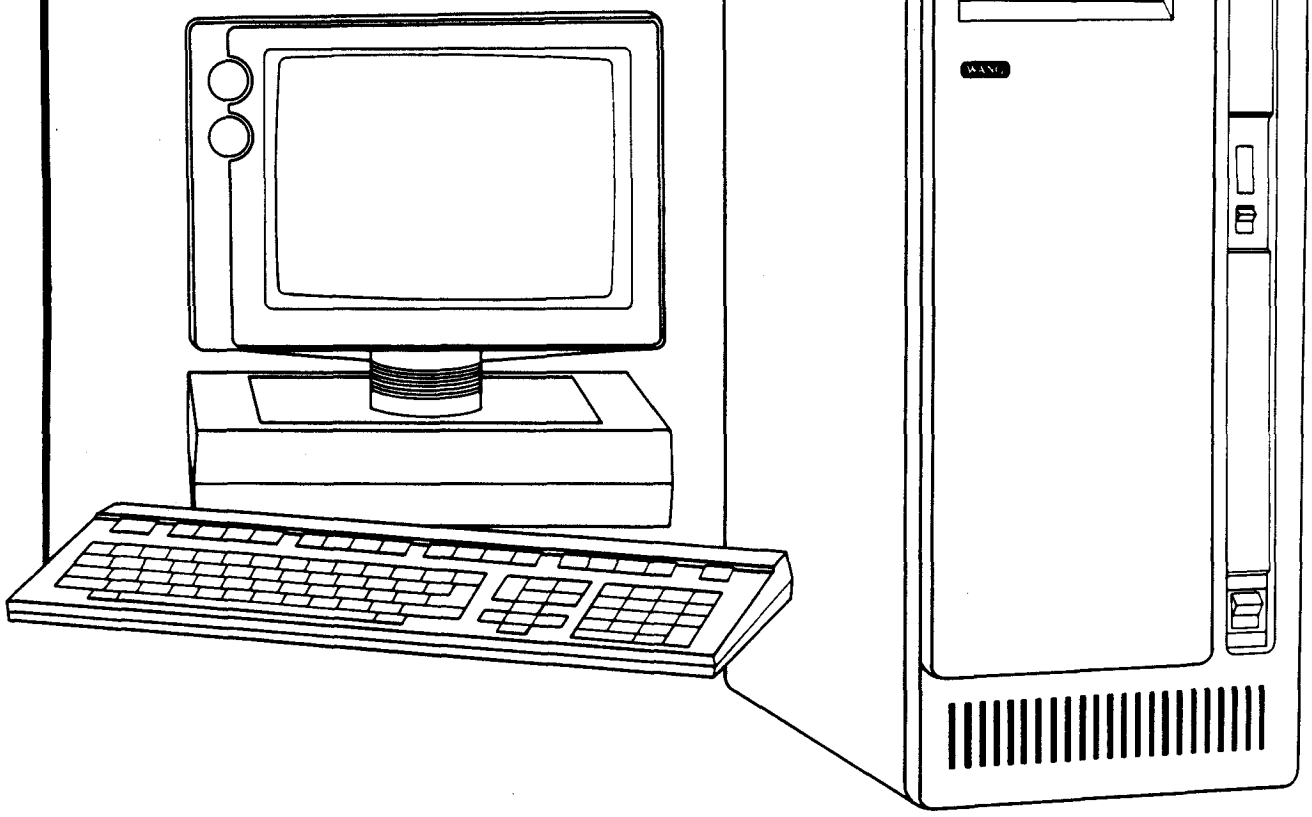
OIS 40/50/60

BOARD REPAIR WORKBOOK VOLUME 2



CUSTOMER ENGINEERING
TRAINING AND DOCUMENTATION

741-9041

WANG

CUSTOMER ENGINEERING TRAINING CENTER

OIS 40/50/60
BOARD REPAIR WORKBOOK VOLUME 2

PREFACE

This document is intended to be used for TRAINING PURPOSES only. The material contained in this document, while accurate during the developement of this workbook, may not reflect the latest developments or changes to the OIS 40/50/60 system.

TECHNICAL SUPPORT DOCUMENTS

OIS 50 INTERNAL PRINTER CONTROLLER HARDWARE SPECIFICATIONS HM-60
OIS 40/50 RESOURCE MANAGEMENT UNIT THEORY OF OPERATION 751-0902
OIS 40/50 RESOURCE CONTROL UNIT THEORY OF OPERATION 751-0911
OIS 40/50 IWS FULL MATRIX CONTROLLER SPECIFICATION HM-67
WL-2630 OIS/VS COLLECTIVE GATE ARRAY SPECIFICATION HM-37
OIS-50 INTERNAL WISE SPECIFICATION REVISION 3 HM-85
OFFICE INFORMATION SYSTEMS OIS 40/50/60 741-1267
OIS SYSTEM ADMINISTRATION GUIDE 700-5562E

First Edition - December, 1985

OUTLINE OF WORKBOOK

	SECTION #	TITLE
VOLUME 1		
	1.	Introduction to System
	2.	Resource Management Unit (RMU)
	3.	Resource Control Unit (RCU)
	4.	Internal Workstation Controller (IWS)
	5.	Appendices (A-E)
VOLUME 2		
	6.	Internal Printer Controller (IPC)
	7.	Internal WISE Controller (IWISE)
	8.	Diagnostics
	9.	Appendices (F-K)

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SECTION 6
INTERNAL PRINTER CONTROLLER (IPC)

SECTION 6
Internal Printer Controller (IPC)

6.1 INTRODUCTION

The Internal Printer Controller, commonaly called the IPC board is designed to control one printer through a modified RS232C serial interface. This board is comprised of four sections.

1. 50BUS Interface
2. Z80A Microprocessor
3. 64K Bytes of Memory
4. RS-232C Interface

The 50BUS interface provides the communication link between the RCU and the Z80A of the IPC. Through this bus, commands and data are transfered to the IPC. This interface is similiar to the 50BUS interface of the other boards in the OIS 40/50/60 system.

The onboard Z80A of the IPC receives instructions and data from the RCU and then goes about transfering the data to the printer through the RS-232C interface. One of the Z80A's responsablities is to monitor the performance of the printer while transferring data to the interface when requested. If a malfuntion should happen the Z80A is informed and it in turn notifies the system of the problem.

In order to increase the speed of the system and reduce the number of transfer operations, the IPC contains 64K of Dynamic RAM. This memory holds the operating codes for the onboard Z80A along with the data to be printed.

The heart of the IPC is the RS-232C interface. This interface consises of a SC2661C Enhanced Programmable Communication Interface (EPCI). The SC2661C is a universal sychronous/asychronous data communication controller chip that provides all the timing and control signals for transfers of data over the RS-232C connector. The onboard Z80A programs the SC2661C upon power up for asynchronous transmition with the proper start/stop and data bits, along with the selected Baud rate. The SC2661C then performs the parallel to serial conversion and inserts the proper number of start and stop bits. At the complection of each byte transfer the SC2661C will inform the onboard Z80A that the next byte can be loaded and status of the current operation can be read through the internal status register of the EPCI.

A block diagram of the IPC showing the four major components, there interconnections with the printer and the OIS 40/50/60 system, is shown in FIGURE 6.1-1. Each of the four section will be described in detail in the following pages.

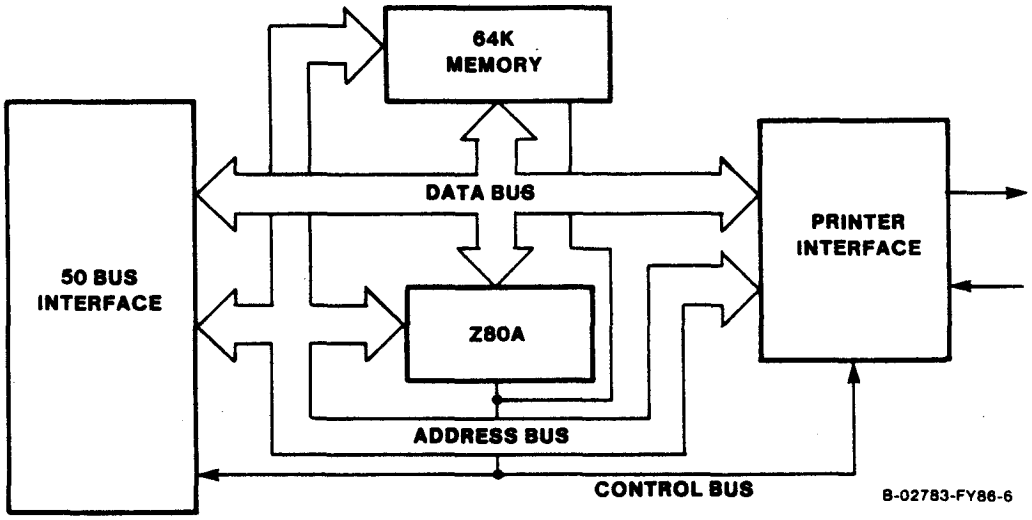

FIGURE 6.1-1
Internal Printer Controller (IPC) Block Diagram

6.2 50BUS Interface

The 50BUS provides a means of communication between the onboard Z80A CPU and the RCU board of the system. When the RCU desires to communicate with the IPC it first generates a BUS REQUEST. Upon receiving this request the onboard Z80A deactivates its busses after the complection of the current instruction, and allows the RCU access to the onboard memory and status registers. This bus request is generated by a combination of the &50BSLCT and &50BUSRQ signal. Both signals are feed through buffer L99 (1A10) to OR gate L74. When both signals are active L74 produces &IPCBSRQ to the Z80A. The Z80A will acknowledge this request by activating pin 23 &BUSAK, thus driving its Data, Address, and Control busses to a tristated condition. &BUSAK is also used to select the 50BUS Address Bus buffers, hence alowing the RCU access. The RCU will then place the appropiate address on the bus and perform the desired transfer operation. The information that the RCU transfers to or from the IPC could be in the form of either data or instructions for the IPC or it could be status information from the IPC. A detailed description of the 50BUS signals and there fuction is given in Sections 3.4.3 and 3.4.4 of Volume 1.

6.3 Z80A Microprocessor

The Z80A of the IPC board has two major tasks to perform. First, upon power up of the system it must receives program instructions from the RCU and then configure the SC2661C chip. Once this has been done the Z80A is responisable for transfering data to the SC2661C for transmition to the printer, and monitoring the status of the printer. The basic structure of the suport chips for the Z80A is the same as the rest of the circuit boards in the OIS 40/50/60 system. The Z80A is driven by a 4Mhz clock supplied by a crystal and associated circuits. If you drsire further information on the structure of the Z80A suport circuits refer to the appropiate section of either the RMU or the IWS controller.

6.3.1 NOP Generation

When the system is first powered on, each of the controller boards must be IPLed. Since each board receives different code and the system can not load all of the boards at the same time each board must be placed in a hold type state until it can be IPLed. This hold state is a function of the NOP generator. When the power is first applied to the system the RCU generates a master reset signal to all boards. This master reset signal known as &MRC is buffered through L99 (1A10) where it is places on the clock input of flipflop L37 (1A8). The "D" input of L37 has +5VDC applied to it via R1. On the trailing edge of &MRC L37 will set causing &NGON to be generated. &NGON will enable data buffer L52 (1B7). The "A" inputs of L52 are all tied to +5VDC, and once L52 is enabled the "Y" outputs will all go low. As you can see from the schematics these outputs are tied diresctly to the Z80A's data bus.

When the &MRC signal was sent to all the boards, the Z80A of the IPC board was placed in a reset state, which caused it to enter into a M1 cycle. During a M1 cycle the Z80A fetches an instruction from the data bus, this instruction is HØØ generated by the NOP generator. A NOP instruction causes the Z80A to perform continuous M1 cycles. When the Z80A is perfroming a NOP instruction the program counter incerments one step for each NOP perfromed. But the Data bus is held at all zero so the Z80A continues to perfrom NOPs. When &NGON was generated it was also sent to L106 the status register. Here it asserted the NOT RUNNING bit. The RCU then works its way through the boards on the system and determines which ones need IPLing. When the RCU finds a NOT RUNNING bit set, it will first generate a restart command to the device to clear the NOT RUNNING bit and disable the NOP generator. Then it will down load a jump to location zero instruction at location zero. This keeps the Z80A in a tight loop, thus keeping the PC register from advancing. Then when the RCU find time it will down load the operation instruction to the board, followed by another restart command. At this time the IPC's Z80A can then go about performing the instructions that it was given.

There are two other times that the NOP generator could be involked. The first is if a parity error is detected during a transfer to or from main memory. If this happens the signal PARERR (Parity Error) is generated and sent to L28 (1B10). It passes through L28 and on to the perset input of L37 the NOP flipflop. This PARERR signal is also sent to the status register to inform the RCU that a problem has occured. The second incident that will invoke the NOP generator is if the pwoer on the printer is turned off and the CTS (Clear to Send) signal is lost. If this happens the &POWERON signal will deactivate, this high level signal will then be places on pin 5 of L28 where it will be inverted and sent to the preset input of L37 the NOP generator flipflop. This &POWERON signal is also sent to the status register for the RCU to read. One final note on the NOP generator operation. If the &POWERON signal is not being generated, either by the printer being turned off or the cable being disconnected, the IPC board will not IPL. This problem can be resolved by placing J4 between pins 2 & 3.

NOTE

If you move J4 from pins 1 & 2 so that you can test the board without a printer connected. Then remember to move it back when you are finished with the test.

6.3.2 I/O Operations

The Z80A of the IPC board communicates to the other devices on the board through memory mapped I/O locations. These operation can be divided into two areas;

1. Device Status and Diagnostic Operations
2. SC2661C Operations

Tables 6.3-1 and 6.3-2 provide a brief explanation of each I/O operation.

TYPE	LOCATION	FUNCTION
IN	07	Device Switch 2
IN	08	Device Switch 1
IN	09	Diagnostic Mode Indicator
IN	0A	Resets the SC2661C
IN	0B	Toggles Diagnostic Mode *
IN	0C	Clears Parity Error Flipflop
IN	0D	Toggles Parity Flipflop *

Table 6.3-1
Device and Diagnostic I/O Operations

* Each read from these locations will cause the state of the flipflop to change states. Further explaination of their operation can be found later in this Section.

The folowing table list the operation associated with the I/O locations that corrisponds to the SC2661C (FPCI) chip. The decoding of these locations are within the SC2661C once the chip has been selected. The SC2661C is selected any time that bit 4 of the address bus is high during an I/O operation.

TYPE	LOCATION	FUNCTION
IN	10	Reads Receive Data Holding Register
OUT	11	Writes to Transmit Holding Register
IN	12	Reads the Status Register
OUT	13	Writes to SYN1/SYN2/DLE Registers *
IN	14	Reads Mode Registers MR1/MR2 *
OUT	15	Writes to Mode Registers MR1/MR2 *
IN	16	Reads Command Register
OUT	17	Writes to Command Register

Table 6.3-2
SC2661C I/O Operations

* Each of these I/O locations have multiple registers assigned to them. Internal circuits in the SC2661C keep track of wich register is to be accessed each time a read or write operation occurs for that location. (i.e. If you perform an OUT 13, you will write to the SYN1 register. Then if you perform another OUT 13, you will write to the SYN2 register. When the maximim number of registers for a given location has been reached the internal circuits will recycle to point to the first register.) The register pointers are reset to their start position when either the reset input of the SC2661C is activated or by reading the Command register. A detailed explaination of each of the registers within the SC2661C can be found in Section 6.5.2.

All I/O operation for the IPC board are selected through three LS138 decoders, L30, 31, and 32 located on sheet 1 of the schematics. Each of these decoders need three enabling signals to alow them to operate, G2A, G2B and G1. The G1 and G2B inputs of each are driven from &BM1 and either &BRD or &BIORQ signals respectivaly. The G1 input is an active high input and will be enabled whenever the Z80A is NOT in a M1 machine cycle. Remembering that the M1 machine cycle is an instruction fetch activity. The G2B input of L31 and L30 are driven by the active low signal of &BRD (Buffered Read). When the Z80A is performing a read operation this signal will be driven low, thus activating the G2B input of these decoders. The G2B input of L32 is driven from the &BIORQ (Buffered I/O request) signal of the Z80A. This signal is activated whenever the Z80A performs an I/O instruction. Before I go any futher let's look at FIGURE 6.3-1 to see how these three decoders are wired.

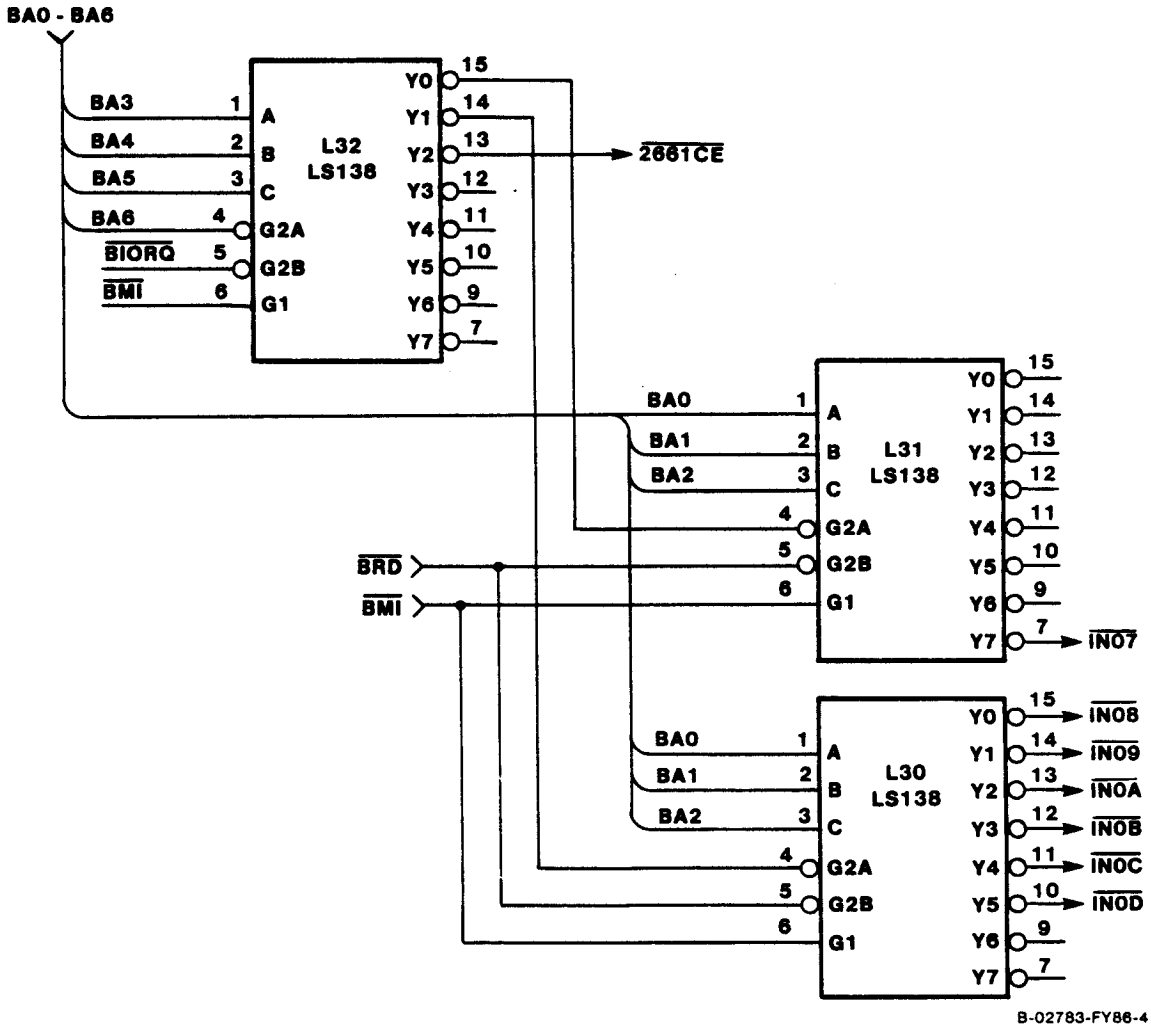

FIGURE 6.3-1
I/O Decoders

The third enable input of both L30 and L31 are driven by one of the outputs of L32. This tells us that L32 must be selected before either L30 or L31 can be enabled. L32 receives it's G2A enable from the BA6 bit of the Address Bus. Whenever this bit is low and the other two enable inputs are activated L32 will decode address bits BA3 - BA5. Only the first three outputs of L32 are used by the IPC board. If BA3 through BA5 are all low then the Y0 output will be driven low. This low out will then enable L31, allowing it to decode BA0 through BA2 of the Address Bus.

The Y1 output of L32, when activated will enable L30, thus allowing it to decode the lower three bits of the Address Bus. Finally when the Y2 output of L32 is active we will select the SC2661. The SC2661 will then decode the lower three bits of the Address Bus.

Let's now take a look at some of the I/O operation and see what functions they perform. The IN07, 08 and 09 operations allow either the system or the onboard Z80A to read the setting of the device switches and the condiction of the Diagnostic Mode Indicator. These three operations are quite simple in that they enable the appropiate buffer, thus placing the contence of the switches or registers on the Data Bus.

The next I/O operation is the IN0A. When the IN0A instruction is performed by the Z80A, L30's Y2 output will be driven low. This high to low transion is inverted and presented to the clock input of flipflop L59 (2B11). The flipflop will set causing the &Q output to go low, generating &WAIT and 2661RST via L58. At the same time the clear input of L57 an LS163 counter is removed. L57 then starts counting. When the QD output goes high on the 8^{th} count flipflop L59 will reset via L67 and L90. This delay is needed to allow the SC2661 time to reset it's internal registers. The &WAIT signal that was generated during this operation was presented to the Z80A placing WAIT states within the instruction cycle.

The IN0B operation allows the system to switch between Normal mode and Diagnostic mode. Each time the IN0B instruction is performed flipflop L35 (1B1) is toggled. When the Normal mode of operation is selected read and write operation to memory occur with even parity. But when the Diagnostic mode of operation is selected read and write operation to memory occur with odd parity. The reason for having odd parity during these transfers is so that the software can check the memory circuits for parity errors.

When a parity error occurs flipflop L59 (3B2) sets, and causes one of two parity error signals to be activated depending on the selected mode of operation. To return this flipflop to the reset condition an IN0C instruction must be preformed. Decoder L30 (1C2) generates IN0C which is gated through AND gate L90 (3B3) to clear flipflop L59.

When the INOD instruction is performed flipflop L89 (2C8) will toggle between Normal parity error responce, and MNI responce. During Normal parity responce, if a parity error occurs the NOP generator is turned on. This causes the Z80A to run in a very tight loop until the problem is recified. For futher information on the NOP generater refer to Section 6.3.1. If the MNI type of resopnce is selected, and a parity error occurs a None Maskable Interrupt will be generated. This type of responce can be used for diagnostic purposes by informing the software that a problem has occured without locking up the micro.

The rest of the I/O operation are all decoded within the SC2661 chip. These operations will be used extencivelly by the Z80A to communicate with the SC2661. The key to these operations is the selection of the SC2661. This is accomplished when BA4 is high and BA3, 5 and 6 are low, and of course the Z80A is performing an I/O operation. When this happens L32 (1F3) generates SC2661CE (2661 chip select). Then the SC2661 decodes the lower three bits of the Address Bus to determine the operation. As I stated before, some of these operations when performed, will selecte different registers within the SC2661 for the same I/O command. It is important to keep track of the number of times a given I/O operation is performed in order to know which register is being accessed. Normally this is done by the software but if during testing the operator tries to read or write to these locations he or she must be aware of the fact that each access will be to a different register. A complete breakdown of the SC2661 operations and commands are descussed in the Section 6.5.

6.4 IPC Memory

The memory of the IPC board consists of nine HM4864-3 64Kx1 memory chips. Eight of these are used for main memory and one for parity. Since these chips are dynamitic they require a 256-row refresh every 2 to 4 Msec. The Z80A provides a 7 bit refresh address at the end of each M1 machine cycle, yielding a total of 128 row addressess. To provide for 256-row addressing a synthetic refresh address bit is multiplexed into the A7R bit of the Z80A Address Bus. The circuits involved in this operation are similar to the ones in the RMU boards.

6.4.1 REFRESH

In a 256-row refresh address operation, the Z80A issues A6 low for the first 128-row refresh and high for the second 128-row refresh. By using this A6 bit as a control input to a "D" type flipflop we can generate a synthetic 256-row refresh address. Referring to FIGURE 6.4-1 and FIGURE 6.4-2 we see the four flipflops that provide this operation. Flipflop L60-1 and L60-2 are used to toggle the synthetic refresh bit while flipflop L51 switches between the synthetic bit and the normal A7 bit, and L43-2 signals the start of refresh.

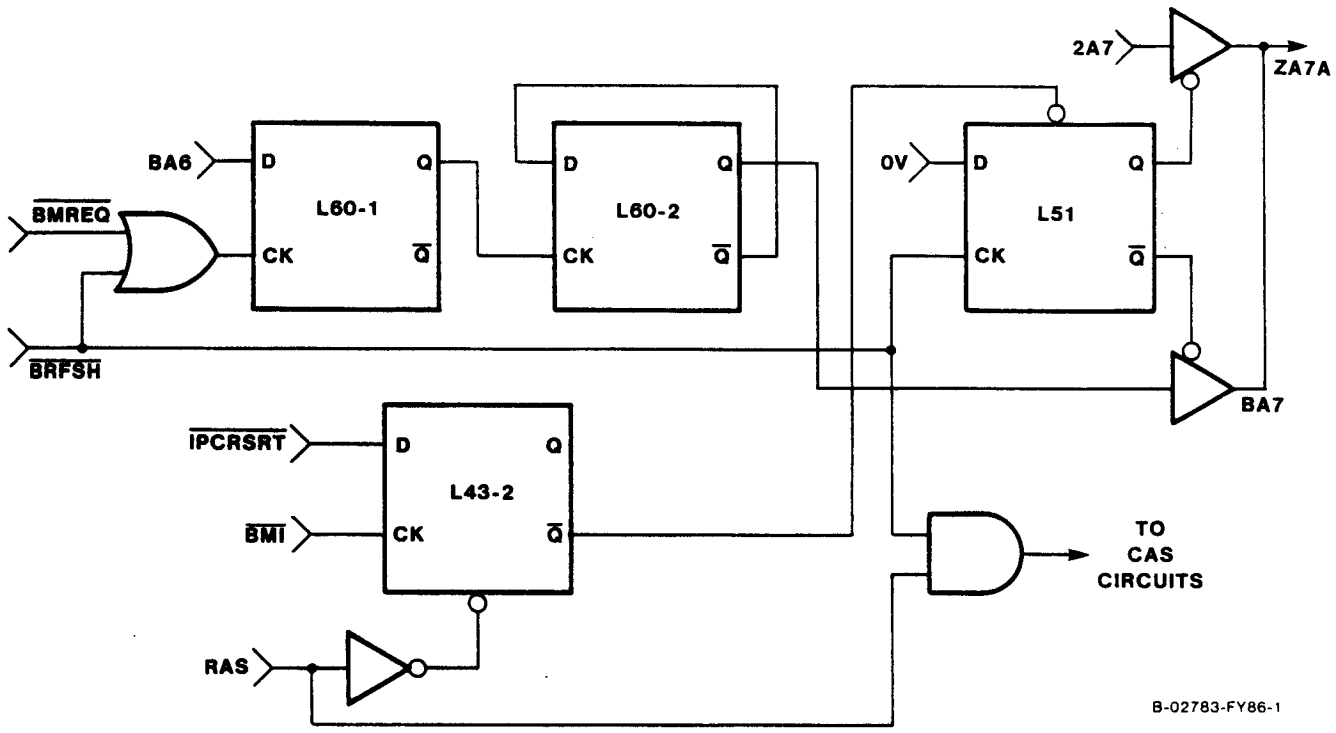

FIGURE 6.4-1
REFRESH LOGIC DIAGRAM

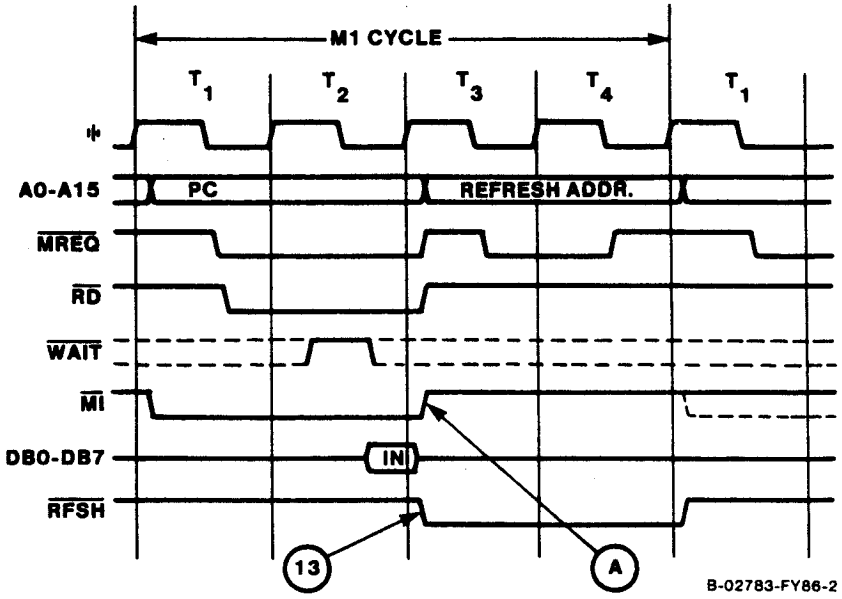

FIGURE 6.4-2
M1 Timing Diagram

Flipflop L51 is normally in a reset state, this enables driver L68 to pass the ZA7 bit from the Z80A to the Address Buss buffer L62. Halfway through the M1 machine cycle &BM1 will deactivate (Refer to FIGURE 6.4-2 Point A) Causing flipflop L43 to set, thus generating Early Refresh (ERFSH) from the "&Q" output. Early Refresh is placed on the preset input of L51, causing it to set and switching the ZA7A output from ZA7 to BA7. The "Q" output of L43 is passed to the "D" input of L94 where on the next 1/2 phi clock pulse L94 will set starting the RAS cycle.

At the same time that &BM1 went high, &BMREQ went high and &BRFSH went low, signaling the start of the refresh cycle (Refer to FIGURE 6.4-2 Point B). In the middle of T3 time &BMREQ became active again, setting up L60-1. During this time (T3 & T4) the Z80A places the refresh address on the Address Bus. Then sometime during T4 state of M1, &BMREQ deactivates again, clocking flipflop L60-1. The state of the BA6 bit of the Address Bus, which is feeding the "D" input of L60-1, will be transfered through to L60-2. Each time the Z80A presents a refresh address on the bus, it (the Z80A) will toggle the state of BA6. When BA6 is in the high state L60-2 will clock and change the state of the synthetic BA7 bit. Using this techeque, a minium of two M1 machine cycle are required to refresh the full 64K bytes of memory. At the end of the refresh cycle &BRFSH will deactivate, this low to high action clocks L51-1 into a reset state, switching the synthetic BA7 bit out of the circuit.

Remember that during a refresh cycle we only need a RAS cycle. While we are in a refresh cycle, &BRFSH signal is low, hence, AND gate L69 is disqualified, blocking the RAS signal from proceeding.

6.4.2 RAS/CAS

There are three different ways that the RAS/CAS cycle can be started. 1.) Normal read or write request, 2.) Instruction fetch, 3.) Refresh cycle. Of these three the Refresh action was decussed in the last section so we will consintrate on the first two.

During a normal read or write operation, this exculdes instruction fetch even though it is in reality a read operation, the Z80A will generate &BMREQ (Buffered Memory Request). This signal will be inverted by L41 (3B11) and passed through gates L50 to generate EPDB (Enable Parity and Data Bus) refer to FIGURE 6.4-3. This signal enables the parity circuits and selects the Memory out buffer. Also the transision of this signal, clocks flipflop L51-2 into a set state causing the "Q" output to go high, hence driving the "D" input of flipflop L94-1 high through OR gate L76. On the next low to high shift of 1/2 phi Z clock L94 will set causing &RAS to generated, signaling

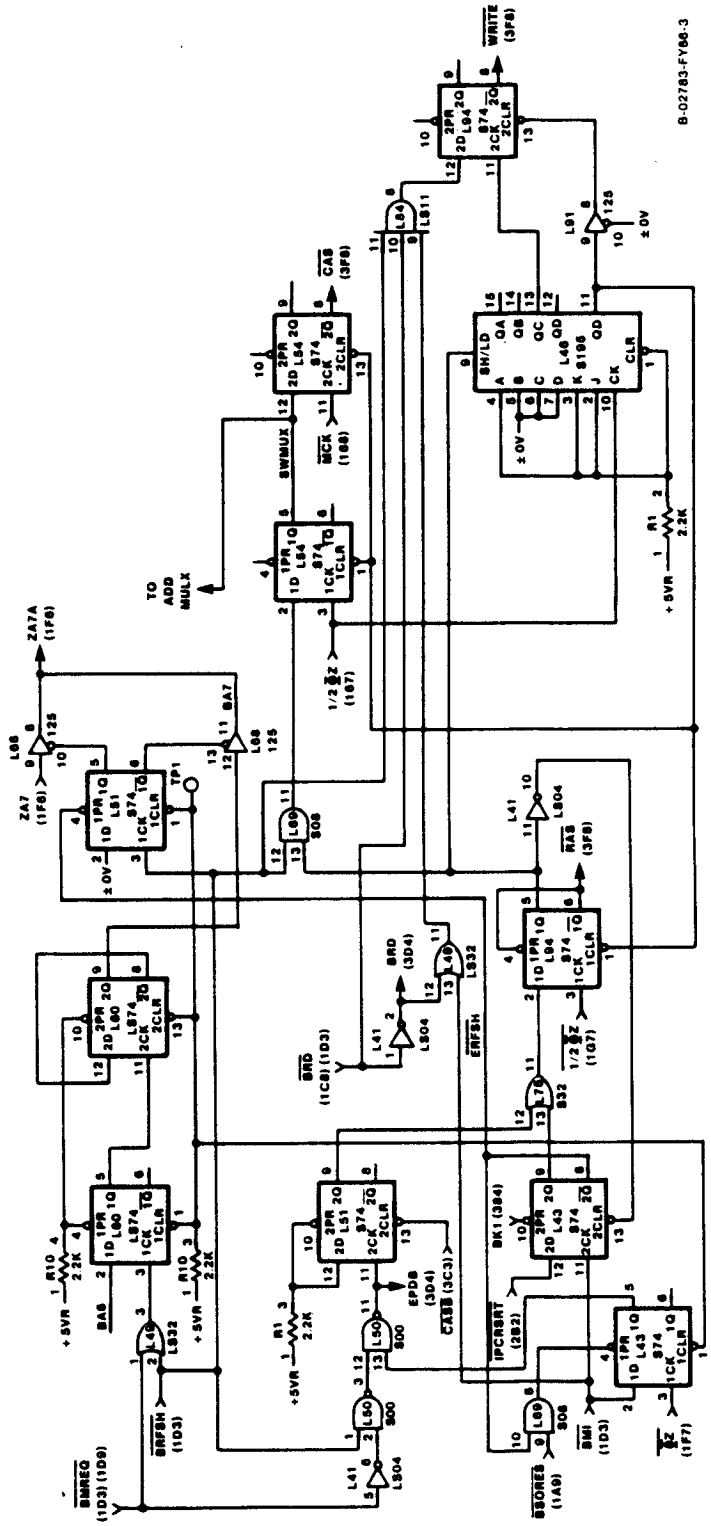

FIGURE 6.4-3
RAS/CAS LOGIC DIAGRAM

the start of the RAS/CAS cycle. The remainder of the RAS/CAS cycle will be descussed later. At the complection of the RAS/CAS cycle L51-2 will be placed in the reset condition by &CASB on its reset input. This will treminate the cycle on the next &1/2 phi z clock.

The RAS/CAS cycle is also started when the Z80A fetches an instruction. When the Z80A begins an instruction fetch cycle it generates &BM1 (Machine 1). This signal is directed to the "D" input of flipflop L43-1. On the next low to high transision of phi Z clock L43 will reset causing the "Q" output to go low. This low is inverted through NAND gate L50 to generate EPDB which then starts the RAS/CAS cycle, just as it did in the last paragraph. Flipflop L43-1 will go back to the set state at T3 time of the M1 cycle, when &BM1 deactivates. The Z80A also generates &BMREQ during the instruction fetch cycle, but it comes at a much later time in the cycle. If the circuits relied on &BMREQ to activate the RAS/CAS cycle during an instruction fetch the address that the PC register of the Z80A placed on the Address Bus would not be stable long enough to generate a reliable address.

To complete the RAS/CAS cycle two more operation must be perfromed. First the address multiplexors must be switched and second the CAS signal must be asserted. Once the RAS flipflop L94 has been set the "Q" output is sent to two locations. The first is the Shift/Load input of shift register L46. This places the register in a shift mode of operation. This register has a two fold operation. One, it determines the complection of the RAS/CAS cycle, and two, it signals the proper time for the write enable signal during a write operation. The second place that the "Q" output of L94-1 is sent is the "D" input of flipflop L54-1, via AND gate L69. Remember, if we are in a refresh cycle AND gate L69 will be disqualified, thus blocking this path. Once the high is placed on the "D" input of L54 and the next low to high transision of 1/2 phi z clock happens L54-1 will set. This generates SWMUX (Swicth Multiplexor) which causes the two address selectors to select the high order bits of the Address Bus. Going back the "Q" output of L54-1 where SWMUX was generated we see that it is also placed on the "D" input of L54-2. On the next low to high transision of &MCK L54-2 will set, generating &CAS from the &"Q" output. At this time the address operation is complete and we are able to perfrom either a read or write.

The only real difference between a read operation and a write operation is that during a write cycle, the Z80A will wait until T4 time before it transfers the data from it's register to the memory. The write enable signal should not be activated until after both RAS and CAS have happened. The timing of this signal is controlled by counter L46. If you recall back when RAS was generated we placed L46 into a shift mode of operation. Then while we were setting up SWMUX and CAS L46 was shifting the single one it had placed in it. When this one