THEORY OF OPERATION

ISBX 218A

FLEXIBLE DISKETTE CONTROLLER

GEORGE ARRIGOTTI

JULY 11, 1983
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iSBX 218/218A COMMON FEATURES

DOUBLE WIDE SBX MULTIMODULE FORM FACTOR.

CONTROLS UP TO FOUR SINGLE/DDOUBLE SIDED
EIGHT INCH DRIVES OR UP TO FOUR SINGLE/
DOUBLE SIDED FIVE AND ONE-QUARTER DRIVES.

SINGLE/DDOUBLE DENSITY MAY BE MIXED.

IBM COMPATIBLE SOFT-SECTORED FORMAT.

DMA OR NON-DMA OPERATION OF SBX BUS.

USES INTEL 8272 FLOPPY DISK CONTROLLER.

PLAN

iSBX 218/218A COMMON FEATURES

iSBX 218A NEW FEATURES

BLOCK DIAGRAM

FUNCTION OF EACH BLOCK

SCHEMATIC VIEW OF EACH BLOCK

THEORY OF OPERATION OF EACH BLOCK

PALS

SOURCES OF FURTHER INFORMATION

218A ADDITIONAL FEATURES

TWO READ/WRITE ONE BIT LATCHES USABLE FOR:

SPINDLE MOTOR ON/OFF CONTROL

HEAD LOAD CONTROL

"IN USE" LED CONTROL

TERMINAL COUNT TO 8272

TDMA MASK

ONE WRITE-ONLY ONE BIT LATCH FOR RESET.

DMA ACKNOWLEDGE (DACK) GENERATOR TO ALLOW

8272 DMA MODE WITH 8089 AND 80186.
218A ADDITIONAL FEATURES (CONTINUED)

ON BOARD PIN SCRAMBLING FOR 5¼" DRIVES.

IMPROVED PHASE LOCKED LOOP CIRCUITRY.

CHOICE OF 125NS OR 250nS WRITE PRECOMPENSATION.

OVERCOMES SEVERAL 8272 BUGS:

WRONG DENSITY HANGUP PROBLEM
NON-EXISTENT DISK HANGUP PROBLEM (READY HANG)
DRQ-TO-COMMAND DELAY SPEC
DMA OVERRUN PROBLEM
DACC MINIMUM PULSE WIDTH PROBLEM

FLEXIBLE DISKETTE CONTROLLER (8272)

HANDLES CONTROL/STATUS LINES TO/FROM DRIVES.

ENCODES/DECODES DATA STREAMS TO/FROM DRIVES.

INTERFACES WITH SBX BUS.

CONTROLS/COORDINATES ALL OTHER BLOCKS.

FUNCTIONAL BLOCKS

FLEXIBLE DISKETTE CONTROLLER (8272)

TIMING AND PHASE LOCKED LOOP LOGIC

READ WINDOW GENERATION LOGIC

READ DATA SHAPING LOGIC

WRITE PRECOMPENSATION LOGIC

DMA SIGNAL GENERATION LOGIC

I/O PORT OPTIONS LOGIC

ISBX BUS INTERFACE

FLEXIBLE DISKETTE DRIVE INTERFACE LOGIC

BUFFERING

MULTIPLEXING

DEMULTIPLEXING

TERMINATION

DRIVE INTERFACE OPTIONS

READY TIMEOUT CIRCUIT
FIGURE 2: fSBX 218A FLEXIBLE DISKETTE CONTROLLER BLOCK DIAGRAM
Timing and Phase Locked Loop Logic

8 and 4 MHz to Precompensation Logic
8 and 4 MHz to the 8272.

Write Clock: 8" MFM 1μs Period
8" FM 2μs Period
5⅞" MFM 2μs Period
5⅞" FM 4μs Period

All pulses about 250ns high time
8272 must always have write clock.

Read Window Generation Logic

CLK3 is VCO frequency divided down:
8" MFM 2 MHz
8" FM 1 MHz
5⅞" MFM 1 MHz
5⅞" FM 0.5 MHz

Window extender adjusts read window
temporarily to catch one late or early bit.

Used by 8272 to separate data from the
combined data/clock stream.

The Voltage Controlled Oscillator (74S124 VCO)
output has three modes:

1. When 8272 VCO signal is high (meaning read), the phase comparator speeds up or
slows down the VCO to match the read data.

2. When 8272 VCO signal is low (meaning not read), the phase comparator locks on to a
known frequency (write clock).

3. When reset button is held, there is no
feedback, and C3 affects frequency.

All should be about 8 MHz.

Read Data Shaping Logic

One shots clean up read data pulses from drive.
Are fired by write clock when VCO signal is low.

Nominal values:
8" MFM 550 ns using 4.99K resistor
8" FM 1100 ns using 10.0K resistor
5⅞" MFM 1100 ns using 10.0K resistor
5⅞" FM 2200 ns using 20.0K resistor
WRITE PRECOMPENSATION LOGIC

TO COUNTER THE EFFECT OF PREDICTABLE BIT SHIFT.

EACH BIT MAY BE WRITTEN EARLY, NORMAL, OR LATE, CONTROLLED BY PS0, PS1.

ALL TRACKS OR JUST INNER TRACKS ARE PRECOMPENSATED.

WRITE DATA TO DRIVE IS LOW WHEN WRITE ENABLE IS INACTIVE.

DMA SIGNAL GENERATION LOGIC

DELAYS DMA REQUEST (DRQ) TO BASEBOARD TO PREVENT AN EARLY COMMAND.

MINIMUM TIMES: 8" DRIVES 800ns

5¼" DRIVES 1600ns

GENERATES MWAIT TO EXTEND DACK OR COMMAND

MINIMUM TIME: 510ns

GENERATES DACK TO 8272 WHEN BASEBOARD CONTROLLER IS 80186 OR 8089 (LIKE 2156)

I/O PORT OPTIONS LOGIC

RESET LATCH - WRITING A ONE FOLLOWED BY WRITING A ZERO PRODUCES A HARDWARE RESET.

LATCH 0 - DEFAULT WIRED TO CONTROL DRIVE SPINDLE MOTOR.

LATCH 1 - DEFAULT WIRED TO CONTROL THE TDMA MASK.

SBX BUS INTERFACE

STANDARD SBX INTERFACE

IMPLEMENTED BY PALS AND THE 8272.
SOURCES OF FURTHER INFORMATION

SBX 218A EXTERNAL PRODUCT SPEC  145935

SBX 218A HARDWARE REFERENCE MANUAL (AVAILABLE LATE AUGUST)

SBX 218A INTERNAL PRODUCT SPEC (AVAILABLE LATE AUGUST)

INTEL 8272 DATA SHEET (IN COMPONENT CATALOG)

SBX 218 MANUAL, ISBC 208 MANUAL (CONTAIN THEORY OF OPERATION SECTIONS FOR VERY SIMILAR CIRCUITS)
LCT LATE NORMAL INT PS1 PSO DSO DS1 ENABLE GND
EARLY WRDATA SPARE13 WE' TDMA DRVSEL3 DRVSEL2 DRVSEL1 DRVSELO VCC

IF (VCC) /WRDATA = /WE +
LCT * /PSO * /PS1 * NORMAL +
LCT * /PSO * PS1 * LATE +
LCT * PSO * /PS1 * EARLY +
/LCT * NORMAL

IF (VCC) /DRVSELO = /DS1 * /DSO
IF (VCC) /DRVSEL1 = /DS1 * DSO
IF (VCC) /DRVSEL2 = DS1 * /DSO
IF (VCC) /DRVSEL3 = DS1 * DSO
IF (VCC) /TDMA = /ENABLE + /INT
IF (VCC) /SPARE13 = VCC

DESCRIPTION

THE WRDATA OUTPUT CONTROLS THE DATA STREAM TO THE DRIVE. WHEN LCT FROM THE 8272 IS ACTIVE, IT GATES OUT THE EARLY, NORMAL, OR LATE SIGNAL DEPENDING ON THE STATE OF PSO AND PS1 FROM THE 8272. WHEN LCT IS INACTIVE (MEANING NO PRECOMPENSATION NEEDED) IT GATES OUT THE NORMAL SIGNAL. ALL THIS ONLY HAPPENS WHEN WRITE ENABLE (WE) IS ACTIVE. OTHERWISE, WRDATA IS LOW.

THE DRVSEL OUTPUTS DECODE DSO AND DS1 FROM THE 8272 AND ARE USED TO SELECT ONE OF THE FOUR DRIVES.
INPUTS INT, ENABLE AND OUTPUT TDMA ALLOW TDMA TO BE MASKED FROM THE SBX BUS.
SPARE13 IS AN UNUSED INPUT/OUTPUT PIN.
PAL U10 OUTPUT PIN 12 WRDATA
(WRITE DATA)

\[
\text{早期 (EARLY)} \\
\text{正常 (NORMAL)} \\
\text{迟 (LATE)} \\
\text{PS} \phi \\
\text{PS1} \\
\text{LCT} \\
\text{WE}
\]

\[
\begin{align*}
\text{早期 (EARLY)} & \quad 11 \\
\text{正常 (NORMAL)} & \quad 3 \\
\text{迟 (LATE)} & \quad 2 \\
\text{PS} \phi & \quad 6 \\
\text{PS1} & \quad 5 \\
\text{LCT} & \quad 1 \\
\text{WE} & \quad 14 \\
\end{align*}
\]

\[
/\text{WRDATA} = /\text{WE} + \\
LCT \times /\text{PS} \phi \times /\text{PS1} \times \text{NORMAL} + \\
LCT \times /\text{PS} \phi \times \text{PS1} \times \text{LATE} + \\
LCT \times \text{PS} \phi \times /\text{PS1} \times \text{EARLY} + \\
/\text{LCT} \times \text{NORMAL}
\]

\underline{PAL CIRCUIT:}

\underline{NOTES:}

\begin{enumerate}
\item \text{When WE is low, the output is always low.}
\item \text{When WE is high and LCT is low, the normal signal is driven out.}
\item \text{Only when WE is high and LCT is high, PS} \phi \text{ and PS1 are used to select the early, normal, or late signal.}
\end{enumerate}

\underline{Alternate Representation:}

\begin{enumerate}
\item LCT
\item PS\phi
\item PS1
\item \text{NORMAL}
\item \text{EARLY}
\item \text{LATE}
\item \text{MUX}
\item \text{C0 B A} \\
\item \text{C1 C2 C3 (74153)} \\
\item \text{WRDATA}
\item \text{WE}
\end{enumerate}
PAL U10 OUTPUT PINS 16, 17, 18, 19
(DRVSEL₂, DRVSEL₂, DRVSEL₁, DRVSEL₀)

DS₀ --- 7 19  ---  DRVSEL₀
DS₁ --- 8 18  ---  DRVSEL₁
          --- 17  DRVSEL₂
          --- 16  DRVSEL₃

EQUATIONS:
/DRVSEL₀ = /DS₁ + DS₀
/DRVSEL₁ = /DS₁ + DS₀
/DRVSEL₂ = DS₁ + /DS₀
/DRVSEL₃ = DS₁ + DS₀

ALTERNATE REPRESENTATIONS:

74139 2 TO 4 LINE DECODER

DS₀ DS₁
PAL UIO OUTPUT PIN 15 TDMA

ENABLE 9 15 TDMA
INT 4

EQUATION: \( \overline{TDMA} = \overline{ENABLE} + \overline{INT} \)

PAL CIRCUIT:

ENABLE  \[\overline{TDMA}\]  INT

ALTERNATE REPRESENTATION:

ENABLE  \[\overline{TDMA}\]  INT
HDLOAD VCO DRQ DACK INDEX BDRESET SPARE7 CLK DELAY GND
INT START RECOVER MDRQT AX BX CX DX TRIGGER VCC

IF (VCC) /MDRQT = /DRQ +
    /DACK +
    BDRESET +
    INT +
    /DELAY * /MDRQT

IF (VCC) /AX = INDEX * VCO +
          VCO * /BDRESET * /AX

IF (VCC) /BX = /INDEX * /AX +
            /AX * /BDRESET * /BX

IF (VCC) /CX = INDEX * /BX +
            /BX * /BDRESET * /CX

IF (VCC) /DX = /INDEX * /CX +
            /BDRESET * VCO * /CX * /DX

IF (VCC) /RECOVER = /RECOVER * /BDRESET * VCO * /DX +
                      INDEX * /DX

IF (VCC) /START = DRQ * DACK * /BDRESET * /INT * /MDRQT

IF (VCC) /TRIGGER = INDEX * HDLOAD +
                  CLK * /HDLOAD

DESCRIPTION OF PINS

DACK - DMA ACKNOWLEDGE TO 8272.
DRQ - DMA REQUEST FROM 8272.
MDRQT - DMA REQUEST TO BASE BOARD.
START - SIGNAL THAT BEGINS THE RC DELAY FOR DRQ.
DELAY - INPUT FROM RC DELAY CIRCUIT.
BDRESET - BASE BOARD OR PROGRAMMED RESET.
AX,BX,CX,DX,RECOVER - STATE MACHINE USED TO OVERCOME THE
  8272 FM-DISK-IN-MFM-SLOT LOCKUP BUG.
VCO - FROM 8272 - INPUT TO THE ABOVE STATE MACHINE.
INDEX - INPUT TO THE ABOVE STATE MACHINE. ALSO FOR RETRIGGER GENERATOR.
TRIGGER - OUTPUT TO KEEP RETRIGGERING THE DRIVE HANGUP ONE SHOT.
HDLOAD - FROM 8272 - INPUT TO RETRIGGER GENERATOR.
CLK - FROM WRITE CLOCK CHAIN - INPUT TO RETRIGGER GENERATOR.
SPARE7 - SPARE INPUT PIN.
PAL 415 Output Pins 13, 15, 16, 17, 18

(Recover, AX, BX, CX, DX)

\[\begin{align*}
VCO & \quad 2 \quad 15 \\
INDEX & \quad 5 \quad 16 \\
BDRESET & \quad 6 \quad 17 \\
& \quad 18 \\
& \quad 13 \quad \text{RECOVER}
\end{align*}\]

AX, BX, CX, DX are not connected to other devices. They are used internally.

EQUATIONS:

\[
\begin{align*}
/AX &= \text{INDEX} \times VCO + VCO \times BDRESET \times /AX \\
/BX &= /\text{INDEX} \times /AX + /AX \times /BDRESET \times /BX \\
/CX &= \text{INDEX} \times /BX + /BX \times /BDRESET \times /CX \\
/DX &= /\text{INDEX} \times /CX + /BDRESET \times VCO \times /CX \times /DX \\
/\text{RECOVER} &= /\text{RECOVER} \times /BDRESET \times VCO \times /DX + \text{INDEX} \times /DX
\end{align*}\]

STATE MACHINE REPRESENTATION:

EXAMPLE:

\[
\begin{array}{cccc}
1 & 1 & 1 & 1
\end{array}\]

\[
\begin{array}{cccccc}
1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}
\]

This path for all states

\[
\begin{array}{cc}
VCO \times \text{INDEX} & VCO \times /\text{INDEX} \\
VCO \times \text{INDEX} & VCO \times /\text{INDEX} \\
VCO \times \text{INDEX} & VCO \times /\text{INDEX}
\end{array}
\]
PAL U15 OUTPUT PIN 19 TRIGGER

INDEX
HDLOAD
CLK

TRIGGER

5
1
8

EQUATION:
\[ \text{TRIGGER} = \text{INDEX} \times \text{HDLOAD} + \text{CLK} \times \neg \text{HDLOAD} \]

PAL CIRCUIT:

INDEX
HDLOAD
CLK

TRIGGER

NOTES:

TRIGGER DRIVES A FALLING-EDGE-TRIGGERED INPUT TO A ONE SHOT. THE OUTPUT OF THE ONE SHOT DRIVES READY TO THE 8272.

WHEN THE HEAD IS LOADED (MEANING AN ACCESS IS BEING MADE) INDEX PULSES FROM THE SELECTED DRIVE WILL KEEP RE_TRIGGERING THE ONE SHOT, INDICATING READY TO THE 8272.

IF THE HEAD IS LOADED AND NO DISKETTE IS INSTALLED IN THE SELECTED DRIVE, THERE WILL BE NO INDEX PULSES AND THE ONE SHOT WILL TIME OUT, INDICATING NOT READY TO THE 8272.

WHEN THE HEAD IS NOT LOADED, A CLOCK SIGNAL Keeps RE_TRIGGERING THE ONE SHOT.

SO THE 8272 READY LINE IS ALWAYS TRUE EXCEPT IN THE NON-EXISTENT DISK ACCESS ATTEMPT DESCRIBED ABOVE.
PAL U15 OUTPUT PINS 12 AND 14 (START AND MDRQT)

EQUATIONS:

/START = DRQ & DACK & /BDRESET & /INT & /MDRQT

/MDRQT = /DRQ +
       /DACK +
       BDRESET +
       INT +
       /DELAY & /MDRQT

PAL CIRCUITS:

CONTINUED →
START AND MDRQ T (CONTINUED)

ALTERNATE REPRESENTATION:

DELAY  

<table>
<thead>
<tr>
<th>DRQ</th>
<th>DACK</th>
<th>BDRESET</th>
<th>INT</th>
</tr>
</thead>
</table>

MDRQT  

START  

NOTES:

THE 8272 SPEC SAYS THAT AFTER IT SENDS OUT DRQ, IT MUST NOT SEE IOQWT FOR 800 µS OR IORD FOR 250 µS (DOUBLE THESE TIMES FOR 5/4" DRIVES). THE PURPOSE THE RC DELAY CIRCUIT IS TO DELAY DRQ BEFORE IT GETS TO THE BASEBOARD. BOTH READ AND WRITE DRQS ARE DELAYED AT LEAST 800 µS (1600 µS FOR 5/4" DRIVES).

A SIGNAL DIAGRAM SHOWING THE SEQUENCE OF EVENTS IS ON THE NEXT PAGE.
1. The DMA cycle begins when the 8272 sends out DRQ, which causes START to go low which lets the RC network begin to decay.

2. When the RC decays to logic zero of a Schmitt trigger, DELAY goes high, which makes MDRQT go active to the baseboard (the reason we did this), which makes START go high, which allows the RC to recharge to be ready for the next cycle.

3. When the RC charges to logic high of a Schmitt trigger, DELAY goes low again.

4. When DACK from the baseboard goes active, MDRQT is removed. Later, the 8272 removes DRQ.
QUAL  MCS1  IORD  IOWRT  MA1  MA2  MRESET  EXTEND  MDACK  GND
CLK3  DACK  RLATCH  RDW  ALATCH  MDO  MLATCH  BDRESET  WAIT  VCC

IF (VCC) /BDRESET = /MRESET * /RLATCH

IF (VCC) /MLATCH = BDRESET +
  /IOWRT * /MCS1 * MA2 * /MA1 * /MDO +
  /MDO * /MLATCH +
  IOWRT * /MLATCH +
  MCS1 * /MLATCH +
  /MA2 * /MLATCH +
  MA1 * /MLATCH

IF (VCC) /RDW = EXTEND * /CLK3 +
  /CLK3 * /RDW +
  /EXTEND * /RDW

IF (/MCS1 * MA2 * /IORD) /MDO = /MA1 * /MLATCH +
  MA1 * /ALATCH

IF (VCC) /ALATCH = BDRESET +
  /MDO * /ALATCH +
  /IOWRT * /MCS1 * MA2 * MA1 * /MDO +
  IOWRT * /ALATCH +
  MCS1 * /ALATCH +
  /MA2 * /ALATCH +
  /MA1 * /ALATCH

IF (VCC) /RLATCH = MRESET +
  /IOWRT * /MCS1 * /MA2 * MA1 * /MDO +
  /MDO * /RLATCH +
  IOWRT * /RLATCH +
  MCS1 * /RLATCH +
  MA2 * /RLATCH +
  /MA1 * /RLATCH

IF (VCC) /DACK = QUAL * /MDACK * /IORD +
  QUAL * /MDACK * /IOWRT +
  QUAL * /MDACK +
  /IORD * /MA1 * /MA2 * /MCS1 +
  /IOWRT * /MA1 * /MA2 * /MCS1

IF (VCC) /WAIT = MDACK * MCS1 +
  MDACK * MA1 +
  MDACK * MA2

DESCRIPTION OF PINS

DACK - DMA ACKNOWLEDGE TO 8272.
BDRESET - RESET TO SBX BOARD.
RLATCH - PROGRAMMABLE RESET LATCH.
MLATCH - MOTOR ON/OFF LATCH.
ALATCH - AUXILIARY LATCH. MAY BE USED FOR DMA TERMINAL COUNT.
EXTEND,CLK3,RDW - READ WINDOW SIGNALS.
MCS1,IORD,IOWRT,MA1,MA2,MDO,MWAIT,MRESET,MDACK - STANDARD SBX SIGNALS.
QUAL - INPUT TO SELECT BETWEEN COMMAND-QUALIFIED DACK AND
        UNQUALIFIED DACK
WAIT - USED WITH RC DELAY CIRCUIT TO PRODUCE MWAIT TO THE SBX
      TO EXTEND DACK.
PAL 019 Output Pin 18

BDRESET

(Board Reset)

Rlatch is an output of the PAL, but is used internally as an input in this circuit.

Equation: \[ \overline{BDRESET} = \overline{MRESET} \cdot \overline{RLATCH} \]

**PAL Circuit:**

\[ \text{MRESET} \quad \overline{BDRESET} \]
\[ \text{RLATCH} \]

**Alternate Representation:**

\[ \text{MRESET} \quad \overline{BDRESET} \]
\[ \text{BDRESET} \]
**PAL 019 Output Pin 17**

*MOTOR LATCH*

- **BDRESET**: 18
- **MCS1**: 2
- **MA1**: 5
- **MA2**: 6
- **IOWRT**: 4
- **MD φ**: 16

**MLATCH** is also used as an output when reading motor latch.

**BDRESET** is also used as an output.

**Equation**: 
\[ \text{MLATCH} = \text{BDRESET} + \frac{\text{IOWRT} \times \text{MCS1} \times \text{MA2} \times \text{MA1}}{\text{MD φ} \times \text{MLATCH} + \text{IOWRT} \times \text{MLATCH} + \text{MCS1} \times \text{MLATCH} + \text{MA2} \times \text{MLATCH} + \text{MA1} \times \text{MLATCH}} \]

**PAL Circuit**:

**Notes**: BDRESET turns the motor off (MLATCH low). An IO write to this address with Bit 0 = 1 turns the motor on; with Bit 0 = 0 turns the motor off.

MLATCH goes through an inverting buffer before going to the drive interface where it is active low.

MLATCH can be read by doing an IO read to the same address. See MD φ output page for details.
PAL U19 OUTPUT PIN 14 RDW (READ WINDOW)

EQUATION: \[ \overline{\text{RDW}} = \overline{\text{EXTEND}} \cdot \overline{\text{CLK3}} + \overline{\text{CLK3}} \cdot \overline{\text{RDW}} + \overline{\text{EXTEND}} \cdot \overline{\text{RDW}} \]

PAL CIRCUIT:

ALTERNATE REPRESENTATION:

NOTES: THIS FUNCTION USED 12 PINS OF U7 ON THE 218 NON A. SINCE IT REQUIRES ONLY 3 PINS OF THE 1618, THE REST OF THE PAL IS AVAILABLE FOR THE NEW 218A FEATURES.
MDφ is also used as an input for other functions in this PAL.

MLATCH and ALATCH are PAL output pins, but are used internally for this circuit.

Equation: \[
\frac{1}{\text{MDφ}} \cdot \left( \frac{1}{\text{MCS1}} \cdot \text{MA2} \cdot \frac{1}{\text{IORD}} \right) = \frac{1}{\text{MA1}} \cdot \frac{1}{\text{MLATCH}} + \frac{1}{\text{MA1}} \cdot \frac{1}{\text{ALATCH}}
\]

PAL Circuit:

Notes:

Usually, MDφ is strictly an input, used for writing to the motor latch, reset latch, and auxiliary latch. However, when an IO read is done to either the motor latch or the auxiliary latch, MDφ becomes an output, driving the state of the selected latch onto the data bus. The "sense" of the data is the same as when the latches are written.

Bit 0 = 1 means latch high (motor on, or TC active).
Bit 0 = 0 means latch low (motor off, or TC inactive).
PAL U19 OUTPUT PIN 15

LATCH 1
(AUXILIARY LATCH)

| BDRESET | 18 |
| MCS1    | 2  |
| MA1     | 5  |
| MA2     | 6  |
| IOWRT   | 4  |
| MDφ     | 16 |

ALATCH

MDφ is also used as an output when reading ALATCH. BDRESET is also used as an output.

EQUATION: \[ ALATCH = BDRESET + \]
\[ IOWRT \times (MCS1 + MA2 + MA1 \times MDφ + MDS1 + ALATCH + IOWRT \times ALATCH + (MCS1 + ALATCH + IOWRT + ALATCH + MA1 + ALATCH) \]

PAL CIRCUIT:

ALTERTATE REPRESENTATION:

NOTES: MRESET forces ALATCH low. An IO WRITE to this address with BIT 0=1 sets ALATCH high; with BIT 0=0 sets ALATCH low. ALATCH may be used to drive TERMINAL COUNT (TC) to the 8272.

IOWRT = 400

MDφ = 1.27 mS

MA1

MA2

ALATCH CAN BE READ BY DOING AN IO READ TO THE SAME ADDRESS. SEE MDφ OUTPUT PAGE FOR DETAILS.
PAL U19 OUTPUT PIN 13 RATCH (RESET LATCH)

EQUATION: \( \overline{\text{RLATCH}} = \overline{\text{MRESET}} + \overline{\text{IOUWT}} \cdot \overline{\text{MCS1}} + \overline{\text{MA2}} \cdot \overline{\text{MA1}} + \overline{\text{MD}} + \overline{\text{MD}} \cdot \overline{\text{RLATCH}} + \overline{\text{IOUWT}} + \overline{\text{MCS1}} \cdot \overline{\text{RLATCH}} + \overline{\text{MA2}} \cdot \overline{\text{RLATCH}} + \overline{\text{MA1}} \cdot \overline{\text{RLATCH}} \)

PAL CIRCUIT:

MRESET

HD

IOUWT

MCS1

MA2

MA1

ALTERNATE REPRESENTATION:

MRESET

MD

IOUWT

MCS1

MA2

MA1

NOTES: MRESET FORCES RLATCH INACTIVE (LOW). AN IO WRITE TO THIS ADDRESS WITH BIT 0 = 1 MAKES RLATCH ACTIVE; WITH BIT 0 = 0 MAKES RLATCH INACTIVE. RLATCH CANNOT BE READ.

RLATCH IS NOT CONNECTED TO OTHER DEVICES ON THE BOARD. IT IS ONLY USED INTERNAL TO THE PAL.
PAL U19 OUTPUT PIN 12

DAC

(DMA ACKNOWLEDGE)

EQUATION:

\[
/\text{DAC} = \text{QUAL} \times /\text{MDACK} \times /\text{IORD} + \\
\text{QUAL} \times /\text{MDACK} \times /\text{IOWRT} + \\
/\text{QUAL} \times /\text{MDACK} + \\
/\text{IORD} \times /\text{MA1} \times /\text{MA2} \times /\text{MCS1} + \\
/\text{IOWRT} \times /\text{MA1} \times /\text{MA2} \times /\text{MCS1}
\]

PAL CIRCUIT:

NOTES:

WHEN MDACK IS AVAILABLE ON THE SBX, IT MAY BE QUALIFIED BY COMMAND (IF QUAL IS TIED HIGH) OR NOT QUALIFIED (QUAL TIED LOW).

WHEN THE DACK GENERATOR OPTION IS USED, THE BASEBOARD WRITES OR READS WITH MA1, MA2 LOW, AND THE PAL SENDS DACK TO THE 8272.
PAL U19 OUTPUT PIN 19  WAIT

EQUATION: \[
\text{WAIT} = \text{MDACK} \times \text{MCS1} + \\
\text{MDACK} \times \text{MA1} + \\
\text{MDACK} \times \text{MA2}
\]

PAL CIRCUIT:

ALTERNATE REPRESENTATION:

NOTES:

WAIT IS HIGH WHENEVER MDACK IS ACTIVE (LOW) OR WHEN MCS1, MA1, MA2 ARE LOW (MEANING THAT A WRITE OR READ TO THE DACK GENERATOR IS ABOUT TO OCCUR).

SIGNAL DIAGRAMS SHOWING THE MWAIT SEQUENCE OF EVENTS ARE ON THE NEXT TWO PAGES.
MWAIT Generator When SBX DACK Is Used

1. MDACK/, from the baseboard goes active, which makes WAIT (PAL output) go low, which makes MWAIT/ go active.
2. Command arrives, so the PAL now gates DACK through to the 8272. (This assumes qualified DACK was jumpered). DACK going low lets the RC start to decay.
3. The RC discharges down to Schmitt trigger logic low which cause MWAIT to go high, indicating to the CPU that no more wait states be inserted.
4. Command ends, so DACK ends, and RC recharges. When it reaches Schmitt trigger high, MWAIT goes low again (no effect on CPU).
5. MDACK/ ends, so WAIT and MWAIT both end.
MCS1, MA1, MA2

WAIT

IORD, or IOWRT

DACK to 8272 (this is the DACK generator)

RC

MWAIT/

1. MCS1, MA1, MA2 FROM THE BASEBOARD GO ACTIVE, WHICH MAKES WAIT (PAL OUTPUT) GO LOW, WHICH MAKES MWAIT/ GO ACTIVE.
2. COMMAND ARRIVES, SO THE PAL PRODUCES DACK AND SENDS IT TO THE 8272 (THIS IS THE DACK GENERATOR).
   DACK GOING LOW LETS THE RC START TO DECAY.
3. THE RC DISCHARGES DOWN TO SCHMITT TRIGGER LOGIC LOW WHICH CAUSE MWAIT TO GO HIGH, INDICATING TO THE CPU THAT NO MORE WAIT STATES BE INSERTED.
4. COMMAND ENDS, SO DACK ENDS, AND RC RECHARGES. WHEN IT REACHES SCHMITT TRIGGER HIGH, MWAIT GOES LOW, AGAIN (NO EFFECT ON CPU).
5. MCS1, MA1, MA2 END, SO WAIT AND MWAIT BOTH END.
NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, ±20%
2. RESISTANCE VALUES ARE IN OHMS, ±10%, ±5%
3. ALL ODD NUMBERED PINS OF J1 ARE CONNECTED TO GROUND.
NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, ±0.1%, 105°C, SOV.
2. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%
3. ALL ODD NUMBERED PINS OF J1 ARE CONNECTED TO GROUND.