SAFETY

PERSONAL

The importance of personal safety cannot be overemphasized. To ensure personal safety and the safety of co-workers, follow established safety practices and procedures at all times.

Look for and obey the DANGER notices found in the maintenance documentation. All CEs must be familiar with the general safety practices and the procedures for artificial respiration outlines in IBM Form 229-1264.

For convenience, this form is duplicated to the right.

MACHINE

To protect machines from damage, turn off power before removing or inserting circuit cards or components. Do not leave internal machine areas needlessly exposed, avoid wearing panel pins when scooping, and handle machine parts carefully, in addition, look for and observe the CAUTION notices found in maintenance documentation.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.

2. Remove all power, ac and dc, when removing or examining major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or inspecting changes in machine connectivity.

3. After turning off wall box power switch, lock in the Off position or tag it with a "Do Not Operate" tag, Form 229-196. Pull power supply cord wherever possible.

4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pins and screwdrivers.
   d. Keep one hand in pocket.
   e. Make sure the person who is watching you can quickly shut off power if necessary.

5. Wear safety glasses when:
   a. Using a hammer to drive pins, removing, replacing, etc.
   b. Power or hand driven drilling, marking, shaping, etc.
   c. Using spring hooks, attaching springs.
   d. Bending, saw cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.

6. Performing any other work that may be hazardous to your eyes. REMEMBER -- THEY ARE YOUR EYES.

7. Follow special safety instructions when performing special tasks, such as handling ceramic oil seals and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.

8. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.

9. Avoid using tools or test equipment that have not been approved by IBM.

10. Remove worn or broken tools and test equipment.

11. Lift or stand to the side, or push using stronger leg muscles -- this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.

12. After maintenance, inspect all safety devices, such as guards, shields, signs, and grounding wires.

13. Each Customer Engineer is responsible to be certain that no person on his partrendered products unsafe or exposed customer personnel to hazards.

14. Place removed machine covers in a safe out-of-the-way place where no one can step on them.

15. Ensure that all machine covers are in place before returning machine to customer.

16. Always place CE tools and cab kits away from each area where no one can step on it; for example, under desk or table.

17. Avoid touching moving mechanical parts when lubricating, checking for leaks, etc.

18. When using instrument, do not touch ANYTHING -- it may be hot.

19. Avoid touching metal clothing that may be caught in moving parts.

20. Safety and the safety practices and the procedures at maintenance documentation.

21. Maintain good housekeeping in area of machine while performing and after-completing maintenance.

22. Keep safety rules and the following safety practices.

ARTIFICIAL RESPIRATION

General Considerations

1. Start immediately -- Seconds Count

2. Do not move victim unless absolutely necessary to remove from danger. Do not use on bed, or bed to chair, or chair to bed.

3. Check Mouth for Obstructions


5. Loosen Clothing -- Keep Visible Warm

6. Keep victim warm, dry, and comfortable. Replace worn or broken test equipment. Make certain that controls are set correctly and that insulated probes of proper capacity are used.

7. Another person familiar with power off controls must be in immediate vicinity.

8. When using test instruments, be certain that controls are in correct position or parts weighing over 60 pounds.

9. Ensure that power supplies, performing mechanical inspection of machine frames, etc., using suitable rubber mats, floor strips, etc.

10. Never wear rings, wrist watches, chains, bracelets, or metal cuff links.

11. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.

12. Another person familiar with power off controls must be in immediate vicinity.

13. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.

14. Never touch moving parts when lubricating, checking for leaks, etc.

15. Avoid touching metal clothing that may be caught in moving parts.

16. Safety and the safety practices and the procedures at maintenance documentation.

17. Maintain good housekeeping in area of machine while performing and after-completing maintenance.

18. Keep safety rules and the following safety practices.

Tube and finger positions

Three mouth-to-mouth breathing position
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OPER—SUBSYSTEM CONCEPTS

BASIC SUBSYSTEM
The IBM 3803-2/3420 Magnetic Tape Subsystem consists of an IBM 3803 Model 2 Tape Control and one or more IBM 3420 Magnetic Tape Units. The 3420 tape units are available in six models with tape speeds of 75, 125, and 200 inches per second (ips) (190.5, 317.5, 508 cm/sec) for Models 3 and 4, 5 and 6, and 7 and 8, respectively.

The 3803 Model 2 operates in 6250 bpi and 1600 bpi modes.

A 3803 tape control without any switching features controls up to eight 3420 tape units (1+7 configuration, also called selection logic).

The 3803 command set, status responses, and basic sense data are compatible with those used by IBM 2400-series tape subsystems. However, there are some major new features.

1. The number of sense bytes and contents of those bytes differ from those used by 2400-series subsystems.

2. All commands not shown on 40-005 and 40-009 set COMMAND REJECT in the sense information which, in turn, sets Unit Check in the status byte, indicating to the system that something is wrong.

3. A sense command must be issued after an error condition sets Unit Check in the unit status byte.

In most instances, non-time-dependent programs that operate successfully on an IBM 2400-series tape subsystem will operate correctly on an IBM 3803-2/3420 subsystem.

3420 TAPE UNIT
Information presented in this section applies to all models of the tape unit.

With compatible features, 3420 Models 3, 5, and 7 can be attached to the 3803-2 without modification.

AUTOMATIC THREADING
A write reel latch secures the file reel to the reel hub automatically. When the operator places a file reel or cartridge on the hub and presses LOAD/REWIND, the power window closes, the write reel latch secures the file reel to the hub, and tape is automatically threaded, loaded into the vacuum columns, and positioned at load point without further operator action.

IBM Easy load cartridge
When used with a solid-flange tape reel (standard IBM 10.5 inch), the optional, IBM Easy Load Cartridge reduces tape handling and helps prevent contamination or physical damage. During a load operation, if the first threading sequence is unsuccessful, tape is rewound into the cartridge and another attempt is made.

TAPE TRANSPORT
A single direct-drive capstan moves tape forward or backward. Air bearings reduce friction and tape wear since the oxide (recording) surface of the tape contacts the read/write head and the tape cleaner. Short, tapered vacuum columns greatly reduce tape inertia when starting and stopping tape. The tapered columns and single, direct-drive capstan start and stop tape quickly and smoothly.

REWINDING
Tape remains in the vacuum columns during rewind operations. Rewind ends when a photocell senses a reflective marker on the beginning-of-tape (load point) reflective marker on tape. During a rewind unload operation, tape is rewound completely onto the file reel. The tape unit is left in unloaded status, with the tape reel and the window open, allowing the operator to remove the file reel.

FILE PROTECTION
A write enable ring must be present in the file reel when writing. To avoid destroying information on tape, the write enable ring is removed. A reel without the ring is "file-protected." FILE PROTECT turns on when the reel is mounted and no writing can occur.

3420 MODELS 4, 6, AND 8
Models 4, 6, and 8 tape units can write and read 6250 bpi tapes with 0.3-inch interblock gaps. Nominal data rates are 470, 780, and 1250 kilobytes per second at 6250 bps.

A tape cleaning mechanism is added. 3420 Models 3, 5, and 7 can be converted in the field to Models 4, 6, and 8.

READ BACK CHECKING
A two-gap read/write head with 0.150 inch (3.81 mm) between read and write gaps allows read back checking during a write operation. Moving forward, tape passes first the write gap, then the read gap.

FULL-WIDTH ERASURE
An erase head applies a strong magnetic field that erases the entire width of tape during write operations. Full-width erasure prevents interchangeability problems when tape is written on one tape unit and read on another; it also reduces the chances of leaving extraneous bits in interblock gaps or skip areas.

During a write, write tape mark, or erase operation, the tape unit monitors the erase head operation. On a 3420 Model 4, 6, or 8, an erase head failure drops tape unit ready status and halts tape motion. On a 3420 Model 3, 5, or 7, an erase head failure sets Unit Check, but does not drop ready status.
RECORDING METHODS

6250 BPI

In 6250 bpi mode, 6250 data bytes per inch (246 data bytes per mm) are recorded in nine parallel tracks on tape. 6250 bpi tapes are written with an identification burst (ID burst) in track 1 at load point. The ID burst is followed by a control burst and a 0.3-inch (7.62 mm) IBG before a data block is written. 6250 bpi is a basic density on 3803 Model 2 and on 3420 Models 4, 6, and 8.

6250 BPI ERROR CORRECTION

The 6250 bpi format employs an error-correcting/detecting code capable of correcting all single-track errors on the strength of the code alone and correcting all double-track errors with the aid of track pointers. Pointers such as phase error and incorrect pattern are indications of questionable data. Data Check and Unit Check are set and Error Recovery Procedures (ERPs) are invoked.

1600 BPI

In 1600 bpi mode, 1600 bytes per inch (63 bytes per mm) are recorded in nine parallel tracks on tape. The data format uses eight of the nine bits for data, the ninth is a parity bit. Data is recorded in odd parity. The data format uses six of the seven bits for data and the seventh bit for parity checking. Data is recorded in either odd or even parity. The six bits of one character can represent a BCD character or six binary bits. For seven-track NRZI operation, a seven-track feature is required on both a 3420 Model 3, 5, or 7 and on the 3803-2.

INTERBLOCK GAP

An interblock gap (IBG) is the erased section of tape used to indicate the end of a block or record. Interblock gaps are:

6250 bpi: 0.3 inch (7.6 mm) nominal.

Nine-track: 0.5 inch (12.7 mm) minimum.

Seven-track: 0.68 inch (17.7 mm) minimum.

MAGNETIC TAPE AND REELS

Most tape volumes that operate satisfactorily on 3420 Models 3, 5, and 7 will operate with equal or better read/write reliability for an equivalent number of bytes transferred on 3420 Models 4, 6, or 8. Tape must conform to IBM Half-Inch Tape Specifications, GA32-0006.

SEVEN-TRACK NRZI

In seven-track NRZI mode, data is recorded at 200, 556, or 800 bpi (7, 6/21, 9/31, 5 bytes per mm). The data format uses six of the seven bits for data and the seventh bit for parity checking. Data is recorded in either odd or even parity. The six bits of one character can represent a BCD character or six binary bits. For seven-track NRZI operation, a seven-track feature is required on both a 3420 Model 3, 5, or 7 and on the 3803-2.

3420 SUBSYSTEM CHARACTERISTICS

<table>
<thead>
<tr>
<th>Model</th>
<th>Tape Speed (Read or Write) (ips)</th>
<th>Start Time, nominal (ms)</th>
<th>Write Access Time, nominal (ms)</th>
<th>Read Access Time, nominal (ms)</th>
<th>Rewind/Unload Time (2400-foot reel) (sec)</th>
<th>Load Operation, approximate time (sec.) to:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model 3</td>
<td>75</td>
<td>0.8</td>
<td>2.9</td>
<td>2.6</td>
<td>60</td>
<td>10</td>
</tr>
<tr>
<td>Model 4</td>
<td>75</td>
<td>0.9</td>
<td>2.9</td>
<td>2.6</td>
<td>60</td>
<td>10</td>
</tr>
<tr>
<td>Model 5</td>
<td>125</td>
<td>0.9</td>
<td>2.9</td>
<td>2.6</td>
<td>60</td>
<td>10</td>
</tr>
<tr>
<td>Model 6</td>
<td>125</td>
<td>0.9</td>
<td>2.9</td>
<td>2.6</td>
<td>60</td>
<td>10</td>
</tr>
<tr>
<td>Model 7</td>
<td>200</td>
<td>1.0</td>
<td>3.0</td>
<td>2.7</td>
<td>60</td>
<td>10</td>
</tr>
<tr>
<td>Model 8</td>
<td>200</td>
<td>1.0</td>
<td>3.0</td>
<td>2.7</td>
<td>60</td>
<td>10</td>
</tr>
</tbody>
</table>

*Read access time is the interval from initiation of a Forward Read command given to the tape control when tape is not at load point, until the first data byte is read when tape is brought up to speed from stopped status. Write access time is the interval from the issuance of a Move command given to the tape unit when tape is not at load point, until the first data byte is written on tape when tape is brought up to speed from stopped status.

**Start time is the interval from the issuance of a Move command to the tape unit, until tape attains 90% of specified velocity.
OPER—3803 MODEL 2 CONTROLS

3803 MODEL 2 TAPE CONTROL

The 3803 Model 2 Tape Control connects to the I/O interface of an IBM System/360 Model 50 and above (by RPO only) or an IBM System/370, Model 135 and above. The tape control has a CE panel, two microprogram control sections, a read section, a write section, and a channel buffer section.

Note: "I/O Interface" refers to a set of lines over which the tape control and system channel exchange control and data signals. Interface lines and operations are described in IBM System/360 and System/370 I/O Interface, Channel to Control Unit, "Original Equipment Manufacturers" Information. Number Order GA22-6974.

The 3803 may exceed an interface signal sequence of 32 microseconds, and may produce a worst case interface signal sequence of up to 50 microseconds on some instructions when in seven-track mode with the two-channel switch feature switch installed.

The 3803 Model 2 operates at 6250 or 1600 bpi. The 3803 Model 2 with appropriate features can process some instructions when in seven-track mode with the two-channel switch feature installed.

ADDRESSING

Every tape unit has a unique device address, which consists of a channel address, a tape control address, and a tape unit address. Pluggable jumpers assign the tape control address when the system is installed. The tape control has separate device interface connectors for each tape unit address. A tape unit's address is determined by the tape control connector to which it is attached. There is no address decoding at the tape unit or device interface level.

METERING

A usage meter is installed in the tape control and in each tape unit. The tape control's usage meter records elapsed time whenever the METERING OUT line is active and the tape control is in online status (Enabled). A tape unit's usage meter records elapsed time when the tape control METERING OUT line is active, tape unit is loaded, and the tape is not at load point. METERING IN is used by the central processing unit (CPU) metering circuits; this line is active from the time a command is accepted by the tape control until Device End is generated for that command. See IBM System/360 and System/370 Interface: Channel to Control Unit OEM" Information. Order Number GA22-6974.

ENABLE/DISABLE SWITCH

This switch allows the tape control and all attached tape units to be put online or taken offline so a customer engineer can use the CE panel switches and indicators to diagnose errors. Whenever the tape control is placed in offline status (Disabled), the usage meters in the tape control and all attached tape units are prevented from running. When the two-channel switch feature is installed, a second Enable/Disable switch is provided on the 3803.

POWER ON/OFF SEQUENCING

Normal power on/power off sequencing for the 3803/2/3420 tape subsystem is controlled by system power interlock circuits. Maintenance activities may necessitate dropping power in the tape control and attached tape units while power remains in the system. To take the subsystem offline, see 12-010.

40-003

3803-2/3420 CONFIGURATIONS

Operation with Model 4/6/8 Tape Units 1250 or 1600 bpi Mode and Models 3/5/7 1600 bpi Tape Units

Operation with Model 4/6/8 Tape Units 1250 or 1600 bpi Mode and Model 3/5/7 Tape Units (1600 bpi PE and 800 NRZI Modes)

40-003

MAXIMUM OF 8 TAPE UNITS PER TAPE CONTROL

For 3420 Model 8 Power Requirements, see 90-180.
OPER—3803 MODEL 2 FEATURES

3803 MODEL 2 FEATURES
Features available on a 3803 Model 2 are nine-track NRZI, seven-track NRZI, two-channel switch, and device switch. For switch feature descriptions, see Section 58-005 through 58-111.

NINE-TRACK NRZI
The nine-track NRZI feature, available on the 3803 Model 2, permits operation in nine-track NRZI mode. Nine-track NRZI operation requires a 3420 Model 3, 5, or 7 Tape Unit with the dual density feature.

SEVEN-TRACK NRZI
The seven-track feature permits operation in seven-track NRZI mode. Seven-track operation with a 3803 Model 2 is at 800/556/200 bpi. The seven-track feature contains both the data translator and data converter for seven-track operations. The operation is similar to that of the 3803-1 with the seven-track feature. For seven-track operation, the seven-track feature on a 3420 Model 3, 5, or 7 and on the 3803 Model 2 is required. The nine-track NRZI feature is a prerequisite for the seven-track feature on the 3803 Model 2.

Writing a tape with the translator on causes eight-bit bytes from the I/O interface to be written on tape as six-bit BCD characters; reading such a tape causes six-bit BCD characters to be translated into their EBCDIC equivalents. When using the translator, data rates are not changed and there are no changes in the tape unit’s operation.

Writing a tape with the data converter on causes four tape characters (24 data bits) to be written for every three storage bytes (24 data bits); reading such a tape reverses the process by converting four tape characters into three storage bytes. When operating with the data converter on, the data transfer rate is 75 percent of the rate with data converter off.

---

DENSITY FEATURE COMBINATIONS

<table>
<thead>
<tr>
<th>Density (bpi) (Note 1)</th>
<th>3803-1</th>
<th>3803-2</th>
<th>3420-3/5/7 (Note 2)</th>
<th>3420-6/6/8 (Note 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6250, 9-Track</td>
<td>Not Applicable</td>
<td>Standard</td>
<td>Not Applicable</td>
<td>6250 Feature</td>
</tr>
<tr>
<td>1600, 9-Track</td>
<td>Standard</td>
<td>Standard</td>
<td>1600 Feature</td>
<td>6250/1600 Feature</td>
</tr>
<tr>
<td>800, 8-Track</td>
<td>Dual Density Feature</td>
<td>9-Track NRZI Feature</td>
<td>Dual Density Feature</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>800, 7-Track</td>
<td>7-Track Feature</td>
<td>7-Track Feature (Note 4)</td>
<td>7-Track Feature</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>556, 7-Track</td>
<td>7-Track Feature</td>
<td>7-Track Feature (Note 4)</td>
<td>7-Track Feature</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>200, 7-Track</td>
<td>800/600 only</td>
<td>7-Track Feature (Note 4)</td>
<td>7-Track Feature</td>
<td>Not Applicable</td>
</tr>
</tbody>
</table>

Notes:
1. Density must be specified for each 9-track 3420 tape unit.
2. 3420-3/5/7 can be operated by a 3803-1 or 3803-2.
3. 3420-6/6/8 can be operated by a 3803-2 only.
4. 9-track NRZI feature is a prerequisite for 7-track feature on 3803-2.
OPER—TAPE COMMANDS

COMMANDS AND INSTRUCTIONS

COMMANDS

Commands executed by this subsystem fall into one of the following three categories:

1. Burst Commands
2. Motion Control Commands
3. Non-Motion Control Commands

The table on this page and the one on 40-008 list the subsystem commands and command codes. Commands not listed will set COMMAND REJECT.

Programming Note: The 3803/3420 subsystem has no interlocking to prevent improper sequencing of write- and read-type operations that may result in writing extraneous bits or leaving partial blocks on tape.

Avoiding these improper sequences is a program responsibility.

Avoid the following two basic sequences:

1. A write-type operation after a forward read-type operation except:
   a. When the block or Tape Mark (TM) read is known to be followed by a TM. A tape mark is a special block used to separate files.
   b. When the block or TM read is known to have been followed by erase record gap (ERG) or is known to have been the last block written before a backward operation.

   For example: R W* avoid. W B R W* allowed.

2. A read forward-type operation following write-type operations.

   For example: R B W* avoid. W B R R* avoid.

W indicates a write-type operation: write, write TM, or (ERG).

R indicates a forward read-type operation: read forward, forward space block, or forward space file.

B indicates a backward read-type operation: read backward, backscape block, or backscape file.

* indicates the logical record on which problems may occur.

Because it may be difficult or impossible to ensure the above safe situations, a write after read forward sequence should be used only in applications where strict control of format and command sequence exists.

Write is allowable following a backscape. Assume the following tape format with labels where * is used to denote a TM:

VOL HDR * DATA SET * EOF * HDR * DATA SET * EOF **

A rewrite of the last data set involves the following safe and proper sequence. After processing the next to last end of file (EOF) and TM, read forward to verify the header (HDR) label of the last data set, backscape, write a new HDR, and rewrite the data set. If a new data set is being added, the read forward verifies the second consecutive TM, and thus, the true end of a data set on this tape. A backscape, write new HDR, etc., completes the sequence.

<table>
<thead>
<tr>
<th>Burst Commands</th>
<th>Command Byte</th>
<th>Command Word (CCW)</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write</td>
<td>0 0 0 0 0 0 1 0 01</td>
<td>0 1 2 3 4 5 6 7</td>
<td>01</td>
</tr>
<tr>
<td>Read Forward</td>
<td>0 0 0 0 0 0 0 1 0 02</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read Backward</td>
<td>0 0 0 0 0 1 1 0 0 0C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sense</td>
<td>0 0 0 0 0 0 0 1 0 0 04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sense Reserve</td>
<td>1 1 1 1 0 1 0 0 0 F4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sense Release</td>
<td>1 1 1 1 0 1 0 0 0 04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Request Track-In-Error</td>
<td>0 0 0 0 1 1 1 1 1 1 B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Loop Write-To-Read</td>
<td>1 1 0 0 1 0 1 1 88</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Set Diagnose</td>
<td>0 1 0 0 1 0 1 1 48</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Motion Control Commands</th>
<th>Command Byte</th>
<th>Command Word (CCW)</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rewind</td>
<td>0 0 0 0 0 1 1 1 0 07</td>
<td>0 1 2 3 4 5 6 7</td>
<td>07</td>
</tr>
<tr>
<td>Rewind Unload</td>
<td>0 0 0 0 1 1 1 1 0F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Erase</td>
<td>0 0 0 0 1 1 1 1 1 1 17</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Write Tape Mark</td>
<td>0 0 0 0 1 1 1 1 1 1 17</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backspace Block</td>
<td>0 0 0 0 1 1 1 1 1 1 1 1 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backspace File</td>
<td>0 0 0 0 1 1 1 1 1 1 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Forward Space Block</td>
<td>0 0 0 0 1 1 1 1 1 1 37</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Forward Space File</td>
<td>0 0 0 0 1 1 1 1 1 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Security Erase</td>
<td>1 0 0 1 0 1 1 1 97</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

BURST COMMANDS

Burst commands transfer data across the channel/tape control interface. Channel End and Device End are signaled when the operation is complete (ending status).

The burst commands are:

Write
Read Forward
Read Backward
Sense
Sense Reserve
Sense Release
Request Track-In-Error
Loop Write-To-Read (maintenance aid*)
Set Diagnose (maintenance aid*)

* Diagnostic programs issue maintenance aid commands via start I/Os (SIOs) that are op-codes in the Channel Command Word (CCW).

WRITE

Write records data on tape as it moves forward and creates an interblock gap (IBG) at the end of each block. The tape control checks the parity of each data byte received from the I/O interface.

READ FORWARD

Read Forward sets the tape unit to forward read status. As the tape moves, data is read until the read head detects the next IBG. The tape control checks and, if necessary and possible, corrects the bits of each byte transferred to the I/O interface. Sensing a tape mark sets Unit Exception with Channel End and Device End in the Unit Status byte.

SENSE

Sense transfers the sense bytes to channel. There are 24 bytes of sense data available. The CCW specifies the number of sense bytes to be transferred and the starting storage address. The information transferred includes unusual conditions associated with the last operation and provides details about the current conditions present in the tape control and tape unit. A sense command addressed to a tape unit that is not ready will be executed.

SENSE RESERVE

Sense Reserve reserves the addressed tape control for the channel issuing this command. The tape control will remain reserved for the channel until either:

- A Sense Release command is issued from the reserving channel, or
- A system reset occurs.

Attempting to select a tape control that is reserved to another channel results in a Control Unit Busy indication. The Sense Reserve command should only be issued by the Control Program.
SENSE RELEASE

Sense Release releases the reserved tape control so it is available to either channel. The Sense Release command should only be issued by the control program.

Programming Note: Sense Reserve and Sense Release commands can only be used on subsystems having the two-channel switch feature. If these commands are issued to a tape control without this feature, COMMAND REJECT results. When using these commands, they must be the first command in a chain or COMMAND REJECT results.

The Sense Reserve and Sense Release commands are not supported by IBM Operating Systems.

REQUEST TRACK-IN-ERROR (REQUEST TIE)

Request TIE returns to the tape control a data byte containing track-in-error information for 9-track and sensing level information for 7-track tape units. This information is transmitted to the channel in sense byte 2 on a Sense command following a Read, Read Backward, Write, or Loop Write to Read command. When issued following a 6250 bpi or PE operation, Request TIE is treated as a No Operation (NOP Reset Sense).

When issued following a 9-track NRZI read operation, a Request TIE either:

- Enables the tape control to perform a correction read operation if the data byte contains a single bit, or
- Does not enable the tape control to perform a correction read operation if the data byte contains bits 6 and 7, which indicate an uncorrectable error.

When issued following a 7-track read operation, the Request TIE byte controls the read clipping level in the following sequence:

  - Second attempt—Middle Level
  - Third attempt—Low Level
  - Fourth attempt—High Level

Clipping levels are cyclically altered in this way as long as read attempts result in Vertical Redundancy Check (VRC) errors.

LOOP WRITE-TO-READ (LWR)

Loop Write-to-Read checks the tape control and tape unit data and control paths without moving tape. In 6250 or 1600 bpi mode, LWR writes and error checks the record. In NRZI mode, LWR writes the record but checks only for Write Trigger VRC errors. Read errors will occur during the NRZI operation but will be reset by ALU2 when the LWR operation is completed.

On 9-track 3420 tape units, a LWR command issued at beginning-of-tape (BOT) is executed in 1600 bpi mode. Elsewhere on tape, LWR is executed in the current operating mode of the tape unit.

LWR does not require the tape unit to be in write status, but the tape unit must be ready. Execution of an LWR does not change the status of the tape unit.

An LWR performed from the processing unit uses the same data path as a Write command.

SET DIAGNOSE '4B'

Set Diagnose is used to call microdiagnostic routines. Bytes are transferred from channel to the tape control to modify the operation of succeeding commands in the chain.

FLAG BYTE 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Diagnostic Write</th>
<th>N/A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Inhibit Postamble</td>
<td>N/A</td>
</tr>
<tr>
<td>1</td>
<td>Inhibit Preamble</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>Var Go-down Time</td>
<td>Var Go-down Time</td>
</tr>
<tr>
<td>3</td>
<td>Var Go-down Time</td>
<td>Var Go-down Time</td>
</tr>
<tr>
<td>4</td>
<td>Inhibit Preamble</td>
<td>Inhibit Preamble</td>
</tr>
<tr>
<td>5</td>
<td>LWR</td>
<td>LWR</td>
</tr>
<tr>
<td>6</td>
<td>TUBO Mask</td>
<td>TUBO Mask</td>
</tr>
<tr>
<td>7</td>
<td>Change Direction</td>
<td>Change Direction</td>
</tr>
</tbody>
</table>

Diagnostic Write

Performs the same function as the 'OB' command.

PE - causes writing to be inhibited in any track when the write data contains successive one bits.

NRZI -

- 9 track - Inhibits writing P bits.
- 7 track - Inhibits writing C bits.

Inhibit Postamble

Prevents writing the last 39 zeros of the postamble.

The ending all-ones marker and the first zero is written.

Variable Go-down Time

Two bytes (flag bytes 3 and 4) are sent to the tape control unit. These bytes are used to control the tape wait time before starting the next operation in the chain following the Set Diagnostic (4B) command.

Count values are:

- 103.15 microseconds to decrement one count.
- 27 milliseconds to decrement the low order counter 256 ('FF') counts and cause one decrement of the high order count.

Inhibit Preamble

Prevents writing the first 39 zeros of the preamble. The last (40th) zero and the beginning all-ones marker is written.

Loop Write-To-Read

Write data is sent to the tape unit. In the MST board it is gated to the read circuits and then returned to the tape control unit for read checking.

Set TUBO Mask

Flag byte 3 is used as a mask to control the tape unit Bus Out. Any bit on in flag byte 3 causes that tape unit Bus Out bit to be held active, and thus prevents the tape unit from writing data for that specific bit.

Change Direction

Change Direction allows the following word (CCW) chain to progress through turnaround, if necessary, and up to the point of activating the Move line to the tape unit. At this point, the operation is terminated. The tape unit is left in forward or backward, write or read status, depending on the operation follow the Change Direction instruction.

FLAG BYTE 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Block Data Check</td>
</tr>
<tr>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>Block Interrupts</td>
</tr>
<tr>
<td>3</td>
<td>Fence Control Unit Busy</td>
</tr>
<tr>
<td>4.7</td>
<td>N/A</td>
</tr>
</tbody>
</table>

FLAG BYTE 3 (OPTIONS)

DMR Go-Up Time in track pulses

GDT Hi order byte of go-down count

TUBO Mask Byte used to mask TU Bus Out

FLAG BYTE 4 (OPTIONS)

DMR Go-down time measure count equivalent to tach pulses. No tach pulse when tape is not moving.

GDT Lo order byte of go-down count.
OPER—TAPE COMMANDS (Cont'd)

MOTION CONTROL COMMANDS

Motion control commands move tape but do not transfer information across the channel/tape control interface.

All motion control commands operate as follows:

1. Channel End is signaled when the command is accepted (initial status).
2. For commands other than Rewind/Unload, device end is signaled when the operation is completed (ending status).
3. The tape control responds with BUSY if the tape control is addressed while executing the command. As a result, the 3800 is obligated to present a CUE interrupt to the channel that received the BUSY as soon as the current operation is complete.

Note: For Rewind/Unload, Channel End is signaled in initial status, and Device End, Control End, Unit Control, and Unit Check are signaled in an interrupt status cycle after the command becomes effective at the tape unit. Device End is signaled again when the operator reloads tape, presses START, and the tape unit goes from not-ready to ready providing the tape control has not been offline in the interim.

Motion control commands are:

REWIND
Rewind/Unload
Erase Gap
Write Tape Mark
Backspace Block
Backspace File
Forward Space Block
Forward Space File
Data Security Erase

REWIND (REW)
Rewind the selected tape unit to rewind tape to load point.

REWIND UNLOAD (REW)
Rewind Unload causes the selected tape unit to rewind tape to load point, removes tape from the columns, finishes winding tape onto the right reel, closes the cartridge (if used), and opens the window.

ERASE RECORD GAP (ERG)
Erase Record Gap causes the selected tape unit to move tape forward and erase tape as follows:

<table>
<thead>
<tr>
<th>Single ERG</th>
<th>Successful ERGs</th>
</tr>
</thead>
<tbody>
<tr>
<td>6250 bpi</td>
<td>3.75 in. (95.3 mm)</td>
</tr>
<tr>
<td>1600 bpi and 800 bpi 9-track</td>
<td>4.2 in. (106.7 mm)</td>
</tr>
<tr>
<td>7-track</td>
<td>4.5 in. (114.3 mm)</td>
</tr>
</tbody>
</table>

WRITE TAPE MARK (WTM)
Write Tape Mark causes the selected tape unit to move tape forward and write a tape mark block. At 6250 and 1600 bpi, a WTM causes the subsystem to write a tape mark preceded by an Erase record gap. Data Check, Equipment Check, and Unit Check can be set during a Write Tape Mark (WTM) operation.

FORWARD SPACE BLOCK (FSB)
Forward Space Block causes the selected tape unit to move tape forward to the interblock gap beyond the next tape mark. No data bytes are transferred. Initial status contains Channel End. Device End is signaled at the completion of the operation. Sensing the tape mark does not set the Unit Exception bit.

Programming Note: The control responds with a Control Unit Busy sequence while performing an ERG, WTM, BSB, BSF, FSB, or FSB operation.

DATA SECURITY ERASE (DSE)
Data Security Erase causes the selected tape unit to erase tape from the point at which the operation is initiated until the end-of-tape marker is sensed. The DSE command is accepted by the tape control only when chained immediately following an Erase Gap command. Receipt of this command under any other condition results in COMMAND REJECT. If the command is accepted, initial status contains Channel End, and Device End is signaled when the operation is complete. An attempt to erase a file-protected tape unit sets COMMAND REJECT. Unit Exception never occurs as a result of this command. Data Security Erase at end of tape (EOT) causes an immediate ending sequence. The tape control does not remain busy after initial selection. An attempt to select the tape unit while executing a DSE results in busy status.

Device End is signaled when the DSE marker is sensed during a normal DSE completion. However, a sense command should be performed to assure EOT was reached. Upon completion of the DSE, the operating program must issue sufficient erase gap commands to ensure erasure of any data written beyond the EOT marker. Issuing 14 erase gap commands, which erases about 4 feet (1.22m) of tape, is generally sufficient. The channel must be enabled for interrupts to detect a Unit Check condition due to manual intervention. When Device End is signaled, a sense command should be performed to ensure the tape unit reached EOT.

The Data Security Erase command is not currently supported by IBM Operating Systems. DOS supports DSE via a Magnetic Tape Command (MTC).
OPER—TAPE COMMANDS (Cont’d)

NON-MOTION CONTROL COMMANDS

Non-motion control commands do not move tape and do not transfer data across the channel/tape control interface.

Channel End and Device End are signaled when non-motion control commands are accepted (initial status).

Non-motion control commands are:

- No-Operation
- Mode Set 1
- Mode Set 2
- Diagnostic Mode Set (maintenance aid)

NO-OPERATION (NOP)

NOP performs no function in the tape control or tape unit, and does not transmit data or move tape. NOP does not reset tape control sense data.

Programming Note: Placing a NOP command at the end of a series of chained commands delays channel disconnect from the tape control until the NOP is executed. Indiscriminate use of this command delays the channel program, and may contribute to a channel overload condition.

MODE SET 1 (MS 1)

Mode Set 1 commands sent to tape controls with the 7-track NRZI feature establish an operating mode for succeeding 7-track NRZI operations. Bits 0 and 1 control density (200/556/800 bpi) and bits 2, 3, and 4 control parity (odd or even), data converter (on or off), and translator (on or off) circuits in the tape control.

See chart on this page.

A Mode Set 1 command affects operation of all 7-track tape units attached to the tape control. Unless reset, the tape control retains its mode setting until it receives another Mode Set command.

MODE SET 2 (MS 2)

Mode Set 2 commands sent to a 3803 Model 2, set the operating mode for succeeding write-type operations. Modes are: 6250 bpi, 1600 bpi PE, or 800 bpi nine-track NRZI. Unless reset, the tape control retains its mode setting until it receives another Mode Set command.

DIAGNOSTIC MODE SET (DMS)

DMS causes an artificial signal-loss condition that checks read and write error detection circuits.

- At 6250 bpi, track P is made all zeros and the program supplies the error correcting code as part of the data.
- At 6250 bpi Diagnostic Read inhibits single- and double-track error corr check characters to channel with data.
- At 1600 bpi, whenever write data contains successive one bits in any track, writing in that track is inhibited until the last one bit is reached.
- In 9-track NRZI mode, no bits are written in track P.
- In 7-track NRZI mode, no bits are written in track C.

A Diagnostic Mode Set command affects only operations for the command chain in which it is issued.

**Mode Set Commands**

<table>
<thead>
<tr>
<th>Mode Set 1 (7-Track) (See Note)</th>
<th>Mode Set 2 (9-Track)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set Density</td>
<td>Parity</td>
</tr>
<tr>
<td>200</td>
<td>556</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
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<td>X</td>
<td>X</td>
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<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note:** Seven-track Mode Set 1 commands are treated as 'NOP reset sense' when issued to a tape control without the seven-track NRZI compatibility feature.
OPER—TAPE COMMANDS (Cont’d)

I/O INSTRUCTIONS
In addition to initiating one of the I/O operations by means of the Start I/O (SIO) instruction, the program can cause certain actions at the tape control by using the Test I/O and Halt I/O instructions.

TEST I/O
A Test I/O instruction performed by the Central Processing Unit (CPU), causes the status byte for the selected tape unit to be sent to the channel for analysis. No actual operation is performed.

Note: A Test I/O command issued to a not ready tape unit results in a contingent connection on tape control units with the two-channel switch.

HALT I/O
A Halt I/O instruction causes transfer to stop. The tape control disconnects from the channel and proceeds independently to the completion of the operation. When the operation is completed, the tape control tries to re-establish connection with the channel to transfer ending status. If addressed while completing the operation, the tape control returns a BUSY signal.

If a Halt I/O instruction is executed after STATUS IN and before tape motion is started during a Write or Read operation, the operation is canceled, and Channel End, Device End, Unit Check, and Data Check are generated.
OPER—WRITE CIRCUITS

WRITE DATA FLOW LOGIC

Seventh-Track Feature

Write Translator and Data Converter 57-020 57-025

A1E2

BN011-BN311

OR DOT IR

BR101

Channel Buffer Out

Without 7-Track Feature, install jumpers

Channel Buffer Gate

Set Byte 1

A1H2

Write Group Buffer

Set Byte 2

A1H2

BW001

Set Write Group Buffer 2 53-020

Set Byte 3

A1H2

BW001

Set Write Group Buffer 2 53-020

Set Byte 4

A1H2

BW001

Format

Write Encoder 5 Buses

A1 (10101)

A2 (01010)

Mark 1

Mark 2

Cnr 1

Cnr 2

Cnr 4

A1H2

BW001-BW051

BW001-BW051

Write Condition

Write Triggers 53-070

A1H2

BW061-BW081

Write Tar VRC

F0021

Format Control

Write Clock and Controls 53-020

Write Counter 53-020

Write Counter = 0

Write Counter = 0 and WC = 0

At020

50-001
ROS 1 TRAP CONDITIONS (Cont'd)

Both hardware and microprograms generate resets. Types of resets are General, Selective, and Machine.

1. **GENERAL RESET** resets all flags, stats, and reserve bits that apply to the selecting interface.

2. **SELECTIVE RESET** performs the same functions except the Control Unit Reserve and Hold Interface bits are not reset.

3. **POWER ON RESET** and CE panel resets generate MACHINE RESET. Turning power on and pressing RESET both generate POWER ON RESET. POWER ON RESET clears some LSRs and initiates INTERFACE CHECKOUT. Channel outbound tags are checked to ensure all are inactive and all inbound tags except OP IN are activated. Contents of the CHANNEL BUS IN register are sent to CHANNEL BUS OUT.

4. **INITIAL SELECTION AB CE traps ROS 1 to 000 at each selection of the tape control.**

5. **LOCK ROS 1 IC traps ROS 1 to 000 when an ALU 1 hardware error occurs.**

   MP2 is activated for the proper reset after Stat B has been set on or off to reset only the selecting interface. CONTROL UNIT BUSY is activated for the duration of the reset and is deactivated at completion of MP2 reset.

   If MP2 has hardware errors, the tape control "hangs up" with BUSY active and loops on a trap address.

   If all steps are completed correctly, the reset is finished. Any failure "hangs up" the tape control at a trap address and BUSY remains active.
6250 WRITE SERVICE REQUIREMENTS

The write buffers fill automatically at the maximum rate permitted by the control unit, cable, and channel delays. This diagram shows when byte requirements occur. The channel must respond only to the average need during the period of overrun, checking such that at least one ECC (error correction code) group remains in control unit buffers at all times until stop occurs. Note that no individual channel byte transfer is overrun checked.

36 bytes are pre-buffered and one ECC group or more must remain in the buffer at all times prior to Stop. This time could permit some data chaining or be considered a safety factor.

Notes:
[1] Proportionately more on lower speed tape units.
[2] The Resync Burst consists of a mark 1 group, 2 sync groups, and a mark 2 group. It is interleaved in a block of data after every 158 data groups, and is used to re-synchronize the read circuits during a 6250 read operation.
6250 READ SERVICE REQUIREMENTS

The channel buffer and both read byte buffers are empty at the start. Overrun is called only if there is insufficient room in the buffer for a waiting ECC group. The ECC rate varies according to corrections required but follows the tape rate average over periods of 50 bytes or more. The channel has until the postamble end to accept all data from the buffer. Note that no individual data transfer is checked for overrun. To overrun, the buffer fills during a channel lag.

There is excess read buffer capacity equivalent to 10 usec available for "slip" or possible data chaining. The time may be distributed or lumped. Overrun check effectively starts at the 34th byte since that is the total buffer capacity.
OPER—CLOCK CIRCUITS

MICROPROCESSOR CLOCKS CONTROL LOGIC

Hardware clocks control both microprocessors (MP1 and MP2). The clocks are stepped by 20.48-MHz pulses.

The MP2 clock is similar to the MP1 clock shown.

The clocks run on either 150- or 200-nanosecond cycles. The length of the cycle depends on the instruction.

The numbers on the clock outputs (CLK1—CLK22) bear no relationship to the times these lines become active within the clock cycle.

Clock Timing Chart

- Short Cycle (150 nsec) - Long Cycle (200 nsec)

0 ns Tap AA011/AB011
25 ns Tap AA011/AB011
50 ns Tap AA011/AB011
75 ns Tap AA011/AB011
100 ns Tap AA011/AB011
125 ns Tap AA011/AB011
150 ns Tap AA011/AB011
175 ns Tap AA011/AB011
(unused)

Ck 1
Ck 4 (Add: 150-0)
ISTO Logic Op 100 ns Tap
Ck 6 (STO)
Ck 7 (not BU)
Ck 8 (BU) Initialize
Ck 11 (ROS Cycle Mode)
Ck 12
Ck 15 (STO)
(Logic Op)
(XFR to LSR)
(ADD)
Ck 16 (XFR to LSR)
Ck 17
Ck 18 (unused in ALU1)
Ck 19 (ADD)
Ck 21 (XFR to LSR)
Ck 22 (Logic Op)
(ADD)

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MICROPROCESSOR 1 INSTRUCTION COUNTER (IC)

MP2 IC is similar on:
ALD A0071, A081, A091
Cards A2L2, A2M2
**OPER—LSR BUFFERS**

**LOCAL STORAGE REGISTERS**

The Local Storage Registers (LSRs) serve as buffers to hold command codes, addresses, error conditions, and any other data the microprocessors use. Each microprocessor has 32 Local Storage Registers. Each register holds one byte (8 bits) of data and a parity bit. The registers are numbered LSR 0 through LSR 31.

Data from the D Register is stored in the LSRs, and the output from the LSRs goes to the A Register and the B Bus.

Microprogram instructions gate the contents of the LSRs to other registers.

When the LSRs are used, Field 1 of the microprogram instruction addresses a specific register.

The procedure on page 12-012 displays contents of local storage registers.

**ROS/LSR Logic**

**STAT REGISTERS**

STAT registers are used for microprocessor to microprocessor communication and for microprocessor to data flow communication.

**MP1 Stat Register Usage**

<table>
<thead>
<tr>
<th>MP1 Stat</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>7</td>
</tr>
</tbody>
</table>

**MP2 Stat Register Usage**

<table>
<thead>
<tr>
<th>MP2 Stat</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>7</td>
</tr>
</tbody>
</table>

**MP1/MP2 Stat Registers**

The MP1 and MP2 Stat Registers are identical except for the gating lines.

\((MP1) + XFR LSR 1 To Stat\)

\((MP2) + XFR LSR 2 To Stat\)
Bits from XOUTA (XOUTA BIT x) are used as follows:

<table>
<thead>
<tr>
<th>Bit ALD Function</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>BW231 Gates PE Mode</td>
</tr>
<tr>
<td>1</td>
<td>AA141 Gates Forward Operation</td>
</tr>
<tr>
<td>2</td>
<td>AA141 Allows envelope loss</td>
</tr>
<tr>
<td>3</td>
<td>CC021 Gates Sync Mode for Detection</td>
</tr>
<tr>
<td>4</td>
<td>BW231 Gates Error Mode</td>
</tr>
<tr>
<td>5</td>
<td>CB111 Gates Detection Frequency</td>
</tr>
<tr>
<td>6</td>
<td>AA141 Gates low gain to read logic</td>
</tr>
<tr>
<td>7</td>
<td>CB111 Gates detection frequency</td>
</tr>
</tbody>
</table>

The contents of XOUTA are gated to MP1 by XFR on XINA TO LSR on A4431. Output of XOUTA in MP2 is known as XINA in MP1.

MP2 XOUTB crossover register is a transfer register sending a byte of information to MP1. This register is primarily used to send sense bytes from MP2 to MP1 for transfer to channel.

Crossover Register

Crossover registers are identical except for the gating lines:

- XFR LSR1 to XOUTA
- XFR LSR2 to XOUTB
- XFR XOUTB (To Trap MP2)
OPER—MP INFORMATION

MICROPROCESSOR LISTINGS
Microprocessors 1 and 2 have different listings that can be identified by ALU1 or ALU2 printed in the upper left corner of each page.

Listings are in four parts:
1. General reference information, sense byte descriptions, Local Storage Register layout, branch condition codes, transfer codes, etc.
2. Equate statements which specify a symbolic name for a value. Equate statements are generally followed by a description of the use of the constant.
3. Listing of the executable instructions.
4. Cross reference

3803-2 / 3420

MICROPROCESSOR INSTRUCTIONS
Microprocessor instructions have the following format:
[label]OPCODE field1,field2[comments]

where label is a one- to eight-character name by which the instruction can be referenced. Branch instructions point to locations in the microprogram by label.

OPCODE is the operation to be performed on the data or addresses in Field 1 or Field 2.

Field 1 is generally the address of a Local Storage Register. In some instructions this field may be a branch condition or ROM page number.

Field 2 is generally a constant, referred to as a decimal number or by a symbolic name. The value of symbolic constants for each microprocessor is listed in the beginning of the listings as EQU statements. In some instructions this field may be a branch address or transfer code.

Field 2 can contain several symbolic constants combined arithmetically, that is, the sum or difference of two or more constants.

For example, the constant in the instruction:

ADO WORK 1,ONES-174

results in the constant hexadecimal FF (ONES) minus the decimal value 174, or a decimal value of 81.

DO MICROPROGRAM EC’s
Microprogram EC’s are applied with two Array Patch Cards, type DE01, which provide auxiliary ROS arrays. The arrays contain four sets of microcode patches (ALU1 and 2 for 3803-1 and 2). Plug each card as shown in Figure 1 in order to select the proper patches for its location. The following patches are active when these two cards are installed (refer to page 52-102 for the patch listings):
1. Alternate Path Device Busy
2. Velocity Retry Extension
3. Turnaround Delay
4. Allocated Busy
5. Truncated Postamble
6. Extra Device End
7. Sense Reset

Verify factory plugging:

Card locations - 82/2

A2G2

Plug 1

location 82/2

ALU 1

Plug 1

location A2G2

Figure 1

52-030

Note: If RPD 510231 is installed see plugging instructions on pages 52-103 / 104.
HIGH-ORDER ROS REGISTER

The High-Order ROS Register in each microprocessor holds the 8 high-order bits of a microprogram instruction. The registers in MP1 and MP2 are identical. Bits 0 through 3 contain the operation code. Bits 4 through 7 contain a branch condition or LSR address. Bit 3 will be zero for OR, AND, ADD, XO, and STO instructions. In these instructions, bit 3=0 allows the addressed LSR to be updated.

Bit 3 in this register serves different purposes, depending on the instruction being executed. Bit 3 is part of the operation code for the modified instructions ORM, ADDM, ANDM, and XOM. This use prevents updating the LSR by blocking the gate to the LSR, CLK 15.

Bit 3 is part of the branch condition code for the BOC instruction. There are 32 branch condition codes used.

LOW-ORDER ROS REGISTER

The Low-Order ROS register in each microprocessor holds the 8 low-order bits of a microprogram instruction. The registers in MP1 and MP2 are identical. The output from these registers goes to the A Bus, the transfer decode circuits, or the Instruction Counter, depending on the instruction.

A REGISTER

The A Register serves as a buffer for information from an LSR that is used as input to the ALU. The contents of the selected LSR are gated to the A Register by XFR LSR TO A REGISTER. The next logic operation (ADD, AND, OR, or XOR) ORs the contents of the A Register with the contents of the instruction's Field 2 and places the result on the A Bus.

During logic operations, the A Register is reset by the CLK 4 line.
OPER—CHANNEL TAGS

CHANNEL TAGS IN REGISTER
The Channel Tags in register holds the channel tags bits until they are transferred to the Channel Bus In. Individual register bits are used as follows:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Chain Hold A</td>
</tr>
<tr>
<td>1</td>
<td>Chain Hold B</td>
</tr>
<tr>
<td>2</td>
<td>Hold Interface or Busy</td>
</tr>
<tr>
<td>3</td>
<td>CU Busy</td>
</tr>
<tr>
<td>4</td>
<td>Service In</td>
</tr>
<tr>
<td>5</td>
<td>Status In</td>
</tr>
<tr>
<td>6</td>
<td>CTI Bit 5 to CE</td>
</tr>
<tr>
<td>7</td>
<td>CTI Bit 6 to CE</td>
</tr>
</tbody>
</table>

CHANNEL BUS IN REGISTER
The Channel Bus In register serves as a buffer to transfer bytes from LSRs in MP1 to channel.
The TUBO register is a buffer to hold control information. High speed output is ORed with data bus bits.

The TUBO register stores MP2 control information for the 3420. The output information is multiplexed with tag lines (MOVE, CONTROL, COMMAND) to control tape unit functions.


**OPER—MP REGISTERS**

**D REGISTERS**

The D Register serves as a buffer between the ALUs and LSRs. A CLK 22 pulse loads the data into the D Register and resets individual positions when no data is available to load them. Transfer (XFR) microinstructions gate input from BUS OUT.

CLK 21 gates D Register input from the ALU during store and transfer operations. During logic operations, this input remains active because CLK 21 does not occur.

**MP1 SPECIAL REGISTER (HARDWARE ERRORS)**

The Special Register in MP1 (AB481) is not used as a conventional register, because the input gate is always active and the latchback is always inactive. MP1 hardware errors merely pass through the register becoming SPEC REG BITS 0-7. When needed, parity bit is generated to maintain odd parity.

Special Register bits are activated as follows:

<table>
<thead>
<tr>
<th>Spec Reg Bit</th>
<th>Error Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ALU Parity Error ALU1</td>
</tr>
<tr>
<td>1</td>
<td>SYS Parity Error ALU1</td>
</tr>
<tr>
<td>2</td>
<td>IC or XFR Parity Error ALU1</td>
</tr>
<tr>
<td>3</td>
<td>Microprogram Error ALU1</td>
</tr>
<tr>
<td>4</td>
<td>Instruction Error ALU1</td>
</tr>
<tr>
<td>5</td>
<td>D Bus Parity error ALU1</td>
</tr>
<tr>
<td>6</td>
<td>Unused</td>
</tr>
<tr>
<td>7</td>
<td>Branch Error Interface ALU1</td>
</tr>
</tbody>
</table>

**MP2 SPECIAL REGISTER (TU BUS IN)**

The Special Register in MP2 (FD011) is used as the Tape Unit Bus In Register. The Device Bus In bits are called DEVICE BITS LATCHED. The register gate is CLK 18 SET TUBI ALU2. When needed, parity bit is generated to maintain odd parity.

**MIST OR TCS REGISTER (MP1)**

The MIST (Multi-Interface Tags) Register (FC181) is used as a Request In Register when the Two-Channel Switch (TCS) feature is installed. This register has four bits assigned as suppressable and non-suppressable REQUEST INS for Channel A and B.

Bit functions are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Suppressable REQUEST IN Channel A</td>
</tr>
<tr>
<td>5</td>
<td>Non-suppressable REQUEST IN</td>
</tr>
<tr>
<td>6</td>
<td>Suppressable REQUEST IN Channel B</td>
</tr>
<tr>
<td>7</td>
<td>Non-suppressable REQUEST IN</td>
</tr>
</tbody>
</table>

3801-2/3420

<table>
<thead>
<tr>
<th>XG1306</th>
<th>213587</th>
<th>See EC History 855958</th>
</tr>
</thead>
</table>

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OPER—ARITHMETIC ADD

ADD/ADDM (HEX CODE A OR B)

1. The LSR byte selected by Field 1 (ROS reg bits 4-7) is placed on the B Bus.
2. The A register is ORed with the constant in Field 2 (ROS reg bits 8-15).
3. The result is placed on the A bus.
4. The A bus and the B bus are added together.
5. The result is placed on the D bus.

If the operation is an ADD, the D bus is stored into the LSR byte addressed by Field 1 and the Hi/Lo latch. The result of an ADDM operation is not stored in an LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the operation is available for branch control. The A Register is reset at the end of the operation.
OPER—LOGICAL AND

AND/ANDM (HEX CODE C OR D)

1. The LSR byte selected by Field 1 is placed on the B bus.
2. The A Register is ORed with the constant in Field 2.
3. The result is placed on the A bus.
4. The A bus and the B bus are ANDed.
5. The result is placed on the D bus.

If the operation is an AND, the D bus is stored back into the LSR byte addressed by Field 1 and the HI/LO latch. The result of an ANDM is not stored in an LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the ANDM operation is available for branch control. The A Register is reset at the end of the operation.

Sample of a Logical AND Instruction
OPER—LOGICAL OR

ORI/ORM (HEX CODE 8 OR 9)

1. The LSR byte selected by Field 1 is placed on the B bus.
2. The A register is ORed with the constant in Field 2.
3. The result is placed on the A bus.
4. The A bus and the B bus are ORed.
5. The result is placed on the D bus.

If the operation is an ORI, the D bus is stored back into the LSR byte addressed by Field 1 and the Hi/Lo latch. The result of an ORM is not stored in the LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the operation is available for branch control. The A Register is reset at the end of the operation.
OPER—LOGICAL EXCLUSIVE OR

XO/XOM (HEX CODE E OR F)

1. The LSR byte selected by Field 1 is placed on the B bus.
2. The A register is ORed with the constant in Field 2.
3. The result is placed on the A bus.
4. The A bus and the B bus are exclusive ORed.
5. The result is placed on the D bus.

If the operation is an XO the D bus is stored in the LSR byte addressed by Field 1 and the Hi/Lo latch. The result of an XOM operation is not stored in an LSR. The result of either operation remains on the D bus until the next ALU operation. While on the D bus, the result of the operation is available for branch control. The A Register is reset at the end of the operation.

Sample Logical Exclusive OR Instruction

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>Mnemonic representation</th>
<th>Reset OP-ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>00010D 1111</td>
<td>ENDWH  XOR CTION XORIN</td>
<td></td>
</tr>
</tbody>
</table>

Programmer's comment
Field 2 mnemonic of the constant
Field 1 mnemonic of the LSR being selected
Mnemonic of Logical Exclusive OR Op code
Mnemonic of the location of the instruction (Label)
Field 2 Hex value of constant
Field 1 Hex value which will select desired LSR
Hex value of Exclusive OR Op code
ROS address at which this instruction is located
**OPER—BRANCH ON CONDITION**

**BOC (HEX CODE 2 OR 3)**

ROS reg Field 1, together with bit 3, is decoded to test one of 32 conditions. If the BOC is met, ROS reg Field 2 is set into the Lo IC. See 52-086 for a complete listing of MP1 and MP2 branch conditions.

The contents of the A reg are not altered.

**Special Condition**—If the two-channel switch or NRZI features are installed, a BOC on these features (BOC on 'MIFTR' or 'NRZFEAT') results in a successful BOC with the Hi IC forced to ROS page 4. See logic diagram.

---

Sample of a Branch On Condition Instruction

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>Mnemonic representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>000286 3F94</td>
<td>BRKVRN BOC OVERRUN SETSTOP</td>
</tr>
</tbody>
</table>

Programmer's comment

Hex 2 mnemonic of the branch to address
Field 1 mnemonic of the branch condition
Mnemonic of the branch on condition Op code
Field 2 hex value of the branch to address
Field 1 + Op code = hex value of the branch condition
Hex value of the BOC Op code
ROS address at which this instruction is located.

(Note: On a BOC met or on a BU, the contents of Field 2 are gated to ROS Address while the IC is being updated.)

---

**Testable Condition**

- BOC Met
- BOC OP Hex 2 or 3
- Page Reg Page 4
- ROS Register
- Lo IC

---

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### OPER—MP1 BRANCHES

#### MP1 BRANCH CONDITIONS

<table>
<thead>
<tr>
<th>BOC Instr. Field 1</th>
<th>ROS Reg Bits</th>
<th>Microprogram Name of Line Sensed</th>
<th>Logic Line Name of Condition Sensed</th>
<th>Branch Cond Logic Page</th>
<th>Source Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0 0 0 0 0</td>
<td>OBUS D Reg equal 0</td>
<td>ALU output all zero ALU1</td>
<td>AB121</td>
<td>AB371</td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>NALCO not ALU carry out</td>
<td>Not ALU carry ALU1</td>
<td>AB121</td>
<td>AB371</td>
</tr>
<tr>
<td>22</td>
<td>1 0</td>
<td>ALUR ALU2/ALU2 Error</td>
<td>Any hardware error ALU2</td>
<td>AB121</td>
<td>AA461</td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>MMFF** MIS or 7-Trk Feature</td>
<td>Feature present ALU1</td>
<td>AB121</td>
<td>AB121</td>
</tr>
<tr>
<td>24</td>
<td>1 0 0</td>
<td>RPE Bus Out parity error</td>
<td>Not Bus Out parity add</td>
<td>AB131</td>
<td>FC151</td>
</tr>
<tr>
<td>25</td>
<td>1 0 0 0</td>
<td>NCUEA Not CU End Chan A</td>
<td>Not CUE pending Chan A</td>
<td>AB131</td>
<td>FC301</td>
</tr>
<tr>
<td>26</td>
<td>1 1 0</td>
<td>SELO Select Out</td>
<td>Gated Select Out</td>
<td>AB131</td>
<td>FC141</td>
</tr>
<tr>
<td>27</td>
<td>1 1 1</td>
<td>DLER Data Check (Not Tape Op)</td>
<td>Write Grp. ‘B’ (Tape Op)</td>
<td>AB131</td>
<td>BW241</td>
</tr>
<tr>
<td>28</td>
<td>1 0 0 0 0</td>
<td>ADDOUT Addr Out A or B</td>
<td>Address Out A B CE</td>
<td>AB171</td>
<td>AB171</td>
</tr>
<tr>
<td>29</td>
<td>1 0 0 1 1</td>
<td>COMOUT Cmd Out A or B</td>
<td>Command Out A B CE</td>
<td>AB171</td>
<td>FC151</td>
</tr>
<tr>
<td>2A</td>
<td>1 0 1 0</td>
<td>STATA Stat A ALU1</td>
<td>Stat A ALU1</td>
<td>AB151</td>
<td>AB141</td>
</tr>
<tr>
<td>2B</td>
<td>1 0 1 1</td>
<td>STAT B Stat B ALU2</td>
<td>Stat B ALU2 to ALU1</td>
<td>AB151</td>
<td>AA141</td>
</tr>
<tr>
<td>2C</td>
<td>1 1 0 0</td>
<td>SELRST Selective Reset</td>
<td>Selective Reset</td>
<td>AB171</td>
<td>FC151</td>
</tr>
<tr>
<td>2D</td>
<td>1 1 0 1</td>
<td>SVCOUT Service Out</td>
<td>Service Out only on write op.</td>
<td>AB171</td>
<td>FC151</td>
</tr>
<tr>
<td>2E</td>
<td>1 1 1 0</td>
<td>SCB Switch to Chan “B”</td>
<td>Switched to Chan “B”</td>
<td>AB161</td>
<td>XM101</td>
</tr>
<tr>
<td>2F</td>
<td>1 1 1 1</td>
<td>POWERST Power On Reset</td>
<td>Math or Gen Reset Chan A, B</td>
<td>AB161</td>
<td>AB161</td>
</tr>
<tr>
<td>30</td>
<td>1 0 0 0 0</td>
<td>DREGD D Reg Bit 0 On</td>
<td>D Bus 0 ALU1</td>
<td>AB121</td>
<td>AB341</td>
</tr>
<tr>
<td>31</td>
<td>1 0 0 1 0</td>
<td>DREG2* D Reg Bit 1 On</td>
<td>D Bus 1 ALU1</td>
<td>AB121</td>
<td>AB341</td>
</tr>
<tr>
<td>32</td>
<td>1 0 0 1 1</td>
<td>DREG3* D Reg Bit 2 On</td>
<td>D Bus 2 ALU1</td>
<td>AB121</td>
<td>AB341</td>
</tr>
<tr>
<td>33</td>
<td>1 0 1 0 1</td>
<td>DREG4* D Reg Bit 3 On</td>
<td>D Bus 3 ALU1</td>
<td>AB121</td>
<td>AB341</td>
</tr>
<tr>
<td>34</td>
<td>1 0 1 0 0</td>
<td>DREGA* D Reg Bit 4 On</td>
<td>D Bus 4 ALU1</td>
<td>AB131</td>
<td>AB351</td>
</tr>
<tr>
<td>35</td>
<td>1 0 1 1 0</td>
<td>DREGA* D Reg Bit 5 On</td>
<td>D Bus 5 ALU1</td>
<td>AB131</td>
<td>AB351</td>
</tr>
<tr>
<td>36</td>
<td>1 1 0 0 0</td>
<td>DREGD D Reg Bit 0 On</td>
<td>D Bus 0 ALU1</td>
<td>AB131</td>
<td>AB351</td>
</tr>
<tr>
<td>37</td>
<td>1 1 0 0 1</td>
<td>DREG* D Reg Bit 1 On</td>
<td>D Bus 1 ALU1</td>
<td>AB131</td>
<td>AB351</td>
</tr>
<tr>
<td>38</td>
<td>1 1 0 1 0</td>
<td>OPRIN Operation In</td>
<td>Channel Operation In</td>
<td>AB171</td>
<td>FC141</td>
</tr>
<tr>
<td>39</td>
<td>1 1 0 1 1</td>
<td>SUPD Suppress Out</td>
<td>Suppress A B</td>
<td>AB171</td>
<td>FC151</td>
</tr>
</tbody>
</table>

---

### Source Logic

- **AB121**
- **AB371**
- **AB151**
- **AA461**
- **AB171**
- **FC041**
- **AB171**
- **XM021**
- **AB161**
- **BW241**
- **BW151**

---

**Notes:**

- **MISR** may be called other names as well.

**If this feature is installed, force HI IC to ROS Page 4.
## MP2 BRANCH CONDITIONS

<table>
<thead>
<tr>
<th>ROC Inst + Field</th>
<th>ROS Reg Bits</th>
<th>Microprogram Name of Line Sensed</th>
<th>Logic Line Name of Condition Sensed</th>
<th>Branch Cond Logic Page</th>
<th>Source Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3 4 5 6 7</td>
<td>DBUG T REG Equal 0 ALU</td>
<td>ALU0</td>
<td>AA121</td>
<td>AA361</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>Not ALU carry</td>
<td>ALU1</td>
<td>AA121</td>
<td>AA361</td>
</tr>
<tr>
<td>22</td>
<td>1</td>
<td>ROCCOTY</td>
<td>ROS rotation (Tape Op)</td>
<td>AA121</td>
<td>CB411</td>
</tr>
<tr>
<td>22</td>
<td>1</td>
<td>CRC NEPR</td>
<td>CRC not equal EPR (Not Tape Op)</td>
<td>AA121</td>
<td>CN011</td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>NORETATT**</td>
<td>Read present</td>
<td>AA121</td>
<td>AA131</td>
</tr>
<tr>
<td>24</td>
<td>1</td>
<td>RD Time</td>
<td>RD Time</td>
<td>AA131</td>
<td>BW221</td>
</tr>
<tr>
<td>25</td>
<td>1</td>
<td>N Seven</td>
<td>N Seven</td>
<td>AA131</td>
<td>AA131</td>
</tr>
<tr>
<td>26</td>
<td>1</td>
<td>TACHFF</td>
<td>Tach Velocity (Write CKT)</td>
<td>AA131</td>
<td>XC031</td>
</tr>
<tr>
<td>27</td>
<td>1</td>
<td>STOP Stop Command</td>
<td>Start Bit 0 ALU1 to ALU2</td>
<td>AA131</td>
<td>AB141</td>
</tr>
<tr>
<td>28</td>
<td>1</td>
<td>ENDTAD End of Zone</td>
<td>End of Data (Tape Op)</td>
<td>XC041</td>
<td>BW241</td>
</tr>
<tr>
<td>28</td>
<td>1</td>
<td>CRROMAT</td>
<td>CRC OK (Not Tape Op)</td>
<td>XC041</td>
<td>CH111</td>
</tr>
<tr>
<td>29</td>
<td>1</td>
<td>NCONVCCK</td>
<td>Data CC Check (Not Tape Op)</td>
<td>XC041</td>
<td>BN011</td>
</tr>
<tr>
<td>29</td>
<td>1</td>
<td>NSAGIC 3D</td>
<td>Inverse TM (Tape Op)</td>
<td>XC041</td>
<td>CC001</td>
</tr>
<tr>
<td>29</td>
<td>1</td>
<td>NCRWB</td>
<td>Start A ALU2</td>
<td>XC041</td>
<td>AA141</td>
</tr>
<tr>
<td>28</td>
<td>1</td>
<td>NSTB Stat B ALU1</td>
<td>Star B ALU1</td>
<td>XC041</td>
<td>AB141</td>
</tr>
<tr>
<td>2C</td>
<td>1</td>
<td>NPTE</td>
<td>Data P Track Only (Tape Op)</td>
<td>XC051</td>
<td>BW231</td>
</tr>
<tr>
<td>2C</td>
<td>1</td>
<td>DEN 556</td>
<td>556 bpi (T-Track)</td>
<td>XC051</td>
<td>BN311</td>
</tr>
<tr>
<td>2D</td>
<td>1</td>
<td>DATA RYD</td>
<td>Data Rdy from DF (Tape Op)</td>
<td>XC051</td>
<td>CH131</td>
</tr>
<tr>
<td>2D</td>
<td>1</td>
<td>RPQ</td>
<td>RPQ</td>
<td>XC051</td>
<td>RPQ</td>
</tr>
<tr>
<td>2E</td>
<td>1</td>
<td>BOR</td>
<td>Beginning of Record (Tape Op)</td>
<td>XC051</td>
<td>CC001</td>
</tr>
<tr>
<td>2F</td>
<td>1</td>
<td>IBG</td>
<td>IBG Detected (Tape Op)</td>
<td>XC051</td>
<td>CC001</td>
</tr>
<tr>
<td>30</td>
<td>1</td>
<td>DREG* D Reg Bit 0 On</td>
<td>D Bus 0 ALU2</td>
<td>AA121</td>
<td>AA331</td>
</tr>
<tr>
<td>31</td>
<td>1</td>
<td>DREG* D Reg Bit 1 On</td>
<td>D Bus 1 ALU2</td>
<td>AA121</td>
<td>AA331</td>
</tr>
<tr>
<td>31</td>
<td>1</td>
<td>DREG* D Reg Bit 2 On</td>
<td>D Bus 2 ALU2</td>
<td>AA121</td>
<td>AA331</td>
</tr>
<tr>
<td>33</td>
<td>1</td>
<td>DREG* D Reg Bit 3 On</td>
<td>D Bus 3 ALU2</td>
<td>AA121</td>
<td>AA331</td>
</tr>
<tr>
<td>34</td>
<td>1</td>
<td>DREG* D Reg Bit 4 On</td>
<td>D Bus 4 ALU2</td>
<td>AA121</td>
<td>AA341</td>
</tr>
<tr>
<td>35</td>
<td>1</td>
<td>DREG* D Reg Bit 5 On</td>
<td>D Bus 5 ALU2</td>
<td>AA131</td>
<td>AA341</td>
</tr>
<tr>
<td>36</td>
<td>1</td>
<td>DREG* D Reg Bit 6 On</td>
<td>D Bus 6 ALU2</td>
<td>AA131</td>
<td>AA341</td>
</tr>
<tr>
<td>37</td>
<td>1</td>
<td>DREG* D Reg Bit 7 On</td>
<td>D Bus 7 ALU2</td>
<td>AA131</td>
<td>AA341</td>
</tr>
<tr>
<td>38</td>
<td>1</td>
<td>NCONVKE</td>
<td>Not Zone Up (Tape Op)</td>
<td>XC051</td>
<td>CC001</td>
</tr>
<tr>
<td>39</td>
<td>1</td>
<td>NCONVKE</td>
<td>Not Zone Up (Tape Op)</td>
<td>XC051</td>
<td>CC001</td>
</tr>
<tr>
<td>39</td>
<td>1</td>
<td>NCONVKE</td>
<td>Not Zone Up (Tape Op)</td>
<td>XC051</td>
<td>CC001</td>
</tr>
</tbody>
</table>

** May be called other names as well.

** If this feature is installed, force Hi IC to ROS Page 4.
1. The contents of ROS reg Fields 1 and 2 are set into the Hi IC and Lo IC.
2. The contents of the A reg are not altered.

Sample of a Branch Unconditional Instruction

- Hex representation
- Mnemonic representation
- Programmer's comment
- Field 1 and 2 - Mnemonic of the branch to address
- Mnemonic of the branch unconditional op code
- Mnemonic of the location of the instruction (Label)
- Field 1 and 2 - Hex value of the branch to address
- Hex value of the BU op code
- ROS address at which the instruction is located

Programmer's comment
Field 1 and 2 - Mnemonic of the branch to address
Mnemonic of the branch unconditional op code
Mnemonic of the location of the instruction (Label)
Field 1 and 2 - Hex value of the branch to address
Hex value of the BU op code
ROS address at which the instruction is located
1. The contents of Field 2 are stored in an LSR selected by Field 1.
2. LSR selection is modified by the condition of the HI/LO latch and ROS register bit 3 (see logic diagram).
3. The A register is reset.

Sample of a STORE Instruction

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>Mnemonic representation</th>
<th>Post Unit Check</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000C7</td>
<td>SETUNTCK STO PNDSTS, UNITCHK</td>
<td>Programmer's comment</td>
</tr>
<tr>
<td></td>
<td>Field 2 mnemonic of the constant</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Field 1 mnemonic of the LSR being selected</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mnemonic of STORE Op code</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mnemonic of the location of the instruction (Label)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Field 2 hex value of constant</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Field 1 hex value which will select desired LSR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hex value of STO Op Code</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ROS address at which this instruction is located</td>
<td></td>
</tr>
</tbody>
</table>
**OPER—TRANSFER LOGIC**

**TRANSFER - XFR (HEX CODE 4 OR 5)**

The hex value (transfer decode) in Field 2 controls all transfer operations. All XFR decodes for both ROS1 and ROS2 are on 52-101.

Some transfer decodes cause data to be transferred between an LSR selected by Field 1 and a hardware register selected by Field 2. LSR selection is modified by the condition of the HI/LO latch and ROS reg bit 3 (see logic diagram).

Some transfer decodes do not select LSRs (that is, Field 1 is ignored). These operations create miscellaneous Set, Reset, and Gating pulses to hardware.

One transfer decode (ROS1 XFR decode of 14) transfers data from one hardware register to another (ROS1 XOUTA to DEAD TRK REG).

Contents of the A register are not altered except as described under special condition 1 below.

**Special Conditions:**

1. Whenever a XFR from LSR to A reg (Field 2 hex 21) is decoded, the XFR is really a logical transfer decode cause data to be transferred from an external register and is being stored in an LSR.

2. Whenever a XFR 'HDWERR' (Field 2 ALU1 = 11 or ALU2 = 44) is decoded, the following actions occur:
   a. Bit 4 in sense byte 11 or 12 (ALU1 or ALU2 respectively) is set.
   b. The UPGM Control Check indicator on the CE panel is turned on.
   c. IC is reset to 000 (ROS1 starts executing at 000—ROS2 holds at 000).

   - For additional information on microprogram control check, see 75-003. "CE Panel Indicators."

2. Whenever these decodes are active, the selection and gating of LSRs is deactivated.

3. For additional information on microprogram control check, see 75-003: "CE Panel Indicators."

---

**Notes:**

1. Only when data is being taken from external registers and is being stored in an LSR.
2. Only when data is being transferred from an LSR to an external register.
3. Whenever these decodes are active, the selection and gating of LSRs is deactivated.

**Sample Transfer Instruction:**

- Hex Representation: 0000A 436D
- Mnemonic representation: RAISEADR XFR CRADR CBI

**Programmers comment:**

- Field 2 (mnemonic of hardware register selected)
- Field 1 (mnemonic of LSR selected)
- Mnemonic of transfer op code
- Mnemonic of the location of the instruction (label)
- Field 2 hex value which will select desired hardware register
- Field 1 hex value which will select desired LSR
- Hex value of XFR op code
- ROS address at which this XFR instruction is located

---

3803-2/3420

XG1700 2739987 849598

See EC History 11-24-79

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## Microprogram Transfer Logic

### Transfer Decode—MP1

<table>
<thead>
<tr>
<th>Field 2</th>
<th>Micro-program Name</th>
<th>Use</th>
<th>Logic Line Names XFR Decode AB181</th>
</tr>
</thead>
<tbody>
<tr>
<td>05</td>
<td>RSTDOMTD</td>
<td>Reset device committed latch</td>
<td>Reset committed latch ALU*</td>
</tr>
<tr>
<td>06</td>
<td>LSR</td>
<td>Set local store latch hi or low</td>
<td>Set LSR hi or lo*</td>
</tr>
<tr>
<td>09</td>
<td>CUREA</td>
<td>Reset CUE or general reset latch int A</td>
<td>Reset CUE Chan A*</td>
</tr>
<tr>
<td>0A</td>
<td>CUREB</td>
<td>Reset CUE or general reset latch int B</td>
<td>Reset CUE Chan B*</td>
</tr>
<tr>
<td>11</td>
<td>HDWERR</td>
<td>Set Sense Byte 11 Bit 4 thrice ROS1 ALU hardware error***</td>
<td>XFR Set Checksum error*</td>
</tr>
<tr>
<td>12</td>
<td>CLEAR</td>
<td>Reset all hardware error latches for ROS1 ROS2 and data flow</td>
<td>Reset Sense Data*</td>
</tr>
<tr>
<td>14</td>
<td>TIP</td>
<td>MP1 XOUTA to Dead Track register</td>
<td>Xfr XOUTA to DT Reg</td>
</tr>
<tr>
<td>18</td>
<td>Spare</td>
<td>Spare Xfr 18</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>AR</td>
<td>LSR to A Reg</td>
<td>Xfr LSR to A Reg</td>
</tr>
<tr>
<td>22</td>
<td>IC</td>
<td>LSR to Instr Ctrl (Lo IC)</td>
<td>Xfr B Bus to IC</td>
</tr>
<tr>
<td>24</td>
<td>TUADR</td>
<td>LSR to TU Address Reg</td>
<td>Xfr TU Address</td>
</tr>
<tr>
<td>28</td>
<td>STAT</td>
<td>LSR to ROS1 Stat Reg</td>
<td>Xfr LSR1 to Stat</td>
</tr>
<tr>
<td>41</td>
<td>XOUTB</td>
<td>LSR to ROS1 XOUTB Reg</td>
<td>Xfr XOUTB to Trap ALU2</td>
</tr>
<tr>
<td>42</td>
<td>XOUTA</td>
<td>LSR to ROS1 XOUTA Reg</td>
<td>Xfr LSR1 to XOUTA</td>
</tr>
<tr>
<td>43**</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>PING</td>
<td>Hardware Error Reset</td>
<td>Reset PING Pulse*</td>
</tr>
<tr>
<td>48</td>
<td>MIST</td>
<td>LSR to set or reset Reg in Tags</td>
<td>Xfr LSR1 to Request Tags</td>
</tr>
<tr>
<td>50</td>
<td>CTI</td>
<td>LSR to Channel Tags in Reg</td>
<td>Xfr LSR1 to Channel Tags</td>
</tr>
<tr>
<td>60</td>
<td>CBI</td>
<td>LSR to Channel Bus in Tags Reg</td>
<td>Xfr LSR1 to Channel Bus In</td>
</tr>
<tr>
<td>81</td>
<td>EXT</td>
<td>ROS2 ALU hardware error reg to LSR</td>
<td>Xfr Ext inputs to LSR1</td>
</tr>
<tr>
<td>82</td>
<td>INHP</td>
<td>Not used</td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>HDW1R</td>
<td>ROS1 ALU hardware error to LSR</td>
<td>Xfr Hardware Reg</td>
</tr>
<tr>
<td>88</td>
<td>XINB</td>
<td>ROS2 XOUTB Reg to ROS1 LSR</td>
<td>Xfr XINB to LSR1</td>
</tr>
<tr>
<td>90</td>
<td>XINA</td>
<td>ROS2 XOUTA Reg to ROS1 LSR</td>
<td>Xfr XINA to LSR1</td>
</tr>
<tr>
<td>90</td>
<td>CBO</td>
<td>Channel Bus Out Reg to LSR</td>
<td>Gate Chan Bus Out to ALU</td>
</tr>
</tbody>
</table>

### Transfer Decode—MP2

<table>
<thead>
<tr>
<th>Field 2</th>
<th>Micro-program Name</th>
<th>Use</th>
<th>Logic Line Names XFR Decode AA171</th>
</tr>
</thead>
<tbody>
<tr>
<td>05</td>
<td></td>
<td>Spare sense byte 11 bit 4 thrice</td>
<td></td>
</tr>
<tr>
<td>06</td>
<td>LSR</td>
<td>Set local store latch hi or to</td>
<td>Set LSR hi or lo*</td>
</tr>
<tr>
<td>09</td>
<td>Reset ERR</td>
<td>Reset error single byte name</td>
<td>File Operation Pulse</td>
</tr>
<tr>
<td>0A</td>
<td>CRC</td>
<td>Shift CRC Pulse</td>
<td>Spae Xfr 1A</td>
</tr>
<tr>
<td>11</td>
<td>Inl</td>
<td>Set Diagnostic Channel Buffer Read</td>
<td>Pulse Reset CRC</td>
</tr>
<tr>
<td>12</td>
<td>POINTERS</td>
<td>Sample pulse to set TIE</td>
<td>Step Format Count</td>
</tr>
<tr>
<td>14</td>
<td>Red Light</td>
<td>Set CE Panel Upreg del DF error</td>
<td>SKR and Del Ctrl</td>
</tr>
<tr>
<td>18</td>
<td>Buff CRC</td>
<td>Sample Buffer CRC error latch</td>
<td>Xfr Xfr 18</td>
</tr>
<tr>
<td>21</td>
<td>AR</td>
<td>LSR to A Reg</td>
<td>Xfr LSR to A Reg</td>
</tr>
<tr>
<td>22</td>
<td>IC</td>
<td>LSR to Instr Ctrl (Lo IC)</td>
<td>Xfr B Bus to IC</td>
</tr>
<tr>
<td>24</td>
<td>TUTAG</td>
<td>LSR to TU Tags Reg</td>
<td>Xfr LSR2 to TU Tags 24</td>
</tr>
<tr>
<td>28</td>
<td>STAT</td>
<td>LSR to ROS2 Stat Reg</td>
<td>Xfr LSR2 to Stat</td>
</tr>
<tr>
<td>41</td>
<td>XOUTB</td>
<td>LSR to ROS2 XOUTB Reg</td>
<td>Xfr LSR2 to XOUTB</td>
</tr>
<tr>
<td>42</td>
<td>XOUTA</td>
<td>LSR to ROS2 XOUTA Reg</td>
<td>Xfr LSR2 to XOUTA</td>
</tr>
<tr>
<td>43**</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>HDWERR</td>
<td>Set Sense byte 12 bit 4 thrice ROS2 ALU hardware error***</td>
<td>Xfr Set Checksum Error</td>
</tr>
<tr>
<td>48</td>
<td>Spare</td>
<td>Spare</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>COMITDO</td>
<td>Reset Device Committed latch pulse</td>
<td>Reset Committed latch Pulse*</td>
</tr>
<tr>
<td>60</td>
<td>TUBO</td>
<td>LSR to TU Bus Out Reg</td>
<td>Xfr LSR to TU Bus Out</td>
</tr>
<tr>
<td>81</td>
<td>TUBI</td>
<td>TU Bus in Reg to LSR</td>
<td>Gate Device Bus In to LSR</td>
</tr>
<tr>
<td>82</td>
<td>INHP</td>
<td>Inhibit Panye on D Bus</td>
<td>Inhibit Panye on D Bus</td>
</tr>
<tr>
<td>84</td>
<td>KADDR</td>
<td>TU Bri Address Reg to LSR</td>
<td>Gate TU Addr to ALU2</td>
</tr>
<tr>
<td>88</td>
<td>XINB</td>
<td>ROS2 XOUTB Reg to ROS2 LSR</td>
<td>Xfr XINB to LSR</td>
</tr>
<tr>
<td>90</td>
<td>XINA</td>
<td>ROS2 XOUTA Reg to ROS2 LSR</td>
<td>Xfr XINA to LSR2</td>
</tr>
</tbody>
</table>

* These transfer operations cause no actual information transfer.
** With transfer decode of 43, transfer decodes 41 and 42 are executed simultaneously.
*** Also sets CE Panel UPGM Error light (Control Check Indicators)

---

![Microprogram Transfer Logic Diagram](image-url)

---

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**Notes:**
- **SG1100:** 27235988
- **84958:** 946627A
- **52-101:** 1. Nov. 78

---

**PATCH STORE MICROCODE LISTINGS**

**ALU1**

<table>
<thead>
<tr>
<th>Instr Addr</th>
<th>Object Code</th>
<th>Source Statement</th>
<th>Patch Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>2DC</td>
<td>ENTER</td>
<td>C400 AND WORK 1, ZERO</td>
<td>ALLOCATED BUSY</td>
</tr>
<tr>
<td>2DD</td>
<td>RETURN</td>
<td>63DE BU 2DE</td>
<td></td>
</tr>
<tr>
<td>328</td>
<td>ENTER</td>
<td>4828 DEPRIM4 XFR STATIMG, STAT</td>
<td>ALTERNATE PATH DEVICE BUSY</td>
</tr>
<tr>
<td>329</td>
<td></td>
<td>38BC BOC STATD. DEPRIM70</td>
<td></td>
</tr>
<tr>
<td>32A</td>
<td></td>
<td>6380 BU 380 FREAREA</td>
<td></td>
</tr>
<tr>
<td>380</td>
<td></td>
<td>3482 FREAREA BOC STATC. CONCONCHA</td>
<td></td>
</tr>
<tr>
<td>381</td>
<td>RETURN</td>
<td>632B BU 328</td>
<td></td>
</tr>
<tr>
<td>382</td>
<td></td>
<td>0981 OKCONCHA ANOM FLAGS, CONCON-CHAIN</td>
<td></td>
</tr>
<tr>
<td>383</td>
<td></td>
<td>2085 BOC DBUS, TAGO</td>
<td></td>
</tr>
<tr>
<td>384</td>
<td>RETURN</td>
<td>6338 PCHOKNA BU 338</td>
<td></td>
</tr>
<tr>
<td>385</td>
<td></td>
<td>0202 TAG0 STD XOUTAIM, SETSTATC</td>
<td></td>
</tr>
<tr>
<td>386</td>
<td></td>
<td>4228 XFR XOUTAIM, STAT</td>
<td></td>
</tr>
<tr>
<td>387</td>
<td></td>
<td>2187 BOC NALCO. PAIDLY</td>
<td></td>
</tr>
<tr>
<td>388</td>
<td></td>
<td>0200 STD XOUTAIM, 0</td>
<td></td>
</tr>
<tr>
<td>38A</td>
<td></td>
<td>4828 XFR STATIMG, STAT</td>
<td></td>
</tr>
<tr>
<td>38B</td>
<td></td>
<td>6384 BU PCHOKNA</td>
<td></td>
</tr>
<tr>
<td>38C</td>
<td>RETURN</td>
<td>633A DEPRIM70 BU 33A</td>
<td></td>
</tr>
<tr>
<td>38E</td>
<td>ENTER</td>
<td>4828 DEPRIM6 XFR STATIMG, STAT</td>
<td></td>
</tr>
<tr>
<td>38F</td>
<td></td>
<td>2282 BOC STATB. CONCONCHA</td>
<td></td>
</tr>
<tr>
<td>337</td>
<td>RETURN</td>
<td>6337 BU 337</td>
<td></td>
</tr>
<tr>
<td>38G</td>
<td></td>
<td>0520 ORI PNSTSS, CUE</td>
<td>EXTRA DEVICE END</td>
</tr>
<tr>
<td>0A4</td>
<td></td>
<td>65OC ANOM PNSTSS, CEND-DEND</td>
<td></td>
</tr>
<tr>
<td>0A5</td>
<td></td>
<td>344A BOC DREG4. RTN1</td>
<td></td>
</tr>
<tr>
<td>0A6</td>
<td></td>
<td>204A BOC DBUS, RTN1</td>
<td></td>
</tr>
<tr>
<td>0A7</td>
<td></td>
<td>4643 XFR PNADODR, XOUTA</td>
<td></td>
</tr>
<tr>
<td>0A8</td>
<td></td>
<td>14EB STD XOUTBM. NDXSTS</td>
<td></td>
</tr>
<tr>
<td>0A9</td>
<td></td>
<td>5441 XFR XOUTBM. XOUTB</td>
<td></td>
</tr>
<tr>
<td>0AA</td>
<td>RETURN</td>
<td>629E RTH1 BU TERMINST2</td>
<td></td>
</tr>
<tr>
<td>0C0</td>
<td>ENTER</td>
<td>1348 STD LINK4, TERMATE</td>
<td>SENSE RESET</td>
</tr>
<tr>
<td>0F1</td>
<td>RETURN</td>
<td>5322 XFR LINK4, IC</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** ENTER Enables the patch store for succeeding instructions, and RETURN Disables the patch store for succeeding instructions.

**ALU 2**

<table>
<thead>
<tr>
<th>Instr Addr</th>
<th>Object Code</th>
<th>Source Statement</th>
<th>Patch Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>213</td>
<td>ENTER</td>
<td>1600 WRTSTR1 STOH SENSE 1, 0</td>
<td>VELOCITY RETRY EXTENSION</td>
</tr>
<tr>
<td>214</td>
<td>RETURN</td>
<td>1300 VELSTR STOH WORK 4, ZERO</td>
<td></td>
</tr>
<tr>
<td>788</td>
<td>ENTER</td>
<td>0200 STD WORK 3, 0</td>
<td></td>
</tr>
<tr>
<td>789</td>
<td>RETURN</td>
<td>1500 STOH WORK 5, ZERO</td>
<td></td>
</tr>
<tr>
<td>15A</td>
<td>ENTER</td>
<td>0708 DODELAY ANOM SENSE 2, HDEN</td>
<td>TURNAROUND DELAY</td>
</tr>
<tr>
<td>15B</td>
<td>RETURN</td>
<td>615C BU 15C</td>
<td></td>
</tr>
<tr>
<td>53E</td>
<td>ENTER</td>
<td>4744 CTRRET6 BU ERASE6</td>
<td>TRUNCATED POSTAMBLE</td>
</tr>
<tr>
<td>744</td>
<td>RETURN</td>
<td>0083 STD WORK 1, X'83</td>
<td></td>
</tr>
<tr>
<td>38E</td>
<td>ENTER</td>
<td>8402 DVRUNTX ORI STATIMG, SETSTATC</td>
<td>ALTERNATE PATH DEVICE BUSY</td>
</tr>
<tr>
<td>38F</td>
<td></td>
<td>6300 BU 3C0 FREAREA</td>
<td></td>
</tr>
<tr>
<td>3C0</td>
<td></td>
<td>4428 FREAREA XFR STATIMG, STAT</td>
<td></td>
</tr>
<tr>
<td>3C1</td>
<td></td>
<td>3A4C PPOLMTIX BOC STATC. TAG00</td>
<td></td>
</tr>
<tr>
<td>3C2</td>
<td></td>
<td>38C6 BOC STATD. EXITPTCH</td>
<td></td>
</tr>
<tr>
<td>3C3</td>
<td></td>
<td>63C1 BU PPOLMTIX</td>
<td></td>
</tr>
<tr>
<td>3C4</td>
<td></td>
<td>0002 TAG00 STD WORK 1, RESET</td>
<td></td>
</tr>
<tr>
<td>3C5</td>
<td></td>
<td>4060 XFR WORK 1, TUDO</td>
<td></td>
</tr>
<tr>
<td>3C6</td>
<td></td>
<td>0004 STD WORK 1, DEVSEL-COMMD</td>
<td></td>
</tr>
<tr>
<td>3C7</td>
<td></td>
<td>4024 XFR WORK 1, TUTAG</td>
<td></td>
</tr>
<tr>
<td>3C8</td>
<td></td>
<td>0000 STD WORK 1, 0</td>
<td></td>
</tr>
<tr>
<td>3C9</td>
<td></td>
<td>4000 ADD WORK 1, 0</td>
<td></td>
</tr>
<tr>
<td>3CA</td>
<td></td>
<td>4034 XFR WORK 1, TUTAG</td>
<td></td>
</tr>
<tr>
<td>3CB</td>
<td></td>
<td>4034 TAG002 ADD WORK 1, 36</td>
<td></td>
</tr>
<tr>
<td>3CC</td>
<td></td>
<td>21CB BOC NALCO. TAG002</td>
<td></td>
</tr>
<tr>
<td>3CD</td>
<td></td>
<td>4050 XFR CONSTM</td>
<td></td>
</tr>
<tr>
<td>3CE</td>
<td>RETURN</td>
<td>6370 EXITPTCH BU POLLMTIX</td>
<td></td>
</tr>
</tbody>
</table>

**52-102**
OPER—OSCILLATOR

OSCILLATOR GATING

Crystal oscillators supply the basic timing pulses that drive the clocks and counters throughout the 3803. The Microsecond Frequency used at any specific time depends on the speed of the tape unit addressed. The Detection Register gates the correct frequency. The master clock controls the read clock stepping pulses.
# READ/WRITE CLOCKS AND COUNTERS

<table>
<thead>
<tr>
<th>CLOCK/COUNTER</th>
<th>ALD</th>
<th>CONTROL [Reset]</th>
<th>INPUT</th>
<th>OUTPUT</th>
<th>MLM PAGE</th>
<th>USE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Clock</td>
<td>BW101</td>
<td>Wr Cond</td>
<td>usec Freq</td>
<td>WC3 - 11</td>
<td>53-020</td>
<td>Flip write triggers at WC7. Sample VRC at WC3 and 11. Step Write Counter at WC3 and 11.</td>
</tr>
<tr>
<td>Write Counter</td>
<td>BW901/BW101</td>
<td>XOUTA 48250l/WC9/WC11/WC5/WC3</td>
<td>0 - 4</td>
<td>Cntr 0 - 4</td>
<td>53-020</td>
<td>Gate Write Encoders BW011 - 051</td>
</tr>
<tr>
<td>Byte Counter</td>
<td>BW901</td>
<td>Tape Op Repowered</td>
<td>75 - 25 Del</td>
<td></td>
<td>53-025</td>
<td>Gates CRC and Residual bytes.</td>
</tr>
<tr>
<td>Group Buffer Counter</td>
<td>CB441</td>
<td>Tape Op</td>
<td>WC3 - 75 or 0 - 75</td>
<td>Binary Counter 1 - 4</td>
<td>53-090</td>
<td>Group Buffer and 6250 Memory Address Control.</td>
</tr>
<tr>
<td>CRIC</td>
<td>BR011</td>
<td>Wr Cyc Latch</td>
<td>75 - 25</td>
<td>CRIC 1 - 5</td>
<td>53-025</td>
<td>Channel Buffer Read In.</td>
</tr>
<tr>
<td>RIC</td>
<td>BR011</td>
<td>Rd Cyc Latch</td>
<td>75 - 25</td>
<td>ROC 1 - 5</td>
<td>53-025</td>
<td>Channel Buffer Read Out.</td>
</tr>
<tr>
<td>Frame Counters</td>
<td>CJ021</td>
<td>Counter Resets</td>
<td>PE Decode A8, A7, A6 - 75</td>
<td>Count = 8</td>
<td>--</td>
<td>Reset Valid Pointer and Hardware Pointer Latches.</td>
</tr>
<tr>
<td>Frame Buffer Counter</td>
<td>CH041</td>
<td>Tape Op</td>
<td>25 - 75</td>
<td>FB1, 2, 4 and Decode 0 - 7</td>
<td>53-095</td>
<td>Controls ECC Group Buffer Address, Error Matrix Switching, Data Correction, and Data Xfer to Channel Buffer.</td>
</tr>
<tr>
<td>RIC (8)</td>
<td>CDx11</td>
<td>Tape Op or Dead Track</td>
<td>8250 Ones or Step RIC</td>
<td>Count 10 Ones or Skip Addr 0 - 31</td>
<td>53-080</td>
<td>Gates address to write bytes into Skew Buffer, and counts 10 ones (8250) or 10 zeros (PE) during preamble.</td>
</tr>
<tr>
<td>ROC (1)</td>
<td>CB411</td>
<td>Tape Op</td>
<td>Step ROC (R02)</td>
<td>ROC 1 - 5</td>
<td>53-080</td>
<td>Gates address to read bytes out of Skew Buffer.</td>
</tr>
<tr>
<td>Microprocessor Clocks</td>
<td>A8011/AA011</td>
<td>Reset ALU/IC</td>
<td>20.48 MHz</td>
<td>B pulses at 0, 25, 50, 75, 100, 125, 150, 175 Nsec</td>
<td>52-005</td>
<td>Controls microprocessor operations.</td>
</tr>
</tbody>
</table>
# OPER—CLOCK CHART

## DATA FLOW CLOCK

<table>
<thead>
<tr>
<th>Clock Output</th>
<th>ALD</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - 50 Clock Bus YA</td>
<td>CD151</td>
<td>Skew and Master Clock Zone 1</td>
</tr>
<tr>
<td>CD251</td>
<td>Skew and Master Clock Zone 2</td>
<td></td>
</tr>
<tr>
<td>CD351</td>
<td>Skew and Master Clock Zone 3</td>
<td></td>
</tr>
<tr>
<td>CH061</td>
<td>Format Character Clocks</td>
<td></td>
</tr>
<tr>
<td>CH081</td>
<td>Residual Frame Controls</td>
<td></td>
</tr>
</tbody>
</table>

| 0 - 50 Clock Bus YB | CB411 | ROC Counter |
| CB101 | E1 Register |
| CN281 | NRZI Hi Clip and Read VRC |

| 0 - 50 Delayed | BS051 | Read Buffer Controls |

| 0 - 50 Clock Bus A1 Delayed | BN051 | DC and Xlate Controls |
| BR071 | Cycle Request Latches |

| -25 - 75 Clock Bus YA | CD151 | Skew and Master Clock Zone 1 |
| CD251 | Skew and Master Clock Zone 2 |
| CD351 | Skew and Master Clock Zone 3 |
| CH061 | Format Character Clocks |
| CH141 | Modular 7 Residue Compare Equal |

| -25 - 75 Clock Bus YB | CB811 | ROC Counter |
| CB351 | Skew and Master Clock Zone 3 |
| CN281 | NRZI Hi Clip and Read VRC |

| -25 - 75 Clock Bus A1 Delayed | BN071 | Read DC and Xlate Control 17-trk Model |
| BR071 | Cycle Request Latches |

| -75 - 25 Delayed | BS051 | Read Buffer Controls |
WRITE CLOCK AND WRITE COUNTER

WRITE CLOCK

<table>
<thead>
<tr>
<th>WC Pulse</th>
<th>ALD</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>BW151</td>
<td>Reset Error Sample. With CNTR=0. Gate Write Controls A1, A2, Mark1, Mark2. Format. Initiate Sample. All Ones Branch Condition.</td>
</tr>
<tr>
<td>1</td>
<td>BW151</td>
<td>Reset WRITE TIME Gate.</td>
</tr>
<tr>
<td></td>
<td>BW151</td>
<td>With WRITE CNTR=0. Flip CNTR B FF. (Write Group B Branch)</td>
</tr>
<tr>
<td>2</td>
<td>BW151</td>
<td>Gate SET 2ND BUFFER.</td>
</tr>
<tr>
<td>3</td>
<td>BW151</td>
<td>Sample WR TGR VRC.</td>
</tr>
<tr>
<td>5</td>
<td>BW091</td>
<td>PE Diagnostic Mode.</td>
</tr>
<tr>
<td>6</td>
<td>BW151</td>
<td>Set SAMPLE FL if CNTR 4 is On. Flip DDD/EVEN CHAR FF.</td>
</tr>
<tr>
<td>7</td>
<td>BW151</td>
<td>Generate WR TGR Gate if not NRZ.</td>
</tr>
<tr>
<td>9</td>
<td>BW091</td>
<td>Step WRITE COUNTER 1.</td>
</tr>
<tr>
<td>11</td>
<td>BW091</td>
<td>Step WRITE COUNTER 4 if 1 and 2 are off.</td>
</tr>
<tr>
<td></td>
<td>BW101</td>
<td>Restart Clock (8250).</td>
</tr>
<tr>
<td>13</td>
<td>BW151</td>
<td>Set WRITE TIME GATE (PE and NRZ).</td>
</tr>
<tr>
<td>15</td>
<td>BW151</td>
<td>Gate SAMPLE SET trigger.</td>
</tr>
<tr>
<td></td>
<td>BW151</td>
<td>Generate WRITE TRIGGER GATE.</td>
</tr>
<tr>
<td></td>
<td>BW101</td>
<td>Restart Clock (PE and NRZ).</td>
</tr>
</tbody>
</table>

WRITE COUNTER

<table>
<thead>
<tr>
<th>Wr Ctr</th>
<th>ALD</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>BW151</td>
<td>With WC0. See WC0 Pulse.</td>
</tr>
<tr>
<td></td>
<td>BW151</td>
<td>Gate END MARK FL.</td>
</tr>
<tr>
<td></td>
<td>BW151</td>
<td>Gate CNTR B FL at WC1.</td>
</tr>
<tr>
<td>1, 2, 4A</td>
<td>BW011-051</td>
<td>Gate Write Encoder.</td>
</tr>
<tr>
<td>4</td>
<td>BW151</td>
<td>With WC6 and Not NRZ, Sample BUFFER EMPTY.</td>
</tr>
<tr>
<td></td>
<td>BW151</td>
<td>With WC15 and NRZ, Sample BUFFER EMPTY.</td>
</tr>
</tbody>
</table>

Write Counter: Gates bytes to the write triggers.
OPER—LOGIC CIRCUITS

WRITE GROUP BUFFER CONTROL

--- Diagram of WRITE GROUP BUFFER CONTROL circuitry. The diagram includes various logic gate symbols, control signals, and connection points labeled with various instructions such as "-Set Byte 1," "-Set Byte 2," "-Set Byte 3," and "-Set Byte 4." The diagram illustrates the flow of data and control signals through the circuit components.

--- Additional notes and labels:
- "-6250 Mode"
- "+Read Cycle"
- "Pseudo Cycle"
- "-Fill Write Group Buffer"
- "-75-125"
- "-75-100"
- "-Stop to Data Flow"
- "End Write Seq"
- "End Cond"
- "+Set CRIC Reg"
- "Byte Ctr 1"
- "Byte Ctr 2"
- "Byte Ctr 4"
- "CRIC 1"
- "CRIC 2"
- "CRIC 4"
- "CRC Cntl"
- "Byte Dist 2"
- "Byte Dist 4"
- "Byte Resid Cntl"
- "Write CRC or Residual (Module 7)"

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OPER—LOGIC CIRCUITS (Cont’d)

- Read Cycle
  53-030
  A1F2
  BR021
  Tape Op
  Read (Reset)
  A1F2
  BR021
  Stop to Data Flow
  A1F2
  BR021
  Read (Reset)
  Channel Buffer Branch
  A1F2
  BR021
  To Microprocessor

+ Read Cycle
  53-030
  A1F2
  (Reset)
  Channel Buffer Branch
  A1F2
  BR021
  Stop to Data Flow
  A1F2
  BR021
  Read (Reset)
  Channel Buffer Branch
  A1F2
  BR021
  To Microprocessor

- Write Cycle
  53-030
  A1F2
  (Reset)
  Channel Buffer Branch
  A1F2
  BR021
  Stop to Data Flow
  A1F2
  BR021
  Read (Reset)
  Channel Buffer Branch
  A1F2
  BR021
  To Microprocessor

- Difference Reset
  53-030
  A1F2
  BR021
  Read Req or Write Cycle
  A1F2
  BR021
  Stop to Data Flow
  A1F2
  BR021
  To Microprocessor

- Difference Reset
  X12/2001
  2735982
  See EC History
  843988
  1 Sep 79
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WRITE SERVICE CONTROLS

Objectives:
1. The ALTERNATE flip flop controls alternate Service In and Data In cycles.
2. The PERMIT flip latch ensures that multiple tag lines will not be active at the same time.
3. Buffer Write Cycle or Req controls Service Different and Buffer.
Objective:
This register is a temporary buffer for the channel buffer write byte from either interface bus out or read data track.

Objective:
An ORC byte character is generated for each ECC group.

Objective:
The POINTER register accumulates the pointers for one group of 6250 data. These pointers are used for correction as required.
Objectives:
1. During a read operation, the A/B registers buffer read data to the CHANNEL BUS IN, each alternately receiving a data byte.
2. During a write operation, output from the A/B register generates CRC bits.
CRC A, B, C, D

CRC A:
- Rd Data Trk P. 0-7
- Read and Tape Op
- Write and Tape Op
- Bus Out Bit P. 0-7

CRC B:
- Read Reg Bits

CRC C:
- Read Data Trk P. 0-7
- Forward Repo
- Read Data Trk 7-0, P

CRC D:
- Rd Data Trk P. 0-7
- Store D Pulse
OPER—CRC DESCRIPTION

CYCLIC REDUNDANCY CHECK (CRC) GENERATION

Two cyclic redundancy check (CRC) errors set sense bits. A CRC error sets sense byte 3, bit 3 and a CRC III error sets sense byte 9, bit 3. See 50-000, 50-001, and 50-002 for relationships to data flow.

CRC GENERATION DURING 9-TRACK WRITE OPERATIONS

Write data from the channel is shifted into the CRC A register (50-000), byte by byte, as the channel buffer is loaded. As the data is being read out of the channel buffer, the output is shifted into the CRC B register (50-000), as demanded by the write section.

Accumulated contents of CRC A and CRC B registers are compared when the channel buffer empties (53-066). Dropping or picking up a bit or bits in transferring data through the channel buffer results in a mismatch and sets P COMPARE ERROR (byte 3 bit 7) and sense byte 9, bit 2.

a. 6250 bpi Mode

The content of the CRC A register is written on tape as the CRC III byte. The CRC III byte is also shifted into the Write CRC generator (50-001) with data and other bytes. Content of the WRITE CRC register is also written on tape as a CRC byte.

b. PE Mode

CRC III is generated during PE operations for write checking, but is not written on tape.

c. 9-Track NRZI Mode

Only the accumulated data bytes generate the CRC byte.

CRC USE DURING READ BACK CHECK OF WRITE OPERATIONS

a. 6250 bpi Mode

Data previously written is read back through the normal read data path and the Check CRC Byte is stored in the CRC D register (50-000). CRC D is compared with CRC B; a mismatch sets CRC III error and sense byte 9, bit 3.

During the read back check, all data bytes and other bytes are shifted in the READ CRC register. The result should be a match pattern in the READ CRC register. Any other pattern sets CRC error only.

b. PE/9-Track NRZI Modes

Only data bytes are read back and stored in CRC C register (50-000). Contents of CRC C register are compared with CRC B (53-066). A mismatch sets CRC III error and sense byte 9, bit 3.

c. 9-Track NRZI Mode

All data bytes are read back and combined with the CRC byte in the READ CRC register (53-065). The accumulated bits should result in a match pattern. Any other pattern sets CRC Error.

CRC GENERATION DURING 9-TRACK READ FORWARD OPERATIONS

CRC generation during a read forward operation is similar to CRC generation during the read back check of a write operation. Data bytes read from tape go to the channel buffer (50-000) and also into CRC A register. CHANNEL BUFFER FULL initiates data transfer to the Interface Bus In and also shifts bytes into CRC B register. Accumulated contents of CRC A and CRC B registers are compared when the channel buffer empties (53-066). Dropping or picking up a bit or bits in transferring data through the channel buffer results in a mismatch and sets P COMPARE ERROR (byte 3 bit 7) and sense byte 9, bit 2.

6250 bpi Mode:

CRC generation and use during 6250 read operations is identical to CRC use during read back checking.

CRC GENERATION DURING 9-TRACK READ BACKWARD OPERATIONS

CRC generation detects the loss or gain of bits transferred through the channel buffer during both read backward and read forward operations.

6250 bpi Mode:

Read CRC error determinations are identical in 6250 read backward and read back checking operations except that bytes are shifted into registers in a reverse order.

The CRC C register accumulates combined data bytes and the check CRC bytes. With no read errors, the result should be a match pattern in the CRC C register. Any other pattern sets CRC III error and sense byte 9, bit 3.

7-Track NRZI operations do not use a CRC checking procedure.
WRITE TRIGGER OPERATION

Data bytes from the CHANNEL BUS OUT consist of binary ones and binary zeros. The tape control and tape unit convert these binary bits to flux changes on tape. The 6250 bpi and NRZI methods of writing distinguish ones from zeros by a flux change for a one and no flux change for a zero.

Phase encoding (PE) distinguishes ones from zeros by the direction of flux change. A flux change in one direction indicates a one bit and in the opposite direction indicates a zero bit.

Write triggers produce magnetic flux changes on tape in one direction when they are flipped on and in the opposite direction when they are flipped off.

6250 BPI WRITE TRIGGER OPERATION

6250 bpi method of writing on tape flips the WRITE TRIGGERS at Write Clock 7 to write one bits on tape. The Write Clock runs to Write Clock 11 and then starts over.

NRZI WRITE TRIGGER OPERATION

For a NRZI write operation, each byte is set into the write encoder. For each one-bit of the byte, the corresponding write trigger is flipped to write a flux reversal on tape. For zero-bits of each byte, the write trigger is not flipped, and thus, no flux reversal is written.

PE WRITE TRIGGER OPERATION

In PE operation, the write clock runs from 0 through 15 for each cycle.

Each byte is set into the write encoder. For each bit of the byte that is a one, the corresponding write trigger is "set up" at WC7. All write triggers are flipped at WC15 to write a byte on tape with flux reversals in one direction for one bits and in the opposite direction for zero bits.
The DEAD TRACK register contains one latch for each track. After ROC has cycled, the Pointer Bus controls setting of DEAD TRACK REGISTER latches. Prior to a ROC cycle, +SOME TRACK MARGINAL indicates that a track is failing and the voting circuits determine which track(s) should be dead tracked. During a PE Write, if a READ BUS signal is too weak or occurs at the wrong time (phase error), the DEAD TRACK latch for that track is turned on to activate correction circuits. The read data for that track is ignored for the remainder of the block or until the DEAD TRACK latch is reset. Once activated, the DEAD TRACK latch remains active until reset by +SENSE RESET or by a resync and time sense (6250). An active DEAD TRACK latch deactivates the RIC for its track, removing the RIC from the RIC-ROC compare and blocking any data from entering the skew buffers for that track.
OPER—RIC/ROC

RIC-ROC

The read section contains nine 32-position Read In Counters (RICs), one for each track, and one 32-position Read Out Counter (ROC).

A RIC specifies which skew buffer position receives the next one or zero bit for a data byte read from tape. When a bit is detected, it is placed in the skew buffer, and the RIC for that track is stepped to the next position.

The ROC selects the skew buffer position from which a byte is transferred to the group buffer.

Initially, all RICs and ROC are reset. As each bit of the first data byte enters skew buffer position 0, the corresponding RIC is stepped from 0 to 1. When none of the RICs are equal to ROC, RIC-ROC NO-COMPARE is activated, indicating that all bits of the byte have entered the skew buffer. RIC-ROC NO-COMPARE gates outputs of the ROC counter to the ROC image register and steps the Read Ready Counter, which times the read out of the skew buffer.

The operation continues in this manner until GROUP BUFFER FULL or IBG becomes active to stop the read out.
SKEW DETECTION

ROCs 2
ROCs 4
ROCs 8
ROCs 16

Compare

(Array) (9)

+PE Writ Skew Tr P

PE Writ Skew

CD151
CD251
CD351

+PE Write Skew Zn 1

+PE Write Skew

Zn 3

A

+PE Mode

OR

DOT

FL

+Write and Tape Op

6250 Write Skew

(Gates GB Full)

+End Sample ST

+Almost Skew Tr P

+Almost Skew

Tr P

6250 Write Skew Zn 1

+Some Track Marginal

(To Dead Track

Control)

Zn 3

A

Some Track Marginal

93-075

+Write Skew Error

OR

DOT

53-085

OR

DOT

Write Skew Error

53-085

Skew Check

Lamp (CE Panel)

Sense Byte 3, Bit 2

Skew

Skew Error

A

1K3

BW241

One for each track

One for each zone

One circuit

OR

(9)

OR

(9)

OR

(9)

OR

(9)

A

A

A

One for each track

One for each zone

One circuit

OR

(9)

OR

(9)

OR

(9)

53-085
GROUP BUFFER COUNTER

Objectives:
1. Limits skew buffer read out to one 6250 group of data (5 bytes per group).
2. Controls skew buffer read out in PE Mode after the first five bytes are read out to give one-byte-in and one-byte-out control.
3. Controls translator operation during a group buffer read out to convert five parallel 6250 bytes into four serial data bytes.
4. Controls translator operation to detect 6250 characters and to decode format marks.
5. Group buffer counter counts to five and conditions translator for read out to ECC group buffer. If ECC group buffer is full, counter stepping is inhibited.
READ CYCLE CONTROLS

Cycle Time

<table>
<thead>
<tr>
<th>A Cycle</th>
<th>B Cycle</th>
<th>All Cycle</th>
<th>ABC Cycle</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 2 3 4 5 6 7</td>
<td>0 1 2 3 4 5 6 7</td>
<td>0 1 2 3 4 5 6 7</td>
<td>0 1 2 3 4 5 6 7</td>
<td>0 1 2 3 4 5 6 7</td>
</tr>
<tr>
<td>Data to ECC Group Buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Group Buffer 1 Full</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ECC Group Buffer Full</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Set ECC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transfer Group A to ECC</td>
<td>Transfer Group B to ECC</td>
<td>If no error, skip ABC Cycle.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Clock is initialized with 00-07 only when TAPE OP becomes active.
Format Groups and PE mode use "A" cycles only.
OPER—INTERFACE

INITIAL SELECTION OF TAPE UNIT

DESCRIPTION
The initial selection sequence is the communication between the channel and tape control that initiates an operation.

During initial selection, the tape control obtains initial status information that indicates the availability of the selected tape unit. If the tape unit response indicates it is available, the tape control activates lines that tell the tape unit to perform a specific command. In response to the command, the tape unit furnishes additional status information that indicates its ability to perform the specified command. If the tape unit is capable of performing the command, the tape control activates MOVE to the tape unit.

The communication between the tape control and tape unit is over the device interface lines.

DEVICE INTERFACE LINES
The device interface is composed of the following lines that perform the listed functions:

- BUS OUT (9 lines): Transmits commands, amplitude sensing levels, write data, and sense byte identification to the tape unit.
- MOVE tag: Initiates tape motion.
- COMMAND tag: In conjunction with BUS OUT, initiates the execution of a command.
- CONTROL tag: In conjunction with BUS OUT, initiates the execution of a control command.
- CLOCK/METER OUT: Causes the tape unit usage meter to run.
- BUS IN (9 lines): Transmits status, sense information, and read data to the tape control.
- TACHOMETER IN/BUSY IN: When no tag is active, this line indicates that the tape unit is busy. When any OUT tag is active, this line carries the capstan tachometer pulses to the tape control.

INTERRUPT: This line signals the tape control that one of the following unusual conditions has occurred in the tape unit:
- Load Check
- Loss of mechanical ready during a rewind
- Transition from not ready to ready status occurred
- Transition from ready to not ready status occurred while the MOVE tag was active
- BOT was sensed during a read backward operation

Example of BUS OUT Tag Status

<table>
<thead>
<tr>
<th>BUS OUT Bit</th>
<th>COMMAND Tag Active</th>
<th>CONTROL Tag Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Backward read</td>
<td>Rewind Unload</td>
</tr>
<tr>
<td>1</td>
<td>Forward read</td>
<td>Not used</td>
</tr>
<tr>
<td>2</td>
<td>Diagnostic (L/WRI)</td>
<td>(Mod 4, 6, 8 only) High Sense ON</td>
</tr>
<tr>
<td>3</td>
<td>Pulse</td>
<td>NRZI or 6250 bpi mode</td>
</tr>
<tr>
<td>4</td>
<td>Write</td>
<td>(Mod 4, 6, 8 only) Diagnostic (set low sense)</td>
</tr>
<tr>
<td>5</td>
<td>Set Extend Stop (Mod 4, 6, 8 only) Data security erase</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Reset error latches</td>
<td>(Mod 4, 6, 8 only) Erase Status</td>
</tr>
<tr>
<td>7</td>
<td>Not used</td>
<td>Rewind</td>
</tr>
</tbody>
</table>

Example of BUS IN Tag Status

<table>
<thead>
<tr>
<th>BUS IN Bit</th>
<th>COMMAND STATUS Byte</th>
<th>CONTROL STATUS Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Backward</td>
<td>Rewind Unload</td>
</tr>
<tr>
<td>1</td>
<td>Gap control</td>
<td>Not used</td>
</tr>
<tr>
<td>2</td>
<td>Diagnostic mode</td>
<td>(Mod 4, 6, 8 only) High Sense ON</td>
</tr>
<tr>
<td>3</td>
<td>(Mod 4, 6, 8 only)</td>
<td>Opposite direction</td>
</tr>
<tr>
<td>4</td>
<td>Write status</td>
<td>(Mod 4, 6, 8 only) Low Sense ON</td>
</tr>
<tr>
<td>5</td>
<td>Extended Stop (Mod 4, 6, 8 only) Erase</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Unit Check</td>
<td>(Mod 4, 6, 8 only) Erase status ON</td>
</tr>
<tr>
<td>7</td>
<td>(Mod 4, 6, 8 only)</td>
<td>Positioning Rewind</td>
</tr>
</tbody>
</table>
# OPER—COMMAND TYPES

## COMMAND SEQUENCE (TAG LINES/STATUS)

<table>
<thead>
<tr>
<th>Write, LIR, Read, Read Backward</th>
<th>Initial Selection</th>
<th>Data Transfer</th>
<th>Ending Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
<td>Command Out</td>
<td>Status In (Present)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sense, Sense Reserve, Sense Release</th>
<th>Initial Selection</th>
<th>(First Sense Byte)</th>
<th>(Last Sense Byte)</th>
<th>Ending Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
<td>Command Out</td>
<td>Status In (Present)</td>
<td>Service Out</td>
</tr>
</tbody>
</table>

**BURST COMMANDS**

<table>
<thead>
<tr>
<th>Request Track in Error</th>
<th>Initial Selection</th>
<th>Data Transfer (TIE Byte)</th>
<th>Ending Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
<td>Command Out</td>
<td>Status In (Present)</td>
</tr>
</tbody>
</table>

**MOTION CONTROL COMMANDS**

<table>
<thead>
<tr>
<th>Rewind</th>
<th>Initial Selection</th>
<th>Tape Rewinding</th>
<th>Interrupt</th>
<th>Ending Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
<td>Command Out</td>
<td>Status In (CHE)</td>
<td>Service Out</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Rewind-Unload</th>
<th>Initial Selection</th>
<th>Interrupt</th>
<th>Ending Status</th>
<th>Interrupt</th>
<th>Ending Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
<td>Command Out</td>
<td>Status In (CHE)</td>
<td>Service Out</td>
<td>Request In</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Write Tape Mark, Space, Erase Gap, Data Security Erase</th>
<th>Initial Selection</th>
<th>Tape Motion</th>
<th>Interrupt</th>
<th>Ending Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
<td>Command Out</td>
<td>Status In (CHE)</td>
<td>Service Out</td>
</tr>
</tbody>
</table>

**NON-MOTION CONTROL COMMANDS**

<table>
<thead>
<tr>
<th>No-Op, Mode Set, Diagnostic Mode Set</th>
<th>Initial Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
</tr>
</tbody>
</table>

**INSTRUCTIONS**

<table>
<thead>
<tr>
<th>Test I/O</th>
<th>Initial Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Out</td>
<td>Address In</td>
</tr>
</tbody>
</table>

**Notes:**

1. Request-in interrupt sequence initiated when 'rewinding' line goes from active to inactive state.
2. Request-in interrupt sequence initiated only if operator reloads and 'readies' tape unit to generate second 'device end.'
OPER—SELECTION AND PRIORITY

TAPE CONTROL AND TAPE UNIT SELECTION

A tape control and tape unit are selected by placing the combined tape control and tape unit address on CHANNEL BUS OUT. The address on CHANNEL BUS OUT is compared with the address assigned to the tape control. (To assign a tape control address, see 90-110.)

If the address on CHANNEL BUS OUT matches the internally generated tape control address, ADDRESS COMPARE is activated and the tape unit address is gated to the TU SELECT register.

The tape unit addresses are determined by the tailgate position to which the tape unit is cabled.

TAPE CONTROL AND TAPE UNIT ADDRESSING

The combined tape control and tape unit address is contained in a single byte. In subsystems without the 16 address feature, bits 0 through 4 are used for the tape control address, and bits 5 through 7 are used for the tape unit address. In subsystems with the 16 address feature, bits 0 through 3 are used for the tape control address, bits 4 through 7 are used for the tape unit address.

Address Byte Structure (8 tape units)

Address Byte Structure (16 tape units)
OPER—SELECTION

TAPE UNIT SELECTION LOGIC

TAPE UNIT SELECTION PRIORITY

On subsystems with a Device Switching feature, more than one tape control may try to access the same tape unit at the same time. To handle this situation, the switching logic uses card jumpers that establish priorities for each tape control in the subsystem. Tape controls with device switching features are shipped with device selection priorities already plugged. It should not be necessary to change these priorities.

Tape Unit Selection

1. A four bit address on the B Bus is set in the TAPE UNIT ADDRESS SELECT register.
2. The inbound and outbound address decoders then decode ROS2's TUTAG BIT 4 and the Address Select lines.
3. One of eight select lines is active to the crosspoint switches to determine which tape unit will be used.

4. On machines with the Two-Channel Switch feature installed, the TUDR BIT 2 SELECT B line and the BUSY/TACH line generate METERING IN to channel B. The NOT TUDR BIT 2 SELECT B line and the BUSY/TACH line generate METERING IN to channel A.
5. This circuit interrogates a tape unit’s status without selecting the tape unit.

See Section 90.

Tape Unit Bus

The inbound and outbound address decoders then decode ROS2's TUTAG BIT 4 and the Address Select lines. One of eight select lines is active to the crosspoint switches to determine which tape unit will be used.

See Section 90.
OPER—PRIORITY

CHANNEL PRIORITY CIRCUITS

- 'Select out' priority determines the order in which tape controls are selected if more than one tape control requires service at the same time.
- A tape control’s 'select out' priority is determined by jumpers in the tape control and by the tape control’s location on the I/O interface.
- The select signal leaves channel on the SELECT OUT line and returns to channel on the SELECT IN line if it is not ‘trapped’ by a tape control requiring service.
- A tape control not requiring service propagates the select signal to the next lower priority tape control.
- Jumpers in each tape control determine whether the tape control will respond to the SELECT OUT line ('select out priority high') or the SELECT IN line ('select out priority low').

- All units shipped from the factory are jumpered for high 'select out' priority. If it is necessary to change the priority, see 90-120.
- Device Selection priority circuits are present in tape subsystems where a tape unit is accessed by more than one tape control. See 54-010. These circuits act as 'tie breakers' when two or more tape controls are trying to select a tape unit at the same time.
- Additional jumpers in the switching logic of each 'host' tape control establish device selection priorities (1, 2, 3, or 4) for each tape control in a tape switching configuration.
OPER—LWR LOGIC

LOOP WRITE TO READ (LWR)

Loop write to read allows checking tape control and tape unit data and control paths without moving tape. The LWR (8B) command can be initiated from the processing unit or the CE panel. An LWR performed from the processing unit uses the same data path as a normal write operation. The following sense byte errors cannot be detected:

Data Checks:
- Early Begin Read Back check
- Early Ending Read Back check
- Slow Begin Read Back check
- Velocity During Write check

Equipment Checks:
- No Block on Record Read Back check
- No Block Detected on WTM Velocity check
- Tach Start failure

A loop write to read operation is initiated from the CE panel by entering the command code (8B), and it receives its data from one of two locations. A count of service responses generates a ripple pattern, which is selected by putting the Command Control switch at the Ripple position. The fixed data comes from the Write Data switches when the Command Control switch is in the Write Data position. A CE panel LWR writes continuously until it is stopped by operating the Reset switch, except when the LWR with gaps jumper is installed (A1S2G08 to ground).

LWR TAPE UNIT OPERATION

The tape control activates SET DIAGNOSTIC and the COMMAND tag. The DIAGNOSTIC MODE latch is set in the tape unit (FT104). READ/WRITE GATE (FT104) ANDs with DIAGNOSTIC MODE to activate LOOP SELECT (FT147). The tape control activates the MOVE tag and drops the COMMAND tag, then the diagnostic latch degates Move command to prevent tape motion. LOOP SELECT active gates BUS OUT data back to tape control via the tape unit response lines.
BASIC RECORDING TECHNIQUE

DESCRIPTION
Three types of recording techniques are used in the IBM 3803/2/3420:
- Phase encoded (PE)
- Non-return to zero IBM (NRZI)
- 6250 bpi group coded recording (GCR)

Data bytes contain a combination of one and zero bits to represent binary ones and zeros. The PE tape system uses a flux change from minus to plus to represent a one bit, and a flux change from plus to minus to represent a zero bit. (The NRZI system uses a flux change in either direction to represent a one bit and lack of a flux change to represent a zero bit.) Flux changes on tape are created by changing the direction of current through the write heads by the write triggers.

PHASE ENCODED (PE)
(See Figure 1)
- At write clock (WC) 15, flip all write triggers to write ones or zeros on tape.
- To write a PE one bit, the write register is reset. Set up write trigger by setting it at WC 7 if not already on from previous byte so that write trigger can be reset at WC 15 (complemented).
- To write a PE zero bit, reset the write trigger at WC 7 so that WC 15 turns it on.

NRZI
(See Figure 2)
Flip write trigger at WC 15 to write one bits only. Do not flip write trigger to indicate a zero bit.

6250 BPI
(See 55-008)

MODE SET 1(SEVEN-TRACK NRZI OPERATION)
Mode set 1 commands sent to seven-track tape controls establish tape unit operating mode for succeeding seven-track NRZI operation. Bits 0 and 1 control parity (odd or even); data converter (on or off) and translator (on or off) circuits in the 3803.

A mode set 1 command affects operation of all seven-track tape units attached to the 3803. Unless reset, the 3803 retains its mode setting until it receives another mode set 1 command.

Mode set 1 commands sent to a 3803 without the seven-track features are treated as no-op commands, except that sense data bytes are reset (no-op reset sense). Channel end and device end are set during initial selection. 200 bpi mode set 1 commands (hex codes 13, 23, 28, and 33) default to 555 bpi.

MODE SET 2 (NINE-TRACK PE/NRZI OPERATION)
Mode set 2 commands sent to PE/NRZI dual density tape controls set operating mode (1600 bpi PE or 800 bpi NRZI) for succeeding write or write tape mark (WTM) operations. Mode set 2 commands sent to a 3803 without the dual density feature are treated as no-op commands, except that sense data bytes are reset (no-op reset sense). Channel end and device end are set during initial selection.

DIAGNOSTIC MODE SET
A diagnostic mode set command causes an artificial signal loss condition that checks read and write error detection circuits.

- In PE mode, whenever write data contains successive one bits in any track, writing in that track is inhibited until the last one-bit is reached.
- In nine-track NRZI mode, no bits are written in track P.
- In seven-track NRZI mode, no bits are written in track C.

A diagnostic mode set command affects only write operations for the command in which it is issued. Channel end and device end are set during initial selection.

Note: For additional information, see 53-070.

55-007
BASIC RECORDING TECHNIQUE (Cont’d)

GROUP CODED RECORDING (6250 BPI)

Group coded recording (GCR) offers many advantages over previously used recording methods. This recording offers higher reliability even with existing tape libraries. Greatly expanded error correction capability has been engineered into GCR. Higher data rates and lower access times give higher throughput, reduced channel time, resulting in higher system performance. Data is recorded on tape, reducing rewind times, shortening the length of tape required for a data set, reducing the number of reels, reducing mounts and dismounts, and improving overall tape handling.

The data is recorded in blocks, or groups of characters. A block of data may be a single character or byte, or a number of bytes as determined by the programming system used. The significant improvements in the GCR mode are:

1. The information data is recorded at an effective density of 6250 bytes per inch (bpi) of tape.
2. The separation between blocks (IBG) is 0.3 inches (7.6 mm).
3. Simultaneous errors in any two of the nine tracks are corrected automatically.

GCR BLOCK

A GCR block consists of a preamble, data, and a postamble (see 55-009). The preamble and postamble are each 80 bytes long and serve to synchronize the read detection circuits in a manner similar to previous 1600 bpi subsystems. The data portion of the block consists of the following:

1. Data to be written by the 6250 bpi feature is continuously collected in seven character groups (9 bits in each character) and is held in the control unit 6250 bpi feature circuitry. (see 50-000 through 50-002 for second level logic details.) An error correction character is generated and then added to the seven characters to make an eight character data group. This data group is then divided into two subgroups of four characters each. The four bits in each of the 9 tracks are encoded into five bits. (see Figure 1a and 1e.) This matrix of bits, 9x10, is recorded on the tape (see Figure 3a on 55-010).

Reading of the tape reverses the process, with error correction occurring where needed. There are as many of these 10 bit storage groups as there are multiples of seven channel data bytes in the record block.

2. The remainder, or last group of the channel data bytes (zero to six bytes) is encoded with whatever pad bytes are necessary, an auxiliary check character, and the error correction code (ECC) generated from these into a 10-byte residual group. This residual data group is created for every block recorded even though no residual bytes are found in the record. The auxiliary check character verifies read and write operations.

3. End of data (EOD) is signaled by a unique subgroup of five bytes immediately preceding the residual group.

4. Following the residual group, a 8-byte cyclic redundancy check (CRC) is encoded into a ten bit group. This group, with the auxiliary check character, ensures the integrity of the read and write operation, including verifying any error corrections that may have taken place.

5. Interleaved into the recorded block, every 158 storage groups, is a resync burst. This burst allows the tape control to put into full operation any track(s) that have lost synchronization or were dead tracked due to tape defects. The action limits dead tracking for greater throughput.

Figure 1a.

Figure 1b.

Figure 1c.

Figure 1d.

Figure 1e.

Note: There are 1106 bytes of channel input data in each 1580 (6250 bpi) group recorded data block written on tape.
GROUP CODED RECORDING 6250 BPI

BASIC RECORDING TECHNIQUE (Cont'd)

GROUP CODED RECORDING 6250 BPI

Synchronizes Read in forward direction

1106 Data Bytes

Remaining data less than 1106 data bytes in multiple of 7 (BB)

Remaining data characters but less than 7

Error Detection

Control Subgroup

Synchronizes read detection in backward mode

Recorded Bits

Preamble

Data

Sync

Mark 1

Data

Sync

Mark 2

Data

End

CRC

Preamble

Control Subgroup

Resync Burst Between Data Bursts

Resets track where synchronization is lost

Preamble and First Data Group

11 Tracks

14 Subgroups

All 1's

16 Subgroups

Note: From first data bytes through residual bytes (9042 fc) equals 6250 bpi of customer data.

Legend

For all bits (tracks 1 through 9):

<table>
<thead>
<tr>
<th>Key</th>
<th>Name</th>
<th>Pattern</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Term</td>
<td>1 0 1 0 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Second 1</td>
<td>0 1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Sync</td>
<td>1 1 1 1 1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Mark 1</td>
<td>0 0 1 1 1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Mark 2</td>
<td>1 1 1 0 0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Second 2</td>
<td>1 1 1 1 0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Data</td>
<td>DDDD DDDD or GGGG GGGG</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Residual</td>
<td>XXXX XXXX or HHHH HHHH</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>CRC</td>
<td>BCCC CCCC</td>
<td></td>
</tr>
</tbody>
</table>

(See 55-010 Legend 2 for data symbols.)

Data Residual and CRC

Postamble and End Data

0.3 inch (7.6 mm)

Subgroup

14 Subgroups at 1's

16 Subgroup Postamble
6250 bpi does not relate to actual writing density on tape, but to effective data density. Actual density (9042 bpi) is greater due to the formatting and encoding. This formatting and encoding method allows error correction for any two tracks simultaneously in error. Also, tracks are not immediately dequeued or dead tracks assigned when an error occurs as they were in the past. It is conceivable that a block could have errors in all nine tracks and appear to the user to be read error free as long as only two tracks have errors at any given instant.

Figure 3a. Encoded Data Group

<table>
<thead>
<tr>
<th>Physical Tracks</th>
<th>DATA GROUP</th>
<th>STORAGE GROUP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Subgroup</td>
<td>Subgroup</td>
</tr>
<tr>
<td>A B A B A B</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>2</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>3</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>4</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>5</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>6</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>7</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>8</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>9</td>
<td>00000</td>
<td>00000</td>
</tr>
</tbody>
</table>

Group Positions

Legend 2. Data Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Data Represented</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>CRC or Pad Characters</td>
</tr>
<tr>
<td>C</td>
<td>Cyclic Redundancy Check Characters</td>
</tr>
<tr>
<td>D</td>
<td>Channel Data Characters</td>
</tr>
<tr>
<td>E</td>
<td>ECC Characters</td>
</tr>
<tr>
<td>G</td>
<td>Encoded Group Recorded Bits</td>
</tr>
<tr>
<td>L</td>
<td>Last Character</td>
</tr>
<tr>
<td>N</td>
<td>Auxiliary CRC</td>
</tr>
<tr>
<td>X</td>
<td>Residual Character</td>
</tr>
</tbody>
</table>

Note: This illustration is only one of nine such circuits. (See 50-001 for further details.)
COMMON START I/O (SIO) ROUTINE

This section introduces the microprogram controls used to read and write a record from load point. Addresses noted within the charts are key checkpoint addresses which perform a major function.

These charts provide major synchronization points within a routine, and lay out a path to check the path through the microcode. The common Start I/O routine is followed by the write operation, then the read operation from load point. The paths shown are for single, unchained operations with no exceptional conditions.

Using the compare ROS stop sync on ROS address of the CE panel (see sequence 10 on page 12-011), synchronization can be developed at various points within the operation being performed.

Remember that many routines are commonly used many times and will provide unreliable synchronization points.

Some knowledge of basic microprogram concepts is assumed. XOUTA and XOUTB registers as well as the status registers A, B, C, and D provide response back and forth between the ALUs. ALU1 basically controls the processing unit channel, while ALU2 controls the device interface. Both ALUs control various portions of the data flow.

ALU2 is a slave to ALU1, and is controlled by a transfer command and XOUTB branch index byte being passed from ALU1 to ALU2. Response from ALU2 is by way of ALU2 status registers.
COMMON START I/O (SIO) ROUTINE (Cont'd)

ALU1

100 Fetch Operation code and decode the command. Store ALU2 branch index byte in XOUTB.

- 11F Rewind X '2F'
- 116 REV/Unload X '29'
- 110 Write X '13'
- 121 ERG X '22'
- 125 DEE X '31'
- 12A WTM X '20'
- 13F SHR X '38'
- 133 RSH X '3C'
- 136 FSR X '30'
- 127 BSF X '3E'
- 143 Read Forward X '33'
- 146 Read Backward X '3A'
- 186 Sense X '06'

408 Branch to Openers.

ALU2

101 Send TU sense byte 0 to XOUTB. Send TU sense byte 1 to XOUTA.

- 103 Branch if TU is busy (Rew, run, OSEI).

- 105 Send model number to the A-register and XOUTA.

- 10E Test device and primes.

- 112/117 Test parity interrupt, and Ready to Not Ready.

11A If start is on in drive, set status D and trap to 000.

Write: 402 - Branch to 220 (See 55-024)
Read: 403 - Branch to 22C (See 55-024)
BRANCH TO WRITE FROM LOAD POINT

Write from load point is performed by controlling drive motion and controls with ALU2. ALU2 also sets the data flow control to write the single 1 or P track identification (ID) at load point.

ALU1 initiates the first data Service-In cycle, then relinquishes data transfer to the hardware. ALU1 also controls the write triggers for all control characters within the preamble, postamble, and resync burst.

Once the data portion of the write command is entered, ALU2 monitors velocity during the tach period transitions to test for velocity change during write.

The write operation is divided into the following steps:

1. Trigger ALU2 to issue a sense reset to the drive. ALU1 will monitor ALU2 Status D, which indicates that ALU2 is finished with sense reset.
2. Fetch TU sense bytes 0 and 1 and test for drive status.
3. Raise Service In for one byte of data before turning control of the channel over to the data flow section.
4. ALU1 again allows ALU2 to perform the write operation.
5. Set Erase in the drive (not Write Status yet) and erase backward, then forward. (Backward 150 tachs, forward 140 tachs.)
6. Test for Tach Start fail or Velocity Error, then write 1-track ID burst.
7. Write self-adjusting gain control (SAGC) burst with the inverse Tape Mark (no zone 1) attached to the end.
8. Set SAGC circuits in the drive to perform read back check.
9. Write record preamble consisting of the following characters: 10101, 01111, seventy 1s, 00111.
10. The hardware data flow section now takes over the writing of data while ALU2 monitors the capstan tach velocity in the drive.
11. Every 1106 channel bytes (158 storage groups on tape), ALU1 intersperses a resync burst consisting of: 00111, 11111, 11111, 11100.
12. When data is complete, the hardware writes an all ones character.
13. ALU1 checks for an all ones character indicating the end of data. This allows for writing of the residual and CRC frames.
14. ALU1 then writes the postamble consisting of the following characters: 11100, seventy 1s, 11110, 10101.
15. ALU2 waits for IBG, then tests for errors. ALU2 finishes by setting Status D and trapping to 000.

WRITE FROM LOAD POINT

ALU1

220  Test ALU2 Status C for Not Ready condition.
221  Test for LWR
225  Test Not File Protect.
22C  Test ALU1 failure.
22F  Reset data flow sense.
331  Track unit check.
379  Store clean status.

ALU2

058  Set ALU1 Status D to indicate sense reset. Trigger ALU2 to do a sense reset to the file.
060  Reset Address In.
068  Command Out dropped. Reset Status In.
06C  Service Out branch, status is accepted.

Index = X'0E'

05E  Bring in clear flag byte and branch to sense reset routine.
1AE  Send device select, command tag, and reset (X'02') to the drive.
1AB  Branch on Status D to bypass ALU1 error reset.
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT

ALU1

070
Set chain if suppress bit is set.

05F
Status accepted - return.

5A3
Drop Status in, Reset Status D. Branch to write routine.

203
Set service return. Test Op in.

711
Reset Service in.

282
Service Out checked. Reset word count to zero in sense.

50C
Entry point for normal write. Fetch TU sense byte 8 and store in XINB.

60D
Drop Service in.

611
Fetch feature byte 1 and stores in XINB.

ALU2

100
Clear error registers.

10C
Drop drive tags.

012
Set Status D and trap to 000.

ALU1

611
Trigger ALU2 to begin write op.

613
Branch if load point.

617
Test for 6150 TU.

629
Test for LWR (Loop write read) at load point (LP).

62C
Test for dual density.

630
Loop while ALU2 completes backward and forward erase. Monitor HIO or error condition.

ALU2

613
Turn on tracer and store write command in Work 4.

216
Test for LWP.

733
See if erase head positioning is needed.

737
Test for BOT.

6D4
Test positioning bit in the drive. Active indicates drive is still moving.

741
Set controls to make erase, select, move, and control tag available to the drive.

530
Set tags and TUBO. Set move and erase move.

535
Finish drive response. Test Control Status Reject.

643
Return by way of CTTLINK.
## WRITE FROM LOAD POINT (Cont'd)

<table>
<thead>
<tr>
<th>ALU1</th>
<th>ALU2</th>
</tr>
</thead>
<tbody>
<tr>
<td>146</td>
<td>Load backward tach count = 150.</td>
</tr>
<tr>
<td>281</td>
<td>Wait for real time, then start count and move tag to the drive.</td>
</tr>
<tr>
<td>28C</td>
<td>Count down check — set no-tach error if 256 counts were received without seeing tach pulse.</td>
</tr>
<tr>
<td>792</td>
<td>COUNTONE tach demean, increase count by one.</td>
</tr>
<tr>
<td>793</td>
<td>Test flag and opposite direction bit.</td>
</tr>
<tr>
<td>796</td>
<td>Count can exit. Drop command tag.</td>
</tr>
<tr>
<td>751</td>
<td>Load forward tach count = 150.</td>
</tr>
<tr>
<td>753</td>
<td>Store write command (X'081') in Work 4. (Sets forward in TU.)</td>
</tr>
<tr>
<td>768</td>
<td>Raise Command tag and place Work 4 on TUBO.</td>
</tr>
<tr>
<td>130</td>
<td>Fetch drive response. Test Command Status Reject.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ALU1</th>
<th>ALU2</th>
</tr>
</thead>
<tbody>
<tr>
<td>178</td>
<td>Drop command tag and TUBO.</td>
</tr>
<tr>
<td>785</td>
<td>Wait for real time, begin count down.</td>
</tr>
<tr>
<td>758</td>
<td>Count down complete, return to routine.</td>
</tr>
<tr>
<td>756</td>
<td>Drop move and store write command in Work 4.</td>
</tr>
<tr>
<td>138</td>
<td>Turnaround and test BOT.</td>
</tr>
<tr>
<td>136</td>
<td>Branch if 6250 feature is present.</td>
</tr>
<tr>
<td>151</td>
<td>Fetch mode set from XINA. Test if 6250 feature is present.</td>
</tr>
<tr>
<td>156</td>
<td>Set 6250 in XOUTAIM.</td>
</tr>
<tr>
<td>134</td>
<td>Fetch drive response. Test Command Status Reject.</td>
</tr>
<tr>
<td>161</td>
<td>Write and command tag to TUBO.</td>
</tr>
<tr>
<td>16C</td>
<td>Fetch drive response. Test Command Status Reject.</td>
</tr>
<tr>
<td>132</td>
<td>Test LWR and turnaround.</td>
</tr>
</tbody>
</table>

---

---
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT

ALU1

631
Status B active. Erase backward and forward complete. Prepare for ALU2 to write 1-track ID.

634
Test LBR.

638
Loop until ALU2 Status B drops indicating 1D burst complete.

ALU2

186
Set 6250 in XOUTA. Set tape Op to data flow. Set Status B.

194
Rise more tag.

196
Check velocity.

211
Interblock gap 18B1 active.

225
Wait for read time then begin testing for tach pulses.

235
Overflow without tach. Set No Tach error.

226
Tach active - increment tach count.

217
Overflow, test gap control.

230
Gap control active. Clear TUBO and reset command tag.

204
Fetch TU sense byte 1. Shift in 1600 mode.

ALU1

ALU1 looping until ALU2 completes 1D burst.

208
Set write burst status. Set ALU2 Status B hold on.

ALU2

208
Store maximum velocity count = ones minus 24.

300
Set count by model. Set initial go count = 4.

327
Test initial 4 count.

313/319
Wait for tech transitions.

336
Four count exhausted. Set ONTRDY, set count = 4.

348
Count four more tach periods, clocking between transitions.

349
Set velocity. Retry if speed is not correct.

379
Set velocity. Retry # A. Repeat if set.

406
Test NIFZ feature. Test load point lim.

606
Set write burst status. Set ALU2 Status B hold on.
WRITE FROM LOAD POINT (Cont'd)

ALU1

ALU1 looping until ALU2 completes ID burst.

604
Load counter and write ID burst for 2 in. (56.8 mm) without checking.

607
Set LP mark flag in tape to force test of burst.

703
Store count in WORK to write 2 in. (56.8 mm) burst.

TA1
Test track 1 ID.

704
Countdown of 256 tachs. Set PERMRDWT (write condition) and ALU2 Status B.

705
Loop until ALU2 is ready to write SAGC burst.

ALU2

Branch to DOTFORA. Gate format to XOUTA. Wait for rise of Clock B.

Branch to DOTFORB. Gate format to XOUTA. Wait for fall of Clock B.

601
ALU2 is ready to write SAGC burst.

641
Branch to DOTFORA.

Gate format to XOUTA.

Wait for rise of Clock B.

643
Branch to DOTFORB.

Gate format to XOUTA.

Wait for fall of Clock B.

645
Repeat 641 and 643 until count is done.

649
SAGC burst written. Set inverse Tape Mark (TIM format = SAGC1.)

655
Inverse Tape Mark complete. Send STOP to R052. Drop write condition.

658
Loop until Status B drops indicating that the IBG is detected.

700
Set CH/BIRST flag in timer.

706
Set for 256 tachs. Set PERMRDWT (write condition) and ALU2 Status B.

708
Test for beginning of record (BOR) and continue countdown.

712
BOR detected. Reset LP mark flag to indicate BOR.

713
Load for 256 more tachs. Continue countdown.

714
Load 101 more tach counts and continue countdown.

716
Test LP mark flag reset in TAB.

724
Branch on Stop command (normal exit).
WRITE FROM LOAD POINT

ALU1

ALU2

ALU1 looping until ALU2
indicates to write record.

Test device attention and
SAIGC check.

Loop until IBG is
detected.

IBG, Reset Status B and
PERMPOINT (write
condition).

Fetch TU sense byte 0.

Fetch TU sense byte 1.

Return to write record.

Store write (X 16F) in
WORK4.

Bypass if 6250 TU.

Branch if write status is
already on.

Test Turnaround.

ALU1

ALU2

156

146

Check backward.

17A

Write status and not read
forward. Skip delay.

181

Write command to TUR.  
Set command tag.

18C

Test response.

182

Test LWR.

18E

Set ALU2 Status B.  
Set tape operation to
data flow.

195

Branch to test
velocity.

21F

Test for active IBG.

230

Test for missing tech.

239

Countdown.

Set to write a frame.  
Loop here until clock B
is active.

65D

Write formatting, not at
Load Point.

663

Store A1 character:  
'Format 10 - 101011'

665

Test diagnostic flags.

6CD

DIOTFORA

Set tape operation to
data flow.

65F

Write status and not
read forward. Skip
delay.

65C

Reset Status B

Set to write a frame.
Loop here until clock B
is active.

65B

Status B

65A

Ready

659

Status B dropped.  Loop
until Status B is set and
ALU2 indicates Ready
for record.

ALU2

ALU1

Set 6250 in XOUTAIM.

ALU2

Set to write a frame.  
Loop here until clock B
is active.

Set 6250 in XOUTAIM.
WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT

ALU1

217
26F
215
308
332
344
379
608
617
618
61A

Test gap control.
Check for 6200 drive and 6250 feature.
Maximum count to 24. Set count for this model to test speed.
Set initial 4 count. Clock through 4 tachs without checking.
Test speed for 4 tach periods, but not during write data.
Velocity okay.
Set velocity. Retry in A Register if off.
Write in progress. Set for recheck.
LP off this time.
Set sync to data flow.
Set Lo Gain. No Loss for 6250.

ALU2

217

Test gap control.

ALU1

6CC
6BB
6CB
6BB
68A/6C3
6CD
6CD
673

A-Frame written. Return for more preamble.
Store A2 if fed with Mark 1 character. (Format 01 + 8 - 01111)
Write B-Frame. Return when clock drops.
Store Mark 1 if fed with Mark 2 character. (Format 11 - 11111)
Set count and write 14 subgroups of all ones (sync) characters (70 ones).
Store Mark 1 character. (Mark 1 - 00111)
Write A-Frame.
Clear format controls ready for data.

Load block recognition time-out count for no BOR or early begin.
Set write condition (Resume Bit = 1).
Wait for block.
Timing okay. Count through part of preamble.
Monitor for Mark 1 Data Ready.
BRANCH TO WRITE FROM LOAD POINT (Cont'd)

WRITE FROM LOAD POINT

ALU1
- Channel hardware data
- Flow controlling write
- data.

676
Load resync counter to
write a resync burst
every 158 storage
groups.

677
Test all ones written by
hardware. End of data.

686/687
End of data. Allow for
residual and CRC
frame (4 groups).

685
Store and write Mark 2
character (Mark 2 -
11100).

686
Write 14 groups of all
ones (Format 11 -
11111).

68C
Store and write A2/Mark
2 character (Format
01 + 4 - 11110).

ALU2
- ALU2 looping until Mark
1 character recognized
data ready.

660
Data ready (Mark 1 active).
Drop sync line.

300
Test velocity while
writing during FC-3.

66C
Exit - End of Data
recognized.

66B
Reset no loss. Test
passamite.

66A
Wait for IBS.

ALU2 looping while
waiting for IBS.

6A3
Store and write a
1-Character (Format 10 -
1001).

6A2
Set Data to data Flow.

6A9
Branch to BURSTWAIT.

388
Loop until ALU2 was
Status D.

SCD
ALU2 finished. Test for
errors, then set pending
status.

ALU2
- ALU2 looping until Mark
1 character recognized
data ready.

6A0
Store and write a
1-Character (Format 10 -
1001).

6A2
Set Data to data Flow.

6A9
Branch to BURSTWAIT.

388
Loop until ALU2 was
Status D.

SCD
ALU2 finished. Test for
errors, then set pending
status.

635
Transfer pointers to box.

636
Branch to ERDUP to
handle errors.

160
Set Status and
Status register.

15F
Set Status D. Trap ALU2
to 000.
BRANCH TO READ FROM LOAD POINT

Read from load point is basically performed by ALU2 and the hardware data flow controls.

Once ALU1 has triggered ALU2 to perform sense reset to the drive, and again to initiate the read from load point, ALU1 is basically finished. ALU1 tests to be sure that the first service cycle takes place, then goes into a loop until ALU2 finishes and sets Status D.

The read forward operation from load point steps follow:

1. ALU1 triggers ALU2 to issue a sense reset to the drive.
2. ALU1 triggers ALU2 to begin the read operation. If Status D from ALU2 is sensed before the first service cycle, an error is signalled.
3. ALU2 tests the status of the drive and checks for correct velocity.
4. Move 3 in. (76.2mm) of tape, then test for a 1-track envelope indicating a 6250 bpi tape.
5. Count through part of SAGC, then initiate read SAGC circuits in the drive.
6. Clock through 550 tachs, then check the Inverse Tape Mark.
7. When IBG is reached, fetch two bytes of drive sense and test status to this point.
8. Set read condition after gap control comes up again, and wait for the Mark 1 character preceding the data.
9. The hardware data flow now takes over until the end of data is sensed.
10. Test for errors. ALU2 sets Status D when finished, altering ALU1.
11. ALU1 compares the modulo count then branches to the status handler.

READ FROM LOAD POINT

ALU1

22C  Test for ALU failure.
22F  Reset data flow error.
231  Test unit check (Status C).
279  Stack clear status.
285  Set ALU1 Status D to indicate sense reset.
      Trigger ALU2 to do sense reset to drive.
060  Reset address in.
068  Command Out Dropped, Reset Status In.
06C  Service Out Status accepted.
070  Set chain flag if Suppress Out is up.
06F  Status accepted, branch.
543  Drop Status In., Reset Status D.
      Load returns.

ALU2

Index = X'0E'

00E  Bring in clear flag byte.
      Branch to sense reset.
149  Send device select, command tag and reset (X'02') to the drive.
1AE  Branch on Status D to bypass ALU2 error reset.
180  Clear error registers.
1CC  Drop drive tag.
122  Set Status D. Trip to 000.
012  Wait for ALU1.

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BRANCH TO READ FROM LOAD POINT (Cont'd)

READ FROM LOAD POINT

5A2
Branch to begin read.

383
Trigger ALU2 to perform forward read.

Loop until Service In/Out

386
Status D without service error.

388
Loop until ALU2 finishes and sets Status D.

ALU1

Index = X '33'

ALU2

Read Forward Routine

033
Turn on read tracer and send read forward command (X'40') to Work 41.

138
Turn round and send BOT and write command.

176
Test Rewind Unload at load point and Read Backward.

17A
Test Backward and Write Status.

186
8250 unit, skip blank.

5CA
Raise select and command tag. Wait for positioning* to drop in the drive.

*Up as long as drive is moving.

161
Move command in Work 4 to TU/D0 (X'40').

166
Set command tag.

16C
Test reverse from TU.

ALU2

ALU2 still hopping until ALU2 finishes.

188
Set Status B. Turn on tape operation to data flow.

194
Raise move tag to TU.

219
Velocity subroutine. Test acceleration.

21F
180 active, wait for read time.

230
Test for capture pulse within 256 bit cycles.

239
Test sensed. Count down and branch on overflow to test gap control from TU.

23F
Gap control on, next command tag.

25E
Test BOT, if on, and setup to move 3 in. (76.2 mm) of tape.

21C/22B
Wait for read time to begin countdown.

26B
3 in. (76.2 mm) of ID area passed. Store count and wait for read time.
BRANCH TO READ FROM LOAD POINT (Cont'd)

READ FROM LOAD POINT

<table>
<thead>
<tr>
<th>ALU1</th>
<th>ALU2</th>
<th>ALU1</th>
<th>ALU2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test 1-track envelope.</td>
<td>ALU1 still looping until ALU2 finishes.</td>
<td>Test 1-track envelope.</td>
<td>ALU1 still looping until ALU2 finishes.</td>
</tr>
<tr>
<td>Test P 1-track error not sensed. Track burst.</td>
<td></td>
<td>Test P 1-track error not sensed. Track burst.</td>
<td></td>
</tr>
<tr>
<td>Increase NRZI count if neither.</td>
<td></td>
<td>Increase NRZI count if neither.</td>
<td></td>
</tr>
<tr>
<td>If count times out, set for Not Capable.</td>
<td></td>
<td>If count times out, set for Not Capable.</td>
<td></td>
</tr>
<tr>
<td>Normal Path</td>
<td></td>
<td>Normal Path</td>
<td></td>
</tr>
<tr>
<td>285 Count through part of SAGC burst. Tape is 6950.</td>
<td></td>
<td>285 Count through part of SAGC burst. Tape is 6950.</td>
<td></td>
</tr>
<tr>
<td>28A Entering SAGC burst. Load set density controls.</td>
<td></td>
<td>28A Entering SAGC burst. Load set density controls.</td>
<td></td>
</tr>
<tr>
<td>32B Set SAGC events in TU (initiate SAGC).</td>
<td></td>
<td>32B Set SAGC events in TU (initiate SAGC).</td>
<td></td>
</tr>
<tr>
<td>293 Count SAGC tasks through SAGC burst.</td>
<td></td>
<td>293 Count SAGC tasks through SAGC burst.</td>
<td></td>
</tr>
<tr>
<td>Nearing end of SAGC. Test BOR and device attention signals.</td>
<td></td>
<td>Nearing end of SAGC. Test BOR and device attention signals.</td>
<td></td>
</tr>
<tr>
<td>Check for inverse Tape Mark (SAGC ID).</td>
<td></td>
<td>Check for inverse Tape Mark (SAGC ID).</td>
<td></td>
</tr>
<tr>
<td>Test device attention.</td>
<td></td>
<td>Test device attention.</td>
<td></td>
</tr>
<tr>
<td>Wait for IBG.</td>
<td></td>
<td>Wait for IBG.</td>
<td></td>
</tr>
<tr>
<td>Fetch 2 bytes of sense from the drive.</td>
<td></td>
<td>Fetch 2 bytes of sense from the drive.</td>
<td></td>
</tr>
<tr>
<td>Link 1 = F8</td>
<td></td>
<td>Link 1 = F8</td>
<td></td>
</tr>
<tr>
<td>Store Read Forward, Ready for record.</td>
<td></td>
<td>Store Read Forward, Ready for record.</td>
<td></td>
</tr>
<tr>
<td>Branch to turnaround.</td>
<td></td>
<td>Branch to turnaround.</td>
<td></td>
</tr>
<tr>
<td>Link 1 = 56</td>
<td></td>
<td>Link 1 = 56</td>
<td></td>
</tr>
<tr>
<td>Show in forward status, skip delay.</td>
<td></td>
<td>Show in forward status, skip delay.</td>
<td></td>
</tr>
<tr>
<td>Read to TUBO (test response).</td>
<td></td>
<td>Read to TUBO (test response).</td>
<td></td>
</tr>
<tr>
<td>Set Status B and tape operation.</td>
<td></td>
<td>Set Status B and tape operation.</td>
<td></td>
</tr>
<tr>
<td>Raise more tag.</td>
<td></td>
<td>Raise more tag.</td>
<td></td>
</tr>
<tr>
<td>Test velocity.</td>
<td></td>
<td>Test velocity.</td>
<td></td>
</tr>
</tbody>
</table>

55-044
BRANCH TO READ FROM LOAD POINT (Cont'd)

READ FROM LOAD POINT

ALU1

ALU2

ALU1 looping until ALU2 finishes.

ALU1 looping until ALU2 finishes.

217
Wait for Gap Control.

046
Set Read Condition.

048
Set sync to hardware.

087
Warning for IBG to drop.

068
IBR detected.

2A6
If not IB00, load resync and control counters.

28E
Branch if read out counter (ROCU rotation, Mark 1 is armed.

2C2
Drop sync line.

2CA
Data times out for resync burst: Wait for end of data.

ALU1

ALU2

ALU1 looping until ALU2 finishes.

ALU2

Data and resync burst being handled by data flow.

2DB
COD detected: Do postamble check.

0AF
Wait until IBG to stop read.

0CD
Test for read errors.

1BB
No error, read stop deactivate force.

635
Transfer pointers.

1D0
Branch to ENDUP and test for errors.

1EA
Set Status 0. ALU2 trapped to 000.

300
Stop to data flow.

3CA
Fetch modulo count and company.

3DB
Set pending status.
OPER—NRZI

NRZI READ DATA FLOW

Note: The 118 ns delay is a NRZI (1) Pulse Generator which uses the de-skewed trailing edge of a NRZI pulse from the tape unit.
WRITE TRANSLATOR (CARD A1E2)

TRANSLATOR

Some tape subsystems use a six-bit BCD code. Each character of the six-bit code can be translated to an equivalent eight-bit character for processing by 9-track tape subsystems. A translator in the tape control translates eight-bit code to six-bit code while writing, and translates six-bit code to eight-bit code while reading. The translator operates only if Microprocessor 1 XOUTA bits 2 and 4 are on at the rise of TAPE OP and Microprocessor 2 Stat bits 0 and 3 are on.

On 7-track write operations with the translator off, the tape control discards the two high-order bit positions (BUS OUT bits 0 and 1) of each byte from channel. Only the six low order data bits (plus a parity bit) are transferred to the tape unit.

On 7-track read operations with the translator off, the tape control inserts zeros in the two high order bit positions (BUS IN bits 0 and 1) of each byte when transferring it to channel.

EBCDIC AND BCD CODES

Notes:
[1] The graphics in these charts may not be identical to those printed by the printer or printer-keyboard. The graphics are intended as references for translating bit codes on a read or write operation.

[2] The write translator accepts the complete EBCDIC code and translates the bits to the BCD code. However, the read translator translates the BCD code only to the bits outlined.

[3] When operating in the even-parity mode, the EBCDIC blank (bl) is translated to a BCD substitute blank (bl), and the BCD substitute blank is translated to an EBCDIC blank (01000000). The odd parity blank's bit code is 000000.
OPER—LOGIC CIRCUITS

READ TRANSLATOR (CARD A1E1)

Read Translator Data Flow
ANDs and ORs translate bits 0-7 to determine EBCDIC code.
WRITE DATA CONVERTER (CARD A1E2)

The data converter is used for 7-track write and read forward operations only.

The data converter is disabled during read backward operations, but is left on for the next write or read forward operation.

The data converter is turned on and off by a mode set command. When Microprocessor 1 XOOUTA BIT 2 is on at the rise of TAPE OP (MP2, Status 0), the data converter is off. When Microprocessor 1 XOOUTA BIT 2 is off at the rise of TAPE OP (MP2, Status 0), the data converter is on.

During a write operation, three 8-bit EBCDIC bytes from channel are converted to four 6-bit BCD characters for writing on tape. If the byte count is not a multiple of three, any remaining bits of the last 6-bit character are set to zero.

DATA CONVERT WRITE TIMING
READ DATA CONVERTER

During a read operation, four 6-bit characters (plus parity) from tape are converted to three 8-bit bytes (plus parity) for transfer to channel. If the character count of the block is not a multiple of four, any remaining positions in the last byte having bits are padded with zeros, and a data convert check is indicated.

```
2A 7A
57 021

+ Set Rd DCC Reg A.
+ Set Rd DCC Reg B.

57 021

- Read Translate Bit 2, 3, 4, 6
- Data Converter ON Now
+ Data Converter ON
+ Data Converter ON

2B 7B

Reg

- Send 1 More
and Cnt 2

+ Reset A Rd DCC Bfr
+ Set Rd DCC Reg A
+ Set Rd DCC Reg B
+ Reset B Rd DCC Bfr

- Send more and Cnt 4 or 6

A

OR

DCC 0-3

- Read Data Bits 0-3

Reg

- Combined ECC Data 0-7

Reg

- Combined ECC Data 2-7

Reg

0-7

Send one more and Cnt 2

OR

1

A

OE

A

57-026
```
OPER—S/360—S/370 SWITCHING (DATA IN HANDLING)

OBJECTIVES

1. The switching circuit enables a 3803-2 to be attached to either a System/360 or a System/370.

2. Selection is accomplished by plugging cards to reflect system type on which the tape subsystem is installed. See installation, Page 90-130 or AA010, Sheet 2.

3. When plugged for S/360, a Service In/Service Out sequence is used.

4. When plugged for S/370, a Service In/Service Out/Data In/Data Out sequence is used.

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A 3803-2 tape control with a two-channel switch (TCS) [1] operates with two channel interfaces. All 3803-2 operations can be performed on either channel interface. Channels attached to the TCS interfaces can be attached to the same system or to separate systems, allowing tape units on the tape control with the TCS feature to be shared by two channels on a single system, or by two systems. In addition to all normal operations, a tape control with this feature can execute Reserve and Release commands for program control of interface switching. The large block in the center of the diagram and the unshaded blocks represent control circuits for a standard tape control. The shaded blocks represent additional logical functions installed on the tape control for the Two-Channel switch.

Channel interface lines going into or out of the tape control pass through interface switch circuits. The circuits consist of gated drivers that connect the tape control to either channel interface (A or B).

Tie-breaker logic (XM101) controls the interface switch lines so only one channel operates the subsystem, preventing one channel from interfering with the operation of the other. When neither interface is reserved or operating, the interface switch circuits are in a neutral state, and either interface can initiate an Initial Selection sequence.

Address decoders monitor the bus out lines of each interface. If the tape control address appears on the bus out lines along with an ADDRESS OUT tag, the decoders send a signal to the interface switch controls. When no interfering conditions exist, the controls connect that interface to the tape control. If the tape control is reserved or operating with the other interface, a 'short busy' sequence is sent to the interface attempting to break in.

When the tape control becomes available, a Control Unit End status byte is sent to the channel that previously received the BUSY signal.

---

[1] TCS is shown at 2CS in logic pages and in the MFI.
The Sense/Reserve command (F4) locks the two-channel switch microprogram is entered by the Reset circuits of the two-channel switch are interlocked so a Reset from one channel cannot disrupt operations on the other channel. A Reset can be accepted only from the operating channel. Resets are further conditioned to prevent a change from destroying information needed by the other channel.

INTERFACE SWITCH CONTROL
A tape control with a Two-Channel switch monitors addresses on two channel interfaces. When the tape control receives its own address, it tries to start an operation with the interface attempting selection. If the tape control is busy or reserved to interface A, interface B ADDRESS OUT is answered with a SHORT BUSY sequence, and vice versa. The interface which received SHORT BUSY will receive a CU END when the tape control is busy or reserved to interface A. If the tape control is available, it tries to start an operation with the interface associated with that latch. The SWITCHED TO CHANNEL A or B latch. The Sense/Release command deactivates the RESERVE flag.

Modifier bits, in positions 0,1,2, and 3 of a Sense command byte identify the reserve and release operations. After Initial Selection, modifier bit 2 determines whether the command is a Reserve or a Release. If bit 2 is on, (command code F4) Reserve is indicated. If bit 2 is off, (command code D4) Release is indicated.

Sense/Release Command [F4]
A Sense/Release command locks the tape control to the interface of whichever channel initiated the command. During Command Out of a Sense/Release command, the current command is masked for the F4 configuration. If an (F4) command is recognized, the microprogram checks for chaining (SETRESV). If chaining is not indicated, CURFLAG (20) is set in FLAGS (LSR 10) to reserve the tape control. If chaining is indicated, Command Reject is set.

In a valid Sense/Reserve command, bit 2 from the CHANNEL TAGS IN (ICT) register (FC161) prevents resetting the SWITCHED TO CHANNEL A or SWITCHED TO CHANNEL B latch (58-030) and the tape control remains reserved to the operating interface. Output of the SWITCHED TO A or B latch blocks interface switch circuits for the opposite interface until a reset or Sense/Release command is received from the operating interface.

Sense/Release Command [D4]
A Sense/Release command resets the RESERVE flag to allow the tape control to operate with either interface. As in the sense/reserve operation, the Sense/Release command checks for chaining. A valid Sense/Release command leaves position 2 of the CHANNEL TAGS IN register reset so the SWITCHED TO CHANNEL A and SWITCHED TO CHANNEL B latches are reset at the end of each chain of commands.

Selection
Address decoders in the tape control continuously monitor both interfaces. If the correct address bits arrive on the bus out lines along with an ADDRESS OUT tag, the SELECT OUT latch is reset. CONTROL UNIT END latch OFF ANDs with a minus output from the SELECT OUT latch to generate TRAP CHANNEL A or TRAP CHANNEL B. As the tape control is idle and is addressed by channel A. The TRAP CHANNEL A line ANDs with the SELECT SIGNAL CHAN A to set the SWITCHED TO CHANNEL A (tie breaker) latch. SWITCHED TO CHANNEL A ANDs with DELAY SELECT SIGNAL CHAN A to generate INITIAL SELECTION CHAN A.

Once interface A is addressed and selected, it arms the CONTROL UNIT BUSY and circuit in interface B. If interface B tries to use the tape control during the time interface A is locked onto the switch, the CONTROL UNIT END latch for interface B is set. When interface A is finished operating, MP1 determines that the Two-Channel switch is installed, and MP2 checks status of the CONTROL UNIT END latches. If either CUE latch is on, MP1 presents CUE status to the interface associated with that latch. The CUE will have a random tape unit address unless presented along with Device End.

Partitioning
Partitioning, achieved by operating the Enable/Disable switches, restricts the accessibility of the tape control to either channel. Partitioning bypasses SELECT OUT and deagtes all interface functions. When both interfaces are partitioned (both switches set to DISABLE), the tape control is offline and the CE panel controls can be used.

Implicit Connection
An implicit connection is one that does not depend on program intervention for release. The duration of the connection is determined by the time required for the tape control to perform a command or a chain of commands. The switch reverts to neutral on completion (at the tape control level) of the last command in a chain.

An implicit connection is extended if the channel stacks primary status. The stacked status must then be accepted by the channel to terminate the connection. If the status byte contains Unit Check, a contingent connection is made and acceptance of the status by the channel does not terminate the connection.

If the channel stacks secondary status containing Unit Exception or Unit Check, connection to that channel will be maintained until the status is accepted by the channel. If the status byte contains Unit Check, a contingent connection is made and acceptance of status by the channel does not terminate the connection.

If the channel stacks secondary status other than Unit Check or Unit Exception, the switch returns to neutral and is available to either channel. Any further attempts by the tape control to present this status to the channel will be rejected.

The tape control is offline and the CE panel controls can be used.

RESER/RELEASE OPERATION
- A Sense/Release command locks the tape control to an interface until a Sense/Release command or a Reset is received from that interface.
- A Sense/Release command resets the RESERVE flag to allow operation on either interface.
- A Sense/Release command deactivates the RESERVE flag, while chained, results in Command Reject.
- After Initial Selection, operation of Sense/Release and Sense/Release commands are identical to a Sense command.

The Sense/Release and Sense/Release commands enable the tape control to remain locked to one interface. Executing a Sense/Release command places a tape control under exclusive control of one channel until that channel issues a Sense/Release command. A Sense/Release command from channel A or B activates the RESERVE flag for A or B. A Sense/Release command deactivates the RESERVE flag.

Modifier bits, in positions 0,1,2, and 3 of a Sense command byte identify the reserve and release operations. After Initial Selection, modifier bit 2 determines whether the command is a Reserve or a Release. If bit 2 is on, (command code F4) Reserve is indicated. If bit 2 is off, (command code D4) Release is indicated.

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CONTEMP CONNECTION

A contingent connection is initiated when the last status byte contains Unit Check. The connection is maintained until a command other than Test I/O or NOP is received from the channel to which status was presented. Any command other than Test I/O or NOP to that tape unit clears the contingent connection if the tape unit is READY.

The purpose of the contingent connection is to ensure an available path to the tape unit and the transmission of sense data from the tape unit to the proper channel. If a Test I/O or NOP is issued by the addressed channel to a tape unit other than the one contingently connected, the tape control responds with SHORT BUSY and retains the connection.

BUSY

While the tape control is operating with one interface, a SELECT from the other interface will be answered with a SHORT BUSY signal (Bits P, 1, 3). Assume that the B interface is operating when the A interface attempts to address the tape control (58-030). The SWITCHED TO CHANNEL B latch blocks the setting of the SWITCHED TO CHANNEL A latch. However, --SELECT SIGNAL CHANNEL A is ANDed with --ADDR COMPARE CHAN A and NOT PROPAGATE SEL OUT CHAN A to reset the CHANNEL A SEL OUT latch. With the latch reset, the minus output of the off side of the latch is ANDed with --ENABLE CHAN A and OPERATIONAL IN to condition one input to the channel A CUE latch. A second conditioning input is OPERATIONAL IN, and the third is the minus output from the CU BUSY AND circuit. Thus, the CUE latch for channel A, is turned on to send CU BUSY STATUS CHAN A to the A interface.

The BUSY signal sent to channel A is a Unit Status byte with bits 1 and 3 on. Bit 3 indicates BUSY, while bit 1 (status modifier) indicates that the BUSY condition applies to the tape control. Bits P, 1, and 3 are forced onto the BUS IN lines at the same time the STATUS IN tag line is forced up. The STATUS IN latch is not turned on during this SHORT BUSY sequence.

CONTROL UNIT END

The CONTROL UNIT END latch (58-030) remains on, remembering that channel B tried to break into channel A operations. This latch also sends +CUE PENDING CHANNEL B to the microprogram branch-on-condition logic (AB1611) to notify the B interface that a Channel End is pending. When the tape control is no longer operating with, or reserved by, interface A, the SW TO CHAN A latch turns off. --TRAP CHAN B is active, and the SELECT CHAN B line is still active to turn on the SW TO CHAN B latch.

The SW TO CHAN B latch gates the output from OPERATIONAL IN to channel B to send a Unit Status byte to channel B. The status byte will contain a CUE (bit 2) indicating the tape control is now available for other operations. A standard REQUEST-IN sequence is used to transmit the CUE status byte.

At the end of an operation, the SW TO CHAN A (or B) latch is reset unless a chain, STACK INTERRUPT, or UNIT CHECK condition exists. OPERATIONAL IN is reset in the Burst Ending Sequence when CHANNEL TAGS IN register bit 7 is reset.

With OP IN reset, no REQUEST IN, no ADDRESS OUT, and no SELECT OUT for the tape control, the SELECT OUT latch is active. (Note that the SELECT OUT latch is turned on when the tape control is inactive.) With the SELECT OUT latch active, the plus output deactivates --RESPONDING TO CHAN A (or B). --RESPONDING TO CHAN A (or B) inactive resets the SW TO CHAN A (or B) latch, and the tape control is available for another selection sequence.

STACK

In some cases the channel may refuse the end status byte, this turns on a 'stack' condition. If the status byte contains Unit Check or Unit Exception, the tape control remains connected to that interface until the channel accepts the status. If the status byte contains Unit Check, the connection is maintained until a command other than NOP or Test I/O is received from the channel to which the status was presented. This procedure makes certain the channel has an opportunity to interrogate a unit check condition before the other channel disturbs the tape control. When the interface connection is maintained because of a unit check, the connection is defined as "contingent" (not part of the normal routine).

Stacking of status other than Unit Check or Unit Exception does not maintain the interface connection. The TCS will be reset to neutral, and the tape control will become available to either channel.

STACK INTERRUPT

A Halt I/O command received by the tape control before the channel accepts the ending status causes the MP1 microprogram to reset OP IN and check for two-channel operation and contingent connection. If a contingent connection is needed to prevent loss of error information, the microprogram branches to a "Hold Interface" routine.

With no contingent connection, an interrupt cycle is initiated to present the stacked status. CONTROL UNIT BUSY will be reset if applied, and HOLD INTERFACE will be set if the STACK or STATUS PENDING flag is on.

DEVICE END

The purpose of Device End circuits is to signal the data channel when a tape unit has completed a task and is ready to accept a new one. On a tape control with the two-channel switch feature, separate LSRS in MP2 are used to store the Device End status for each channel. The second Device End LSR ensures that the Device End is returned to the channel that initiated the operation.

A Device End received while the two-channel switch is in a neutral state causes the tape control to enter an interrupt status. The tape control then presents the Device End to the channel that initiated the Device End operation, if that interface has not been partitioned. Partitioning resets pending Device Ends for that interface.

An interrupt due to a Control Unit End sends Device End, including the address of that device, and Control Unit End, to the channel.
OPER—TIE BREAKER (TCS)

TCS SELECTION AND TIE-BREAKER LOGIC
(PART 1)

Note: See 58-012 for description of circuit operation.
OPER—DEVICE SWITCHING CONFIGURATIONS

DESCRIPTION

Device switching allows access to a maximum of sixteen tape units by two, three, or four tape controls, and permits simultaneous operation of as many tape units as there are tape controls.

3803 Models 1 and 2 can be mixed in a switching configuration; however, attempting to access a 3420 Model 4, 6, or 8 through a 3803 Model 1 produces unpredictable results.

Device switching is performed via the Communicator and Device Switch features. Three Device Switch features (58-051) available with the tape subsystem are:

- 2 Control Switch used with 2x8 and 2x16 configurations
- 3 Control Switch used with 3x8 and 3x16 configurations
- 4 Control Switch used with 4x8 and 4x16 configurations

The minimum switching subsystem configuration allows two tape controls to access up to 8 tape units and is called a 2x8 configuration. The maximum configuration is 4 tape controls and 16 tape units (4x16). A non-switching configuration (1x8) is referred to as Selection Logic.

Device Switching logic is installed only in those tape controls that have attached tape units. The location of the Device Switches depends on the configuration desired. For example: In a 2x8, 3x8, or 4x8 configuration, the switching feature is required only on the first tape control while in the 2x16, 3x16, and 4x16 configurations, the switching feature is required on Tape Controls 1 and 2 (58-051). The 2x16 configuration consists of two tape controls, each with a Communicator 1, a 2 Control Switch, and eight tape units. The tape controls may be connected to either different channels of the same system or on different systems.

Device switching logic is logically invisible (except for BUSY responses during Initial Selection and Device End Interrupts, which result when tape units become available). Device switching logic is modular to allow flexibility for a variety of system configurations. Subsystem priority and device addressing are assigned by pluggable jumpers within the switch. Any tape unit may be partitioned (made unavailable) to any tape control via toggle switches on the tape control operator's panel (58-060).

2 Control Switch

The 2 Control Switch is a 2x8 configuration of hardware switching logic (58-051, 58-055). Tape Units 0 - 7 (attached to Tape Control 1) can be accessed by the Communicator in Tape Control 2 as well as the Communicator of Tape Control 1. A 2x16 configuration is obtained by installing a 2 Control Switch in both Tape Controls 1 and 2, allowing the Communicator in each tape control to access its own eight 3420s, as well as 3420s of the other tape control.

3 Control Switch

A 3x8 configuration is obtained by installing a 3 Control Switch in Tape Control 1 only and a Communicator 1 in Tape Controls 2, 3, and 4 (58-051). Tape units attach to Tape Control 1.

A 3x16 configuration is obtained by installing a 3 Control Switch in both Tape Controls 1 and 2. A third tape control must be added to the configuration. Tape Control 3 does not contain any switching hardware or attach any tape units, but each contains a Communicator.

The 3 Control Switch and the 4 Control Switch are expansions of the 2 Control Switch. They allow access to eight attached tape units by the additional Communicators.

4 Control Switch

A 4x8 configuration is obtained by installing a 4 Control Switch in Tape Control 1 and a Communicator 1 in Tape Controls 2, 3, and 4 (58-051). Tape units attach to Tape Control 1.

A 4x16 configuration is obtained by installing a 4 Control Switch in both Tape Controls 1 and 2. Two more tape controls must be added to the configuration. Tape Controls 3 and 4 do not contain any switching hardware or attach any tape units, but each contains a Communicator.
OPER—DEDEVICE SWITCHING CONFIGURATIONS (Cont'd)

**Notes:**

1. Maximum of 16 tape units and 4 tape controls.
2. Tape units attach only to tape controls with switching features.
3. Any or all control units may have two channel switch features.
4. For 3420 Model 8 power requirements, see 90-180.
OPER—2x8 SWITCH LOGIC

OPERATOR PANEL SWITCHES (16)

Switch Section A on Tape Control 1 directs Tape Control 1's access path to Tape Units 0-7. Switch Section B on Tape Control 1 directs Tape Control 2's access to Tape Units 0-7.

Addresses Jumpered 0-7

Secondary Interface

Switch Section A

Crosspoint Switches

Tape Unit 0

Communicator 1 Feature

Addresses Jumpered 0-7

Secondary Interface

Primary Interface

The Secondary Interface is not used on the 2 x 8, 3 x 8, or 4 x 8 configurations.

Secondary Primary Interface

58-055
Tape Control 1

- Communicator 1 Feature Addresses Jumpered 0-7
- Secondary Interface
- Primary Interface
- Interboard Flat Cables
- Switch Section A
- Switch Section B
- TU Online/Offline Switches (Enable/Disable)
- Crosspoint Switches

Tape Control 2

- Communicator 1 Feature Addresses Jumpered 8-15
- Secondary Interface
- Primary Interface
- Interboard Flat Cables
- Switch Section A
- Switch Section B
- TU Online/Offline Switches (Enable/Disable)
- Crosspoint Switches

Switch section A on tape control 1 directs tape control 1's access path to tape units 0-7. Switch section B on tape control 1 directs tape control 2's access to tape units 6-7. Switch section A on tape control 2 directs tape control 2's access to tape units 8-15. Switch section B on tape control 2 controls the access of tape control 1 to tape units 8-15.

OPERATION

The Device Switch is controlled by lines from the tape control. Although there are necessary switching delays, data transfers, control requests, and responses, tape unit status is sent to the tape control as if the switch were not present.

Selection: When DEVICE SELECT (58-090) is activated, with the device address on the DEVICE SWITCH bus and the node is enabled, the switch tries to set the COMMITTED latch for the node. Note: A "node" is the logic circuitry required to select and assign one tape unit to a requesting tape control. If the device has already been selected by another tape control, a BUSY indication is returned to the tape control attempting selection. If the device is not busy, the COMMITTED latch is set. The latch output is then sent to the other tape control nodes for that device to prevent selection by them. At the same time the committed latch will become active and GATE BUS OUT will be the response to the selecting tape control. The BUS OUT and BUS IN connection has now been established between the tape control and tape unit. SWITCH SELECT is not required to select a tape unit, although it is always active in 3803 subsystems.

Committed: Once the COMMITTED latch is set for a given node, it remains set until reset by the selecting tape control. Reset is accomplished by addressing and sending a 50 ns pulse on the SET/RESET line.

Priority: When two or more tape controls attempt to select a tape unit at the same time, priority of access is determined by jumpers plugged on Tape Controls 1 and 2 (58-100). See Section 90 for plugging details.

LINE DEFINITIONS (58-100)

Busy/Tach: The BUSY/TACH line indicates the state of the device (busy or not busy) to the tape control.

Device Operating Interface A and B (2 lines): A device operating line is active when a committed tape unit (one for which a COMMITTED latch has been set) has its BUSY/TACH line active. The DEVICE OP INTF A line to the tape control is used for generating the METERING IN line for its channel interface. The DEVICE OP INTF B line serves the same function but is used by the second channel interface when the Two-Channel Switch feature is installed.

Run Meter: When the node is enabled, the RUN METER line is sent to the device for meter operation.

Set/Reset: The SET/RESET line is tied active so the ENABLE/DISABLE latch can be set to the corresponding state of the Enable/Disable switch on the operator's panel.
OPER—4x16 SWITCH LOGIC

Notes:
[1] The maximum switch configuration consists of 16 tape units and 4 tape controls.
[2] Tape units attach only to the tape controls with device switching features.
[3] Any or all tape controls may have a Two-Channel Switch feature.
Functional Units of the Device Switch are:

1. **Logic Section**: The logic section communicates with the tape control to provide status, device address, and accessing interlocks. The information exchanged establishes tape unit attachment to the tape control and presents switch status to the operating tape control or controls in the subsystem configuration.

2. **Crosspoint Section**: The crosspoint section is a switch matrix capable of switching twelve inbound and twelve outbound lines. Each node (tape control/tape unit path) is controlled by the logic section.

3. **Communicator**: The communicator replaces the selection logic circuits and associated device interface cabling in the basic tape control with different logic circuits and cabling to the device switches. The communicator divides the device interface into primary and secondary and controls the gating of each according to the address of the device being selected. The communicator consists of interface drivers and receivers.

   The Communicator 1 feature has only one external (primary) interface. The Communicator 2 feature has two external interfaces (primary and secondary). The secondary interface connects attached tape units through Switch Section A (58-055, 58-060). The primary interface connects a 3003 that does not have tape units attached to another tape control through Switch Section B.

4. **Tape Unit Online/Offline Switches**: Tape unit toggle switches (58-060, 58-100) are located on the operator's panel of each tape control having a device switch feature. These switches enable the operator to determine tape unit availability to each tape control in the configuration. In a 4x16 configuration, four tape controls can access 16 tape units so there are 64 toggle switches, 32 each on Tape Controls 1 and 2. There are no switches in Tape Controls 3 and 4.

**Note**: Refer to charts located in ALD XC-700 pages.

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**Schematic Diagram**: Device Switching Functional Units (All reside in TCU-1)

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**Charts and Diagrams**: Crosspoint Section: The crosspoint section is a switch matrix capable of switching twelve inbound and twelve outbound lines. The Communicator replaces the selection logic circuits and associated device interface cabling in the basic tape control with different logic circuits and cabling to the device switches. The communicator divides the device interface into primary and secondary and controls the gating of each according to the address of the device being selected. The communicator consists of interface drivers and receivers.
Gating a control unit to device path node on or off effects switching at the device interface level.

Each node consists of parts of three logic cards. The crosspoint cards (B) contain the electronic switches needed to switch the bus in or out lines for a node. The switch logic card (A) contains the circuitry to control the crosspoint switch and communications to the tape controls.

1. The crosspoint (XPT) switches are gated by the set to the COMMITTED latch.
2. COMMITTED lines prevent simultaneous selection of the same device by more than one tape control.
3. INTERFACE COMMITTED, COMMITTED, and DEVICE BUSY are ANDed to generate DEVICE OPERATIONAL, which is sent to the tape control to develop METER IN for the channel interface.
4. DEVICE END INTERRUPT lines are scanned by the tape control to determine which tape unit has a DEVICE END INTERRUPT pending.
5. BUSY/TACH is available to the tape control when the node is selected and enabled and the DEVICE BUSY or SWITCH BUSY line is inactive.

Switch Logic Card
See Fig 58-100 for detail.
Note: See ALD pages XCnnn.
CE PANEL DESCRIPTION

3803 CE PANEL DESCRIPTION

CE PANEL SWITCHES

PANEL ENABLE (TWO-POSITION TOGGLE)

Panel Enable

On/Off

Active only if ROS is in normal mode. It may be necessary to raise the Set ROS Mode momentary switch to establish this mode. The Panel Enabled light is ON when the switch is ON.

Note: If the Panel Enabled light does not light, set the ROS Mode rotary switch to Norm and operate the Set ROS Mode switch (momentary).

On

Allows the CE panel functions identified by yellow lettering to be performed with the Interface Disabled light either on or off. Allows all CE panel functions to be performed with the Interface Disabled light ON.

OFF

Degates the following functions:
1. Stop On—Control Check
2. Stop On—Data Flow Check
3. Reset/Start or Step
4. ROS Mode
5. Command Control switches (3)

STOP ON-CONTROL CHECK (TWO-POSITION TOGGLE)

Stop On

Active only while ROS is in Stop mode.

On

Stops both ALUs when any control check is recognized in the ALU selected by the ALU1/ALU2 switch. The exact stopping location depends on the type of error; it is usually two less than the stop address except for a BOC. Generally, microprogram-detected errors will not be recognized until a transfer hardware error (XFR HDWERR) microinstruction is executed. Most other errors will stop the ALUs when the failure occurs. Disables the compare register equal features of the ROS Mode switch Stop position.

OFF

Allows normal tape control operation.

STOP ON-DATA FLOW CHECK (TWO-POSITION TOGGLE)

Stop On

Active only while Interface Disabled light is ON (CE Mode).

On

Stops both ALUs at the completion of a command in which a failure occurs on Unit Check condition.

OFF

Normal tape control operation.

Note: When in CE Mode, the tape control stops on Unit Exception, regardless of switch position. To inhibit a Stop-On-Unit-Exception when tape control is in CE Mode, jumper AA1T2J12 to ground.
LAMP TEST (TWO-POSITION TOGGLE)
Lamp Test
Allows you to test the CE panel indicator lights.

ROS MODE (SEVEN-POSITION ROTARY)
Active only while the Panel Enabled light is on. After selecting any of the seven positions of the ROS Mode switch, activate the Set ROS Mode momentary toggle switch to set the mode.

Rst/Cmpr
When the IC address of the selected ALU equals the data in the compare register, both ALUs reset to location 000 and allowed to continue running. (The Display Select switch must be in IC position.)

Rst/Err
When a control check occurs, both ALUs are reset to location 000 and allowed to continue running.

Set IC
Allows the contents of the compare register to set IC of the ALU selected by the ALU1/ALU2 switch.

Norm
Normal running condition of both ALUs.

Stop
When the data in the compare register equals the IC address of the ALU selected by the ALU1/ALU2 switch, and the Display Select switch is in IC position, both ALUs are stopped. The instructions at the stopped addresses will not have been executed.

When the Stop On-Control switch is active, both ALUs are stopped only when an error occurs in the ALU selected by the ALU1/ALU2 switch.

Note: If compare equal stop function does not work, make sure the Control Check Stop switch is off.

Step
Operating the Start or Step momentary switch allows stepping the ALU selected by the ALU1/ALU2 switch, while the ALU not selected runs normally.

Cycle
Allows the repetitive execution of an instruction at a selected address. Step or stop at the instruction address on which you want to cycle. Set ROS Mode to Cycle and press Start or Stop.

ALU1/ALU2 (TWO-POSITION TOGGLE)
ALU 1
ALU 2
Selects the ALU to be controlled by the ROS Mode switch.

Selects the ALU when the Display Select switch is set to the IC, Bus In, Bus Out, Hi ROS, or Low ROS position.

SET ROS MODE/SET CE COMPR
(TWO-POSITION MOMENTARY TOGGLE)

Set ROS Mode
Sets the selected ROS mode.

Set CE/Compr
Sets the data, selected by the three hex rotary switches into the register selected by the Data Entry Select switch. The Set CE/Compr switch operates without the panel enabled or the interface disabled.

COMMAND CONTROLS

DISPLAY SELECT (SEVEN-POSITION ROTARY)

1. Displays command/device in conjunction with Data Entry Select.
2. Displays Write Data/Go Down or Byte Cl/Multiplier in conjunction with Data Entry Select.

Note: Some stop-on-error conditions stop the CE clock, which prevents displaying the contents of the CE registers.

CmprReg
Displays data currently in the compare register in indicators 0 through 11.

IC
Displays the IC address of the selected ALU in indicators 0 through 11.

Bus In
With ALU1 selected, displays Channel Bus In data in indicators 0 through 7 and in Tags in indicators 8 through 11.

With ALU2 selected, displays TU Bus In data in indicators 0 through 7 and the device address in indicators 8 through 11.
REF—CE PANEL (Cont’d)

Bus Out
With ALU1 selected, displays Channel Bus Out data in 0 through 7, and outbound control or tags in 8 through 11. Parity is only assured when the microprogram activates CHANNEL BUS OUT.

With ALU2 selected, displays TU Bus Out data in 0 through 7 and outbound controls or tags in 8 through 11.

HI ROS
With ALU1 selected, displays ROS1 data bits 0-7 P1 in 0 through 7 and control lines in 9 through 11.

With ALU2 selected, displays ROS2 data bits 0-7 P1 in 0 through 7 only.

Low ROS
With ALU1 selected, displays ROS1 data bits 8-15 P2 in 0 through 7 and control lines in 9 through 11.

With ALU2 selected, displays ROS2 data bits 8-15 P2 in 0 through 7 only.

DATA ENTRY SELECT (SEVEN-POSITION ROTARY)

Data Entry Select

<table>
<thead>
<tr>
<th>Command</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
</tr>
<tr>
<td>001</td>
<td>1</td>
</tr>
<tr>
<td>010</td>
<td>2</td>
</tr>
<tr>
<td>011</td>
<td>3</td>
</tr>
<tr>
<td>100</td>
<td>4</td>
</tr>
<tr>
<td>101</td>
<td>5</td>
</tr>
<tr>
<td>110</td>
<td>6</td>
</tr>
<tr>
<td>111</td>
<td>7</td>
</tr>
<tr>
<td>000</td>
<td>8</td>
</tr>
<tr>
<td>001</td>
<td>9</td>
</tr>
</tbody>
</table>

With ALU1 selected, displays ROS1 data bits 8-15 P2 in 0 through 7 and control lines in 9 through 11.

With ALU2 selected, displays ROS2 data bits 8-15 P2 in 0 through 7 only.

Cmdr Reg
Allows data in the three Data Entry switches to be entered in the compare register.

Cmd 1, 2, 3, and 4
With the Data Entry Select switch in one of the four positions (Cmd 1, 2, 3, or 4), a command and its associated device address (0-F) may be entered into one of the four command positions.

Byte Cnt
The three Data Entry switch positions determine the total byte count. The left and center switches count to a maximum of 255. The right, or Multiplier switch counts in multiples of 1024. Position zero of the Multiplier switch adds zero to the total of the other two switches. Position 1 would add 1024, 2 would add 2048, etc. To provide a byte count of 3140, set the left and center switches each to 4, and set the right switch to 3.

Note: Check to ensure you get the correct byte count.

Byte Count
Dialized
Written
00 to FE
Byte Count diali ed +3
FF
2

Write Data Go Down
Write Data and Go Down determine those bits to be written and establishes the go-down time. The left and center data entry switches determine the bits to be written. For example, the Ripple/Wr Data switch in Wr Data, 0 in the left switch, and 3 in the center switch.

writ ing the fol lowing:
0 1 2 3 4 5 6 7
1 0 0 0 0 1 1

Note: The P bit is automatically generated when required.

The right switch determines the go-down time. Position zero gives a go-down of 6.0 milliseconds. The total range is from 6.0 milliseconds to approximately 0.5 second. Each position, 0 to F, represents approximately 26 milliseconds. A setting of 3 results in a go-down time of 6 milliseconds + (3 x 26), or approximately 84 milliseconds.

• To write continuously, jumper from AA1R2J12 to ground.
• To do an LWR with go-down time, jumper from AA1S2G08 to ground.

Data Entry
The three rotary switches are used to enter data into various registers. Set a command into the left switch and the TU address into the right switch. For example, 01A entered into the Command register indicates a write command to device A.

CONTROL CHECK INDICATORS

Hi IC Parity/HI ROS Reg Pty
Checks the 16 branch conditions not checked by the HI IC PARITY/HI ROS register circuits. (A total of 32 BOCs are checked.) If an even number of BOC groups are active, a BOC error is indicated.

B- Bus Parity
Checks the output of an LSR for odd parity on the B Bus on instructions which transfer data from ALU to an external register. If parity is even, the error is gated to the hardware error latches and CE panel indicator.

Note: When displaying the LSRs, B-Bus parity errors can occur because LSRs are not set to odd parity with power-on reset.

Hi IC Pty/HI ROS Reg Pty
The circuits that set this indicator are:
1. Hi IC parity check.
2. Hi ROS register parity check.
3. Instruction Decode error. (ROS instruction check to be sure only one ROS operation was decoded.)
4. BOC Error. (Check of 16 branch conditions.)

Lo IC Pty/Low ROS Reg Pty
Checks parity of the IC (low order) and ROS register (low order). An even parity error sets the HARDWARE ERROR latch and CE panel indicator. Lo IC Parity is checked only on a BU or a successful BOC. Low ROS Parity is checked on every instruction cycle.

CE PANEL INDICATORS
INTF'S DISABLED
Indicates when the tape control is offline. The manual Enable/Disable switch(es) on the CU operator’s panel must be in Disabled position before the lamp comes on.

CMPR EQUAL

Indicates that the data entered in the CE/Compare register equals that contained in any register selected for comparison.
Checks the parity of information to be stored in an LSR at 100 ns time. Bits 0-8 from the D Bus are exclusive-ORed with the P bit from Bus Out. Even parity sets the D BUS PARITY ERROR latch and HARDWARE ERROR latch, and lights the CE panel indicator. This error condition is only checked on a transfer of data into the ALU from an external source.

U Pgm
Monitors the selected ALU and signals an error when the ALU detects any hardware error, including checksum errors for both ALUs.

Data Flow Check Indicators

P Comp
The P Comp indicator (also C Compares) is set by the following conditions:
1. When parity of the byte sent to the channel buffer on read operations is wrong.
2. Buffer Overrun.
3. Write Address error.
4. If CHANNEL BUFFER READ IN counter gets out of step.
5. Write buffers are empty when a write tape cycle occurs.

Skew
Set when vertical misalignment of bits exceeds acceptable limits. (If all bits in a byte are not received by the read circuits within a specified period, the bit has excessive “skew” and Skew Error is set.)

Skew Error is set:
1. During a 6250 bpi/PE read operation if RIC leads ROC by 30 bits.
2. During a 6250 bpi write operation if RIC leads ROC by 14 bits.
3. During a PE write operation if RIC leads ROC by 4 bits.
4. During a NRZI write operation by skew gate.

Read VRC
1. 6250 bpi Mode
   a. Set during single-track error correction if a match is not found.
   b. Set during a write operation if hardware pointer and correction code indicate different tracks.
2. Set during a PE operation if a parity error occurs and no track pointers are on.

CRC
Set during 6250 bpi and 9-track NRZI operations when the CRC byte calculated for a read operation does not match the CRC byte written on tape.

Wr Tgr
Set when the output of the write triggers has incorrect parity.

NOTES ON CE PANEL OPERATION

- A Start I/O command to a tape unit that has Unit Check or Busy in its initial status byte will prevent stepping to the next command. This condition can be caused by a Not Ready tape unit.
- CE command sequence hang up: when an error occurs on a 3803 with the Two-Channel Switch (TCS) feature installed, a “contingent connection” is established without Stop On Error ON. This is caused by dedicated sense data from the failing tape unit. There are three ways to proceed:
  1. Issue a Sense command to the same tape unit after any other type of command.
  2. Issue all four internal program commands, except a Test I/O or NOP, to the same tape unit. A Mode Set command can also cause a hang condition, so it may be necessary to replace this command following initial setup.
  3. In order to allow command cycling to multiple tape units without changing the command setup, set ROS Mode to Rst/Cmp using IC address 302 on ALU1. This restarts both microcodes at 000 on contingent-connection conditions and performs a general reset. To eliminate the need for pressing the CE Command Start pushbutton, connect a jumper from AB202510 (General Reset FC041) to AA1T20G5 (Start Key Latch PK035).
The tools and test equipment listed in this section are required to properly service 3420 Magnetic Tape Units and 3803 Tape Controls.

### TOOLS AND TEST EQUIPMENT

#### KEPT AT THE BRANCH OFFICE

<table>
<thead>
<tr>
<th>Part</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>198821</td>
<td>Stress Tape (order from Mechanicsburg)</td>
</tr>
<tr>
<td>432152</td>
<td>Master Signal-Level Tape (order through IBM Sales) (See Note 1)</td>
</tr>
<tr>
<td>451064</td>
<td>Degausser (See Note 1)</td>
</tr>
<tr>
<td>453522</td>
<td>Developing Solution</td>
</tr>
<tr>
<td>586145</td>
<td>*Digitec 251 Meter (Digitec 201 Meter, P/N 453046, may be used if available)</td>
</tr>
<tr>
<td>251274</td>
<td>Adapter Hose</td>
</tr>
<tr>
<td>251372</td>
<td>Tape Cleaning Kit</td>
</tr>
<tr>
<td>184862</td>
<td>Stress Tape</td>
</tr>
<tr>
<td>453500</td>
<td>Manometer, inch (two needed for series connection) (See Notes 1 and 2)</td>
</tr>
<tr>
<td>453504</td>
<td>Tape Transport Cleaner</td>
</tr>
<tr>
<td>453511</td>
<td>Oscilloscope (Model 453, 454, 561, 545, 766H or equivalent)</td>
</tr>
<tr>
<td>453516</td>
<td>Tape Developping Solution</td>
</tr>
<tr>
<td>251315</td>
<td>Pressure Divider</td>
</tr>
<tr>
<td>251316</td>
<td>Tape Transport Cleaner</td>
</tr>
<tr>
<td>251539</td>
<td>Capstan Box Wrench (read adjustment capstan)</td>
</tr>
<tr>
<td>251206</td>
<td>Crimping Tool</td>
</tr>
<tr>
<td>453522</td>
<td>Tape Transport Cleaner</td>
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</tr>
<tr>
<td>251206</td>
<td>Crimping Tool</td>
</tr>
</tbody>
</table>

#### MASTER TAPES

Master skew tapes and master signal-level tapes are manufactured to rigid specifications. They are the standards that are used by CEs to obtain optimum tape unit performance. Because tape unit performance is directly affected by the accuracy of these master tapes, the following precautions should be taken:

1. Use master tapes only for their intended purpose.
2. Handle tapes with care.
3. Make only full-reel passes in order to have even wear throughout the length of the tape.
4. Identify master tapes as such and mark the reels with the letter "m," as a reminder to make full passes only.

### MASTER SIGNAL-LEVEL TAPES

Master signal-level tapes have the ability to produce a signal to within ±2% of the primary master. A primary master, which is established as an IBM standard, is the base for instrument alignment.

All new master signal-level tapes are checked at 3200 FCI and 800 FCI. The suffix letter “A” is added to the part number to allow field identification of 3200/800 FCI tapes as opposed to the former 800/556 FCI tapes. Thus, for example, a master signal-level tape checked out at both 3200 FCI and 800 FCI would have P/N 432152A2.

### DEGAUSSER

Caution: The degausser will demagnetize any material such as tape, disks, etc. Power off the tape unit.

To degauss the read/write head:

1. Remove magnetic tape from the tape unit. Do not place the tape on top of the tape unit.
2. Plug degausser into 110 Vac receptacle.
3. Press the pushbutton on the degausser while it is at least 1 foot (30.5 cm) away from the read/write head and move it slowly toward the head.
4. Hold the degausser against the front surface of the head for about 10 seconds.
5. Pull the degausser straight away from the head very slowly to a distance of at least 1 foot (30.5 cm) and release the pushbutton.

---

TOOLS AND TEST EQUIPMENT (Cont'd)

WATER MANOMETER

Note: The use of a 30 inch (76.20 cm) manometer or the 80 inch (203.20 cm) pressure/vacuum gauge is not dependent on the English (metric) system of measurement.

Use the requested tool by part number and name, and measure to the specified units (whether metric or English) to obtain the desired adjustment or reading.

Shown are several setups for using the water manometer, part number 453500. Part A shows a single manometer measuring a pressure of greater than 30 inches (76.20 cm). Part B shows two manometers in series measuring a pressure between 30 and 60 inches (76.20 cm and 152.90 cm). Part C shows using the pressure divider and a single manometer measuring a pressure greater than 30 inches (76.20 cm).

General instructions for using the manometer are:
1. Remove the tee from the tee and hose assembly, and connect the hose on the line to be checked.
2. Set up the water manometer by opening both top valves one full turn from closed position. (Incorrect readings will occur if valves are opened too far.)

Connect the pressure-sensing hose to one port, leaving the other port open.
3. Fill the water manometer with tap water, maintaining the water level near the 0 position on the scale. Zero the manometer by sliding the scale up or down until the 0 mark lines up within 0.2 inch (5.7 mm) of the bottom of the meniscus in both columns.
4. Set conditions for the specific item to be checked according to the pneumatic-adjustment decal located on the transfer valve and manifold.
5. Read the vacuum level. (The vacuum level is the sum of the displacement of the water level in each column.)

PROCEDURES

Note: Take readings at bottom of meniscus.

1. Using a single manometer to measure a pressure of less than 30 inches (76.20 cm). Read at bottom of each meniscus and add the two readings together to get total pressure (W). W = 2.0 + 1.7 = 3.7.

2. Using two manometers in series to measure a pressure between 30 and 60 inches (76.30 and 152.40 cm). Read at bottom of each meniscus and add the four readings together to get total pressure (the sum of X + Y). X + Y = 2.0 + 1.7 + 2.0 + 1.7 = 7.4 inches.

3. Using a pressure divider with a single manometer to measure a pressure of greater than 30 inches (76.30). First, measure a known pressure of less than 30 inches. Second, insert the divider and adjust the divider's adjusting screw until the manometer reading is 40% of its original reading. Third, measure the pressure of greater than 30 inches by reading at the bottom of each meniscus, adding the two readings together (to get Z), and multiplying Z by 2.5 to get pressure. 2.5Z = 2.5(2.0 + 1.7) = 25(3.7) = 9.25 inches. The maximum reading possible with this combination is 75 inches (190.50 cm).

4. Using a pressure/vacuum gauge to measure a pressure greater than 80 inches (203.20 cm).
   a. Measure a known pressure less than 80 inches (203.20 cm).
   b. Insert the pressure divider between the measurement part and the gauge and adjust the divider’s adjusting screw until the gauge reads 40% of its original reading.
   c. Measure the pressure greater than 80 inches (203.20 cm) and record the reading (Z).
   d. Multiply Z by 2.5 to get the total pressure.

Example: If Z reading is 33.2, 33.2 x 2.5 = 83.0 inches

PRESSURE/VACUUM GAUGE

Shown below is pressure/vacuum gauge, part 54953B. To use the gauge:
1. Attach the gauge hose to the fitting to be tested.
2. Read the dial directly in pressure or vacuum. (For measurements above 80 inches (203.20 cm), add 1 inch (2.54 cm) to the reading for each 1/16 inch (1.59 mm) of pointer travel beyond the end of the scale.)
3. Caution: Disconnect from test point before loading or unloading tape unit to prevent damage or mis calibration of gauge.
**TOOLS AND TEST EQUIPMENT (Cont'd)**

### 3420 FIELD TESTER

**Caution:** Use extreme care when attaching the field tester because an error can damage the tape unit, the tester, or both. Be sure to use only the 3420 field tester, part 1765342, when doing offline maintenance on 3420 tape units. Do not use the 2420 Field Tester. When testing Models 4, 6, and 8, a field tester at EC level 734316 must be used. A temporary jumper must be installed from K2P02 to M2D06 for 6250 operation.

When operated with the field tester, the tape unit loads and unloads tape, reads, writes, and moves tape forward or backward. To test several tape units simultaneously, use the manual controls on the tape control CE panel.

To use the field tester:

1. Unload the tape unit.
2. Switch the unit off line at the logic gate. To ensure that the on-off line switch circuitry is operating correctly, monitor the + interface disable and + interface on-off lines. Refer to page FT910 of the 3420 ALDS. Check the following levels for proper operation of the on-off line switch circuits.

<table>
<thead>
<tr>
<th>Position of On-Off SW</th>
<th>A1L6D04</th>
<th>A1L6B03</th>
</tr>
</thead>
<tbody>
<tr>
<td>Online</td>
<td>+6v</td>
<td>-6v</td>
</tr>
<tr>
<td>Offline</td>
<td>Gnd</td>
<td>Gnd</td>
</tr>
</tbody>
</table>

3. With the arrow on the cable pointing up, plug the tester into the wiring side of the logic gate at location A1N5. Another way to be sure the cable is plugged correctly is to make sure the notches on the cable connector are toward the center of the logic gate. Select, on the tape unit operator's panel, comes on when the Read/Write switch is in the READ position, or in the WRITE position with the MOVE tag active. You can now use the tester switches to load and Ready the tape unit.

Caution: The field tester can cause tape dump and damage under the following conditions:

1. When moving tape with field tester, the direction switch position is changed before activating "Stop." 
2. When attached to a tape unit and set to "Fwd" and either "St/Stop" or "Go," the tape unit is loaded and goes to Load Point and becomes Ready. If RESET on the tape unit console is activated and the tape unit does not dump tape, and then Reset is followed by activating UNLOAD, the tape will run off the end of the reel.
3. When using "Alt Dir," RESET is activated on the tape unit.

Conditions 1, 2, and 3 above can be eliminated by always putting the tester in "Stop" before doing any other operation.

The switches on the tester operate the tape unit by remote control as follows:

- **Start/Reset**
  - Operates the same as the control on the tape unit operator's panel. It makes the unit ready. Reset resets the unit.
  - **Ld Rew/Rew Unld**
  - Ld Rew loads tape if none is loaded, and rewinds tape to load point if tape was loaded but is not at load point. Rew Unld rewinds tape from any position, unloads the unit, closes the cartridge if one is used, and lowers the power window.
  - **Up/Fwd**
  - Up/Fwd controls either the time the MOVE line is active during a start/stop operation, or the duration of forward motion in an alternate-direction operation.
  - **Dn/Bkwd**
  - Dn/Bkwd controls either the time the MOVE line is inactive during a start/stop operation, or the duration of backward motion in an alternate-direction operation.
  - **St/Stp/Go/Stop**
  - St/Stp causes interruptions in tape motion. Use the Up/Fwd control and Slow/Fast switch to adjust go-down time. Use the Dn/Bkwd control and Slow/Fast switch to adjust go-down time. Go ensures continuous tape movement. Use the Alt Dir/Fwd/Bkwd switch to control direction. Stp halts tape motion.
  - **Alt Dir/Fwd/Bkwd**
  - St/Stp/Go/Stop switch must be at Go to enable this switch. Alt Dir is active in read status only; it moves tape alternately forward and backward. Use Up/Fwd control and Slow/Fast switch to adjust duration of forward movement. Use Dn/Bkwd control and Slow/Fast switch to adjust duration of backward movement. Fwd causes forward tape motion. Bkwd causes backward tape motion.
  - **Slow/Fast**
  - This is a range switch for the Up/Fwd and Dn/Bkwd controls. Slow extends the go-up/down timing range to approximately 3.0 seconds. Fast decreases the go-up/down timing range to approximately 7.0 ms.
  - **Write/Read**
  - Write causes the tape unit to write with gaps. Each time the tape unit writes, as in a start/stop operation, it generates a PE gap of 0.528 inch (13.4 mm) and a GCR gap of 0.275 inch (7.0 mm). Read causes continuous reading.
  - **8/16/32 (Models 3, 5, 7)** See Note
  - This switch controls the frequency of the tester's write oscillator. The three positions result in write frequencies of 800 fci (NRZI), 1600 and 3200 fci (PE), respectively.
  - **16/32/64 (Model 4, 6, 8)** See Note
  - When a field tester at EC level 734316 is used on 3420 Models 4, 6, and 8 with the provided jumper installed, these switch positions represent 1600, 3200, and 6400 fci as the label shows. Frequencies generated by the tester are for practical offline test only. Do not confuse these tester frequencies with normal online recording densities.
  - **Note:** The back panel wiring on cable position A1N5 on Models 4, 6, and 8 is such that the frequency of the tester is doubled.
SUBSYSTEM PREVENTIVE MAINTENANCE

GENERAL CLEANING INSTRUCTIONS

This procedure makes all previous 3420 tape unit cleaning procedures obsolete.

Items used by this procedure are contained in the IBM Tape Cleaning Kit, part number 352465 (see Figure 1).

Use IBM tape transport cleaner, part 8493001. Performance results cannot be guaranteed when other chemical formulations are used. Other chemical formulations have not been tested by IBM, and their use may impair performance or cause damage to the tape unit or tape.

DANGER

When using tape cleaner, do not get it on skin or clothing. Follow the instructions on the container. Do not use metal instruments to clean any part of the tape unit.

Figure 1. IBM Tape Cleaning Kit

DAILY CLEANING PROCEDURE

To promote reliable tape unit performance, all of the steps listed below must be performed every eight hours. Clean the tape unit in the sequence presented in this section.

1. Read/write and erase heads (see 85-001)
2. Cleaner blade, BOT/EOT block, rewind plunger, and threading channel reflector (see 85-002)
3. Tape transport (see 85-003)
4. Capstan (see 85-004)
5. File reel hub (see 85-004)
SUBSYSTEM PREVENTIVE MAINTENANCE (Cont’d)

TAPE UNIT CLEANING PROCEDURE FOR 3420 MODELS 3 THROUGH 8

1. R/W AND ERASE HEADS
   1.1 Unload tape and remove from tape unit.
   1.2 Open outer A and inner B doors.

1.3 Dampen clean area of lint-free cloth with tape cleaner.

1.4 When cleaning Models 3, 5, and 7, hold the inspection mirror down, use dampened cloth to clean the R/W and erase heads C using a circular motion.

1.5 When cleaning Models 4, 6, and 8, hold autocleaner in and clean the R/W and erase heads C with a dampened cloth using a circular motion. To reach the inside tracks, wrap the dampened cloth around a cotton swab.

1.6 Repeat steps 1.3 and 1.4 or 1.5 until cloth remains clean.

1.7 Use inspection mirror for Models 3, 5, and 7 or dental mirror for Models 4, 6, and 8, to carefully inspect heads. (Clean mirror with dry cloth, if dirty.) If heads do not look clean, perform step 1.8, otherwise wipe heads with dry clean cloth and go to step 2.

To remove stubborn residue from heads—

1.8 Use either style head cleaning brush dampened with tape cleaner to remove residue C and then return to step 1.3.
TAPE UNIT CLEANING PROCEDURE FOR
3420 MODELS 3 THROUGH 8

2. CLEANER BLADE, BOT/EOT BLOCK,
REWIND PLUNGER, AND THREADING
CHANNEL REFLECTOR

2.1 Hold the inspection mirror down, or the
autocleaner in, when cleaning. Use a cotton swab
dampened with tape cleaner to clean the following
items.

2.1.1 BOT/EOT block E
2.1.2 Rewind plunger/filler block F
2.1.3 Threading channel reflector G

2.2 Use the head cleaning brush (P/N 6851781)
dampened with tape cleaner to clean the cleaner
block H. Wipe with cloth.
3. TAPE TRANSPORT

3.1 Install capstan cover.

3.2 Dampen cotton swab with tape cleaner and clean the following:
   3.2.1 Front and back guides.
   3.2.2 D-bearing.

3.3 Use a lint-free cloth dampened with tape cleaner to clean the following:
   3.3.1 Threading plates.
   3.3.2 Back of inner door.
   3.3.3 Back wall and sides of vacuum columns.
   3.3.4 Air bearings. Note: If residue remains in vacuum column corners, perform steps 3.3.5 and 3.3.6, otherwise go to step 3.4.

To remove stubborn residue in corners of vacuum columns—
   3.3.5 Put clean felt pad on handle making sure the handle does not go through the end of pad.
   3.3.6 Dampen felt pad with tape cleaner and clean vacuum column corners as shown. Make sure no contact is made with capstan cover and/or capstan.

Caution: You may need to use water to remove residue left in the vacuum columns by some tapes. Do not get water on any other part of the machine. Water will damage the capstan.

   3.3.7 Use a lint-free cloth dampened with tape cleaner to remove any residue left by the felt pad.

3.4 Check bottom of vacuum columns for bits of tape and remove if present.

3.5 Remove capstan cover and replace in storage area.
TAPE UNIT CLEANING PROCEDURE FOR 3420 MODELS 3 THROUGH 8

4. CAPSTAN CLEANING—NORMAL PROCEDURE

This procedure must be done at regular intervals by the customer. Tape will slip on a dirty capstan while accelerating.

Caution: Any capstans not kept free of glaze will eventually build a deposit that cannot be removed by a reasonable amount of scrubbing.

4.1 Wrap a clean, dry cloth around one index finger and a lint-free cloth dampened with tape cleaner around the other index finger.

4.2 Vigorously wipe the capstan rubber with the dampened cloth (without bending the capstan) while rotating the capstan with the dry-cloth-covered finger.

4.3 Continue this procedure until the capstan has a definite dull rubber finish. Any glaze must be removed in order to operate reliably.

4.4 If the glaze cannot be removed, follow the special Glazed Capstan Cleaning procedure on page 08-700.

5. FILE REEL HUB

5.1 With a lint-free cloth dampened with tape cleaner, use a light pressure to clean the following:

5.1.1 Back rubber flange

5.1.2 Rubber ring or rubber pads on some models.

6. CARTRIDGE RESTRAINT

6.1 Use a lint free cloth to clean lower restraint. This metal is porous and the air flow can be restricted by using fluids or abrasive material during cleaning.
### SUBSYSTEM PREVENTIVE MAINTENANCE (Cont'd)

#### 3803/3420 PREVENTIVE MAINTENANCE SCHEDULE

#### 3420 Tape Unit

<table>
<thead>
<tr>
<th>Code U R</th>
<th>Location Operation</th>
<th>Frequency</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Door Slide and Stop Pin</td>
<td>4 months</td>
<td>Lubricate the door side and the stop pin with IBM 417.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>General Cleaning</td>
<td>4 months</td>
<td>1. Clean front deck and base.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. Remove tape cleaner block and clean with tape cleaner.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3. Remove air bearing (0 bearing) next to EOT/BOT block and clean. Inspect guides on back bearing and replace if grooved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5. Clean EOT/BOT channel mirror.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6. Clean the fiber optic lamp. Use a tissue lightly moistened with water.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Caution: Allow lamp to cool before cleaning.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Remove the manifold and fiber bundles to provide access to the lamp. Replace the lamp (08-620) if it is not clear. Note: Cleaning or replacement of the fiber optic lamp may require the readjustment of the EOT/BOT and capstan motors.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Capstan Tach Squaring Circuit</td>
<td>4 months</td>
<td>Check and adjust Capstan Squaring. See 08-150 or 08-130. Ensure capstan is free from dents and does not bind.</td>
</tr>
<tr>
<td></td>
<td>Capstan Tracking</td>
<td>4 months</td>
<td>Check and adjust Capstan Tracking. See 08-000.</td>
</tr>
<tr>
<td></td>
<td>EOT/BOT</td>
<td>4 months</td>
<td>Check and adjust EOT/BOT. See 08-580.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>File Protect Pin</td>
<td>4 months</td>
<td>1. Push plunger in, check for bind.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. Check that plunger extends in front of the right hub flange.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3. Replace unit if any checks produce unsatisfactory results.</td>
</tr>
<tr>
<td></td>
<td>Power Window Safety Bail</td>
<td>4 months</td>
<td>Check for the correct operation of the power window safety bail. If incorrect, tighten the set screw in the safety bail terminator, and adjust the safety bail switch assembly (see 08-000).</td>
</tr>
<tr>
<td></td>
<td>Parts Replacement</td>
<td>12 months</td>
<td>Order one of the following B/Ms for required parts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- B/M 8649227 Tachometer type filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- B/M 86492274 Cuno type filter</td>
</tr>
<tr>
<td></td>
<td>Tape Cleaner Block</td>
<td>12 months</td>
<td>Replace the tape cleaner block. Supplied with parts replacement B/M.</td>
</tr>
<tr>
<td></td>
<td>Pneumatic Supply</td>
<td>12 months</td>
<td>Check pneumatic supply belts.</td>
</tr>
<tr>
<td></td>
<td>Input Filter</td>
<td>12 months</td>
<td>Replace filter element of the pressure pump input filter. Supplied with parts replacement B/M. Check for Puristat or Cuno type.</td>
</tr>
<tr>
<td></td>
<td>Cooling Filter</td>
<td>12 months</td>
<td>Clean cooling air filter or replace as necessary.</td>
</tr>
<tr>
<td></td>
<td>Air Bearing Cleaning</td>
<td>12 months</td>
<td>1. Remove bearings.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. Brush each bearing to remove oxide deposits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3. Install new decorative covers on air bearing. Supplied with parts replacement B/M.</td>
</tr>
<tr>
<td></td>
<td>Vacuum Cylinder Door Foam</td>
<td>12 months</td>
<td>Inspect foam in front of vacuum cylinder door glass. See 08-690. If foam replacement is required, order B/M 4489244.</td>
</tr>
<tr>
<td></td>
<td>DC Voltage</td>
<td>12 months</td>
<td>Check the dc voltages. 08-516.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EOT/BOT</td>
<td>12 months</td>
<td>Remove EOT/BOT by removing the two screws and gently move block forward being careful not to damage the fiber bundles if present. Clean EOT/BOT with a cotton swab dampened with tape cleaner. Replace EOT/BOT block.</td>
</tr>
<tr>
<td></td>
<td>Capstan Motor Mod-8</td>
<td>12 months</td>
<td>Clean screens on back of motor with vacuum cleaner.</td>
</tr>
<tr>
<td></td>
<td>Radius Sense</td>
<td>12 months</td>
<td>Clean the ends of the fiber optic bundle if present with a damp cloth, see 08-610 for removal. Apply a light pad to the handle and lightly dampen with tape cleaning fluid. Hold pad to the inside front of the left reel flange and spin by hand. This will clean the reflective strips (located inside the reel).</td>
</tr>
<tr>
<td></td>
<td>Real Tach</td>
<td>12 months</td>
<td>Check real tach for loose. Replace real tach if damaged.</td>
</tr>
<tr>
<td></td>
<td>Glass Bead Tape</td>
<td>12 months</td>
<td>Inspect glass bead tape on stubby bar and vacuum columns. See note. Ensure that stubby bars are not loose and have proper clearance. See 08-000.</td>
</tr>
<tr>
<td></td>
<td>High Speed Rewind Plunger</td>
<td>12 months</td>
<td>Check operation of the High Speed Rewind Plunger. See 08-005 Models 3, 5, and 7 only.</td>
</tr>
<tr>
<td></td>
<td>Autocleaner Check</td>
<td>12 months</td>
<td>1. Check operation of autocleaner by marking the ribbon and observing ribbon movement. The ribbon should move from bottom to top.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. Check the supply of autocleaner ribbon. Order a new autocleaner cartridge when approximately 3/4 inches of ribbon is visible through the cartridge window. Models 4, 6, and 8 only.</td>
</tr>
<tr>
<td></td>
<td>Preamps</td>
<td>12 months</td>
<td>Check and adjust preamps (08-298 or 09-300).</td>
</tr>
</tbody>
</table>

#### 3803 Control Unit

<table>
<thead>
<tr>
<th>Code U R</th>
<th>Location Operation</th>
<th>Frequency</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Air Filter</td>
<td>2 months</td>
<td>Check cooling air filter for restriction of air flow. Clean or replace as required.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>dc Voltage</td>
<td>6 months</td>
<td>Check dc voltages. Adjust as required to the levels specified on dc panel.</td>
</tr>
</tbody>
</table>

#### Code Chart

<table>
<thead>
<tr>
<th>Code</th>
<th>Location Operation</th>
<th>Frequency</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>U R</td>
<td>Output Filter</td>
<td>36 months</td>
<td>Replace with P/N 2524998.</td>
</tr>
<tr>
<td></td>
<td>Vacuum Tubing</td>
<td>60 months</td>
<td>Replace vacuum tubing (order B/M 4414600).</td>
</tr>
<tr>
<td></td>
<td>Pressure Tubing</td>
<td>60 months</td>
<td>Replace pneumatic pressure tubing (order B/M 4414608).</td>
</tr>
<tr>
<td></td>
<td>Vacuum Pressure Switches</td>
<td>60 months</td>
<td>Replace vacuum pressure switch (order B/M 868176).</td>
</tr>
<tr>
<td></td>
<td>Right switch plate</td>
<td>- - - - - -</td>
<td>- seven holes - B/M 8681765</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- - - - - -</td>
<td>- five holes, one switch top, three grouped center, one at bottom - B/M 8681766</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- - - - - -</td>
<td>two switches top, three at bottom - B/M 8681764</td>
</tr>
</tbody>
</table>

#### Note:

Inspect the glass bead surface of the stubby bars and vacuum columns. Replace if the glass bead is nicked, scratched, burred or has an area obviously worn to the touch. (If not obviously worn, do not replace!)

Run finger on the glass bead surface at the bottom of the vacuum column. This is a good glass bead surface and may be used as a reference. A worn glass bead surface will cause tape motion problems.
SUBSYSTEM INSTALLATION

INTRODUCTION
This section contains installation instructions for the IBM 3803 Model 2/3420 Magnetic Tape Subsystem. Companion publications pertaining to this product are:

1. 3803 Model 2/3420 Subsystem Description, GA32-0021
2. 3420 Model 4, 6 and 8 Parts Catalog, S132-0007
3. 3803 Models 1 and 2 Parts Catalog, S132-0004
5. 3803/3420 OLT Users Guide

Safety Note: Ensure your own safety by using caution at all times and by being aware of potentially dangerous areas of the machine. Read and follow the safety suggestions in Form 229-1264, a pocket-sized card issued to all customer engineers and reprinted at the front of this manual.

Caution: No portion of this procedure is to be omitted. Perform all steps including checks and adjustments.

INSTRUCTIONS
Perform the following basic steps for each 3803 Model 2/3420 installation, regardless of the subsystem configuration:

1. Refer to the checklist on 90-020 and initial each box when an installation procedure is completed.
2. Complete the configuration worksheet on 90-040. Refer to the instructions on 90-030.
3. Unpack units. (See Unpacking Instructions on this page.)
4. Remove the wire seal from the 3B03 and 3420's, 90-1BO, only at this time.
5. Install four caster locks.
6. Install front and both side kickplates. See 90-090.
7. Install rear kickplate. See 90-090.
8. Install and plug cables. See 90-050 through 90-080.
9. Plug address/feature/priority card jumpers to match configuration requirements, see 90-110.
10. Rework the 3420 Field Tester, see 90-170.

Note: Before moving 3420 tape units into place, be sure to remove packing tape from the air flow mercury switch and install the front kickplate. Check ESD grounding. See 90-190, F7 and FB before moving machines into place.

Note: The tag and bus cable pairs must be of equal length. Paired cables of unequal length cause timing errors resulting in hard-to-diagnose subsystem problems.

12. Perform all checks and adjustments on 90-190.
13. Run system diagnostics on 90-200. (Refer to User's Guide.)
14. If any Emulator is run on a S/360, install jumper, see 90-200.
15. Generate a read only tape, on 90-200.

Note: It is possible to combine 3803 Models 1 and 2 in one subsystem. Be sure your customer understands that a 3803 Model 1 tape control cannot address any 3420 Models 4, 6, or 8 tape units.

UNPACKING INSTRUCTIONS
Unpack tape control and tape units.
Refer to Unpacking Instructions, which are in a plastic envelope attached to each unit. Move discarded packing material away from work area. File Unpacking Instructions for future reference if tape subsystem is to be moved.

Note: Make sure customer's power matches subsystem requirements. Check for correct blower and motor rotation.
11. Perform power supply checks and note special tape unit power supply requirements, see 90-180.
SUBSYSTEM INSTALLATION (Cont'd)

CHANNEL ATTACHMENT

The 3803 Model 2 at 6250 bpi will attach to these systems via the indicated channels:

<table>
<thead>
<tr>
<th>System</th>
<th>3420-6</th>
<th>3420-6</th>
<th>3420-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>370: 195</td>
<td>2860/2880</td>
<td>2860/2880</td>
<td>2860/2880</td>
</tr>
<tr>
<td>370: 165</td>
<td>2860/2880</td>
<td>2860/2880</td>
<td>2860/2880</td>
</tr>
<tr>
<td>370: 165-2</td>
<td>2860/2880</td>
<td>2860/2880</td>
<td>2860/2880</td>
</tr>
<tr>
<td>370: 165</td>
<td>2860/2880</td>
<td>2860/2880</td>
<td>2860/2880</td>
</tr>
<tr>
<td>370: 158</td>
<td>BKMPX</td>
<td>BKMPX</td>
<td>BKMPX</td>
</tr>
<tr>
<td>370: 155-2</td>
<td>BKMPX</td>
<td>BKMPX</td>
<td>BKMPX</td>
</tr>
<tr>
<td>370: 155</td>
<td>BKMPX</td>
<td>BKMPX</td>
<td>BKMPX</td>
</tr>
<tr>
<td>370: 145</td>
<td>SEL</td>
<td>SEL</td>
<td>SEL</td>
</tr>
<tr>
<td>370: 135</td>
<td>SEL</td>
<td>SEL</td>
<td>SEL</td>
</tr>
<tr>
<td>360: 195</td>
<td>2860/2880</td>
<td>2860/2880</td>
<td>2860/2880</td>
</tr>
<tr>
<td>360: 91</td>
<td>2860</td>
<td>2860</td>
<td>2860</td>
</tr>
<tr>
<td>360: 95</td>
<td>2860/2880</td>
<td>2860/2880</td>
<td>2860/2880</td>
</tr>
<tr>
<td>360: 75</td>
<td>2860</td>
<td>2860</td>
<td>2860</td>
</tr>
<tr>
<td>360: 65-67</td>
<td>2860</td>
<td>2860</td>
<td>2860</td>
</tr>
<tr>
<td>360: 50</td>
<td>N/A</td>
<td>N/A</td>
<td>SEL</td>
</tr>
</tbody>
</table>
### INSTALLATION CHECKLIST
3803-2 TAPE CONTROL

<table>
<thead>
<tr>
<th>Installation Procedure</th>
<th>Reference Page</th>
<th>Initial Box When Completed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration Worksheet</td>
<td>90-020</td>
<td></td>
</tr>
<tr>
<td>Unpacking</td>
<td>90-000</td>
<td></td>
</tr>
<tr>
<td>Cables</td>
<td>90-060 90-070 90-080</td>
<td></td>
</tr>
<tr>
<td>Cable Retaining Bar</td>
<td>90-080</td>
<td></td>
</tr>
<tr>
<td>Kickplates</td>
<td>90-090</td>
<td></td>
</tr>
<tr>
<td>Address/Priority/Feature Plugging</td>
<td>90-110</td>
<td></td>
</tr>
<tr>
<td>Card and Cable Seating</td>
<td>90-000</td>
<td></td>
</tr>
<tr>
<td>Operator's Panel Labels</td>
<td>90-160</td>
<td></td>
</tr>
<tr>
<td>Wire Seal Removal</td>
<td>90-180</td>
<td></td>
</tr>
<tr>
<td>Check Capacitor Mounting Screws</td>
<td>90-180</td>
<td></td>
</tr>
<tr>
<td>Power Supply Checks</td>
<td>90-180</td>
<td></td>
</tr>
<tr>
<td>ESD Check and Adjustment</td>
<td>90-190</td>
<td></td>
</tr>
<tr>
<td>System Diagnostics</td>
<td>90-200</td>
<td></td>
</tr>
<tr>
<td>Emulator (If applicable)</td>
<td>90-200</td>
<td></td>
</tr>
<tr>
<td>Generate READ ONLY Tape</td>
<td>90-200</td>
<td></td>
</tr>
</tbody>
</table>

### 3420 TAPE UNIT

<table>
<thead>
<tr>
<th>Installation Procedure</th>
<th>Reference Page</th>
<th>Initial Each Box When Completed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unpacking</td>
<td>90-000</td>
<td>0/8 1/9 2/10 3/11 4/12 5/13 6/14 7/15</td>
</tr>
<tr>
<td>Cables</td>
<td>90-060 90-070</td>
<td></td>
</tr>
<tr>
<td>Caster Locks</td>
<td>90-000</td>
<td></td>
</tr>
<tr>
<td>Kickplates</td>
<td>90-090 90-100</td>
<td></td>
</tr>
<tr>
<td>Field Tester Conversion</td>
<td>90-170</td>
<td></td>
</tr>
<tr>
<td>Wire Seal Removal</td>
<td>90-180</td>
<td></td>
</tr>
<tr>
<td>Power Supply Checks</td>
<td>90-180</td>
<td></td>
</tr>
<tr>
<td>Checks and Adjustments</td>
<td>90-190</td>
<td></td>
</tr>
<tr>
<td>System Diagnostics</td>
<td>90-200</td>
<td></td>
</tr>
</tbody>
</table>
Complete the configuration worksheet on Page 90-040 for your installation. Check customer requirements before configuring each system. When installation is completed, place worksheet in the front of subsystem ALDs and keep as a subsystem cabling history.

Complete all applicable blocks in the worksheet for each 3803 tape control:

1. Indicate each 3803 serial number in decimal.
2. Indicate processing unit/Channel identity and cable numbers.
3. Assign an address to each 3803 tape control in hex (bits 0-4. Example: 18X/3BX).
4. Assign "Select Out" priority ("high"/"low") for each interface by checking applicable box.
5. Assign 3420 addresses to each 3803. Check the 0-7 (low order) block on one "host" 3803, and the 8-F (high order) block on the other "host" 3803.
6. Assign "Select Out" priority ("high"/"low") for each interface by checking applicable box.
7. Draw in cabling for your configuration and insert cable key numbers.
**SUBSYSTEM INSTALLATION (Cont’d)**

**CONFIGURATION WORKSHEET**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Select Out Priority</td>
<td>(Hex)</td>
<td>(High)</td>
<td>(Low)</td>
<td>(Hex)</td>
<td>(High)</td>
</tr>
<tr>
<td>I/O TAILGATE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Symbols 1 through 6 refer to control switch paths A through D of the device switching feature. (See Section 5B for further information on this feature.)

---

3803 Serial Number | (Decimal) |
--- | --- |
Select Out Priority  | (Hex)      | (High)    | (Low)                | (Hex)      | (High)    | (Low) |
I/O TAILGATE         |            |           |                      |            |           |       |
--- | --- |

3803 Serial Number | (Decimal) |
--- | --- |
Select Out Priority  | (Hex)      | (High)    | (Low)                | (Hex)      | (High)    | (Low) |
I/O TAILGATE         |            |           |                      |            |           |       |
--- | --- |

---

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SUBSYSTEM INSTALLATION (Cont'd)

SECTION A: DEVICE SWITCHING FEATURE

A-1 Tape subsystem configuration flexibility is provided by field-installable switching features that allow up to 16 tape units to be switched between four tape controls. The three device switching features available with the tape subsystem are:

2 Control Switch (2 X 8 or 2 X 16 configuration, see Figures 1 and 4 on page 90-051)
3 Control Switch (3 X 8 or 3 X 16 configuration, see Figures 2 and 3 on page 90-051)
4 Control Switch (4 X 8 or 4 X 16 configuration, see Figures 5 and 6 on page 90-052)

A 3803 must have a Communicator installed in order to be switched. The Communicator sends tape unit selection and device interface signals to one of two device switches, depending on whether tape units 0 through 7 or 8 through F are being addressed. The location of the device switches depends on the configuration desired. For example: In a 2, 3, or 4 X 8 configuration, the switching feature is required only on the first 3803.

The Communicator is installed by removing the selection logic circuits and the associated device interface cabling in the basic 3803. Different logic circuitry and cables to the device switches are then installed.

Using a combination of the Communicator and the 2, 3, or 4 Control Switch, two, three, or four interconnected tape controls can address a maximum of 16 tape units. Figures 1 through 6 show some possible switching configurations and cabling.

Note:

[1] The dark gray end of the signal cable is indicated by the arrow tip. (See Figure 1, 90-060.)

Figure 7. Cable Connectors

Note: The dark gray end of the signal cable is indicated by the arrow tip. (See Figure 1, 90-060.)
Figure 5. 4 x 8 Switch Option

Figure 6. 4 x 16 Switch Option
SUBSYSTEM INSTALLATION (Cont'd)

SECTION B. SUBSYSTEM CABLING

B-1 Unpack the interface and power cables and lay in place.

Refer to the "Key Number" or "Connector ID" and "X-Length" shown on each interface cable label when placing cables (see Figure 3).

Refer to power cable connector (see Figure 2) to ensure that power cables will be located correctly.

Caution: Ensure that the color scheme on the connectors is followed.

B-2 Plug Cables and Terminators:

a. Plug cables at tape control and tape units. Each tape unit's address is determined by the position on the tape control interface panel to which its signal cable is connected.

Caution: Do not connect 3803 power cable to customer's receptacle at this time.

b. Insert terminators in "outgoing" cable positions in subsystems where "outgoing" cables 132 and 133 are not used.

c. Install cable retaining bars when cabling is complete.

B-3 Observe "from" and "to" designations given in Figure 1, Page 90-070. Red or red-striped labels indicate "from" end of cables; white labels indicate "to" ends of cables.

---

Note: On chrome plated tape unit signal cable connectors, observe the color at the center screw hole.

---

Figure 1. Signal Cable

Figure 2. Power Cable

Figure 3. Dimension Explanation

"X" Dimension = Distance Between Cable Entry Holes In Floor

"Y" & "Z" Dimension = Distance Above the Floor from the Entry Hole to the Connection within the Machine

Total Length = sum of X, Y, and Z dimensions.
SUBSYSTEM INSTALLATION (Cont'd)

SECTION B. SUBSYSTEM CABLING (Cont'd)

Figure 1. External Cables

Note: Cables are identified by either key number or connector ID.

<table>
<thead>
<tr>
<th>Group No.</th>
<th>Conn. ID</th>
<th>Plug Location</th>
<th>Cable Group</th>
<th>Key No.</th>
<th>Cable P/N</th>
<th>From</th>
<th>To</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>DIS-1A1</td>
<td>129</td>
<td>2281630</td>
<td>3420 Signal 60 Hz</td>
<td>3803</td>
<td>4, 5, 7</td>
</tr>
<tr>
<td>3920</td>
<td>1B (Chan A)</td>
<td>DIS-1A1</td>
<td>130</td>
<td>130 B</td>
<td>5359320</td>
<td>3803</td>
<td>Multiplexer Channel</td>
<td>1, 9</td>
</tr>
<tr>
<td>3920</td>
<td>2B (Chan A)</td>
<td>DIS-1A1</td>
<td>131</td>
<td>131 B</td>
<td>5359320</td>
<td>3803</td>
<td>Control Unit</td>
<td>1, 9</td>
</tr>
<tr>
<td>3920</td>
<td>4B (Chan B)</td>
<td>DIS-1A1</td>
<td>132</td>
<td>132 B</td>
<td>5359320</td>
<td>3803</td>
<td>Channel-Adapter</td>
<td>1, 3, 9</td>
</tr>
<tr>
<td>3920</td>
<td>7A (Chan B)</td>
<td>DIS-1A1</td>
<td>133</td>
<td>133 B</td>
<td>5359320</td>
<td>3803</td>
<td>Channel EPO</td>
<td>2</td>
</tr>
</tbody>
</table>

Figure 2. Channel Cable Maximum Length for 6250 bpi.

<table>
<thead>
<tr>
<th>System</th>
<th>From 3803-2</th>
<th>To Channel</th>
<th>Length - Feet (Meters)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5/360</td>
<td>3420-8</td>
<td>2860-8</td>
<td>72 (22.0) 119 (36.3)</td>
</tr>
<tr>
<td>5/370</td>
<td>3420-8</td>
<td>2880-135</td>
<td>72 (22.0)</td>
</tr>
<tr>
<td>4331</td>
<td>3420-6/8</td>
<td>None</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Notes:

1. To attach eight or less tape controls to one channel, the last tape control must be attached to the channel with a sum of no more than 200 feet (61,0m) of cable. If the tape control is attached to a 3420-8, subtract 15 feet (4,5m) for each intervening control unit between the channel and the last tape control. If the tape control is attached to a 3420-8, subtract 20 feet (6,1m) for each intervening control unit between the channel and the last tape control (see Note 10). For cable length limitations when attaching 3803-2 at 6250 BPI, see Figure 2.

2. Sequence and Control (EPO).

3. Channel to channel adapter (Sales Feature 1850).

4. Total cable length from a 3420 tape unit to the most remote 3803 tape control must not exceed 120 feet (36.6m). (Group 129 or 142, or 143, plus group 136-141.)

5. Includes both signal and power cable. A maximum of eight 3420 tape units can be connected to each 3803 Tape Control 1 and 2. Tape units cannot be connected to tape control 3 and 4 for power requirements unless they are used with cable group 144.

6. Parenthesis indicates cables to be used in World Trade countries for 60 Hz machines.

---

[Text continues with various notes and specifications relevant to the cables and systems described, including notes on power, sequence, and channel connections.]

---

[Figure and diagrams showing cable connections and length specifications are included, along with specific notes on cable usage and limitations.]

---

[The page includes various tables and figures that detail specific cable group numbers, connector IDs, and their respective uses and limitations, ensuring comprehensive coverage of the subsystem installation and cabling.]
SUBSYSTEM INSTALLATION (Cont'd)

SECTION B. SUBSYSTEM CABLING (Cont'd)

Caution: Refer to ALD AA005 Feature Plug List before installing a replacement logic board.

Notes:

Two-channel switch diagnostics AD through AG can only be run when both channel interfaces are cabled to the same central processing unit. If it is necessary to run diagnostics AD through AG during initial checkout, plan temporary cabling to meet this requirement.

[1] Both EPO cables must be plugged if the two channel switch feature is installed, and the two channels are not on the same processing unit or not on the same channel frame. Remove any temporary jumper plugs.

[2] For cable, part 5466456 (48 pin), use terminator, part 2282675 (bus) and 2282676 (tag).

For cable, part 5440849 (bus) and 5440850 (tag).

[3] Panel Y1 is located in position O1A-A3 unless the 3803-2 has optional features installed. On feature machines, panel Y1 is located in position O1X-Y.

[4] For cable group number, key number, part number, to and from relationship, see Figure 1 on 90-070.

* Cables plugged when the two-channel switch feature is present.

Notes:

Two-channel switch diagnostics AD through AG can only be run when both channel interfaces are cabled to the same central processing unit. If it is necessary to run diagnostics AD through AG during initial checkout, plan temporary cabling to meet this requirement.

[1] Both EPO cables must be plugged if the two channel switch feature is installed, and the two channels are not on the same processing unit or not on the same channel frame. Remove any temporary jumper plugs.

[2] For cable, part 5466456 (48 pin), use terminator, part 2282675 (bus) and 2282676 (tag).

For cable, part 5440849 (bus) and 5440850 (tag).

[3] Panel Y1 is located in position O1A-A3 unless the 3803-2 has optional features installed. On feature machines, panel Y1 is located in position O1X-Y.

[4] For cable group number, key number, part number, to and from relationship, see Figure 1 on 90-070.

* Cables plugged when the two-channel switch feature is present.
SUBSYSTEM INSTALLATION (Cont'd)

SECTION C. KICKPLATES

C-1 Install 3803 front and rear kickplates and 3420 rear kickplates as shown in Figure 1.

1. Attach pins, nuts, and retaining clips to front and rear frame members of the 3803 and rear frame member of each 3420 as shown in Figure 1.
2. Mount kickplates by pushing brackets onto pins. Clips must be positioned below lower flange of brackets.

Note: Leave 3420 rear kickplates off until cabling is complete.
3. Turn nuts on pins to level kickplates.
4. If necessary, realign 3803 covers after kickplate installation.

C-2 Install 3420 front kickplates as shown in Figure 2.

1. Install front kickplates before moving tape units into place.
2. Elongated holes in the bracket allow kickplate to be leveled and adjusted to clear the front cover.

Figure 1. 3803 (Front and Rear Kickplates) 3420 (Rear Kickplates)

Figure 2. 3420 (Front Kickplates)
SECTION C. KICKPLATES (Cont'd)

C-3 Install 3803 and 3420 side kickplates as shown in Figure 3.

1. Install side kickplates only on the machines at each end of a group. Use screw P/N 731629.
2. Open or remove covers to attach kickplates. Use 12-inch (305 mm) kickplate, part 2501286 (notched corner), on cover adjacent to tape unit power door hinge. Use 1 1/8-inch (333 mm) kickplate, part 5356406, on remaining side covers for 3420 tape units and 3803 tape controls.

C-4 Typical Subsystem Configuration

Sufficient side kickplates, parts 2501286 and 5356406, are shipped for the configuration shown in Figure 4. Kickplates are not provided for installation between adjacent tape units. Order additional side kickplates by MES, if needed for other configurations.

C-5 Install caster locks (4 each), P/N 280336.
SUBSYSTEM INSTALLATION (Cont'd)

SECTION D. TAPE CONTROL
ADDRESS/FEATURE/PRIORITY CARD PLUGGING

D-1 3803 Address (Channel "A"): Verify factory plugging.

Card row 6-1
Card location = B3M2
Card type = 2258
"1"3-high" card

Example:
Bus Out 4 3 2 1 0
Card Row 6 9 4 3 1
Card Col.
Z
Y
X

Plug if 3803 has device switching capability.
Plug if 3803 has selection logic (1xS)
with 3420s addressed 0-F.

Example shows card plugged for:
a. 3803 with address = 8
b. With device switching capability.

D-2 Disconnect-In Handling: S/360 or S/370.

Card row 4-2
Card location = B2L2
Card type = 1538
"1"2-high" card

Plug this position for 360.

Plug this position for 370.

Plugging Data
360 Plug 360 if either Chan A (or B with 2CS) is connected to any channel that does not have disconnect in handling capability.
370 Plug 370 if Chan A (and B with 2CS) is connected to any channel that has disconnect in handling capability.

Card row 36-34
Card location = B2L2
Card type = W046
"1"3-high" card
SUBSYSTEM INSTALLATION (Cont'd)

SECTION D. TAPE CONTROL ADDRESS/FEATURE/PRIORITY CARD PLUGGING
(Cont'd)

D-3 Select Out Priority:

Tape controls are factory-wired to respond to a select out signal (high priority). If ("low priority") is desired, change the B2 panel wiring to convert a 3803 tape control to respond to a select in signal. Refer to wiring charts below for rework.

<table>
<thead>
<tr>
<th>'High' Priority (3803 Responds to 'Select Out')</th>
<th>'Low' Priority (3803 Responds to 'Select In')</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel A (FC281)</td>
<td></td>
</tr>
<tr>
<td>From</td>
<td>To</td>
</tr>
<tr>
<td>V4D09</td>
<td>S2P09</td>
</tr>
<tr>
<td>74B09</td>
<td>V4D08</td>
</tr>
<tr>
<td>52P11</td>
<td>T4D09</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel B (XM181)</td>
<td></td>
</tr>
<tr>
<td>From</td>
<td>To</td>
</tr>
<tr>
<td>U4C02</td>
<td>R2P09</td>
</tr>
<tr>
<td>U4B08</td>
<td>U4B04</td>
</tr>
<tr>
<td>R2P11</td>
<td>U4D09</td>
</tr>
</tbody>
</table>

b. Two-channel switch feature (3803 Address Channel "B"). Verify factory plugging.

Card location = 82N2
Card type = 9149

D-4 Features (when applicable to your machine):

a. Two Channel Switch Feature: Verify factory plugging.

Card location = 8202
Card type = W032

Example:

Channel Address
Bus Out 4 3 2 1 0
Card Row 6 5 4 3 2 1
Card Col T S R

Plug for
Plug for
Plug if 3803 has device switching capability.
Plug if 3803 has selection logic (1x8) with 3420s addressed 0-7.
Plug if 3803 has selection logic (1x8) with 3420s addressed 8-F.

Example shows card plugged for:

a. 3803 with address = 8.
b. With device switching capability.

c. NRZI Feature: Verify factory plugging.

Card location = A2M2
Card type = 9149

Example shows card plugged:

Card location = A2M2
Card type = 9032

Example shows card not plugged:

Card location = A2M2
Card type = 9032
SUBSYSTEM INSTALLATION (Cont'd)

SECTION D. TAPE CONTROL
ADDRESS/FEATURE/PRIORITY CARD
PLUGGING (Cont'd)

D-5 Primary/Secondary Tape Unit Interface Control:

a. With device switching capability.

Card row 27-25
Card location = A2E2
Card type = 9909

b. With selection logic (1x8).

Card row 30-28
Card location = A2E2
Card type = 9910

---

D-6 a. Data In Handling: S/360 or S/370.

Card row 48'47 40 35

Plug each channel independently as follows:

*360  Plug 360 if the attached channel does not have data in/data out capability.

**370  Plug 370 if the attached channel has data in/data out capability.

If attached to a 2880 channel, bus out checks may occur if channel timings are not optimized.

*W/O 2CS—Channel B may be plugged to 360 or 370 since it is not used.

---

Note: A 3803 tape control with selection logic (1x8) only uses the secondary interface.
D-7 Tape Switching Feature Address Control: Change or verify jumper plugging of host 3803 tape controls only.

1. For installations with less than a full complement of 3420 tape units (for example, 2x12), plug all cards present as if the non-existent tape units had addresses assigned to them.

Jumper cable locations for switch cards:

<table>
<thead>
<tr>
<th>Card Row</th>
<th>Column</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

2. As each switch card is pulled, refer to the chart on Page 90-150 and verify that device selection priority assignments are correct.
SUBSYSTEM INSTALLATION (Cont'd)

SECTION D. TAPE CONTROL
ADDRESS/FEATURE/PRIORITY CARD
PLUGGING (Cont'd)

D-8 Device Selection Priority Assignments: Verify that factory plugging of priority jumpers on the switch cards is correct.

Plugging Rules:
1. A priority must be assigned to each set of cards.
2. No duplication of priority should exist between sets of cards in one 3803 tape control.
3. All cards must have T23-U23 connected by a jumper wire.
4. Factory plugging for these cards should be as shown, and should not have to be changed for any installation.
5. This plugging establishes priority; if two 3803s try to access the same 3420 tape unit simultaneously, the 3803 with the least number of jumpers will take control.

Connect a jumper cable to locations for switch cards as shown below:

---

3803 Switch Path "A"
Location: B3H2 B3K2
Priority 1

3803 Switch Path "B"
Location: B3J2 B3L2
Priority 2

3803 Switch Path "C"
Location: A2N2 A3S2
Priority 3

3803 Switch Path "D"
Location: A3P2 A3T2
Priority 4

---

3803-2/3420
J09600 2736027 See EC History 845960 01
See 1 of 2 1 See 76

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SECTION D. TAPE CONTROL
ADDRESS/FEATURE/PRIORITY CARD
PLUGGING (Cont'd)

D-9 Apply labels to tape control operator's panel as shown.

a. Operator's Panel Labels
   For the 3803 that "hosts" tape units 0-7:
   1. Use labels furnished to indicate addresses of tape control associated with each group of operator panel switches.
   2. Apply 3420 address labels 0-7 above each group of switches as shown.

b. Operator's Panel Labels
   For the 3803 that "hosts" tape units 8-F:
   1. Use labels furnished to indicate tape control addresses associated with each group of operator panel switches.
   2. Apply 3420 address labels 8-F above each group of switches as shown.

Note: Symbols through refer to control switch paths A through D of the device switching feature.
FIELD TESTER CONVERSION

Do the following rework to make the field tester compatible with 3420 Models 4, 6, and 8. The new EC Level is 734316. (The field tester remains compatible to 3420 Models 3, 5, and 7.)

1. Remove the four screws from the bottom of the tester. Then remove the cover. Check the probe side of the card/connector socket block:
   a. If connections are made by means of a printed circuit card, replace the cover and four retaining screws, then skip to step 7.
   b. If connections are made by means of wire wrapping, proceed to step 2.

2. Remove the logic card, unplug the signal cables, and slide the connector block out.

3. Delete yellow wire from B1G02 to A2B13.

4. Add #30 gauge SLT wire from B1J05 to A2B13.

5. Reassemble the tester: slide the connector block into the tester, plug the cables, and install the logic card.

6. Replace the cover and the four retaining screws.

7. Install label, part 1845758, to the right of the data rate switch (8, 16, 32) as shown.

8. Install label, part 1845760, over the existing instructions (1-3) on top of the tester.

9. Before converting a Model 3, 5, or 7 tape unit to a Model 4, 6, or 8, take the tape unit offline. Then connect the field tester.
   Note: Simulate a Model 4, 6, or 8 by grounding N5B02 on the tape unit.

10. Mount and load a CE work tape. Then set the field tester to WRITE CONTINUOUS. See 80-020.

11. Scope test point A1H111 (WRITE DATA TRACK P), at the tape unit. Observe a full write cycle period and compare to the chart below. Make sure the data rate switch is set correctly for the tape unit model being used.
   Note: Times are nominal and are given in microseconds. Tolerance is ±5%.

---

<table>
<thead>
<tr>
<th>Data Rate Switch Position</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8</td>
</tr>
<tr>
<td>3</td>
<td>32.8</td>
</tr>
<tr>
<td>4</td>
<td>—</td>
</tr>
<tr>
<td>5</td>
<td>20.0</td>
</tr>
<tr>
<td>6</td>
<td>—</td>
</tr>
<tr>
<td>7</td>
<td>12.4</td>
</tr>
<tr>
<td>8</td>
<td>—</td>
</tr>
</tbody>
</table>

Note: Take any 3420 tape unit Incident Report (IR) and code your time, using Service Code 33, ECA #991.

---

1. Unload drive before plugging or unplugging tester.
2. Place tape unit in off-line status.

---

<table>
<thead>
<tr>
<th>MOD 4,6,8</th>
<th>1600</th>
<th>6250</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>32</td>
<td>N/A</td>
<td>64</td>
</tr>
</tbody>
</table>

---

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SUBSYSTEM INSTALLATION (Cont'd)

SECTION E. POWER SUPPLY CHECKS

E-1 Remove the wire seal from the 3420 tape unit J1 power connector, and the wire seal from around the 3803 Model 2 power plug.

E-2 With power off, check the 18 filter capacitor mounting screws on the 3803 Model 2 tape control's -6v and -4v power supplies. If loose, tighten the screws being careful not to over-torque and damage the power board. Also, check all other power supply screws and connections. (See 08-575.)

E-3 With power off, check that the customer's supply voltage matches that shown on the voltage rating label.

Note: To connect a 3803 tape control for operation at a different input voltage, refer to 3803 logic page YF010 (60 Hz) or YF015 (50 Hz).

See Page 08-570 to determine if each tape unit has a modified power supply. Then, refer to logic pages listed for the connections to be changed:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Logic Pages Affected</th>
<th>Test Point</th>
<th>Tolerance (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 Hz</td>
<td>YB010*, YB020*, YB030#</td>
<td>-6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td></td>
<td>YB015*, YB025#, YB035#</td>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

3420 Tape Unit Models 4, 6, and 8:

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

Note 1: Ripple specifications for -4v and -6v are 24 mv peak-to-peak. Measure at power supply. Refer to DC Logic page for your machine for TB locations. YB020, YB025 or YF020, YF035.

3803 Tape Control

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4v</td>
<td>±0.01v</td>
</tr>
<tr>
<td>4.0v</td>
<td>±0.1v</td>
</tr>
</tbody>
</table>

Note 2: Ripple specification for -4v is 80 mv peak-to-peak and for -6v is 10 mv peak-to-peak. Measure at power supply.

Caution: A ground loop has been purposely installed in the 3803 tape control for electro-static discharge (ESD) control. The installed ground loop is in the tape signal tail gate connector, and must be disassembled to check for other ground loops.

The tape control is checked at the factory for ground loops.

E-4 Customer Power Phasing

Check three-phase ac power receptacles to ensure proper motor rotation in each unit. Any improper phasing must be corrected before power is applied to the subsystem.

E-5 With power on, check that all blowers and motors operate correctly.

a. Incorrect phasing of input voltage causes the tape unit pneumatic supply motor to turn backward, preventing the tape unit from loading.

b. The cooling fan assembly blower motor in the tape unit will run backwards. Remove filter from machine and observe the direction of the fan as power is dropped. Fan should turn clockwise when viewed from below. (See arrow.)

Note: All blowers in the tape control are single phase.

E-6 Mount and load a tape. Using a Digital Voltmeter, part 453585, 453046, or equivalent, check that the +6 volt and -4 volt power supplies are within the tolerances listed:

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

Note 3: Ripple specifications for +6v and -4v are 24 mv peak-to-peak. Measure at power supply.

3420 Tape Unit Models 3, 5, and 7:

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

Note: To connect a 3803 control's connections.

E-7 With power off, check that the customer's voltage rating, refer to 3803 logic page YF010 (60 Hz) or YF015 (50 Hz).

See Page 08-570 to determine if each tape unit has a modified power supply. Then, refer to logic pages listed for the connections to be changed:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Logic Pages Affected</th>
<th>Test Point</th>
<th>Tolerance (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 Hz</td>
<td>YB010*, YB020*, YB030#</td>
<td>-6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td></td>
<td>YB015*, YB025#, YB035#</td>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

3420 Tape Unit Models 4, 6, and 8:

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

Note 1: Ripple specifications for -4v and -6v are 24 mv peak-to-peak. Measure at power supply. Refer to DC Logic page for your machine for TB locations. YB020, YB025 or YF020, YF035.

3803 Tape Control

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4v</td>
<td>±0.01v</td>
</tr>
<tr>
<td>4.0v</td>
<td>±0.1v</td>
</tr>
</tbody>
</table>

Note 2: Ripple specification for -4v is 80 mv peak-to-peak and for -6v is 10 mv peak-to-peak. Measure at power supply.

Caution: A ground loop has been purposely installed in the 3803 tape control for electro-static discharge (ESD) control. The installed ground loop is in the tape signal tail gate connector, and must be disassembled to check for other ground loops.

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<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

Note 3: Ripple specifications for +6v and -4v are 24 mv peak-to-peak. Measure at power supply.

3420 Tape Unit Models 3, 5, and 7:

<table>
<thead>
<tr>
<th>Test Point</th>
<th>Tolerance (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6v</td>
<td>±0.1v</td>
</tr>
<tr>
<td>4.06v</td>
<td>±0.06v</td>
</tr>
</tbody>
</table>

Special Power Requirements—3420 Model 8, 80 Hz Only

In certain 1x8 or 2x16 - 3420 configurations, which include the 3420 Model 8, a single 3803 cannot supply the necessary for the operation of the subsystem without a special power feature. The table below shows the maximum number of tape units that may be powered from one 3803 without this special feature.

<table>
<thead>
<tr>
<th>Number of</th>
<th>Number of</th>
<th>Number of</th>
</tr>
</thead>
<tbody>
<tr>
<td>3420</td>
<td>3420</td>
<td>3420</td>
</tr>
<tr>
<td>Model 8's</td>
<td>Model 7's</td>
<td>Model 3-6</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

* If only one 3420 Model 8, then any combination of seven additional tape units is permissible.

If your customer's requirement exceeds the table, you must order SF8001 for the 3803(8). For example, if he needs more than six Model 8's or two Model 8's and six Model 3-6's on a single 3803.

In all cases where this power supply feature is ordered, the customer must install a 100 Amp power source.
SUBSYSTEM INSTALLATION (Cont'd)

SECTION F. CHECKS AND ADJUSTMENTS

Note: Make sure the write head card is seated properly before continuing.

This section outlines checks, adjustments, and tests to ensure that the tape units and tape controls operate normally when the subsystem is turned over to the customer. See "Checks, Adjustments, Removals, and Replacements" sections of this manual for details.

F-1 Altitude Vacuum Level Setting—3420

Using a water manometer with a pressure divider; or a pressure/vacuum gauge, part 5495384, measure the vacuum according to the decal on the transfer valve. If incorrect:
   a. 3420 Models 3 through 7:
      Check that the vacuum pump belt and transfer valve plug are set as shown in 08-410.
   b. 3420 Model 8 only:
      Adjust vacuum line restrictor to obtain vacuum shown in 08-410.

F-2 Regulator Air Pressure—3420

Check/adjust pressure as shown in 08-405.

F-3 Capstan—3420

Caution: Allow fiber optics lamp to warm up 20 to 30 minutes before making adjustments.

Do capstan tach adjustment. See 08-130 for models 3, 5, 7 or 08-120 for models 4, 6, 8.

F-4 Mechanical Skew—3420

a. Visually check tracking before adjusting the skew plate. Perform procedure on page 08-150 or 08-160.
   b. Check that mechanical skew meets the specifications given in 08-170 (1600 and 6250 bpi) or 08-180 (NRZI).

F-5 BOT/EOT—3420

Caution: Allow fiber optics lamp to warm up 20 to 30 minutes before making the adjustments.

Verify BOT/EOT adjustment. See 08-580.

F-6 Autocleaner Tape Direction—3420

Caution: Do not check autocleaner until tape unit has been positioned online, and just prior to returning machine to customer.

Check that autocleaner tape moves from bottom to top by marking tape and observing direction. See 08-380, "Autocleaner Operational Check".

F-7 ESD Grounding—3420 and 3803

Check that each door strike and roller assembly is adjusted correctly to ensure sufficient electro-static discharge (ESD) grounding.

   3420 lower rear door (1).
   3803 upper and lower on the front and rear doors (4).

This adjustment is accomplished as follows:
   a. With the screws loose, adjust the roller assembly so the door roller will latch on the strike plate.
   b. If necessary, adjust the plate mounted between the strike and frame to ensure proper grounding between the plate and finger stock assembly.

Note: Check that the door latching adjustment is still correct.

F-8 ESD Grounding—3803

a. Check the adjustment of the ESD plates on both the left and right sides. Be sure the plates are installed with the hem toward the inside of the machine.

Caution: Be sure that the plates are not adjusted to bow too much because the plates will reverse bow when the door is closed and lose proper grounding.

b. If necessary, adjust the plates so that each one bows out sufficiently to make contact with the hat section of the side cover.

c. Check the side door latch for a firm latching and adjust, if necessary.

F-9 Data Flow Clock Asymmetry Adjustment—3803

If the A1C2 card is replaced in the 3803, see ALD AA010 sheet 2 of 3, for adjustment procedure. (Originally factory adjusted.)
SECTION G. SYSTEM DIAGNOSTICS

Note: Make sure the write head card is seated properly before continuing.

G-1 Run 3420 OLTS A-K, M-X and AB through AG. (AB) through AG must be run under OLTSEP. AB is a diagnostic for 3803s with a device switching feature. AD through AG are optional for 3803s with the two-channel switch feature. (You must have a "dedicated" system to run diagnostics AB through AG.)

Note: OLT section 3420L will run only under sense switch setting (3420L/EXT=9). Verify PE clipping levels on machines with PE feature.

G-2 Verify serial numbers, EC levels, and features from the diagnostic printout.
   a. If the tape control information is incorrect, see plugging chart on 90-210, or AAO10 in the 3803 ALDs.
   b. If the tape unit information is incorrect, see plugging chart on 90-210, and 90-212 or A6106 in the 3420 ALDs.

G-3 When the diagnostics have run error free, generate and save for future use a read only tape in 6250 bpi mode.
   a. Enter the following as shown:
      `r 01;DEVICE/3420A-G/fe,ext=z/'
   b. To ensure that a good tape has been generated, the program must run without error. When a good tape has been generated, remove the write enable ring.
   c. Mark this reel 6250 bpi READ ONLY and save for diagnostic use with Section 00-010 of the MLMs.

Note: The CE should retain the output from Sections "V" and "W" of the OLTS which will give a printed table listing of all tape unit performance measurements.
SUBSYSTEM INSTALLATION (Cont'd)

SECTION G. SYSTEM DIAGNOSTICS (Cont’d)

G-4 Tape Control Serial Number/EC Level/Feature Code: Verify from diagnostic printout that factory plugging is correct when diagnostics are run.

Plugging example: tape control serial number is 10430, with 9-track feature.

Feature code tape control serial number

<table>
<thead>
<tr>
<th>Sense Byte 13</th>
<th>Card row</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Bit</td>
<td>Card Col.</td>
</tr>
<tr>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
</tr>
</tbody>
</table>

Tape control serial no.
Low order in hex

Sense Byte 14

<table>
<thead>
<tr>
<th>Sense Byte 14</th>
<th>Card row</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Bit</td>
<td>Card Col.</td>
</tr>
<tr>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
</tr>
</tbody>
</table>

When plugged, the columns will become either a one (1) or a zero (0).

Two channel switch, device switching, and EC level:

Purpose

<table>
<thead>
<tr>
<th>Sense Byte 17</th>
<th>Card row</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Bit</td>
<td>Card Col.</td>
</tr>
<tr>
<td>0</td>
<td>49</td>
</tr>
<tr>
<td>1</td>
<td>44</td>
</tr>
<tr>
<td>2</td>
<td>39</td>
</tr>
<tr>
<td>3</td>
<td>34</td>
</tr>
<tr>
<td>4</td>
<td>33</td>
</tr>
<tr>
<td>5</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>31</td>
</tr>
<tr>
<td>7</td>
<td>30</td>
</tr>
</tbody>
</table>

When plugged, the columns will become either a one (1) or a zero (0).
### SUBSYSTEM INSTALLATION (Cont'd)

#### SECTION G. SYSTEM DIAGNOSTICS

**Cont'd**

G-5  Tape Unit Serial Number/Model Number/EC Level/ Feature Code. Verify from diagnostic printout that factory plugging is correct on all tape units when diagnostics are run (3420) ALD A6106.

<table>
<thead>
<tr>
<th>Tape Model</th>
<th>Alpha</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model 3</td>
<td>A, B, P</td>
</tr>
<tr>
<td>Model 5</td>
<td>C, D, Q</td>
</tr>
<tr>
<td>Model 7</td>
<td>E, F, R</td>
</tr>
<tr>
<td>Model 4</td>
<td>G, H, S</td>
</tr>
<tr>
<td>Model 6</td>
<td>I, K, T</td>
</tr>
<tr>
<td>Model 8</td>
<td>M, N, U</td>
</tr>
</tbody>
</table>

**Notes:**

1. The original model number is the high-order digit or alpha character in the serial number, and is not changed with model conversion. See table to convert alpha to model type.

2. For tape units with a high order digit in the serial number, other than 3 through 8; the diagnostic will print the original model number as the high order digit of the serial number.

---

**International Corporation 1976, 1979, 1980**

**Card**

**Model**

**Copyright**

**Notes:**

- The original model number is the high-order digit or alpha character in the serial number, and is not changed with model conversion.

---

**System Diagnostics**

**Level/ Feature Code:** Verify from diagnostic printout that factory plugging is correct on all tape units when diagnostics are run (3420) ALD A6106.

**International Corporation 1976, 1979, 1980**

**Card**

**Model**

**Copyright**
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