User's Guide

HP Debug User Interface

for SH7020/30 Series

Printing History

New editions are complete revisions of the manual. The date on the title page changes only when a new edition is published.

A software code may be printed before the date; this indicates the version level of the software product at the time the manual was issued. Many product updates and fixes do not require manual changes, and manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual revisions.

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Alternating current.

Direct current.

On (Supply).

Off (Supply).

Frame (or chassis) terminal. A connection to the frame (chassis) of the equipment which normally include all exposed metal structures.

Warning

This Warning sign denotes a hazard. It calls your attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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This Caution sign denotes a hazard. It calls your attention to a operating procedure, practice, condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note

Note denotes important information. It calls attention to a procedure, practice, condition or the like, which is essential to highlight.

In This Book

The HP B3754A Debug User Interface, which is used with the HP 64785A/B Emulator, is a high-level language debugger for the Hitachi SH7020/30 Series.

This book describes processor-specific functions and usage of the HP B3754A Debug User Interface.

For common functions and usage of the HP Debug User Interface, refer to the *HP Debug User Interface User's Guide*.

For installation of the HP Debug User Interface, refer to the *HP Debug User Interface Installation Guide*.

For installation of the HP 64785A/B Emulator, refer to the *HP 64785 SH-7000 Emulator Terminal Interface User's Guide*.

Note

Contents

Contents

1

Connecting the Target System

Connecting the Target System

This chapter shows you how to connect the emulator to your target system.

Overview

To connect the HP 64785A/B Emulator and the target system, the **QFP cable** and the **QFP socket/adapter** (attached to the QFP cable products) are used.

Caution

To prevent the emulator and the target system from being damaged, be sure to follow the cautions below when handling them.

*   **To prevent damage by static discharge, use the emulator in a place resistant to static electricity.**

*   **Be sure to turn off the emulator and the target system before connecting them.**

*   **Be sure that orientation of each connector is right.**

*   **Check that the ground line of the emulator and that of the target system are properly connected.**

*   **When turning the system on, switch on the target system first and then the emulator.**

*   **When turning the system off, switch off the emulator first then the target system.**

The **QFP cable** is a cable assembly to connect the PGA adapter to the QFP socket/adapter on the target system. Use one of the following QFP cables.

Table 1-1. Supported Processors of Each QFP Cable

Processor	Package (Pitch)	QFP Cable
SH7032/34	QFP-112 (.65 mm)	**HP 64785C**
SH7020/21	TQFP-100 (.5 mm)	**HP 64785D**

The **QFP socket/adapter** is a part to adapt the the QFP cable to the target system. You must solder this part to your target system. The QFP socket/adapter can be used as a "socket" to mount a real processor. The following QFP socket/adapters are provided.

Table 1-2. QFP Socket/Adapters

Processor	Package (Pitch)	QFP Socket/Adapter
SH7032/34	QFP-112 (.65 mm)	**HP 64785-61620**
SH7020/21	TQFP-100 (.5 mm)	**HP 64785-61621**

To connect the target system,

1 Verify both the emulator and the target system are turned off.

2 Solder the QFP socket/adapter to the target system.

3 Attach the QFP cable to the emulation probe.

4 Align pin #1 of the QFP cable and the QFP socket/adapter, then fix them with four screws.

5 Turn on the target system and then the emulator.

Caution

Do not apply excessive force to the QFP cable. It may cause damage to the QFP cable, the QFP socket/adapter and the target system.
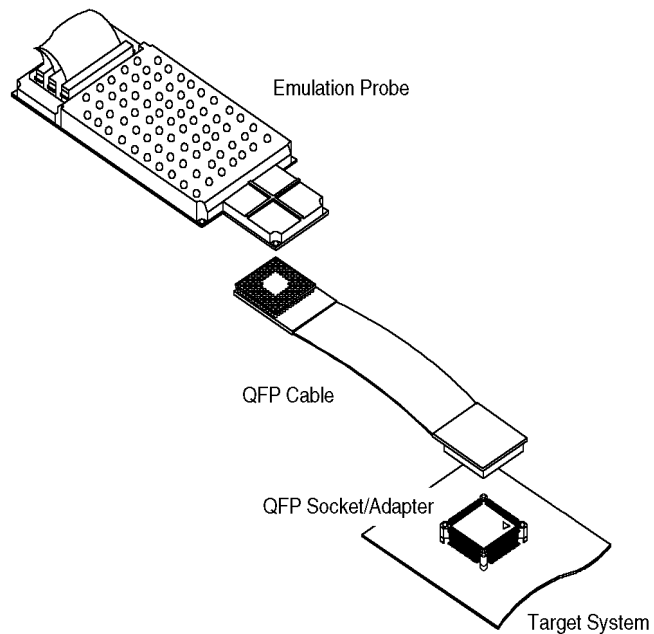
Figure 1-1. Connecting the Target System

Note

2

Configuring the Emulator

Configuring the Emulator

This chapter shows you how to set the following items to configure the emulator.

- Hardware Options

- Memory Map

Hardware Options

The emulator can be configured to suit developments of various target systems and user programs by setting the hardware options.
The HP 64785A/B Emulator has the following hardware options.

- **Memory Type of Area 1**

- **PA8/BREQ Pin Function**

- **Restrict to Real Time**

- **Set Breakpoints at Delay Slot**

- **Quick-Break Mode**

- **Break on Write to ROM**

- **Processor Type**

- **Processor Operation Mode**

- **Stack Pointer Reset Value**

Note

When using the analyzer boards **HP 64704A**, setting the trace clock speed is also required.
Refer to "Trace Clock Speed" in Chapter 5.

Setting the Hardware Options

To set the hardware options,

1 Choose **Settings→Configuration→Hardware...** (Alt, S, C, H) from the control menu of the Debug window.

2 Set the hardware options using the Emulator Configuration dialog box.

3 Click the OK button.

Note   Set the hardware options prior to setting the memory map.

Note   In the Emulator Configuration dialog box, the option button checked means **Yes**, the option button not checked means **No**.

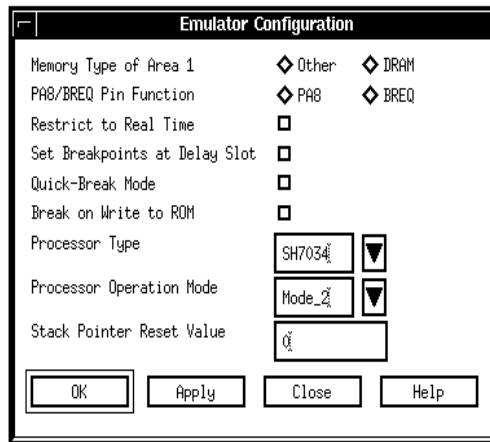**Note**   Setting the hardware options will drive the emulator into a reset state.

Figure 2-1. Emulator Configuration Dialog Box

Memory Type of Area 1

This option allows you to select the memory type of area 1.

Other   Select this option when using area 1 as the external
               memory space or not using it at all.

               The emulator uses area 1 as 4M bytes space.

DRAM   Select this option when using area 1 as DRAM space.

               The emulator uses area 1 as 16M byte space.

Note   This option is set to control the operation of the emulator when it accesses
               area 1.

               Note that it does not set the DRAM enable bit (DRAME) in the bus control
               register (BCR). Set the DRAME with the user program or manually, in the
               same manner for other registers.

PA8/BREQ Pin Function

This option allows you to select the function of the PA8/$\overline{\text{BREQ}}$ pin.

PA8   Select this option when the PA8/$\overline{\text{BREQ}}$ pin is used as PA8
               input/output or is not used in your target system.

BREQ   Select this option when the PA8/$\overline{\text{BREQ}}$ pin is used as bus
               request ($\overline{\text{BREQ}}$) input in your target system.

Note   This option is set to control the operation of the emulator in a bus-released
               state.

               Note that it does not set the PA8 mode bit (PA8MD) in the port A control
               register 1 (PACR1). Set the PA8MD with user programs or manually, in the
               same manner for other registers.

Restrict to Real Time

The emulator has to break to the monitor to access processor registers and target memory. While running the user program, this break is done implicitly and called "temporary break".

With temporary breaks, the user program cannot be executed in real time. This may cause unexpected result if your target system circuitry is dependent on constant execution time of the program code.

This option allows you to select whether the emulator is restricted to real-time runs.

Yes   The emulator is restricted to real-time runs.

While running the user program, all commands that cause a temporary break are refused. The user program is guaranteed to be executed in real time.

Commands to display/modify registers and target memory are not allowed when the emulator is running the user program. However, you can still execute the run control commands such as reset, break, run, step.

No   The emulator is not restricted to real-time runs.

All commands, regardless of whether or not they require a break to the monitor, are accepted by the emulator.

Set Breakpoints at Delay Slot

A breakpoint at delay slot causes slot invalid instruction exception when it is hit during user program execution.

This option allows you to allow/prohibit setting a breakpoint at delay slot.

Yes   Allows you to set a breakpoint at delay slot.

No   Prohibits you from setting a breakpoint at delay slot. Normally, select this option.

When setting a breakpoint at delay slot is prohibited, the emulator checks if the instruction before the requested breakpoint address is a delayed branch or not. For a delayed branch, the emulator will not set the breakpoint, recognizing it an invalid setting.

Note that it cannot be evaluated if the code checked is an instruction or data. Therefore, if data immediately in front of the requested breakpoint address is the same code as a delayed branch, setting a breakpoint will fail. In such cases, select **Yes**.

Quick-Break Mode

This option allows you to select whether the emulator does "quick" temporary break to access processor registers and target memory while running the user program.

Yes   Quick-break is used for a temporary break to the monitor.

Monitor execution period in the quick-break mode is shortened to several tens of microseconds or several hundred microseconds, while that in the normal break mode is several milliseconds or several tens of milliseconds.

While running the monitor, the emulator responds to no interrupts. Try this setting to eliminate a problem caused by interrupt response time during program execution.

No   Quick-break is not used for a temporary break to the monitor.

Note   While running the monitor, the emulator responds to no interrupts.
The emulator suspends interrupt requests in the monitor; the requests will be serviced upon return to the user program.

Break on Write to ROM

This option allows you to select whether the emulator breaks to the monitor when the user program writes to a memory area mapped as on-chip ROM or ROM.

Yes   The emulator breaks to the monitor when the user program writes to a memory area mapped as on-chip ROM or ROM.

No   The emulator does not break to the monitor upon a write to ROM.

Processor Type

This option allows you to select the emulation processor.

SH7032   The emulator emulates the SH7032.

SH7034   The emulator emulates the SH7034.

SH7020   The emulator emulates the SH7020.

SH7021   The emulator emulates the SH7021.

Processor Operation Mode

This option allows you to select the processor operation mode.

Mode_0   The emulator operates in mode 0.

Mode_1   The emulator operates in mode 1.

Mode_2   The emulator operates in mode 2.

Note   The user program cannot be executed if this setting and the MD2 to MD0 states in the target system does not correspond.

Stack Pointer Reset Value

This option allows you to specify the value that the stack pointer (SP, R15) is set to when the monitor is entered after emulation reset.

The stack pointer must be set to a 32-bit address and take a value multiple of 4. Normally, specify the default value of the user program.

Memory Map

The HP 64785A/B Emulator memory mapper allows you to define up to 16 different map terms. The minimum size of each map term is 16k bytes. You can specify one of the following memory types to each map term.

eram   Emulation RAM.

   This area operates as read/write emulation memory.

erom   Emulation ROM.

   This area operates as read only emulation memory. When the user program writes to this area, the data is not written. And, you can configure the emulator to break to the monitor at an attempted write to this area.

tram   Target RAM.

   This area operates as read/write target memory.

trom   Target ROM.

   This area operates as read only target memory. You can configure the emulator to break to the monitor when the user program writes to this area.

grd   Guarded memory.

   This area operates as an access-prohibited area. When the user program attempts to access to this area, the emulator breaks to the monitor. Access with emulator commands are also prohibited.

The memory type of other area (area of no map terms defined) can be defaulted to **tram** or **trom**.

Note   When $\overline{\text{BREQ}}$ is used in the target system operating with the clock faster than **16.6 MHz**, one state access to the emulation memory is not allowed.

Note

When the **HP 64173A** 4 Mbyte memory module is used in the target system operating with the clock faster than **16.6 MHz**, one state access and DRAM short pitch access are not allowed.

Note

The emulation memory has no parity bits.

Parity is generated and checked for the parity bits of the target system, even when accessing the emulation memory.

Note

The target system cannot perform direct memory access to the emulation memory.

Note

Single address mode transfer to the emulation memory by internal DMAC is not allowed.
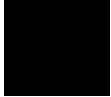
Setting the Memory Map

To set the memory map,

1 Choose **Settings→Configuration→Memory Map...** (Alt, S, C, M) from the control menu of the Debug window.

2 Set the memory map using the Memory Map dialog box.

- **Setting a map term**

    1. Specify an area to the Address Range text box.

    Format: *<start address>..<end address>*

    2. Select a memory type in the Attribute option box.
    3. Click the Apply button.

- **Deleting a map term**

    1. Select a map term in the Map Term list box.
    2. Click the Delete button.

- **Deleting all map terms**

    1. Click the Del.All button.

- **Setting a memory type of other area**

    1. Select a memory type in the Other option box.

3 Click the Close button.

Note   Set the hardware options prior to setting the memory map.

Note   Map terms cannot be set crossing area and/or shadow boundaries.

Note   Setting the memory map will drive the emulator into a reset state.
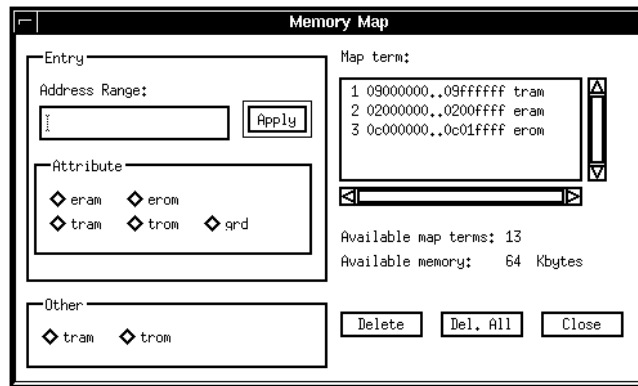
Figure 2-2. Memory Map Dialog Box

On-Chip ROM

The on-chip ROM is mapped automatically as the memory dedicated for the on-chip ROM regardless of the memory map settings. Mapping to this area will result in an error.

When the user program attempts to write to addresses mapped as on-chip ROM, data will be protected. Also, you can set the emulator to break to the monitor upon a write to this area by the user program.

On-Chip RAM

The on-chip RAM is mapped automatically as the memory dedicated for the on-chip RAM regardless of the memory map settings. Mapping to this area will result in an error.

On-Chip Peripheral Module Registers

The on-chip peripheral module registers work as the on-chip peripheral module registers regardless of the memory map settings. You don't have to map this area. Mapping to this area will result in an error.

Address/Data Multiplexed I/O Space

Address/data multiplexed I/O space is always accessed as target RAM regardless of the memory map settings.

Configuration Commands

You can also configure the emulator by configuration files or command files. The HP B3754A Debug User Interface has the following configuration commands. Case is not significant in both commands and parameters.

Note

The hardware option commands should appear followed by the memory map commands.

Note

The hardware option commands and the memory map commands must be placed between its own start and end commands.

Table 2-1. Configuration Commands

Command	Parameter 1	Parameter 2	Operation
config	start		Start of Hardware Option Commands
config	area1	dram | other	Memory Type of Area 1
config	breq	enable | disable	P8/BREQ Pin Function
config	rrt	enable | disable	Restrict to Real Time
config	bpds	enable | disable	Set Breakpoints at Delay Slot
config	qbrk	enable | disable	Quick-Break Mode
config	rombreak	enable | disable	Break on Write to ROM
config	chip	*<processor type>*	Processor Type
config	mode	*<mode number>*	Processor Operation Mode
config	rsp	*<sp value>*	Stack Pointer Reset Value
config	end		End of Hardware Option Commands
map	start		Start of Memory Map Commands
map	*<map range>*	*<memory type>*	Setting Map Term
map	other	*<memory type>*	Setting Memory Type of Other Area
map	end		End of Memory Map Commands

enable | disable   Specify **enable** when **Yes**, **disable** when **No**.

<processor type> Specify one of the following emulation processors.

- **SH7032**
- **SH7034**
- **SH7020**
- **SH7021**

<mode number> Specify a number from **0** to **2** for the processor operation mode.

<sp value> Specify a 32-bit address which takes a value multiple of 4. Normally, specify the default value of the user program.

<map range> Specify an area to be mapped.

  Format: *<start address>..<end address>*

<memory type> Specify one of the following memory types.

- **eram**
- **erom**
- **tram**
- **trom**
- **grd**

For a memory type of other area, **eram**, **erom** and **grd** cannot be specified.

```
# Configuration File

# Hardware Options
config start
config area1 dram
config bpds disable
config breq disable
config chip SH7034
config mode 2
config qbrk enable
config rrt disable
config rsp 0
config rombreak enable
config end

# Memory Map
map start
map 09000000..09ffffff tram
map 02000000..0200ffff eram
map 0c000000..0c01ffff erom
map other tram
map end
```
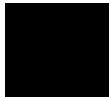
Figure 2-3. Configuration File Example

3

Language Tools

Language Tools

This chapter describes language tools which can be used with the HP B3754A Debug User Interface.

Hitachi Language Tools

The HP B3754A Debug User Interface can debug user programs created with the following Hitachi language tools.

Table 3-1. Hitachi Language Tools

Tool	Command	Description
C Compiler	**shc**	SH Series C Compiler
Assembler	**asmsh**	SH Series Assembler
Linker	**lnk**	H Series Linkage Editor

For version numbers of language tools supported by the HP B3754A Debug User Interface, contact your nearest HP support office.

Command Options

This section describes important command options when using the Hitachi language tools.

C Compiler

–debug   Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

Assembler

–debug   Generates debug information.
You must always specify this option. Modules without debug information cannot be debugged.

Linker

–debug   Generates debug information.
You must always specify this option. Programs without debug information cannot be debugged.

Note

4

Emulation Status

Emulation Status

This chapter describes the emulation status messages which are displayed in the Debug window.

An emulation status message is displayed in the Debug window.
The HP B3754A Debug User Interface has the following emulation status
messages.

- **Emulation reset**

  The emulator is resetting the processor.

  The resetting procedure falls into two categories;power-on reset when
  the NMI of the target system is High, manual reset when Low.

- **Running in monitor**

  The emulator is executing the monitor.

- **Running user program**

  The emulator is executing the user program.

- **Awaiting target reset**

  The emulator is awaiting a reset signal from the target system.

  When a "run from reset" command is executed, the emulator enters this
  state. During this state, the emulator cannot break to the monitor.

- **Target reset**

  The target system is resetting the processor.

  When the emulator accepts the $\overline{\text{RES}}$ signal from the target system while
  running the user program, the emulator enters this state. During this
  state, the emulator cannot break to the monitor.

- **Bus grant**

  A bus-released state.

  When the emulator accepts the $\overline{\text{BREQ}}$ signal from the target system, the
  emulator enters this state.

- **Sleep**

  Sleep mode.

  Sleep mode is cleared when the emulator breaks to the monitor. When
  entering the monitor from sleep mode, the program counter (PC) points
  to the next instruction from the SLEEP instruction.

- **Standby**

  Standby mode.

  Standby mode is cleared when the emulator breaks to the monitor. When entering the monitor from software standby mode, the program counter (PC) points to the next instruction from the SLEEP instruction.

- **No target power**

  The target system's power is off.

- **Slow clock**

  The processor's clock is abnormally slow or stopped.

  A broken-down clock on the target system may cause this state.

- **Unknown state**

  An abnormal state.

  The emulator also enters this state when the $\overline{\text{WAIT}}$ signal from the target system is left asserted.
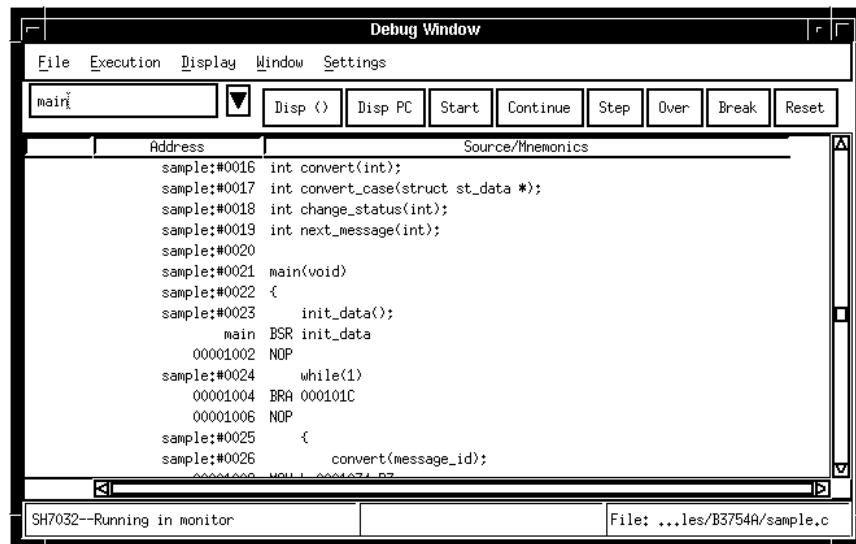

Figure 4-1. Debug Window

5

Trace

Trace

This chapter describes trace functions specific to the HP B3754A Debug User Interface.

Trace Clock Speed

When using the analyzer board **HP 64704A**, setting the trace clock speed.

Incorrect setting of the trace clock speed will result in improper tracing. The analysis capability of time and state count depends on this setting.

To set the trace clock speed, choose **Settings→Trace Clock Speed→** (Alt, S, S,) from the control menu of the Trace window.

Very Fast (V)   This setting is not used for the HP B3754A Debug User Interface. Do not select this setting.

Fast (F)   Select this setting when the processor's clock speed is greater than **16.6 MHz**.

Only counting state is available.

Slow (S)   Select this setting when the processor's clock speed is less than **16.6 MHz**.

Both state or time counting are available.

The analyzer boards **HP 64794A/C/D** have no trace clock speed setting.

Data and Status Conditions

This section describes the data and status conditions in the following dialog boxes of the HP B3754A Debug User Interface.

• Trace Trigger Store Condition dialog box.

• Trace Pattern dialog box of sequential trace.

Data Condition

The data bus to the emulation analyzer is 32-bit width. You should consider which of four byte data is valid when setting the data condition.

Bus width, access size, and address determine the valid byte data among the four, as shown in the following table. Use "**x**" for invalid byte data to set the data condition.

Table 5-1. Data Condition Settings

| Area | Bus Width | Access Size | Address | Upper Word | | Lower Word | | Example |
				Upper Byte	Lower Byte	Upper Byte	Lower Byte	
On-Chip ROM On-Chip RAM	32-Bit	Byte	4n	Valid	-	-	-	**0a1xxxxxx**
			4n+1	-	Valid	-	-	**0xxb2xxxx**
			4n+2	-	-	Valid	-	**0xxxxc3xx**
			4n+3	-	-	-	Valid	**0xxxxxxd4**
		Word	4n	Valid	Valid	-	-	**0a1b2xxxx**
			4n+2	-	-	Valid	Valid	**0xxxxc3d4**
		Long Word	4n	Valid	Valid	Valid	Valid	**0a1b2c3d4**

Table 5-1. Data Condition Settings (Continued)

| Area | Bus Width | Access Size | Address | Upper Word | | Lower Word | | Example |
				Upper Byte	Lower Byte	Upper Byte	Lower Byte	
External Memory	8-Bit	Byte	n	-	-	-	Valid	`0xxxxxxa1`
		Word	2n (1st)	-	-	-	Valid	`0xxxxxxa1`
			2n+1 (2nd)	-	-	-	Valid	`0xxxxxxb2`
		Long Word	4n (1st)	-	-	-	Valid	`0xxxxxxa1`
			4n+1 (2nd)	-	-	-	Valid	`0xxxxxxb2`
			4n+2 (3rd)	-	-	-	Valid	`0xxxxxxc3`
			4n+3 (4th)	-	-	-	Valid	`0xxxxxxd4`
	16-Bit	Byte	2n	-	-	Valid	-	`0xxxxa1xx`
			2n+1	-	-	-	Valid	`0xxxxxxb2`
		Word	2n	-	-	Valid	Valid	`0xxxxa1b2`
		Long Word	4n (1st)	-	-	Valid	Valid	`0xxxxa1b2`
			4n+2(2nd)	-	-	Valid	Valid	`0xxxxc3d4`
On-Chip Peripheral Module Registers	8-Bit	Byte	n	-	-	-	Valid	`0xxxxxxa1`
		Word	2n (1st)	-	-	-	Valid	`0xxxxxxa1`
			2n+1 (2nd)	-	-	-	Valid	`0xxxxxxb2`
	16-Bit	Byte	2n	-	-	Valid	-	`0xxxxa1xx`
			2n+1	-	-	-	Valid	`0xxxxxxb2`
		Word	2n	-	-	Valid	Valid	`0xxxxa1b2`
		Long Word	4n (1st)	-	-	Valid	Valid	`0xxxxa1b2`
			4n+2 (2nd)	-	-	Valid	Valid	`0xxxxc3d4`

Status Condition

You can specify the following items as the status condition.

fetch	Instruction fetch cycle.
data	Data access cycle.
read	Read cycle.
write	Write cycle.
byte	Byte access cycle.
word	Word access cycle.
long	Long word access cycle.
cpu	CPU cycle.
dma	DMA controller (DMAC) cycle.
intack	Interrupt acknowledge cycle. When the emulator breaks to the monitor, an interrupt acknowledge cycle may also happens.
refresh	Refresh cycle.
wrrom	Write cycle to an area mapped as on-chip ROM or ROM.
grd	Access cycle to an area mapped as guarded memory.
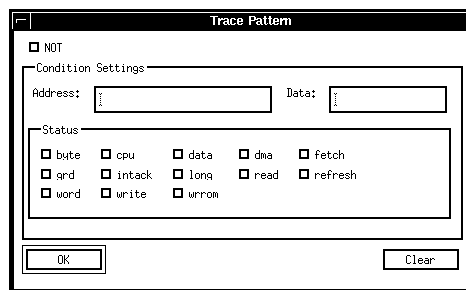
Figure 5-1. Trace Pattern Dialog Box

6

Windows

Windows
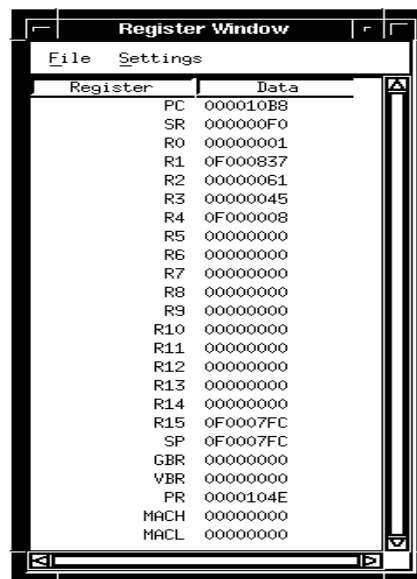
This chapter describes windows specific to the HP B3754A Debug User Interface.

Register Window

In the Register window of the HP B3754A Debug User Interface, the internal registers of the CPU can be displayed and modified.

- Program Counter (PC)

- Status Register (SR)

- General Registers (R0 to R15)

- Stack Pointer (SP)

- Global Base Register (GBR)

- Vector Base Register (VBR)

- Procedure Register (PR)

- Multiply-Accumulate Registers (MACH, MACL)

```
┌─────────────────────────────────────┐
│          Register Window             │
├─────────────────────────────────────┤
│  File   Settings                     │
├─────────────────────────────────────┤
│    Register    │    Data             │
│           PC   000010B8              │
│           SR   000000F0              │
│           R0   00000001              │
│           R1   0F000837              │
│           R2   00000061              │
│           R3   00000045              │
│           R4   0F000008              │
│           R5   00000000              │
│           R6   00000000              │
│           R7   00000000              │
│           R8   00000000              │
│           R9   00000000              │
│          R10   00000000              │
│          R11   00000000              │
│          R12   00000000              │
│          R13   00000000              │
│          R14   00000000              │
│          R15   0F0007FC              │
│           SP   0F0007FC              │
│          GBR   00000000              │
│          VBR   00000000              │
│           PR   0000104E              │
│         MACH   00000000              │
│         MACL   00000000              │
└─────────────────────────────────────┘
```

Figure 6-1. Register Window

Peripheral Window

In the Peripheral window of the HP B3754A Debug User Interface, all registers of the following on-chip peripheral modules can be displayed and modified.

- Interrupt Controller (INTC)

- User Break Controller (UBC)

- Bus State Controller (BSC)

- DMA Controller (DMAC)

- 16-Bit Integrated Timer Pulse Unit (ITU)

- Programmable Timing Pattern Controller (TPC)

- Watchdog Timer (WDT)

- Serial Communication Interface (SCI)

- A/D Converter

- Pin Function Controller (PFC)

- I/O Ports

- System Control Registers
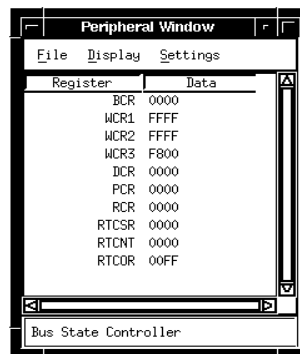
Figure 6-2. Peripheral Window

7

Restrictions and Limitations

Restrictions and Limitations

This chapter describes restrictions and limitations.

The HP B3754A Debug User Interface and the HP 64785A/B Emulator have
the following restrictions and limitations.

- **One state access**

  When $\overline{\text{BREQ}}$ is used in the target system operating with the clock, faster
  than **16.6 MHz**, one state access to the emulation memory is not allowed.

- **Memory module**

  When the **HP 64173A** 4 Mbyte memory module is used in the target
  system operating with the clock faster than 16.6 MHz, one state access
  and DRAM short pitch access are not allowed.

- **Parity bit**

  The emulation memory has no parity bits.

  Parity is generated and checked for the parity bits of the target system,
  even when accessing the emulation memory.

- **Direct Memory Access**

  The target system cannot perform direct memory access to the
  emulation memory.

- **Single address mode transfer**

  Single address mode transfer to the emulation memory by internal DMAC
  is not allowed.

- **Warp mode**

  HP 64785A/B emulator does not support warp mode, that is, setting the
  warp mode bit (WARP) in the bus control register (BCR) does not drive
  the emulator into the warp mode.

- **Reset Output**

  The emulator ignores the $\overline{\text{RES}}$ signal from the target system.

- **Interrupts**

  While running the monitor, the emulator responds to no interrupts.

  The emulator suspends interrupt requests in the monitor; the requests
  will be serviced upon return to the user program.
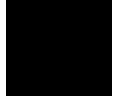
- **Watchdog Timer**

  When entering the monitor, the watchdog timer (WDT) stops counting regardless of its mode, watchdog or interval. And, it resumes counting upon return to the user program.

- **Sleep and Standby Modes**

  Sleep and standby modes are cleared when the emulator breaks to the monitor.

  When entering the monitor, the program counter (PC) points to the next of the SLEEP instruction.

Index

Index