FIRST AID KIT
for
LINE GENERATOR
BY
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MEMO

DATE: October 23, 1972

TO: Whom it may concern

FROM: Mho

SUBJECT: First Aid Kit for LG or What to do until Cheadle comes

A copy of the test procedure for the Line Generator is available to all interested parties from the Engineering file.

This procedure is written in the form of if... then... and has been used by the test department for system test. The procedure is not complete and the idea is to complete it as time goes by and more systems get tested.

As it stands, however, it may be helpful to anybody who happens to have a problem with the Line Generator. Any suggestions regarding this document should be directed to Test department.

Thanks

Mho
ACCEPTANCE

The Line Generator should not be accepted to test unless the following are checked.

1) Power Supplies

Three power supplies are used in the linear (analog) portion of the LG. The LG cannot share these supplies with any other device.

These power supplies must be checked before installation and must have acceptance tags.

**Do not begin test without being sure that the supplies have been tested.

Check the following for possible error:

Quiet VCC ( +5 volts )
Uses blue and black twisted pair to the back pannel. Blue =+5 if black=ground.

+,-15 Volts
Uses purple/black; red/black twisted pairs.
red=+15, black=ground, purple=-15.

-6Ø volts
Uses orange/black twisted pair
orange=-6Ø, black=ground.

These wires should be connected to the back pannel according to the printed circuit writings.

In addition to these another power supply is used for the digital portion of the system that is connected to the conventional place on the cage.

2) The Cards

The system uses the following boards.

Assy# Quan.
108109 1
109114 1
108103 (2)
Assy#       Quan.
1Ø81Ø4      1
1Ø8115      1
1Ø81Ø7      1
1Ø811ø      (2)
1Ø81ø8      1
1Ø8113 or A 1Ø8114

A pattern generator may take the place of a cable.

There are also four metal shields that are quite sacred and
should be in their respective position or Allah
will mess up the system.

The print on the next page (1Ø81Ø1 - 6Ø1) shows the card
layout. Note that slot 17 is occupied by one of
these shields. Slot 17 would normally be "Scope
1" to the conventional line generators. This is our nice
way of saying that the conventional line generators (as
they leave E & S) do not have a "Scope 1" to the programmers.
TEST PROCEDURE

During the test of LG any time there is a need for pulling out or inserting a card power should be turned off. Let us say this applies to analog and digital boards for a few reasons.

1) Power Up

Powering up is mainly making sure that all voltages are

***************OF THE CORRECT POLARITY***************

AND VALUE.

A) Without the cards plugged in

Adjust all voltages to .01 volts (for now) for ground use the ground on the back pannel where all analog grounds meet as referance for analog voltages and the digital ground for +5 digital v. <sup>5</sup> 1/2 AT R, S. (V,A)

B) Turn power off and plug in the following boards

Pattern generator or cable from the clipper.
Control 1Ø81Ø9
Sw. light 1Ø9114
X and Y Digital 1Ø81Ø3
Z Digital 1Ø81Ø4

Put the DVM probes on the digital V and power up. If the voltage has dropped more than .3 volts you have got problems. See Note 1

C) Turn off power and plug in the ramp card 1Ø81Ø8
This time check + or - 15 volt line. If those are OK check quiet VCC.

D) Turn off power and plug in scope select 1Ø8115
this fellow uses + -15, and digital VCC.

E) Before inserting the D/A converters use an ohmmeter to check the Ohmic resistance between analog ground and the -6ØV strip on each D/A card. This needs to be done only the first time the board is being tested or if a component has been replaced.

The following table is a list of resistances for a typical board.
-60V. - Analog ground  200K
A. ground - -60V.  100ohms

-Ref. ground  Short either way

-25 - ground  1 MEG
Ground - -25  20 OHMS
+ and -15 - A. ground  200K
1-Alpha and alpha ramps have very little resistance to ground.

After plugging these boards in try all the voltages. The levels should not be less than .3 volts different from original settings.

F) With all the cards plugged in adjust all voltages to the nominal levels (+ or -.01 volts or less)

**NOTE: 1.**

If at any time during test of the line generator a voltage is shorted due to a board stop test and find the short. Do not take chances because many problems may be caused. Note that the problem may not be on the board.

2) Adjusting the ramp card

Check this card for the following wrong polarity capacitors
There must be at least 12 of these. If you could not find any backwards capacitors let someone else look for them.
If there is a capacitor in backwards and the system is turned on for any appreciable amount of time the opamp associated with the capacitor may stop to serve.

The next two sheets are schematic of the ramp card
108108-605
Four Opamps need to be zeroed out (input offset set to zero)

These four are

(Page 1) D1 and D2

(Page 2) D6 and D7

All except D1 can be adjusted by shorting the input through the output** and adjusting the output to less than .2 mvolts of its respective ground.

D1 is a follower and should be adjusted by grounding the +input and setting the output to zero

** note that in setting the offset for D6 the input compensation network (IE 30K and 10 PF) must be considered a part of the Opamp.

****** If you cannot zero any one opamp for any reason there may be one of the following reasons

Bad Pot
Wrong value pot
Pot leads not soldered
Amp leads not soldered
Bad Amp
Amp Oscilating
If the last one is the case you are in trouble.
Check the frequency of oscillation and if it is high (around 10 MHZ) chances are a small capacitor at the output will help out. (See note 2)
At any rate this is really the classic case of Engineer vs. unstability.

**Note 2**

If the frequency of oscillation is too high chances are that the wire that is being used as a short is too long. To verify this you can put a 100PF capacitor in parallel with the short and see if the oscillation stops. If this is the case zero the opamp and don't worry anymore. Ever.

3) Testing the control sequence.

** For this part of the test only, the following cards are not needed

Scope select
X,Y, and X D/A
Scope Driver
To start the test input a pattern that is fairly simple.

Preferably a move draw command. Note the following.

The LG is never used in relative mode and therefore the REL light must be off. If it is not refer to cable pin 96 (absolute 1.96) or the control card (sheet 5 of 108109-601/605 B2).

Try to stay away from dash, center, or timed modes at this stage they will just add to the confusion.

The drawing on the next page (108114=101 S1) (This will be refered to as the maintenance pannel in this write up) Shows the lights and their respective names.

For this part of the test the system should be put in single step and no overlap mode.

A reset should put us in wait state.

The system must single step through as shown in the state chart.

The control card only receives a flag from the cable and two flags from the ramp card (pages 1 and 4 of 108109-601). As a result if it does not leave wait state or not return to it chances are that the other guys are not flagging.

A case where 32 or 33 on the back pannel are held low is shown.

** It is adviseable to check the values of R & C's on the control card against the guzzinta before test.
NOTES:
2. INSTALL WHITE PLASTIC SLEEVES ON ALL TOGGLE SWITCHES.
3. INSTALL RED PLASTIC SLEEVE ON THE PUSHBUTTON SWITCH.
Sequence: No Overlap

<table>
<thead>
<tr>
<th>State</th>
<th>Wait 1</th>
<th>state 2</th>
<th>state 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Settled</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Input</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Flag 1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Wait 2</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Flag 2</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Wait 3</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Flag 3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Analog Wait</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
After state 3 the control card is expecting two signals
from the ramp card. These signals are (alpha 1 or alpha 0)
If one of these signals is not coming through the machine
will go into some undefined state. To verify that the
problem is coming from the ramp card you can unseat it and
try to single step the line generator. If it goes through
its states the problem is in the ramp card otherwise you have
to check the control card.

4) Testing the ramp

The cards X, Y, and Z digital go through card test and
it is safe to believe that they are OK. (During the system
test)

The ramp card generates the ramp according to the size
of the SM and LA numbers. (Sheet 1 of 18818-605)

A few words should be said about the operation of this card
since it is the heart of the system.

The A/D converter on Page 1 is really a D/A.
The operation is simple. There will be current
flowing through the diodes into the opamp except
for when the input to the corresponding inverter
is holding the anode side of the diode low.

A 1K pot is put in series with the 2.7K resistor at the
input of D2. This will change the offset level
of D2 in order to get the two ramps exactly
equal. The pattern on the next page is a demo of
where this can be adjusted. Note that the dashed
lines are drawn on alternate cycles (odd, even)
** Note that the +ref is the output of an inverter that changes the polarity of -ref. This inverter is supplied with a trim pot (R85 1Ø81Ø8-6Ø1 sheet 2). This pot can be used to further equalize the ramps. It could be adjusted best using the pattern shown on the next page.
CORRECT

+ REF. NOT
ADJUSTED
If this level is not quite right the difference between the two ramps will be observed in a group of lines that are drawn from (to) a single point.

**Note that the two TIS75 fets never get switched because the system is never used in timed mode.**
The multiplying D/A converter on sheet 2 of 108108-605 is a little more elaborate. The two 73's are used to enable or inhibit I/L or -1/L signals into the D/A. These fets are used because of their low on resistance. They should however, turn off at about the same voltage. If the off voltages are drastically different the ramps may or may not show a difference but the lines will.

Alpha Ramp must go from .7 volts to -5.7 volts. If the limits of the ramp are not close to these numbers the 1-alpha ramp will be offset in the other direction. If this is the case check the two transistors. (2N697 and 2N1131 @75)

The LM304 and its driver the 2N2905 are fairly good friends they live together and burn together. As a result if -ref is not holding steady it is not wise to change only one of the two.

** The RC network going from alpha to (1-alpha) ramps (108108-601 sheet 2 D-1) is a fix.
The test engineer is allowed to change the values of 220 ohms and 100 PF to some other values if the finds necessary.

** The test engineer is also allowed to put a lead network on the (1-alpha) amp by putting a 7.5 capacitor across R67.
The effect of this capacitor will become observable in a star pattern.
5) Testing the D/A's

The X and Y D/A's (1Ø811Ø) accept 12 pairs of bits and output an analog signal that is between Ø and -1Ø volts.

There are also two deglitching signals that are used to keep the output quiet while the numbers are changing size (such as a transition from A 3 to 4 or 7 to 8 etc.)

Two voltage levels are generated on each card (+4.3 and -25 volts). It is advisable that these levels are checked before the test begins.

Four analog signals are introduced to the card (alpha, 1-alpha ramps; -ref and analog ground). It is important to make sure that the D/A is not loading any one of these signals.

** It is advisable that the 1-alpha ramp be checked when a D/A card is plugged in for the first time. This will reflect any distortion that may be introduced into the alpha ramp as well as 1-alpha.

Sheets 1 and 2 of 1Ø811Ø-6Ø1 are shown.
SEE SHEETS 2 & 3 FOR LADDER DRIVER DETAIL

RESISTANCE VALUES FOR R1 TO R24 ARE MEASURED TO 0.01% AND VALUES FOR D/A NETWORK ARE PICKED BY COMPUTER PROGRAM, BUT RESISTANCE IS MEASURED WITH GATE SHOWN TO SOURCE AND FETS FOR DRIVERS ARE SELECTED BY COMPUTER PROGRAM.

EQUIVALENT RESISTANCE = 10K

DEGLITCH CIRCUIT

NOTE: RESISTOR TOLERANCE IS INDICATED BY NUMBER OF DIGITS. FOR EXAMPLE:
10K0 ± 1% METAL FILM 1/8W
10K ± 1% METAL FILM 1/8W
10K ± 5% METAL FILM 1/8W
EXCEPT WHERE MARKED OTHERWISE
BASIC PATTERN FOR TESTING D/A'S

X HIGH ORDER BITS

GND

-REF

LOW ORDER BITS

GND

-REF

RAMP
Note that the fet's are symmetric and in that sense they are all used in similar manner.

Also note that the 29Ø7 transistors are connected in a pseudo differential configuration and therefore Q137-148 will turn on only if all other transistors in their corresponding rows are off.

A suggested pattern for testing the X D/A is shown on the next page. A similar pattern could be used for Y.
The output of each bit is taken on the fet side of the 19.98 K resistors.

If the D/A card passes this test it is almost home. A number of other patterns should be tried and in a failing case the problem can be traced to its source by noting the frequency of occurrence of the problem in one cycle. For example in the above pattern if the lines are bad in half of the scope and OK in the other half it is obvious that the most significant bit is not working right.

A supplement to this manual will be available that has a number of patterns and their respective significance listed.
The Z D/A

The Z D/A is similar to X and Y D/A's except in a few points.

The output opamp has a gain of 1 therefore the output levels are ground to -ref.

No reencoding is done here.

There are only 8 Z bits.

The same procedure can be used to test this card with the exception that the output will not be observable as easily on the scope.

It is adviseable that the output of the Z D/A studied carefully with an osilloscope.
6) Scope Select Card

This card takes care of the dash and center dash sequences.

There is a mod oscillator on this card that generates a 50 mhz sine wave that is run through a bunch of flip flops to get down to some reasonable frequency.

With any luck this setup will be redesigned sometime soon. So don't sweat it.

The parts of this that are important to note follow: the scope select logic can be checked easily by grounding one of the "IN" inputs and making sure that the corresponding "Sel" follows.

The signal intcor should be checked as a function of the line length. (refer to 1Ø8115-6ØØ sheet 3)

If the output of X and Y D/A's are noisy the deglitch logic may be failing.
7) The scope drivers.
ECO A-1 on Mho's Memo on What to do until Cheadle comes.

Setting the tabs on the scope driver.

The scope driver (108113) has two delay lines that are used to compensate for the length of the cable between the line generator and the scope and also for the delay (if any) of the scope yoke with respect to its video amplifier.

The INTENSIFIER signal (logical product of Select and Intensify) is fed into a delay line and there are 20 taps available from the delay line.

The delay line enables us to delay the start point of the input signal or to lengthen it or both. The circuit does not allow shortening the signal in any way.
The circuit that makes this magic possible is the transistor pair (Q4, Q5 or Q6, Q7).

A decision was made sometime after the first system to treat the short vectors different therefore there are two transistor pairs and four tap connectors available. For any line, however, only one of the pair is used.

When the intensifier signal is on the tap connector that is closest to the input will determine the input beginning of the line. Note that the two tap connectors are symmetric and therefore the first transistor that is turned on will start the line.

On the other hand the second tap, the one further down the line, will stay on longer and therefore the end point is determined by this one.

This results in the following procedure for setting these taps.

Connect both wires together and fond the best starting point for the lines (staps for short lines and L taps for long ones) the following pattern is recommended

![Diagram](image-url)
Once the starting point of the line is found the end can be extended if necessary.

NOTE

This is not going to be quite so easy so the Prophet suggests trying to center the lines first. That means that if you are showing the squares tie the two taps together and try to find the best picture (which means that the lines may not quite meet but they are off the same from both sides) Then move the two taps away from each other hence changing the begining and the end of the lines simultaneously.

If more delay is required it will be evident when you are following the procedure but if the thing acts like nothing you have seen before check and see if the Unblank cable is terminated properly.
(1) Stopped at 1004

(2) S. Stepped 9 times
   a) Data into layer & swallow
   b) C2, move, settled
   input wait, all on
   Wait 2
   Wait 3
   Analyze

(3) Stepped 1 time
   a) Settled input out
   b) Odd value, B(12) on
   c) New layer & swallow
   d) C1, input wait, wait 2 are on

(4) Stepped 11 times
   a) D(1), out, odd out
   b) C2 on, input wait & flag 2 on

(5) Stepped once
   a) D(1) flag 1 on
   b) flag 2 stick on
   c) input wait out

(6) Stepped 24 times
   a) Channel looks up
   b) L6 same as above
NO OVERLAP

1) Slipped 9 times
   a) D(1) on
   b) C(2) on C(1) off
   c) move on
   d) data into longer & smaller

2) Slipped once
   a) D(1) on
   b) settled out
   c) Wait 3, ready wait out
   d) odd values on
   e) C(1) on C(2) off
   f) 2 sand.....data

3) Slipped 28 times
   a) channel C looks back up

4) reset once
   before input wait y on
   after delay wait z y on
   after input want 2 y on
   reset again
   settled, W2, AW) all on