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Data Systems Design's products are warranted against defects in materials and workmanship. For DSD products sold in the U.S.A., this warranty applies for ninety (90) days from date of shipment.* DSD will, at its option, repair or replace either equipment or components which prove to be defective during the warranty period. This warranty includes labor, parts and surface travel costs of system modules or components. Freight charges for other than surface travel or for complete systems returned for repair are not included in this warranty. Equipment returned to DSD for repair must be shipped freight prepaid and accompanied by a Material Return Authorization number issued by DSD. Repairs necessitated by shipping damage, misuse of the equipment, or by hardware, software, or interfacing not provided by DSD are not covered by this warranty.

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PREFACE

The material in this manual is subject to change without notice. The manufacturer assumes no responsibility for any errors which may appear in this manual.

Please note that DEC, PDP, RT-11, and UNIBUS are registered trademarks of the Digital Equipment Corporation.

SAFETY

Operating and maintenance personnel must at all times observe sound safety practices. Do not replace components, or attempt repairs to this equipment with the power turned on. Under certain conditions, dangerous voltage potentials may exist when the power switch is in the off position, due to charges retained by capacitors. To avoid injury, always remove power cord before attempting repair procedures.

Data Systems Design, Inc. will accept no responsibility or liability for injury or damage sustained as a result of operation or maintenance of this equipment with the covers removed and power applied.

CAUTION

This equipment had been tested with a class A computing device and has been found to comply with Part 15 of FCC Rules. See instruction manual. Operation in a residential area may cause unacceptable interference to radio and TV reception requiring the operator to take whatever steps are necessary to correct the interference.
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CHAPTER I

INTRODUCTION

The DSD 480 is an advanced double sided, double density flexible disk system for use with LSI-II and PDP-II computers. A complete system contains a chassis with two double sided disk drives, controller/formatter electronics and power supply, a separate interface card for LSI-II or PDP-II computers, interconnecting cables, a diagnostic diskette, and complete documentation. The system components are described below.

CONTROLLER/FORMATTER MODULE

The intelligence of the DSD 480 resides in the microcode of the controller/formatter module. It accepts commands sent across the interface cable and controls the operation of the disk drives.

This module contains a microprogrammed read/write controller and an 8-bit microprocessor. The interface/controller module is connected to the disk drives, the interface bus connector, and the power distribution assembly.

Near the top of the controller/formatter module is a set of eight switches mounted in a dual in-line package (DIP). These switches are used to establish different system configurations and to specify the self-contained "HYPERDIAGNOSTICS" used during maintenance operations. Located near the switch is a row of eight LED indicator lights which help you interpret the status of "HYPERDIAGNOSTICS" operation. Appendix A contains information about the standard jumper positions in this controller.

The controller/formatter is capable of formatting diskettes in any DEC or IBM format. This capability allows you to recover diskettes with altered formatting information. It also allows you to select a sequential interleave data pattern which may improve your system's throughput.

DISK DRIVES

The DSD 480 is equipped with two double-sided disk drives installed in the chassis. The drives write data or retrieve data from the flexible disks.

The drives used in the DSD 480 each consist of read/write and control electronics, read/write heads, a head positioning mechanism and a drive motor.

Each drive is fastened to the DSD 480 chassis by four screws accessible from the underside of the chassis. A 50-conductor flat-ribbon cable connects the controller module to the drives. Two additional cables provide AC and DC power to the connectors on each drive. Appendix B contains a copy of the maintenance manual published by the drive manufacturer.
COMPUTER INTERFACE CARD

The computer interface card is a printed circuit board that accepts commands from the computer and passes them to the controller/formatter module. Data Systems Design manufactures interface modules for the DEC LSI-11 and PDP-11 computers.

POWER SUPPLY

The DSD 480 power supply is an open-frame unit using linear regulators. Direct current output voltages include: +5 volts, +24 volts, and unregulated -12 volts. The power supply contains two trimmer potentiometers which can be used to adjust the +5 and +24 volt outputs.

INTERCONNECTING CABLE

The 10 foot, 26-conductor interconnecting cable serves as a signal path between the controller/formatter module and the computer interface card. The connectors on the ends of each cable are keyed on pin 23 to insure proper connection. Cable lengths greater than 10 feet require twisted pair leads and are not supplied or supported by DSD.

WARNING

Interconnecting cable should never exceed 20 feet.
UNPACKING AND INSPECTION

When your DSD 480 shipment arrives, inspect the shipping container immediately for evidence of mishandling during transit. If the container is damaged, request that the carrier's agent be present when the package is opened.

Compare the packing list attached to the shipping container with your purchase order to verify that the shipment is correct. Report any discrepancies to DSD Customer Service.

Unpack the shipping container and inspect each item for external damage such as broken controls and connectors, dented corners, bent panels, scratches and loose components.

If any damage is evident, notify DATA SYSTEMS DESIGN immediately.

Retain the shipping container and packing material for examination in the settlement of claims or for future use.

POWER REQUIREMENTS

The DSD 480 is shipped in one of two line voltage ranges:

100-120 VAC
or
220-240 VAC.

Systems which are configured for one range cannot easily be reconfigured for the other range.

CAUTION

The procedure required to convert between a low voltage range (100-120 VAC) and a high voltage range (220-240 VAC) is far more complicated than just changing the position of the printed circuit board. This conversion requires changing the fan, the two AC spindle motors in the disk drives, the motor capacitors associated with the spindle motors, and the fuse. NEVER change the position of the printer circuit board from the low line voltage range (100-120 Volts) to the high voltage range (200-240 volts) without changing the AC motors. These motors will be damaged if operated at the wrong voltage.
The DSD 480 may be configured to compensate for low power line voltages (100 VAC in the low voltage range or 220 VAC in the high voltage range). If your power line voltage is below 120 VAC (or 240 VAC in high voltage range) you may reconfigure the DSD 480 to compensate as follows:

1) Disconnect power from the unit by removing the AC power cord from the rear of the chassis.

**WARNING**

Failure to disconnect power before attempting this procedure may cause bodily injury.

2) Slide plastic shield to expose fuse.

3) Remove fuse by moving the lever marked "FUSE PULL".

4) Remove PC board adjacent to fuse holder. (See Figure 2-1)

5) Reorient and replace PC board so that desired voltage marking is visible after installation.

6) Replace fuse and reattach power card.

![AC Power Connector Assembly](image)

**Figure 2-1. AC Power Connector Assembly**

The DSD 480 is shipped in either a 60 Hz or a 50 Hz configuration. The line frequency must be within 1 Hz of the proper value for correct operation.
OPERATIONAL ENVIRONMENT

All flexible disk systems manufactured by DATA SYSTEMS DESIGN perform efficiently in normal computer room environments. Temperature, humidity, and cleanliness are three environmental considerations that can affect the reliability of diskette use. Refer to the DSD 480 data sheet for system specifications.

INSTALLING THE DSD 480 CHASSIS

The DSD 480 chassis must be installed within ten feet (3 meters) of the interface module's location to accommodate the length of the interconnecting cable. If the computer system operator will be changing diskettes often, it may be convenient to install the chassis close to the console terminal.

The DSD 480 may be either mounted in a standard 19-inch rack or installed on a table top.

The DSD 480 chassis should be mounted in such a way that the air flow behind the fan is unrestricted. The temperature of the air entering the chassis should not exceed 40°C (104°F).

The following procedure should be used to mount the DSD 480 in a standard 19 inch instrumentation rack:

NOTE

The DSD 480 is shipped in Mode 2 (RX02 compatible configuration. If you wish to change this configuration, or to run the HYPERDIAGNOSTIC exercisers for incoming inspection, it will be easier to do so before installing the unit in a rack. To change the operating mode, refer to the "HARDWARE MODES" section of Chapter 2. The HYPERDIAGNOSTICS are described in detail in Chapter 5.

1) Attach the optional slim-line chassis mounts to your rack using the hardware supplied with the mounts. Note that the left and right rear extender brackets are not interchangeable. Figure 2-2 illustrates the correct relationship of the rack mounting components.

2) Slide the DSD 480 chassis on the mounts until the two bullets at the rear of the chassis mounts engage the corresponding holes in the rear of the chassis as shown in Figure 2-3.

3) Remove the molded front "pop" panel from the chassis by pulling out the top of the panel.
4) Secure the chassis in the rack by bolting the front flange to the front rails of the rack as shown in Figure 2-4.

Figure 2-2. Chassis Slides Mounting
Figure 2-3. Securing the DSD 480 in a Rack
You may now replace the "pop" panel by pushing it straight back onto the two "head locks".

DSD 480 CHASSIS CABLE CONNECTIONS

The following procedure describes the installation of the AC power cord and the interface bus cable:

1) **VERIFY LINE POWER SWITCH IS OFF.**

2) Plug the female end of the power cord into the connector on the back of the chassis. (The plastic shield must be raised.)

3) Plug the other end into an AC power receptacle.

4) Route the free end of the interface bus cable over to the rear of the chassis.

5) Plug the interface cable into the 26 pin connector so that the striped side of the cable is toward the middle of the chassis.

Be sure the position of the clipped pin in the chassis connector matches the position of the plugged hold in the cable connector.

INSTALLING THE DSD 480 INTERFACE MODULE AND CABLE

Ensure that all system and line power is off before proceeding with this section of the DSD 480 installation. There are separate procedures for LSI-II and PDP-II based systems.

The hardware bootstrap program on the interfaces is preset to a specified range of addresses. These addresses may conflict with other devices or bootstraps already installed in your computer. In order to resolve address conflicts, you may either
disable the bootstrap completely or move it to an alternate base address. We recommend that the bootstrap be moved rather than disabled in order to keep it available.

**LSI-II Based Systems**

The DSD 480 interface module for LSI-II based systems, including the PDP-11/03, is a dual-wide card marked "P/N 4432". DATA SYSTEMS DESIGN ships this interface module configured as follows:

- **REGISTER ADDRESS:** 777170
- **BOOTSTRAP PROM:** ENABLED AT 773000
- **INTERRUPT VECTOR:** 264
- **INTERRUPT PRIORITY:** BR4
- **OPERATING MODE:** MODE 2 (RX02 COMPATIBLE)

The module allows you to select one of four device register addresses, one of four bootstrap PROM (Programmable Read Only Memory) starting addresses, and a 7-bit interrupt vector address. Table 2-1 lists standard and alternate addresses for the registers and starting boot PROMs. As shown in Figure 2-5, there is a separate jumper which, when installed, disables the bootstrap PROM.

<table>
<thead>
<tr>
<th>TABLE 2-1. LSI-II Register and Boot PROM Addresses</th>
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<tbody>
<tr>
<td>STARTING REGISTER ADDRESS</td>
</tr>
<tr>
<td>777170 (STANDARD)</td>
</tr>
<tr>
<td>777160</td>
</tr>
<tr>
<td>777140</td>
</tr>
<tr>
<td>777150</td>
</tr>
<tr>
<td>STARTING BOOT PROM ADDRESS</td>
</tr>
<tr>
<td>773000 (STARTING)</td>
</tr>
<tr>
<td>771000</td>
</tr>
<tr>
<td>* 775000</td>
</tr>
<tr>
<td>** 766000</td>
</tr>
</tbody>
</table>

* Use only this address of the system if configured for 31K of memory (0-774000).
** Do not use this address for the bootstrap in systems with over 28K of memory.

**NOTE**

When the interrupt vector jumpers are in place, the associated bit of the vector address is a "0". Thus, if all seven vector jumpers were to be installed, the vector address would be 000. Check your module against Table 2-1 and Figure 2-5 to ensure that it has been configured to match your system requirements before installation. Most system software assumes a device address of 777170 and an interrupt vector of 264. If
Interrupt Vector
Jumpers IV8-IV2
  Shorted = 0
  Open = 1

Normal Vector
is 2648:
IV8 = Shorted
IV7 = Open
IV6 = Shorted
IV5 = Open
IV4 = Open
IV3 = Shorted
IV2 = Open

DBST
Shorted = Disabled boot
Open = Enable boot

Figure 2-5. LSI-11 Computer Interface Card Diagram
you change either of these numbers, corresponding changes will be required in the software. Also, be sure to read the explanation of the bootstrap and diagnostic programs if non-standard addresses are used.

The following procedure describes how to install the LSI-II interface module:

1) **VERIFY LINE POWER IS OFF**

2) Plug one end of the interface cable into the interface module so that pin 1 (the striped side) is closest to the edge of the board. Note that the position of the clipped pin on the module connector matches the position of the plugged hole on the cable connector.

3) Plug the opposite end of the interface cable into the keyed connector mounted on the rear panel of the chassis. Note that the position of the clipped pin on the module connector matches the position of the plugged hole on the cable connector.

Now you are ready to plug the module into the lowest numbered available Q-Bus slot.

---

**NOTE**

No open Q-Bus slots are allowed between the processor and the DSD 4432 interface module. Since this module uses both interrupts and DMA (Direct Memory Access), a break in either of the grant propagation chains will prevent the interface module from obtaining control of the Q-Bus. Figure 2-6 shows how Q-Bus slots are numbered on the standard backplanes available from DEC. Some Q-Bus interface cards (e.g. serial interfaces and memory) do not pass the DMA grant signal. Ensure that the DMA signal is reaching the LSI-II interface (4432).

**PDP-II BASED SYSTEMS**

The DSD 480 interface module for all PDP-II based systems, except the PDP-11/03, is a quad card. DATA SYSTEMS DESIGN ships this interface module configured as follows:

- **REGISTER ADDRESS:** 777170
- **BOOTSTRAP PROM:** ENABLED AT 771000
- **INTERUPT VECTOR:** 264
- **INTERUPT PRIORITY:** BR5
- **OPERATING MODE:** MODE 2 (RX02 COMPATIBLE)

This interface module is marked "4430".

The twelve position shunt located at coordinates C-5 on the 4430 interface module is used to configure device register addresses and the bootstrap program starting address. Figure 2-7 is an illustration of the PDP-II interface module. It shows how the twelve shunt positions are numbered.
Figure 2-6. Option Priority in LSI-II Backplanes
Figure 2-7. PDP-II Computer Interface Card Diagram
Shunt positions 1 and 2 are used to configure the bootstrap program starting address as follows:

<table>
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<th>STARTING BOOT PROM ADDRESS</th>
<th>POSITION 1</th>
<th>POSITION 2</th>
</tr>
</thead>
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<tr>
<td>773000</td>
<td>OPEN</td>
<td>OPEN</td>
</tr>
<tr>
<td>771000 (STANDARD)</td>
<td>OPEN</td>
<td>CLOSED</td>
</tr>
<tr>
<td>775000</td>
<td>CLOSED</td>
<td>OPEN</td>
</tr>
<tr>
<td>766000</td>
<td>CLOSED</td>
<td>CLOSED</td>
</tr>
</tbody>
</table>

The bootstrap program contained on the interface module occupies 256 words of memory space, starting at one of the four selectable addresses shown above. If you do not want the bootstrap program to respond to any addresses, the bootstrap disable jumper should be installed as shown in Figure 2-7.

Shunt positions 3 through 12 correspond to address bits A3 through A12 respectively when configuring the device register address. A closed shunt position corresponds to a binary 0 and an open shunt position corresponds to a binary 1. When the PDP-II interface module is shipped, it is configured to respond to a base register address of 777170 (octal). This is done by having shunt positions 7 and 8 left closed, and positions 3, 4, 5, 6, 9, 10, 11 and 12 punched open.

The eight position shunt located at coordinates B-12 is used to configure the interrupt vector address. Figure 2-7 shows how the eight shunt positions are numbered. Position 1 is not used. Positions 2 through 8 correspond to interrupt vector address bits IV2 through IV8 respectively. A closed shunt position corresponds to a binary 0 and an open shunt position corresponds to a binary 1.

When this interface module is shipped, it is configured to have an interrupt vector address of 264 (octal). This is done by having shunt positions 3, 6 and 8 left closed, and positions 2, 4, 5 and 7 punched open.

If the interrupt priority level must be changed, cut and jumper the circuit board to resemble the diagram corresponding to the desired interrupt priority level as shown in Figures 2-8 and 2-9. If the priority levels will be changed often, cut the six permanent traces and install the four 8-pin IC sockets in the positions outlined on the board. Placing either four-position shunts or DIP-Switches in the sockets will allow for repeated jumper changes. The interrupt priority jumpers are located at coordinates A-9 and A-10 on the interface module circuit board. Interrupt priority level 4 is the lowest and level 7 is the highest.

If the system is to be operated in Mode 1 (RX01 compatible) when the EN RX01 jumper located near coordinates A-12 must be installed. This number is removed for RX02 compatible operation.
Figure 2-8. PDP-11 Interrupt Priority Levels
The following procedure describes how to install the PDP-11 module:

1) **VERIFY LINE POWER IS OFF.**

2) Check that the jumpers on the interface module are configured correctly.

3) Plug one end of the interface cable into the interface module so that pin 1 (striped side) is closest to the module handle.

4) Confirm that the position of the clipped pin on the module connector matches the position of the plugged hole on the cable connector.

5) Plug the module into a convenient SPC (Small Peripheral Controller) slot.

Be sure there is grant continuity between the processor and the interface module. If there are open SPC slots between the processor and the interface module, place a grant continuity card in slot D.
NOTE

Since the 4430 interface module uses DMA (Direct Memory Access), you must be sure there is no backplane jumper or foil trace between backplane pins CA1 and CB1 of the selected SPC slot. These two pins normally connect NPG (Non-Processor Grant) IN to NPG OUT. Usually the pins are left connected since most Small Peripheral Controllers do not use DMA. If this jumper is not removed and a 4430 interface module is installed configured either for RX01 or RX02 compatible operation, the computer system will stop. Replace the jumper any time the 4430 module is removed.

Figure 2-10. Typical UNIBUS Hex Backplane
HARDWARE MODES

The DSD 480 may be configured for one of three operating modes or a "HYPERDIAGNOSTIC" mode. The desired mode is selected by means of a DIP-Switch located on the controller module. Each mode is described briefly below and in detail in Chapters 4 and 5. The DSD 480 is shipped in Mode 2 (RX02 compatible).

Mode 1 (RX01 Compatible)

In RX01 mode, the DSD 480 emulates the DEC RX01. Recording is done in IBM 3740 (DEC single density) format only. Data are transferred by programmed I/O. Single sided diskettes only may be used in RX01 mode.

Mode 2 (RX02 Compatible)

In the RX02 mode, the DSD 480 is configured to emulate the DEC RX02. In this mode, it reads and writes in DEC double density and IBM 3740 single density diskette formats. Data are transferred by DMA. The DSD 480 also reads and writes on double-sided diskettes in DEC double density, IBM 3740 (DEC single density) and IBM 2D-256 double density formats. The DSD RT-11 monitor patch program must be executed to activate two-sided operation under RT-11. The procedure is described in Chapter 4. Once this operation has been performed, these formats are transparent to DEC software.

Mode 3 (Extended IBM)

The DSD 480 IBM mode is a "superset" of the RX02 mode. In addition to the RX02 mode formats, the DSD 480 also reads and writes in all other IBM formats. A modified software handler is required to support the additional formats not available in Mode 2 (RX02). More detail is provided in the software section, Chapter 4.

"HYPERDIAGNOSTIC" Mode

DSD's exclusive "Hyperdiagnostics" are a library of microprogrammed routines for stand-alone exercising and monitoring of the disk system. The routines are selected from the DIP-Switch or the controller module. Chapter 5 provides a complete description of "Hyperdiagnostic" operation.

Switch Selection of Operating Mode

DATA SYSTEMS DESIGN ships the DSD 480 configured for Mode 2 (RX02 Compatible) operation. Selection of other modes is done via the DIP-Switch on the controller module. For Mode 1 operation, the jumper "ENRX01" on the LSI-II or PDP-II interface card must also be installed. Figure 2-11 shows the DIP-Switch selector. The switches may be set conveniently with a ball point pen or other sharp implement. Table 2-2 lists the controller DIP-switch functions. Figure 2-12 illustrates the proper switch settings for normal mode operation.
This indicates a switch position to be selected by the user.

This shows switch 4 in the "1" or OPEN position.

This shows switch 1 in the "0" or Closed position.

Figure 2-11. Controller/Formatter Module DIP-Switch
<table>
<thead>
<tr>
<th>SWITCH NUMBER</th>
<th>SWITCH NAME</th>
<th>WHEN CLOSED</th>
<th>WHEN OPEN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,2,3</td>
<td>Self Test Select</td>
<td>All Closed for Normal Operation</td>
<td>Selects a Hyper Diagnostic Function</td>
</tr>
<tr>
<td>4</td>
<td>Mode Select</td>
<td>Selects RX02 or Mode 2 (RX02 compatible) or Mode 3 (IBM compatible)</td>
<td>Select Mode 1 (RX01 compatible)</td>
</tr>
<tr>
<td>5</td>
<td>Drive Mapping Select</td>
<td>Left Drive = Unit 0</td>
<td>Right Drive = Unit 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Right Drive = Unit 1</td>
<td>Left Drive = Unit 1</td>
</tr>
<tr>
<td>6</td>
<td>Drive Type Select</td>
<td>Single Sided Drive</td>
<td>Double Sided Drive</td>
</tr>
<tr>
<td>7</td>
<td>Extended Format Select</td>
<td>Mode 2 Read all DEC and IBM 26 Sector Formats</td>
<td>Mode 3 Read all DEC and IBM Formats</td>
</tr>
<tr>
<td>8</td>
<td>Select Number of Drives</td>
<td>Operate One Drive</td>
<td>Operate Two Drives</td>
</tr>
</tbody>
</table>
### Specifics "Normal" Mode

- Specifies RX02 Configuration
- Specifies Normal Drive Mapping
- Specifies Drive Type
- RX02 Configuration
- Specifies 2-Drive System

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 3, 5, 6, 8</td>
<td>Closed</td>
</tr>
<tr>
<td>4, 7</td>
<td>Open</td>
</tr>
</tbody>
</table>

**Black Dot is on Depressed Side of Switch.**

- Closed = 0
- Open = 1

---

**Figure 2-12. Controller DIP-Switch Settings: Normal Modes**
CHAPTER 3

BASIC SYSTEM OPERATION

This section explains how to turn on and operate your DSD 480 after correctly installing it. Chapter 2 details the installation procedure.

APPLYING AC POWER

Once the correct AC (alternating current) power is connected, simply turn the line switch on the DSD 480 chassis to the "ON" position. The location of the line switch is shown in Figure 3-1.

The DSD 480 chassis and the interface module can be safely powered up in either order. There is no danger of writing on diskettes loaded in the drives during power up or power down cycles.

![Back Panel of DSD 480](image)

Figure 3-1. Back Panel of DSD 480
INSERTING A DISKETTE

Open the DSD 480 drive door, and insert the diskette into the drive as shown in Figure 3-2. Close the drive door.

You are now ready for an initialization response check of your computer and flexible disk system.

Figure 3-2. Orientation of Diskette for Insertion
INITIALIZATION RESPONSE CHECK

When the DSD 480 is connected correctly to the host computer, it performs an initialization response (INIT) upon power-up. An initialization response can also be forced by any of the following operator console actions:

LSI-II BASED SYSTEMS

1) Flip the INIT switch (if there is one) on the host computer.
2) Using ODT (Octal Debugging Tool), enter the "G" command at any arbitrary starting address.
3) Using ODT, write the number 40000 into the DSD 480 RXCS register, normally at address 777170.

PDP-II BASED SYSTEMS

1) Generate a UNIBUS INIT by depressing the START switch or button on the processor.
2) Using the console, write the number 40000 into the DSD 480 RXCS register, normally at address 777170.

Each time you generate an INIT, you should hear the drives as the controller moves the head to track 0. The activity lights on the front of the drives should come on briefly. If a diskette is loaded into drive 0 (normally the left hand drive) you should also hear the head load. The drive 0 activity light remains on slightly longer as the controller reads track 1/sector 1 of the diskette into the sector buffer.

If you did not observe the results described above, ensure that you have:

1) Applied power to both the computer mainframe and the DSD 480 chassis.
2) Connected both ends of the DSD 480 interface bus cable in the proper orientation. (The red drive select lights remain on if the cable is reversed.)
3) Generated a system or device initialize signal by one of the methods described above, and the signal is reaching the DSD 480 interface.
4) Closed the drive doors.
5) Set the controller module DIP-Switch as described earlier in this chapter.
6) If the system fails to respond, the problem may be caused by low power supply voltage. This condition is indicated if all LEDs on the 480 controller board (inside chassis) are illuminated.

If you are still unable to force an INIT, refer to Chapter 5.
SYSTEM BOOTSTRAPPING

STANDARD LSI-II AND PDP-II SYSTEMS

Before attempting to bootstrap your DEC operating system diskette, ensure that the DSD 480 operating mode (RX01 or RX02 compatible) matches the system device handler. The DSD 480 will boot from either single or double sided DEC-formatted diskettes if the appropriate operating system files are present. Mode 1 (RX01 compatible) operates with single sided, single density diskettes only. The RT-11 monitor files DXMNSJ.SYS or DXMNF.B.SYS must be present.

In Modes 2 and 3, the DSD 480 will boot from either single or double density diskettes provided that the file DYMNJSJ.SYS or DYMNF.BS.YS is present. Chapter 4 describes how to convert a single density operating system diskette to double density operation. It also describes how to generate bootable double-sided diskettes.

NOTE

For 2-sided diskettes the monitor files must be on side zero.

The DSD 480 features a built-in hardware bootstrap program on the LSI-II and PDP-II interface modules. When this 512-byte (256 16 bit words) program is executed by the computer, the operating system is automatically loaded into memory from either a single or double density diskette. The bootstrap also performs diagnostics which confirm operation of the interface, controller and processor memory. These diagnostics include:

1) A fill and empty buffer test which verifies the sector buffer and DMA transfer capability. It loads a data pattern into the controller sector buffer, then reads it back into memory and compares the results.

2) A command and status register bit-latch test that confirms correct operation using the DSD 480 interface register.

3) A computer memory test that checks contiguous memory to 28 K for both data and address line errors.

If a malfunction is detected during execution of any of these tests, the computer either HALTs or continuously executes a program loop. If this occurs, refer to Appendix D.

NON-STANDARD DEVICE ADDRESSES

Most DSD 480 systems are configured so the command and status register responds to address 177170. This address is regarded as the "standard" device address for the first flexible disk system installed on LSI-II or PDP-II based computer systems. Under certain circumstances, you may want to configure your DSD 480 system to respond to a non-standard device address. If this is done, the bootstrap procedure is slightly modified.
The following are descriptions of several types of bootstrap starting procedures:

1) RXCS at 777170

If the shunts on the interface module are set up so that the bootstrap program base address is 773000 for LSI-II or 771000 for PDP-11, and the RXCS = 777170 (standard address), then bootstrap by starting the computer at the bootstrap program base address.

2) RXCS at 777150

If the interface module is modified so that the RXCS = 777150, the system is bootstrapped by starting the computer at the bootstrap program base address plus 20 (octal). In this case the base address is 173020.

3) Alternate Base Addresses

If the interface module is modified so that the device address is any legal address other than 777150 or 777170, follow this procedure:

a) Write the device address (e.g. 177160) into memory address 000000.

b) Write the number 000340 into CPU register 0 (RO).

c) Write the number 000002 into CPU Register 1 (R1).

You can now start the computer at the bootstrap program base address plus 40 (octal). In this case the start address is 773040.

NOTE

If the DSD 480 is configured for a non-standard device address, the system device handler on the operating system must be altered. In addition, the bootstrap on the diskette must be updated to include the revisions to the monitor.

ROM (READ ONLY MEMORY) INSTALLED AS MAIN MEMORY

The DSD 480 bootstrap program reports a memory error if a block of ROM (read-only memory) is installed within the first contiguous block of read/write memory below 30 K. If you encounter a memory error caused by ROM installed as main memory, refer to the following section.

BOOTSTRAPPING WITHOUT SYSTEM TEST FUNCTIONS

The following procedure describes how to skip all of the system test functions included in the DSD 480 bootstrap program and to directly bootstrap the operating system:
1) The LINE-TIME CLOCK switch must be off.

2) Deposit the device address of the device to be bootstrapped in location 000000. (typically 777170)

You may now start the CPU at 524 (octal) address locations beyond the boot base address.

ACCEPTANCE TESTING

When the DSD 480 is first installed, you may confirm proper operation by running the "VERIFY" routine of the software diagnostic program, FLPEXR. This routine will run continuously unless halted. All system functions will have been tested when the message "short pass completed" is printed. The diagnostic may be halted when this occurs. Please refer to Chapter 6 for a complete discussion of software diagnostics.
CHAPTER 4

SOFTWARE

OPERATING MODES

The DSD 480 has three operating modes; Mode 1 (RX01 compatible), Mode 2 (Rx02 compatible), and Mode 3 (Extended IBM). The procedure for selecting the proper mode is described in Chapter 2. Modes 1 and 2 are fully DEC-compatible. To activate double sided support in these modes, a patch to the RT-11 V3B monitor is required. The procedure is described in detail below. IBM 26 sector per track formats both single and double density can also be written or read in a DEC-compatible mode - transparent to DEC software.

In Mode 3, the DSD 480 hardware will read and write all IBM diskette formats in addition to DEC formats. A modified device software handler is required to support these formats. Mode 3 protocol is described in detail in this chapter. A complete description of the various operating modes is provided in Table 4-1.

DISKETTE COMPATIBILITY

The DSD 480 will accept all DEC or IBM-compatible soft-sectored diskettes. A description of the DEC and IBM formats is provided in Table 4-1.

NOTE

Single Sided Diskettes:

1) DEC's single sided, single density format is the same as the IBM 1-128 format (also called IBM 3740). The diskettes are equivalent and may be used interchangeably.

Double Sided Diskettes:

2) For two-sided, single density, DEC-compatible operation, the DSD 480 uses IBM 2-128 formatted diskettes. This is simply the DEC single density format repeated on both sides of the diskette.

3) DEC and IBM double density formats are significantly different. IBM writes both headers and data in double density while DEC writes headers in single density and data in double density. Since DEC does not currently offer double-sided diskettes, the two-sided, double density DEC format is generated from IBM 2-128 (single density) diskettes by changing the data sections to double density. Two-sided, DEC double density diskettes are easily generated on the DSD 480 using the "set media density" command described under "Formatting Diskettes."
<table>
<thead>
<tr>
<th>DISKETTE TYPE (IBM PART #)</th>
<th>FORMATTED CAPACITY (BYTES)</th>
<th>NUMBER OF SURFACES</th>
<th>TRACKS PER SURFACE</th>
<th>TRACK 0, SIDE 0</th>
<th>TRACK 1-76</th>
<th>TRACK 0, SIDE 1</th>
<th>TRACK 1-76</th>
<th>SECTORS PER TRACK</th>
<th>SUPPORTED BY DSD 440</th>
<th>SUPPORTED BY DSD 470</th>
<th>SUPPORTED BY DSD 490</th>
<th>IBM SYSTEM OR DEVICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEC Single Density</td>
<td>IBM 3740</td>
<td>256,256</td>
<td>1</td>
<td>77</td>
<td>0</td>
<td>128</td>
<td>128</td>
<td>-</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>RX01, RX02</td>
</tr>
<tr>
<td>IBM Diskette 1</td>
<td>IBM 1-128</td>
<td>246,272</td>
<td>1</td>
<td>74</td>
<td>2</td>
<td>128</td>
<td>128</td>
<td>-</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>RX01, RX02, IBM</td>
</tr>
<tr>
<td>IBM Diskette 2</td>
<td>IBM 2-128</td>
<td>492,544</td>
<td>2</td>
<td>74</td>
<td>2</td>
<td>128</td>
<td>128</td>
<td>-</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>RX02, IBM</td>
</tr>
<tr>
<td>IBM Diskette 2D</td>
<td>IBM 2D-256</td>
<td>985,088</td>
<td>2</td>
<td>74</td>
<td>2</td>
<td>256</td>
<td>256</td>
<td>-</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>RX02, IBM</td>
</tr>
<tr>
<td>IBM Diskette 2D</td>
<td>IBM 2D-128</td>
<td>1,136,640</td>
<td>2</td>
<td>74</td>
<td>2</td>
<td>256</td>
<td>256</td>
<td>-</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>IBM</td>
</tr>
<tr>
<td>IBM Diskette 2D</td>
<td>IBM 2D-102a</td>
<td>1,212,416</td>
<td>2</td>
<td>74</td>
<td>2</td>
<td>102a</td>
<td>128</td>
<td>-</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>IBM</td>
</tr>
<tr>
<td>IBM Diskette 2D</td>
<td>IBM 2D-256</td>
<td>985,088</td>
<td>2</td>
<td>74</td>
<td>2</td>
<td>256</td>
<td>256</td>
<td>-</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>IBM</td>
</tr>
</tbody>
</table>
DEC COMPATIBLE MODES

Modes 1 and 2 of the DSD 480 are fully DEC-compatible. Mode 2 (RX02 compatible) data transfers are done with DMA (direct memory access). Reading and writing is done in either single or double density. Mode 1 operation is single density only. Data transfer is by Programmed I/O.

SINGLE SIDED OPERATION

Although the DSD 480 has double-sided disk drives, it will, of course, operate with single-sided diskettes. In fact, with single-sided diskettes, the DSD 480 provides a true emulation of the DEC RX02 (or RX01).

DOUBLE SIDED OPERATION

The DSD 480 allows the user to take full advantage of double capacity by activating double sided support in the DEC system monitor. Under double sided operation, bit 9 of the device COMMAND AND STATUS REGISTER (RXCS) is used to select diskette side I for reading or writing, and bit 1 of the ERROR AND STATUS REGISTER (RXES) is used to indicate "side I Ready".

The resulting RT-11 or RSX-11 monitor is fully DEC compatible. The operating system will function properly with DEC hardware (RX02) and all DEC utilities and applications programs. Appendix I describes the procedure for implementing double sided support in the DEC RT-11 and RSX-11 system monitors.

After double sided support has been installed in the monitor, the operating system will automatically check for the presence of double sided diskettes, and performs appropriate directory and housekeeping functions to make double or single sided operation fully software transparent. All system utilities (PIP, DUP, DIR, etc.) will function correctly with single or double sided diskettes.

For example, when a double sided diskette is initialized using "DUP" under RT-11, the monitor will recognize that the diskette is double sided. If the diskette is double density, there will be 1962 free blocks. If the disk is single density and double sided, there will be 974 free blocks.

If the user inserts a single sided diskette into the system, the monitor and floppy controller will recognize that the diskette is single sided and function properly.

NOTE

Double sided diskettes will not function properly in a single sided drive.
SINGLE DENSITY DISKETTES IN A DOUBLE DENSITY RX02-COMPATIBLE SYSTEM

The DSD 480 allows previously recorded single density file diskettes to be read and written by a double density operation system. The double density software device handler also reads and writes previously recorded single density diskettes. The expected density of a diskette is specified with the initial command sent by the device handler to the DSD 480. If the density of the diskette does not match the density specified in the command, the DSD 480 will report a density error to the device handler. In response, the handler will retransmit the command specifying the correct density. The entire operation is automatic, thus freeing you from manually checking each diskette to determine its density.

IBM 2D-256 COMPATIBILITY IN MODE 2

While in RX02 mode, it is possible to read and write in IBM 2D-256 double density format, in the same fashion as a normal diskette. This allows the operator to exchange programs and data between DEC and IBM systems using the normal RX02 command structure.

As described earlier, IBM double density differs from DEC double density in that IBM sector headers and data are written in double density while DEC headers are single density and data are double density (Table 4-1). Note also that track 0 of an IBM 2D diskette is written in single density while the other 76 tracks are double density. This track is not normally used for data, and is not used by DEC RT-11 or RSX-11 software. Hence, it is possible to use an IBM 2D-256 diskette as a DEC system diskette. The procedure for generating a system diskette is described later.

The DSD 480 controller will automatically recognize the format of the diskette being used. IBM 2D-256 diskettes may be accessed with the standard DEC read and write calls or, if they contain a DEC operating system, they may be booted directly in the normal fashion.

MODE 3

Mode 3 (Extended IBM) of the DSD 480 is an extension of Mode 2. It allows the user full compatibility with all DEC and IBM diskette formats. In addition, alternate track assignment is provided in a software transparent fashion. Mode 3 uses a special software device protocol which is described in this chapter. It is the user's responsibility to implement a device handler to support this protocol.

PROGRAMMING INTERFACE

The system interface with the DSD 480 varies according to the host computer type and the operational mode for which the system is configured. The characteristics of the DSD 480 operation are embedded in the controller. A separate protocol for each mode is used to communicate with the interface module and host computer program.
The remainder of this chapter is organized by computer family and operational mode.

NOTE

All address locations and numerical machine values are represented in octal format.

DEC II FAMILY

The system interface with the DSD 480 is identical for the LSI-II and PDP-II.

During Mode 1 (RX01 Compatible) or Mode 2 (RX02 Compatible) operation, data are transferred to and from the diskette in fixed length blocks called sectors. A sector contains 64 sixteen bit words when the system is being used in single density mode, and 128 sixteen bit words in double density mode. During Mode 3 (Extended IBM) operation, data are transferred in sectors of variable lengths.

The programmer can direct the DSD 480 controller to perform several operations or tasks. Each of these tasks is used to facilitate the storage and retrieval of information on a diskette.

As an example, two operations are needed to move a sector of data from main memory to a particular sector on a diskette. The first operation is called FILL BUFFER. This is used to move the data from computer memory to a RAM buffer which is an internal part of the disk controller. The second operation is called WRITE SECTOR. This positions the read/write head of a flexible disk drive over the specified portion of the diskette, and writes the data stored in the controller's sector buffer on the diskette.

The programmer communicates his task requirements to the DSD 480 controller through two physical registers which are addressed as though they were in computer memory. The CONTROL AND STATUS REGISTER is normally located at address 777170 octal. The DATA BUFFER REGISTER is normally located at address 777172 octal.

There are a total of seven "logical registers" that are mentioned throughout this chapter. These registers represent such information as data, controller status, track address and sector address. The programmer always reads and writes logical registers through the DATA BUFFER REGISTER, which is a physical register.

A task is initiated by writing a specific bit pattern to the CONTROL AND STATUS REGISTER. Each task is associated with a specific "protocol." A protocol is a set of rules which determine the parameters or data the computer should be passing through the DATA BUFFER REGISTER during the execution of a task.

For example, operations which move the read/write head in the disk drive require a track and sector address. The protocol for these functions is as follows:

1) The command is written to the CONTROL AND STATUS REGISTER.
2) The sector address is written to the DATA BUFFER REGISTER when the controller requests it.

3) The track address is written to the DATA BUFFER REGISTER when the controller requests it.

The DSD 480 operational modes influence the protocol associated with the various tasks. The main difference in these modes centers on data transfer and storage characteristics. In Mode I, programmed I/O is used exclusively for the transfer of both data and parameters between the computer and controller. In Modes 2 and Mode 3, programmed I/O is used to transfer parameters, but DMA is used to transfer data between the controller and main memory.

In Mode 1, data are recorded on a diskette in single density only. In Modes 2 and 3, data are recorded in either single density or double density.

MODE I (RX01 COMPATIBLE) OPERATION

The system assumes MODE I operation when the "RX01" switch (located on the controller module) is placed in the "I" position and when the "ENRX01" jumper is installed on the PDP-11 or LSI-11 interface boards. Any program that runs successfully with the DSD 210, DSD 110, DSD 440 or the DEC RX-11 (or RXV-11) runs equally well on a DSD 480 system configured for operation in MODE 1.

PERIPHERAL DEVICE REGISTERS

Programs communicate with the DSD 480 through two peripheral device registers. They are as follows:

<table>
<thead>
<tr>
<th>NAME</th>
<th>DESCRIPTION</th>
<th>OCTAL LOCATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXCS</td>
<td>COMMAND AND STATUS REGISTER</td>
<td>777170</td>
</tr>
<tr>
<td>RXDB</td>
<td>DATA BUFFER REGISTER</td>
<td>777172</td>
</tr>
</tbody>
</table>

Peripheral device registers reside in the top 4K words of the DEC-11 family computers' memory address space. They are addressed as memory and any instruction that can operate on a memory location can operate on a peripheral device register in the same way. For information explaining how to assign non-standard bus addresses to these registers, see the section in Chapter 2 that describes installation of the interface module and cable.

COMMAND AND STATUS REGISTER (RXCS)

Writing bit patterns to this physical register controls the DSD 480. The format for this register is shown in Table 4-1. The RXCS register also provides important status information and error indications when read by the program.
**DATA BUFFER REGISTER (RXDB)**

The RXDB is physically a shift register that provides the communication link between the host processor and the DSD 480 system. The logical information passed through this physical register is based upon a predetermined protocol which is defined in the Mode I protocols section in this chapter.

If the DSD 480 is not in the process of executing a command, the RXDB can be written without risk. However, during the execution of an instruction, the RXDB register will only provide or accept information (according to the RXDB protocol) when the TRANSFER REQUEST flag is set.

**NOTE**

Data may be lost if the correct protocol is not followed. Only RXDB bits 0-7 are accepted by the controller. Bits 8 through 15 are ignored.

The following descriptions explain the various logical register formats of the physical Data Buffer Register of RXDB.

**Data Buffer (RXDB)**

The data buffer register is used by the function in process to transfer data to and from the controller data buffer. All information is transferred as a byte through bits 0-7 of the RXDB.

**Disk Track Address (RXTA)**

At the proper time during commands requiring a track number (e.g. write sector, read sector), the track number is written to the physical RXDB register as if it were a logical register. This is the TRACK ADDRESS REGISTER (RXTA = 777172). Track numbers from 0-76 (decimal) are valid.

**Disk Sector Address (RXSA)**

At the proper time during commands requiring a sector address (e.g. write sector, read sector) the sector address is written to the physical RXDB register as if it were a logical register. This is the SECTOR ADDRESS REGISTER (RXSA = 777172). Sector addresses from 1-26 (decimal) are valid. The controller microprocessor masks bits 6 and 7 of the RXSA to zeroes.

**System Error and Status Register (RXES)**

The RXES is a logical register that is implemented using the physical RXDB shift register. It provides status and error information about the drive that has been selected in bit 4 of the physical RXCS register. At the completion of a command, the controller
places the RXES register into the data buffer register (RXDB = 777172) so that the host processor can check the status of the most recent operation.

BIT 7 - DR V RDY - Drive Ready

This bit, when set, indicates that the selected drive has a diskette installed correctly. The Drive Ready bit is only valid immediately following the Ready Status function. The bit is valid for drive 0 immediately following an initialize.

BIT 6 - DD - Deleted Data

This bit indicates that a deleted data address mark was found during the last READ SECTOR operation or that the last command was WRITE DELETED DATA SECTOR.

BIT 5 - DR V DEN - Drive Density

This bit indicates the density of the diskette installed in the selected drive. When asserted, double density is indicated. This bit is updated during READ or WRITE SECTOR operations.

BIT 4 - DEN ERR - Density Error

This bit indicates that during a READ or WRITE SECTOR operation, the controller found that the density of the selected diskette did not match the density given in the command. The operation is terminated and the ERROR and DONE bits are set.

BIT 3 - WP - Write Protect (RX01 Mode only)

This bit is set whenever a write is attempted on a write-protected diskette. This RXDB bit along with the ERROR and DONE bits of the RXCS is set when the controller/drive subsystem loses power, or the IBUS cable is disconnected.

BIT 2 - ID - Initialize Done

This bit indicates that the controller/drive subsystem has just completed an initialization sequence. This sequence may have been started by a power failure, bus INIT, or programmed INIT.

BIT 1 - PAR - Parity Error

This bit indicates that a parity error was detected when a command or parameter was being shifted from the interface to the controller/drive subsystem. The operation is terminated; the ERROR and DONE bits are set.

BIT 0 - CRC - CRC Error

This bit indicates that a CRC (Cyclic Redundancy Check) Error was detected during the last Read sector operation. The operation is terminated; the ERROR and DONE bits are set.

The bit layout of this register is shown in Figure 4-1.
### Table 4-2. Mode 1 Command and Status Register

Format for RXCS Register

<table>
<thead>
<tr>
<th>BIT</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ER — Error detected, cleared by INITIALIZE or new command. Read Only</td>
</tr>
<tr>
<td>14</td>
<td>IN — INITIALIZE the DSD 480. The DONE flag will be negated, the controller will self-test, drive 1 will seek to track 0, drive 0 will seek to track 0. A READ SECTOR operation on drive 0, track 1, sector 1 will occur if a diskette is in place; the ERROR AND STATUS REGISTER will be set to 0, the INITIALIZE DONE bit will be set in the ERROR AND STATUS REGISTER, and if drive 0 is ready, then the DRIVE READY bit will be set in the ERROR AND STATUS REGISTER. The INITIALIZE bit takes precedence over all other bits in the RXCS register.</td>
</tr>
<tr>
<td>13-8</td>
<td>UNUSED</td>
</tr>
<tr>
<td>7</td>
<td>TR — TRANSFER REQUEST indicates to the program that the DATA BUFFER REGISTER has been emptied and needs loading or is loaded and needs emptying. Read only.</td>
</tr>
<tr>
<td>6</td>
<td>IE — INTERRUPT ENABLE permits an interrupt to occur when the DONE flag is set. It is a read/write bit.</td>
</tr>
<tr>
<td>5</td>
<td>DN — DONE flag indicates the completion of an operation. The DONE flag is a read only bit.</td>
</tr>
<tr>
<td>5-4</td>
<td>UN2 UN1 — Diskette drive unit select bits. The binary encoding of these bits selects drive 0-3. Drive selection only occurs if a drive related function is executed. A point of incompatibility exists when a triple or quad drive system is configured. DEC bootstraps assume that bit 5 is a &quot;read only&quot; bit, so they write into it with impunity. As a result, drive 2 is selected by mistake during bootstrapping. In systems configured for single or dual drive operation, bit 5 can be written into with impunity.</td>
</tr>
<tr>
<td>3-1</td>
<td>FN — FUNCTION SELECT</td>
</tr>
<tr>
<td>0-7</td>
<td>Function select bits are write only.</td>
</tr>
<tr>
<td>0</td>
<td>EX — Execute. When set, causes the function coded in RXCS bits 3-1 to be executed.</td>
</tr>
</tbody>
</table>
Figure 4-1. Mode 1 Register Formats
Error Register (RXER)

The RXER is a logical register that is implemented using the RXDB shift register. It contains a definitive code identifying an error condition. The RXER is available only after the "Read Error Register" command (II). At the completion of this command, the controller places the contents of the RXER into the data buffer so that the host processor may read the definitive error code.

Bits 15-8: Not Used
Bits 7-0: Definitive Error Code
Refer to Table 4-3

MODE I PROTOCOLS

Protocols are required in the DSD 480 because the computer interface module and the DSD 480 controller communicate mostly through a single physical I/O register (RXDB). Because of this constraint, the controller must identify parameters being passed to it by the order in which they are transmitted through the register link.

The following sections describe the proper protocol for each of the possible commands that can be sent to the controller. Failure to adhere to the correct protocol will result in lost or incorrect data.

FILL SECTOR BUFFER (000)

The FILL SECTOR BUFFER command is used to fill a storage buffer inside the DSD 480 with 128 eight bit bytes of data from the host processor. Other functions can later be used to either write that data to the diskette, or transfer it back to the processor.

When the FILL SECTOR BUFFER command is given, the DSD 480 responds by clearing the DONE flag, RXCS bit 5. The controller then requests the first byte of data by setting the TRANSFER REQUEST flag, RXCS bit 7. At this time, one byte of data should be written into the lower eight bits of the RXDB register by the host processor. When the processor writes a byte into the RXDB register, the TRANSFER REQUEST flag is cleared.

When the TRANSFER REQUEST flag is again set by the controller, another byte of data is transferred to the RXDB register. This process is repeated until a total of 128 bytes have been transferred. When the controller has the 128 bytes needed to fill the buffer, TRANSFER REQUEST is left clear, and the DONE flag, RXCS bit 5 will be set. If the INTERRUPT ENABLE bit (RXCS bit 6), is set, an interrupt request will occur when the DONE flag is set.

NOTES

1) Data will not be accepted unless the TRANSFER REQUEST flag is set.

2) If the ERROR flag, RXCS bit 15, is set, the specific error must be obtained from the RXER (see READ ERROR REGISTER section).
3) The controller will ignore all data sent after byte 128.

4) Since the FILL BUFFER command is not associated with any one drive, RXCS bit 4 does not affect this function.

Interrupts are generated by the logical "AND" of DONE and INTERRUPT ENABLE. If the DONE bit is set the first time you set the interrupt enable bit you will get a spurious interrupt.

EMPTY SECTOR BUFFER (001)

The EMPTY SECTOR BUFFER function is used to transfer the contents of the sector buffer to the computer. The sector buffer is loaded from a previous FILL SECTOR BUFFER or READ SECTOR command.

When the EMPTY BUFFER command is given, the controller responds by clearing the DONE flag, RXCS bit 5. The controller then sets the TRANSFER REQUEST flag (RXCS bit 7), to indicate that a byte of data is available for reading. The data byte appears in the lower 8 bits of the RXDB data register.

When the host computer reads the byte, the TRANSFER REQUEST flag is cleared. The TRANSFER REQUEST flag is again set when the controller has placed another byte of data in the RXDB register. This process is continued until all 128 bytes have been transferred to the host computer. After the 128 byte of data have been transferred, the TRANSFER REQUEST flag will remain cleared and the DONE flag will be set. An interrupt request will be generated if the INTERRUPT ENABLE bit was set when DONE became true.

NOTES

1) Data will not be accepted unless the TRANSFER REQUEST flag is set.

2) If the ERROR flag, RXCS bit 15, is set, the specific error must be obtained from the RXER (see READ ERROR REGISTER section).

3) The controller will ignore all data sent after byte 128.

4) Since the FILL BUFFER command is not associated with any one drive, RXCS bit 4 does not affect this function.

5) The EMPTY BUFFER function does not modify the contents of the sector buffer.

Interrupts are generated by the logical "AND" of DONE and INTERRUPT ENABLE. If the DONE bit is set the first time you set the interrupt enable bit you will get a spurious interrupt.
WRITE SECTOR (010)

The WRITE SECTOR function is used to transfer the contents of the sector buffer to a specified track and sector of the diskette. When the WRITE SECTOR command is given, the controller clears the logical RXES register and DONE flag.

Next, the controller sets the TRANSFER REQUEST flag, RXCS register bit 7, to request a sector address. The program responds by writing the desired sector address (RXSA) into the data buffer register (RXDB=777172). This clears the TRANSFER REQUEST flag. As soon as the controller shifts the sector address over the interface cable, it asserts TRANSFER REQUEST again. This time the program responds by writing the desired track address (RXTA) into the data buffer register. This clears the TRANSFER REQUEST flag.

After the track address is received, the controller commands the selected drive to seek to the right track and locate the right sector. TRANSFER REQUEST stays unasserted for the remainder of the function.

If the correct track and sector are found, the controller writes the 128 bytes of data from the sector buffer, plus two bytes of Cyclic Redundancy Check (CRC) onto the diskette. When this is finished, the controller completes the function by writing the RXES data to the data buffer register and setting the DONE flag. As in all functions, an interrupt request is generated if the interrupt enable bit (RXCS bit 6), was set when DONE became true.

If the controller is unable to locate the specified diskette track, the RXER is set to a 150. If the specified sector cannot be found within two diskette revolutions, the RXER is set to a 70. Both of these error conditions cause the function to be terminated. The ERROR flag, RXCS bit 15, and the DONE flag, RXCS bit 5 are asserted. As with the error-free termination, an interrupt request will be generated if the interrupt enable bit was set when the DONE flag became true.

NOTES

1) The contents of the sector buffer are not modified by the WRITE SECTOR function.

2) The contents of the sector buffer ARE modified as a result of a power failure and an initialize command. Be sure that valid data is written back into the sector buffer following either of these conditions. This is especially true before executing the WRITE SECTOR command.

3) If the sector number written into the RXSA is 152 (octal) the WRITE SECTOR function becomes a WRITE FORMAT TRACK function.
READ SECTOR (011)

The READ SECTOR function is used to locate a specified track and sector of a diskette and then transfer the contents of the data field into the controller's sector buffer.

When the READ SECTOR command is given, the controller clears the RXES register and the DONE flag. Next, the controller sets the TRANSFER REQUEST flag, RXCS bit 7, to request a sector address. The program responds by writing the desired sector address (RXSA) into the data buffer register which clears the TRANSFER REQUEST flag.

After receiving the track address, the controller causes the selected drive to seek to the desired track and locate the remainder of this function. If the correct track and sector are located, the controller looks for a data address mark (DAM) or a deleted data address mark (DDAM). When a valid mark is found, this marks the beginning of the 128 byte data field on the diskette.

At that point, the following 128 bytes are read from the diskette and stored in the controller data buffer. The two CRC bytes are read immediately after the data field. An error-free read is indicated if the address mark, 128 bytes of data, and two bytes of CRC produce a zero residue when passed sequentially through the CRC checker hardware circuits. As soon as the data is available in the buffer, the controller terminates the function by writing the RXES to the data buffer register and setting the DONE flag. An interrupt request will be generated if the interrupt enable bit, RXCS bit 6, is set when DONE was asserted.

If the deleted data address mark is detected, the controller sets the deleted data flag. This flag appears in the ERROR/STATUS register (RXES bit 6). If a CRC error is detected, the controller sets RXES bit 0 and the ERROR flag (RXCS bit 15) as an indication seek errors and missing sector errors are reported just as in the WRITE SECTOR function.

READ STATUS (101)

The READ STATUS command is used to determine the current status of the drive selected by RXCS bit 4. The status information passed back indicates if the drive is ready.

When the command is issued, the DONE flag is cleared. The controller checks to see that the selected drive's door is closed, a diskette is inserted, and the diskette is up to speed.

The speed is determined by measuring the amount of time between successive index pluses. Since this measurement takes an average of 250 milliseconds, excessive use of the READ STATUS function will cause reduced throughput.

If the drive is ready, the controller sets bit 7 (DRV RDY) of the RXES. The controller terminates this function by shifting the RXES over to the RXDB and setting the DONE flag. An interrupt request will be generated if the interrupt enable bit (RXCS bit 6), was set when DONE became true.
WRITE DELETED DATA SECTOR (110)

This function performs the same task as WRITE SECTOR. The difference is that this command writes a deleted data address mark just before the data field. The standard WRITE SECTOR function writes a regular data address mark. When a sector which was written with a deleted data address mark is read, bit 6 of the RXES is set to reflect this.

READ ERROR REGISTER (111)

When a command terminates because of an error condition, RXCS ERROR (bit 15 of the command and status register), is set. Under these conditions, a code is available in the RXER which can be used to identify the specific error. The READ ERROR REGISTER command is used to access that code. Table 4-2 shows the RXER code meanings.

When the READ ERROR REGISTER command is initiated, the DONE flag is cleared. The controller moves the logical RXER register into the physical data buffer register (RXDB), and signals completion of the transfer by asserting the DONE flag.

NOTE

This is the only command that DOES NOT terminate with the RXES placed in the RXDB. The information contained in the RXER should be read immediately after the ERROR flag (RXCS bit 15) is set. Subsequent commands or an INITIALIZE operation clear the RXER.

STATUS INFORMATION

Status information is usually needed to determine the status of a drive or the cause of an error. To determine drive related status (DRIVE READY), the READ STATUS command should be used. When the ERROR flag (RXCS bit 15), is set following a function, the RXES should be read first. Remember that the logical RXES register is left in the physical RXDB register following all functions EXCEPT the READ ERROR REGISTER function.

As shown in Figure 4-1, the RXES has error bits for CRC ERROR, PARITY ERROR, POWER LOW, and DENSITY ERROR. If no error bits are set in the RXES, the definitive error code can be obtained using the READ ERROR REGISTER command. The code interpretations are shown in Table 4-3.
Table 4-3. Mode I Error Register Codes (RXER)

<table>
<thead>
<tr>
<th>OCTAL CODE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>No error</td>
</tr>
<tr>
<td>010</td>
<td>No drive 0 or drive 0 failed to find track 0 on INIT</td>
</tr>
<tr>
<td>020</td>
<td>No drive 1 when DIP switch indicates there should be a drive 1, or drive 1 failed to find track 0 on INIT</td>
</tr>
<tr>
<td>030</td>
<td>Track 0 found while stepping in on initialize</td>
</tr>
<tr>
<td>040</td>
<td>Track address passed to controller was invalid (76)</td>
</tr>
<tr>
<td>050</td>
<td>Track 0 found before desired track while stepping</td>
</tr>
<tr>
<td>070</td>
<td>Requested sector not found in two revolutions</td>
</tr>
<tr>
<td>100</td>
<td>Write/protect violation</td>
</tr>
<tr>
<td>110</td>
<td>No read data signal present</td>
</tr>
<tr>
<td>120</td>
<td>No preamble found</td>
</tr>
<tr>
<td>130</td>
<td>Preamble found, but no address mark within window</td>
</tr>
<tr>
<td>140</td>
<td>CRC error on what appeared to be a header</td>
</tr>
<tr>
<td>150</td>
<td>Address in good header did not match desired track</td>
</tr>
<tr>
<td>160</td>
<td>Too many tries for an ID address mark</td>
</tr>
<tr>
<td>170</td>
<td>Data address mark not found in allotted time</td>
</tr>
<tr>
<td>175</td>
<td>DEC double density address mark on non-DEC diskette</td>
</tr>
<tr>
<td>200</td>
<td>CRC error on data field; RXES bit 0 also set</td>
</tr>
<tr>
<td>210</td>
<td>Parity error on interface cable; RXES bit 1 also set</td>
</tr>
<tr>
<td>220</td>
<td>Read/write controller failed maintenance mode test</td>
</tr>
<tr>
<td>230</td>
<td>Invalid word count specified</td>
</tr>
<tr>
<td>240</td>
<td>RX02 density error</td>
</tr>
<tr>
<td>245</td>
<td>IBM density error</td>
</tr>
<tr>
<td>250</td>
<td>Wrong key for set media density or format command</td>
</tr>
<tr>
<td>260</td>
<td>Indeterminate density</td>
</tr>
<tr>
<td>265</td>
<td>Diskette not compatible with RX01 on RX02 mode</td>
</tr>
<tr>
<td>270</td>
<td>Read/write controller write-format failure</td>
</tr>
<tr>
<td>320</td>
<td>Read/write controller detected write circuit failure</td>
</tr>
<tr>
<td>330</td>
<td>Read/write controller timed out on reset</td>
</tr>
<tr>
<td>340</td>
<td>Master controller out of SYNC with RD/WRT controller</td>
</tr>
<tr>
<td>350</td>
<td>Non-existent memory error during DMA</td>
</tr>
<tr>
<td>360</td>
<td>Drive not ready during format command</td>
</tr>
<tr>
<td>370</td>
<td>AC power low caused abort of write activity</td>
</tr>
</tbody>
</table>
TYPICAL SEQUENCES OF OPERATIONS

The programming examples shown in Tables 4-4 and 4-5 illustrate how to write routines which successfully manipulate the DSD 480 system.

Table 4-4. Fill / Empty RX01 Sector Buffer Example

<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>177170</td>
<td>RXCS=177170</td>
<td>;CONTROL AND STATUS REGISTER</td>
</tr>
<tr>
<td>177172</td>
<td>RXDB=177172</td>
<td>;DATA BUFFER REGISTER</td>
</tr>
<tr>
<td>01000</td>
<td>012700</td>
<td>READ RX01 SECTOR</td>
</tr>
<tr>
<td>000007</td>
<td></td>
<td>;BUILD READ SECTOR CMD IN RO</td>
</tr>
<tr>
<td>01004</td>
<td>000405</td>
<td>BR SYNTAX</td>
</tr>
<tr>
<td>01006</td>
<td>012700</td>
<td>WRITE RX01 SECTOR ROUTINE</td>
</tr>
<tr>
<td>000005</td>
<td></td>
<td>;BUILD WRITE SECTOR CMD IN RO</td>
</tr>
<tr>
<td>01012</td>
<td>000402</td>
<td>BR SYNTAX</td>
</tr>
<tr>
<td>01014</td>
<td>012700</td>
<td>;WRITE DELETED DATA RX01 SECTOR</td>
</tr>
<tr>
<td>000015</td>
<td></td>
<td>;BUILD WRITE DELETED DATA</td>
</tr>
<tr>
<td>01020</td>
<td>005767</td>
<td>SYNTAX: TST UNIT</td>
</tr>
<tr>
<td>001114</td>
<td></td>
<td>;SECTOR COMMAND IN RO</td>
</tr>
<tr>
<td>01024</td>
<td>001402</td>
<td>BEG 1$</td>
</tr>
<tr>
<td>01026</td>
<td>052700</td>
<td>BIS #20,RO</td>
</tr>
<tr>
<td>000020</td>
<td></td>
<td>;SET UNIT 1</td>
</tr>
<tr>
<td>01032</td>
<td>010037</td>
<td>1$: MOV RO, @#RXCS</td>
</tr>
<tr>
<td>177170</td>
<td></td>
<td>;ISSUE COMMAND TO CONTROLLER</td>
</tr>
<tr>
<td>01036</td>
<td>105737</td>
<td>2$: TSTB @#RXCS</td>
</tr>
<tr>
<td>177170</td>
<td></td>
<td>;WAIT FOR TRANSFER REQUEST</td>
</tr>
<tr>
<td>01042</td>
<td>100375</td>
<td>3$: BPL 2$</td>
</tr>
<tr>
<td>01044</td>
<td>016736</td>
<td>MOV SECTOR, @#RXDB</td>
</tr>
<tr>
<td>000064</td>
<td></td>
<td>;PASS SECTOR TO CONTROLLER</td>
</tr>
<tr>
<td>177172</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01052</td>
<td>105737</td>
<td>3$: TSTB @#RXCS</td>
</tr>
<tr>
<td>177170</td>
<td></td>
<td>;WAIT FOR TRANSFER REQUEST</td>
</tr>
<tr>
<td>01056</td>
<td>100375</td>
<td>4$: BPL 3$</td>
</tr>
<tr>
<td>01060</td>
<td>016737</td>
<td>MOV TRACK, @#RXDB</td>
</tr>
<tr>
<td>000052</td>
<td></td>
<td>;PASS TRACK TO CONTROLLER</td>
</tr>
<tr>
<td>177172</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01066</td>
<td>032737</td>
<td>4$: BIT #100040, @#RXCS</td>
</tr>
<tr>
<td>100040</td>
<td></td>
<td>;TEST FOR DONE_ERROR</td>
</tr>
<tr>
<td>177170</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01072</td>
<td>001774</td>
<td>5$: BEQ 4$</td>
</tr>
<tr>
<td>01076</td>
<td>100401</td>
<td>BMI ERFIN</td>
</tr>
<tr>
<td>01100</td>
<td>000207</td>
<td>RTS PC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>;ERROR BIT SET?</td>
</tr>
<tr>
<td></td>
<td></td>
<td>;RETURN TO CALLING ROUTINE</td>
</tr>
</tbody>
</table>

4-17
Table 4-4. Fill / Empty RX01 Sector Buffer Example
(continued)

01102 013767 ERFIN: MOV @#RXDB,GENSTT ;SAVE GENERAL STATUS
     177172
     000032
01110 012737 MOV #17,##RXCS ;REQUEST DEFINITIVE STATUS
     000017
     177170
01116 105737 5$: TSTB @#RXCS ;LOOK FOR DONE FLAG
     177170
01122 001775 MOV @#RXDB,RO ;SAVE DEFINITIVE STATUS IN RO
     177172
01124 013700 5$: TSTB @#RXCS ;LOOK FOR DONE FLAG
01130 000261 BEQ 5$ ;RETURN TO CALLING ROUTINE
     177170
01132 000207 MOV @#RXDB,RO ;LEAVE DEFINITIVE STATUS IN RO
01136 000001 SEC ;CARRY SET TO INDICATE ERROR
     177170
01140 000000 RTS PC ;RETURN TO CALLING ROUTINE
01142 000000 UNIT: .WORD 0 ;DRIVE 0 = DRIVE 1
01146 000000 SECTOR: .WORD 1 ;DESired SECTOR ADDRESS
01150 000000 TRACK: .WORD 1 ;DESired TRACK ADDRESS
01154 000000 GENSTT: .WORD 0 ;GENERAL STATUS VARIABLE
| RXCS=177170; CONTROL AND STATUS REGISTER |
| RXDB=177172; DATA BUFFER REGISTER |

<table>
<thead>
<tr>
<th>READ RX01 SECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>01000 12700 READ: MOV #7, RO</td>
</tr>
<tr>
<td>000007</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WRITE RX01 SECTOR ROUTINE</th>
</tr>
</thead>
<tbody>
<tr>
<td>01006 12700 WRITE: MOV #5, RO</td>
</tr>
<tr>
<td>000005</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WRITE DELETED DATA RX01 SECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>01014 12700 WRTDD: MOV #15, RO</td>
</tr>
<tr>
<td>000015</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WRITE COMMAND IN RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>01020 005767 SYNTAX; TST UNIT</td>
</tr>
<tr>
<td>000114</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>UNIT 0 OR UNIT 1?</th>
</tr>
</thead>
<tbody>
<tr>
<td>01024 001402 BEG 1$</td>
</tr>
<tr>
<td>01026 052700 BIS #20, RO</td>
</tr>
<tr>
<td>00020</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ISSUE COMMAND TO CONTROLLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>01032 010037 1$: MOV RO, R RXCS</td>
</tr>
<tr>
<td>177170</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WAIT FOR TRANSFER REQUEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>01036 105737 2$: TSTB RXCS</td>
</tr>
<tr>
<td>177170</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PASS TRACK TO CONTROLLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>01060 016737 MOV TRACK, RXDB</td>
</tr>
<tr>
<td>000052</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TEST FOR DONE AND ERROR</th>
</tr>
</thead>
<tbody>
<tr>
<td>01066 032737 4$: BIT #100040, RXCS</td>
</tr>
<tr>
<td>100040</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ERROR BIT SET?</th>
</tr>
</thead>
<tbody>
<tr>
<td>01074 001774 BEQ 4$</td>
</tr>
<tr>
<td>01076 100401 BMI ERFIN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RETURN TO CALLING ROUTINE</th>
</tr>
</thead>
<tbody>
<tr>
<td>01100 000207 RTS PC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SAVE GENERAL STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>01102 013767 ERFIN; MOV RXDB, GENSTT</td>
</tr>
<tr>
<td>177172</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>REQUEST DEFINITIVE STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>01110 012737 MOV #17, RXCS</td>
</tr>
<tr>
<td>000017</td>
</tr>
</tbody>
</table>

4-19
Table 4-5. Read / Write / Write Deleted Data RX01 Sector Example
(continued)

01116 105737 5$: TSTB @#RXCS ;LOOK FOR DONE FLAG
177170
01122 001775 BEQ 5$
01124 013700 MOV @#RXDB, RO ;LEAVE DEFINITIVE STATUS IN RO
177172
01130 000261 SEC ;CARRY FLAG SET INDICATES ERROR
01132 000207 RTS PC ;RETURN TO CALLING ROUTINE
;
01134 000001 SECTOR: .WORD 1 ;DESIRED SECTOR ADDRESS
01136 000001 TRACK: .WORD 1 ;DESIRED TRACK ADDRESS
01140 000000 UNIT: .WORD 0 ;UNIT - 0=DRIVE 0, 1=DRIVE 1
01142 000000 GENSTT: .WORD 0 ;GENERAL STATUS VARIABLE

COMMON PROGRAMMING MISTAKES

This section illustrates common programming mistakes that can cause data loss and/or error indications.

1) An illegal track or sector address is sent to the controller.
   A. Valid sectors are 1-26 (decimal).
      (There is no sector 0)
   B. Valid tracks are 0-76 (decimal).

2) The READ STATUS command requires up to two revolutions of the disk to complete. To avoid excessive delays, use this command only when necessary.

3) After reading or writing, the INITIALIZE DONE bit (RXES bit 2) may be checked for indication of power failure. A short power outage causes DONE to set without any error indication even though invalid data may have been read or written.

4) The drive select bit, RXCS bit 4 is not scanned by the controller during FILL BUFFER and EMPTY BUFFER functions.

5) A two-way-sector interleave should be used for maximal throughput when using a DMA interface. A three way interleave is desirable when using programmed transfer.

A FILL BUFFER command usually precedes a WRITE SECTOR command. Similarly, a READ SECTOR command precedes an EMPTY BUFFER command.

Interrupts

An interrupt is requested by the interface module whenever the INTERRUPT ENABLE and DONE bits of the physical command and status register, RXCS, both become set. Only a single interrupt can occur per request. The standard interrupt sector address location is 264.
MODE 2 (RX02 COMPATIBLE) OPERATION

The system assumes MODE 2 operation when rocker #4 on the controller module DIP-switch is placed in the closed position. The system operates only according to MODE 2 protocol when connected to an interface module capable of DMA. Any program that runs with the DEC RX211 (or RXV211) runs successfully on a DSD 480 system configured for operation in MODE 2.

PERIPHERAL DEVICE REGISTERS

Programs communicate with the DSD 480 through two peripheral device registers:

<table>
<thead>
<tr>
<th>NAME</th>
<th>DESCRIPTION</th>
<th>OCTAL LOCATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX2CS</td>
<td>COMMAND AND STATUS REGISTER</td>
<td>177170</td>
</tr>
<tr>
<td>RX2DB</td>
<td>DATA BUFFER REGISTER</td>
<td>177172</td>
</tr>
</tbody>
</table>

Peripheral device registers reside in the top 4K words of DEC-II family computers' memory address space. They are addressed as memory and any instruction that operates on a memory location can operate on a peripheral device register in the same way.

COMMAND AND STATUS REGISTER (RX2CS)

Writing the bits of this physical register controls the DSD 480. The format for this register is shown in Figure 4-2. The RX2CS register also provides important status information and error indications when read by the user program.

BIT 15 - ER - Error detected, cleared by INITIALIZE or the issuance of a new command. Read Only bit.

BIT 14 - IN - INITIALIZE the DSD 480

The DONE flag is negated, the controller resets some internal variables, and then executes the self-test microcode. The disk drives are homed to track 0.

If the controller is configured in "NORMAL" mode, the controller reads track 1 sector 1 of the diskette in drive 0. When the READ SECTOR function is attempted, the INITIALIZE DONE bit in the error/status register is set. If there was a readable diskette in drive 0, the DRIVE READY bit is also set. If the diskette is in double density, then the drive density bit is set. The DONE flag is set when the controller has completed the Initialization sequence. The INITIALIZE bit takes precedence over all other bits in this register. Bit 14 is a Write Only bit.

BIT 13 - A17 - Extended Address Bit 17

This write only bit is asserted on UNIBUS or Q-BUS address line 17 when the DSD 480 is transferring data via direct memory access. This bit is cleared by an INITIALIZE. A17 will toggle if A01-A16 are all ones and the bus address register is incremented by the logic.
BIT 12 - A16 - Extended Address Bit 16

This write only bit is asserted on UNIBUS or Q-BUS address line 16 when the DSD 480 is transferring data via direct memory access. This bit is cleared by an INITIALIZE. A16 will toggle if A01-A15 are all ones and the bus address register is incremented by the logic.

BIT 11 - RX02 System Identification Bit

This read only bit provides an easy way for software to differentiate RX01 systems from RX02 systems.

BIT 10 - Reserved for Possible Future Use

BIT 9 - HS - Head Select Bit

This read/write bit selects side 0 or side 1 (lower head or upper head). It is set to select side 1, and cleared to select side 0.

BIT 8 - DEN - Density of Function

This read/write bit specifies the density of the function encoded in bits 1-3. High density is specified when this bit is set.

NOTE

Even though the FILL BUFFER and EMPTY BUFFER functions do not involve magnetic media, a valid density bit is required so that the controller can evaluate the validity of the word count parameter.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| ER | IN | A17 | A16 | RX02 | HS | DEN | TR | IE | DN | UNI | FN | FN | FN | EX |

Figure 4-2. Mode 2 Command and Status Register Format

4-22
BIT 7 - TR - TRANSFER REQUEST Flag

This read only bit indicates to the program that the DATA BUFFER REGISTER is empty and needs loading, or is loaded and needs emptying.

BIT 6 - IE - INTERRUPT ENABLE Bit

This read/write bit, when set, allows an interrupt to be generated whenever the DONE flag is set.

BIT 5 - DN - DONE Flag Indicates the Completion of an Operation

This read only bit works in conjunction with the interrupt enable bit to generate interrupts.

BIT 4 - UNI - Drive Unit Select Bit

The binary encoding of this read/write bit selects drive 0-1. Drive selection only occurs if a drive related function is executed.

BITS 3-1 - FN - FUNCTION SELECT

The binary encoding of these write only bits selects the function to be performed by the DSD 480 system.

<table>
<thead>
<tr>
<th>BINARY</th>
<th>OCTAL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
<td>FILL BUFFER</td>
</tr>
<tr>
<td>001</td>
<td>1</td>
<td>EMPTY BUFFER</td>
</tr>
<tr>
<td>010</td>
<td>2</td>
<td>WRITE SECTOR/FORMAT</td>
</tr>
<tr>
<td>011</td>
<td>3</td>
<td>READ SECTOR</td>
</tr>
<tr>
<td>100</td>
<td>4</td>
<td>SET MEDIA DENSITY</td>
</tr>
<tr>
<td>101</td>
<td>5</td>
<td>READ STATUS</td>
</tr>
<tr>
<td>110</td>
<td>6</td>
<td>WRITE DELETED DATA SECTOR</td>
</tr>
<tr>
<td>111</td>
<td>7</td>
<td>READ ERROR CODE</td>
</tr>
</tbody>
</table>

BIT 0 - EX - Execute the function encoded in bits 3-1 of this register. This is a write only bit.

DATA BUFFER REGISTER (RX2DB)

The RX2DB is physically a shift register that provides the communication link between the host processor and the DSD 480 system. The logical register information passed through is based upon a predetermined protocol.

If the DSD 480 is not in the process of executing a command, the RX2DB is written without risk of adverse effects. However, during the execution of an instruction, the RX2DB register provides or accepts information (according to the RX2DB protocol) when the TRANSFER REQUEST flag is set.
CAUTION

Data may be lost if the correct protocol is not followed.

The following descriptions explain the various logical register formats of the physical Data Register (or RX2DB).

Data Buffer (RX2DB)

The data buffer register is used by the function in process to transfer data to and from the disk controller data buffer. All information is transferred as a byte through bits 0-7 of the RXDB.

Disk Track Address (RX2TA)

During commands such as WRITE SECTOR and READ SECTOR, which require a track number -- or a cylinder number, during double sided operation -- this number is written into the physical RX2DB register as if it were a logical register. This is the Track Address Register (RX2TA = 777172). Track or cylinder numbers from 0 to 76 (decimal) are valid.

Disk Sector Address (RX2SA)

During commands such as WRITE SECTOR and READ SECTOR, which require a sector address, this address is written into the physical RX2DB register as if it were a logical register. This is the Sector Address Register (RX2SA = 777172). For sectors of fixed length, addresses from 1 to 26 are valid. The range of valid variable length sector addresses may be different. Bits 6 and 7 of RX2SA are masked to zero.

Word Count Register (RX2WC)

The Word Count Register specifies the number of words to be transferred between the controller sector buffer and main memory via Direct Memory Access (DMA). For a fixed length double density sector, the maximum word count is 128 (decimal), or 256 bytes. For a fixed length single density sector, the maximum word count is 64 (decimal), or 128 words. For variable length sectors, the maximum word count may be different.

If each case, the programmer loads the actual word count -- not the 2's complement of the word count -- into the Word Count Register.

Bus Address Register (RX2BA)

This register specifies the bus address to which data is to be transferred during any DMA operation. It is a 16 bit counter on the DSD 480 interface module for the PDP-11 and LSI-11. It increments by two following each data transfer.
The bus address register cannot be read. It should always be loaded with the starting address of a data buffer in memory at the appropriate time during the FILL BUFFER, EMPTY BUFFER, or READ EXTENDED STATUS functions. If you try to load bit 0 with a 1 it will be ignored.

**System Error and Status Register (RX2ES)**

The RX2ES register is another logical register that is implemented using the physical RX2DB shift register. It provides status and error information about the drive that is selected by bit 4 of the physical RX2CS register. At the completion of a command, the controller places the RX2ES register into the data buffer register (RX2DB = 777172) so that the host processor can check the most recent operation. When the controller completes a function which did not actually select a drive (e.g. FILL BUFFER, EMPTY BUFFER), the RX2ES "UNIT SEL" bit and "DRV DEN" bit remains unmodified. All the other RX2ES bits are cleared at the initiation of each new function. See Figure 4-3 for the bit layout of this register.

**BITS 15, 14**

**NOTE**

Bits 13 through 15 of the RXZES are not defined or used by the RX02. When the DSD 480 is used in a pure RX02 emulation, these bits will have no significance. In Mode 2, the DSD 480 defines these bits to provide diskette format information.

**Sector Size**

Only valid during read status function (101)

These bits are set during an IBM Mode read maintenance function to indicate the sector size of diskette in specified unit.

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Sectors/Track</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>26 Sector/Track</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>15 Sectors/Track</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>8 Sectors/Track</td>
</tr>
</tbody>
</table>

**NOTE**

The sector size indicates the size of cylinders 1 to 76 not cylinder 0. On IBM diskettes, track always has 26 sectors/track.
BIT 13: IBM Double Density

Only valid during read status function (101)

Set during maintenance status to indicate that selected drive contains an IBM 2D diskette.

NOTE

Bits 15, 14, 13, 5 specify the type of diskette in selected drive in read status function.

<table>
<thead>
<tr>
<th>Bit</th>
<th>IBM DEC Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

BIT 12- Not used/reserved.

BIT 11 - NXM - Non-Existent Memory Error

This bit is set if during a DMA cycle the interface does not receive a bus reply when it tries to write/read a word to or from memory. Usually this means the address in the RX2BA or the extended address bits in the RX2CS are invalid. The operation is terminated; the error and done bits are set. To recover from this error condition, generate either a bus INIT or a programmed INIT.

BIT 10 - WC OVFL - Word Count Overflow

This bit is set if the word count specified during a fill or empty buffer command is too large for the sector size indicated by the density bit. The operation is terminated; the Error and Done bits are set.

BIT 9 - HD SEL- Head Selected

This bit indicates the read/write head selected during the immediately preceding read or write operation. It is set to indicate the upper head, and cleared to indicate the lower head.

BIT 8 - UNIT SEL - Unit Select

This bit indicates the disk drive selected during the immediately preceding read or write operation. It is set to indicate drive 1, and cleared to indicate drive 0.
BIT 7 - DRV RDY - Drive Ready

This bit, when set, indicates that the selected disk drive has a diskette correctly installed and up to speed. The Drive Ready bit is valid immediately following the Read Status function. This bit is also valid for drive 0 immediately following an initialization.
Figure 4-3. Mode 2 Register Formats
BIT 6 - DD - Deleted Data

This bit indicates that a deleted data address mark was found during the last Read Sector operation or that the last command was Write Deleted Data Sector.

BIT 5 - DR V DEN - Drive Density

This bit indicates the density of the diskette installed in the drive indicated by bit 8. It is updated during read or write sector operations.

BIT 4 - DEN ERR - Density Error

This bit indicates that during a READ SECTOR, WRITE SECTOR, WRITE DELETED DATA SECTOR, OR READ STATUS operation the diskette density did not match the density bit of the RX2CS. Any operation is terminated; ERROR and DONE bits are set.

BIT 3 - PWR LO - Power Low

This bit indicates a power failure in the controller/drive subsystem. It will also be set if the interface cable becomes disconnected. Any operation is terminated; the ERROR and DONE bits are set.

BIT 2 - ID - Initialize Done

This bit indicates that the controller/drive subsystem has just completed an initialization sequence. This sequence may have been started by a power failure, bus INIT, or programmed INIT.

BIT 1 - SD1 RDY - Side 1 Ready

Bit 1 and bit 7 are both set when a double sided diskette is correctly installed and up to speed. When bit 7 is set but bit 1 is not set, a single sided diskette is installed. A single-sided diskette is restricted to side 0 functions only.

BIT 0 - CRC - Cyclic Redundancy Check Error

This bit indicates that a cyclic redundancy error was detected during the last Read Sector operation. The operation is terminated; the ERROR and DONE bits are set.

MODE 2 PROTOCOLS

Protocols are required in the DSD 480 because the computer interface module and the intelligent portion of the DSD 480 are connected by a single serial data link. Therefore, the controller must identify parameters based on the order in which they are transmitted across the data link.

The following sections describe the protocol for each command that can be sent to the controller. Failure to adhere to the correct protocol results in lost or incorrect data.
FILL SECTOR BUFFER (000)

The FILL SECTOR BUFFER command is used to fill a storage buffer inside the DSD 480 with data from computer memory. Other functions can be used later to write that data to the diskette, or transfer it back to memory.

When the FILL SECTOR BUFFER command is given, the DSD 480 responds by clearing the DONE flag, RX2CS bit 5. The controller then requests a word count by setting the TRANSFER REQUEST flag. The program should respond by writing a valid RX2WC into the RX2DB. When TRANSFER REQUEST is again asserted by the controller, the program should respond by writing a valid starting memory address (RX2BA) into the RX2DB.

As soon as the RX2BA is loaded, TRANSFER REQUEST is cleared and remains cleared for the duration of this function. The data bytes are now transferred directly from memory to the controller sector buffer. When the word count is decremented to zero and the controller has zero-filled the remainder of the sector buffer (if necessary), DONE is asserted. An interrupt request is generated if the interrupt enable bit, RX2CS bit 6, was set when DONE become true. The RX2ES register will be found in the RX2DB at the completion of the function.

NOTE

1) Bit 4 of the RX2CS does not affect this function since no disk drives need be selected.

2) The DENSITY bit, RX2CS bit 8, must be correctly set since this bit is used by the controller in evaluating the validity of the word count.

EMPTY SECTOR BUFFER (001)

The EMPTY SECTOR BUFFER function is used to transfer the contents of the sector buffer to main memory. The sector buffer is loaded from a previous FILL SECTOR BUFFER or READ SECTOR command.

When the EMPTY SECTOR BUFFER command is given, the controller responds by clearing the DONE flag (RX2CS bit 5). The controller then sets the TRANSFER REQUEST flag (RX2CS bit 7) to request the word count register. The program should respond by loading a valid word count into the data buffer register.

When TRANSFER REQUEST is asserted again, the program responds by loading the starting memory address into the data buffer register. When this is done, the controller clears the TRANSFER REQUEST flag and it remains clear for the rest of the operation.

The data in the sector buffer is transferred to memory one word at a time until the word count is decremented to zero. When the data has been transferred, the controller places the RX2ES into the data buffer register and sets the DONE flag. If the interrupt enable bit is set, an interrupt request is initiated when DONE becomes true.
The notes above that apply to the FILL BUFFER command apply equally to the EMPTY SECTOR BUFFER command. In addition, note that the EMPTY BUFFER function does not modify the contents of the sector buffer.

WRITE SECTOR (010) (Bit 9 selects side 0/side 1)

The WRITE SECTOR function is used to transfer the contents of the sector buffer to a specified track and sector of the diskette.

When the WRITE SECTOR command is given, the controller clears the logical RX2ES register and the DONE flag. Next, the controller sets the TRANSFER REQUEST flag, RX2CS register bit 7, to request a sector address. The program responds by writing the desired sector address. The program responds by writing the desired sector address (RX2SA) into the data buffer register. This clears the TRANSFER REQUEST flag. As soon as the controller shifts the sector address over the interface cable, it asserts TRANSFER REQUEST again. This time the program responds by writing the desired track address (RX2TA) into the data buffer register. This clears the TRANSFER REQUEST flag.

After the track address is received, the controller causes the selected drive to seek the desired track. TRANSFER REQUEST is left reset for the remainder of the function. The heads of the selected drive are positioned over the specified track and are loaded against the media. If the controller does not know the density and format of the media, it determines density and format by reading a random sector.

If media density does not agree with the command density (RX2CS bit 8), the operation is terminated. Bit 4 of the RX2ES register indicates a density error. If the densities agree, the controller checks the track address and looks for the specified sector address. If the correct track and sector are found, the controller writes either 128 bytes of single density data or 256 bytes of double density data from the sector buffer to the diskette. Two CRC bytes are written immediately after the data.

If the controller is unable to locate the specified diskette track, the RX2ER is set to a 150. If the specified sector cannot be found within two diskette revolutions, the RX2ER will be set to a 70. These error conditions, and the density error, cause the function to be terminated. The ERROR flag, RX2CS bit 15, and the DONE flag, RX2CS bit 5 are asserted when the function completes in this way. As with the error-free termination, an interrupt request is generated if the interrupt enable bit was set when the DONE flag became true.

NOTES

1) The contents of the sector buffer are not modified by the WRITE SECTOR function.

2) If the contents of the sector buffer are modified as a result of a power failure or the initialize command, programmers must be sure that valid data is written back into the sector buffer following either of these conditions. This is especially true before executing the WRITE SECTOR command.
3) Sector numbers 152 through 157 and 160 through 162 transform the WRITE SECTOR function turns into a WRITE FORMAT TRACK function. Refer to "FORMAT" section of this chapter for details.

**READ SECTOR (011)** (Bit 9 selects side 0/side 1)

The READ SECTOR function is used to locate a specified track and sector of a diskette and then transfer the contents of the data field into the controller's sector buffer.

During Mode 2 operation, the controller clears the logical RX2ES register and the DONE flag when the READ SECTOR command is given. Next, the controller sets the TRANSFER REQUEST flag (RX2CS bit 7) to request a sector address. The program responds by writing the desired sector address (RX2SA) into the data buffer register (RX2DB=777172). This clears the TRANSFER REQUEST a second time. The program responds by writing the desired track address (RX2TA) into the data buffer register which clears the TRANSFER REQUEST flag.

After receiving the track address, the controller causes the selected drive to seek to the desired track. TRANSFER REQUEST is left reset for the remainder of this function. The controller loads the heads against the media and determines the density of the media if it is not already known. If the diskette density does not agree with the command density (RX2CS bit 8), an error is reported and the function is terminated. If the densities agree, the controller looks for the specified sector. When the right sector is located, the controller looks for the appropriate data, or deleted data address mark. When the mark is found, the controller transfers the following 128 (or 256) bytes into the sector buffer. The two CRC bytes are read immediately after the data field. An error-free read is indicated if the address mark, data bytes, and two bytes of CRC check bytes produce a zero residue when passed sequentially through the CRC checker hardware circuits. As soon as the data is available in the buffer, the controller terminates the function by writing the RX2ES to the data buffer register and setting the DONE flag. An interrupt request is generated if the interrupt enable bit was set when DONE became true.

If the deleted data address mark was detected, the controller will set the deleted data flag. This flag appears in the ERROR/STATUS register (RX2ES bit 6). If a CRC error is detected, the controller will set RX2ES bit 0 and the ERROR flag (RX2CS bit 15). Seek errors and missing sector errors are reported just as in the WRITE SECTOR function.

**SET MEDIA DENSITY (100)**

This command is used to initialize an entire DEC-formatted diskette to some specified density. When the SET MEDIA DENSITY command is executed, the controller attempts to write zeroes in every field on the diskette. Bit 8 of the RX2CS determines the recording density and the type of Data Address Mark to be written in each data field. No sector headers are written when the SET MEDIA DENSITY command is executed.

4-32
FUNCTION PROTOCOL

When the command is received, the controller clears the DONE flag and the logical RX2ES register. Next, the controller sets the TRANSFER REQUEST flag. The program responds by writing a "key byte" into the physical RX2DB. If the key byte is an ASCII "I" or 111 octal, the SET MEDIA DENSITY function is executed. If the byte written into the RX2DB is not an "I", the DONE and ERROR flags are set and the operation terminates. The error register is loaded with a 250 to indicate an invalid key. The purpose of the key is to make it difficult to erase all of the data on a diskette.

As soon as the safety character "I" is received, the controller moves the heads to track 0. When sector 1 is found, the controller starts writing. If bit 8 of the RX2CS was a 0, a single density Data Address Mark and 128 FM zeroes are written. If bit 8 of the RX2CS was a 1, a double density Data Address Mark and 256 DEC MFM zeroes are written. After writing all 26 sectors on track 0, the controller seeks to track 1, 2, ... writing all 26 sectors on each track. This continues until either every sector has been written through track 76: sector 26, or a bad header is found. The ERROR and DONE flags are set if the operation terminates due to a bad header.

The SET MEDIA DENSITY function takes about 26 seconds, depending on the sector interleave. It should never be interrupted before it is done. If the function does not terminate normally, an illegal diskette which has Data Address marks of both densities may have been created. If this happens, the diskette should be completely rewritten. If the SET MEDIA DENSITY function is not complete because of an unreadable header, the TRACK FORMAT procedure can be used to rewrite the incorrect header information.

READ STATUS (101)

The READ STATUS command is used to determine the current status of the drive selected by RX2CS bit 4. The status information passed back is: 1) drive readiness, and 2) the density of the diskette currently in the drive.

When the command is issued, the DONE flag is cleared. The controller checks the selected drive's door is closed, a diskette is inserted, and that the diskette is up to speed. Diskette speed is determined by measuring the amount of time between successive index pulses. Since this measurement takes an average of 250 milliseconds, excessive use of the READ STATUS function will cause reduced throughput. If the drive is ready, the controller sets bit 7 (DRIVE READY) of the RX2ES. Next, the controller loads the heads and reads the first sector it finds. The diskette density and format are determined and encoded into bits 13, 14, and 15 of the RX2ES. Refer to System Error and Status Register for description.

If a double density address mark is detected, bit 5 (DRV DEN) of the RX2ES is set. If a single density mark is found, bit 5 is cleared. The controller terminates the function by shifting the RX2ES over to the RX2DB and setting the DONE flag. An interrupt request is generated if the interrupt enable bit, RX2CS bit 6, was set when DONE become true.
WRITE DELETED DATA SECTOR (110)

This function performs the same task as WRITE SECTOR except it writes a deleted data address mark just before the data field. The standard WRITE SECTOR function writes a regular data address mark. When a sector written with a deleted data address mark is read, bit 6 of the logical RX2ES register is set. The density bit associated with this function (RX2CS bit 8) determines whether a single or double density deleted data address mark is written.

READ EXTENDED STATUS (111)

The READ EXTENDED STATUS command is used to retrieve a number of internal controller registers, including the error register. These registers are transferred to memory using direct memory access. As soon as the command is loaded into the RX2CS, the DONE flag goes false. The controller then asserts the TRANSFER REQUEST flag.

The program then loads a starting memory address into the RX2DB. The controller transfers 4 words directly to memory beginning with the specified address. When the words are in memory, the controller asserts DONE. This generates an interrupt request if interrupt enable had been previously set.

The words transferred to memory are as follows:

<table>
<thead>
<tr>
<th>WORD 1 - LO BYTE</th>
<th>DEFINITIVE ERROR CODE (SEE TABLE 4-6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>WORD 1 - HI BYTE</td>
<td>WORD COUNT REGISTER</td>
</tr>
<tr>
<td>WORD 2 - LO BYTE</td>
<td>CURRENT TRACK ADDRESS OF DRIVE 0</td>
</tr>
<tr>
<td>WORD 2 - HI BYTE</td>
<td>CURRENT TRACK ADDRESS OF DRIVE 1</td>
</tr>
<tr>
<td>WORD 3 - LO BYTE</td>
<td>TARGET TRACK OF CURRENT DISK ACCESS</td>
</tr>
<tr>
<td>WORD 3 - HI BYTE</td>
<td>TARGET SECTOR OF CURRENT DISK ACCESS</td>
</tr>
<tr>
<td>WORD 4 - BIT 0</td>
<td>DENSITY OF READ ERROR REGISTER COMMAND</td>
</tr>
<tr>
<td>WORD 4 - BIT 4</td>
<td>DRIVE DENSITY OF DRIVE 0</td>
</tr>
<tr>
<td>WORD 4 - BIT 5</td>
<td>HEAD LOAD BIT</td>
</tr>
<tr>
<td>WORD 4 - BIT 6</td>
<td>DRIVE DENSITY OF DRIVE 1</td>
</tr>
<tr>
<td>WORD 4 - BIT 7</td>
<td>UNIT SELECT BIT</td>
</tr>
<tr>
<td>WORD 4 - HI BYTE</td>
<td>TRACK ADDRESS OF SELECTED DRIVE</td>
</tr>
</tbody>
</table>
Table 4-6. Modes 2 and 3 Definitive Error Codes

<table>
<thead>
<tr>
<th>OCTAL CODE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>No error</td>
</tr>
<tr>
<td>010</td>
<td>No drive 0 or drive 0 failed to find track 0 on INIT</td>
</tr>
<tr>
<td>020</td>
<td>No drive 1 when DIP switch indicates there should be a drive 1, or drive 1 failed to find track 0 on INIT</td>
</tr>
<tr>
<td>030</td>
<td>Track 0 found while stepping in on initialize</td>
</tr>
<tr>
<td>040</td>
<td>Track address passed to controller was invalid (&gt;76)</td>
</tr>
<tr>
<td>050</td>
<td>Track 0 found before desired track while stepping</td>
</tr>
<tr>
<td>070</td>
<td>Requested sector not found in two revolutions</td>
</tr>
<tr>
<td>075</td>
<td>Too many bad headers on &quot;IBM 2D&quot; diskette</td>
</tr>
<tr>
<td>100</td>
<td>Write protect violation</td>
</tr>
<tr>
<td>110</td>
<td>No read data signal present</td>
</tr>
<tr>
<td>120</td>
<td>No preamble found</td>
</tr>
<tr>
<td>130</td>
<td>Preamble found, but no address mark within window</td>
</tr>
<tr>
<td>140</td>
<td>CRC error on what appeared to be a header</td>
</tr>
<tr>
<td>150</td>
<td>Address in good header did not match desired track</td>
</tr>
<tr>
<td>160</td>
<td>Too many tries for an ID address mark</td>
</tr>
<tr>
<td>170</td>
<td>Data address mark not found in allotted time</td>
</tr>
<tr>
<td>175</td>
<td>DEC double density address mark on non-DEC diskette</td>
</tr>
<tr>
<td>200</td>
<td>CRC error on data field; RXES bit 0 also set</td>
</tr>
<tr>
<td>210</td>
<td>Parity error on interface cable; RXES bit 1 also set</td>
</tr>
<tr>
<td>220</td>
<td>Read/write controller failed maintenance mode test</td>
</tr>
<tr>
<td>230</td>
<td>Invalid word count specified (Mode 2 only)</td>
</tr>
<tr>
<td>235</td>
<td>Word count error during FILL or EMPTY BUFFER (Mode 3 only)</td>
</tr>
<tr>
<td>240</td>
<td>Density error; DEC format</td>
</tr>
<tr>
<td>245</td>
<td>Density error; IBM format</td>
</tr>
<tr>
<td>250</td>
<td>Wrong key for set media density or format command</td>
</tr>
<tr>
<td>255</td>
<td>Incorrect &quot;sector size identifier&quot; used in RXISA</td>
</tr>
<tr>
<td>260</td>
<td>Indeterminate density, or no diskette present</td>
</tr>
<tr>
<td>265</td>
<td>Diskette not compatible with RX01 on RX02 mode</td>
</tr>
<tr>
<td>270</td>
<td>Read/write controller write-format failure</td>
</tr>
<tr>
<td>320</td>
<td>Read/write controller detected write circuit failure</td>
</tr>
<tr>
<td>330</td>
<td>Read/write controller timed out on reset</td>
</tr>
<tr>
<td>340</td>
<td>Master controller out of SYNC with RD/WRT controller</td>
</tr>
<tr>
<td>350</td>
<td>Non-existent memory error during DMA</td>
</tr>
<tr>
<td>360</td>
<td>Drive not ready during format command</td>
</tr>
<tr>
<td>370</td>
<td>AC power low caused abort of write activity</td>
</tr>
</tbody>
</table>
TYPICAL SEQUENCE OF OPERATIONS

The programming examples shown in Tables 4-7 and 4-8 illustrate how to write routines which will manipulate the DSD 480 Flexible Disk System in Mode 2 operation (RX02 compatible).

NOTE

These examples will not execute a DMA to or from extended memory.

Table 4-7. Fill / Empty RX02 Sector Buffer Example

;PROGRAMMING EXAMPLE
;FILL / EMPTY RX02 SECTOR BUFFER
;
177170 RXCS=177170 ;CONTROL-STATUS REGISTER
177172 RXDB=177172 ;DATA BUFFER REGISTER
;
;EMPTY RX02 SECTOR BUFFER
00000 012700 EMPBUF: MOV #3, RO ;BUILD EMPBUF COMMAND IN RO
00003
00004 000402 BR FNCENT
;
00006 012700 FILBUF: MOV #1, RO ;FILL RX02 SECTOR BUFFER ROUTINE
00001
00012 005737 FNCENT: TST UNIT ;UNIT 0 OR UNIT 1?
000154'
00016 001402 BEG 1$ ;SET UNIT
00020 052700 BIS #20, RO
00023
00024 005737 1$: TST DEN ;HIGH OR LOW DENSITY?
00027
00030 001402 BEQ 2$ ;SPECIFY HIGH DENSITY
00032 052700 BIS #400,RO
00035
00036 010037 2$: MOV RO,@#RXCS ;ISSUE COMMAND TO CONTROLLER
177170
00042 105737 3$: TSTB @#RXCS ;WAIT FOR TRANSFER REQUEST
177170
00046 100375 BPL 3$ ;PASS WORDCOUNT TO CONTROLLER
00050 013737 MOV WRDCNT,@#RXDB
00053
177172
00056 105737 4$: TSTB @#RXCS ;WAIT FOR TRANSFER REQUEST
177170
00062 100375 BPL 4$
Table 4-7. Fill / Empty RX02 Sector Buffer Example
(continued)

```
00064 013737        MOV BUFA DR,$RXDB        ;PASS BUS ADDRESS TO CONTROLLER
  000152'        177172
00072 032737        BIT #1 00040,$RXCS        ;TEST FOR DONE AND ERROR
       100040
         177170
00100 001774        BEQ 5$
00102 100401        BMI ERFIN        ;ERROR BIT SET?
00104 000207        RTS PC
00106 012737        ERFIN: MOV #17,$RXCS        ;GET DEFINITIVE STATUS
  000017
  177170
00114 105737        TSTB #$RXCS        ;WAIT FOR TRANSFER REQUEST
       177170
00120 100375        BPL 6$
00122 012737        MOV #ERBUF,$RXDB        ;SEND ERROR BUFFER ADDRESS
       00156'
         177172
00130 032737        7$: BIT #40,$RXCS        ;WAIT FOR DONE BIT
       000040
         177170
00136 001774        BEQ 7$
00140 113700        MOVB #$ERBUF,RO        ;LEAVE ERROR REGISTER IN RO
  000156'
00144 000000        HALT
00146 000000        DEN: .WORD 0        ;DENSITY - 0=SINGLE 1=DOUBLE
00150 000100        WRDCNT: .WORD 100        ; - FULL SD BUFFER =100
00152 002000        BUFADR: .WORD 2000        ;BUFFER ADDRESS VARIABLE
00154 000000        UNIT: .WORD 0        ;0=DRIVE 0, 1=DRIVE 1
00156 000000        ERBUF: .WORD 0        ;ERROR BUFFER
```

4-37
Table 4-8. Read / Write RX02 Sector Example

;PROGRAMMING EXAMPLE
;READ / WRITE RX02 SECTOR

;CONTROL AND STATUS REGISTER
RXCS=177170
RXDB=177172

;READ RX02 SECTOR
READ: MOV #7,RO

;BUILD READ SECTOR COMMAND IN RO

;DATA BUFFER REGISTER

;WRITE RX02 SECTOR ROUTINE

;BUILD WRITE SECTOR COMMAND IN RO

;UNIT 0 OR UNIT 1?
SYNTAX: TST UNIT

;SET UNIT
BEQ 1$
BIS #20, RO

;HIGH OR LOW DENSITY?
1$: TST DEN
BIS #20, RO

;SPECIFY HIGH DENSITY
BEQ 2$
BIS #400, RO

;ISSUE COMMAND TO CONTROLLER
MOV RO,@RXCS

;WAIT FOR TRANSFER REQUEST
TSTB @RXCS
BPL 3$

;PASS SECTOR TO CONTROLLER
MOV SECTOR,@RXDB

;WAIT FOR TRANSFER REQUEST
TSTB @RXCS
BPL 4$

;PASS TRACK NUMBER
MOV TRACK,@RXDB

;TEST FOR DONE AND ERROR
BIT #100040,@RXCS

;ERROR BIT SET?
BEQ 5$

;GET DEFINITIVE STATUS
MOV #17,@RXCS

;WAIT FOR TRANSFER REQUEST
TSTB @RXCS
Table 4-8. Read / Write RX02 Sector Example

(continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Instruction/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>00120</td>
<td>100375</td>
<td>BPL 6$</td>
</tr>
<tr>
<td>00122</td>
<td>102737</td>
<td>MOV  @ERBUF,@RXDB   ;SEND ERROR BUFFER ADDRESS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00156'</td>
</tr>
<tr>
<td>00130</td>
<td>032737</td>
<td>BIT #40,@RXCS       ;WAIT FOR DONE BIT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000040</td>
</tr>
<tr>
<td></td>
<td></td>
<td>177170</td>
</tr>
<tr>
<td>00136</td>
<td>001774</td>
<td>BEQ 7$</td>
</tr>
<tr>
<td>00140</td>
<td>113700</td>
<td>MOVB @ERBUF,RO     ;LEAVE ERROR REGISTER IN RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>000156'</td>
</tr>
<tr>
<td>00144</td>
<td>000000</td>
<td>HALT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>;DEN: .WORD 0       ;DENSITY - 0=SINGLE I=DOUBLE</td>
</tr>
<tr>
<td>00150</td>
<td>000001</td>
<td>SECTOR: .WORD 1     ;DESIRED SECTOR ADDRESS</td>
</tr>
<tr>
<td>00152</td>
<td>000001</td>
<td>TRACK: .WORD 1      ;DESIRED TRACK ADDRESS</td>
</tr>
<tr>
<td>00154</td>
<td>000000</td>
<td>UNIT: .WORD 0       ;UNIT - 0=DRIVE 0 I=DRIVE 1</td>
</tr>
<tr>
<td>00156</td>
<td>000000</td>
<td>ERBUF: .WORD 0      ;ERROR BUFFER</td>
</tr>
</tbody>
</table>

COMMON PROGRAMMING MISTAKES

This describes common programming mistakes that can cause data loss and/or error indications.

1) Illegal track or sector address sent to the controller
   A. Valid fixed length sectors are 1-26 (decimal).
   B. Valid tracks are 0-76 (decimal).

2) Incorrect word count for current length of variable length sector.

3) The READ STATUS command requires up to two revolutions of the disk to complete. To avoid excessive delays, use this command only when necessary.

4) After reading or writing, the INITIALIZE DONE bit, RX2ES bit 2, may be checked for an indication of power failure. A short power outage will cause DONE to set without any error indication.

5) The drive select bit, RX2CS bit 4, is not decoded by the controller during FILL BUFFER and EMPTY BUFFER functions.

6) It is recommended that a two-sector interleave (Sectors 1, 3, 5 etc.) be used for optimal data transfer rate.

7) For single density recording, only a 128 bytes/sector diskette can be used. For IBM double density recording, only an IBM 2D 256 bytes/sector diskette can be used.
Typically a FILL BUFFER command precedes a WRITE SECTOR command. Similarly, a READ SECTOR command precedes an EMPTY BUFFER command.

Interrupts

An interrupt is requested by the interface module whenever the INTERRUPT ENABLE and DONE bits of the RX2CS both become set. The standard interrupt sector address is location 264.

MODE 3 (Extended IBM)

The system is in "IBM extended" mode when both switch #4 is closed and switch #7 is open. IBM protocol is observed when a DMA type interface is used.

NOTE

The DSD 480 will run RX02/DSD 480 compatible software when in IBM mode. However, to use the full capability of the DSD 480 in IBM mode, a special handler must be written that will observe the protocol described in this section.

PERIPHERAL DEVICE REGISTERS

Programs communicate with the DSD 480 through two peripheral device registers:

<table>
<thead>
<tr>
<th>NAME</th>
<th>DESCRIPTION</th>
<th>OCTAL LOCATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXICS</td>
<td>COMMAND AND STATUS REGISTER</td>
<td>777170</td>
</tr>
<tr>
<td>RXIDB</td>
<td>DATA BUFFER REGISTER</td>
<td>777172</td>
</tr>
</tbody>
</table>

Peripheral device registers reside in the top 4K words of DEC-11 family computers' memory address space. They are addressed as memory and any instruction that operates on a memory location can operate on a peripheral device register in the same way.

COMMAND AND STATUS REGISTER (RXICS)

Writing the bits of this physical register controls the DSD 480. The format for this register is shown in Figure 4-2. The RX2CS register also provides important status information and error indications when read by the user program.

BIT 15 ER - Error detected, cleared by INITIALIZE or the issuance of a new command. Read Only bit.

BIT 14 - IN - INITIALIZE the DSD 480

The DONE flag is negated, the controller resets some internal variables, and then executes the self-test microcode. The disk drives are homed to track 0.

4-40
If the controller is configured in "NORMAL" mode, the controller reads track 1
sector 1 of the diskette in drive 0. When the READ SECTOR function is attempted, the
INITIALIZE DONE bit in the error/status register is set. If there was a readable diskette
in drive 0, the DRIVE READY bit is also set. If the diskette is in double density, then the
drive density bit is set. The DONE flag is set when the controller has completed the
Initialization sequence. The INITIALIZE bit takes precedence over all other bits in this
register. Bit 14 is a Write Only bit.

BIT 13 - A17 - Extended Address Bit 17

This write only bit is asserted on UNIBUS or Q-BUS address line 17 when the DSD
480 is transferring data via direct memory access. This bit is cleared by an
INITIALIZE. A17 will toggle if A01-A16 are all ones and the bus address register is
incremented by the logic.

BIT 12 - A16 - Extended Address Bit 16

This write only bit is asserted on UNIBUS or Q-BUS address line 16 when the DSD
480 is transferring data via direct memory access. This bit is cleared by an
INITIALIZE. A16 will toggle if A01-A15 are all ones and the bus address register is
incremented by the logic.

BIT 11 - RX02 System Identification Bit

This read only bit provides an easy way for software to differentiate RX01 systems
from RX02 systems.

BIT 10 - Reserved for Possible Future Use

BIT 9 - HS - Head Select Bit

This read/write bit selects side 0 or side 1 (lower head or upper head). It is set to
select side 1, and cleared to select side 0.

BIT 8 - DEN - Density of Function

This read/write bit specifies the density of the function encoded in bits 1-3. High
density is specified when this bit is set.

NOTE

Even though the FILL BUFFER and EMPTY BUFFER functions
do not involve magnetic media, a valid density bit is required
so that the controller can evaluate the validity of the word
count parameter.
Figure 4-4. Mode 3 Command and Status Register Format

BIT 7 - TR - Transfer Request Flag

This read only bit indicates to the program that the DATA BUFFER REGISTER is empty and needs loading, or is loaded and needs emptying.

BIT 6 - IE - Interrupt Enable Bit

This read/write bit, when set, allows an interrupt to be generated whenever the DONE flag is set.

BIT 5 - DN - DONE Flag Indicates the Completion of an Operation

This read only bit works in conjunction with the interrupt enable bit to generate interrupts.

BIT 4 - UNI - Drive Unit Select Bit

The binary encoding of this read/write bit selects drive 0-1. Drive selection only occurs if a drive related function is executed.

BIT 3-1 - FN - Function Select

The binary encoding of these write only bits selects the function to be performed by the DSD 480 system.

<table>
<thead>
<tr>
<th>BINARY</th>
<th>OCTAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0 = FILL BUFFER</td>
</tr>
<tr>
<td>001</td>
<td>1 = EMPTY BUFFER</td>
</tr>
<tr>
<td>010</td>
<td>2 = WRITE SECTOR</td>
</tr>
<tr>
<td>011</td>
<td>3 = READ SECTOR</td>
</tr>
<tr>
<td>100</td>
<td>4 = SET MEDIA DENSITY</td>
</tr>
<tr>
<td>101</td>
<td>5 = READ STATUS</td>
</tr>
<tr>
<td>110</td>
<td>6 = WRITE DELETED DATA SECTOR</td>
</tr>
<tr>
<td>111</td>
<td>7 = READ ERROR CODE</td>
</tr>
</tbody>
</table>
BIT 0 - EX - Execute the function encoded in bits 3-1 of this register. This is a write only bit.

DATA BUFFER REGISTER (RXIDB)

The RXIDB is physically a shift register that provides the communication link between the host processor and the DSD 480 system. The logical register information passed through is based upon a predetermined protocol.

If the DSD 480 is not in the process of executing a command, the RX2DB is written without risk of adverse effects. However, during the execution of an instruction, the RXIDB register provides or accepts information (according to the RX2DB protocol) when the TRANSFER REQUEST flag is set.

CAUTION

Data may be lost if the correct protocol is not followed.

The following descriptions explain the various logical register formats of the physical Data Register (or RXIDB).

Data Buffer (RXIDB)

The data buffer register is used by the function in process to transfer data to and from the disk controller data buffer. All information is transferred as a byte through bits 0-7 of the RXDB.

Disk Track Address (RXITA)

At the proper time during commands requiring a track number (e.g. write sector, read sector), the track number is written to the physical RXIDB register as if it were a logical register. This is the TRACK ADDRESS REGISTER (RXITA = 777172). Track numbers from 0-76 (decimal) are valid.

Disk Sector Address (RXISA)

During commands such as READ SECTOR or WRITE SECTOR, which require a sector address, this address is written into the physical RXIDB register as if it were a logical register. This is the Sector Address Register (RXISA = 777172). Addresses from 1 to 26 (decimal) are valid provided it does not exceed the number of sectors per track of the diskette being accessed.

In addition to the sector address, the programmer must "or" in the "sector size identifier" as explained below. (Mode 3 only.)
This provides an interlock to insure that the handler knows what type diskette is installed in the selected drive. This also verifies to the handler that the FILL prior to the WRITE was valid.

The "sector size identifier" is coded into bits #7, #6, and #5 as follows:

<table>
<thead>
<tr>
<th># Sectors Per Track</th>
<th>Sector Size Identifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>26 (Includes Dec SD &amp; DD)</td>
<td>0 0 0</td>
</tr>
<tr>
<td>15</td>
<td>0 1 0</td>
</tr>
<tr>
<td>8</td>
<td>1 0 0</td>
</tr>
</tbody>
</table>

For Example: To access sector #1 on an 8 sector/track disk you would write 2018 into RXISA.

BIT 7 6 5 4 3 2 1 0

RXISA 1 0 0 0 0 0 0 1

Sector Size Sector Number Identifier

Word Count Register (RXIWC)

The Word Count Register specifies the number of words to be transferred between the controller sector buffer and main memory via DMA (direct memory access). The word count, of course, must not exceed the sector size of the diskette being accessed.

<table>
<thead>
<tr>
<th>Sector Size (Bytes)</th>
<th>Maximum Word Count (Decimal)</th>
<th>Octal</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>64</td>
<td>100</td>
</tr>
<tr>
<td>256</td>
<td>128</td>
<td>200</td>
</tr>
<tr>
<td>512</td>
<td>256</td>
<td>400</td>
</tr>
<tr>
<td>1024</td>
<td>512</td>
<td>1000</td>
</tr>
</tbody>
</table>

Note that the IBM Mode (Mode 3) Word Count Error code is 235 (not 230 as in Mode 2).

Bus Address Register (RXIBA)

This register specifies the bus address to which data is to be transferred during any DMA operation. It is a 16 bit counter on the DSD 480 interface module for the PDP-11 and LSI-11. It increments by two following each data transfer.

The bus address register cannot be read. It should always be loaded with the starting address of a data buffer in memory at the appropriate time during the FILL BUFFER, EMPTY BUFFER, or READ EXTENDED STATUS functions. If you try to load bit 0 with a 1 it will be ignored.
System Error and Status Register (RXIES)

The RXIES register is another logical register that is implemented using the physical RXIDB shift register. It provides status and error information about the drive that is selected by bit 4 of the physical RXICS register. At the completion of a command, the controller places the RXICS register into the data buffer register (RXIDB = 777172) so that the host processor can check the most recent operation. When the controller completes a function which did not actually select a drive (e.g. FILL BUFFER, EMPTY BUFFER), the RX2ES "UNIT SEL" bit and "DRV DEN" bit remains unmodified. All the other RXIES bits are cleared at the initiation of each new function. See Figure 4-3 for the bit layout of this register.

Bits 15,14: Sector Size

NOTE

Only valid during read status function (101)

These bits are set during an IBM Mode read maintenance function to indicate the sector size of diskette in specified unit.

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Sectors/Track</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>26 Sector/Track</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>15 Sectors/Track</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>8 Sectors/Track</td>
</tr>
</tbody>
</table>

NOTE

The sector size indicates the size of cylinders 1 to 76 not cylinder 0. On IBM diskettes, track always has 26 sectors/track.

Bit 13: IBM Double Density

Only valid during read status function (101)

Set during maintenance status to indicate that selected drive contains an IBM 2D diskette.

NOTE

Bits 15, 14, 13, 5 specify the type of diskette in selected drive in read status function.
Bit 15  Bit 14  Bit 13  Bit 5  IBM DEC Type
0 0 0 0  IBM 1,2 - 128/DEC SD
0 1 0 0  IBM 1,2 - 256
1 0 0 0  IBM 1 - 512
0 0 0 1  DEC Double Density
0 0 1 1  IBM 2D - 256
0 1 1 1  IBM 2D - 512
1 0 1 1  IBM 2D - 1024

Bit 12  Not used/reserved

BIT 11 - NXM - Non-exsistent Memory Error
This bit is set if during a DMA cycle the interface does not receive a bus reply when it tries to write/read a word to or from memory. Usually this means the address in the RXIBA or the extended address bits in the RXICS are invalid. The operation is terminated; the error and done bits are set. To recover from this error conditions, generate either a bus INIT or a programmed INIT.

BIT 10 - WC OVFL - Word Count Overflow
This bit is set if the word count specified during a fill or empty buffer command is too large for the sector size indicated by the density bit. The operation is terminated; the Error and Done bits are set.

BIT 9 - HD SEL- Head Select
This bit indicates the read/write head selected during the immediately preceding read or write operation. It is set to indicate the upper head, and cleared to indicate the lower head.

BIT 8 - UNIT SEL - Unit Select
This bit indicates the disk drive selected during the immediately preceding read or write operation. It is set to indicate drive 1, and cleared to indicate drive 0.

BIT 7 - DR V RDY - Drive Ready
This bit, when set, indicates that the selected disk drive has a diskette correctly installed and up to speed. The Drive Ready bit is valid immediately following the Read Status function. This bit is also valid for drive 0 immediately following an initialization.
Figure 4-5. Mode 3 Register Formats

4-47
BIT 6 - DD - Deleted Data
This bit indicates that a deleted data address mark was found during the last Read Sector operation or that the last command was Write Deleted Data Sector.

BIT 5 - DRV DEN - Drive Density
This bit indicates the density of the diskette installed in the in the drive indicated by bit 8. It is updated during read or write sector operations.

BIT 4 - DEN ERR - Density Error
This bit indicates that during a READ SECTOR, WRITE SECTOR, WRITE DELETED DATA SECTOR, OR READ STATUS operation the diskette density did not match the density bit of the RXICS. Any operation is terminated; ERROR and DONE bits are set.

BIT 3 - PWR LO - Power Low
This bit indicates a power failure in the controller/drive subsystem. It will also be set if the interface cable becomes disconnected. Any operation is terminated; the ERROR and DONE bits are set.

BIT 2 - ID - Initialize Done
This bit indicates that the controller/drive subsystem has just completed an initialization sequence. This sequence may have been started by a power failure, bus INIT, or programmed INIT.

BIT 1 - SDI RDY - Side 1 Ready
Bit 1 and bit 7 are both set when a double sided diskette is correctly installed and up to speed. When bit 7 is set but bit 1 is not set, a single sided diskette is installed. A single-sided diskette is restricted to side 0 functions only.

BIT 0 - CRC - Cyclic Redundancy Check Error
This bit indicates that a cyclic redundancy error was detected during the last Read Sector operation. The operation is terminated; the ERROR and DONE bits are set.

MODE 3 PROTOCOLS
Protocols are required in the DSD 480 because the DSD 480 are connected by a single serial data link. Therefore, the controller must identify parameters based on the order in which they are transmitted across the data link.

The following sections describe the protocol for each command that can be sent to the controller. Failure to adhere to the correct protocol results in lost or incorrect data.
**FILL SECTOR BUFFER (000)**

The FILL SECTOR BUFFER command is used to fill a storage buffer inside the DSD 480 with 128, 256, 512, or 1024 eight-bit bytes of data from computer memory. Other functions can be used later to write that data to the diskette, or transfer it back to memory.

When the FILL SECTOR BUFFER command is given, the DSD 480 responds by clearing the DONE flag, RXICS bit 5. The controller then requests a word count by setting the TRANSFER REQUEST flag. The program should respond by writing a valid RXIWC into the RXIDB. The word count must be less than the sector size (in words). When TRANSFER REQUEST is again asserted by the controller, the program should respond by writing a valid starting memory address (RXIBA) into the RXIDB.

As soon as the RXIBA is loaded, TRANSFER REQUEST is cleared and remains cleared for the duration of this function. The data bytes are now transferred directly from memory to the controller sector buffer. When the word count is decremented to zero and the controller has zero-filled the remainder of the current 256 byte partition sector buffer (if necessary), DONE is asserted. An interrupt request is generated if the interrupt enable bit, RXICS bit 6, was set when DONE become true. The RXIES register will be found in the RXIDB at the completion of the function.

**NOTE**

1) Bit 4 of the RXICS does not affect this function since no disk drives need be selected.

2) The DENSITY bit, RXICS bit 8, must be correctly set since this bit is used by the controller in evaluating the validity of the word count.

**EMPTY SECTOR BUFFER (001)**

The EMPTY SECTOR BUFFER function is used to transfer the contents of the sector buffer to main memory. The sector buffer is loaded from a previous FILL SECTOR BUFFER or READ SECTOR command.

When the EMPTY SECTOR BUFFER command is given, the controller responds by clearing the DONE flag (RXICS bit 5). The controller then sets the TRANSFER REQUEST flag (RXICS bit 7) to request the word count register. The program should respond by loading a valid word count into the data buffer register. The word count must reflect the 512 word per sector limit on IBM diskettes.

When TRANSFER REQUEST is asserted again, the program responds by loading the starting memory address into the data buffer register. When this is done, the controller clears the TRANSFER REQUEST flag and it remains clear for the rest of the operation.
The data in the sector buffer is transferred to memory one word at a time until the word count is decremented to zero. When the data has been transferred, the controller places the RXIES into the data buffer register and sets the DONE flag. If the interrupt enable bit is set, an interrupt request is initiated when DONE becomes true.

The notes above that apply to the FILL BUFFER command apply equally to the EMPTY SECTOR BUFFER command. In addition, note that the EMPTY BUFFER function does not modify the contents of the sector buffer.

<table>
<thead>
<tr>
<th>Sector Size (Bytes)</th>
<th>Word Count Limit</th>
<th>Octal</th>
<th>High Byte</th>
<th>Low Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>64</td>
<td>000</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>256</td>
<td>128</td>
<td>000</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>512</td>
<td>256</td>
<td>000</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>1024</td>
<td>512</td>
<td>001</td>
<td>000</td>
<td></td>
</tr>
</tbody>
</table>

**WRITE SECTOR (010)**

When the WRITE SECTOR command is given, the controller clears the logical RXIES register and the DONE flag. Next the controller sets the TRANSFER REQUEST flag, RXICS register bit 7, to request a sector address. The program responds by writing the desired sector address (RXISA) into the data buffer register. This clears the TRANSFER REQUEST flag. The "sector size identifier" must be coded into bits 6 and 7 of the sector address register (RXISA). As soon as the controller shifts the sector address over the interface cable, it asserts TRANSFER REQUEST again. This time the program responds by writing the desired track address (RXITA) into the data buffer register. This clears the TRANSFER REQUEST flag.

If media density does not agree with the command density (RXICS bit 8), the operation is terminated. Bit 4 of the RXIES register indicates a density error. If the densities agree, the controller checks the track address and looks for the specified sector address. The number of bytes written by the controller is determined by the density and sector size of the current diskette. If an incorrect sector size is specified, the operation will terminate without writing (ERROR=255). Two CRC bytes are written immediately after the data.

**NOTE**

1) The contents of the sector buffer are not modified by the WRITE SECTOR function.

2) If the contents of the sector buffer are modified as a result of a power failure or the initialize command, programmers must be sure that valid data is written back into the sector buffer following either of these conditions. This is especially true before executing the WRITE SECTOR command.
3) Sector numbers 152 through 162 (octal) are special format keys. Refer to the FORMAT function for their definition.

4) When writing a IBM 2D (Double Density) diskette, track 0 must be written with a command density = single density.

5) The density of IBM diskettes if determined by the headers on the IBM diskette.
   
   The density of a diskette must not be determined on track 0, as track 0 is single density whether the rest of the disk is single or double density.

READ SECTOR (011) (Bit 9 selects side 0/side 1)

The READ SECTOR function is used to locate a specified track and sector of a diskette and then transfer the contents of the data field into the controller's sector buffer.

During Mode 2 operation, the controller clears the logical RX2ES register and the DONE flag when the READ SECTOR command is given. Next, the controller sets the TRANSFER REQUEST flag (RXICS bit 7) to request a sector address. The program should respond by writing the desired sector address (RXISA) into the data buffer register (RXIDB=777172). This clears the TRANSFER REQUEST flag. The "sector size identifier" must be coded into bits 6 and 7 of the SECTOR ADDRESS REGISTER (RXISA). As soon as the controller shifts the sector address over the interface cable, it asserts TRANSFER REQUEST a second time. The program responds by writing the desired track address (RXITA) into the data buffer register which clears the TRANSFER REQUEST flag.

After receiving the track address, the controller causes the selected drive to seek to the desired track. TRANSFER REQUEST is left reset for the remainder of this function. The controller loads the heads against the media and determines the density of the media if it is not already known. If the diskette density does not agree with the command density (RXICS bit 8), an error is reported and the function is terminated. If the densities agree, the controller looks for the specified sector. When the right sector is located, the controller looks for the appropriate data, or deleted data address mark.

When the mark is found, the controller transfers the bytes into the sector buffer. The number of bytes transferred is determined by the density and sector size of the current diskette. If an incorrect sector size is specified, the operation will terminate without reading (ERROR=255). The two error-free are read immediately after the data field. An error-free read is indicated if the address mark, data bytes and two bytes of CRC check bytes produce a zero residue when passed sequentially through the CRC checker hardware circuits. As soon as the data is available in the buffer, the controller terminates the function by writing the RXIES to the data buffer register and setting the DONE flag. An interrupt request is generated if the interrupt enable bit was set when DONE became true.
If the deleted data address mark was detected, the controller will set the deleted data flag. This flag appears in the ERROR/STATUS register (RXIES bit 6). If a CRC error is detected, the controller will set RXIES bit 0 and the ERROR flag (RXICS bit 15). Seek errors and missing sector errors are reported just as in the WRITE SECTOR function.

NOTE

All IBM diskettes are written in single density on track 0. Determination of diskette density should be made on other than track 0.

SET MEDIA DENSITY (100)

This command is used to initialize an entire DEC-formatted diskette to some specified density. When the SET MEDIA DENSITY command is executed, the controller attempts to write zeroes in every field on the diskette. Bit 8 of the RXICS determines the recording density and the type of Data Address Mark to be written in each data field. No sector headers are written when the SET MEDIA DENSITY command is executed.

FUNCTION PROTOCOL

When the command is received, the controller clears the DONE flag and the logical RXIES register. Next, the controller sets the TRANSFER REQUEST flag. The program responds by writing a "key byte" into the physical RXIDB. If the key byte is an ASCII "l" or 111 octal, the SET MEDIA DENSITY function is executed. If the byte written into the RXIDB is not an "l", the DONE and ERROR flags are set and the operation terminates. The error register is loaded with a 250 to indicate an invalid key. The purpose of the key is to make it difficult to erase all of the data on a diskette.

As soon as the safety character "l" is received, the controller moves the heads to track 0. When sector 1 is found, the controller starts writing. If bit 8 of the RXICS was a 0, a single density Data Address Mark and 128 FM zeroes are written. If bit 8 of the RXICS was a 1, a double density Data Address Mark and 256 DEC MFM zeroes are written. After writing all 26 sectors on track 0, the controller seeks to track 1, 2, ..., writing all 26 sectors on each track. This continues until either every sector has been written through track 76: sector 26, or a bad header is found. The ERROR and DONE flags are set if the operation terminates due to a bad header.

The SET MEDIA DENSITY function takes about 26 seconds per diskette side, depending on the sector interleave. It should never be interrupted before it is done. If the function does not terminate normally, an illegal diskette which has Data Address marks of both densities may have been created. If this happens, the diskette should be completely formatted. If the SET MEDIA DENSITY function is not complete because of an unreadable header, the TRACK FORMAT procedure can be used to rewrite the incorrect header information.

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READ STATUS (101)

The READ STATUS command is used to determine the current status of the drive selected by RXICS bit 4. The status information passed back is:

1) Drive readiness
2) Side #1 readiness if two sided disk
3) IBM information now included in upper 3 bits of "RXIES".
   15:14 = sector length identifier.
   13 = IBM double density
4) Drive density

To determine density the controller searches for IBM DD header then single density if necessary. Based on header and DAM, the diskette is determined.

When the command is issued, the DONE flag is cleared. The controller checks the selected drive's door is closed, a diskette is inserted, and that the diskette is up to speed. Diskette speed is determined by measuring the amount of time between successive index pulses. Since this measurement takes an average of 250 milliseconds, excessive use of the READ STATUS function will cause reduced throughput. If the drive is ready, the controller sets bit 7 (DRIVE READY) of the RXIES. Next, the controller loads the heads and reads the first sector it finds. The diskette density and format are determined and encoded into bits 13, 14, and 15 of the RXIES.

If a double density address mark is detected, bit 5 (DRV DEN) of the RXIES is set. If a single density mark is found, bit 5 is cleared. The controller terminates the function by shifting the RXIES over to the RXIDB and setting the DONE flag. An interrupt request is generated if the interrupt enable bit, RXICS bit 6, was set when DONE become true.

READ EXTENDED STATUS (111)

The READ EXTENDED STATUS command is used to retrieve a number of internal controller registers, including the error register. These registers are transferred to memory using direct memory access. As soon as the command is loaded into the RXICS, the DONE flag goes false. The controller then asserts the TRANSFER REQUEST flag.

The program then loads a starting memory address into the RXIDB. The controller transfers 4 words directly to memory beginning at the specified address. When the words are in memory, the controller asserts DONE. This generates an interrupt request if interrupt enable had been previously set.

The words transferred to memory are as follows:
WORD 1 - LO BYTE  DEFINITIVE ERROR CODE (SEE TABLE 4-9)
WORD 1 - HI BYTE  HI BYTE OF PREVIOUS WORD COUNT
WORD 2 - LO BYTE  CURRENT TRACK ADDRESS OF DRIVE 0
WORD 2 - HI BYTE  CURRENT TRACK ADDRESS OF DRIVE 1
WORD 3 - LO BYTE  TARGET TRACK OF CURRENT DISK ACCESS
WORD 3 - HI BYTE  TARGET SECTOR OF CURRENT DISK ACCESS
WORD 4 - BIT 0   DENSITY OF READ ERROR REGISTER COMMAND
WORD 4 - BIT 4   DRIVE DENSITY OF DRIVE 0
WORD 4 - BIT 5   HEAD LOAD BIT
WORD 4 - BIT 6   DRIVE DENSITY OF DRIVE 1
WORD 4 - BIT 7   UNIT SELECT BIT
WORD 4 - HI BYTE  TRACK ADDRESS OF SELECTED DRIVE

WRITE DELETED DATA (110) - (Mode #3)

* This function performs with the same protocol as a write sector under IBM - Mode #3.

* NOTE

On IBM double density diskettes the deleted data address mark is always single density (the header determines IBM density).
### Table 4-9. Modes 2 and 3 Definitive Error Codes

<table>
<thead>
<tr>
<th>OCTAL CODE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>No error</td>
</tr>
<tr>
<td>010</td>
<td>No drive 0 or drive 0 failed to find track 0 on INIT</td>
</tr>
<tr>
<td>020</td>
<td>No drive 1 when DIP switch indicates there should be a drive 1, or drive 1 failed to find track 0 on INIT</td>
</tr>
<tr>
<td>030</td>
<td>Track 0 found while stepping in on initialize</td>
</tr>
<tr>
<td>040</td>
<td>Track address passed to controller was invalid (&gt;76)</td>
</tr>
<tr>
<td>050</td>
<td>Track 0 found before desired track while stepping</td>
</tr>
<tr>
<td>070</td>
<td>Requested sector not found in two revolutions</td>
</tr>
<tr>
<td>075</td>
<td>Too many bad headers on &quot;IBM 2D&quot; diskette</td>
</tr>
<tr>
<td>100</td>
<td>Write protect violation</td>
</tr>
<tr>
<td>110</td>
<td>No read data signal present</td>
</tr>
<tr>
<td>120</td>
<td>No preamble found</td>
</tr>
<tr>
<td>130</td>
<td>Preamble found, but no address mark within window</td>
</tr>
<tr>
<td>140</td>
<td>CRC error on what appeared to be a header</td>
</tr>
<tr>
<td>150</td>
<td>Address in good header did not match desired track</td>
</tr>
<tr>
<td>160</td>
<td>Too many tries for an ID address mark</td>
</tr>
<tr>
<td>170</td>
<td>Data address mark not found in allotted time</td>
</tr>
<tr>
<td>175</td>
<td>DEC double density address mark on non-DEC diskette</td>
</tr>
<tr>
<td>200</td>
<td>CRC error on data field; RXES bit 0 also set</td>
</tr>
<tr>
<td>210</td>
<td>Parity error on interface cable; RXES bit 1 also set</td>
</tr>
<tr>
<td>220</td>
<td>Read/write controller failed maintenance mode test</td>
</tr>
<tr>
<td>230</td>
<td>Invalid word count specified (Mode 2 only)</td>
</tr>
<tr>
<td>235</td>
<td>Word count error during FILL or EMPTY BUFFER (Mode 3 only)</td>
</tr>
<tr>
<td>240</td>
<td>Density error; DEC format</td>
</tr>
<tr>
<td>245</td>
<td>Density error; IBM format</td>
</tr>
<tr>
<td>250</td>
<td>Wrong key for set media density or format command</td>
</tr>
<tr>
<td>255</td>
<td>Incorrect &quot;sector size identifier&quot; used in RXISA</td>
</tr>
<tr>
<td>260</td>
<td>Indeterminate density, or no diskette present</td>
</tr>
<tr>
<td>265</td>
<td>Diskette not compatible with RX01 on RX02 mode</td>
</tr>
<tr>
<td>270</td>
<td>Read/write controller write-format failure</td>
</tr>
<tr>
<td>320</td>
<td>Read/write controller detected write circuit failure</td>
</tr>
<tr>
<td>330</td>
<td>Read/write controller timed out on reset</td>
</tr>
<tr>
<td>340</td>
<td>Master controller out of SYNC with RD/WRT controller</td>
</tr>
<tr>
<td>350</td>
<td>Non-existent memory error during DMA</td>
</tr>
<tr>
<td>360</td>
<td>Drive not ready during format command</td>
</tr>
<tr>
<td>370</td>
<td>AC power low caused abort of write activity</td>
</tr>
</tbody>
</table>
DISKETTE FORMATTING

CAUTION

This procedure will allow magnetically damaged diskettes to be repaired. Formatting may cause permanent loss of data if not done correctly.

The DSD 480 can write format diskettes in nine different formats. Either a single track or the entire diskette may be formatted. If an entire diskette format is selected the DSD 480 will automatically format cylinder zero of IBM diskettes in the correct format.

NOTES

1) The DEC RX02 does not support the command protocol described below. It is a special feature unique to the DSD 480.

2) Diskette formatting may be performed when the DSD 480 is in any of its operating modes (1, 2, or 3). However, the resulting diskette may not be compatible with this mode (e.g., IBM 2D formats may not be read in Mode 1). Refer to Table 4-1 for format compatibility.

DISKETTE FORMAT PROTOCOL

1) The user program issues the "WRITE-SECTOR" function code (010) to the controller via the COMMAND and STATUS REGISTER (RX2CS or RXICS). Bit 9 of the register will select the desired side:

   0 = Side 0
   1 = Side 1

   The density bit (Bit 8) is ignored.

2) The controller will next clear the done flag and issue Transfer Request (Bit 7 of RXCS).

3) The user program must now write an octal value into the data buffer (RX2DB or RX1DB) corresponding to the desired format. Table 4-8 lists the formats available. If an entire diskette format is selected, the protocol is finished and the format will be executed when the operation is completed, the controller will assert done. An interrupt will occur if Bit 6 (Interrupt enable) is set by the format command.

   For single track formats, the Transfer Request flag will be issued, requesting the track address. After the track address has been supplied, the controller will continue to assert transfer request for the desired sector. The number of sectors is determined by the format. Thus, for a 26 sector diskette, the transfer request will be issued 26 times. The
sectors may be written in any desired order. Thus a non-standard interleave pattern may be chosen.

The controller does not check uniqueness. After the appropriate number of sectors have been selected, the controller will format the track. Upon completion of the format, "DONE" will be asserted in the RX2CS (or RXICS) and an interrupt will occur if interrupts are enabled by bit #6 of RX2CS (or RXICS).

NOTE
(on Table 4-9)

If IBM formats are selected, note that track 0 always has 26 sectors per track. Therefore, all 26 sector numbers must be supplied to format track 0.

Also, note that track 0, side 0 of an IBM double density disk is always single density.

Table 4-10. Diskette Format Codes

<table>
<thead>
<tr>
<th>ID CODE</th>
<th>DESCRIPTION</th>
<th>DENSITY</th>
<th>#SECTORS/TRACK</th>
<th>TRACK #</th>
</tr>
</thead>
<tbody>
<tr>
<td>1528</td>
<td>Format disk in single density on one track. This format is compatible with both DEC and IBM. Side selection done when command given to RX2CS (or RXICS).</td>
<td>Single</td>
<td>26</td>
<td>0 to 76</td>
</tr>
<tr>
<td>1538</td>
<td>Format disk in DEC modified MFM, double density, on one track. This format is only DEC compatible. Side selection done when command given to RX2CS.</td>
<td>Double</td>
<td>26</td>
<td>0 to 76</td>
</tr>
<tr>
<td>1548</td>
<td>Format entire disk with FM coded, single density. This format is the same as &quot;152&quot;s and is done on both sides of a two sided diskette.</td>
<td>Single</td>
<td>26</td>
<td>0 to 76</td>
</tr>
<tr>
<td>1558</td>
<td>Format entire disk with DEC modified MFM, double density. This format is only DEC compatible. Both sides of a two sided disk are formatted.</td>
<td>Double</td>
<td>26</td>
<td>0 to 76</td>
</tr>
</tbody>
</table>
156g  Format one track on disk with IBM single density FM coding. All tracks except 0 have 15 sectors per track on tracks 1 to 76, with 256 bytes per sector.

157g  Format one track on disk with IBM single density FM coding. All tracks, except track 0, have 8 sectors per track, with 512 bytes/sector on tracks 1 to 76.

160g  Format one track on disk with IBM double density MFM coding. All tracks have 26 sectors. TRK 0, side 0 is single density. Must use two sided disk.

161g  Format one track on disk with IBM double density MFM coding. All tracks have 15 sectors except track 0. Track 0, Side 0, is single density, FM with 26 sectors. Track 0, side 1 is double density with 26 sectors/track.

162g  Format one track on disk with IBM double density, MFM. TRK 1 to 76 are 8 sector/track with 1024 bytes/sector. Track 0 same as "161"s format.

POWER FAIL

When a power failure occurs or DC power to the DSD 480 is interrupted, the controller gradually drains the filter capacitors and stops executing microcode. The program knows the controller/drive subsystem has lost power when the DONE and ERR bits are set in the RX2CS, and the PWR LOW bit is set in the RX2DB.

When power is restored, and the controller DIP-Switch is configured for "NORMAL mode, the DSD 480 controller initiates the following sequence:

1) DONE is cleared.

2) Controller executes the hardware self-tests.
3) All drives positioned to track 00.

4) RX2ES is cleared of all active error bits.

5) The controller reads sector 1, track 1 of unit 0 into buffer and leaves drive #0 at track #1.

6) Bit 2 of RX2ES (INITIALIZE DONE) is set.

7) Bits 7 (DRIVE READY) and 5 (DRIVE DENSITY) of RX2ES are updated according to the status of drive 0.

At the end of this sequence, RX2CS bit 5 (DONE) is set.
CHAPTER 5

HARDWARE SELF-TESTING

The DSD 480 diagnostics simplify incoming inspection and speed fault isolation with easy-to-use maintenance capabilities including both extensive self-testing and complete interactive system level testing. These capabilities, combined with the reliability and modular construction of the DSD 480 system, help minimize the cost of long-term ownership. Additionally, the DSD 480 is able to run DEC diagnostics without modification. This chapter covers the self-testing capabilities of the DSD 480. Recommendations are made for initial DSD 480 acceptance testing and for subsequent troubleshooting of suspected system malfunctions.

There are two types of DSD 480 self-tests. First, there are those that execute automatically on power-up. Second, there are user selectable self-tests known as "HYPERDIAGNOSTICS". Hyperdiagnostics should be performed when the DSD 480 is first installed or whenever a computer system fault condition is suspected. These tests should be performed before any computer resident diagnostics are attempted.

AUTOMATIC SELF-TESTING

The microprocessor in the DSD 480 controller executes several system hardware tests following power-up or an initialization. These tests are executed even when the system is in a user selectable, stand alone, self-test mode. You cannot inhibit these tests from executing, and you cannot operate the system should one of them detect a malfunction.

Just before each of these controller test routines is executed, the microprocessor writes the error code associated with the failure of that particular test in LED indicators 5 through 8 on the controller board. In the event the test detects a malfunction, the controller microprocessor will halt leaving the error code displayed. The green RUN LED (labelled "LED 9") indicator and LED indicators 1, 3 and 4 will be off. LED indicator 2 will be on. LED indicators 5, 6, 7 and 8 contain the error code. The error code interpretations are in Table 5-1.

Should an error occur and the solution to the problem is not obvious, try cycling the main power several times. If the error persists, call the Data Systems Design Customer Service Department for assistance.

In addition to the controller self-tests, the DSD 480 has self-test routines built into the bootstrap program on the the LSI-11 and PDP-11 interface cards. These routines and their error conditions are described in Chapter 3.
USER SELECTABLE SELF-TESTS: HYPERDIAGNOSTICS

The DSD 480 controller may be operated in two modes. In NORMAL mode, the DSD 480 controller is connected to a host computer through an interface module. The user program and/or operating system software controls all of the functions performed by the data storage system.

In "HYPERDIAGNOSTIC" mode, the interface cable is disconnected from the DSD 480 chassis and the controller microprocessor executes routines which are selected by the eight position DIP-switch on the controller module. These routines are started and stopped by applying and removing AC power. To select a test routine, the main AC power switch located on the rear of the chassis must be in the OFF position. You can then select the individual "HYPERDIAGNOSTIC" routine by changing the settings of the DIP-Switch. To initialize a test, resume power.

These DIP-Switch selectable routines were named "HYPERDIAGNOSTICS" because they are a decisive improvement over standard self-test procedures. They perform the following types of diagnostic functions:

- Simplified acceptance tests requiring no special test equipment for operation.
- Drive-independent controller self-tests.
- Extensive drive utility routines and composite system exercisers.
- Simplified disk drive alignment and adjustment procedures.

In addition, nine LED indicators on the DSD 480 controller module designate the status of "HYPERDIAGNOSTIC" operation.

The major benefit of the "HYPERDIAGNOSTICS" is in their stand-alone ability to easily verify correct disk drive system and controller operation. With this feature, faults in subsystems may be quickly isolated when a total computer system malfunctions.

TEST SELECTION INDICATOR LIGHTS AND DIP-SWITCH

Figure 5-1 shows the relative location of the nine indicator LEDs and the DIP-Switch test selector on the controller module.
FIGURE 5-1. Controller Module Indicator Lights and DIP-Switch Orientation

Note that two of the LEDs are green and the remaining seven are red. LED 1 is green, and is located nearest the DIP-Switch. LEDs 2 through 8 are all red, and are located next to LED 1. The meanings of LEDs 1 through 8 will vary according to whether the system is in NORMAL or "HYPERDIAGNOSTIC" mode, and whether the microprocessor is running or halted. LED 9, which also is green, is ON when the microprocessor is running and OFF when the microprocessor is halted. LED 9 is referred to as the RUN LED.

NOTE

If there is ever doubt as to whether a particular LED Indicator is ON or OFF, view the indicator from directly on axis.

The drive activity LEDs are mounted in the eject button on the front of each disk drive. They indicate that the head is loaded against the media. These LEDs may flash on and off about once every second to indicate an error condition. This flashing continues until an INIT occurs or several seconds have elapsed since the occurrence of the error.
The 8 position DIP-Switch is used to select options in Normal Mode operation and select tests to be run in "HYPERDIAGNOSTIC" Mode. Figure 5-2 shows how the switch are numbered, and which physical position of a switch corresponds to a binary "1" a which position corresponds to a "0".

![Diagram of DIP-Switch]

- This indicates a switch position to be selected by the user.
- This shows switch 4 in the "1" or OPEN position.
- This shows switch 1 in the "0" or Closed position.

Figure 5-2. Controller Module DIP-Switch
<table>
<thead>
<tr>
<th>SWITCH NUMBER</th>
<th>SWITCH NAME</th>
<th>WHEN CLOSED</th>
<th>WHEN OPEN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,2,3</td>
<td>Self Test Select</td>
<td>All Closed for Normal Operation</td>
<td>Selects a Hyper Diagnostic Function</td>
</tr>
<tr>
<td>4</td>
<td>Mode Select</td>
<td>Selects RX02 or Mode 2 (RX02 compatible) or Mode 3 (IBM compatible)</td>
<td>Select Mode 1 (RX01 compatible)</td>
</tr>
<tr>
<td>5</td>
<td>Drive Mapping</td>
<td>Left Drive = Unit 0 Right Drive = Unit 1</td>
<td>Right Drive = Unit 0 Left Drive = Unit 1</td>
</tr>
<tr>
<td></td>
<td>Select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Drive Type</td>
<td>Single Sided Drive</td>
<td>Double Sided Drive</td>
</tr>
<tr>
<td></td>
<td>Select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Extended Format</td>
<td>Mode 2 Read all DEC and IBM 26 Sector Formats</td>
<td>Mode 3 Read all DEC and IBM Formats</td>
</tr>
<tr>
<td></td>
<td>Select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Select Number of Drives</td>
<td>Operate One Drive</td>
<td>Operate Two Drives</td>
</tr>
</tbody>
</table>

**Figure 5-3. Controller DIP-Switch Functions**

**NORMAL MODE**

In normal mode, the DSD 480 controller is connected to a host computer through an interface module. The user program and/or operating system software controls all of the functions performed by the data storage system.

**DIP-Switch Settings for NORMAL Operation**

As described in Chapter 4, the DSD 480 has three modes of normal operation. The DIP-Switch settings for these modes are illustrated below. Note that the DSD 480 is shipped in Mode 2 (RX02 compatible) configuration.

**Indicator Light (LED) Definitions During Normal Operation**

Figure 5-5 illustrates the significance of the LED indicators during normal operation. LEDs 5 through LED 8 are used to display an "error class" code. When a LED is on, this corresponds to a binary 1. When a LED is off, it corresponds
CONTROLLER DIP-SWITCH SETTINGS

Key:

These Dip Switches are found on the controller board inside the DSD 480 chassis.

This indicates a switch position to be selected for specific function.

This shows switch 1 in the "1" or OPEN position.

Normal Operation

Normal Operation is Specified When Switches 1, 2, and 3 are Closed

RX02 Mode 2/3
RX02 Compatible Operation (EN RX01 jumper should be removed on interface)

RX01 Mode 1
RX01 Compatible Operation (EN RX01 jumper should be installed on interface)

Mapping of Drive Unit Numbers
Left Drive = Unit 0
Right Drive = Unit 1

Right Drive = Unit 0
Left Drive = Unit 1

Drive Type
For Normal or HyperDiagnostic Modes

Drive Type
Single Sided

Drive Type
Double Sided

Extended Format Select
Mode 2
DEC/IBM
28 Sector Format

Mode 3
DEC/IBM
All Formats

Number of Drives
Single Drive System

Dual Drive System

Figure 5-4. Controller DIP-Switch Settings
### Drive Alignment Routines

* (See Shugart Drive Maintenance Manual for Procedures)

<table>
<thead>
<tr>
<th>Switch Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 1 0 0 0 X</td>
<td>Head Load Timing Adjustment</td>
</tr>
<tr>
<td>0 0 1 0 1 0 X</td>
<td>Track 0 Detector Adjustment</td>
</tr>
<tr>
<td>0 0 1 1 0 X</td>
<td>Seek Track 01 and Load Head</td>
</tr>
<tr>
<td>0 0 1 1 1 X</td>
<td>Seek Track 02 and Load Head</td>
</tr>
<tr>
<td>0 1 0 0 0 X</td>
<td>Seek Track 16 and Load Head</td>
</tr>
<tr>
<td>0 1 0 0 1 X</td>
<td>Butterfly Seek Test</td>
</tr>
<tr>
<td>1 0 0 0 1 X</td>
<td>Single Pass Sequential Scan Test</td>
</tr>
<tr>
<td>1 0 0 1 0 0 X</td>
<td>Continuous Sequential Scan Test</td>
</tr>
</tbody>
</table>

### Drive Related System Tests

<table>
<thead>
<tr>
<th>Switch Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Single Pass General Exerciser with Write Format Single Density</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Single Pass General Exerciser without Write Format</td>
</tr>
</tbody>
</table>

### Drive Independent System Tests

<table>
<thead>
<tr>
<th>Switch Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Test Read/Write Controller</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Test Phase Locked Loop and CRC Checker/Generator Hardware</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Verify Proper Orientation of the Drive and Bus Cables</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Continuously Execute Hardware Self-Test Microcode Includes PLL and RWC Testing</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Continuous General Exerciser Routine Starting with Write-Format Single Density</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Continuously General Exerciser Routine</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Single Pass General Exerciser with Write Format Single Density</td>
</tr>
</tbody>
</table>

### General System Exercisers

<table>
<thead>
<tr>
<th>Switch Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Continuous General Exerciser Routine</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Continuous General Exerciser Routine Start with Write-Format Single Density</td>
</tr>
<tr>
<td>1 2 3 4 5 6 7 8</td>
<td>Single Pass General Exerciser with Write Format Single Density</td>
</tr>
</tbody>
</table>

---

*Note: To write-format a diskette in double density:*

1. Execute single density Write-Format routine
2. Execute double density Set Media Density operation
3. Switch 8 Selects Drive
   - 0 : Drive 0
   - 1 : Drive 1
CONTROLLER L.E.D. DECODING CHART

These LEDs are found on the controller board inside the DSD 460 chassis.

Key:

<table>
<thead>
<tr>
<th>LED</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>0 = Off</td>
</tr>
<tr>
<td></td>
<td>1 = On</td>
</tr>
</tbody>
</table>

HyperDiagnostic Errors

<table>
<thead>
<tr>
<th>LED</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>9</td>
<td>(RUN)</td>
</tr>
</tbody>
</table>

- 0: No Error Since Power On
- 1: Operator Error (Write Protect/Drive Not Ready)
- 2: Wrong Density Mark Encountered
- 3: Bus Error
- 4: Drive Bus Cable Backwards or Interface Without Power
- 5: Power Fail
- 6: Interface Error
- 7: Drive Error
- 8: Drive Error
- 9: Drive Error

Hardware Self-Test Errors

<table>
<thead>
<tr>
<th>LED</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>9</td>
<td>(RUN)</td>
</tr>
</tbody>
</table>

- 0: Unassigned
- 1: 8253 Watch-Dog Timer Failure
- 2: Interface Shift Register Error
- 3: Parity/Latched INIT Logic Fault
- 4: 8155 RAM Failure
- 5: Phase-Locked-Loop Failure
- 6: Read/Write Controller Failure
- 7: CRC/Serial Data Path Failure
- 8: 8155 Timer Failure
- 9: Unrecognized Dip-Switch Setting

Notes:
1. All error LEDs appear solid on, the microprocessor is being held reset. Check for sufficient power to controller board
2. The drive activity LEDs are mounted on the diskette eject button of each drive and are used to indicate the drive associated with an error. A LED will remain on to indicate which drive was selected at the time of a HyperDiagnostic error.

Figure 5-5. Controller LED Decoding Chart
Figure 5-6. Controller DIP-Switch Settings; Normal Modes

to a binary 0. The code bits read from left to right where LED 5 is the most significant bit and LED 8 is the least significant bit. Each error class code represents a grouping of one or more definitive error codes that are passed to the main computer on command. The definitive error codes are described in Chapter 4. They may be accessed from the computer console terminal by executing the READ ERROR REGISTER (Mode 1) or READ EXTENDED STATUS (Modes 2 or 3) commands to read the error register, ERREG.

NOTE

If all LEDs remain on, the processor is held reset. This can be a result of low voltage on the controller.
<table>
<thead>
<tr>
<th>Binary Code Seen on LED#s 5678</th>
<th>Error Class</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0</td>
<td>No errors have occurred since power on or last init</td>
</tr>
<tr>
<td>0001</td>
<td>1</td>
<td>Operator error - write protect violation (ERREG = 100) or drive not ready (ERREG = 360)</td>
</tr>
<tr>
<td>0010</td>
<td>2</td>
<td>Programming error - density/key (ERREG = 240, 245, 250, or 255)</td>
</tr>
<tr>
<td>0011</td>
<td>3</td>
<td>Programming error - drive/track address (ERREG = 040)</td>
</tr>
<tr>
<td>0100</td>
<td>4</td>
<td>Programming error - word count/ NxM (ERREG = 230, 235 or 350)</td>
</tr>
<tr>
<td>0101</td>
<td>5</td>
<td>Indeterminate density (ERREG = 70, 75, or 260)</td>
</tr>
<tr>
<td>0110</td>
<td>6</td>
<td>Seek error (ERREG = 150)</td>
</tr>
<tr>
<td>0111</td>
<td>7</td>
<td>Header CRC error (ERREG = 140)</td>
</tr>
<tr>
<td>1000</td>
<td>8</td>
<td>Data CRC error (ERREG = 200)</td>
</tr>
<tr>
<td>1001</td>
<td>9</td>
<td>Sector unrecoverable (ERREG = 070, 120, 130, 160, 170 or 175)</td>
</tr>
<tr>
<td>1010</td>
<td>A</td>
<td>No read data signal present (ERREG = 110)</td>
</tr>
<tr>
<td>1011</td>
<td>B</td>
<td>Read/write contr. failure (ERREG = 220, 320, or 330)</td>
</tr>
</tbody>
</table>

Table 5-1. LED Error Class Codes in NORMAL Mode (Mode 1, Mode 2, or Mode 3)(Both Green LEDs On)
Table 5-1. LED Error Class Codes in NORMAL Mode (Mode 1, Mode 2, or Mode 3)(Both Green LEDs On) (continued)

<table>
<thead>
<tr>
<th>BINARY CODE SEEN ON LED#5 5678</th>
<th>ERROR CLASS</th>
<th>INTERPRETATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1100</td>
<td>C</td>
<td>MASTER CONTROLLER FAILURE (ERREG = 340)</td>
</tr>
<tr>
<td>1101</td>
<td>D</td>
<td>DRIVE FAILURE (ERREG = 010, 020, 030, 050)</td>
</tr>
<tr>
<td>1110</td>
<td>E</td>
<td>INTERFACE PARITY ERROR (ERREG = 210)</td>
</tr>
<tr>
<td>1111</td>
<td>F</td>
<td>WRITE OR WRITE-FORMAT FAILURE (ERREG = 270 or 370)</td>
</tr>
</tbody>
</table>

The error class code is displayed in the LEDs as soon as the error is detected. The code resets to zero if the power is switched off and then on or if an INIT is generated over the IBUS cable. The drive activity LEDs are also used to indicate the occurrence of errors. Whenever bit 15 of the control and status register indicates the occurrence of an error (other than density error), the controller microprocessor flashes the activity LED of the drive associated with the error about every second. This flashing stops when either a system initialize is forced by the host computer, or after approximately two minutes elapse.

Table 5-2. Error Register Codes

<table>
<thead>
<tr>
<th>LED CODE ERROR (OCTAL)</th>
<th>CLASS</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>010</td>
<td>D</td>
<td>DRIVE 0 FAILED TO HOME ON INIT</td>
</tr>
<tr>
<td>*020</td>
<td>D</td>
<td>DRIVE 1 FAILED TO HOME ON INIT</td>
</tr>
<tr>
<td>030</td>
<td>D</td>
<td>ENCOUNTERED TRACK 0 WHILE STEPPING IN ON INIT</td>
</tr>
<tr>
<td>040</td>
<td>3</td>
<td>INVALID DRIVE OR TRACK ADDRESS SPECIFIED</td>
</tr>
<tr>
<td>050</td>
<td>D</td>
<td>TRACK 0 ENCOUNTERED UNEXPECTEDLY</td>
</tr>
<tr>
<td>070</td>
<td>5</td>
<td>REQUESTED SECTOR NOT FOUND IN TWO REVOLUTIONS</td>
</tr>
<tr>
<td>075</td>
<td>5</td>
<td>TOO MANY BAD HEADERS ON &quot;IBM 2D&quot; DISKETTE</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
<td>ATTEMPTED TO WRITE ON PROTECTED DISKETTE</td>
</tr>
<tr>
<td>110</td>
<td>A</td>
<td>NO READ DATA SIGNAL PRESENT</td>
</tr>
<tr>
<td>120</td>
<td>9</td>
<td>PREAMBLE NOT FOUND</td>
</tr>
<tr>
<td>130</td>
<td>9</td>
<td>PREAMBLE FOUND BUT NO ID ADDRESS MARK FOLLOWED</td>
</tr>
<tr>
<td>*140</td>
<td>7</td>
<td>HEADER CRC ERROR</td>
</tr>
<tr>
<td>150</td>
<td>6</td>
<td>TRACK OR HEAD ADDRESS MISMATCH</td>
</tr>
<tr>
<td>160</td>
<td>9</td>
<td>TOO MANY TRIES FOR AN ID ADDRESS MARK</td>
</tr>
<tr>
<td>170</td>
<td>9</td>
<td>PREAMBLE FOUND BUT NO DATA ADDRESS MARK FOLLOWED</td>
</tr>
<tr>
<td>175</td>
<td>9</td>
<td>DEC DOUBLE DENSITY ADDRESS MARK ON NON-DEC DISKETTE</td>
</tr>
</tbody>
</table>
Table 5-2. Error Register Codes (continued)

<table>
<thead>
<tr>
<th>LED CODE (OCTAL)</th>
<th>CLASS MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>8 DATA CRC ERROR</td>
</tr>
<tr>
<td>210</td>
<td>E INTERFACE PARITY ERROR</td>
</tr>
<tr>
<td>220</td>
<td>B READ/WRITE CONTROLLER SELF TEST FAILURE</td>
</tr>
<tr>
<td>230</td>
<td>4 INVALID WORD COUNT SPECIFIED</td>
</tr>
<tr>
<td><strong>235</strong></td>
<td>4 WORD COUNT ERROR DURING FILL OR EMPTY BUFFER</td>
</tr>
<tr>
<td>240</td>
<td>2 RX02 DENSITY ERROR</td>
</tr>
<tr>
<td>245</td>
<td>2 IBM DENSITY ERROR</td>
</tr>
<tr>
<td>250</td>
<td>2 WRONG KEY FOR SET MEDIA DENSITY</td>
</tr>
<tr>
<td>255</td>
<td>2 IMPROPER &quot;SECTOR SIZE IDENTIFIER&quot; USED IN RXISA</td>
</tr>
<tr>
<td>260</td>
<td>5 INDETERMINATE DENSITY</td>
</tr>
<tr>
<td>265</td>
<td>5 IBM 2D DISKETTE OTHER THAN 256 BYTES/SECTOR ERROR</td>
</tr>
<tr>
<td>270</td>
<td>F READ/WRITE CONTROLLER WRITE-FORMAT FAILURE</td>
</tr>
<tr>
<td>320</td>
<td>B READ/WRITE CONTROLLER WRITE FAILURE</td>
</tr>
<tr>
<td>330</td>
<td>B READ/WRITE TIMED OUT ON RESET</td>
</tr>
<tr>
<td>340</td>
<td>C MASTER CONTROLLER OUT OF SYNC WITH READ/WRITE CONTROLLER</td>
</tr>
<tr>
<td>350</td>
<td>4 NON-EXISTENT MEMORY ENCOUNTERED DURING DMA</td>
</tr>
<tr>
<td>360</td>
<td>1 DRIVE NOT READY DURING WRITE-FORMAT COMMAND</td>
</tr>
<tr>
<td>370</td>
<td>F AC LOW ABORT OF WRITE OR WRITE FORMAT</td>
</tr>
</tbody>
</table>

* THESE CODES DO NOT ASSERT ERROR IN RXCS, ALL OTHERS DO.

** VALID IN IBM MODE ONLY.

"HYPERDIAGNOSTIC" MODE

The "HYPERDIAGNOSTICS" are used to adjust, exercise, or test the controller drives independently of the host computer system and associated software.

The DSD 480 chassis need only be connected to an AC power outlet to run the "HYPERDIAGNOSTICS". You select particular tests and particular disk drives using the DIP-Switch on the controller board. Test results are designated through a combination of the nine indicator LEDs on the controller board in the DSD 480 chassis. After the switch and LED conventions are explained, the details of each "HYPERDIAGNOSTICS" routine will be discussed.

DIP-Switch Settings For "HYPERDIAGNOSTIC" Operation

Switch 1 through Switch 7

These are used to select the desired test. Any time switches 1, 2, and 3 are zeroes, the microprocessor assumes "NORMAL" mode operation. Switch 1 is the most significant bit and Switch 7 is the least significant bit.
Switch 8

When the switch is a 0, drive 0 is selected; when it is a 1, drive 1 is selected. Not all the tests involve a drive, so in some cases the position of Switch 8 is irrelevant.

The general exerciser tests are capable of testing more than one drive and should be used for initial acceptance testing. These two tests (Switch codes 11110 and 11111) interpret Switch 8 as the number of drives to be exercised. If Switch 8 is a 0, only drive 0 will be exercised. If Switch 8 is a 1, both drive 0 and drive 1 will be exercised.

NOTE

There is no drive mapping function available in "HYPERDIAGNOSTIC" mode. This function is only available when the system is operating in NORMAL mode.

The following is the detailed procedure for running a particular "HYPERDIAGNOSTIC":

1) Remove power from the controller/drive subsystem using the AC switch on the rear of the chassis. Do not tamper with the DIP-Switch settings while power is on EXCEPT when explicitly directed to do so for a particular test.

2) Set the eight switches to select the desired test, and in some cases, the desired drive. The DIP-Switch configurations are shown in Figure 5-4.

3) Use a pointed object (such as a ball point pen) to depress the rocker switches and set them to the desired setting.

4) Restore AC power.

NOTE

A technique that can be used to confirm your switch settings is the DIP-SWITCH/LED "HYPERDIAGNOSTIC". The code for this test is (10000). Once the microprocessor recognizes this test code, it reads the DIP-Switch and echoes the setting in the LEDs. Once this test is running, change the DIP-Switch to the desired test setting and verify the setting in the LEDs.

If the LEDs reflect the correct switch setting, the specific function indicated by the switches can be executed by simply powering the unit down, and then up again.
**Indicator Light (LED) Definitions During "HYPERDIAGNOSTIC" Operation**

Except where noted otherwise, the LED indicators function as follows:

- **LED 1** is off to indicate that the selected "HYPERDIAGNOSTIC" is in progress and is not completed.
- **LED 1** is flashing to indicate that the selected "HYPERDIAGNOSTIC" is successfully completed.
- **LED 2** flashes to indicate that a two-sided diskette is being used in selected drive.
- **LED 3** is on to indicate the system is writing on a diskette. In general, you should not turn off the power while LED 3 is still on, as a FORMAT routine or SET MEDIA DENSITY may be in progress.
- **LED 4** is on to indicate the system is reading from a diskette.

As with the hardware self-tests, the controller microprocessor halts whenever it detects an error. You can determine when the microprocessor is halted by observing the green "RUN" LED shown in Figure 5-1. An error code is displayed in LEDs 5 through 8 when the microprocessor detects an error and halts. Errors that involve a host computer interface, such as non-existent memory and parity errors, do not occur during execution of any of the "HYPERDIAGNOSTICS".

Table 5-3 shows the code interpretations. The activity LED of the drive selected when the failure was detected is left on.

### Table 5-3. "HYPERDIAGNOSTIC" Error Code Interpretation

<table>
<thead>
<tr>
<th>BINARY CODE</th>
<th>INTERPRETATION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LEDs 5678</strong></td>
<td></td>
</tr>
<tr>
<td>0000</td>
<td>NO ERRORS HAVE OCCURRED SINCE POWER ON OR LAST INIT</td>
</tr>
<tr>
<td>0001</td>
<td>OPERATOR ERROR - WRITE PROTECT VIOLATION (ERREG = 100) - OR DRIVE NOT READY (ERREG = 360)</td>
</tr>
<tr>
<td>0010</td>
<td>THIS ERROR CODE NOT CURRENTLY ASSIGNED</td>
</tr>
<tr>
<td>0011</td>
<td>IBUS CABLE BACKWARDS OR INTERFACE MODULE WITHOUT POWER</td>
</tr>
</tbody>
</table>

5-14
<table>
<thead>
<tr>
<th>BINARY LED 5678</th>
<th>INTERPRETATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0100</td>
<td>DRIVE BUS CABLE IS INSTALLED BACKWARDS</td>
</tr>
<tr>
<td>0101</td>
<td>INDETERMINATE DENSITY (ERREG = 260)</td>
</tr>
<tr>
<td>0110</td>
<td>SEEK ERROR (ERREG = 150)</td>
</tr>
<tr>
<td>0111</td>
<td>THIS ERROR CODE NOT CURRENTLY ASSIGNED</td>
</tr>
<tr>
<td>1000</td>
<td>*DATA CRC ERROR (ERREG = 200)</td>
</tr>
<tr>
<td>1001</td>
<td>SECTOR UNRECOVERABLE (ERREG = 070, 120, 130, 160, OR 170)</td>
</tr>
<tr>
<td>1010</td>
<td>DRIVE READ SIGNAL LOST (ERREG = 110)</td>
</tr>
<tr>
<td>1011</td>
<td>READ/WRITE CONTROLLER FAILURE (ERREG = 220, 320, OR 330)</td>
</tr>
<tr>
<td>1100</td>
<td>MASTER CONTROLLER FAILURE (ERREG = 340)</td>
</tr>
<tr>
<td>1101</td>
<td>DRIVE FAILURE (ERREG = 010, 020, 030, 050)</td>
</tr>
<tr>
<td>1110</td>
<td>DATA PATTERN READ NOT THE SAME AS PATTERN WRITTEN</td>
</tr>
<tr>
<td>1111</td>
<td>WRITE OR WRITE-FORMAT FAILURE (ERREG = 270 or 370)</td>
</tr>
</tbody>
</table>

*Most CRC errors are attributed to worn media. Switch diskettes and restart the "HYPERDIAGNOSTIC" by cycling the AC power switch.
TEST STRATEGY USING "HYPERDIAGNOSTICS"

A substantial portion of a DSD 480 system can be checked using only "HYPERDIAGNOSTIC" routines included in the controller microcode. No host computer or interface module is required to perform the initial test procedure described below.

This procedure is used to confirm that the controller/drive subsystem is fully operational but any system malfunction related to an interface module or interface cable will not be detected. If your system is either unable to boot or unable to run the programs on diagnostic diskette, the "HYPERDIAGNOSTICS" are an excellent way to determine if the problem lies in the interface module/cable or in the controller/drive subsystem. The following procedure describes how to check your DSD 480 with "HYPERDIAGNOSTICS".

1) **Verify the power switch is OFF.**

2) Remove the top cover by turning the three fasteners at the rear of the computer and sliding it straight off.

3) Connect the AC power cord. Make sure the interface cable is not connected to the DSD 480 chassis.

4) Place write-enabled, blank, formatted diskettes in both drive 0 and drive 1.

5) Using a ball point pen, or similar object, place the code 10000001 in DIP-Switch. This particular code selects the DIP-SWITCH/1 HYPERDIAGNOSTIC test.

6) Power-up the unit by flipping the power switch ON. The RUN light or Light Emitting Diode) should remain on. Lights 1 through 8 should echo the settings of switches 1 through 8 by being lighted for a binary "1" and off for binary "0".

7) Place the code 11110001 (GENERAL EXERCISER TEST) in the DIP-Switch. Verify that lights 1 through 4 and 8 are on and 5 through 7 are off.

8) Start the general exerciser test by turning power off and then back on. The test will start on drive 1. After about 6½ minutes, the test should switch to drive 0.

The test will continue alternating between drives until power is removed or an error is detected. If an error occurs, the microprocessor will HALT, causing the RUN light to extinguish. An error code will be displayed in LEDs 5 through 8. The controller/drive subsystem should be considered fully functional if the GENERAL EXERCISER TEST be run for a half hour or longer without the occurrence of an error halt. Should an error occur, make sure you are using good quality diskettes. If you believe the unit is malfunctioning, contact the Data Systems Design Customer Service Department for assistance.
NOTE

The hardware self-tests and the "HYPERDIAGNOSTICS" report errors by writing an error code in LEDs 5 through 8 and then halting. The microprocessor executes the hardware self-tests before it gets to the switches. LED 2 will be ON following an error detected by the hardware self-test routines. LED 2 is OFF following an error detected by most of the "HYPERDIAGNOSTIC" routines.

LEDs 5 through 8 have a different meaning when the microprocessor is executing a "HYPERDIAGNOSTIC" routine but has not yet detected any error. If the RUN LED is still ON, LEDs 5, 6, and 7 encode density, and LED 8 encodes selected drive. Coding is shown in Table 5-4.

<table>
<thead>
<tr>
<th>LED #</th>
<th>DENSITY OF SELECTED DISK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>DEC SD/IBM 1, 2 - 128 (IBM 3740)</td>
</tr>
<tr>
<td>0 0 1</td>
<td>IBM 1, 2 - 256</td>
</tr>
<tr>
<td>0 1 0</td>
<td>IBM 1 - 512</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Indeterminate Density (Drive probably not ready)</td>
</tr>
<tr>
<td>1 0 0</td>
<td>IBM 2D - 256</td>
</tr>
<tr>
<td>1 0 1</td>
<td>IBM 2D - 512</td>
</tr>
<tr>
<td>1 1 0</td>
<td>IBM 2D - 1024</td>
</tr>
<tr>
<td>1 1 1</td>
<td>DEC DD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LED 8</th>
<th>SELECTED DRIVE</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>0</td>
</tr>
<tr>
<td>ON</td>
<td>1</td>
</tr>
</tbody>
</table>

INDIVIDUAL "HYPERDIAGNOSTIC" TESTS

There are five types of "HYPERDIAGNOSTIC" tests. Each type is described below.
GENERAL SYSTEM EXERCISERS. These tests are designed to thoroughly exercise all parts of the DSD 480 controller/drive subsystem. IBM 3740 single density, DEC RX02 double density, and IBM 2D double density diskettes may be used.

There are two tests of this type. Unlike the other "HYPERDIAGNOSTIC" tests, these routines operate on multiple drives.

- GENERAL EXERCISER STARTING WITH WRITE-FORMAT SINGLE DENSITY (11110)

Switch 8 is used to specify the drive to be exercised. As an example, if Switch 8 were set to a 1, the general exerciser would first exercise drive 1, then drive 0, then drive 1, etc. If Switch 8 were set to a 0, only drive 0 would be exercised. It is important that all drives to be exercised are loaded with write-enabled diskettes. The sequence of operations is listed below:

1) Execute hardware self-tests (no drives involved).
2) Write-format selected drive according to IBM 3740 single density.
3) Sequential read of all sectors on selected drive.
4) Sequential write/read of all sectors on selected drive.
5) Butterfly read of all sectors on selected drive.
6) Double density set media density on selected drive.
7) Sequential read of all sectors on selected drive.
8) Sequential write/read of all sectors on selected drive.
9) Butterfly read of all sectors on selected drive.
10) Single density set media density on selected drive.
11) Determine next logical drive unit, and if that unit has not already been write-formatted once, go to step (2); otherwise go to step (3).

This general exerciser test takes about six minutes per drive, including the write-format cycle that occurs during the first pass for each drive.

- GENERAL EXERCISER (11111)

This test is similar to the previous one (11110), except that Step (2) is not executed.

- SINGLE PASS GENERAL EXERCISER WITH FORMAT (10111XIX)

This test is similar to the general exerciser (11110) except that after one pass the test will end and flash LED #1 if no error occurs. This test includes a write format before any reads or writes are attempted.
• SINGLE PASS GENERAL EXERCISER WITHOUT FORMAT (10111X0X)

This test is a one pass general exerciser without the format before reads or writes. After successful completion, LED #1 will flash. If errors occur, they will be displayed in LEDS #4 to #8.

DRIVE ALIGNMENT ROUTINES. These routines are used with an alignment diskette available from the drive manufacturer. These routines execute even if no diskette is installed and/or the drive door is left open. No ERROR-HALT will occur if the selected drive is not ready. The following is a description of the six test routines executed by the microprocessor:

• HEAD LOAD TIMING ADJUSTMENT ROUTINE (00100)

This routine starts by moving the selected drive's read/write head to track 00. Once there, the head is loaded and unloaded at approximately 5 times per second. The head is loaded for 100 milliseconds before the cycle is repeated. The routine is terminated by disconnecting AC power from the chassis.

• TRACK 00 DETECTOR ASSEMBLY ADJUSTMENT ROUTINE (00101)

This routine starts by moving the selected drive's read/write head to track 00. The head is then alternately moved between track 01 and track 02 about once every 70 milliseconds. The head is loaded during this test. The routine is terminated by disconnecting AC power.

• SEEK TRACK 01 AND LOAD HEAD (00110)

This routine starts by moving the selected drive's read/write head to track 00. Next, the head is positioned at track 01 and loaded against the media. The head remains loaded until power is removed.

• SEEK TRACK 02 AND LOAD HEAD (00111)

This routine starts by moving the selected drive's read/write head to track 00. Next, the head is positioned at track 02 and loaded against the media. The head remains loaded until power is removed.

• SEEK TRACK 38 AND LOAD HEAD (01000)

This routine starts by moving the selected drive's read/write head to track 00. Next, the head is positioned at track 38 and loaded against the media. The head remains loaded until power is removed.

• SEEK TRACK 76 AND LOAD HEAD (01001)

This routine starts by moving the selected drive's read/write head to track 00. Next, the head is positioned at track 76 and loaded against the media. The head remains loaded until power is removed.
To take the drives out of the DSD 480 system, remove the screws from the bottom of the chassis so that the drives can be turned on their side. Many of the adjustment screws and oscilloscope test points are located on the underside of the drives.

**DRIVE INDEPENDENT SYSTEM TESTS.** These tests are designed to exercise those parts of the DSD 480 controller which are not drive-dependent. There are five tests of this type:

- **TEST READ/WRITE CONTROLLER (01100)**
  
  This routine causes the read/write controller hardware to be continuously cycled through its internal self-test microcode. Run this test if you believe the read/write controller hardware is not performing reliably. Should this test generate an error, the code is 1011. LED 2 will also be ON if this error is reported.

- **TEST PHASE LOCKED LOOP/CRC GENERATOR (01101)**
  
  This routine checks the operation of the phase locked loop (PLL) circuitry by counting the number of PLL CLOCK cycles that occur during a 50 millisecond interval. This test determines if a READ problem is being caused by the phase locked loop circuitry. If it is, the error code is 1010.

  **NOTE**

  LED 2 will be on if this error is reported.

  The second half of this test verifies that the CRC generator/checker and serial data path are functioning properly. If this test detects a malfunction, the error code is 1100. LED 2 will also be on.

- **TEST CABLE ORIENTATION (01110)**
  
  This test is used to verify that both the interface bus cable (connecting the controller to the interface module) and the drive bus cable (connecting the controller to the drives) are installed correctly. The interface bus cable must be connected on both ends and the interface module must have power in order to run this test. The interface bus cable must be disconnected at one or both ends when running all "HYPERDIAGNOSTIC" tests EXCEPT this one. If there is an error, Table 5-4 indicates which cable is causing the problem. If there is no cable at all, this test will pass.

- **HARDWARE SELF-TEST LOOP (01111)**
  
  The DSD 480 microprocessor executes the hardware self-test once after powering up. When this "HYPERDIAGNOSTIC" routine is selected, the
microprocessor keeps executing the hardware self-test indefinitely until either power is removed or an error is detected. LEDs 5, 7, and 8 flash on and off when this routine is executing error-free.

NEW TEST

• EXTENDED HARDWARE SELF-TEST LOOP (01011)

The DSD 440 Microprocessor executes the Standard hardware self test done on power up then it tests the read/write controller CRC Generator and phase lock loop. The sequence is repeated until power down or an error is detected. Led's 5, 6, 7 and 8 flash when this routine is executing error free.

• DIP-SWITCH/LED TEST ROUTINE (10000)

This routine is used to determine if the microprocessor can read all 8 switches in the DIP-Switch, and illuminate LED's 1 through 8. The routine reads the DIP-Switch and writes that byte to the LED bank. For example, if Switch 2 is in the 1 position, then LED 2 is on. If Switch 2 is in the 0 position, then LED 2 is off.

Since the microprocessor is executing this loop continuously, the state of a LED should appear to change immediately following a switch position change.

This is the only case in which the settings of the DIP-Switch should be changed with power on. Changing them at other times can cause erroneous operation.

These tests are terminated by removing power.

DRIVE RELATED SYSTEM TESTS. These tests are designed to exercise the drives on the assumption the DSD 480 controller is fully operational. There are five tests of this type:

• BUTTERFLY SEEK TEST (10001)

This routine starts by moving the selected drive's read/write head to track 00. The head positioner is then moved back and forth in a "butterfly" pattern. This pattern consists of the following series of tracks: 76, 01, 75, 02, 74, 03 . . . After one complete cycle, the microprocessor tries to move the head positioner to track 00. If the track 00 signal is not asserted, the error code is reported in the LED indicators and the microprocessor halts. If the track 00 signal is asserted, the test is repeated.

• CONTINUOUS SEQUENTIAL SCAN TEST (10010X0X)

This routine starts by moving the selected drive's read/write head to track 00. The head is then loaded and the media density is determined and displayed in the LEDs. The controller then sequentially reads every sector of every track. If no errors occur, the test is repeated. If an error does occur, the microprocessor halts and the error code is displayed in LEDs 5 through 8.
The meanings associated with the 16 possible error codes are shown in Table 5-4. The code displayed in LEDs 5 through 8 is not an error code UNLESS the green LED (LED 9) is off and the head positioner is not moving.

- SINGLE PASS SEQUENTIAL SCAN TEST (10010X1X)

This routine does the same seek/read pattern as the continuous sequential scan, but after 1 pass the test is ended. If successful, LED #1 will flash and the scan will end.

- BUTTERFLY SCAN TEST (10011)

This routine is similar to the sequential scan test, except for the sequence of tracks read. This test takes longer than the sequential scan test to read the same total number of sectors because of the added positioner step and head load time. This test detects problems associated with seeking and/or reading.

NOTE

The data on the diskette during the above two tests are ignored. Only a CRC error or other hardware detected error will be reported.

- SEQUENTIAL WRITE/READ TEST (11000)

This routine starts by moving the selected drive's read/write head to track 00. Next, the density of the write-enabled diskette inserted in the drive is determined. The routine then sequentially writes pseudo-random data on every track and sector of the diskette, in the appropriate density. After writing, every track and sector on the diskette is sequentially read and compared to what was written. Any error encountered is identified in the LEDs when it occurs and the machine halts. The write cycle only happens once. The read cycle is repeated indefinitely until power is disconnected or an error is detected. LEDs 3 and 4 are used to determine if the routine completes the write cycle.

These tests should be executed whenever a drive is replaced or realigned.

**DRIVE UTILITY ROUTINES.** These utilities allow formats with the DSD 480. There are eight utilities of this type:

- **WRITE-FORMAT DISKETTE IN IBM 1-128 (3740)** Single Density Format (11001X0X) (26 sector/track; 128 bytes/sector)
This routine starts by moving the selected drive's read/write head to track 00. Next the entire diskette is formatted with 26 sectors per track using the "FM" single density format. After all tracks have been written, the disk is sequentially scanned. After successful completion of the format (scan cycle, the read/write head will unload and LED #1 will flash indicating the finish of this routine.

NOTE

If a single sided disk is used, the format will be done on side #0 only. This will result in a single sided diskette that is compatible with IBM part number 2305830 (IBM 1-128).

If a double sided disk is used, both sides will be formatted. This results in a double sided diskette that is compatible with IBM part number 1766870 (IBM 2-128).

- WRITE FORMAT DISKETTE IN IBM 2D-256 Double Density Format (26 sectors/track; 256 bytes/sector) (11001X1X) (Diskette must be double sided)

This routine starts by moving the selected drive's read/write head to track 00. Next the entire diskette is write formatted with 26 sectors per track, using MFM double density bit coding. After all tracks are formatted, one sequential scan pass takes place. If the routine successfully completes the format/scan cycle, the head will be unloaded and LED #1 will flash indicating successful completion. If an error occurs, it will be displayed in LED's 5 to 8 and LED 9 will be turned off.

This results in diskettes that are compatible with IBM part number 1766872.

- WRITE FORMAT DISKETTE IN IBM 1-256 or IBM 2-256 Single Density Format. (15 sectors/track; 256 bytes/sector) (11100X0X)

This routine is the same as the 26 sector, single density format (11001X0X) except that 15 sectors per track (256 bytes per sector) are written on tracks 1 to 76. This results in diskettes that are compatible with IBM diskette numbers:

  Single sided - IBM Part Number: 2305845  
  Double sided - IBM Part Number: 2736700

- WRITE FORMAT DISKETTE IN IBM 2D-512 Double Density Format (15 sectors/track; 512 bytes/sector) (11100X1X) (Must be double sided)

This routine is the same as the 26 sector double density format (11001X1X) except that 15 sectors per track (512 bytes/sector) are written on tracks 1 to 76. This results in diskettes that are compatible with IBM diskette number 1669044.
• WRITE FORMAT DISKETTE IN IBM 1-512 Single Density Format. (8 sectors/track; 512 bytes/sector) (11101X0X) (Must be single sided diskette.)

This routine is the same as the 26 sector single density format (11001X0X) except 8 sectors per track (512 bytes/sector) are written on tracks 1 to 76.

This results in diskettes that are compatible with IBM diskette number 1669954.

• WRITE FORMAT DISKETTE IN IBM 2D-1024 Double Density Format. (8 sectors/track; 1024 bytes/sector) (11101X1X) (Must be double sided diskette)

Same as 26 sector double density format (11001X1X) except 8 sectors per track (with 1024 bytes/sector) are written on tracks 1 to 76.

Results in diskettes that are compatible with IBM part number 1669045.

• SET MEDIA TO SINGLE DENSITY (11010)

This routine starts by moving the selected drive's read/write head to track 00. Next, every sector on the write-enabled diskette is written with a single density data address mark, 128 bytes of zeroes, and 2 CRC bytes. Unlike the previous write-format routine, this one does not modify the sector headers. Control is transferred to the sequential scan test as soon as all sectors are written. LEDs 3 and 4 are used to determine when the writing has stopped and the reading has begun.

• SET MEDIA TO DOUBLE DENSITY (11011)

This routine starts by moving the selected drive's read/write head to track 00. Next, every sector on the write-enabled diskette is written with a double density data address mark, 256 bytes of DEC modified frequency modulation (MFM) zeroes and 2 Cyclic Redundancy Check (CRC) bytes. This routine does not modify the sector headers. Control is transferred to the sequential scan test as soon as all sectors are written. LEDs 3 and 4 are used to determine when the writing has stopped and the reading has begun.

These tests can also be used to reformat magnetically damaged diskettes without a computer.
CHAPTER 6

COMPUTER RESIDENT DIAGNOSTICS

All DSD flexible disk systems with an LSI-II or PDP-II interface board are shipped with a diskette containing an interactive diagnostic program called FLPEXR. This section explains the operation of this comprehensive set of tests and utility programs.

The diagnostic diskette also contains a modified driver to provide RSX-IIM, version 4.0 with DSD floppy disk support in a 22-bit Q-Bus environment. Complete procedures for installing the modified driver are contained on the diskette.

PROGRAM LOADING AND MONITOR PROTOCOL

FLPEXR requires a standard console device, an LSI-II or PDP-II computer and at least 12K words of memory. Loading FLPEXR can be accomplished by two methods. One method is to bootstrap the diagnostic diskette. This loads FLPEXR into memory automatically. The other method requires an RT-II operating system. The FLPEXR diagnostic diskette has an RT-II compatible directory and file space. The files on the diagnostic diskette can be accessed using standard RT-II procedures. For example, FLPEXR can be run from an RT-II system by typing.

```
RU<DEV:><FLPEXR <CR>
```

where<DEV:><might be DX0:, DX1:, DY0:, DY1: as appropriate.

Once the FLPEXR diagnostic program has been loaded into memory, the diagnostic diskette should be removed from the drive so it is not erased. Since both bootstrap and diagnostic programs handle RX01 and RX02 protocols, FLPEXR diagnostic diskette may be used with any DEC compatible disk system.

After FLPEXR is loaded into memory, a brief description is displayed on the terminal which includes the version number of the program and a memory map. This memory map indicates the ranges of the address space which responds with SSYNC (or BRPLY) when accessed by the host computer. A list of all the available commands may be obtained by typing an "H" (HELP).

Two high quality, write-enabled formatted diskettes should be installed in the FLPEXR drives before proceeding with any of the tests.

FLPEXR types "<CRLF>!" when starting, and then the program attempts an INIT (initialize) instruction. When the INIT cycle is successful, the program types the prompt word: "DD MODE:" or "MODE:.". This prompt string allows the operator to input a command. Each of the possible commands is described below.

Legal responses to "MODE:" are listed in Table 6-1. Only the characters enclosed in parenthesis need to be typed. The parenthesis should NOT be typed. When the typed string is recognized the terminal "BELL" will sound at which time <CR> should be typed. The program will fill in the remaining characters and then proceed to execute the function.

6-1
FLPEXR DIAGNOSTIC ROUTINES

This section describes each functional mode of interactive operation for the FLPEXR diagnostic program. The purpose of each test and all communication protocol with the operator is also described:

Table 6-1. FLPEXR Diagnostic Routines

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V)ERIFY</td>
<td>General Exerciser</td>
</tr>
<tr>
<td>(SH)ORT VERIFY</td>
<td>Short Exerciser</td>
</tr>
<tr>
<td>(M)AP ADDRESS</td>
<td>Memory and Device Map</td>
</tr>
<tr>
<td>(FI)LL EMPTY</td>
<td>Fill/Empty Buffer Test</td>
</tr>
<tr>
<td>(SEQ)READ</td>
<td>Sequential Write/Read Test</td>
</tr>
<tr>
<td>(SEQ)READ</td>
<td>Sequential Read</td>
</tr>
<tr>
<td>(RA)NDOM R/W</td>
<td>Random Read/Write</td>
</tr>
<tr>
<td>(RE)AD RANDOM</td>
<td>Read Random</td>
</tr>
<tr>
<td>(SC)AN</td>
<td>Scan</td>
</tr>
<tr>
<td>(SEE)K RANGE</td>
<td>Seek Range</td>
</tr>
<tr>
<td>(ST)ATUS</td>
<td>Display Status Information</td>
</tr>
<tr>
<td>(RE)SET STATUS</td>
<td>Change Status</td>
</tr>
<tr>
<td>(SAVE)VE STATUS</td>
<td>Save Status on Diskette</td>
</tr>
<tr>
<td>(DUMP C)IR BUFFER</td>
<td>Display Circular Output Buffer</td>
</tr>
<tr>
<td>(SET U)NIT</td>
<td>Set Unit</td>
</tr>
<tr>
<td>(SE)T T)RACK</td>
<td>Set Track Limits</td>
</tr>
<tr>
<td>(SE)CTOR INCREMENT</td>
<td>Specify Sector Interleave</td>
</tr>
<tr>
<td>(I)NTERRUPT</td>
<td>Set Interrupt Status</td>
</tr>
<tr>
<td>(DE)NSITY LOCKUP</td>
<td>Lock Density to Current Density</td>
</tr>
<tr>
<td>(SET D)EVICE</td>
<td>Set Device</td>
</tr>
<tr>
<td>(SET M)EDIA DENSITY</td>
<td>Set Media Density</td>
</tr>
<tr>
<td>(F)ORMAT</td>
<td>Format Diskette</td>
</tr>
<tr>
<td>(DU)PLICATE</td>
<td>Duplicate</td>
</tr>
<tr>
<td>(CO)MPARE</td>
<td>Compare by Sector</td>
</tr>
<tr>
<td>(DUMP O)CTAL</td>
<td>Data Dump in Octal Format</td>
</tr>
<tr>
<td>(DUMP B)YTE</td>
<td>Data Dump in Byte Format</td>
</tr>
<tr>
<td>(DUMP A)SCII</td>
<td>Data Dump in ASCII Format</td>
</tr>
</tbody>
</table>

- VERIFY — (V)ERIFY

The VERIFY test does one pass of a SHORT ACCEPTANCE TEST, on the first 7 tracks and then resets the limit variables back to the normal default values. It then induces an automatic "CTRL P" to inhibit all but error printout and initiates the long verify test.
EXAMPLE VERIFY
SESSION
(Operator responses underlined)

#DD MODE: VERIFY<CR>

HAVE YOU INSTALLED 'SCRATCH' DISKS?(Y OR N): Y
SET DENSITY TO (S, D): S
ARE YOU SURE? (Y OR N): Y
VERIFY TEST NOW STARTING

SCAN CRC CHECKED WRITING READING
INTERRUPTS ENABLED
WRITING READING

- SHORT VERIFY -- (SH)ORT VERIFY

This interactive program changes the track range used by the VERIFY TEST so that only the first 9 tracks of each selected drive are tested. This SHORT VERIFY TEST is repeated until stopped.

- HELP

The HELP command causes all the valid "MODE:" responses to be displayed on the console terminal. The "MODE:" prompt is typed when this function is complete.

- MAP ADDRESS -- (M)AP ADDRESS

The MAP ADDRESS command causes a memory and device address map of your system to be displayed on the console terminal. This is the same map displayed when the FLPEXR program is first loaded. In addition, the interrupt vector address associated with each disk interface is displayed. The "MODE:" prompt is typed when this function is complete.

EXAMPLE "MAP ADDRESS"

#DD MODE: MAP ADDRESS<CR>

( 0 - 157776)
( 160100 - 160106 )
( 165000 - 165776 )
( 171000 - 171776 )
( 172300 - 172316 )
( 172340 - 172356 )
( 172520 - 172536 )
( 173000 - 173776 )
( 176700 - 176746 )
( 177170 - 177172 )
EXAMPLE "MAP ADDRESS" (Continued)

#DD MODE: MAP ADDRESS CR

( 177510 - 177516 )
( 177546 - 177546 )
( 177560 - 177616 )
( 177640 - 177656 )
( 177776 )

DEV: 177170 INT @ 264

NOTE

This example indicates that a device is installed at location 177170 with interrupt vector at location 264.

• FILL-EMPTY -- (FILL) EMPTY

The FILL-EMPTY test checks the FILL BUFFER and EMPTY BUFFER controller commands. If the controller under test is configured in RX01 compatible mode, then the test involves only programmed I/O. If the controller is configured as an RX02, the controller does FILL/EMPTIES into three different buffers so as to verify proper operation of all possible address bits. FILL/EMPTIES are done in both densities covering all possible word counts. Since this test does not manipulate the drives, the system will operate in silence. This test continues until you type a "CTRL R".

• SEQUENTIAL WRITE/READ -- (SEQW)/R

The SEQUENTIAL WRITE / READ test writes pseudo-random data sequentially on all selected drives. The test then reads all the data and checks it. The message "WRITING" is typed on the console terminal when the test first starts writing. The message "READING" is typed when the test starts reading. This test continues until the operator types "CTRL R". It also performs a set media density operation if the diskette is not of the expected density.

NOTE

The following three tests require a SEQUENTIAL WRITE pass be done first in order to initialize the pseudo-random data. Data compare errors are reported if this is not done.

• SEQUENTIAL READ -- (SEQ)READ

The SEQUENTIAL READ test reads the data on all selected drives sequentially and compares the data pattern against what was written. The program types "READING" at the beginning of each pass. This test continues until you type "CTRL R".

6-4
- **RANDOM READ/WRITE -- (R)ANDOM R/W**

  The RANDOM READ/WRITE test selects a random sector of a selected drive, then reads or writes it. It checks data when appropriate. This test continues until you type "CTRL R".

- **READ RANDOM -- (R)EAD RANDOM**

  The READ RANDOM test reads randomly selected sectors. Data is checked following each read. This test continues until you type "CTRL R".

- **SCAN -- (S)CAN**

  The SCAN test reads all sectors on all selected drives sequentially and checks for CRC errors. It also determines media density. No direct data checking takes place in this test. Only status is checked. After all units are scanned once, the "MODE:" prompt is displayed on the console.

- **SEEK RANGE -- (S)EIK RANG**

  The SEEK RANGE function is a versatile drive test that performs all possible seeks within the operator specified track and seek length boundaries. It specifies a read on the first sector that can be read on the destination track after compensating for step and head load times. Thus it is a worst case test of the drive stepper motor and head setting. Track status information will be continuously displayed during execution of this test.

  **EXAMPLE**

  
  #DD MODE: SEEK RANGE

  NOTE: ALL TIMES ARE GIVEN IN 'OCTAL' TENTHS OF MSEC

  SEEK LENGTH ( 1 ): 3 THROUGH ( 27 ): 30
  850 SEEK TIME ( 36 ): 850 SECTOR OFFSET: ( 4 ): 800 SEEK TIME: ( 120 ): 800 SECTOR OFFSET ( 6 ): COVERING TRACTS ( 0 ): 1 THROUGH ( 114 ): 10 3 4 ...

- **STATUS -- (S)TATU**

  The STATUS function causes all the current status information including hardware errors, data errors, and pass counts to be displayed on the console terminal. Displaying status information does not reset the status counts. See the RESET STATUS function below. The "MODE:" prompt is typed when this function is complete.
EXAMPLE

#MODE: STATUS<CR>

UNIT #0 #BAD=3 #RD/WRT=2049 #XFERS=0 B-DATA=0 ST=110 #='3

- **RESET STATUS -- (RES)ET STATUS**

  The RESET STATUS function first displays all the available status counts. Next, the display will ask whether all of the status counts need resetting. You respond with a "Y", all of the error, pass, etc. counts will be reset to zero. The "MODE:" prompt is typed when this function is complete.

- **SAVE STATUS -- (SA)VE STATUS**

  The SAVE STATUS command causes all the status counts associated with a particular drive to be written on track 0, sector 1 of the diskette in that drive. Only the SET MEDIA DENSITY commands over-write track 0, so the status data associated with each drive can be safely stored away. This function is used by the acceptance test so that it can survive a loss of main computer CPU memory without any loss of cumulative error data. The "MODE:" prompt is typed when this function is complete.

- **RECOVER STATUS -- (REC)OVER STATUS**

  The RECOVER STATUS routine performs the opposite function performed by the SAVE STATUS function. The status data stored away on track 0, sector 1 of the diskette in each drive is transferred back from the diskette to the status/counter variables in memory. The "MODE:" prompt is displayed when this function is complete.

- **DISPLAY CIRCULAR OUTPUT BUFFER -- (DUMP C)IR BUFFER**

  The DUMP C function is used to display the output buffer associated with all console terminal output. This function is useful on systems where the console terminal is a CRT. Messages previously output can be re-examined on the console. The buffer can be cleared after it is displayed by this function.

**MODE SETTING COMMANDS:**

- **SET UNIT -- (SET U)NIT**

  This function enables the operator to specify which drives are to be accessed by the various test functions. The default drives are units 0 and 1. The currently selected units are printed first. It prompts with "UNIT:", expecting a number between 0 and 3, inclusive. Unit numbers are accepted as long as they are valid. When a non-number is typed to a unit request, the units currently selected are prompted and the program returns to MODE.
NOTE

1) If using a two drive system then selection of units 2 and 3 is invalid and will cause an error.

2) If units are set by "SET DEVICE", "SET DEVICE" will override "SET UNIT" - Example: "SET UNIT". See the "SET DEVICE" function for more information.

EXAMPLE OF
"SET DEVICE" overriding "SET UNIT"

#DD MODE: SET UNIT<CR>
- LOADED BY SET DEVICE FLAGS
  UNITS SELECTED 0

• SET TRACK -- (SET T)RACK

This function enables the operator to specify lower and upper track limits for all other test functions. The default lower track limit is track 0 and upper track limit is track 76. The "MODE:" prompt is issued after you enter the new limits.

EXAMPLE

"SET TRACK" used to set track range from track 1 to track 10

#DD MODE: SET TRACK<CR>
FROM 0: 1 THROUGH 14: 10

• SECTOR INCREMENT -- (SEC)TOR INCREMENT

This function enables you to specify the sector increment value. The number is added to the present sector address to determine the next sector address in the functions that read multiple sectors on a single track. If this number were 1 and the diskette did not have an interleaved format, an entire revolution would be required to read each sector. On LSI-11 processors, the default increment value is 3. On PDP-11 processors the default increment value is 2. The "MODE:" prompt is issued after the new value has been entered.

#DD MODE: SECTOR INCREMENT = 3-2<CR>
#DD MODE: SECTOR INCREMENT = 2-3<CR>

• SET INTERRUPT STATUS -- (I)NTERRUPT

The SET INTERRUPT STATUS function enables you to test the disk system with interrupts either enabled or disabled. If interrupts are enabled, the program ensures that an interrupt occurs whenever it is appropriate. The operator
enters a 0 to disable interrupts and a 1 to enable interrupts. This function is also used in ACCEPTANCE and VERIFY to set "Interrupts Enabled" and "Interrupts Disabled".

EXAMPLE

#DD MODE: INTERRUPT<CR>
CURRENTLY INTERRUPTS ARE DISABLED (D)
INPUT NEW STATUS (ENABLE OR DISABLE)
(E OR D): D

• DENSITY LOCKUP -- (DE)NSITY LOCKUP

The "DENSITY LOCKUP" function allows you to lock the current disk density during the various tests. This feature is useful when testing for a problem that occurs in one density only, or when the disk density can not be changed by a SET MEDIA DENSITY function.

EXAMPLE

#DD MODE: DENSITY LOCKUP<CR>
DENSITY IS CURRENTLY UNLOCKED
DO YOU WISH TO LOCK THE DENSITY (Y or N): Y

#DD MODE:

• SET DEVICE -- (SET D)EVICE

This function facilitates testing controllers that are not configured at the standard device I/O address and interrupt vector. It also enables the FLPEXR test program to simultaneously exercise multiple controllers. The function protocol asks you for device address, interrupt vector, and flag word. If a space is typed, the program steps past that field, leaving it intact. To return to "MODE:", type a "CR" (carriage return) in response to "RXCS:". The flag word is organized as follows:

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA</td>
<td>DBS</td>
<td>DDN</td>
<td>US3</td>
<td>US2</td>
<td>US1</td>
<td>US0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

When set to a 1, the bit labeled:

DMA indicates the device should be tested as an RX02.
DBS indicates the device is double sided.
DDN indicates double density operation is enabled.
US3 indicates this device contains a drive unit 3.
US2 indicates this device contains a drive unit 2.
US1 indicates this device contains a drive unit 1.
US0 indicates this device contains a drive unit 0.

US0, US1, US2, US3 do an implicit "SET UNIT" function when set. The normal flag variable for RX02 mode is 4400 (octal). The normal flag variable for RX01 is 0000 (octal). The normal flag for double sided RX02 operation is 7400 (octal).
EXAMPLE SET DEVICE

MODE: SET DEVICE<CR>

SET THE DEVICE FLAGS FOR EACH SYSTEM AS FOLLOWS:

4000: ENABLES DMA OPERATION IF AVAILABLE
2000: SETS 850 TIMING (ELSE 800)
1000: ENABLES DOUBLE SIDED OPERATION IF DOUBLE SIDED DRIVE AND DISK USED
400: ENABLE DENSITY SWITCHING IF RX02/440/480
20: ENABLE UNIT #1 ON CURRENT DEVICE
10: ENABLE UNIT #0 ON CURRENT DEVICE

RXCS @ 177170: INT @ 264 INTVEC = 264 FLAGS:4400 6410
RXCS @ 0:

FORMAT INITIALIZATION COMMANDS

- SET MEDIA DENSITY (SET MEDIA DENSITY)

  This function enables the operator to initialize a diskette to single density or double density format. The function prompts for function confirmation, unit, and desired density. To select single density, respond with an "S". Type "D" to select double density.

  The SET MEDIA DENSITY command is used to implement this function, so no headers are rewritten; however, this causes any status that may have been saved on track 0, sector 1 to be erased. The "MODE:" prompt is issued when this function is complete. This function causes any status saved on track 0, sector 1 to be erased.

  #MODE: SET MEDIA DENSITY<CR>

  DO A SET MEDIA ON ALL DEVICES? (Y OR N):N
  UNIT: SET DENSITY TO (S,D):S
  ARE YOU SURE? (Y OR N):Y

- REFORMAT -- (FO)RMAT

  This function is used to rewrite diskette headers, as well as all the other data on a particular diskette. It also prompts you for confirmation, unit, and sequential or interleaved format.
  Sequential track header format is 01, 02, 03, ..., 24, 25, 26.

  RT-II maps block numbers 0,1 ... into the sector sequence 1,3,5,7, 9,11,13,15, ... to achieve a "two-way interleave". This provides enough time to process each sector before the next sector comes around on the diskette. The interleave option in FORMAT writes the following sequence of sector numbers on the diskette following the index pulse:

  01 19 12 03 21 14 05 23 16 07 25 08 09
  02 20 11 04 22 13 06 24 15 08 26 17 10

6-9
When the two way logical sector interleave generated by RT-II is combined with the physical sector sequence written on the diskette by the FORMAT interleaved function, a net three-way system interleave is achieved, thus there are two physical sectors between logical registers 1 and 3. This improves system throughput when there is heavy input/output overhead, as often occurs with foreground/background monitor.

**#MODE: FORMAT**

**ARE YOU SURE? Y**

A PARTIAL FORMAT IS GOING TO OCCUR COVERING TRACK 1 to TRACK 10 UNIT: O

**SEQUENTIAL SECTOR FORMAT? (Y OR N): Y**

<table>
<thead>
<tr>
<th>DENSITY</th>
<th>TYPE</th>
<th>SUPPORTED ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEC SD(IBM SD 2-128)</td>
<td>0</td>
<td>440,480,210,110</td>
</tr>
<tr>
<td>DEC DD</td>
<td>1</td>
<td>440,480</td>
</tr>
<tr>
<td>DEC SD(ALL OF DISK)</td>
<td>2</td>
<td>470,480</td>
</tr>
<tr>
<td>DEC DD(ALL OF DISK)</td>
<td>3</td>
<td>470,480</td>
</tr>
<tr>
<td>IBM SD (2-256)</td>
<td>4</td>
<td>480</td>
</tr>
<tr>
<td>IBM SD (2-512)</td>
<td>5</td>
<td>480</td>
</tr>
<tr>
<td>IBM DD (2D-256)</td>
<td>6</td>
<td>480</td>
</tr>
<tr>
<td>IBM DD (2D-512)</td>
<td>7</td>
<td>480</td>
</tr>
<tr>
<td>IBM DD (2D-1024)</td>
<td>8</td>
<td>480</td>
</tr>
</tbody>
</table>

**DESired SELECTION? (0 to 8): 4**

**DO YOU WISH TO DO SIDE #0? (Y OR N): Y**

**DO YOU WISH TO DO SIDE #1? (Y OR N): Y**

**DUMP AND COPY UTILITY COMMANDS**

**NOTE**

The SECTOR INCREMENT function may be used to specify sector sequencing.

- **DUPLICATE -- (DUP)LICATE**

The DUPLICATE utility command enables the operator to make a duplicate copy of a diskette. The function prompts for a source drive unit number and a destination drive unit number. For each possible sector address, the function performs a READ SOURCE SECTOR, WRITE DESTINATION SECTOR, READ DESTINATION SECTOR, and COMPARE DATA.

**#DD MODE: DUPLICATE<CR>**

SOURCE UNIT: 0

TO DESTINATION UNIT:

TO DESTINATION UNIT:

- **COMPARE -- (CO)MPARE**

The COMPARE utility command enables the operator to compare two diskettes starting at a specific address. The function prompts for: SOURCE UNIT,
STARTING TRACK, STARTING SECTOR, NUMBER OF SECTORS, and DESTINATION UNIT.

- OCTAL DUMP BY SECTORS -- (DUMP O)CTAL

This utility command enables the operator to cause an octal dump of specified sectors to the console terminal. The function prompts for: UNIT, STARTING TRACK, STARTING SECTOR, and NUMBER OF SECTORS.

#DD MODE: DUMP OCTAL CR
SOURCE UNIT:0 TRACK: 0 SECTOR: 1 # SECTORS:2 DDEN DRIVE #0 AT TRACK #0, SECTOR #1 SIDE #0
SC=1
0: 0 0 0 3776 0 0 0 0
20: 0 0 0 0 0 0 0 0
40: 0 0 0 0 0 0 0 0
60: 0 0 0 0 0 0 0 0
100: 0 0 0 0 0 0 0 0
120: 0 0 0 0 0 0 0 0
140: 0 0 0 0 0 0 0 0
160: 0 0 0 0 0 0 0 0
200: 0 0 0 3722 0 0 0 0
220: 0 0 0 0 0 0 0 0
240: 0 0 0 0 0 0 0 0
260: 0 0 0 0 0 0 0 0
300: 0 0 0 0 0 0 0 0
320: 0 0 0 0 0 0 0 0
340: 0 0 0 0 0 0 0 0
360: 0 0 0 0 0 0 0 0
DDEN DRIVE #0 AT TRACK #0, SECTOR #4 SIDE #0
SC=2
0: 0 0 0 0 0 0 0 0
20: 0 0 0 0 0 0 0 0
40: 0 0 0 0 0 0 0 0
60: 0 0 0 0 0 0 0 0
100: 0 0 0 0 0 0 0 0
120: 0 0 0 0 0 0 0 0
140: 0 0 0 0 0 0 0 0
160: 0 0 0 0 0 0 0 0
200: 0 0 0 0 0 0 0 0
220: 0 0 0 0 0 0 0 0
240: 0 0 0 0 0 0 0 0
260: 0 0 0 0 0 0 0 0
300: 0 0 0 0 0 0 0 0
320: 0 0 0 0 0 0 0 0
340: 0 0 0 0 0 0 0 0
360: 0 0 0 0 0 0 0 0

- BYTE DUMP BY SECTORS -- (DUMP B)YTE

This utility command enables the operator to cause a binary dump of specified sectors to the console terminal. The function prompts for: UNIT, STARTING TRACK, STARTING SECTOR, and NUMBER OF SECTORS.
ASCII DUMP BY SECTORS -- (DUMP A)SCII

This utility command enables the operator to cause an ASCII dump of specified sectors to the console terminal. The function prompts for: UNIT, STARTING TRACK, STARTING SECTOR, and NUMBER OF SECTORS.

For more details on the above listing, refer to the program listing from the source files included on the diagnostic diskette.

FLPEXR PROGRAM STATUS AND ERROR DISPLAYS

FLPEXR types out error and status information under a wide variety of circumstances. All printouts to the console terminal are sent to a circular buffer in memory as well. The buffer size is determined by available memory. The circular buffer is useful if a hard copy console terminal is not being used and you need to examine error printouts no longer on the face of the CRT screen. The display output buffer (DUMP C) function is used to examine messages in the circular buffer. Each of the status variables that might appear on the console terminal is explained below:

DEV XXX Is printed only when running multiple controllers. XXX are the last 3 octal digits of the RXCS address for the system whose error/status data is being displayed.

UN U U represents the logical drive unit number for which the error/status data is being displayed.

TRACK= TK Track address at time of status/error printout.
SECTOR= SC Sector address at the time of status/error printout.
RXCS= XY Shows the contents of the command and status register.
RXDB= XY Shows the contents of the data buffer register. It should normally be 0 or 214 octal following an INIT.

INTERRUPT ERROR: X if X is less than 0, this indicates that an expected interrupt failed to occur. If X is greater than 0, this indicates that more than one interrupt occurred.

#BAD= XX This variable indicates the number of status errors detected.

#RD/WRT= XX This variable indicates the number of sectors that were transferred error-free.

#XFERS= XX This variable indicates the number of fill/empty command cycles that were completed successfully.

B-DATA= XX Number of data errors where a byte or word of data did not compare with the value the program was expecting. This is different than a CRC error, which would be counted as bad status. There can be up to 128 data errors in 1 sector.
DEFSTT = DEFINITIVE ERROR STATUS  Error code associated with the error currently being displayed. The meaning of each error code can be found in Table 5-2.

SIDE I  Indicates an error has occurred on side I (second side of a diskette). Error messages not specifying side I relate to side 0.

If in RX02 compatible mode, and CTRL L has been typed to select expanded error printout mode, the following additional status variables appear in the error printout:

D0@TK = TK  Track address of drive 0
D1@TK = TK  Track address of drive 1
CURTK = TK  Track address of the current selected logical unit
CSCT = SC  Sector address of the current selected logical unit
DSTT = XX  Drive status byte - each of the bits in this status byte is used to encode some information about one or both of the flexible disk drives and/or the media presently installed. The bits get decoded into words which are displayed with the other status. These words are explained below.

US0  Drive 0 is currently selected
US1  Drive 1 is currently selected
DNOL  Drive 0 currently contains a low density diskette
DN0H  Drive 0 currently contains a high density diskette
DNIL  Drive 1 currently contains a low density diskette
DN1H  Drive 1 currently contains a high density diskette
HDUP  Head on currently selected unit is up (unloaded)
HDLD  Head on currently selected unit is loaded
TRKRD = TK  Track address read from a sector header. This number would only be useful following a DEFSTT = 150 error.

DEF-RXDB = XX  Contents of the RXDB following a definitive error status command.

A number of 2-character activity codes are displayed in the context of error printouts. The codes listed below indicate what the diagnostic was doing when the error was detected.

<table>
<thead>
<tr>
<th>ACTIVITY</th>
<th>CODE</th>
<th>MEANING</th>
</tr>
</thead>
<tbody>
<tr>
<td>FILL-EMPTY</td>
<td>FB</td>
<td>Problem loading sector buffer</td>
</tr>
<tr>
<td>FILL-EMPTY</td>
<td>E1,E2</td>
<td>Sector buffer data did not check during an empty buffer operation</td>
</tr>
<tr>
<td>FILL-EMPTY</td>
<td>FL,EL</td>
<td>DMA fill or empty error to low mem. buffer</td>
</tr>
<tr>
<td>FILL-EMPTY</td>
<td>FD,ED</td>
<td>DMA fill or empty error to ctr. mem. buffer</td>
</tr>
<tr>
<td>ACTIVITY</td>
<td>CODE</td>
<td>MEANING</td>
</tr>
<tr>
<td>------------------</td>
<td>-------</td>
<td>--------------------------------------------------------------------------</td>
</tr>
<tr>
<td>FILL-EMPTY</td>
<td>FH, EH</td>
<td>DMA fill or empty error to high mem. buffer</td>
</tr>
<tr>
<td>SEQ. WRITE</td>
<td>SW, CW</td>
<td>Problem during sequential write</td>
</tr>
<tr>
<td>SEQRD</td>
<td>SR</td>
<td>Problem during sequential read</td>
</tr>
<tr>
<td>RANDOM</td>
<td>RW, RC, RR</td>
<td>Random (write, check, read) activity when error was detected</td>
</tr>
<tr>
<td>ANY READ RETRY</td>
<td>XE</td>
<td>Empty buffer check before retrying read</td>
</tr>
<tr>
<td>DUP UTILITY</td>
<td>IN</td>
<td>Error reading the source diskette</td>
</tr>
<tr>
<td>DUP UTILITY</td>
<td>CW</td>
<td>Error checking what was just written</td>
</tr>
<tr>
<td>DELETED DATA</td>
<td>DW, DR</td>
<td>Deleted data flag failure</td>
</tr>
</tbody>
</table>

The following printouts are examples of what the FLPEXR diagnostic program outputs to the console under varying circumstances.

**EXAMPLE 1:** Operator requests status of currently selected drive during a test by typing LF.

```
0 TRACK=0 SECTOR=4 BAD=0 RD/WRT=0 XFERS=0 B-DATA=0
```

**EXAMPLE 2:** Operator requests status of both drives using the "STATUS" command.

```
UN 0 BAD=0 RD/WRT=0 XFERS=0 B-DATA=0
UN 1 BAD=0 RD/WRT=0 XFERS=0 B-DATA=0
```

**EXAMPLE 3:** Disk was write protected.

```
Error detected on drive #1 at track #1, Sector #1
error code was 100
#BAD=1 #RD/WRT=2002 #XFERS=0 B-DATA=0
```

**EXAMPLE 4:** Read on drive with no disk installed.

```
Error detected on drive #0 at track #1, Sector #11
error code was 110
#BAD=3 #RD/WRT=2049 XFERS=0 B-DATA=0
```
CHAPTER 7

CUSTOMER SERVICE

NOTE

This section applies to DSD products sold within the continental USA only. International customers should contact their local distributor for service or repair.

SERVICE PROCEDURE

If any operational problems are encountered with the DSD systems, the customer should proceed as follows:

1) Use the manual and diagnostic tools supplied with the system to assemble a good description of the problem. Do not simply package the system and ship it to Data Systems Design for repair.

2) Isolate the problem to a replaceable module. Use a telephone as near to the system as possible to call Customer Service Support if advice is needed.

3) Return the failed module or modules to Data Systems Design for repair or replacement using the Material Return Procedure outlined below.

By calling DSD Customer Service Support before removing assemblies, the customer:

1) Minimizes the chances for misinterpretation of diagnostic results.

2) Establishes exchange priority.

3) Guarantees the minimum service charge (plus applicable shipping charges) to resolve his problem. Advice is absolutely free.

In many instances, the problem is merely an out-of-adjustment power supply or a loose cable connection. In these cases, if the customer uses our telephone-advisory service, the equipment is up and running again quickly.

CUSTOMER SERVICES

1) Telephone troubleshooting advice and diagnostic assistance.

2) Module exchange and repair services.

3) Technical information and operation advice.

4) Returned system repair.
APPENDIX A

Standard Jumper Positions on Interface and Controller Modules
1. MARK 2 DIGIT LOADING CODE, REV AND 4 DIGIT SERIAL NUMBER
2. APPLY ELASTIC MASK OR EQUIVALENT WHERE SHOWN
3. REMOVE PIN 23 FROM ITEM 156 26 PIN CONNECTOR
4. REMOVE PIN 34 FROM ITEM 118 50 PIN CONNECTOR
5. R53 AND R54 ARE ORIENTED WITH PIN 9 AT NOTCH MARK IN SILICON PIN IN SMD. ALL RESISTORS BY PACKS HAVE A DOT OR GROOVE ON PACKAGE TO INDICATE PIN 1
6. ADJACENT ROWS OF VERS PINS TO BE ASSEMBLED WITH MATING TRACKS BEFORE INSTALLING IN BOARD
7. HAND SOLDER OSMOSIS 55 BUS BARS AND CONNECTOR ITEM 16 AFTER WAVE SOLDER AND CLEANING
8. TRIM LEADS PLUG TO BOARD AT LOCATIONS A44, A45, AND A6 AFTER WAVE SOLDER
9. SOCKETED COMPONENTS TO BE INSTALLED AFTER WAVE SOLDER
10. VERS PINS NOT INSTALLED IN LOCATION P5
11. BEFORE ASSEMBL JUMPER ITEM 121
12. RESISTOR R52 IS USED ONLY WHEN IC 68X REPLACES IC 68Y IN LOCATION X8
13. FACTORY SELECTED PARTS
14. CAP C9 NOT USED
15. CUT JUMPER BETWEEN PINS 18 AND 19 WHERE SHOWN
16. DENOTES MINI JUMPERS # DENOTES WIRE WRAP JUMPERS

DIMENSIONS ARE IN INCHES
TOLERANCES ARE 0.005 INCHES
APPENDIX B

Disk Drive Maintenance Manual
CONTROL DATA®
FLEXIBLE DISK DRIVE
MODEL 9406-4

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS DATA
WIRE LISTS

MAGNETIC PERIPHERALS INC.
A subsidiary of
CONTROL DATA CORPORATION

HARDWARE MAINTENANCE MANUAL
<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>SHEETS AFFECTED</th>
<th>MANUAL/SECTION REVISION STATUS</th>
<th>CHANGE AUTHORITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>81 MAY 29</td>
<td>ISSUE</td>
<td>A A A A A A A A A A</td>
<td>Magdeburger</td>
</tr>
<tr>
<td>B</td>
<td>81 JUL 27</td>
<td>ii</td>
<td>A A A A B A A A A A A A</td>
<td>PL 20598</td>
</tr>
<tr>
<td>C</td>
<td>81 OCT 13</td>
<td>ii</td>
<td>A A A A C A A B A A</td>
<td>PL 20644</td>
</tr>
<tr>
<td>D</td>
<td>82 FEB 13</td>
<td>ii, vi</td>
<td>A D A D D A A B A A</td>
<td>PL 20679</td>
</tr>
</tbody>
</table>
This manual provides the information needed to install, operate and maintain the Control Data Corporation Model 9406-4 Flexible Disk Drive (FDD) and is intended to support customer engineers who require detailed information about the Flexible Disk Drive's operation.

The total content of the manual is comprised of two publications, each having a unique publication number, and is contained in one volume. The Manual's publication number, 77653520, is that of the front matter, Sections One through Seven, and Section Nine. This number should be used when making reference to the Model 9406-4 Flexible Disk Drive Hardware Maintenance Manual.

This manual applies to several configurations of the FDD. Refer to the equipment name plate located on the right hand side of the unit (as viewed from the front) to determine the appropriate Hardware Product Configurator (HPC) and Equipment number as shown in the Flexible Disk Drive Configurator Sheet, page iv.

Sections VIII Parts Data is identified by the unique Publication number 77653522.

EMI NOTICE

NOTICE: This equipment has been designed as a component to high standards of design and construction. The product, however, must depend on receiving adequate power and environment from its host equipment in order to obtain optimum operation and to comply with applicable industry and governmental regulations. Special attention must be given by the host manufacturers in the areas of safety, power distribution, grounding, shielding, audible noise control, and temperature regulation of the device to insure specified performance and compliance with all applicable regulations. This equipment is a component supplied without its final enclosure and therefore is not subject to standards imposed by FCC Rules for Electro-Magnetic Interference (EMI). Federal Docket 20780/FCC 80-148 Part 15.
**FLEXIBLE DRIVE CONFIGURATOR SHEET**

![Diagram of Flexible Drive Configurator](image)

1. **EQUIPMENT IDENTIFICATION NO. (BRXXX-X)**
2. **HARDWARE PRODUCT CONFIGURATOR (HPC) NUMBER**
3. **AC POWER REQUIRED (ON UNITS LABELED 50/60 HZ, CHECK CONFIGURATION OF SPINDLE-MOTOR PULLEY FOR FREQUENCY).**
4. **EQUIPMENT SERIES CODE STATUS NUMBER**
5. **UNIT SERIAL NUMBER**

---

**NOTES:**

1. **PARTS BREAKDOWN IDENTIFICATION** - From unit nameplate (see above representation), find HPC number. After reading instructions for use of Section 8, Illustrated Parts Catalog, of this manual, use HPC number to determine specific parts configuration for unit in question.

2. **EQUIPMENT INQUIRIES** - Equipment inquiries should reference the unit's Equipment Identification Number and Series Code, Number from unit nameplate, as represented above.
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## GENERAL DESCRIPTION

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## OPERATION

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## INSTALLATION AND CHECKOUT

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</tr>
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<td>9-2</td>
</tr>
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1.1 INTRODUCTION

The Model 9406-4 Flexible-Disk Drive (FDD) is a compact, portable, random-access, data-storage device that interfaces with a central processor via a control unit. Input/Output data and control signals are transmitted by means of an I/O cable.

1.2 PURPOSE AND USE OF EQUIPMENT

Data, in the form of magnetized bits, is written on, or read from the tracks of a rotating diskette. The FDD uses a single, flexible, removable diskette enclosed in a sealed jacket. The unit may be configured for hard-sector or soft-sector operation.

1.3 PRODUCT DESCRIPTION

The major FDD components are the spindle, disk drive motor, read/write heads, stepping motor, track-indexing devices and printed-circuit board.

The options include Data/Clock Separation and Sector Separation.

1.3.1 PHYSICAL DESCRIPTION

The physical dimensions for the equipment are as follows:

<table>
<thead>
<tr>
<th></th>
<th>9406-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>4.62 inches (117.4 mm)</td>
</tr>
<tr>
<td>Width</td>
<td>9.50 inches (241.3 mm)</td>
</tr>
<tr>
<td>Depth</td>
<td>4.25 inches (362 mm)</td>
</tr>
<tr>
<td>Weight</td>
<td>12 lbs. (5.44 kg)</td>
</tr>
</tbody>
</table>

1.3.2 ELECTRICAL DESCRIPTION

The electrical specifications for the equipment are as follows:

- DC Power Source (Supplied by Host Equipment)
  
  +24 volts (+10%) @ 0.120A Max when Deselected
  @ 0.70 A Typical when Stepping
  + 5 volts (+5%) @ 0.6 A Typical

- AC Power Source - Refer to the FDD nameplate to determine AC power requirements.
1.3.3 PERFORMANCE CHARACTERISTICS

The equipment specifications for the FDD are as follows:

- **ACCESSING TIME**
  
<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Access Time</td>
<td>248 ms</td>
</tr>
<tr>
<td>Maximum One-Track Access Time</td>
<td>23 ms</td>
</tr>
<tr>
<td>Average Access Time</td>
<td>91 ms</td>
</tr>
</tbody>
</table>

- **RECORDING**
  
<table>
<thead>
<tr>
<th>Mode</th>
<th>Density (nominal)</th>
<th>Double Frequency</th>
<th>MFM</th>
<th>Track</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Head 0</td>
<td>1836 BPI (72 BPmm)</td>
<td>3672 BPI (145 BPmm)</td>
<td>Outer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3268 BPI (129 BPmm)</td>
<td>6536 BPI (257 BPmm)</td>
<td>Inner</td>
</tr>
<tr>
<td></td>
<td>Head 1</td>
<td>1879 BPI (74 BPmm)</td>
<td>3758 BPI (148 BPmm)</td>
<td>Outer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3408 BPI (134 BPmm)</td>
<td>6816 BPI (268 BPmm)</td>
<td>Inner</td>
</tr>
</tbody>
</table>

  | Data Transfer Rate   | 249,984 bits/sec | 499,968 bits/sec    |
  | Bits/Byte           | 8                | 8                    |
  | Bits/Track          | 41,664           | 83,328               |
  | Tracks/Surface      | 77               | 77                   |
  | Sectors             | Format Determined| Format Determined    |

- **DATA CAPACITY**
  
  | Bytes/Track         | 5,208            | 10,416               |
  | Bits/Track          | 41,664           | 83,328               |
  | Bits/Surface        | 3,208,128        | 6,416,256            |
• **FLEXIBLE DISKETTE**
  (Optional)

  Diskette Dimensions

  Useable Diskette Recording Surfaces

  Diskette Surface Diameter

  Recording Radii (Nominal)

  Head 0

  Head 1

  Diskette Surface Coating

  Diskette Velocity

• **READ/WRITE HEADS**

  Heads/Unit

  Track Width

  Track Spacing

  Erase to Read/Write Gap

  CDC 421 Single-Sided, Single-Density
  CDC 423 Single-Sided, Double-Density
  CDC 425 Double-Sided, Double-Density

  8x8 inches (203.2 x 203.2 mm)
  (including jacket)

  2

  7.88 in. (200.1 mm)

  Track 76 2.0290 in. (51.5 mm) Inner
  Track 00 3.6123 in. (91.8 mm) Outer
  Track 76 1.9457 in. (49.4 mm) Inner
  Track 00 3.5290 in. (89.6 mm) Outer

  Magnetic Oxide

  360 r/min

  2

  0.013 in. (0.33 mm)

  0.02083 in. (0.529 mm)

  0.036 in. (0.914 mm)
2.1 INTRODUCTION
The FDD is under direct control of the input/output and power sources. No special start-up procedure is required. Operation is fully automatic and requires no operator intervention during normal operation.

2.2 OPERATING INSTRUCTIONS
Verify that power and I/O cables are securely attached before operation.

2.2.1 FLEXIBLE DISKETTE LOADING
a. Apply AC/DC power to unit.
b. Open FDD door.
c. Remove diskette from storage envelope as shown in Figure 2-1.
d. Be sure the Write-Protect slot in the jacket is open, as shown in Figure 2-1, if the diskette is to be write-protected.
e. If a diskette with a Write-Protect slot is not utilizing the Write Protect, that is, it will be written on, the slot must be covered with a piece of tape which is opaque to infrared.
f. Carefully slide diskette into FDD, as shown in Figure 2-1, until jacket is solidly against stops and sets the ejector mechanism.
g. Carefully close unit door. Ensure that jacket is properly seated, spindle has engaged diskette, and door is closed and latched.
h. Protect the empty envelope from liquids, dust, and metallic materials.

2.2.2 FLEXIBLE DISKETTE REMOVAL
a. Open FDD door to stop diskette rotation and disengage spindle.
b. Remove diskette from FDD and put it in its storage envelope.
c. Close FDD door.

2.3 ERROR RECOVERY
The following paragraphs give information needed to recover from possible errors in equipment operation.

2.3.1 SEEK ERROR
Seek errors will rarely occur unless the stepping rate is exceeded. In the event of a seek error, recalibration of track location can be achieved by repetitive Step Out commands until a Track 00 signal is received.

2.3.2 WRITE ERROR
To guard against degradation from imperfections in the media, no more than four attempts to write a record should be used when read after write errors are encountered. In the event a record cannot be successfully written within four attempts, it is recommended that the sector or track be labeled defective and an alternate sector or track assigned. If more than two defective tracks are encountered, it is recommended that the diskette be replaced.
2.3.3 READ ERROR

In the event of a Read error, up to five attempts should be made to recover with re-reads. If after five attempts the data has not been recovered, retract the head to Track 00, reseek to the data track and attempt five additional rereads. Unloading the head when data transfers are not imminent will increase the data reliability and extend the diskette life.

2.4 DISKETTE HANDLING RECOMMENDATIONS

Since the recorded diskette contains vital information, reasonable care should be exercised in its handling. Longer diskette life and trouble free operation will result if the following recommendations are followed.

a. Do not use a writing device which deposits flakes e.g., lead or grease pencils, when writing on diskette jacket label.
b. Do not fasten paper clips to diskette jacket edges.
c. Do not touch diskette surface exposed by jacket slot.
d. Do not clean diskette in any manner.
e. Keep diskette away from magnetic fields and from ferromagnetic materials that may be magnetized.
f. Return diskette to envelope when removed from FDD.
g. Protect diskette from liquids, dust, and metallic substances at all times.
h. Do not exceed the following storage environmental conditions:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>50°F to 125°F (10°C to 56.1°C)</td>
</tr>
<tr>
<td>Relative Humidity</td>
<td>8% to 80%</td>
</tr>
<tr>
<td>Maximum Wet Bulb</td>
<td>85°F (29.4°C)</td>
</tr>
</tbody>
</table>

i. Diskettes should be stored in a box or cabinet when not in use.
j. Remove diskette before applying or removing power to the FDD.
3.1 INTRODUCTION

This section provides the information and procedures necessary to put an FDD into operation.

3.2 UNPACKING

Unpack FDD as follows:

a. Cut banding and lift top half of styrofoam shell from unit.

b. Lift unit in polyethylene bag from bottom half of styrofoam shell and remove unit from polyethylene bag.

During unpacking, care must be used so that any tools being used do not inflict damage to the unit. As a unit is unpacked, inspect it for possible shipping damage. All claims for this type of damage should be filed promptly with the carrier involved. If a claim is filed for damages, save the original packing materials.

3.3 INSTALLATION

Install the FDD in the designated location in the host equipment. Remove blank head protective diskette from unit.

3.4 CABLING AND CONNECTIONS

Connect the AC cable, I/O cable, and DC cable if applicable between the FDD and host equipment. Adequate circuit protective devices must be provided by the host equipment to meet applicable safety standards.

3.4.1 INPUT-OUTPUT CABLE

The maximum cable length from connector to connector is 25 feet (7.62 m). The characteristic impedance should be 150 ohms.

The information relative to the I/O connector (J1) and pin/signal assignments are defined in Figures 5-1, 5-3 and 5-4.

The terminating resistor pack RM5 (see Figure 5-4) is to be installed in the end FDD (farthest from the controller) ONLY. Terminators in more than one FDD may result in damage to the controller.

3.4.2 DC POWER CONNECTION

The mating connector cable should consist of 18 AWG minimum. Refer to Figure 3-2 for connector part numbers.
3.4.3 AC POWER CONNECTION

The mating connector cable should consist of stranded wire, 18 AWG minimum with center-pin connection utilized as frame ground. Refer to Figure 3-1 connector part numbers and attachment.

3.5 ENVIRONMENT

Operating and storage environments of the FDD are as follows:

| Operating: | 40° to 115°F (4.4° to 46.1°C) 12°F (6.6°C)/hr. max. fluctuation 20% to 80% relative humidity (providing there is no condensation) |
| Non-Operating: | -30° to +150°F (-35° to 65°C) 5% to 95% relative humidity (providing there is no condensation) Max. Wet Bulb 80°F (27°C) |

3.6 INITIAL CHECKOUT

This procedure should be used to determine that the FDD is operational. The procedure assumes that the unit is installed and the I/O and power cables are connected.

a. Ensure that the shipping insert has been removed before applying power.
b. Apply AC power to unit and visually check that the spindle rotates.
c. Apply DC power to unit.
d. Insert diskette as described in Section 2.
e. Apply a head-load-command signal to the unit and close the access door. Check that the head-load solenoid actuates, and the door-closed switch is actuated.
f. Apply a stepping-command signal to the unit and check that the actuator steps the head as commanded.
g. Remove diskette.
h. Remove the command signals and power from the unit.
3.6.1 OPERATION FREQUENCY

If the required operating frequency is different than that which the unit is configured, a procedure for converting operating frequencies using the dual-diameter reversible pulley is provided in Section 6, "Frequency Conversion".

![Diagram of cable connector and recepticle on FDD assembly]

**FIGURE 3-1. AC CABLE ASSEMBLY**

<table>
<thead>
<tr>
<th>PIN 8</th>
<th>USE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+24</td>
</tr>
<tr>
<td>2</td>
<td>+24 Return</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
</tr>
<tr>
<td>5</td>
<td>+5</td>
</tr>
<tr>
<td>6</td>
<td>+5 Return</td>
</tr>
</tbody>
</table>

Mating Connector Amp 1-480270-0
Pins Amp 60619-1

**FIGURE 3-2. DC CONNECTOR**
4.1 INTRODUCTION

The basic functions performed by the FDD are: (1) receive and generate control signals, (2) position the Read/Write heads on selected tracks, and (3) write or read data upon command from the FDD controller. These functions are accomplished upon selection after initial indication to the controller that the FDD is ready to operate and accept commands.

The theory of operation for the FDD is divided into two parts. The first part gives a general theory of operation. The second part gives a detailed functional description of all major components, both electronic and mechanical, and describes all signals exchanged between the FDD and the controller.

Sections 4 and 5, Theory of Operations and Diagrams, respectively, which follow, detail operation of both hard-sector/data-separation configurations, and soft-sector/composite-read-data configuration(s).

Separate PWA's and schematics for both sets of configurations are contained in Section 5.

4.2 GENERAL DESCRIPTION

The basic function of the FDD is to indicate to the controller when it is ready to operate, and respond to the commands of the controller to: (1) receive and generate control signals; (2) position the Read/Write heads to selected tracks; and (3) write or read data on the diskette when selected. All of the functions described which are options are switch selectable.

Signals received and transmitted by the FDD are shown in Figure 4–1. Some signals received by the FDD are gated with Drive Select so that no stepping, reading or writing can be performed on an unselected FDD. Also, some signals generated within the FDD are gated with Drive Select so that they can not be transmitted from an unselected FDD.

During the write operation, the selected FDD must have heads loaded, Head Select, Write Enable and Write Data signals. The Write Enable line remaining high implies a read operation. Under these conditions, the FDD will transmit -Read Data signals to the controller. Some models of the FDD which contain a data separator will also transmit -Sep Clock and -Sep Data signals to the Controller.

Controller Step and Direction commands are received initiating a track seek operation on a selected FDD.

Positioning the carriage-mounted Read/Write heads is accomplished by a band-driven stepper motor. Each step command from the user system increments the stepper motor which, in turn, moves the band. The band increments the Read/Write heads one track position for each step command. The selected FDD transmits a Track 00 signal to the controller whenever the Read/Write heads are at Track 00.
FIGURE 4-1. FUNCTIONAL BLOCK DIAGRAM
A reading or writing operation begins by placing the Read/Write heads in contact with the diskette with a Head-Load command and at the desired track. To write on the diskette, Write Enable is set by the controller to condition the write logic. The write current then in the head, reverses polarity synchronous with the high-to-low transitions of the Write-Data pulses from the controller. The current reversals cause magnetic flux reversals on the desired diskette track. Erasure of previously recorded data is simultaneously accomplished during the writing operation in addition to a delayed-tunnel-erase which ensures disk inter-changeability.

To read from the diskette, magnetized bits in the format of the pre-recorded data are sensed by the Read/Write heads. This signal is amplified, digitized and transmitted to the user system.

4.3 FUNCTIONAL DESCRIPTION

Refer to Figures 4-1, 5-2, and the Schematic Diagram (Section 5) for the following discussion.

The FDD is divided into the following major functional areas:

a. Control Logic  
b. Write Logic  
c. Stepper Control  
d. Read Logic  
e. Diskette Drive  
f. Read/Write Head  
g. Index  
h. Door Lock  
i. Drive Select

4.3.1 CONTROL LOGIC

The functions of the control logic are to generate the signals that: (a) establish the ready status of the FDD; (b) step the Read/Write heads in or out upon selection and command of the controller; (c) load the heads on the diskette for read/write operations; (d) protect the diskette from writing if the write-protect slot is present; (e) indicate when the Read/Write head is at Track 00; (f) generate the Index and Sector pulses when the diskette is rotating and the FDD is selected; (g) lock the FDD door latch; (h) unit selection of the FDD; (i) select head 0 or 1 for Read/Write operation; (j) indicate that the door has been open while the drive was not selected; (k) indicate single or two-sided diskette; (l) indicate visually that the drive has one or more functions performed by the Activity LED.

a. Drive Ready

This line is used to indicate to the FDD controller that the diskette is inserted correctly, the door is closed, and that two index pulses have been detected. This line is not inhibited by the select line within the drive. This line can be inhibited by Drive Sel at the ready output. Switches R, RR and DR may apply.

If a single-sided diskette is installed when switch DR is closed, READY will be active (logical zero) if head 0 is selected, but false (logical 1) if head 0 is selected. Conversely, if a two-sided diskette is installed, READY will be active when either side of the diskette is selected.

When switch DR is open and a single-sided diskette is inserted, head 0 or head 1 may be selected and READY will not be inhibited.
(1) **Radial Ready**

This option enables the user to monitor the Ready line of each drive on the interface. This can be useful in detecting when an operator has removed or installed a diskette in any drive. Normally, the Ready line from a drive is only available to the interface when it is selected.

Switch RR must be open on each FDD used on the interface when this option is used. Switch R may be closed on only one FDD on the interface: this FDD will have Ready on output pin 22. The remaining FDDs in the interface must utilize their own Ready lines, each using a different alternate I/O line. These outputs may be wire-wrapped or soldered to the appropriate staked pins with 30-gauge wire. (see Figure 5-4).

b. **Power on Reset**

At initial voltage application, comparator U18 generates a reset pulse of approximately 70 ms in length. This prevents the drive from writing during power on and resets the Index, In Use, Disk Change and Stepper Motor Logic.

c. **Step and Direction**

Each step command received causes the Read/Write heads to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero-to-one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be at least 1 µs before the trailing edge of the step pulse. Refer to Figure 5-2 for these timings.

Step pulses are inhibited during a write operation and movement which would position the Read/Write heads behind Track 0.

d. **Head Load and Door Closed**

The Read/Write heads of a selected FDD can be loaded only when the disk is fully installed and the front-panel door is closed.

When the controller sends a Head-Load signal, the head-load solenoid is energized causing the load plate to actuate. The actuation of the load plate permits the head arms to load the heads against the diskette surface. The door-closed switch also is used to inhibit the READY signal when the door is opened.

(There are several different options when configuring head load (see Figure 5-3, sheet 1). Shunts C DD, A, D, X and B may apply).

e. **Write Protect**

The Write-Protect function is accomplished through use of an LED (light-emitting diode) and a photo-transistor. These are mounted such that the presence of a Write Protect slot in the jacket of the diskette will cause pin 5 of U24 to be driven low. This signal is gated with Drive Select and Write Enable to inhibit writing on any diskette possessing a write-protect slot. Closing switch WP enables write inhibit. **CAUTION.** If switch WP is off, the drive can write on a protected diskette.

f. **Track Zero**

Track 00 signal is generated when the carriage-assembly tab is sensed by the Track 00 optical switch. Closing this switch causes U12 Pin 5 to switch high assisted by hysteresis. The output is gated with ØAC and Drive Select to provide the Track 00 signal that is transmitted to the controller from U10 pin 11.
g. Index, Sector and Diskette-Type Circuitry

The beginning of each diskette track is indicated by an Index pulse. The diskette rotates between a light source (LED) and a sensor (photo transistor). When the Index hole in the diskette passes under the light source, light is detected by the sensor. The sensor output is amplified and transmitted to the controller as the Index pulse when the FDD is selected. The drive has two Index detectors, one for two-sided diskettes and one for single-sided diskettes. U16 determines the type of diskette involved. This signal is gated with Drive Select and sent to the interface by U25 pin 3 through switch 2S.

Two-sided and single-sided Index is gated at U11 pins 12 and 13 and is provided to U19 pin 12 for shaping.

An Index/Sector separator is provided on some models of the FDD. Proper operation of the Ready function requires that the Index pulses be separated in the FDD.

Whenever a 32-hole hard-sectored diskette is used, Index/Sector pulses arrive at 5.2 -ms intervals with one Index pulse nested between two sector pulses at 2.6 ms nominally. When using the hard-sector functions, Index and Sector pulse-output widths are $0.4 \pm 0.2$ ms when switch E is closed.

When using the soft-sector function, the Index output-pulse width if $1.8 \pm 0.4$ us. Switches SS, HS, RI, S and I may be applicable (see Figure 5-3, sheet 3).

h. Door Lock and In Use

The Door Lock circuit can be latched on under Drive Select control so that the door can remain locked without maintaining the active state of In Use. To implement this option, close switches D and DL. Then, if the appropriate Drive Select line is activated while In Use is active U28-9 will be set, which holds the door-lock circuit active. To unlock the door, Drive Select is activated again while In Use is inactive. This will reset U28-9.

The Door Lock may also be optioned such that it is only active while the In Use line is active. Switch D is closed; Switch DL is open.

i. Drive Select

The Drive Select function will inhibit command and status signals such as Index, Sector, Head Load, Write Data and Ready unless optioned otherwise. The position of the FDD in a daisy-chain configuration is determined by the activation of Switch 4. Switches DD and A apply. (see Figure 5-3, sheet 1).

4.3.2 WRITE LOGIC

A write operation begins with a Write Enable command from the controller when the FDD is selected. This command simultaneously enables the Write-Data switching drivers (flip flop U28 pins 5 and 6), the Write-Data gate U22 pin 6, blocks the input to the read circuit by reverse-biasing diodes in U3, and after a delay energizes the erase windings. Data applied to the Write-Data input alternately switches a constant write current through the write drivers to the head windings. Low-current operation used when writing on physical track 43 and greater, is selected by switching a shunt resistor R59 into the write-current source. Current source U13 provides current to the emitters of the write transistors U30. Switch LC applies.
4.3.3 HEAD-SELECT LOGIC

Head-Select signal when low selects head 1 by turning on U9 pin 7 causing its collector to be at +12 volts while U9 pin 1 is at ground. When the Head-Select signal goes high, it will cause U9 pin 7 to ground and U9 pin 1 to +12 volts selecting head 0.

In systems containing no more than two drives per controller, each Read/Write head can be assigned a separate drive address. In such cases, the four Drive Select lines can be used to select the four Read/Write heads. To implement this option, close switch S3 and properly set switch S5. For example, the first drive may have switch 4-1 and switch 5-3 closed while the second drive has switch 4-3 and switch 5-1 closed. With this jumper configuration installation, the four Drive Select lines have the following selection functions:

1. Drive Select 1 selects head 0 of first drive;
2. Drive Select 2 selects head 1 of first drive;
3. Drive Select 3 selects head 0 of second drive;
4. Drive Select 4 selects head 1 of second drive.

U13 and U9 pin 8 control the +12 voltage with respect to loss of +5 control voltage. Switch S2 is closed for this option. Head selection may be performed by the direction line if optioned by closing switch S1. When direction is low, head 1 is selected. When direction is high head 0 is selected.

(Refer to Figure 5-3, schematic sheets 2 and 3.)

4.3.4 DISK CHANGE

This customer-selectable option is enabled by closing switch DC. It will provide a true signal (logical zero) to the interface (pin 12) when Drive Select is activated, if while deselected the drive has gone from a Ready to a Not Ready (door open) condition. This line is a reset on the true to false transion of Drive Select if the drive has gone Ready. Timing of this line is illustrated in Figure 5-2. The circuitry is illustrated in Figure 5-3, schematic sheet 4. The output of flip-flop U7 pin 6, goes high when the door is opened, but output gate U10-6 is not enabled until the drive is selected. When the Drive Select line goes false, U7 pin 6 will be clocked high.

4.3.5 READ LOGIC

Read operation is enabled when the Read/Write heads are loaded on the diskette and Write Enable is not commanded. With Write Enable not commanded, the data blocking diodes U3 are forward-biased and data sensed by the Read/Write head is fed to the Read Data circuit. The read signal from the diskette is in the form of a sine wave.

This analog signal is amplified by U1, filtered, differentiated by C6/R11 and C7/R12 amplified by U2, and coupled to a comparator/logic circuit to detect zero crossings and reject noise in the differentiated read signal.

The out-of-phase comparators U5 pins 7 and 12 have rise and fall times whose differences are exaggerated by slow-down capacitor C27. This results in a narrow negative pulse at U11 pin 6 which triggers a one-microsecond retriggerable one-shot U15 pin 9.
Flip flop U7 pins 8 and 9 perform a noise-rejection function in that noise near the
zero crossings of the amplified differentiated data only result in retriggering U15
pin 9. This appears as jitter in the clock for the flip flop whose data input, derived
from redundant comparator U8 pin 12, has by that time stabilized.

Another slow-down capacitor, C32 causes a negative pulse to appear at the output
of U11 pin 8 whenever the flip flop toggles. Although shifted in time by approximately
the delay of one-shot U15 pin 9, each pulse corresponds to a zero crossing of the
differentiated signal, and a peak of the analog read signal. Jitter at the flip-flop
clock input and U9 pin 8, which is due to noise at the zero crossings, will not affect
the 200-ns composite-data pulse width (see Figure 5-3, schematic sheet 4).

4.3.6 DISKETTE DRIVE

Diskette drive is accomplished by clamping the diskette between the cone assembly
and belt-driven spindle. The spindle is rotated at 360 r/min by the diskette drive
motor. A dual pulley permits 50- or 60-Hz operation without a motor change.

4.3.7 READ/WRITE HEADS

The Read/Write heads are in direct contact with the diskette during read or write
operation. Head load is achieved by a solenoid-actuated load plate allowing the
head arms to load the Read/Write heads against the diskette. The head surfaces are
designed for maximum signal transfer to and from the magnetic surface of the diskette
with minimum head/disk wear. The tunnel-erase gap DC-erases the intra-track
area to improve off-track signal-to-noise ratio and permit diskette interchange between
drives.

4.4 CONTROL AND DATA LINE CHARACTERISTICS

All signal lines must be terminated at the receiver with a characteristic impedance
of 150-ohms, typically. Transmission is by 26 AWG (min.), 150-ohm flat cable
or twisted pair (one twist per inch) with a maximum line length of 25 feet. Figure
5-1 shows the timing of typical operations.

4.4.1 LOGIC LEVELS

The following definitions will be used throughout this manual:

low = Logic 1, Active State                   Refers to the low-voltage condition
                  +0.4 VDC Max.

high = Logic 0, Inactive State               Refers to the high-voltage condition
                  +2.4 VDC Min.

4.4.2 TRANSMITTER CHARACTERISTICS

The FDD uses the TTL 7438 (quad 2-input buffer or driver) or equivalent to transmit
all control and data signals. This transmitter is capable of sinking a current of 48
ma with an output voltage of 0.4 volts. The host controller must provide the necessary
pull-up resistor.

4.4.3 LINE-RECEIVER CHARACTERISTICS

The FDD uses SN7414 gates or equivalent for line receivers. The input of each
receiver is terminated in 150 ohms.

4.4.4 CONTROL AND DATA LINE FUNCTIONS

The signals that are exchanged are described in Table 4-2 and are shown relative to a point of origin in Figure 4-1.

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-STEP</td>
<td>A 1- microsecond (minimum) logic 1 level pulse on this line causes the head to move one track as determined by the direction line.</td>
</tr>
<tr>
<td>-DIRECTION</td>
<td>A logic 1 level on this line and step pulse causes the head to move one track inward toward the center of the diskette. A logic 0 level on this line and step pulse causes the head to move one track outward from the center of the diskette. (Refer to paragraph 4.3.3, Head-Select Logic for further usage of the line).</td>
</tr>
<tr>
<td>-HEAD LOAD (Alternate I/O)*</td>
<td>A logic 1 level on this line loads the heads against the diskette.</td>
</tr>
<tr>
<td>-WRITE ENABLE</td>
<td>To enable the FDD write driver, this line is held at a logic 1.</td>
</tr>
<tr>
<td></td>
<td>To disable the FDD write driver and enable the FDD read circuitry, this line is held at logic zero.</td>
</tr>
<tr>
<td>-WRITE DATA</td>
<td>This line contains the composite coded write clock and data information to the FDD.</td>
</tr>
<tr>
<td>-LOW CURRENT (Alternate I/O)*</td>
<td>This line reduces write current for physical tracks 43 or greater. A logic 1 level reduces write current. If the FDD includes the Track 43 kit this line will not be applicable.</td>
</tr>
<tr>
<td>-DRIVE SELECT (1 of 4 lines)</td>
<td>A logic 1 level on this line with switches DD, A, and one set of switch 1 contacts closed enables the FDD interface. (Refer to paragraph 4.3.3a, Head Selection, for further usage of these lines.)</td>
</tr>
<tr>
<td>-IN USE (Alternate I/O)*</td>
<td>A logic 1 level on this line illuminates an LED indicator on the front panel of the FDD and activates a solenoid which locks the door-latch mechanism preventing opening of the door.</td>
</tr>
<tr>
<td>-HEAD SELECT</td>
<td>A logic 1 level on this line selects head 0 (lower diskette surface). A logic 0 selects head 1.</td>
</tr>
</tbody>
</table>

*Alternate I/O Unassigned - Unused I/O pins 4, 6 and 8. These may be customer defined.
**SIGNAL**

**FUNCTION**

**OUTPUT LINES**

- **READY**
  A logic 1 level indicates that the door is closed, a diskette is rotating, and two Index pulses have been sensed. This output may be optioned to use an alternate I/O pin.

- **INDEX**
  This line gives an indication of the rotational position of the diskette by outputting a logic 1 pulse for every Index hole of the diskette. This output may be configured to use an alternate I/O pin if desired.

- **DISK CHANGE**
  (Alternate I/O)*
  This line gives indication that there was a loss of Ready from the Door Closed signal going false while the drive was not selected. The status of this output can only be monitored when the drive is selected.

- **TRACK 00**
  A logic 1 level indicates that the head is positioned over Track 00.

- **WRITE PROTECT**
  Logic 1 level indicates that the write-protect slot on the diskette is uncovered.

- **READ DATA**
  This line contains the unseparated data and clock information.

- **TWO-SIDED**
  (Alternate I/O)*
  A logic 1 indicates a two-sided diskette and a logic 0 a single-sided diskette.

Some models of the FDD contain Data/Clock and Index/Sector separators. For these models the following output lines are functional:

- **SEPARATED DATA**
  This line contains the separated data information.

- **SEPARATED CLOCK**
  This line contains the separated clock information.

- **SECTOR**
  This line gives an indication of the rotational position of the diskette by outputting a logic 1 pulse for every sector hole of the diskette. (For soft-sector configurations this line is inactive.) This output may be configured to use an alternate I/O pin.

*Alternate I/O Unassigned — Unused I/O pins 4, 6, and 8. These may be customer defined.

**The signals are valid when double-frequency recording without missing clock is used, and switch FS is closed. The signals are valid when double-frequency recording with missing clock is used and switch TS is closed.
4.5 CUSTOMER-SELECTABLE FEATURES

This section details the numerous customer-selectable features available. Standard and optional PWA configurations are presented in the following paragraphs and in Table 4-2.

Part numbers for switches are included below.

<table>
<thead>
<tr>
<th>SWITCH</th>
<th>CDC PART NUMBER</th>
<th>AMP PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 (10-position)</td>
<td>83462207</td>
<td></td>
</tr>
<tr>
<td>S2 (8-position)</td>
<td>83452205</td>
<td></td>
</tr>
<tr>
<td>S3 (8-position)</td>
<td>83452205</td>
<td></td>
</tr>
<tr>
<td>S4 (4-position)</td>
<td>83452201</td>
<td></td>
</tr>
<tr>
<td>S5 (4-position)</td>
<td>83452201</td>
<td></td>
</tr>
</tbody>
</table>

As shipped from the factory, the PWA's are configured as detailed in Table 4-2.

The following is an alphabetical listing of each feature and its description.

A allows gating of Drive Select with the Head-Load signal to create drive selection.

B allows interactive gating of Drive Select and Head-Load. Without this feature there can be no interaction (gating) at the interface between these two signals.

C brings the Head-Load signal from J1-18 to the Head-Load control logic. CC must be used with C. Also, CC must be off when C is off.

CC brings the Head-Load signal from J1-18 to the Head-Load control logic. CC must be used with C. Also, CC must be off when C is off.

D incorporates the In-Use input control signal on the interface (signal supplied by user's controller). Control of the door-lock solenoid, activity light and Head-Load solenoid can be affected by use of this feature.

DC brings the interface the following information. Ready condition on the drive became inactive (false) either while the drive was selected or deselected. Drive Select must be strobed (toggled) to reset a diskette change "true" condition. It is assumed that the loss of Ready is due to the door on the drive being opened, thereby alerting the system operator to a possible diskette change in the drive.

DD brings the Drive Select input into gating with control logic. Without this feature, all of the Drive Select inputs will be isolated from the FDD logic.

DL allows the low-to-high transition of unit selection to act as a trigger for a D flip-flop. This output status of the flip-flop depends upon the logic status of the In-Use input line which controls the door-lock solenoid, activity LED and Head-Load solenoid to activation with drive deselection and reselection. This is dependent upon the status of the In-Use 1/O line at the time of Drive Select (or reselect) with feature IU enabled.
DR The Ready output from the drive will go false if a single-sided diskette is installed in the drive and head #1 is selected. This feature prevents using the wrong side of a single-sided diskette in a double-sided drive.

E reduces the pulse width of index/and/or sector pulses from 1.8 to 0.4 milliseconds. This feature is not present on all PWA configurations; it is only available with the Sector/Index feature.

FS provides Separated Data and Separated Clock if a "missing clock" format is not being utilized with the FM only recording. This feature is not present on all PWA configurations; it is only available with the Sector/Index feature.

HO allows control of the Head-Load solenoid via the Head-Load or Drive Select inputs on the interface.

HS with a soft-sector diskette installed, produces no Index pulses on the interface so no Ready signal will be generated; however it does produce one sector pulse on the sector output. With a 32-hole hard-sector diskette installed, produces separated sector/index at the interface at the designated locations with a 1.8-millisecond pulse width (true) on the sector and index outputs. If feature E is enabled along with HS, produces separated sector/index at the interface with a 0.4-millisecond pulse width (true) on the sector and index outputs. In most hard-sector applications, both features E and HS are installed. This feature is not present on all PWA configurations.

I brings the Index signal to the drive interface at J1-20.

IU allows control of the Head-Load solenoid via the In-Use signal on the interface after Drive Select strobing to "latch" activation. Feature DL must be applied for this latching of Head-Load solenoid will not deactivate.

MM (multi-media) optimizes inner track write current for high resolution media.

R brings Drive Ready to the interface at J1-22.

RI gates Drive Select with Index and Sector. The Index and Sector status will be at the interface only while the drive is selected. (Sector is required at the interface only if hard-sector formatting is being utilized.)

RR gates Drive Select with Ready. The Ready status will be at the interface only while the drive is selected.

S brings hard sector pulses to the interface at J1-24 if hard-sector formatting is being utilized.) This feature is not present on all PWA configurations.

SS brings Index to the interface if a soft-sector diskette is installed. If a hard-sector diskette (32-hole) is installed, Index/Sector composite will be on the Index output line and Separated Sector will be on the Sector line if feature S is also implemented. Feature SS is not present on all PWA configurations.

SI allows control of head selection by the Direction line input signal after having accessed the desired track (conditional).
S2 allows control of head selection by the Head Select input via the interface at J1-14.

S3 allows control of head selection by a Drive Select input line. This is a conditional configuration. Only two drives can be addressed on a four-drive daisy-chain system. The standard DIP switch configuration is as follows:

<table>
<thead>
<tr>
<th>DRIVE</th>
<th>HEAD 0</th>
<th>HEAD 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>S4-3 closed. Drive select by J1-30.</td>
<td>S5-1 closed. Drive select by J1-32.</td>
</tr>
</tbody>
</table>

TS provides Separated Data and Separated Clock outputs at the interface in the FM recording mode only (single density). The data separator will not lose sync when the IBM missing clock format is being utilized (not to be confused with MFM recording) as with Feature FS. Feature TS is not present on all PWA configurations.

WP inhibits writing internally in the drive when a write protected diskette has been inserted in the drive. (I/O is notified.) Allows write if protected when off.

x allows gating of the Head-Load signal with Drive Select to "create" the Head-Load signal.

y allows control of the activity light by the Head-Load signal if In-Use is not being utilized.

z allows control of the activity light by the Drive Select signal if In-Use is not being utilized.

2S brings the status of the diskette in the drive to the interface at J1-10. This signal status indicates that either a single- or double-sided diskette is in the drive after two index holes have been sensed.

LC allows interface pin 2 to switch the FDD write current to a lower level for improved read margins on physical tracks 43 through 77.
TABLE 4-2. CUSTOMER SELECTABLE FEATURES

<table>
<thead>
<tr>
<th>SWITCH</th>
<th>STANDARD PWA CONFIGURATION</th>
<th>OPTIONAL PWA CONFIGURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Radial Head Load X</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>Radial Head Load X</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>Alternate Input-Head Load</td>
<td></td>
</tr>
<tr>
<td>CC</td>
<td>Alternate Input-Head Load</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>Alternate Input-In-Use</td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td>Disk Change</td>
<td></td>
</tr>
<tr>
<td>DD</td>
<td>Standard Drive Select Enable X</td>
<td></td>
</tr>
<tr>
<td>DL</td>
<td>Door Lock Latch</td>
<td></td>
</tr>
<tr>
<td>DR</td>
<td>Double Side Ready</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>0.4 ms Index Pulse</td>
<td>N/A</td>
</tr>
<tr>
<td>FS</td>
<td>False Separation</td>
<td>N/A</td>
</tr>
<tr>
<td>HO</td>
<td>Allow Head Load</td>
<td>X</td>
</tr>
<tr>
<td>HS</td>
<td>Hard Sector Enable</td>
<td>N/A</td>
</tr>
<tr>
<td>I</td>
<td>Index Output</td>
<td>X</td>
</tr>
<tr>
<td>IU</td>
<td>Head Load With In-Use</td>
<td></td>
</tr>
<tr>
<td>MM</td>
<td>Reduced Write Current</td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>Ready Output</td>
<td>X</td>
</tr>
<tr>
<td>RI</td>
<td>Radial Index and Sector</td>
<td>X</td>
</tr>
<tr>
<td>RR</td>
<td>Radial Ready</td>
<td>X</td>
</tr>
<tr>
<td>S</td>
<td>Sector Output</td>
<td>N/A</td>
</tr>
<tr>
<td>SS</td>
<td>Soft Sector Enable</td>
<td>N/A</td>
</tr>
<tr>
<td>S1</td>
<td>Side Select Using Direction Select</td>
<td></td>
</tr>
<tr>
<td>S2</td>
<td>Standard Side Select Input</td>
<td>X</td>
</tr>
<tr>
<td>S3</td>
<td>Side Select Using Drive Select</td>
<td></td>
</tr>
<tr>
<td>TS</td>
<td>True Separation</td>
<td>N/A</td>
</tr>
<tr>
<td>WP</td>
<td>Inhibit Write When Write Protected X</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>Radial Head Load</td>
<td>X</td>
</tr>
<tr>
<td>Y</td>
<td>In Use From Head Load</td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>In Use From Drive Select</td>
<td>X</td>
</tr>
<tr>
<td>2S</td>
<td>Two-Sided Status Output</td>
<td></td>
</tr>
<tr>
<td>LC</td>
<td>Low Current</td>
<td>X</td>
</tr>
</tbody>
</table>

N/A = Not available on Standard PWA
4.6 ALTERNATE I/O
The Model 9406-4 Flexible Disk Drive can be modified by the user to function differently than the standard method described in paragraph 4.6 and listed in Table 4-2. This paragraph will describe how to achieve alternate functions.

4.6.1 RADIAL READY
This alternate function enables the user to monitor the ready line of the interface of each drive in a radial configuration. The normal function of the drive is to make the ready line available on the interface only when the drive has been selected. When 2, 3, or 4 drives are connected in a radial configuration, the "Radial Ready" function will be available when the drives are modified as follows:

Drive 1
No modifications are required if the user is satisfied with the Radial Ready signal on pin 22 of J1.

Drive 2
1. Open RR (Open SW1-5).
2. Open R (Open SW1-7).
3. With a wire wrap jumper, connect alternate I/O Pin 10 (Figure 4-3) to I/O pin #1. The ready line will now be on pin 12 of J1. Pin 10 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

Drive 3
1. Open RR (Open SW1-5).
2. Open R (Open SW1-7).
3. With a wire wrap jumper, connect alternate I/O Pin 10 (Figure 4-3) to I/O pin #2. The ready line will now be on pin 10 of J1. Pin 10 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

Drive 4
1. Open RR (Open SW1-5).
2. Open R (Open SW1-7).
3. With a wire wrap jumper, connect alternate I/O pin 10 (Figure 4-3) to I/O pin #3. The ready line will now be on pin 8 of J1. Pin 10 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

4.6.2 RADIAL INDEX
This alternative function enables the user to monitor the index line of each drive so that the drive can be selected just prior to the index. When 2, 3, or 4 drives are connected in a radial configuration, the index signal will be available at the interface when the drives are modified as follows:

Drive 1
No modifications are required if the user is satisfied with the Radial Index signal on pin 20 of J1.

Drive 2
1. Open RI (Open SW1-8).
2. Open I (Open SW1-6).
3. With a wire wrap jumper, connect alternate I/O pin 9 (Figure 4-3) to I/O pin #1. The index signal will now be on pin 12 of J1. Pin 9 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.
Drive 3
1. Open RI (Open SW1-8).
2. Open I (Open SW1-6).
3. With a wire wrap jumper, connect alternate I/O pin 9 (Figure 4-3) to I/O pin #2. The index signal will now be on pin 10 of J1. Pin 9 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

Drive 4
1. Open RI (Open SW1-8).
2. Open I (Open SW1-6).
3. With a wire wrap jumper, connect alternate I/O pin 9 (Figure 4-3) to I/O pin #3. The index signal will now be on pin 8 of J1. Pin 9 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

4.6.3 RADIAL HEAD LOAD
This alternative function enables the user to load the heads without a unit select signal (i.e., the heads can be loaded without the drive being selected). When 2, 3, or 4 drives are connected in a radial configuration, the heads of any drive can be loaded when desired by modifying the drives as follows:

Drive 1
No modifications are required if the user is satisfied with the Radial Head Load Command on pin 18 of J1.

Drive 2
1. Open C (Open SW2-8).
2. With a wire wrap jumper, connect alternate I/O pin 6 (Figure 4-3) to I/O pin #1. The head load command will be applied on pin 12 of J1. Pin 6 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

Drive 3
1. Open C (Open SW2-8).
2. With a wire wrap jumper, connect alternate I/O pin 6 (Figure 4-3) to I/O pin #2. The head load command will be applied on pin 10 of J1. Pin 6 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.

Drive 4
1. Open C (Open SW2-8).
2. With a wire wrap jumper, connect alternate I/O pin 6 (Figure 4-3) to I/O pin #3. The head load command will be applied on pin 8 of J1. Pin 6 can be jumpered to any unused 1 through 5 alternate I/O pin if the user desires.
5.1 INTRODUCTION

This section contains the printed-circuit-board documentation and related timing diagrams.

Figure 5.1 shows interface connections of all AC, DC and I/O lines applicable to the FDD.

Figure 5-2 shows timing diagrams which illustrate signal/time relationships during read, write, step-in and step-out operations. Figure 5-3 is the printed-circuit board schematic and Figure 5-4 contains the assembly drawing.

* Reference Section 4 for uses of these lines.

FIGURE 5-1. INTERFACE CONNECTIONS
<table>
<thead>
<tr>
<th>HPTC</th>
<th>PWA ASSY. 7768-77653520-D</th>
<th>PWA ASSY. 7768-77618-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>101</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>102</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>103</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>104</td>
<td>X</td>
<td></td>
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<tr>
<td>105</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>106</td>
<td>X</td>
<td></td>
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<tr>
<td>107</td>
<td>X</td>
<td></td>
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<tr>
<td>108</td>
<td>X</td>
<td></td>
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<tr>
<td>109</td>
<td>X</td>
<td></td>
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<tr>
<td>110</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>112</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>113</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>114</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>115</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>116</td>
<td>X</td>
<td></td>
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<tr>
<td>117</td>
<td>X</td>
<td></td>
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<td>118</td>
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<tr>
<td>120</td>
<td>X</td>
<td></td>
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<tr>
<td>121</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>122</td>
<td>X</td>
<td></td>
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<tr>
<td>123</td>
<td>X</td>
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<td>124</td>
<td>X</td>
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<tr>
<td>125</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>126</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>
FIGURE 5-2A. TIMING (SHEET 1 OF 2)
FIGURE 5-2A. TIMING (SHEET 2 OF 2)
FIGURE 5-2B. STEP/DIRECTION OPERATION
A minimum 18-millisecond delay is required between step pulses, if a direction change has taken place and no read/write operation was performed.

FIGURE 5-2E. GENERAL CONTROL AND DATA TIMING COMBINED
FIGURE 5-3. SCHEMATICS (SHEET 1 OF 9)
(SOFT-SECTOR CONFIGURATION)
### SIGNAL NAME | SHEET
---|---
(POR) | 4
+24V | 6
+READY | 7
+UNIT-SEL | 7
+UNIT-SEL | 4
-Z-SIDED | 7
-DIRECTION | 6
-DISK-CHANGE | 4
-DOOR-LOCK | 8
-DOOR-LOCK | 4
-DRIVE-SEL-1 | 4
-DRIVE-SEL-2 | 4
-DRIVE-SEL-3 | 4
-DRIVE-SEL-4 | 4
-HEAD-LOAD | 4
-HEAD-SEL | 9
-IN-USE | 5
-INDEX | 7
-LOW-CURRENT | 6
-PIN | 9
-READ | 8
-READ-DISABLE | 9
-READY | 7
-SINGLE-SIDED-6-HDI-SEL | 7
-SINGLE-SIDED-AND-HDI-SE | 5
-STEP | 6
-TRK0 | 6
-UNIT-SEL | 4
-WRITE-PROTECT | 9
-WRT-DATA | 8
-CT-ERASE+0 | 9
-CT-ERASE+0 | 8
-CT-ERASE+1 | 8
-CT-ERASE+1 | 9
-DOOR-CLOSED | 7
-ERASE+0 | 6
-ERASE-1 | 8
-HD-1-SEL | 6
-HD-SEL(DIR) | 6
-HD-SEL(DIR) | 4
-HD-SEL(UNIT-SEL) | 4
-HEAD-SEL(UNIT) | 8
-PULL-UP-1 | 5
-PULL-UP-2 | 4
-R/W-0 | 8
-R/W-1 | 8
-R/W-0 | 8
-R/W-1 | 8
-READ | 8
-READ-DATA | 5
-SHIELD-0 | 8
-SHIELD-1 | 8
-U2B-09 | 5
-US-07 | 5
-US-12 | 6
-US-02 | 9

| I/O PIN | SHEET | SIGNAL NAME |
---|---|---|
J102 | 1 | LOW-CURRENT |
J110 | 0 | 2-SIDED |
J112 | 0 | DISK-CHANGE |
J114 | 1 | HEAD-SEL |
J116 | 1 | IN-USE |
J118 | 1 | HEAD-LOAD |
J120 | 0 | INDEX |
J122 | 0 | READY |
J126 | 1 | DRIVE-SEL-1 |
J128 | 1 | DRIVE-SEL-2 |
J130 | 1 | DRIVE-SEL-3 |
J132 | 1 | DRIVE-SEL-4 |
J135 | 1 | WRITE-DATA |
J134 | 1 | DIRECTION |
J135 | 1 | STEP |
J142 | 0 | TRKO |
J144 | 0 | WRITE-PROTECT |
J146 | 0 | READ-DATA |
J201 | 0 | R/W-0 |
J202 | 0 | R/W-0 |
J203 | 0 | SHIELD-0 |
J204 | 0 | CT-ERASE+0 |
J205 | 0 | CT-ERASE+0 |
J207 | 0 | ERASE+0 |
J208 | 0 | R/W-1 |
J209 | 0 | R/W-1 |
J210 | 0 | CT-ERASE+1 |
J211 | 0 | CT-ERASE+1 |
J212 | 0 | SHIELD-1 |
J214 | 0 | ERASE+1 |
J308 | 0 | +24V |
J140 | 1 | WRT-ENABLE |

**FIGURE 5-3. SCHEMATIC (SHEETS 2/3 OF 9)**
FIGURE 5-3. SCHEMATIC (SHEET 4 OF 9)
FIGURE 5-3, SCHEMATIC (SHEET 5 OF 9)
FIGURE 5-3. SCHEMATIC (SHEET 7 OF 9)
FIGURE 5-3, SCHEMATIC (SHEET 8 OF 9)
FIGURE 5-3. SCHEMATIC (SHEET 9 OF 9)
ALTERNATE I/O PINS

1. INTERFACE PIN #12
2. INTERFACE PIN #10
3. INTERFACE PIN #8
4. INTERFACE PIN #6
5. INTERFACE PIN #4
6. HEAD LOAD (SEE SCH)
7. IN USE (SEE SCH)
8. 2 SIDED
9. INDEX
10. READY

U10DES
U9, U8, U7, U6, U5, U4, U3, U2 - LM393
U1, U11, U15 - 74HC14
U12, U13, U14 - 74LVC14

DC POWER CONNECTOR
MATING CONNECTOR P4

- RECOMMENDED CONNECTOR
BERG NO. CONTACTS 48005
KEY 65307-001 75979867
HOUSING 65839-012 51870305

INTERFACE CONNECTOR J3

THE RECOMMENDED CONNECTORS FOR PI ARE LISTED BELOW.

MATING HOSING 1-583717-1 WITH CONTACT PINS 3NW25/1IN-5
CONTACT AMP 563616-5 (CRIMP) 563854-3 (SOLDER)
FLAT CABLE - 3M SCOTCH FLEX 3415-001

COMPONENT SIDE - A KEY SLOT IS PROVIDED BETWEEN PINS 4 AND 6 FOR OPTIONAL CONNECTOR KEYING.
SOLDER SIDE

FIGURE 5-4. ASSEMBLY, INTERFACE AND DC POWER MATING CONNECTORS
6.1  INTRODUCTION

This section contains the instructions required to maintain the FDD. The information is provided in the form of preventive maintenance, troubleshooting and corrective maintenance.

6.2  MAINTENANCE TOOLS

The Special tools (or equivalent) required to maintain an FDD are as follows:

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>CDC MODEL NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alignment Diskette (Single-Side)</td>
<td>421-51W*</td>
</tr>
<tr>
<td>Alignment Diskette (Two-sided)</td>
<td>425-51W*</td>
</tr>
</tbody>
</table>

6.3  TROUBLESHOOTING

An improperly adjusted FDD may exhibit symptoms of one that has a malfunction; therefore, the Adjustment Procedures (paragraph 6.4) should be performed before assuming that the drive has failed.

**TABLE 6-1. ADJUSTMENT REFERENCE**

<table>
<thead>
<tr>
<th>Adjustment Paragraph No.</th>
<th>Adjustment Identification</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.4.1</td>
<td>Write-Splice Check and Adjustment</td>
</tr>
<tr>
<td>6.4.2</td>
<td>Actuator Alignment</td>
</tr>
<tr>
<td>6.4.3</td>
<td>Clamshell-Closed Switch Adjustment</td>
</tr>
<tr>
<td>6.4.4</td>
<td>Track 00 Stop Adjustment</td>
</tr>
<tr>
<td>6.4.5</td>
<td>Diskette Ejector Adjustment</td>
</tr>
<tr>
<td>6.4.6</td>
<td>Diskette Load-Pad Adjustment</td>
</tr>
<tr>
<td>6.4.7</td>
<td>Head-Unload Clearance Adjustment</td>
</tr>
<tr>
<td>6.4.8</td>
<td>Low-Current-Switch Optical-Sensor Adjustment</td>
</tr>
<tr>
<td>6.4.9</td>
<td>Azimuth Adjustment</td>
</tr>
</tbody>
</table>

*Available through local CDC sales office or distributor.*
6.3.1 DC VOLTAGE AND SIGNAL CHECK

a. Input power should be +5VDC ±5% and +24VDC ±10% measured at the input to the FDD (refer to paragraph 3.4.2).

b. Test Points: The signals at the test points should conform to the various diagrams and waveforms as listed in Table 6.2.

3. Signals should conform to Figure 5-1 and Figure 6-1 through 6-3.

<table>
<thead>
<tr>
<th>Test Point No.</th>
<th>Refer to Fig. No.</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>5-2, 6-2, 6-3</td>
<td>Analog Read Data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Resolution (Differential)</td>
</tr>
<tr>
<td>4</td>
<td>5-2, 6-2, 6-3</td>
<td>Analog Read Data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Low Resolution (Differential)</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ-2</td>
<td></td>
<td>Door Close</td>
</tr>
<tr>
<td>TJ-4</td>
<td></td>
<td>Write Protect</td>
</tr>
<tr>
<td>TJ-8</td>
<td></td>
<td>Trk 43 Sensor</td>
</tr>
<tr>
<td>TJ-12</td>
<td></td>
<td>Phase C</td>
</tr>
<tr>
<td>TJ-16</td>
<td></td>
<td>Phase A</td>
</tr>
<tr>
<td>TJ-18</td>
<td></td>
<td>D. S. Index Sensor</td>
</tr>
<tr>
<td>TJ-20</td>
<td></td>
<td>Trk 0 Sensor</td>
</tr>
<tr>
<td>TJ-11</td>
<td></td>
<td>Head-Load Output</td>
</tr>
<tr>
<td>TJ-15</td>
<td></td>
<td>LED Driver</td>
</tr>
<tr>
<td>TJ-17</td>
<td></td>
<td>Door Lock Driver</td>
</tr>
<tr>
<td>TJ-19</td>
<td></td>
<td>SS Index Sensor</td>
</tr>
</tbody>
</table>

TABLE 6-2. TEST POINTS
FIGURE 6-1. DIFFERENTIAL READ SIGNAL FOR ENTIRE TRACK

FIGURE 6-2. DIFFERENTIAL READ SIGNAL FOR PORTION OF OUTER TRACK

FIGURE 6-3 WRITE DATA, WRITE F/F OUTPUT, AND HEAD WRITE VOLTAGE FOR OUTER TRACK
6.4 ADJUSTMENT PROCEDURES
6.4.1 WRITE-SPLICE CHECK AND ADJUSTMENT

Alignment Diskette 421-51W and 425-51W are used to perform this procedure.

a. Precondition the alignment diskette by allowing it to reach room temperature for one hour.

b. Install the alignment diskette.

**CAUTION**

The Alignment Diskette is for read only. Extreme caution should be used to assure this diskette is not written on.

c. Seek to Track 00, then seek to Track 01 and Read on head 0. (No data is recorded on Track 1.)

d. Connect Channel 2 of scope to TP3 on the PWA, Channel 1 to Index J1-20 of the PWA. Set up the scope as follows:

<table>
<thead>
<tr>
<th>Channel 2 Volt/Div</th>
<th>0.1 volt/div</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 1 Volt/Div</td>
<td>2 volt/div</td>
</tr>
<tr>
<td>Channel 2 Voltage</td>
<td>AC</td>
</tr>
<tr>
<td>Channel 1 Voltage</td>
<td>DC</td>
</tr>
<tr>
<td>Vert. Mode</td>
<td>Add</td>
</tr>
<tr>
<td>Slope (Sync)</td>
<td>Pos</td>
</tr>
</tbody>
</table>

- Source to: Channel 1
- Coupling to: Low Freq.
- (High Freq. Reject)
- Trig Mode to: Channel 1
- Time Base to: 50 ms/div

e. Adjust the time of the write-splice bit until it measures per 200 ± 100 μs. Refer to Figure 6-4a to adjust the time, loosen the single-sided sensor set screw holding the (single-sided-sensor) phototransistor located on the bottom of the chassis toward the front of the unit, (Figure 6-4b). Using the adjustment tab protruding through the casting, move the phototransistor until the specification is met. Tighten the set screw while observing the scope signal. Verify that the adjustment did not change.

f. All scope settings are to remain as defined in the original setup in Step 1, but it may be necessary to slightly adjust the sync. Seek to Track 00 then seek to Track 01 and perform a read. While observing the signal on the scope, remove and reinsert the diskette three times.

After each insertion, verify that the change in the time from Index to write splice is less than 50 μs.

Repeat Steps b through f using Alignment Diskette 425-51W for the two-sided sensor adjustment tab and its associated set screw, as required.
FIGURE 6-4A. WRITE-SPLICE-TIMING

FIGURE 6-4B. SINGLE-AND TWO-SIDED SENSOR ADJUSTMENT MEANS
6.4.2 ACTUATOR ALIGNMENT

a. The alignment diskette shall be preconditioned by allowing it to reach room temperature for one hour.

b. Install the alignment diskette.

[CAUTION]

The Alignment Diskette is for read only. Extreme caution should be used to assure this diskette is not written on.

c. Connect Channel 1 of scope to TP3 on the PWA and Channel 2 to TP4 on the PWA.

d. Connect the external sync probe to index at J1-20 on PWA.

e. Set up the scope as follows:

- Channel 1: volts/div to: 0.1 volts/div
- Channel 2: volts/div to: 0.1 volts/div (Inverted)
- Channel 1: input to: AC
- Channel 2: inputs to: AC
- Vertical Mode to: Add
- Slope (Sync) to: Negative
- Trigger Source to: External
- Trigger Coupling to: Low Frequency (High Frequency Reject)
- Trigger Mode to: Normal
- Time Base to: 20 ms/div

f. Apply DC power to the drive.

g. Step to Track 38 (00100110) and perform a read on head 0.

NOTE

The trigger level is adjusted for repetitive display of data "Cateyes" consisting of two lobes (refer to Figure 6-6).

h. Change the volts/div of Channel 1 and Channel 2 to 0.02 volts/div. For an acceptable aligned unit, the voltage ratio of the smaller lobe to the larger lobe should exceed 80%.
If not in alignment, slightly loosen the stepper-motor mounting screws, (see Figure 6-9), slowly rotate the stepper motor until the amplitudes of both lobes are the same, and tighten the hardware. If there is insufficient adjustment range of the motor, perform the following:

i. Return the carriage to Track 0 and remove DC power.
ii. Loosen the stepper-motor hardware and rotate the stepper motor to each end of its adjustment range, leaving it approximately centered. Snug the hardware.
iii. Ensure that the pulley clamping screw is loose.
iv. With the probes and scope set per Steps c and d above, apply DC power.
v. Reading with Head 0, move the carriage back and forth in the vicinity of Track 0 to maximize the signal obtained (ensure that the pulley is slipping relative to the motor shaft). Tighten the pulley clamp hardware carefully so as not to move the carriage off Track 0.
vi. Seek to Track 38, again reading on Head 0.
vii. Using the adjustment tool, slowly rotate the motor until the amplitudes of both lobes is the same, and tighten the stepper-motor hardware.

j. Return to Track 0, then seek back to Track 38. Verify the adjustment. If the specification is not met, readjust the stepper motor, return to zero and seek back to Track 38. Repeat the adjustment until the specification is met.
k. Perform Track 0 Stop Adjustment.
l. Remove alignment diskette.

6.4.3 CLAMSHELL-CLOSED SWITCH ADJUSTMENT
Close the clamshell and check that it is latched. Turn the setscrew clockwise until the switch makes contact. Turn the setscrew one additional turn and a half. Open
and close the clamshell several times while observing the door-closed signal.

6.4.4 TRACK 0 STOP ADJUSTMENT
a. After applying DC power to the drive, return the carriage to Track 0.
b. Loosen Track 0 stop/cover hardware and slide the stop to the rear of the adjustment slot in the motor adapter.
c. Place a 0.030-in. (0.76mm) shim through the adjustment slot and between the cover stop and the carriage stop.
d. Slide the cover stop forward until contact is made with the 0.030-in. (0.76mm) shim, and tighten the hardware.
e. After adjustment, the gap between the cover stop and the carriage stop should be greater than 0.20 in. (0.51mm) and less than 0.035 in. (0.89mm).

6.4.5 DISKETTE EJECTOR
Insert a diskette fully and note a clicking noise as the ejector engages a pin on the clamshell.
While observing the ejector, latch and latch block (Figure 6-6) through the 1/2 in. (12.7mm) hole in the sidewall, close the clamshell. Note that closing the clamshell moved the ejector further to the rear allowing the latch to rotate counterclockwise until the tip drops over the step in the latch block.

With the clamshell closed, adjust the latch block (Figure 6-6) so the tip of the latch just clears the step.
Check by opening the clamshell slowly and observing the clamshell position when the diskette is ejected. To avoid damage, it is to be ejected when the clamshell is 1/4 in. (6.35mm) max. from the fully opened position. If further adjustments is required, move the latch block as indicated by the arrows and instruction in Figure 6-6.
Operate several times and observe that the diskette ejection is within the 1/4 in. (6.35mm) max. described above.
6.4.6 DISKETTE-LOAD-PAD ADJUSTMENT

a. Refer to Figure 6-7.
b. Energize Solenoid
c. Loosen Solenoid mounting screws (2x).
d. Move solenoid down on bracket to obtain a clearance of 0.010 to 0.015 in. (0.254 to 0.381 mm) between the load plate and the lift extension of the upper-head arm at the location of minimum clearance. Move the carriage through its full travel manually to determine the location of minimum clearance.

![FIGURE 6-7. LOAD PAD ADJUSTMENT]

6.4.7 HEAD-UNLOAD CLEARANCE

Adjust set screw on clamshell for 0.100 in. to 0.125 in. (2.54 to 3.175 mm) clearance per Figure 6-8 between flyer pads with head-load solenoid de-energized and clamshell closed.
6.4.8 LOW CURRENT SWITCH OPTICAL-SENSOR ADJUSTMENT

Some models may contain an internal Track 43 switch.

Verify adjustment 6.4.2 before beginning this adjustment.

Adjust the Low-Current-Switch optical sensor (on top of Track "0" bracket) for the proper output when positioned between Physical Tracks 42 or less and Physical Track 43 or greater.

a. Set up the scope as follows:

Channel Probe: TJ-14 or J8-2
Channel 1: volts/div to 1 V/div (0.1/div for X 10 Probe)
Channel 1: input to DC
Vertical Mode to: Channel 1
Scope (sync) to: Positive
Trigger Source to: Internal
Trigger Coupling to: DC
Trigger Mode to: Auto
Time Base to: 20 ms/div

b. Perform a seek to Physical Track 42.

c. Adjust the optical sensor for +2.4 V min.

d. Perform a seek to Physical Track 43.
e. Verify the scope reads +0.5 V max.
f. Repeat b, c and d if necessary until the DC levels in Steps c and e are met.

6.4.9 AZIMUTH ADJUSTMENT

Using an alignment diskette, seek to Track 76 and adjust azimuth by turning the azimuth set screw in the guide-rod boss. The set screw should be adjusted in such a way that the azimuth pattern is optimized between head "0" and head "1." See Figure 6-10.1 for optimum azimuth alignment. The azimuth of both heads must be less than ±12 minutes from nominal.

6.5 REMOVAL AND REPLACEMENT PROCEDURES

The following procedures give the proper sequence for removal and replacement of major assemblies. To avoid damage to parts, the procedure must be performed in sequence.

6.5.1 PRINTED-CIRCUIT BOARD (PWA)

a. Disconnect I/O Cable from J1 (refer to Figure 5-3).
b. Disconnect harnesses from connectors on printed-circuit board.
c. Remove screw from printed-circuit board adjacent to connector J1.
d. Remove PWA by detaching it from the push-in clips.
e. To replace printed-circuit board, push clips through printed-circuit board.
f. Replace screw adjacent to connector J1.
g. Reconnect harness and I/O cable.
h. Set dipswitches.
i. Perform write-splice check and adjust as necessary (par. 6.4.1).

6.5.2 CARRIAGE REPLACEMENT

Refer to Figures 6-9 and 6-10.

a. Remove clamshell and front panel.
b. Disconnect head and stepper-motor cables from PWA.
c. Remove head cables from wire guide. Remove Track "0" cover/stop.
d. Loosen hardware securing pulley to stepper-motor shaft.
e. Remove hardware securing stepper motor to motor adapter.
f. Hold pulley and carefully remove stepper motor from pulley and adapter.
g. Slide carriage out (to approximately Track 0), and loosen guide bar clamp screw closest to spindle.
h. Slide carriage in (to approximately Track 76), and remove the other guide bar clamp screw.
i. Carefully remove the carriage, pulley and guide bar.
j. After removing guide bar from carriage, unhook band spring from pin on carriage and remove spring.
k. Remove pulley clip and screw from pulley.
l. Remove band clip and nut from end of carriage.
m. Reverse above procedure to install new carriage, except:

i. Replace band with new band assembly;
ii. Leave pulley and band clips loose before installing band spring;
iii. After band spring is installed, rotate pulley the length of the foam pad to verify proper alignment. A misaligned pulley can be detected by either hearing a scraping or scratching noise, or a careful examination.
FIGURE 6-9. POSITIONING AND HEAD-LOAD MECHANISM, CLAMSHHELL COVER RAISED.
FIGURE 6-10. HEAD-LOAD CARRIAGE AND STEPPER MOTOR DETAILS
of the gap between the split portion and the inner solid portion of the band. If the pulley is not exactly aligned, insert a small tool (screwdriver), into the spring hook closest to the band and apply sufficient force to relieve tension on the band. While holding the spring with hand, twist the pulley relative to the band in an effort to realign the band and pulley, and release the spring. Check for exact alignment. Repeat this procedure until the band and pulley are exactly aligned, and then tighten band and pulley clip hardware.

iv. After carefully reinstalling the carriage assembly (ensuring that the swing arm tab is positioned above the load plate), and securing the guide bar, place the drive in a vertical position (motor up) so that the pulley is below the tail end of the carriage. At this point, check that the pulley is still properly aligned. If the pulley is misaligned, the carriage must be removed and the alignment procedure repeated. After ensuring the alignment is correct, with one hand position and hold the pulley in the approximate center of the locating hole in the motor adapter and carefully slide the motor shaft through the pulley bore, and seat the motor in the motor adapter. Use at least one screw at this point to hold the motor in place, ensuring that the screw is centered in the motor mount hole to facilitate later adjustment. Run the carriage back and forth by hand a few times so that the pulley is oriented properly on the shaft, and resume reassembly.

n. Perform the Actuator Alignment (6.4.2) after completing mechanical assembly.
o. Reinstall Track - cover/stop and perform Track 0 Stop Adjustment (6.4.4).
p. Perform azimuth adjustment (6.4.9).

6.5.3 DRIVE MOTOR ASSEMBLY

a. Perform removal procedure for printed-circuit board (paragraph 6.5.1).
b. Remove screws securing drive-motor cable clamps.
c. Remove AC connector from bracket.
d. Remove spindle drive belt.
e. Remove three (3) nuts or screws securing drive motor.
f. Remove drive-motor assembly (drive motor, capacitor, and AC connector).
g. To replace drive-motor assembly perform in reverse Steps f through a.

6.5.4 STEPPER-MOTOR REPLACEMENT

a. Disconnect stepper-motor cables from PWA and cut cable ties as required.
b. Loosen hardware securing pulley to stepper-motor shaft.
c. Remove hardware securing stepper motor to motor adapter.
d. Hold pulley and carefully remove stepper motor from pulley and motor adapter.
e. Reverse above procedure to install new motor, except: Check pulley alignment and installation per paragraph 6.5.2.m (iv).
f. Perform Actuator Alignment, 6.4.2.
6.6 FREQUENCY CONVERSION

6.6.1 OPERATING FREQUENCIES CONVERSION PROCEDURE

This procedure is to be used to convert the FDD unit from 60 Hz operation to 50 Hz operation, or vice versa. This is accomplished by reversing the dual-diameter reversible pulley on the spindle-motor shaft using the following steps:

a. Remove AC power.
b. Remove printed-circuit board assembly per paragraph 6.5.1.
c. Remove the belt from the spindle-motor pulley. (Accessible from the underside of unit.)
d. Loosen setscrew and remove pulley.
e. Reserve pulley and replace on motor shaft.
f. Position pulley allowing tolerance of 0.039 in. (0.99 mm) ± 0.10 in. (0.254 mm) between shoulder of motor mounting screws and pulley (Figure 6-11).
g. Tighten down setscrew.
h. Replace belt and printed-circuit board.

CAUTION

It is IMPORTANT that the new operating frequency be marked on the unit's rating nameplate.

NOTE: When converting from 60 Hz to 50 Hz, the same belt may be used. When converting from 50 Hz to 60 Hz, a new belt must be installed.
7.1 INTRODUCTION

This section contains detailed information on the logic circuits used in the FDD. The logic consists of two types of circuits: discrete component and integrated circuits (IC). Integrated circuits are contained within a single chip and discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

7.2 PHYSICAL DESCRIPTION (LOGIC)

All components are mounted on one side of the printed circuit board. The board is 7.0 x 8.0 inches (178 mm X 203 mm) and contain both IC and discrete component circuits.

7.3 USE OF RELATIVE LEVEL INDICATORS

The relative level indicator is a small triangle located on the input or output to a logic block. The presence or absence of this indicator indicates the conditions that are necessary to satisfy the function of the logic block. The presence of the triangle indicates a 0 logic level on that line is needed to satisfy the function. The absence of the triangle indicates a logical 1 is needed to satisfy the function.

The relative level indicator depicts the occurrence of inversion. Figure 7-1 shows some representative examples of the relative level indicator being used in this manner.

![Figure 7-1: Inversion Conventions](image)

7.4 INTEGRATED CIRCUITS

Figure 7-2 shows an example of a schematic block and the information that it contains. The first line gives the function symbol which identifies the logic function that the block performs. Refer to Figure 7-3 for a summary of function symbols. The second line gives the CDC element number. The third line on the schematic block gives the circuit reference designation.
FIGURE 7-2. INTEGRATED CIRCUIT

<table>
<thead>
<tr>
<th>FUNCTION SYMBOLS</th>
</tr>
</thead>
<tbody>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; AND GATE OR INVERTER</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; OR GATE OR INVERTER</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; EXCLUSIVE OR</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; ONE SHOT</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; SUMMING CIRCUIT, NUMBER FOLLOWING (EXAMPLE 100) INDICATES GAIN OF 100</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; LEVEL CONVERSION - TRANSMISSION LINE TO LOGIC LEVEL, SWITCH STATE TO LOGIC LEVEL OR LOGIC LEVEL TO POWER OUTPUT</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; SCHMITT TRIGGER (LOWER TRIP POINT ADJUSTABLE)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GENERAL SYMBOLS</th>
</tr>
</thead>
<tbody>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; INDICATES NON STANDARD LOGIC LEVEL</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; INDICATES ANALOG SIGNAL</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; TEST POINTS</td>
</tr>
<tr>
<td>&amp; &amp; &amp; &amp; &amp; &amp; INHIBITING INPUT</td>
</tr>
</tbody>
</table>

FIGURE 7.3. SCHEMATIC SYMBOLS
8.1 INTRODUCTION
This section contains an illustrated parts breakdown that describes and illustrates all variations of the (band-driven) Model 9406-4 Flexible Disk Drive (FDD). In general, parts are in disassembly sequence but do not necessarily indicate the maximum recommended disassembly of parts in this field.

8.2 ILLUSTRATIONS
Item numbers within a circle (1) indicate an assembly (group of parts). Item numbers without a circle, 1, indicate a single part; a group of parts that are pinned or press fitted together; or a group of parts which is normally replaced as an assembly.

8.3 PARTS LIST
In addition to the accompanying parts list on each illustration, two additional Parts Lists are available; the Top-Down Assembly/Component Parts List and the Cross Reference Index. Instruction for the use of all Parts Lists is given in para. 8.6.

8.4 PRODUCT CONFIGURATIONS
In conjunction with Table 8-1, Figure 8-1 serves two purposes;
1. When used with Table 8-1, it identifies all unique parts and assemblies for each FDD variation.
2. It identifies by sheet location where all major assemblies are broken down.

8.4.1 HARDWARE PRODUCT CONFIGURATOR (HPC)
To determine what parts are used on a particular model, find the applicable HPC number in Table 8-1. The item numbers at the top of Table 8-1 corresponds with the item numbers in Figure 8-1. All parts and assemblies that apply to the HPC number will be identified with an 'X' ('0' means not applicable). NOTE: The HPC Number is identical to the Equip. Ident. No. shown on the label.

8.5 REPLACEMENT PARTS
When ordering replacement parts for the FDD, the inclusion of the following information for each part ordered will ensure positive identification:

2. Publication Number 77653522 
3. Figure and Item Number 
4. Identification Number and Description 

NOTE: Before ordering parts however, refer to paragraph 8.5.1 Spare Parts.
8.5.1 SPARE PARTS

This Illustrated Parts Breakdown is complete to the extent that all parts and assemblies are depicted and identified. Replacement part availability depends on the materials and provisioning operation of the supplier.

To assist the service representative in selecting replacement parts with minimum requisitioning lead times, engineering-recommended spare parts which reflect the intended service level of the device are identified with the letters SP adjacent to the item number on the face of each illustration. Replaceable non-spared items will require longer requisitioning lead times.

### TABLE 8-1. PRODUCT CONFIGURATION

<table>
<thead>
<tr>
<th>ITEM NUMBERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>3333333333 3333333333 3444444444 4444444444 4444444444 4444444444 4444444444</td>
</tr>
<tr>
<td>0000000001 5555555555 9000000000 0111111111 2222222222 3333333333 44555667777</td>
</tr>
<tr>
<td>1234567890 0123456789 9012345678 9012345678 0123456789 0123456789 0101010123</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HPC</th>
<th>ITEM NUMBERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>77618101</td>
<td>X000000000G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618102</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618103</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618104</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618105</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618106</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618107</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618108</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618109</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618110</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618111</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618112</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618113</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618114</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618115</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618116</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618117</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618118</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618119</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
<tr>
<td>77618120</td>
<td>X000000000 G X000000000 X0X00X0000 X000000000 X000000000 X0X0000000 X000000000 X0X0000000 X0X0000000</td>
</tr>
</tbody>
</table>
FIGURE 8-1. PRODUCT CONFIGURATION
FIGURE 8-2. TOP MECHANICAL ASSEMBLY (SHEET 1 OF 2)
* SEE DIAGRAM SECTION OF MANUAL FOR CORRECT CIRCUIT BOARD IDENTIFICATION AND BREAKDOWN.

**FIGURE 8-2. TOP MECHANICAL ASSEMBLY (SHEET 2 OF 2)**
FIGURE 8-3. DRIVE MOTOR AND LIFTER ASSEMBLIES
FIGURE 8-4, FRONT PANEL ASSEMBLY

77653522-B 8-7
FIGURE 8-5. FEATURE KITS
FIGURE 8-6. CLAMSHELL AND LOAD PLATE ASSEMBLIES
**FIGURE 8-7. HARNESS ASSEMBLIES**

---

<table>
<thead>
<tr>
<th>ITEM IDENT NO</th>
<th>DESCRIPTION</th>
<th>WHERE USED</th>
</tr>
</thead>
<tbody>
<tr>
<td>520 77649294</td>
<td>SOLNOID WATL PROTEC ASM</td>
<td>301</td>
</tr>
<tr>
<td>524 77649284</td>
<td>UPPER HARNESS ASM</td>
<td>301</td>
</tr>
<tr>
<td>525 77649201</td>
<td>LOWER HARNESS ASM</td>
<td>301</td>
</tr>
<tr>
<td>531 10125803</td>
<td>WASHER</td>
<td>520</td>
</tr>
<tr>
<td>536 444277400</td>
<td>CABLE TIL</td>
<td>524</td>
</tr>
<tr>
<td>536 444277400</td>
<td>CABLE TIL</td>
<td>520</td>
</tr>
<tr>
<td>609 75883121</td>
<td>CABLE TIE</td>
<td>525</td>
</tr>
<tr>
<td>609 75883121</td>
<td>CABLE TIE</td>
<td>524</td>
</tr>
<tr>
<td>645 77685730</td>
<td>UPPR CABLE TIE</td>
<td>525</td>
</tr>
<tr>
<td>646 75883175</td>
<td>UPPEX GUIDE ASM</td>
<td>524</td>
</tr>
<tr>
<td>647 75883175</td>
<td>UPPEX GUIDE ASM</td>
<td>646</td>
</tr>
<tr>
<td>648 75883175</td>
<td>UPPEX GUIDE ASM</td>
<td>646</td>
</tr>
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<td>UPPEX GUIDE ASM</td>
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<tr>
<td>650 75883175</td>
<td>UPPEX GUIDE ASM</td>
<td>646</td>
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<tr>
<td>651 75495024</td>
<td>TEMINAL</td>
<td>646</td>
</tr>
<tr>
<td>652 10126217</td>
<td>SCREW</td>
<td>520</td>
</tr>
<tr>
<td>655 75495024</td>
<td>INDEX DETECTOR ASM</td>
<td>524</td>
</tr>
<tr>
<td>656 77685725</td>
<td>LOWLH CABLE</td>
<td>525</td>
</tr>
</tbody>
</table>
ITEM IDENT NO  DESCRIPTION  WHERE USED
502  77649275  ACTUATOR ASM  201
531  10125803  WASHER  202
502  03392164  SCREW  202
589  10127102  SCREW  202
591  10127901  WASHER  202
660  77049235  CARriage ASM  202
661  77049281  LAND ASM  202
662  77049282  FLAME PAD  202
663  77049283  DAMP SPRING  202
664  77049284  PULLEY  202
665  77049285  PULLEY CLIP  202
666  77049286  LAND CLIP  202
667  09325006  HINGE PIN  202
668  51777500  BOLT  202
669  73006503  WASHER  202
690  73006503  EJECTOR  523
691  73006503  LATCH  523
692  7580500  SPRING TENSION  523
693  00848201  RETAINING RING  523
694  75861575  EJECTOR SPRING  523

FIGURE 8-9. ACTUATOR AND EJECTOR ASSEMBLIES
FIGURE 8-9. STEPPER BRAKE AND CARRIAGE ASSEMBLIES
FIGURE 8-10. FEATURE KITS
8.6 PARTS LIST INSTRUCTIONS

8.6.1 ILLUSTRATION PARTS LISTS

The parts list for each illustration is an extract from the Top-Down Assembly/Component Parts list and contains only those parts depicted. Refer to paragraph 8.6.2 for explanation of parts list.

8.6.2 TOP-DOWN ASSEMBLY/COMPONENT PARTS LIST

a. Starts at HPC level and lists all parts in Item Number sequence.
b. Correlates Item numbers with part Identification numbers and the Description of each.
c. Identifies where each part is used (where used column) within the device by listing the item number(s) of the next higher assembly.

NOTE

The same part may be used in any number of assemblies or sheet locations.

8.6.3 CROSS REFERENCE INDEX

a. Lists all parts in numeric sequence (by Identification Number).
b. In conjunction with the referenced sheet number (third column) and illustrations, defines the physical location of each item identified.

8.6.4 SHEET NUMBER REFERENCING

Sheet numbers referenced on Parts Lists and Illustrations refers to sheet locations in this section. Example: Sheet reference 3 represents sheet 8-3, sheet 4 represents sheet 8-4, etc.
TOP-DOWN ASSEMBLY/COMPONENT PART LIST
ITEM IDENT NO

DESCRIPTION

WHERE

USED SHEET

-joi-776~90i4-------TOP-MlCHANicAL-ASM---------hPC-----50j-301 7764,U14
TOP MECHANICAL ASH
HPC
S05
TOP MECHANICAL ASM
HPC
S04
301 77649014
350 77646650
DRIVE HeTOR ASM
IIPC
S06
350 7764665U
DRIVE ~luTOR AS~
HPC
S03
351 77646651
DRIVE MOTOH ASM
HPC
S06
351 77646651
DHIVE ~1()TOR ASM
HPC
S03
DRIVE. ~OTOR ASM
HPC
~06
352 77646652
352 77646652
DRIVE MOTOR ASM
HPC
503
353 77646u53
DRIVE MOTOR ASh
IIPC
~06
353 77046653
DRIVE MUTOR ASM
HPC
503
354 77646655
~hIVE MOTOR ASM
hPC
503
354 '17646655
DRIVI:: HUTOR ASM
HPC
OC6
400 '17581102
Cl.hMSHELL
UPC
S03
SO~
402 776437UO
CLM.SHELL ASfi
II PC
402 77643700
CLAfiSHELL ASf,
H~C
503
405 n050~89
LATCh "oM
HPC
S03
41077631402
FkUH PAIlEL (hARRO.)
HPC
~03
411 77631302
FhON1 PAI.EL (WIG':)
HPC
503
412 77031406
FRONT PlhEL (NARRO~)
HPC
S03
415 750015'{0
SPRING
HPC
503
420 75~97201
bUTTOh
HPC
S03
~UTTON
HPC
S03
421 15897206
4jO 1'{043501
~'RONT PAhEL AS~I (f,ARhO.)
HPC
507
430 77643501
~HONT PAhEL ASM (NAkR0.)
HPe
~03
431 '('{643502
HONT PAilEL ASH (.IDE)
HPC
507
F~ONT PANEL ASH (wI~E)
HPC
503
431 77&43502
432 77&43~03
F~ONT PAllEL A~H (t'ARRO~)
HPC
507
432 77643503
FHC~T PAllEL ASK (hARRO.)
HFC
503
440 75882037
"RITE PROTECT
HPC
508
440 '15802037
WhITE PROT~CT
HPC
S03
450 75b82185
INDEX DETEC1CR KIT
HPC
508
450 75862185
INDEX DETECTOR KIT
IIPC
S03
460 7588997~
DOOR INTEfiL0CK KIT
hPC
S08
460 7588997~
DOOR INTERLOCK KIT
HPC
SD3
4'{0 77649000
T~ACK 43 KIT
HPC
S03
470 77649000
TRACK 43 KIT
HPC
508
471 1~~63336
KOUNTIN~ KIT, SlUE
HPC
513
471 756b3336
~lCUNTING KIT, SIU[
HPC
003
472 '15894197
MOUNTING KIT, BunCM
hPC
513
472 756Y4197
M~UNTIhG KIT, BeTTCM
hPC
S03
TRACK '0' UETECT ASK
HPC
508
473 77649046
47j 77649046
TRACK '0' OEnCT AS'"'
HPC
503
500 75803128
YA5E (MACHIN~U)
301
505
500 15883128
BASE (KACHIN~L)
301
504
501 75b81591
SPINDLE
301
504
ACTUATUR A5f,
301
S05
502 '17049278
502 1'1649270
ACTUATOR ASM
301
511
503 7586289,
LIt'Tlk ASh
301
S04
50j 7586269,
LUTER ASM
301
S06
504 77649030
STEpn~ BRAKE A~M
301
S05
504 77649030
STEPPER BRAKl A5M
301
512
505 75888675
bAIL ASH
301
504
50& 77641148
LOAD PLAll ASM
301
SOy
506 77647148
LOA~ PLATE AS~I
301
504
CA~HIAGE GUIDE
301
505
507 75881326
508 75b~1275
ROD GUIDE
301
505
50~ 77646600
PULLEY SPINDLE
301
504
510 7'1613697
BALL BEAkING
301
504
511 93529005
SPRII.G wAVE WASHER
301
S04
512 77649255
f;010~ ADAPTER
301
~05
513 77646890
CaVER STOP
310
505
~14 758b8590
HlhGE PIN
301
505
515 75b88591
H!kGE. PIli
301
504
51b 75888595
PIN
301
504
517 75890210
fllTCfl PIN
301
S04
518 75890211
H!TCH PIti
30 1
SO~
519 75888570
CLAMSHELL SPklN~
301
S04
520 7764n94
SOLND .RIH PRuTECT ASH
301
,04
520 77049294
~OLl'D .RIU PROTECT A~M
301
510
521 75293203
FLAT bl::LT
301
504
522 '15083240
LATCH bLOCK
301
505
525 'l50~9396
EJECTOR' ASH
301
S05
523 '1,&89396
EJECTOH A5~1
301
512
524 ""049284
UPPlR hARliE5S ASM
301
504
524 77649204
UPPI::R HAhNESS AS~
301
~10
525 77649221
LOIoiER HARNESS ASH
301
505
525 1'1649221
LO.ER HARhE~S ASM
301
510
wIRE GUI[)[
301
505
526 7764ti151
~27 75774732
PUSH Ih CLIP
301
S05
52<1 75774'{36
PU~H IN CLIP
301
505
529 10127334
SCHE~
301
S04
530 10125005
.A5HER
301
SO~
530 10125605
WASHER
301
S05
530 10125605
.ASHEh, FLAT
472
513
531 10125803
WASHER
301
S04
531 10125803
.ASHEk
502
511
531 10125803
WASHEk
520
S10
532 93592164
SCRE.
502
S11
532 935~2164
SCRE.
301
S05
532 <,3592164
SCREW
301
504
533 15004600
SChE~
301
SO~
534 18862916
SCRI::W
301
S05
~3, 935Y2162
SCRl.
301
S04
535 93592162
SCREw
301
505
535 93592102
SC~['
503
506
536 94271400
CABLE. TIE
301
S04
53<> <,4277400
CAULE TIL
473
S08
536 94277400
CABLE TIE
520
S10
536 94277400
CAbLE TIl::
52~
510
537 10126401
WASHER
301
S04
538 10125712
~CRE'
301
504

77653522-B

I TEM I DENT NO

DESCRI PTION

WHERE USED SHEET

-540-716~~2i5-------GuiDE-ROD-SPRiNG-----------301-----~05-541
542
542
543
550
551
555
556
560
561
562
563
564
565
566
567
568
569
575
,76
577
578
579

93819248
935~215U

93592158
77648216
75726Y25
75726924
75738402
75738480
62121108
83435504
16439600
77649003
77647990
77<>~8209

75896006

SCREw
SCREw
SCRE.
SHIM
MOTOR
MOTOR
CAPACITOR
CAPACITOR
TERflINAL
CONTACT
CAPACITOR BRACKET
AC CAbLE
AC CONNECTOR BRACKET
DC CABLE
CRIVl PULLEY

83413405

SCRl~

93592202
10126104
75882740
75882735
7765b915
75882'{25
77658910

SCRl.

560 92021009
585 75293954
586 00848201
587 75882333
588 '/1636695
589 10127102
,89 10127102
589 10127102
590 75806502
591 1012~801
591 10125801
592 77648205
593 77612981
594 77610030
595 77646804
596 75899160
597 92H20166
598 10127166
600 75889295
601 75885407
602 1'7646590
603 9~376903
603 94376903
605 776~9007
606 77641995
607 75293~55
60977612011
60977612011
60~ 77612011
610 75881363
615 75880751
616 75b89215
617 10127169
620 77647980
621 77649099
622 '{5882038
623 77647147
624 77646623
625 94376916
630 75b81895
631 75882011
632 93564057
633 920330S'{
634 93820'{82
635 93820248
636 75881715
637 75881892
638 75888607
639 75888610
640 75881710
641 758b2016
642 17610637
645 77685730
646 75883075
647 75883181
648 75'{20001
6~9 92498024
650 77631900
651 '15882328
652 10126217
653 10127114
655 75889295
656 77685725
660 77643425
661 77649281
662 '{7649282
663 77649283
664 17646618
665 77646362
666 77661198
667 09035006
668 53777900
668 537.,.,900
669 75806503
675 77646670
676 77649035
677 77646880
678 75880531

~ASHEk

COVER
CYLINDER
PISTOII
ROLLER
SPHING
[,O.EL PlI.
CONI'ECTU~ HOUSING
RETAINING RING
SOLENOlt ASM
50LEhOID liOUNT
SCREW
SCREW
SCRE.
WASIIER
WASHU
"ASHER
CABLE
DIOCE
DOHL PIlI
BUMPER
LATCH SPRING
SCREW
5CRE.
INDEX DETECTOR ASM
OPTICAL S.ITCh
SENSOR PLAT~
SCREW
SCRE'
TRACK '0' OPTICAL S.ITCH
TRACK '0' BRACKET
CONNECT(;R HUUSlhG
CAULE TIE
CABLl TIE
CA~LE TIE
OPTICAL S.ITCh
SoITCH
NUT PLAT£
SCREw
LOA~ PLATl
PIVOT BRACKET
r'OAI.
SPR ING
PIVOT PIN
SCRE.
CONE ASM
SPRING
WASHER
RETAINING RING
SCREw
SCREw
CONE
BEARING
SHAFT
RETAIIllR
SPACER
COhPRl5SIOIl SPRING
SCREw
UPPER CAbLE
UPPER GUI~E ASM
UPPlK GUIDE
PHOTO S()URCE
TEkHINAL
SOLE~OID URACKET
SOL[NOID ASM
SCREw
SChEo
IhDEX DETECTOR ASM
LO.[R CABLE
CARRIAGE ASH
UAND ASH
FOAM PAD
BAND SPRING
PULLEY
PULLEY CLIP
BAND CLIP
ROLL PIll
NUT
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UPPER ARM ASM
LO_ER ARH A5M
LO~ER CARRIAGE
TGP COHR

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8-15


## TOP-DOWN ASSEMBLY/COMPONENT PART LIST

<table>
<thead>
<tr>
<th>ITEM IDENT NO</th>
<th>DESCRIPTION</th>
<th>WHERE USED SHEET</th>
</tr>
</thead>
<tbody>
<tr>
<td>670 75880785</td>
<td>ARM SPRING</td>
<td>660 S12</td>
</tr>
<tr>
<td>680 75488790</td>
<td>SPRING RETAINER</td>
<td>660 S12</td>
</tr>
<tr>
<td>681 10125013</td>
<td>SCREW</td>
<td>660 S12</td>
</tr>
<tr>
<td>682 94277614</td>
<td>CAULK TIL</td>
<td>660 S12</td>
</tr>
<tr>
<td>683 10127110</td>
<td>SCREW</td>
<td>660 S12</td>
</tr>
<tr>
<td>684 75684136</td>
<td>CAULK PROTECT</td>
<td>660 S12</td>
</tr>
<tr>
<td>685 77643437</td>
<td>LOAD PLATE LIFTER</td>
<td>301 S04</td>
</tr>
<tr>
<td>690 75690961</td>
<td>EJECTION</td>
<td>523 S11</td>
</tr>
<tr>
<td>691 75690966</td>
<td>LATCH</td>
<td>523 S11</td>
</tr>
<tr>
<td>692 75693550</td>
<td>SPRING TORSION</td>
<td>523 S11</td>
</tr>
<tr>
<td>693 90044861</td>
<td>RETAINING RING</td>
<td>523 S11</td>
</tr>
<tr>
<td>694 75601575</td>
<td>EJECTION SPRING</td>
<td>523 S11</td>
</tr>
<tr>
<td>700 77649925</td>
<td>STEPPEN ASH</td>
<td>504 S12</td>
</tr>
<tr>
<td>701 77643995</td>
<td>BRACK</td>
<td>504 S12</td>
</tr>
<tr>
<td>702 77649923</td>
<td>SPRING</td>
<td>504 S12</td>
</tr>
<tr>
<td>703 77619675</td>
<td>STEPPER TOP才会</td>
<td>700 S12</td>
</tr>
<tr>
<td>704 75293954</td>
<td>CONNECTOR HOUSING</td>
<td>700 S12</td>
</tr>
<tr>
<td>710 75685061</td>
<td>MOUNTING ADAPTER</td>
<td>471 S13</td>
</tr>
<tr>
<td>711 75686167</td>
<td>ADAPTER</td>
<td>472 S13</td>
</tr>
<tr>
<td>712 10127111</td>
<td>SCREW</td>
<td>471 S13</td>
</tr>
<tr>
<td>713 10127121</td>
<td>SCREW</td>
<td>472 S13</td>
</tr>
</tbody>
</table>
9.1 INTRODUCTION

The following paragraphs contain the following wire lists: Upper-Harness Assembly; Lower-Harness Assembly; Stepper Motor; DC Harness; Sensor Assembly Track 43; Door-Lock-Solenoid Activity LED and Head Assemblies.

9.2 UPPER-HARNESS ASSEMBLY

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Violet</td>
<td>S/S Index Anode</td>
<td>J6-1</td>
<td>15 (381mm)</td>
</tr>
<tr>
<td>Gray</td>
<td>D/S Index Cathode</td>
<td>J6-5</td>
<td>15 (381mm)</td>
</tr>
<tr>
<td>Brown</td>
<td>Common Door Switch</td>
<td>J6-3</td>
<td>15 (381mm)</td>
</tr>
<tr>
<td>Yellow</td>
<td>N/O Door Switch</td>
<td>J6-4</td>
<td>15 (381mm)</td>
</tr>
</tbody>
</table>

9.3 LOWER-HARNESS ASSEMBLY

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yellow</td>
<td>D/S Index Collector</td>
<td>J9-4</td>
<td>13 (330mm)</td>
</tr>
<tr>
<td>Brown</td>
<td>D/S Index Emitter</td>
<td>J9-5</td>
<td>13 (330mm)</td>
</tr>
<tr>
<td>Orange</td>
<td>S/S Index Collector</td>
<td>J9-2</td>
<td>13 (330mm)</td>
</tr>
<tr>
<td>Black</td>
<td>S/S Index Emitter</td>
<td>J9-3</td>
<td>13 (330mm)</td>
</tr>
</tbody>
</table>

9.4 STEPPER MOTOR

<table>
<thead>
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<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orange</td>
<td>ØA</td>
<td>J3-1</td>
<td>8 (203mm)</td>
</tr>
<tr>
<td>Brown</td>
<td>ØB</td>
<td>J3-3</td>
<td>8 (203mm)</td>
</tr>
<tr>
<td>Yellow</td>
<td>ØC</td>
<td>J3-5</td>
<td>8 (203mm)</td>
</tr>
<tr>
<td>Red</td>
<td>ØD</td>
<td>J3-7</td>
<td>8 (203mm)</td>
</tr>
</tbody>
</table>

9.5 DC HARNESS

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Red</td>
<td>J4-5 +5V</td>
<td>J10-5</td>
<td>8 (203.2mm)</td>
</tr>
<tr>
<td>Black</td>
<td>J4-2 GND</td>
<td>J10-6</td>
<td>8 (203.2mm)</td>
</tr>
<tr>
<td>Orange</td>
<td>J4-1 +24V</td>
<td>J10-1</td>
<td>8 (203.2mm)</td>
</tr>
<tr>
<td>Brown</td>
<td>J4-3 +24V Return</td>
<td>J10-2</td>
<td>8 (203.2mm)</td>
</tr>
</tbody>
</table>

9.6 SENSOR ASSEMBLY TRACK 43, TRACK 00 HARNESS ASSEMBLY

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Red</td>
<td>Current-Switch Collector</td>
<td>J8-3</td>
<td>7.3 (185.4mm)</td>
</tr>
<tr>
<td>White</td>
<td>Current-Switch Cathode</td>
<td>J8-6</td>
<td>7.3 (185.4mm)</td>
</tr>
<tr>
<td>Blue</td>
<td>Current-Switch Emitter</td>
<td>J8-4</td>
<td>7.3 (185.4mm)</td>
</tr>
<tr>
<td>Green</td>
<td>Current-Switch Anode</td>
<td>J8-5</td>
<td>7.3 (185.4mm)</td>
</tr>
<tr>
<td>Brown</td>
<td>Anode Track 0</td>
<td>J8-7</td>
<td>7.3 (229mm) 185.4</td>
</tr>
<tr>
<td>Yellow</td>
<td>Cathode Track 0</td>
<td>J8-8</td>
<td>7.3 (229mm) 185.4</td>
</tr>
<tr>
<td>Orange</td>
<td>Emitter Track 0</td>
<td>J8-10</td>
<td>7.3 (229mm) 185.4</td>
</tr>
<tr>
<td>Black</td>
<td>Collector Track 0</td>
<td>J8-9</td>
<td>7.3 (229mm) 185.4</td>
</tr>
</tbody>
</table>

77653520-A
### 9.7 DOOR-LOCK SOLENOID ACTIVITY LED

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>Door-Lock Solenoid+</td>
<td>J7-3</td>
<td>16 (406mm)</td>
</tr>
<tr>
<td>Black</td>
<td>Door-Lock Solenoid-</td>
<td>J7-4</td>
<td>16 (406mm)</td>
</tr>
<tr>
<td>Brown</td>
<td>Activity LED Anode</td>
<td>J7-2</td>
<td>16 (406mm)</td>
</tr>
<tr>
<td>Blue</td>
<td>Activity LED Cathode</td>
<td>J7-1</td>
<td>16 (406mm)</td>
</tr>
</tbody>
</table>

### 9.8 HEAD ASSEMBLIES

#### Head 0

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>Read/Write</td>
<td>J2-1</td>
</tr>
<tr>
<td>White</td>
<td>Read/Write</td>
<td>J2-2</td>
</tr>
<tr>
<td>White</td>
<td>Shield</td>
<td>J2-3</td>
</tr>
<tr>
<td>Green</td>
<td>Erase+</td>
<td>J2-4</td>
</tr>
<tr>
<td>Red</td>
<td>Center Tap</td>
<td>J2-5</td>
</tr>
<tr>
<td>-</td>
<td>Key</td>
<td>J2-6</td>
</tr>
<tr>
<td>Yellow</td>
<td>Erase-</td>
<td>J2-7</td>
</tr>
</tbody>
</table>

#### Head 1

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>Read/Write</td>
<td>J2-8</td>
</tr>
<tr>
<td>White</td>
<td>Read/Write</td>
<td>J2-9</td>
</tr>
<tr>
<td>Red</td>
<td>Center Tap</td>
<td>J2-10</td>
</tr>
<tr>
<td>Green</td>
<td>Erase+</td>
<td>J2-11</td>
</tr>
<tr>
<td>White</td>
<td>Shield</td>
<td>J2-12</td>
</tr>
<tr>
<td>-</td>
<td>Key</td>
<td>J2-13</td>
</tr>
<tr>
<td>Yellow</td>
<td>Erase-</td>
<td>J2-14</td>
</tr>
</tbody>
</table>

### 9.9 SOLENOID HARNESS ASSEMBLY

<table>
<thead>
<tr>
<th>Wire Color</th>
<th>Origin</th>
<th>Destination</th>
<th>Approximate Length, Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>Head-Load Solenoid+</td>
<td>J5-1</td>
<td>9 (229mm)</td>
</tr>
<tr>
<td>Black</td>
<td>Head-Load Solenoid-</td>
<td>J5-2</td>
<td>9 (229mm)</td>
</tr>
<tr>
<td>Green</td>
<td>Write-Protect Anode</td>
<td>J5-5</td>
<td>9 (229mm)</td>
</tr>
<tr>
<td>Red</td>
<td>Write-Protect Collector</td>
<td>J5-7</td>
<td>9 (229mm)</td>
</tr>
<tr>
<td>Blue</td>
<td>Write-Protect Emitter</td>
<td>J5-8</td>
<td>9 (229mm)</td>
</tr>
<tr>
<td>White</td>
<td>Write-Protect Cathode</td>
<td>J5-4</td>
<td>9 (229mm)</td>
</tr>
</tbody>
</table>

*77653520-A*
APPENDIX C

Flexible Diskette Description

and Maintenance
APPENDIX C

DISKETTE DESCRIPTION

In standard IBM 3740 single density format, a diskette stores up to 256, 256 bytes of data. In DEC double density format, a diskette stores up to 512, 512 bytes of data. DEC double density format diskettes are made from a standard IBM 3740 format diskette by changing the data address mark on each sector and by writing the data in MFM double density format. Configuration choices for diskettes are:

1. Double or single sided.
2. Hard sectored or soft sectored.
3. With or without a write protect notch.

The DSD 480 is shipped with double sided drives. This gives the DSD 480 the ability to read whether single or double sided diskettes.

If a single sided diskette is used, the controller will only allow actions on side #0. When double sided diskettes are used, the controller will read, write or format both sides.

NOTE

Do not use IBM double density diskette Part No. 1766872. These diskettes are intended for use on double-sided drives only.
The DSD 480 requires the use of soft sectored diskettes. To determine if you have a soft or hard sectored diskette, rotate the mylar diskette inside the envelope while looking through the index mark access hole. If you observe more than one hole punched in the mylar diskette you have a hard sectored diskette. Soft sectored diskettes have only one index hole punched in them.

The data and programs stored on a diskette can be protected from being rewritten. The diskette is "write-protected" by uncovering a notch in the sealed protective jacket at the location shown in Figure C-2. When the write protect notch is uncovered, nothing can be written on the diskette. When the write protect notch is covered, writing is allowed on the diskette. Any opaque tape can be used to cover the write protect notch.

Figure C-1. Diskettes
Unlike rigid diskettes, industry standards have been established for the physical format of the recorded data on diskettes. Each of the formats used by the DSD 480 -- IBM 3740 single density and DEC double density -- records data on 77 concentric tracks, at a track density of 48 tracks per radial inch. Each track is divided into 26 sectors. Each sector contains 128 eight bit bytes of user data in single density format and 256 eight bit bytes of user data in double density format.

Each sector has an ID (identification) field and a data field. A unique bit pattern known as the ID address mark enables the controller to recognize the start of an ID field. The ID field also contains a track address byte, a head address byte, and a sector address byte. Appended to these diskette address bytes is a pair of CRC (cyclic redundancy check) bytes. These are used to determine if a data error has occurred while reading the diskette address data.

The controller is able to find the sector it wants to read or write by scanning the ID fields. Note that the ID field just described is the same for diskettes containing single density data and those containing double density data. In both cases, all the data bytes contained in the ID field are encoded using the "double frequency" recording technique associated with single density.
Following the ID field of each sector is the data field. The beginning of the data field is identified by another unique bit pattern called the Data Address Mark. After this mark are the 128 or 256 bytes of data and another pair of CRC check bytes. Figure C-3 is a schematic representation of a single density track format. Figure C-4 shows the format of a DEC double density track. Note that only the 256 user data bytes and the 2 CRC bytes following the data are encoded in double density using the MFM ("modified frequency modulation") recording technique. All the other fields (preamble, postamble, and ID) are recorded in the same manner as the single density formatted track.
Figure C-3. General Track Format
### DEC Double Density Track Format

<table>
<thead>
<tr>
<th>Byte</th>
<th>ID Address Mark</th>
<th>Track Address</th>
<th>Zeros</th>
<th>Sector Address</th>
<th>Zeros</th>
<th>CRC</th>
<th>CRC</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>3</td>
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</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **IDAM = FE/C7**
- **DAM = FD/C7**
- **DDAM = F9/C7**
- **Data/Clock**

### Figure C-4

- **Gap 1**: 320 Bytes
- **Gap 2**: 5 Bytes
- **Gap 3**: 6 Bytes
- **Data Field**: 46 Bytes
- **Index Address Mark**: 46 Bytes

---

**Note:**
- Write gate turn on for update of next data field.
- Where Hex 00 or FF is optional, FF is recommended.
DISKETTE CARE GUIDELINES

The following handling recommendations for diskettes should be followed to prevent unnecessary loss of data or interruptions of system operation.

1. Do not touch the exposed diskette surface.
2. Keep the diskette away from heat and sunlight.
3. Do not use paper clips on the diskette.
4. Do not expose the diskette to magnets or tools that may have become magnetized.
5. Keep diskettes stored in their envelopes. Diskettes not being used should be stored vertically in a file box.
6. Do not write on the envelope containing the diskette.

The reliability of your system depends on the care you exercise in handling your diskettes.
IBM DISKETTE TYPES

IBM DISKETTE 1

The IBM Diskette 1, also known as a one-sided diskette, has a recording surface on one side only. Because the diskette drive can have a read/write head that contacts both sides, the side of the diskette that is opposite the recording surface is also finished to a smooth surface. The IBM Diskette 1 is available in three formats: 128, 256, and 512 bytes per sector.

128 Bytes per Sector (IBM Part 2305830)

This diskette has 77 tracks (00 through 76), with one track per cylinder. Each cylinder on this diskette, including the index cylinder (00), consists of 26 sectors with 128 bytes per sector. Cylinders 1 through 74 are available for user data providing 1924 sectors of 246,272 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

When this diskette is used for basic data exchange, 73 cylinders (1 through 73) are used. Cylinder 74 is not used. A basic data exchange diskette provides 1898 sectors or 242,944 bytes.

256 Bytes per Sector (IBM part 2305845)

This diskette has 77 tracks (00 through 76), with one track per cylinder. The index cylinder (00) consists of 26 sectors with 128 bytes per sector. Cylinders 1 through 76 have 15 sectors per cylinder. Each sector is 256 bytes long. Cylinders 1 through 74 are available for user data providing 1110 sectors or 284,160 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

512 Bytes per Sector (IBM Part 1669954)

This diskette has 77 tracks (00 through 76) with one track per cylinder. The index cylinder (00) consists of 26 sectors with 128 bytes per sector. Cylinders 1 through 76 have 8 sectors per cylinder. Each sector is 512 bytes long. Cylinders 1 through 74 are available for user data providing 592 sectors or 303,104 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

IBM DISKETTE 2

The IBM Diskette 2, also know as a two-sided diskette, has a recording surface on each side. The IBM Diskette 2 is available in two formats: 128 and 256 bytes per sector.

128 Bytes per Sector (IBM Part 1766870)

This diskette has 77 cylinders (00 through 76). The index cylinder (00) consists of 26 sectors with 128 bytes per sector on each side of the diskette for total of 52 sectors. Cylinders 1 through 76 each have 26 sectors with 128 bytes per sector on each
side of the diskette for a total of 52 sectors per cylinder. Cylinders 1 through 74 are available as primary cylinders for data providing 3848 sectors or 492,544 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

256 Bytes per Sector (IBM Part 2736700)

This diskette has 77 cylinders (00 through 76). The index cylinder (00) consists of 26 sectors with 128 bytes per sector on each side of the diskette for a total of 52 sectors. Cylinders 1 through 76 each have 15 sectors with 256 bytes per sector on each side of the diskette for a total of 30 sectors per cylinder. Cylinders 1 through 74 are available as primary cylinders for data providing 2220 sectors or 568,320 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

IBM DISKETTE 2D

The IBM Diskette 2D is a two-sided, double-density diskette. Two-sided, of course, means that the diskette has a recording surface on each side. Double density means that the bits on this diskette are written at twice the density of the bits on the IBM Diskettes 1 and 2.

256 Bytes per Sector (IBM Part 1766872)

This diskette has 77 cylinders (00 through 76). The index cylinder (00) consists of 26 sectors with 128 bytes per sector on side 0 and 26 sectors with 256 bytes per sector on side 1, for a total of 52 sectors. Each 256-byte sector on cylinder 0 contains two 128-byte data set labels. Cylinders 1 through 76 each have 26 sectors with 256 bytes per sector on each side of the diskette for a total of 52 sectors per cylinder. Cylinders 1 through 74 are available as primary cylinders for data providing 3848 sectors or 985,088 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

512 Bytes per Sector (IBM Part 1669044)

This diskette has 77 cylinders (00 through 76). The index cylinder (00) consists of 26 sectors with 128 bytes per sector on side 0 and 26 sectors with 256 bytes per sector on side 1, for a total of 52 sectors. Each 256-byte sector on cylinder 0 contains two 128-byte data set labels. Cylinders 1 through 76 each have 15 sectors with 512 bytes per sector on each side of the diskette for a total of 30 sectors per cylinder. Cylinders 1 through 74 are available as primary cylinders for data providing 2220 sectors or 1,136,640 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.

1024 Bytes per Sector (IBM Part 1669045)

This diskette has 77 cylinders (00 through 76). The index cylinder (00) consists of 26 sectors with 128 bytes per sector on side 0 and 26 sectors with 256 bytes per sector on side 1 for a total of 52 sectors. Each 256-byte sector on cylinder 0 contains two 128-byte data set labels. Cylinders 1 through 76 each have 8 sectors with 1024 bytes per sector on each side of the diskette for a total of 16 sectors per cylinder. Cylinders 1 through 74 are available as primary cylinders for data providing 1184 sectors or 1,212,416 bytes. Cylinders 75 and 76 are reserved for alternative cylinder assignment.
APPENDIX D

LSI-II and PDP-11

Bootstrap PROM Program
DSD 440 BOOTSTRAP PROM

1. TITLE: DSD 440 BOOTSTRAP PROM
2. BOT440 MAC 22-MAR-79
3. IIF NDF $PDP11.
4. IIF DF $PDP11.

BOOTSTRAP FOR DSD440 FLOPPY DISK CONTROLLER

BOOTS EITHER SINGLE OR DOUBLE DENSITY FLOPPIES

ALSO WORKS WITHOUT CHANGE IN RX01 - DSD-210 MODE

NOTE - THE DISKETTE BEING BOOTTED MUST HAVE THE CORRECT MONITOR

FOR THE EXISTING HARDWARE CONFIGURATION

** NOTE ON BOOTING WHILE REAL TIME CLOCK IS ENABLED **

THIS BOOT CAN BE STARTED WITH A RUNNING REAL TIME CLOCK IN 2 WAYS

1) ENSURING THAT THE STACK IS POINTING TO NON-EXISTANT MEMORY THUS

FORCING A DOUBLE BUS ERROR ON ANY INTERRUPT AND TYPING

"173000G" AND TYPING "P" IF HALTS OCCUR DUE TO ATTEMPTED INTERRUPTS.

2) BY SETTING THE PSW AHEAD OF TIME TO DISABLE INTERRUPTS BY TYPING

"P5 340(CR)" AND "R71 173000(CR)" AND Hitting "P"

IF A 173000G IS TRIED AND A CLOCK INTERRUPT OCCURS

AFTER THE FIRST INSTRUCTION AND BEFORE THE THIRD INSTRUCTION THEN TYPE "P"

UNTIL THE CLOCK IS DISABLED.

THE BOOTSTRAP PROCEEDS IN 4 STEPS

1) SELECT DEVICE DETERMINES DEVICE TO BE BOOTED

2) RAM TEST CHECKS ALL AVAILABLE MEMORY FOR STUCK BITS

ON BOTH DATA AND ADDRESS LINES (0-30K)

DOES BOTH DATA = ADDRESS AND PATTERN TESTS

1) LOADS MEMORY TO O'S AND SIZES MEMORY

2) LOADS MEMORY = ADDRESS AND CHECKS

3) LOADS MEMORY = ADDRESS COMPLEMENT. CHECKS

4) LOADS MEMORY WITH THE REPEATING PATTERN OF

131617, 154702, 166343, 173161, 175470

3) FILL-EMPTY

CHECKS DSD440 - PROCESSOR DATA PATH FOR

SYNTAX AND DATA ERRORS. ALSO INSURES ALL

AVAILABLE ADDRESS LINES TOGGLE UNDER DMA.

CHECKS FILL-EMPTY WITH BUFFERS AT 774.

17700, 137700, 37670, 17700: IF MEMORY EXISTS.

READS IN BLOCK 0 FROM DISKETTE IN EITHER

RX01 OR RX02 MODE AND STARTS AT LOC 0

ALSO SELECTS CORRECT DENSITY IN RX02 MODE.

ERROR HALTS OR HANG UP LOOPS (ADDRESSES RELATIVE TO BOOT BASE ADDR)

156 HALT MEMORY ERROR AT LOC -2(R4). READ RO. EXPECT ZERO

204 HALT MEMORY ERROR AT -2(R4). READ RO. EXPECT 0

252 HALT FILL-EMPTY ERROR IF R5=BOOT+522. SP=5000

2) MEMORY ERR IF R5=BOOT+112, SP=5002

3) LOOP UNIL ADDRESS SELECTED FOR BOOTING DOESN'T RESPOND

304 HALT ERROR FLAG IN RXCS SET AFTER INIT

324 HALT RXCS INTERFACE REGISTER STUCK BIT PROBLEM

364 HALT RXDB INTERFACE LATCH PROBLEM. NOTE C(RXDB)

400-402 LOOP DSD440 TRANSFER REQUEST HANGUP (FILL-EMPTY)

414-416, 452-454 TRANSFER REQUEST HANGUP (FILL-EMPTY)

476-600, 604-604 TRANSFER REQUEST HANGUP (BOOTSTRAP)

502-524, 556-650 TRANSFER REQUEST HANGUP (BOOTSTRAP)

742-746 LOOP DSD440 FLAG WAIT ROUTINE HANGUP

774 HALT FLOPPY READ ERROR. PROCEED TO TRY NEXT DRIVE

C(SP) = DEFINITIVE ERROR STATUS

C(R5) = SECTOR # WITH PROBLEM

C(RO) = DRIVE # WITH ERROR
THIS USUALLY HAPPENS WITH A BAD DISKETTE AND MAY OCCUR IF AN UN-BOOTABLE DISKETTE IS IN DRIVE 0. A "PROCEED" FROM HERE RESULTS IN ATTEMPTING TO BOOT THE OTHER DRIVE.

START ADDRESSES

BOOT+0 (Typically 173000) Boots device with RXCS at 177170
BOOT+20 (Typically 173020) Boots device with RXCS at 177150
BOOT+40 (Typically 173040) General device entrance - user

SET'S R0=340, R1=2. LOC 0 = desired RXCS

If real time clock must be left on then set

$5/340<CR> and R7/173040<CR> and proceed

A "BOOT" on an 11/04 or 11/34 prints R0, R4, SP, R7 on the terminal.

If an error halt occurs at boot+774 while booting then booting again on an 11/04 or 11/34 prints out the following.

RO = current drive # being booted from.
R4 = load address where error occurred.
SP = definitive status of error.
R7 = error halt addr+2

Note - a halt or hangup occurring between 742-746 that will not respond to break or halt is generally due to lack of DMA grant continuity on the bus. User should put DSD440 interface card closer to the processor and ensure grant continuity.

DSD440 - RX02 register syntax defs

RXCS=177170
ERR INIT X M X02 ?? SID DEN TRQ IEN DON UNI FUN FUN GO
ERR= 1000000 ERR ERROR FLAG
400000 INI LOAD INTO RXCS TO INITIALIZE
300000 XM EXTENDED MEMORY SELECT BITS
DBDMA= 4000 X02 = 1 if RX02 mode syntax
400 DEN SET = 1 FOR DOUBLE DENSITY
200 TRQ TRANSFER REQUEST - DATA TO/FROM RXDB
16 FUN FUNCTION <0-7> - SET "GO" TO EXEC

RXDB=RXCS+2

N XM WCV SID DRV DRV DEL DSK DEN A/C INT SID CRC
#1 RDY DAT DEN ERR LOW DON RLY ERR

REGISTER USAGE IN DSD440 SECTION

XCS= X1 R1 POINTER TO RXCS
XDB= X2 R2 POINTER TO RXDB
LDP= X4 R4 LOAD POINTER
SET= X5 R5 CURRENT SECTOR # (1.3.5.7)
(SP) WORD COUNT FOR CURRENT DENSITY

UNIT # BOOTED FROM (0.1)

000000 012706 BOT170.:MOV #1. SP; INHIBIT INTERRUPTS IN ONE INSTRUCTION
000004 012700 MOV #340. RO; SET PROCESSOR STATUS WORD
000010 106400 MTPS RO; FROM REG SINCE READ-MODIFY-WRITE CYCLE INTO PROM CAUSES TIMEOUT

Above 5 words become /MOV #340. RO /MOV RO. @177776 /NOP /IN PDP-11 BOOT
DSD 440 BOOTS TRAP PROM MACRO M113 15-SEP-BO 11.25 PAGE 1-2

DLS-11 VERSION

000012 012710 MDV #177170. (RO) : SET DEVICE ADDRESS
000016 000040 BR BOTCOM
000020 012700 BOT150 MDV #340. RO : SET PROCESSOR STATUS WORD
000024 012400 MTPS RO : IN ORDER TO DISABLE INTERRUPTS
000026 000024 NDF : MAKE MINIMAL CHANGES TO PDP-11
000030 012710 MDV #177150. (RO) : LOAD ALTERNATIVE DEVICE ADDR

000034 005001 BOTCOM CLR R1 : SET UP MEM TEST PTR
000036 011021 MDV (RO), (R1)+ : LOAD DEVICE ADDR INTO LOC 0

000040 012706 BGTGEN: MDV #5002; SP : INIT STACK
000044 000005 RESET
000046 004467 JSR R4. MEMGH : GET POINTER TO TRAP ROUTINE

000052 012766 TRAP4: MDV #341. 2(SP) : SETS CARRY ON TRAP TO 4
000056 000041 CLR
000060 000002 RTI : ALSO SETS CURRENT PRIORITY HIGH
000062 047177 ; WORD 47177 : LSI-11 CHECKSUM WORD FOR BOTCHK
000064 05021 ; WORD 57012 IF PDP-11 BOOT

000068 010421 CLR (R1)+ : BUMP TO LOC 4
000070 010521 MDV R4. (R1)+ : LOAD TRAP VECTOR
000072 010102 MDV RO. (R1)+ : LOAD TRAP PSW VALUE = 340

000074 05022 2$ : CLR (R2)+ : FIND TOP OF AVAILABLE MEMORY
000076 103400 BCS 4$ : CARRY SET BY TRAP TO 4
000078 020227 CMP R2. #160000 : AT END OF PDP-11 ADDR SPACE?
000080 103773 BLO 2$ : FILL EMPTY TEST - DONE AT MULTIPLE BUFFER ADDRESSES IN ORDER
000082 05042 4$ : CLR -(R2) : SET POINTER TO LAST LOCATION+2
000084 004567 JSR R5. MEMCHK : TEST TO TOP OF MEMORY
000086 000022 ; FILL EMPTY TEST - DO AT MULTIPLE BUFFER ADDRESSES IN ORDER TO TOGGLE ALL ADDRESS BITS IN SYSTEM MEMORY
000088 004567 JSR R5. FILEMP : DO FILL-EMPTY BUFFER TEST

000090 001500 ; FILL EMPTY TEST - DO AT MULTIPLE BUFFER ADDRESSES IN ORDER TO TOGGLE ALL ADDRESS BITS IN SYSTEM MEMORY
000092 017700 10<5>100 ; START FILL AT BEGINNING OF
000094 017700 10<5>1624 ; PATTERN REPETITION LEFT BY RAM TEST
000096 037676 10<5>3262 ; DO DMA TEST ACROSS ALL ADDRESS BITS

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DSD 440 BOOTSTRAP PROM MACHO M1113 15-SEP-80 11 25 PAGE 1-3
LSI-11 VERSION

000126 077704 10+<3*6540 > THAT CAN BE SH IN AVAILABLE MEMORY
000130 137760 10+<3*#816 < SO ALL BITS TOGGLE OK
000132 000000 0 : ADDRESS TERMINATOR
000134 000573 BR BOT440 **********
DSD 440 BOOTSTRAP PROM MACRO M1113 15-SEP-80 11.25 PAGE 2
LSI-11 VERSION

ROUINE TO TEST MEMORY FROM C(R1) = LOW LIMIT
TO C(R2) = UPPER LIMIT BEYOND TEST
IF ERRORS FOUND HALTS WITH R4 POINTING TO ERROR LOC. OR 2 BEYOND
RO = DATA READ

000136 010104 MEMCHK MOV R1, R4 ; GET STARTING ADDRESS
000140 010400 2$: MOV R4, R0 ; KILL FLAG <MOV R4, (R4)+;
00014C 010024 CMP R0, (R4)+ ; LOAD CONTENTS = ADDRESS
000150 020402 CMP R4, R2 ; AT END OF TEST?
000154 103774 BLO 2$ ;
000158 024404 CHKADP CMP -(R4), R4 ; CHECK BACK DOWN TO START ADDR
00015C 001400 BEQ NCKADP ; DATA READ IN ERROR IN RO
000160 000000 HALT ; STUCK BIT IN DATA OR ADDRESS!!
000164 020401 NCKADP CMP R4, R1 ; STUCK BIT POINTING TO ERROR LOCO OR
000168 101372 BHI CHKADP ; 2 BEYOND ; RO
00016C 005124 CHKCOM MOV (R4)+ ; MAKE LOC = ADDR COMPLEMENT
000170 020402 CMP R4, R2 ; AT END OF TEST?
000174 103775 BLO SETCOM ;
000178 010104 MOV R1, R4 ; START AT BEGINNING
00017C 060414 CHKCOM ADD R4, (R4) ; SHOULD BE ALL 1's
000180 012400 MOV (R4)+, R0 ; DATA SHOULD = ALL ZEROS
000184 001401 BEQ NCKCOM ;
000188 000000 HALT ; STUCK DATA BIT IF NO HALT AT +15b
00018C 020402 NCKCOM CMP R4, R2 ;
000190 103771 BLO CHKCOM

SETUP TO LEAVE A PATTERN OF 1 011 001 110 001 111 1 B ROTATED
RIGHT INTO 4 SUCCESSIVE WORDS
USED AS MEM BACKGROUND AND FILLE-EMPTY DATA

000212 010104 MOV R1, R4 ; SET INITIAL ADDRESS
000214 012703 SETPAT. MOV #131617, R3 ; SET INITIAL PATTERN
000218 020402 2$: CMP R4, R2 ; END OF ADDRESS RANGE?
00021C 103004 BHI CHKPAT ; GO CHECK DATA IF AT END
000220 010324 MOV R3, (R4)+ ; CARRY SET BY CMP INSTRUCTION
000224 105214 INC (R4) ; ROTATE AND LOAD AGAIN
000228 012400 ASR R3 ;
00022C 103773 BCS 4$ ;
000230 000770 BR SETPAT
000234 010104 CHKPAT: MOV R1, R4 ; SET INITIAL ADDRESS
000238 012703 CHKPTL: MOV #131617, R3
00023C 131617
000240 020324 3$: CMP R3, (R4)+ ; DATA OK?
000244 001403 BEQ 4$ ;
000248 016400 MOV -(R4), R0 ; SET DATA READ FOR LOOKING
00024C 000000 HALT ; PATTERN SENSITIVITY ERROR
000250 020402 4$: CMP R4, R2 ; AT END OF ADDRESS RANGE?
000254 105203 ASR R3 ;
000258 006203 BCS 3$ ; CARRY SET BY CMP INSTRUCTION
00025C 000764 BR CHKPTL

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LSI-11 VERSION

000266 000205 FILEXT RTS R5
DSD 440 BOOTSTRAP PROM MACRO M1113 15-SEP-80 11:25 PAGE 3
LSI-II VERSION

, FILL - EMPTY BUFFER TEST

000320 012504 FILEMP. MOV /R5+, R4 / GET BUFFER ADDRESS
000322 001777 BEQ FILET1
000324 00404 TST 404(R4) / DOES MEMORY EXIST?
000330 103777 BCS FILEEMP / NO - STEP TO END OF LIST
000332 000300 FILBUF. CLR RO
000334 011001 MOV (R0), XCS / GET RXCS ADDR
000336 010102 MOV XCS, XDB / INIT FOR RXDB
000338 000476 CALL WTFLAG / WAIT FOR DONE FLAG UP
00033A 000452 FILET1
000340 103777 BCS / LOOP IF NO BUS RESPONSE
000342 001775 BIT #ERR! DBDMA. (R1) / ERROR SET OR RX02?
000344 001417 BPL +4 / HALT IF ERROR
000346 000000 BEQ RXFIEM / IF RX01 MODE THEN NO LATCH TEST
000348 001417 BEQ RXFIEM / IF RX02 INTERFACE LATCHED/BIT TEST
00034A 012722 MOV #1420, (XDB)+ / LOAD INTO RXCS
00034C 002711 CMP #5460, (XCS) / DID THEY LATCH OK?
000350 005764 MOV 000000
000352 001401 BEQ +4 / STUCK BITS IN RXCS
000354 000300 CMP #1420, (XDB) / LATCHED OR IN RXDB?
000356 012737 MOV 1173767, (XOS) / RXHALT
000358 001420 BNE RXHALT / NO - BAD INTERFACE.
00035A 012712 RXDBTS. MOV #173767, (XDB) / CHECK RXDB LATCH
00035C 002712 CMP #173767, (XDB) / DID THEY LATCH
00035E 001401 BEQ +4 / RXHALT:
000360 000000 RXHalt: HLT / HALT IF INCORRECT BIT LATCHUP
000362 012746 MOV #200, -(SP) / SAVE THE WORD-COUNT
000364 012752 MOV #401, (XDB)+ / DO FILL COMMAND
000366 000000 RXFIEM: MOV XCS, XDB / Set up RXDB Pointer
000368 012776 MOV #200, -(SP) / Save the Word-Count
00036A 002711 TSTB (XCS) / Wait for TRREG
00036C 010376 BPL -2 / RX02 Style Fill?
00036E 004000 000400
000370 012746 MOV #401, (XDB)+ / Do Fill Command
000372 000000 RXFIEM: MOV XCS, XDB / Set up RXDB Pointer
000374 012752 MOV #200, -(SP) / Save the Word-Count
000376 010377 TSTB (XCS) / Wait for TRREG
000378 000376 BPL -2 / RX02 Style Fill?
00037A 001401 BEQ FILEX1 / NO - Do RX01 Style Prog Xfer
00037C 011001 MOV (SP), XCS / Wordcount (+200)
00037E 010377 TSTB (XCS) / Wait for TRREG
000380 000376 BPL -2 / RX02 Style Fill?
000382 010412 MOV R4, (XDB) / Buffer Addr
000384 004767 CALL WTFLAG / Wait for Done, Error, or TRREG
000386 000314 FILEX1
000388 010571 TSTB (R1) / Check for TRREG on RX01
00038A 012746 RXHalt: HLT / RX02 Style Fill?
00038C 000000 RXFIEM: MOV XCS, XDB / Set up RXDB Pointer
00038E 010571 TSTB (R1) / Check for TRREG on RX01
000390 012716 MOV #100, (SP) / Single Density RX01 Count
000440 000770  BR  FILEX1  ; CHECK FOR ANOTHER BYTE

; NOW EMPTY SECTOR BUFFER AND CHECK DATA VALIDITY

000442 022424  EMPBFT:  CMP  (R4)+, (R4)+  ; BUMP EMPTY BUFFER ADDR
000444 012711  MOV  #403, (XCS)  ; DO ERROR IF NO DATA TRANSFER
000450 010403  MOV  R4, R3  ; SAVE BUFFER START ADDRESS
000452 100376  TSTB  (XCS)  ; WAIT FOR TRREQ
000454 032711  BPL  -2  ; DO EMPTY BUFFER COMMAND
000456 004000  BIT  BBDMA, (XCS)  ; IS IT IN RX02 MODE?

000462 001404  BEQ  EMPX01  ; NO - DO RX01 STYLE EMPTY
000464 011612  MOV  (SP), (XDB)  ; LOAD WORD COUNT
000466 100376  TSTB  (XCS)  ; WAIT FOR TRREQ
000470 100376  BPL  -2  ; AND FILL BUFFER ADDR+2
000472 010412  MOV  R4, (XDB)  ; WAIT FOR ERROR, DONE OR TRREQ
000474 004767  EMPX01:  CALL  WTFLAG  ; TRREQ FROM RX01 TYPE EMPTY?
000500 000242  TSTB  (XCS)  ; NO - CHECK DATA
000502 100002  BPL  CHKEMP  ; LOAD THROUGH DATA POINTER
000504 111223  MOVB  (XDB), (R3)+
000506 004567  EMPX01  ; MAKE WORD COUNT INTO BYTE COUNT

000510 006316  CHKEMP.  ASL  (SP)  ; SET R2 = END ADDR TO CHECK
000512 010402  MOV  R4, R2
000514 062602  ADD  (SP)+, R2
000516 177514  JSR  R5, CHKPTL  ; DO DATA CHECK
000522 000662  BR  FILEMP  ; DO NEXT FILL-EMPTY
DSD 440 Bootstrap PROM

MACRO M1113 15-SEP-80 11 25 PAGE 4

LBA-11 VERSION

: Boot the device in loc 0, registers used as indicated below

; RO  UNIT # BOO TED FROM (0, 1)
000001 XCS= X1 ; R1  POINTER TO RXCS
000002 XDB= X2 ; R2  POINTER TO RXDB
000004 LDP= X4 ; R4  LOAD POINTER
000005 SCT= X5 ; R5  CURRENT SECTOR # (1, 2, 3, 5, 7)
; (SP) WORD COUNT FOR CURRENT DENSITY

000524 005000 BDT440 CLR MOV (R0), R1  ; SET INITIAL UNIT (0, 1, 2, 3)
000526 011001 MOV (R0), R1  ; SET RXCS POINTER
000530 004001 BR BDT440  ; ALLOW SAME UNIT

000532 005200 NXTUNT INC R0  ; BUMP DRIVE #
000534 011704 BDT440 MOV (R0), R1  ; INIT STACK POINTER
000536 005004 CLR LDP  ; INIT LOAD ADDRESS POINTER
000540 000500 BIC #RDTRB-UNTDEC. R0  ; ALWAYS INSURE VALID UNIT #
000544 004367 JSR R3, UNTDEC  ; GEN A POINTER INTO RDTBL
000550 000002 RDTBL, .BYTE 7, 27 : 47, 67  ; READ SECTOR FUNC FOR DRIVE 0, 1
000552 000003 UNTDEC ADD R0, R3  ; POINTER TO READ COMMAND
000554 111303 MOV R3, R3  ; GET THE COMMAND
000556 012746 MOV #100. -(SP)  ; SET LOW DENSITY WORDCOUNT
000560 001000

000562 001000 MOV #1, SCT  ; INIT SECTOR TO READ
000566 004767 RDTLP. CALL WFLAG  ; WAIT FOR DONE FLAG SET?
000572 001002 MOV XCS, R2  ; COPY RXCS POINTER
000574 010322 MOV R3, (R2)+  ; LOAD READ COMMAND
000576 105711 TSTB (XCS)  ; WAIT FOR TRREQ
000580 100036 BPL  ; -2
000582 010912 MOV SET (XDB)  ; LOAD SECTOR
000584 105711 TSTB (XCS)  ; LOAD TRACK
000586 100036 BPL  ; -2
000588 010712 MOV #1. (XDB)  ; SET TO D.D. WORD COUNT
000590 000001

000592 000120 CALL WFLAG  ; WAIT FOR DONE
000594 000120 TST (XCS)  ; CLUDGE SINCE DEC RX02 SETS ERROR
000596 000010 BPL EMPBUF  ; EMPTY IF NO ERROR
000598 000020 BIT #20. (XDB)  ; IS ERROR A DENSITY ERROR?
00059A 001450 BEQ DEFINST  ; NO- DO DEFINITIVE STATUS
00059C 002503 BIS #400. R3  ; SET COMMAND TO DOUBLE DENSITY
00059E 000400

000600 000000 MOV #200. (SP)  ; SET TO D.D. WORD COUNT
000602 000755 BR RDTLP  ; AND TRY READING AGAIN

000604 010346 EMPBUF. MOV R3, -(SP)  ; GET COMMAND COPY
000606 040716 BIC #4, (SP)  ; MAKE INTO AN EMPTY BUFFER COMMAND

000608 000004
LSI-11 VERSION

001000      BOTLST
000000      END      BOT170

000000      END

To boot try to boot on other drive.
DSD 440 BOOTSTRAP PHOM MACHU M1113 15-SEP-80 11 25 PAGE 4-3

**SYMBOL TABLE**

<table>
<thead>
<tr>
<th>BootStrap</th>
<th>0000534R</th>
<th>002 EMPBUF</th>
<th>0000644R</th>
<th>002 RXDB = 177172</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0T0M</td>
<td>0000534R</td>
<td>002 EMPD0N</td>
<td>0000714R</td>
<td>002 RXD0BIS = 000352R</td>
</tr>
<tr>
<td>B0T10M</td>
<td>0000040R</td>
<td>002 EMPX01</td>
<td>0000474R</td>
<td>002 RXFEM = 000436R</td>
</tr>
<tr>
<td>B0T11M</td>
<td>001000RQ</td>
<td>002 F1LBUF</td>
<td>0000302R</td>
<td>002 RXHALT = 000364R</td>
</tr>
<tr>
<td>B0T12M</td>
<td>000020RQ</td>
<td>002 FILEMP</td>
<td>0000270R</td>
<td>002 SCT = 00000003</td>
</tr>
<tr>
<td>B0T13M</td>
<td>000000RQ</td>
<td>002 FILEXT</td>
<td>0000266R</td>
<td>002 S0TCM = 000164R</td>
</tr>
<tr>
<td>B0T14M</td>
<td>000524R</td>
<td>002 FILEX01</td>
<td>0000432R</td>
<td>002 SETPAT = 000214R</td>
</tr>
<tr>
<td>C0M1</td>
<td>000150R</td>
<td>002 LD0P = 0000004</td>
<td>TRAP4 = 000053R</td>
<td></td>
</tr>
<tr>
<td>C0M2</td>
<td>000174R</td>
<td>002 MEMCHA = 000136R</td>
<td>UND0CE = 000565R</td>
<td></td>
</tr>
<tr>
<td>C0M6</td>
<td>000610R</td>
<td>002 MEMORA = 00064R</td>
<td>WIE0MDN = 000675R</td>
<td></td>
</tr>
<tr>
<td>C0M7</td>
<td>000234R</td>
<td>002 NCKADP</td>
<td>0000160R</td>
<td>002 WIEQLA0 = 000745R</td>
</tr>
<tr>
<td>C0M8</td>
<td>000536R</td>
<td>002 NCKCOM</td>
<td>0000306R</td>
<td>002 WIEQXS = 0000001</td>
</tr>
<tr>
<td>C0M9</td>
<td>000732R</td>
<td>002 N0TKNT</td>
<td>0000532R</td>
<td>002 XDB = 0000002</td>
</tr>
<tr>
<td>D0F0ST</td>
<td>000752R</td>
<td>002 RD0P</td>
<td>0000566R</td>
<td>002 DBRMA = 004000</td>
</tr>
<tr>
<td>D0FNT</td>
<td>000754R</td>
<td>002 R0TBL</td>
<td>0000550R</td>
<td>002 ERR = 000000</td>
</tr>
<tr>
<td>EMPF0T</td>
<td>000442R</td>
<td>002 RX0BL</td>
<td>177170</td>
<td></td>
</tr>
</tbody>
</table>

| ABS.      | 000000  | 000 |
| B0OT      | 001000  | 001 |

**ERRORS DETECTED:** 0

**VIRTUAL MEMORY USED:** 321 WORDS (2 PAGES)
**DYNAMIC MEMORY USED:** 2922 WORDS (10 PAGES)
**ELAPSED TIME:** 00:00:09

D0T440/DS: GBL, D0T440/N0SF= D0T440 MAC

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APPENDIX E

Controller Error Code Descriptions
and Causes
ERROR CODE DESCRIPTIONS AND CAUSES

Error Code: 010

Drive 0 failed to home on INIT

Possible Causes:

- No Drive 0 in system.
- Bad track 0 sensor. This is especially possible if noise is noted during drive stepping operation and if the head is at the outside of the diskette.
- Drive electronics could be incorrectly jumpered causing the stepper motor to be actuated by the Headload Signal instead of the drive select signal. (HL is jumpered instead of DS.)

Check Next:

- Drive 0 jumpers.
- Track 00 sensor on Drive 0.
- Drive flash indicating the error. (If not then the system could consist of two Drive 1's.)

Error Code: 020

Drive 1 failed to home on INIT. (Track 0 not found while head was stepping out.)

Possible Causes:

- No Drive 1 in system when the configuration switch is set for a 2 drive system.
- Bad track 0 sensor (open) on Drive 1.
- Two Drive 0's.
- Stepper motor failure.

Check Next:

- Head position on Drive 1. If the head is at the outside of the diskette and noise accompanies the stepping operation, then the track 00 sensor probably failed on Drive 1.
- If both drive activity lights flash together then there are probably two drive 0's.
• Check if there is a Drive 1. (This could be a single drive system with the controller module set for a two-drive system.)

Error Code: 030

Track 0 found while stepping in on INIT. (This can happen on either Drive 0 or Drive 1.)

Possible Causes:

• Track 00 sensor is shorted.
• The STEP-IN L line is stuck-at-low.
• The drive could have been out beyond track zero during INIT.
• Drive is wired incorrectly so that "headload" enables the stepper instead of "drive select".
• Drive cable is installed backwards.
• Stepper motor failure.

Check Next:

• Drive flash indicating INIT error.
• Drive signal STEPIN L is shorted.
• Check if drive was at negative track and try the INIT operation again.
• Check jumpers on drive electronics.
• If the drive cable is backwards then both drives would have heads loaded and activity lights would be on.

Error Code: 040

Invalid drive or track address specified.

Possible Causes:

• Software operation requesting Drive 1 in a one-drive system.
• DIP-Switch on the controller/formatter module set incorrectly.
• There is a software error.

Check Next:

• Immediately after the error, use the "Extended Status Dump" command (#7) to find the requested drive and track.
Error Code: 050
Track 0 encountered unexpectedly.

Possible Causes:
- This could be a problem in the controller module but it must be intermittent. Normally, the controller would find 30 error on INIT.
- Stepper failure (over step outwards toward track 0).
- Direction line failed.

Check Next:
- This is a rare failure which implies a seek problem.

Error Code: 070
Requested sector not found in two revolutions.

Possible Causes:
- Desired ID sector has a hard CRC error.
- Improperly formatted diskette (missing sector requested).
- R/WC time out while looking for a byte in header (controller failure).

Check Next:
- Check if a bad diskette is inserted in the system.
- Check if the drive is generating bad diskettes because of excessive wear.

Error Code: 075
Too many bad headers on what was thought to be IBM 2D diskette.

Possible Causes:
- One track bad on diskette.
- Incorrect format.

Try Next:
- Reformat track(s) which appear to be bad.
**Error Code: 100**

Write-protect violation (attempt to write on write-protected diskette).

Possible Causes:

- Error occurs during write, format or set media density commands.
- Diskette write-protect tab is missing.
- Diskette write-protect tab is not an opaque sticker.
- Shorted write-protect sensor.
- Format operation attempted on a drive not containing a diskette. (This could not occur during normal write on the missing diskette because a 260 error would occur first.)

Check Next:

- Write-protect tab.
- Write-protect sensor on related disk drive.

**Error Code: 110**

Drive read signal lost (48 microseconds elapsed with no read pulses from the drive).

Possible Causes:

- Head load problem (headload solenoid).
- Weak head load solenoid.
- Defective component installed in the drive electronics.
- Bad negative supply. (This is only used for analog read circuits.)
- Head is trying to read on non-existent Drive 1.
- Drive electronics could be jumpered incorrectly (headload select).
- The L jumper may be inserted on the drive resulting in a shorted regulator on the drive electronics board.

Check Next:

- Check if head is loaded.
- Check the negative power supply at the drive.
- Check that Drive 1 is jumpered correctly by using the INIT cycle.
• Check the jumpering on the drive electronics.

Error Code: 120

No preamble found (R/W Controller could not identify preamble-independent of phase-lock loop).

Possible Causes:
  • Damaged media (track erased)
  • Drive pulley size is incorrect.
  • Read signal is weak or fading.

Check Next:
  • Check if DSD 480 RX2ES indicates the drive is ready.
  • Check drive read signal strengths.

Error Code: 130

Preamble found but no IDAM within window (preamble seems to continue forever).

Possible Causes:
  • Down-level microcode on DSD 480 cannot find IDAM.
  • Diskette is misformatted.
  • Although mark not found, read/write controller and PLL were able to continue finding valid preamble so that circuitry must be OK.

Check Next:
  • Use FRD480 or scan "Hyperdiagnostic" to verify that error occurs on multiple tracks.
  • Check another diskette.

Error Code: 140

CRC error on what appeared to be a header (This error code is not accompanied by the error flag in the RXCS).

Possible Causes:
  • Head-load problem has occurred. This includes head bounce problems as well as more common head-load problems.
- This error can only show-up in the "non-0" error status print-out of FRD480 as it does not generate an error abort.
- Suspected header is internally inconsistent with it's CRC.

**Error Code: 150**

Track or head in good header did not match expected. (The CRC code on the ID sector field was correct; the track or head within the ID sector field did not match expected value.)

Possible Causes:
- Bad drive exists.
- Stepper motor is malfunctioning.
- Bad head guide shaft bearing exists.
- A step circuit on drive PCB is defective.
- Invalid diskette format.

Check Next:
- Use seek test on FRD480.
- Use butterfly seek test in "HYPERDIAGNOSTICS".

**Error Code: 160**

Too many tries for an IDAM. (Can find a preamble so R/WC is OK but overflows bad IDAM counter.)

Possible Causes:
- Phase-lock loop has problem in controller.
- Read channel in drive is weak.

Check Next:
- Use good diskette in drive under test to check drive signal amplitude.
- Check DSD 480 controller with PLL "HYPERDIAGNOSTIC" test.

**Error Code: 170**

Preamble found but no Data Address Mark followed. (Correct ID sector found, valid data preamble found, but no DAM followed.)
Possible Causes:
- Diskette is miswritten.
- Damaged media.

Check Next:
- Verify read operation on DSD 480 using good diskettes.

Error Code: 175
DEC double density address mark found on a diskette with 15 or 8 sectors per track (diskette is not DEC or IBM compatible).

Possible Causes:
- Set media attempted on an IBM single density diskette which was not DEC compatible.

Check Next:
- Try known good diskette and/or reformat bad diskette.

Error Code: 200
Data CRC error

Possible Causes:
- Diskette is defective.
- Read head in drive is weak.
- Read channel on drive PCB is weak.
- Electrical interference (EMI) is occurring.
- Diskette is contaminated with airborne particles.

Check Next:
- See if error was hard or soft, depending if in FRD480 the error occurred once or twice.
- Attempt to read diskette on a different drive to check drive alignment problem (possibly diskette was read or written misaligned).
- Examine diskette for signs of damage and wear from head load pad.
- Note that 200 errors are generally permitted intermittent in nature. They can be caused by a variety of unpredictable events including lightning and power glitches.

E-7
Error Code: 210
Parity error on interface cable.

Possible Causes:

- Electro-magnetic interference is occurring.
- Interface to controller cable is wearing out or is near AC power lines.
- Interface board is defective.
- Controller board is defective.

Check Next:

- Check if parity error occurs often. If not, it is most likely a result of sporadic interference.
- Use extended self-test to trouble-shoot DSD 480 controller.

Error Code: 220
Read/write controller self-test failure (unexpected R/WC error).

Possible Causes:

- DSD 480 board has a hardware problem. Under no conditions should R/WC interrupt 8085 with error code equal 0.

Check Next:

- Check interrupt circuit on DSD 480 controller board.

Error Code: 230 (Only valid in Mode 2)
Invalid word count specified

Possible Causes:

- This code results from a programming error.

Check Next:

- Immediately use Extended Status Dump to determine diskette media density and requested word count.

Error Code: 235 (IBM Mode only)
Word count error during "fill buffer" or "empty buffer" in IBM mode. (Word count greater than limit set by density of command.)
NOTE

This error code may be used to identify that system is in "IBM Mode" by checking the error code after a word count that is greater than 100

If error code = 230 then system is RX01 or RX02 mode.

If error code = 235 then system is in IBM mode.

Possible Causes:

- Word count greater than 100 if double density bit set (=1), or word count greater than 400 if single density (density bit = 0 in RXCS).

Check Next:

- Use IBM "status test" to get word count and check validity.
- Try doing fill or empty buffer in RX02 Mode.

Error Code: 240

Density error (density mismatch)

Possible Causes:

- This is a normal occurrence in system software.
- Write gate or other write circuit on disk drive failed.

Check Next:

- Check to see if alternate drive will execute software properly. May be a write circuit problem.
- Note that 240 error does not cause flashing of activity LEDs as 240 error is common occurrence.

Error Code: 245

Density error on an IBM 2D (double density) diskette.

Possible Causes:

- Wrong command density used for density of disk (e.g. density bit cleared). When IBM 2D diskette is referenced on tracks 1 to 76.
- Track 0, side 0 of IBM 2D diskette not referenced with single density command.
- Disk with mixed formats being used.
Check Next:
- Try read on cylinder 1 to 76 with the density bit = 1.
- Read on cylinder #0, side #0 with density bit = 0.
- Try to reformat bad track(s) to correct density/sector length.

Error Code: 250
Wrong key word for Set Media Density
Possible Cause:
- Set Media Density command has programming error.

Error Code: 255
Wrong sector identifier used during read or write.
Possible Causes:
- Disk has been changed to new format and handler has not updated sector size bits (Bits 7:6 of RXISA).

Check Next:
- Use correct "sector size bits."

Error Code: 260
Indeterminate density (system was unable to determine density of selected diskette).
Possible Causes:
- Any read error while checking density could cause 260 error. If read signal is lost 110 error could occur instead.
- Diskette has bad data, possibly caused by drive write problem.
- Two Drive 0's exist, both of which have diskettes inserted.
- Selected drive has head-load problem.

Check Next:
- Check if diskette is readable on alternate drive.
- Check if system INITs properly, and if there are two Drive 0's.
Check if head loads at all.

Check for headload problem on DSD 480 controller module.

**Error Code: 265**

Tried to use a diskette with other than 26 sector/track in RX01 or RX02 compatible mode. (Diskette recognizes but it is incorrect for selected mode.)

Possible Causes:
- RX01 or RX02 mode selected when IBM mode desired.
- Wrong type disk is being used.

Check Next:
- Use 26 sector/track diskette in RX01 and RX02 mode.
- Insure both switch #4 and #7 set to proper positions.

**Error Code: 270**

R/WC write format failure (time-out waiting for index mark at beginning of format operation or at end of format operation).

Diskette must be in system as earlier index pulse was required to get past 360 error time-out.

Possible Causes:
- Disk is spinning too slowly, caused by 60 Hz pulleys on drive powered by 50 Hz AC.

Check Next:
- Use Read Status Command to see if selected diskette is spinning at correct speed.

**Error Code: 320**

Read/write controller write failure (R/WC time-out failure during write or format).

Possible Causes:
- DSD 480 controller has failed.

Check Next:
- Use extended self test or SA 4 to check hand shake between 8085 and R/WC.
• This error indicates that a read/write controller command took much longer
than it normally should have.

**Error Code: 330**

Read/write controller time-out on reset (R/WC did not return ready after INIT).

Possible Causes:
• Drive motor is dragging.
• The DSD 480 board has a hardware problem.
• Line frequency incorrect

Check Next:
• Check R/WC and 8085 handshake using extended self-test or SA 4.

**Error Code: 340**

Master controller out of sync with R/WC on controller module.

Possible Causes:
• 4440 hardware failure has occurred.

Check Next:
• Check R/WC to 8085 handshake using extended self-test or SA 4.

**Error Code: 350**

Non-existent memory error during DMA (after DMA error occurs system is locked-up and
it is impossible to retrieve this error code).

Possible Causes:
• Interface board (bus address register) is bad.
• A programming error exists (invalid buffer address specified).
• Memory board has failed.

Check Next:
• Use hardware bootstrap to execute RAM test in host computer memory.
• Try booting in RX01 mode in order to avoid use of DMA circuit. This pins
problems down to DMA circuit and Q-bus or UNIBUS.
Error Code:  360

Drive not ready during format command (error indicates missing index pulse at beginning of format command).

Possible Causes.

- Diskette is not spinning or spinning too slow (60 Hz pulley, 50 Hz power).
- 800 jumper is missing on drive

Check Next:

- Use Read Status to check to see if selected drive is spinning at correct speed.
- Verify selected drive, being Drive 0, can use INIT operation to check if drive is ready. If ready, read will occur on drive 0. If not ready, read will not occur on drive 0.

Error Code:  370

AC power caused abort of write activity

Possible Causes:

- Power OK is sensed before write operation or format operation. If AC power is not OK at that point the write operation is aborted. Since the AC power-low detect circuit is not stuffed in a normal controller board this error should never occur.

Check Next:

- Check primary AC power if AC detect circuit is stuffed on the 4440 board.
APPENDIX F

Implementation of Double Sided Support For The DSD 480
DOUBLE SIDED SUPPORT UNDER RT-II

Double sided support under RT-II V3B may be "activated" by one of two methods. DSD supplies a software device handler which is equivalent to the DEC device handler with appropriate flags and conditionals enabled for doubled sided support. This handler may be assembled into the RT-II DY monitor (FB or SJ) by following the system generation procedure as supported by DEC. Alternately, to save the effort required to perform a "sys gen", DSD supplies a command file which will automatically patch the RT-II V3B monitor to activate the two sided features.

If the user elects to perform a sys gen, the DSD handler DYDSD.MAC (found on the DSD diagnostic diskette) must first be renamed to DY.MAC and substituted for the MACRO-II source file, DY.MAC provided by DEC. The DSD handler, containing double sided support may then be installed into the RT-II monitor by following the procedure described in the RT-II System Generation Manual supplied by DEC.

DOUBLE SIDED SUPPORT UNDER RSX-II M

The DSD 480 diagnostic diskette contains an SLP (source language patch) program which will implement double sided support in the RSX-II M V3.2 monitor. The DEC RSX-II M release package provides instructions for installing SLP programs into the operating system.

THE DSD MONITOR PATCH PROGRAM FOR RT-II

The Monitor Patch Program takes a DYMNSJ or DYMNFB monitor from the DEC RT-II V3B system distribution and replaces the DY handler currently in the distribution monitor with a double sided DY handler. The new monitor has the same characteristics as the original monitor, such as batch support, 60 Hz line time clock, all handlers supported by the distribution monitor, and no error logging.

The monitor patch program would be used under the following conditions:

1) The distribution RT-II V3B monitor provided by DEC is sufficient for the user's normal applications. Except for not having double sided support.

2) The user does not wish to perform a System Generation.

3) The user has not changed the normal distribution monitor with customized patches, relating to the user's system.

If these conditions are not met, a System Generation may be required.

The DYMNSJ or DYMNFB monitor may be generated from the first or second release of RT-II V3B. The distribution DYMNSJ or DYMNFB monitor that will be modified can be found on the distribution diskette shown below:
<table>
<thead>
<tr>
<th>First DX KIT Release of RT-II V3B</th>
<th>Disk Label No.</th>
<th>Dated</th>
</tr>
</thead>
<tbody>
<tr>
<td>DYMNSJ. SYS</td>
<td>AS-5781B-BC</td>
<td>11 March 78</td>
</tr>
<tr>
<td>DYMNF. SYS</td>
<td>AS-5781B-BC</td>
<td>11 March 78</td>
</tr>
<tr>
<td>Second DX KIT Release of RT-II V3B</td>
<td>Disk Label No.</td>
<td>Dated</td>
</tr>
<tr>
<td>DYMNSJ. SYS</td>
<td>AS-5783C-BC</td>
<td>27 March 79</td>
</tr>
<tr>
<td>DYMNF. SYS</td>
<td>AS-5783C-BC</td>
<td>27 March 79</td>
</tr>
</tbody>
</table>

or either DY KIT release may be used.

To use the DSD Monitor Patch Program, the following are required:

1) A minimal DY-bootable system diskette with the following files:

   - SWAP. SYS
   - DYMNSJ. SYS from the RT-II
   - DYMNF. SYS distribution diskette
   - DIR. SAV
   - PIP. SAV
   - DUP. SAV
   - FORMAT. SAV
   - TT. SYS
   - EDIT. SAV
   - DUMP. SAV

   **NOTE**
   - This diskette must have a minimum of 100 free blocks and may be either single or double density.
   - Be sure to copy the bootstrap onto the diskette using the COPY/BOOT command.
   - The monitors used on this system diskette will be patched and placed on another diskette.
   - Copy the files from the distribution disk. Don't use the originals.

2) A blank/initialized (zeroed directory) diskette.

3) The DSD Diagnostic Diskette with the required DSD patch files.
The actual patch process is accomplished as follows:

1) Insert the system diskette into drive DYO (drive 0).

2) Insert the DSD Diagnostic Diskette into drive DYI (drive 1). Leave Diagnostic Disk write protected to insure no errors.

3) Boot the DYO system diskette in drive 0.

4) Run the indirect command file PATSET.COM on DYI.
   To run the indirect command file, type:
   
   @DYI:PATSET
   
   This indirect command file will copy the required patch program pieces onto the system diskette in drive 0 (DYO).

5) Remove the DSD Diagnostic Diskette from DYI (drive 1).

6) Insert the blank/initialized diskette into DYI (drive 1).

7) To create a DYMNSJ.SYS monitor with double sided support, type:
   
   @DYO:PATSJ
   
   To create a DYMNFB.SYS monitor with double sided support, type:
   
   @DYO:PATFB
   
   These indirect files will create a new system monitor (DYMNSJ or DYMNFB) on drive I, then will copy the necessary support files from DYO to DYI, and then will boot the system diskette in DYI. This diskette can then be modified as desired and used as the new master for double sided monitors.