

IDENTIFICATION

Product Code:	MAINDEC 15-D1A0-D (D)
Product Name:	PDP-15 Basic Memory Checkerboard (Low and High Versions)
Date Created:	October 22, 1969
Maintainer:	Diagnostics Group
Author:	J. W. Richardson



COPYRIGHT © 1969
DIGITAL EQUIPMENT CORPORATION

1. ABSTRACT

The PDP-15 Basic Memory Checkerboard programs test 3D core memories for failure on half-selected lines under worst case noise conditions. Their use is intended for 4K systems. Either program will loop until stopped by the operator, or an error is detected.

2. REQUIREMENTS

Equipment

A standard PDP-15.

Storage

There are two versions of this MAINDEC. The Low End program occupies memory locations 200 to 506, and tests memory from 1000 to 7777 octal. The High End program occupies locations 7400 to 7674, and tests memory from 0000 to 7377 octal.

3. LOADING PROCEDURE

The loading procedure is identical for either program.

- a. Place the tape in the reader.
- b. Place the BANK MODE switch on a 1.
- c. Set the ADDRESS switches to 17700.
- d. Press I/O RESET, and then READ-IN.

4. STARTING PROCEDURE

- a. 200 is the starting address for the Low End program.
- b. 7400 is the starting address for the High End program.
- c. The AC switches do not effect the normal operation of the program. However, they may be used to suppress error halts. See section 6.

5.

PROGRAM DESCRIPTION

The program tests memory using four different patterns. Three of the patterns are variations of a checkerboard type, plus the complement of each, making a total of six. The fourth pattern is included to test the effects of prolonged reading of a memory location that contains 000000 and all other intersecting addresses contain 777777. As an example, the program may write 777777 in every Y axis address from 0000 through 7300. The Y axis is addressed using bits 6 - 11. The program then deposits 000000 in address 0000 and then reads (LAC*) address 0000 1024 times. Each Y address intersecting X line 00 is then read and checked to make sure that each contains 777777. If a "weak" core is present, it may switch to the 0 state using this test method.

Shown below are the three checkerboard patterns and their complements as they would appear in a portion of one bit plane. Each pattern complements every 40 octal addresses. The X axis is addressed by MA bits 12 - 17, and the Y axis by bits 6 - 11.

Pattern 1: 463144

	Y axis		Y axis
	0 10011001		0 01100110
X axis	10011001	X axis	01100110
	⋮		⋮
	40 01100110		40 10011001

Pattern 2: 631460

	Y axis		Y axis
	0 11001100		0 00110011
X axis	11001100	X axis	00110011
	⋮		⋮
	40 00110011		40 11001100

Pattern 3: 525250

	Y axis		Y axis
	0 10101010		0 01010101
X axis	10101010	X axis	01010101
	⋮		⋮
	40 01010101		40 10101010

The control words used to generate the patterns are:

Pattern 1: 463144 and 314633

Pattern 2: 631460 and 146317

Pattern 3: 525250 and 252527

6. ERROR HALTS

Listed below are the six possible halts which may occur. Halts E1 through E4 apply to the memory checkerboard tests (patterns 1, 2 and 3), and E5 and E6 are used for the fourth pattern (tagged BURST on the program listing).

Two addresses are given for each halt; the first is for the Low End test and the second for the High End test.

<u>C (MO)</u>	<u>Tag</u>	<u>Description</u>
362 7557	E1	A memory location does not contain 777777 or 000000. The AC displays the address of the location in error. Press CONT for next halt.
364 7561	E2	The AC displays the contents of the location in error. Record the value and press CONT for the next halt.
366 7563	E3	The AC displays the data the location should have contained. Press CONT again.
370 7565	E4	The AC displays the control word used to generate the current checkerboard pattern. The value will equal 463144, 631460 or 525250 or their complements - 314633, 146317 or 252527. Press CONT resume testing with the next sequential memory location.
450 7643	E5	An error was detected during pattern 4. A memory location does not equal 777777. The AC displays the failing address. Bits 12 - 17 indicate the X axis address which contains 000000. Bits 6 - 11 indicate the Y axis address which should have contained 777777. Press CONT for the next halt.

<u>C (MO)</u>	<u>Tag</u>	<u>Description</u>
452 7645	E6	The AC displays the data read from the failing address. Press CONT to test the next sequential Y axis address.

Error Suppression

Further error halts for any bit position in the checkerboard tests (halts E1 - E4) may be suppressed by placing the corresponding AC switch on a 1 before pressing CONT after the last error halt (E4). An error halt will occur for any failing bit position whose corresponding AC switch is on a 0. Error halts for all bit positions may be restored by restarting from 200 (Low) or 7400 (High).

Any one of the six checkerboard patterns (3 plus complements) may be used exclusively by placing the correct control word in 3 locations (see error halt E4 above). For the Low End test these locations are 460, 461 and 462. For the High End test the locations are 7671, 7672 and 7673. Either set of 3 locations normally contain 463144, 631460 and 525250, respectively.

Error suppression for pattern 4 is not provided. To loop on any failing address do the following:

1. Manually DEPOSIT the failing address in the location tagged PATR on the listing.
2. Place a NOP 2 locations before the tag BUST (BUST -2).
3. Set the ADDRESS switches to the address of tag BRSTA. Press I/O RESET, and then START.

The location tagged PATR contains the failing address.

Location BUST -2 normally contains an ISZ PATWD.

7. EXECUTION TIME

Either program requires approximately 20 seconds to run all 7 patterns.

8. LISTING

.TITLE LOCK 15

/
 /PDP-15 BASIC 4K MEMORY CHECKERBOARD,
 /S.A.=200. (RESIDES IN LOW - TESTS HIGH)
 /
 /COPYRIGHT 1969 DIGITAL EQUIPMENT CORP.,
 /MAYNARD, MASS.
 /
 /J. RICHARDSON
 /

.ABS

00200			.LOC 200	
	/			
00200	777777	BEGIN	LAW	-1
00201	040453		DAC	BITSUP
00202	777775		LAW	-3
00203	040454		DAC	PATCNT
00204	200456		LAC	PATN
00205	040457		DAC	NXTPAT
	/			
00206	220457	CKLP	LAC*	NXTPAT
00207	040465		DAC	CNTRL
00210	100215		JMS	TEST
00211	440457		ISZ	NXTPAT
00212	440454		ISZ	PATCNT
00213	600206		JMP	CKLP
00214	600202		JMP	BEGIN+2
	/			
00215	000000	TEST	0	
00216	100263		JMS	WRITE
00217	200471		LAC	K1
00220	040470		DAC	BITCON
00221	100270		JMS	READ
00222	200470		LAC	BITCON
00223	744010		RCL	
00224	040470		DAC	BITCON
00225	740200		SZA	
00226	600221		JMP	TEST+4
00227	600374		JMP	RURST
00230	777774	COMP	LAW	-4
00231	260457		XOR*	NXTPAT
00232	540465		SAD	CNTRL
00233	620215		JMP*	TEST
00234	040465		DAC	CNTRL
00235	600216		JMP	TEST+1
	/			
	/GENERATE PATTERN			
	/			
00236	000000	GENPAT	0	
00237	200465		LAC	CNTRL
00240	040472		DAC	SVMSTR
00241	200501		LAC	(1000
00242	040473		DAC	SyADR
00243	771000		LAW	-7000
00244	040474		DAC	SVLTH

/CONTROL WORD COUNT
 /CONTROL WORD POINTER
 /GET A CONTROL WORD
 /SAVE
 /WRITE PATTERN AND TEST
 /INCREMENT POINTER
 /DONE ALL IF SKIP
 /DO NEXT PATTERN
 /START OVER
 /WRITE THE PATTERN
 /USED TO COMPLEMENT BITS
 /READ AND TEST
 /SETUP FOR NEXT BIT
 /TEST NEXT BIT POSITION
 /CHECK FOR LAST PATTERN
 /DID COMPLEMENT
 /WRITE COMPLEMENT
 /CURRENT PATTERN WORD
 /SAVE
 /ADDRESS COUNTER

```

00245 777714      LAC      =7?
00246 343466      DAC      CT24      /COUNTS 4 X 16 SHIFTS
00247 200472      LAC      SVMSTR      /CURRENT CONTROL WORD
00250 340475      DAC      PATR      /SAVE
00251 777762      WCNT      LAW      =2?
00252 340467      DAC      CT16      /COUNTS 16 SHIFTS
00253 200475      LAC      PATR      /CONTROL WORD
00254 744010      RCL
00255 340475      DAC      PATR
00256 751400      SZL:CLA
00257 740001      COMPL      CMA
00260 340455      DAC      PATWD      /WRITE 777777
00261 200455      LAC      PATWD
00262 620236      JMP*      GENPAT      /EXIT TO WRITE OR READ
/
00263 000000      WRITE      0
00264 100236      JMS      GENPAT      /GET A WORD
00265 360473      DAC*      SVADR      /WRITE
00266 100307      JMS      CKXY      /CHECK FOR PATTERN INVERSION
00267 620263      JMP*      WRITE
/
                /READ AND TEST
/
00270 000000      READ      0
00271 100236      JMS      GENPAT      /GET A WORD
00272 340477      DAC      GOOD      /SAVE
00273 200470      LAC      BITCON
00274 260473      XOR*      SVADR      /COMPLEMENT A BIT
00275 060473      DAC*      SVADR      /WRITE WITH INVERTED BIT
00276 200470      LAC      BITCON
00277 260473      XOR*      SVADR      /RE-COMPLEMENT
00300 060473      DAC*      SVADR      /RESTORE
00301 220473      LAC*      SVADR      /READ
00302 540477      SAD      GOOD      /COMPARE
00303 741000      SKP
00304 600343      JMP      ERROR      /O.K.
00305 100307      RTN      JMS      CKXY      /ERROR PATH
00306 620270      JMP*      READ      /CHECK FOR PATTERN INVERSION
                /EXIT
                /ROUTINE TO CHECK FOR PATTERN INVERSION
/
00307 000000      CKXY      0
00310 440474      ISZ      SVLTH      /DONE 4K IF SKIP
00311 741000      SKP
00312 620307      JMP*      CKXY      /EXIT TO WRITE OR READ
00313 440466      ISZ      CT04      /DONE WITH Y AXIS IF SKIP
00314 741000      SKP
00315 600324      JMP      Y64      /DONE 64 Y LINES
00316 200473      LAC      SVADR
00317 340500      V64      TAD      K100      /INCREMENT Y ADDRESS BY 1
00320 040473      DAC      SVADR
00321 440467      ISZ      CT16
00322 600253      JMP      WCNT+2      /CHECK FOR 16 LOCATIONS
00323 600247      JMP      WCNT      /NOT YET
                /RESTORE COUNT
/

```


00400	440473		ISZ	SVADR	
00401	200502		LAC	(10000	
00402	540473		SAD	SVADR	/DONE IT EQUAL
00403	741000		SKP		
00404	600376		JMP	WONS	
00405	200501		LAC	(1000	
00406	240473		DAC	SVADR	/1000 IS STARTING ADDR
00407	340500		TAD	K100	
00410	040473		DAC	PATR	/SAVES XY COORDINATE
00411	200475	BRSTA	LAC	PATR	
00412	040474		DAC	SVLTH	/Y LINE ADDRESS
00413	776000		LAW	-2000	/-512 DECIMAL
00414	040455		DAC	PATWD	
00415	160473		DZM*	SVADR	/CLEAR LINE XN
00416	220473		LAC*	SVADR	/READ 000000
00417	440455		ISZ	PATWD	/DISTURB LINE 512 TIMES
00420	600416		JMP	.-2	
00421	777777	BUST	LAW	-1	
00422	260474		XOR*	SVLTH	/DATA MUST BE 777777
00423	741200		SNA		/SHOULD NOT SKIP
00424	600430		JMP	CEND	/OK
00425	740001		CMA		
00426	040476		DAC	BAD	
00427	600446		JMP	-E5-1	/ERROR PATH
00430	200500	CEND	LAC	K100	
00431	340474		TAD	SVLTH	/Y AXIS PLUS 1
00432	040474		DAC	SVLTH	
00433	200502		LAC	(10000	
00434	500474		AND	SVLTH	
00435	540502		SAD	(10000	/DONE ALL Y FOR CURRENT X
00436	741000		SKP		/IF EQUAL
00437	600421		JMP	BUST	/READ NEXT Y ON CURRENT X
00440	440473		ISZ	SVADR	/INCREMENT X ADDRESS
00441	440475		ISZ	PATR	/INCREMENT X+Y ADDRESS
00442	200503		LAC	(1100	
00443	540473		SAD	SVADR	/DONE 63 X LINES IF EQUAL
00444	600230		JMP	COMP	/WRITE NEXT CHECKERBOARD
00445	600411		JMP	BRSTA	/TEST NEXT X WITH Y02
	/				/THRU Y63
00446	200474		LAC	SVLTH	
00447	740040	E5	HLT		/AC = FAILING X + Y63 LINE
00450	200476		LAC	BAD	
00451	740040	E6	HLT		/AC = BAD DATA
00452	600430		JMP	CEND	/READ ANOTHER
	/				
	/				/CONSTANTS AND STORAGE REGISTERS
	/				
00453	777777	BITSUP	LAW	-1	
00454	000000	PATCNT	0		
00455	000000	PATWD	0		
00456	000460	PATN	.-2		
00457	000460	NXTPAT	.-1		
00460	463144			463144	
00461	631460			631460	

00462	525250		525250
00463	000040	K40	40
00464	000077	K77	77
00465	000000	CNTRL	0
00466	000000	CT04	0
00467	000000	CT16	0
00470	000000	BITCON	0
00471	000001	K1	1
00472	000000	SYMSTR	0
00473	000000	SVADR	0
00474	000000	SVLTH	0
00475	000000	PATR	0
00476	000000	BAD	0
00477	000000	GOOD	0
00500	000100	K100	100
	/		
00001		.LOC	1
00001	600001	JMP	1
00002	777777	LAW	-1
00003	777777	LAW	-1
00004	777777	LAW	-1
00005	777777	LAW	-1
	000000	.END	
00501	001000	*L	
00502	010000	*L	
00503	001100	*L	

NO ERROR LINES

.TITLE CKH15

```

/
/PDP-15 BASIC 4K MEMORY CHECKERBOARD
/SA = 7400, (RESIDES IN HIGH - TESTS LOW)
/
/COPYRIGHT 1969, DIGITAL EQUIPMENT CORP.,
/MAYNARD, MASS.
/
/J. RICHARDSON
/

```

.ABS

```

00001          .LOC 1
/
00001 600001    JMP      1
00002 777777    LAW      -1
00003 777777    LAW      -1
00004 777777    LAW      -1
00005 777777    LAW      -1
/
00200          .LOC 200
/
00200 607400    JMP      BEGIN
/
07400          .LOC 7400
/
07400 777777    BEGIN    LAW      -1
07401 047657    DAC      BITSUP
07402 777775    LAW      -3
07403 047660    DAC      PATCNT    /CONTROL WORD COUNT
07404 207667    LAC      PATN      /CONTROL WORD POINTER
07405 047670    DAC      NXTPAT
/
07406 227670    CKLP     LAC*     NXTPAT    /GET A CONTROL WORD
07407 047662    DAC      CNTRL    /SAVE
07410 107415    JMS      TEST     /WRITE PATTERN AND TEST
07411 447670    ISZ     NXTPAT    /INCREMENT POINTER
07412 447660    ISZ     PATCNT    /DONE BOTH IF SKIP
07413 607406    JMP      CKLP     /DO NEXT PATTERN
07414 607402    JMP      BEGIN+2  /START OVER
/
07415 000000    TEST     0
07416 107462    JMS      WRITE    /WRITE THE PATTERN
07417 207655    LAC      K1
07420 047663    DAC      BITCON   /USED TO COMPLEMENT BITS
07421 107467    JMS      READ     /READ AND TEST
07422 207663    LAC      BITCON
07423 744010    RCL
07424 247663    DAC      BITCON   /SETUP FOR NEXT BIT
07425 740200    SZA
07426 607421    JMP      TEST+4    /TEST NEXT BIT POSITION
07427 607571    JMP      BURST    /TEST ALL X LINES WITH
/
07430 777774    COMP     LAW      -4    /Y LINE #61,
07431 267670    XOR*     NXTPAT    /CHECK FOR LAST PATTERN
07432 547662    SAD      CNTRL

```

```

07433 627415      JMP*   TEST      /HAVE DONE COMPLEMENT
07434 647662      DAC    CNTRL     /WRITE COMPLEMENT
07435 607416      JMP    TEST+1
/
/GENERATE PATTERN
/
07436 000000      GENPAT 0
07437 207662      LAC    CNTRL     /CURRENT CONTROL WORD
07440 047664      DAC    SVMSTR    /SAVE
07441 147665      DZM    SVADR     /ADDRESS COUNTER
07442 770400      LAW    -7400
07443 047666      DAC    SVLTH
07444 777704      LAW    -74
07445 047650      DAC    CT04      /COUNTS Y LINES
07446 207664      LAC    SVMSTR    /CURRENT CONTROL WORD
07447 047652      DAC    PATR      /SAVE
07450 777760      WCNT   LAW    -20
07451 047651      DAC    CT16      /COUNTS 16 SHIFTS
07452 207652      LAC    PATR      /CONTROL WORD
07453 744010      RCL
07454 047652      DAC    PATR
07455 751400      SZL:CLA
07456 740001      COMPL CMA
07457 047661      DAC    PATWD
07460 207661      LAC    PATWD
07461 627436      JMP*   GENPAT    /EXIT TO WRITE OR READ
/
07462 000000      WRITE 0
07463 107436      JMS    GENPAT    /GET A WORD
07464 067665      DAC*   SVADR     /WRITE
07465 107506      JMS    CKXY      /CHECK FOR PATTERN INVERSION
07466 627462      JMP*   WRITE     /DONE 7500 IF SKIP
/
/READ AND TEST
/
07467 000000      READ  0
07470 107436      JMS    GENPAT    /GET A WORD
07471 047654      DAC    GOOD      /SAVE
07472 207663      LAC    BITCON
07473 267665      XOR*   SVADR     /COMPLEMENT A BIT
07474 067665      DAC*   SVADR     /WRITE WITH INVERTED BIT
07475 207663      LAC    BITCON
07476 267665      XOR*   SVADR     /RE-COMPLEMENT
07477 067665      DAC*   SVADR     /RESTORE
07500 227665      LAC*   SVADR     /READ
07501 547654      SAD    GOOD      /COMPARE
07502 741000      SKP
07503 607540      JMP    ERROR    /OK
07504 107506      RTN   JMS    CKXY /ERROR PATH
07505 627467      JMP*   READ     /CHECK FOR PATTERN INVERSION
/EXIT
/
/ROUTINE TO CHECK FOR PATTERN INVERSION
/
07506 000000      CKXY  0
07507 447666      ISZ   SVLTH     /DONE 4K IF SKIP

```

07510	741000		SKP		
07511	627506		JMP*	CKXY	/EXIT TO WRITE OR READ
07512	447650		ISZ	CT04	/DONE WITH Y AXIS IF SKIP
07513	741000		SKP		
07514	607523		JMP	Y64	/DONE 64 Y LINES
07515	207665		LAC	SVADR	
07516	347656	N64	TAD	K100	/INCREMENT Y ADDRESS BY 1
07517	047665		DAC	SVADR	
07520	447651		ISZ	CT16	/CHECK FOR 16 LOCATIONS
07521	607452		JMP	WCNT+2	/NOT YET
07522	607446		JMP	WCNT-2	/RESTORE COUNT
	/				
07523	447665	Y64	ISZ	SVADR	/INCREMENT X LINE BY 1
07524	777704		LAW	=74	
07525	047650		DAC	CT04	/RESTORE Y LINE COUNTER
07526	207665		LAC	SVADR	
07527	507647		AND	K77	
07530	047665		DAC	SVADR	
07531	547646		SAD	K40	/COMPLEMENT PATTERN IF EQUAL
07532	741000		SKP		
07533	607520		JMP	N64+2	/START WITH NEW X-Y COMBO
07534	207664		LAC	SVMSTR	/PATTERN CONTROL WORD
07535	740001		CMA		
07536	047664		DAC	SVMSTR	/COMPLEMENTED CONTROL WORD
07537	607520		JMP	N64+2	
	/				
	/				
07540	047653	ERROR	DAC	BAD	/SAVE
07541	741200		SNA		/CHECK FOR FULL WORD ERROR
07542	607555		JMP	E1-1	/FULL WORD ERROR
07543	740001		CMA		
07544	741200		SNA		
07545	607555		JMP	E1-1	/FULL WORD ERROR
07546	207653		LAC	BAD	
07547	507657		AND	BITSUP	/SEE IF BIT SUPPRESSED
07550	740200		SZA		
07551	740001		CMA		
07552	507657		AND	BITSUP	
07553	741200		SNA		
07554	607504		JMP	RTN	/BIT SUPPRESSED
	/				
07555	207665		LAC	SVADR	
07556	740040	E1	HLT		/AC = FAILING ADDRESS
07557	207653		LAC	BAD	
07560	740040	E2	HLT		/AC = BAD DATA
07561	207654		LAC	GOOD	
07562	740040	E3	HLT		/AC = GOOD DATA
07563	207662		LAC	CNTRL	
07564	740040	E4	HLT		/AC = PATTERN CONTROL WORD
07565	750004		LAS		/SUPPRESSED BITS
07566	740001		CMA		
07567	047657		DAC	BITSUP	
07570	607504		JMP	RTN	/READ ANOTHER

/

/READ AND TEST Y LINES 01 TO 49 WITH X

/LINES 00 THRU 63. EACH X LINE WILL EQUAL
 /000000. AN X LINE WILL BE READ 1024 TIMES
 /AFTER WHICH, ALL Y LINES INTERSECTING,
 /WITH THAT X LINE WILL BE READ AND TESTED
 /FOR BIT ERRORS.

07571	147665	BURST	DZM	SVADR	
07572	777777	WONS	LAW	-1	
07573	067665		DAC*	SVADR	/WRITE 1'S IN 0000 TO 7400
07574	447665		ISZ	SVADR	
07575	207674		LAC	(7400	
07576	547665		SAD	SVADR	/DONE IF 7400
07577	741000		SKP		
07600	607572		JMP	WONS	
07601	147665		DZM	SVADR	/0000 IS STARTING ADDRESS
07602	207656		LAC	K100	
07603	047652		DAC	PATR	/SAVES XY COORDINATE
07604	207652	BRSTA	LAC	PATR	
07605	047666		DAC	SVLTH	/Y LINE ADDRESS
07606	776000		LAW	-2000	/=1024 DECIMAL
07607	047661		DAC	PATWD	
07610	167665		DZM*	SVADR	/CLEAR LINE XN
07611	227665		LAC*	SVADR	/READ 000000
07612	447661		ISZ	PATWD	/DISTURB LINE 1024 TIMES
07613	607611		JMP	*2	
07614	777777	BUST	LAW	-1	
07615	267666		XOR*	SVLTH	/DATA MUST BE 777777
07616	741200		SNA		/SHOULD NOT SKIP
07617	607623		JMP	CEND	/OK
07620	740001		CMA		
07621	047653		DAC	BAD	
07622	607641		JMP	E5-1	/ERROR PATH
07623	207656	CEND	LAC	K100	
07624	347666		TAD	SVLTH	/Y AXIS PLUS 1
07625	047666		DAC	SVLTH	
07626	207674		LAC	(7400	
07627	507666		AND	SVLTH	
07630	547674		SAD	(7400	
07631	741000		SKP		/DONE ALL Y ON CURRENT X LINE
07632	607614		JMP	BUST	/IF EQUAL
07633	447665		ISZ	SVADR	/READ NEXT Y ON CURRENT X
07634	447652		ISZ	PATR	/INCREMENT X ADDRESS
07635	207656		LAC	K100	/INCREMENT X+Y ADDRESS
07636	547665		SAD	SVADR	/DONE 64 X LINES IF EQUAL
07637	607430		JMP	COMP	/WRITE NEXT CHECKERBOARD
07640	607604		JMP	BRSTA	/TEST NEXT X WITH Y01 THRU Y60
/					
07641	207666		LAC	SVLTH	
07642	740040	E5	HLT		/AC = FAILING X + Y61 LINE
07643	207653		LAC	BAD	
07644	740040	E6	HLT		/AC = BAD DATA
07645	607623		JMP	CEND	

/CONSTANT AND STORAGE REGISTER

07646	000040	K40	40
07647	000077	K77	77
07650	000000	CT04	0
07651	000000	CT16	0
07652	000000	PATR	0
07653	000000	BAD	0
07654	000000	GOOD	0
07655	000001	K1	1
07656	000100	K100	100
07657	777777	BITSUP	LAW
07660	000000	PATCNT	0
07661	000000	PATWD	0
07662	000000	CNTRL	0
07663	000000	BITCON	0
07664	000000	SVMSTR	0
07665	000000	SVADR	0
07666	000000	SVLTH	0
07667	007671	PATN	,+2
07670	007671	NXTPAT	,+1
07671	463144		463144
07672	631460		631460
07673	525250		525250
	/		
07674	000000		.END
	007400	+L	

-1

NO ERROR LINES