8011 Disc Memory Controller
OPERATION & MAINTENANCE MANUAL
8011 Disc Memory Controller

OPERATION & MAINTENANCE MANUAL

AMCOMP

686 WEST MAUDE AVENUE
SUNNYVALE, CALIFORNIA 94086

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## REVISION RECORD

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This manual describes the AMCOMP 8011 Disc Memory Controller. The controller is used with the Data General Corporation Nova Series Computers to write data into or read data out of the AMCOMP models 8400 or 8500 Disc Memory Units.

This manual is divided into six chapters as follows:

Chapter 1 - General Information
Chapter 2 - Installation and Checkout
Chapter 3 - Operation and Interface
Chapter 4 - Theory of Operation
Chapter 5 - Maintenance
Chapter 6 - Drawings and Parts Lists

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Chapter 1

GENERAL INFORMATION
GENERAL INFORMATION

1-1  INTRODUCTION

This chapter contains general information pertaining to the AMCOMP 8011 Disc Memory Controller (figure 1-1). The information in this chapter consists of a general description, a physical description and a functional description. Specifications and characteristics for the controller are listed in table 1-1 of this chapter.

1-2  GENERAL DESCRIPTION

The 8011 Controller consists of a formatter assembly, an adapter board, interconnecting cables, and a diagnostic program. The formatter assembly consists of a single printed circuit (PC) board, a slide mountable chassis, and a DC power supply. The controller operates with Data General Corporation Nova Series Computers in writing data to or reading data from the disc memory units. The adapter PC board deals with Nova Computer interface functions, and the formatter PC board with AMCOMP disc memory control functions.

The controller can interface up to four (daisy-chain configuration) 8430 or 8530 Disc Memory Units. These disc units range from 16 to 128 tracks each for the 8400, and from 16 to 256 tracks each maximum for the 8530. The track selection and size configuration is accomplished through the power connection of "E" pins in the formatter PC board.

Each track on a disc contains 32 sectors and each sector contains 16 subsectors. Each subsector stores 16 words plus a 16-bit cyclic code word and parity bit. The 16 subsectors that comprise one sector may or may not be adjacent to each other on a track, depending upon the interlace factor wired into the formatter PC board. The subsector interlacing is used to change the average data transfer rate of the system and allowing the disc to be matched with the speed of the various Nova Computers. The formatter PC board can be wired for 1:1, 2:1, 4:1, or 8:1 interlace factors.

An interleaving feature, available as an option, changes the numbering scheme of the tracks and assures processor time between consecutively numbered sectors. (See paragraph 1-5.)

Error checking is provided by a 16-bit cyclic code word and an odd parity bit that are automatically written by the controller at the end of each subsector. When each subsector is read, the cyclic code and the parity bit are read and compared against the code that was generated from the previous 16 words. If the codes differ, the data error status flag is set indicating a data error.
Figure 1-1. 8011 Disc Memory Controller
When the 8011 Controller is providing a diagnostic mode of operation, it allows approximately one-half of its circuitry to be checked independently of the disc memory units. During this mode of operation, 16 words of data are transferred between the Nova Computer and the controller without accessing the disc memory units. Note that there must be a disc on line to run the diagnostic mode.

1-3 PHYSICAL DESCRIPTION

The formatter PC board and power supply are contained in a 19-inch rack-mountable chassis (formatter assembly). The adapter PC board plugs into an input/output slot in the Nova Computer. (See table 1-1 for specifications and characteristics.)

<table>
<thead>
<tr>
<th>TABLE 1-1. SPECIFICATIONS AND CHARACTERISTICS</th>
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</thead>
<tbody>
<tr>
<td><strong>Power Requirements</strong></td>
</tr>
<tr>
<td><strong>Formatter Assembly</strong></td>
</tr>
<tr>
<td>Voltage</td>
</tr>
<tr>
<td>Frequency</td>
</tr>
<tr>
<td>Run Current</td>
</tr>
<tr>
<td><strong>Adapter Board</strong></td>
</tr>
<tr>
<td>Voltage</td>
</tr>
<tr>
<td>Current</td>
</tr>
<tr>
<td><strong>Environmental Specifications</strong></td>
</tr>
<tr>
<td>Operating Temperature</td>
</tr>
<tr>
<td>Non-Operating Temperature</td>
</tr>
<tr>
<td>Temperature Change</td>
</tr>
<tr>
<td>Relative Humidity (Operating)</td>
</tr>
<tr>
<td>Relative Humidity (Non-Operating)</td>
</tr>
<tr>
<td><strong>Physical Characteristic</strong></td>
</tr>
<tr>
<td><strong>Formatter Assembly</strong></td>
</tr>
<tr>
<td>Height</td>
</tr>
<tr>
<td>Width</td>
</tr>
<tr>
<td>Depth</td>
</tr>
<tr>
<td>Weight</td>
</tr>
</tbody>
</table>
TABLE 1-1. SPECIFICATIONS AND CHARACTERISTICS (continued)

<table>
<thead>
<tr>
<th>Adapter Board (plugged in computer slot)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>0.5 in. (1.27 cm.)</td>
</tr>
<tr>
<td>Width</td>
<td>15.0 in. (38.10 cm.)</td>
</tr>
<tr>
<td>Depth</td>
<td>15.0 in. (38.10 cm.)</td>
</tr>
</tbody>
</table>

1-4 FUNCTIONAL DESCRIPTION

At the start of any operation the computer sends instructions to the controller. These instructions specify the starting core memory address, unit address, track address, and sector address. They also specify the operation to be performed (read, write, or diagnostic mode).

In addition to the instructions from the Nova Computer, the operational software can provide instruction (DOC) to allow a subsector address and subsector count to be specified.

After selection of the unit address and track address, specified in the instruction from the computer, the controller selects the disc operation contained in the computer instruction by generating either the start (READ) or pulse (WRITE) function.

If the controller is placed in the diagnostic mode, the read and write operations specified by the computer are performed only between the computer and controller. (See chapters 3 and 4 for more complete functional information.)

1-5 INTERLEAVING

Since the controller cannot process consecutively physically adjacent sectors on a track, the sectors are numbered alternately with the numbering scheme changing from one track to the next as shown in the tracks of figure 1-2. With such numbering arrangement, the program can process consecutively numbered sectors in a given track and switch to the first sector of the next track all with minimum waiting time. Thus, switching time between sectors is 2.085 milliseconds except when switching from sector 3 to sector 4 for which the time is double (2 sectors apart), i.e., 4.17 milliseconds. The interleave of figure 1-2 shows the track-sector configuration for a 3600-rpm disc unit with 4:1 interlace factor.
Figure 1-2. Track-Sector Configuration
Chapter 2

INSTALLATION AND CHECKOUT
INSTALLATION AND CHECKOUT

2-1 INTRODUCTION

This chapter provides installation instructions for the 8011 Disc Memory Controller. Included in this chapter are unpacking and equipment location instructions, an installation procedure, tables and diagrams, and voltage selection procedure. The installation procedure, tables and diagrams provide the following instructions:

1. Wiring and connecting the cable assemblies between the Nova Computer and the formatter assembly.
2. Installing the adapter PC board.
3. Wiring the Nova Computer backplane (cables 1060024 and 1060025).
4. Wiring the formatter PC board for the proper system configuration.
5. Wiring the disc memory units for address assignments.
6. Connecting the disc memory unit or units to the formatter assembly.

2-2 UNPACKING AND INSPECTION

The controller is shipped in a special packing case. As the equipment is unpacked, care should be exercised to prevent damage to the finished surfaces of the unit. All parts should be inspected for evidence of damage during shipment. If the packing case or any unit parts are damaged, advise the manufacturer and file a claim with the transfer company. The following procedure should be followed for unpacking and inspecting the unit:

a. Open the packing case and remove the contents. Check items removed against the shipping list to verify packing case contents. Contact AMCOMP in the event there is a shortage.

b. Remove any additional packing material and verify that the serial number of the unit corresponds to that shown on the shipping invoice.

NOTE

If reshipment of unit becomes necessary, a new packing case may be acquired from the manufacturer. The manufacturer is not responsible for damage incurred during shipment due to faulty packing.
c. Visually inspect the exterior of the unit for evidence of any physical damage that may have occurred in transit. Inspect the cover for dents or abrasions.

d. Check for broken or damaged components and broken or loose wires on connectors.

**NOTE**

If any damage is discovered, notify the manufacturer and the transfer company immediately. If manufacturer is not notified of the damage to the unit and damaged unit is subsequently operated may void the warranty.

2-3 **EQUIPMENT LOCATION**

The formatter assembly is a slide mountable chassis mounted on the cabinet together with the outer slides. The adapter PC board is installed in a selected slot within the Nova Computer chassis.

2-4 **INSTALLATION PROCEDURE**

A cabling diagram for a typical 8011 Disc Memory Controller is shown in figure 2-1. Tables 2-1, 2-2 and 2-3 list the signals between the adapter and formatter board, between formatter and disc memory unit, and between adapter board and Nova Computer. Install the controller as follows:

a. Select an I/O slot on the Nova Computer for installing the adapter PC board and then wire backplane connector end of CPU-A cable assembly (Part No. 1060024) to pins of electrical connector A of selected I/O slot according to wiring connections given in table 2-1.

b. Wire backplane connector end of CPU-B cable assembly (Part No. 1060025) to pins of electrical connector B of selected I/O slot in accordance with wiring connections given in table 2-1.

c. Install the adapter PC board in selected I/O slot.

d. Connect one of the two formatter cable assemblies (Part No. 1060019) to connector J2 on formatter PC board via backplane connector J3. Connect other end (P2) of this cable to CPU-A cable assembly (figure 2-1).

e. Connect other formatter cable assembly (Part No. 1060019) to connector J1 on formatter PC board via backplane connector J1. Connect other end (P2) of this cable assembly to CPU-B cable assembly (figure 2-1).

**CAUTION**

Connector J1 on formatter board (J1 on backplane) must be connected to CPU-B on computer, and connector J2 (J3 on backplane) must be connected to CPU-A on computer, or electrical damage to equipment may result.
NOTES:

1. ALL CABLES ARE CONNECTED ON A ONE-TO-ONE BASIS.

2. MAXIMUM I/O CABLE LENGTH BETWEEN FORMATTER PC BOARD AND LAST DISC MEMORY UNIT IS 30 FEET.

3. TERMINATORS E4 AND E5 MUST BE REMOVED FROM ALL BUT LAST DISC MEMORY UNIT IN THE DAISY-CHAIN.

4. POWER TO THE DISC MEMORY UNIT WITH TERMINATORS (LAST UNIT) MUST BE ON WHILE THE OTHER DISC UNITS ARE IN OPERATION.

Figure 2-1. Typical 8011 Disc Memory Controller Cabling Diagram (Daisy-Chain Configuration)
<table>
<thead>
<tr>
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<th>SIGNAL MNEMONIC</th>
<th>ORIGINATION</th>
<th>CONNECTOR/PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buffer Empty</td>
<td>BFEMTY</td>
<td>X</td>
<td>J2-19</td>
</tr>
<tr>
<td>Buffer Full</td>
<td>BFFUL-</td>
<td>X</td>
<td>J2-21</td>
</tr>
<tr>
<td>Buffers</td>
<td>BUDDS</td>
<td>X</td>
<td>J2-39</td>
</tr>
<tr>
<td>Data Bit 00</td>
<td>DB00</td>
<td>X</td>
<td>J1-9</td>
</tr>
<tr>
<td>01</td>
<td>DB01-</td>
<td>X</td>
<td>J1-11</td>
</tr>
<tr>
<td>02</td>
<td>DB02-</td>
<td>X</td>
<td>J1-13</td>
</tr>
<tr>
<td>03</td>
<td>DB03-</td>
<td>X</td>
<td>J1-15</td>
</tr>
<tr>
<td>04</td>
<td>DB04-</td>
<td>X</td>
<td>J1-17</td>
</tr>
<tr>
<td>05</td>
<td>DB05-</td>
<td>X</td>
<td>J1-19</td>
</tr>
<tr>
<td>06</td>
<td>DB06-</td>
<td>X</td>
<td>J1-21</td>
</tr>
<tr>
<td>07</td>
<td>DB07-</td>
<td>X</td>
<td>J1-23</td>
</tr>
<tr>
<td>08</td>
<td>DB08-</td>
<td>X</td>
<td>J1-25</td>
</tr>
<tr>
<td>09</td>
<td>DB09-</td>
<td>X</td>
<td>J1-27</td>
</tr>
<tr>
<td>10</td>
<td>DB10-</td>
<td>X</td>
<td>J1-29</td>
</tr>
<tr>
<td>11</td>
<td>DB11-</td>
<td>X</td>
<td>J1-31</td>
</tr>
<tr>
<td>12</td>
<td>DB12-</td>
<td>X</td>
<td>J1-33</td>
</tr>
<tr>
<td>13</td>
<td>DB13-</td>
<td>X</td>
<td>J1-35</td>
</tr>
<tr>
<td>14</td>
<td>DB14-</td>
<td>X</td>
<td>J1-37</td>
</tr>
<tr>
<td>15</td>
<td>DB15-</td>
<td>X</td>
<td>J1-39</td>
</tr>
<tr>
<td>Data Register Arrival</td>
<td>DRAVL-</td>
<td>X</td>
<td>J2-43</td>
</tr>
<tr>
<td>Data Register Full</td>
<td>DRFUL-</td>
<td>X</td>
<td>J2-17</td>
</tr>
<tr>
<td>Data Register Set</td>
<td>DRSETPS-</td>
<td>X</td>
<td>J2-41</td>
</tr>
<tr>
<td>Data Bit 00</td>
<td>DB00-</td>
<td>X</td>
<td>J1-9</td>
</tr>
<tr>
<td>01</td>
<td>DB01-</td>
<td>X</td>
<td>J1-11</td>
</tr>
<tr>
<td>02</td>
<td>DB02-</td>
<td>X</td>
<td>J1-13</td>
</tr>
<tr>
<td>03</td>
<td>DB03-</td>
<td>X</td>
<td>J1-15</td>
</tr>
<tr>
<td>04</td>
<td>DB04-</td>
<td>X</td>
<td>J1-17</td>
</tr>
<tr>
<td>05</td>
<td>DB05-</td>
<td>X</td>
<td>J1-19</td>
</tr>
<tr>
<td>06</td>
<td>DB06-</td>
<td>X</td>
<td>J1-21</td>
</tr>
<tr>
<td>07</td>
<td>DB07-</td>
<td>X</td>
<td>J1-23</td>
</tr>
<tr>
<td>08</td>
<td>DB08-</td>
<td>X</td>
<td>J1-25</td>
</tr>
<tr>
<td>09</td>
<td>DB09-</td>
<td>X</td>
<td>J1-27</td>
</tr>
<tr>
<td>10</td>
<td>DB10-</td>
<td>X</td>
<td>J1-29</td>
</tr>
<tr>
<td>11</td>
<td>DB11-</td>
<td>X</td>
<td>J1-31</td>
</tr>
<tr>
<td>12</td>
<td>DB12-</td>
<td>X</td>
<td>J1-33</td>
</tr>
<tr>
<td>13</td>
<td>DB13-</td>
<td>X</td>
<td>J1-35</td>
</tr>
<tr>
<td>14</td>
<td>DB14-</td>
<td>X</td>
<td>J1-37</td>
</tr>
<tr>
<td>15</td>
<td>DB15-</td>
<td>X</td>
<td>J1-39</td>
</tr>
<tr>
<td>Data Register Full</td>
<td>DRFUL-</td>
<td>X</td>
<td>J2-17</td>
</tr>
<tr>
<td>Data Register Gate</td>
<td>DRCGAT-</td>
<td>X</td>
<td>J2-23</td>
</tr>
<tr>
<td>DOC Instruction</td>
<td>DOCX</td>
<td>X</td>
<td>J2-31</td>
</tr>
<tr>
<td>End Error</td>
<td>ENDER-</td>
<td>X</td>
<td>J2-15</td>
</tr>
</tbody>
</table>
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<thead>
<tr>
<th>SIGNAL DEFINITION</th>
<th>SIGNAL MNEMONIC</th>
<th>ORIGINATION</th>
<th>CONNECTOR/PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>FORMATTER BOARD</td>
<td>ADAPTER BOARD</td>
</tr>
<tr>
<td>End Strobe</td>
<td>ENDS</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Initiate</td>
<td>INIT</td>
<td>X</td>
<td>J2-35</td>
</tr>
<tr>
<td>Read Operation</td>
<td>RDOP</td>
<td>X</td>
<td>J1-41</td>
</tr>
<tr>
<td>Read Sector Go</td>
<td>RSGO-</td>
<td>X</td>
<td>J1-43</td>
</tr>
<tr>
<td>Reset</td>
<td>RST</td>
<td>X</td>
<td>J2-33</td>
</tr>
<tr>
<td>Sector Continue</td>
<td>SCOPCK</td>
<td>X</td>
<td>J2-11</td>
</tr>
<tr>
<td>Operation Clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status In</td>
<td>STATIN</td>
<td>X</td>
<td>J2-25</td>
</tr>
<tr>
<td>Subsector Address</td>
<td>SALDS-</td>
<td>X</td>
<td>J2-29</td>
</tr>
<tr>
<td>Load One-Shot</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Track/Sector</td>
<td>TSASET</td>
<td>X</td>
<td>J2-27</td>
</tr>
<tr>
<td>Address Set</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Write Operation</td>
<td>WROP</td>
<td>X</td>
<td>J1-45</td>
</tr>
<tr>
<td>Write Sector Go</td>
<td>WSGO-</td>
<td>X</td>
<td>J1-47</td>
</tr>
</tbody>
</table>

TABLE 2-2. FORMATTER BOARD/DISC MEMORY UNIT I/O SIGNAL AND PIN ASSIGNMENTS (CONNECTOR J3)

<table>
<thead>
<tr>
<th>SIGNAL DEFINITION</th>
<th>SIGNAL MNEMONIC</th>
<th>INPUT TO FORMATTER</th>
<th>OUTPUT FROM FORMATTER</th>
<th>PIN No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disc Ready</td>
<td>DSCRDY</td>
<td>X</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td>X</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Head Change</td>
<td>HEAD CHANGE</td>
<td></td>
<td>X</td>
<td>32</td>
</tr>
<tr>
<td>Perm Address</td>
<td>PERM ADDRESS</td>
<td>X</td>
<td></td>
<td>17</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td></td>
<td>X</td>
<td>18</td>
</tr>
<tr>
<td>Read</td>
<td>READ</td>
<td></td>
<td></td>
<td>27</td>
</tr>
<tr>
<td>Read Clock</td>
<td>RD CLK</td>
<td>X</td>
<td></td>
<td>39</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td>X</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>Read Data</td>
<td>RD DATA</td>
<td>X</td>
<td></td>
<td>31</td>
</tr>
<tr>
<td>Sector Clock</td>
<td>SCLK</td>
<td>X</td>
<td></td>
<td>23</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td>X</td>
<td></td>
<td>24</td>
</tr>
<tr>
<td>Sector Write</td>
<td>SWD</td>
<td></td>
<td>X</td>
<td>25</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td>X</td>
<td></td>
<td>26</td>
</tr>
<tr>
<td>Track Address 0</td>
<td>TA0</td>
<td>X</td>
<td></td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>TA1</td>
<td>X</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>TA2</td>
<td>X</td>
<td></td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>TA3</td>
<td>X</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>TA4</td>
<td>X</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>TA5</td>
<td>X</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>TA6</td>
<td>X</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>TA7</td>
<td>X</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>TA8</td>
<td>X</td>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

2-5
TABLE 2-2. FORMATTER CARD/DISC MEMORY UNIT I/O SIGNAL AND PIN ASSIGNMENTS (CONNECTOR J3) (continued)

<table>
<thead>
<tr>
<th>SIGNAL DEFINITION</th>
<th>SIGNAL MNEMONIC</th>
<th>INPUT TO FORMATTER</th>
<th>OUTPUT FROM FORMATTER</th>
<th>PIN No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Track Origin</td>
<td>TO</td>
<td>X</td>
<td></td>
<td>21</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td></td>
<td></td>
<td>22</td>
</tr>
<tr>
<td>Unit Select 0</td>
<td>USEL 0</td>
<td></td>
<td>X</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>USEL 1</td>
<td></td>
<td>X</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>USEL 2</td>
<td></td>
<td>X</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>USEL 3</td>
<td></td>
<td>X</td>
<td>12</td>
</tr>
<tr>
<td>Write</td>
<td>WRRT</td>
<td></td>
<td></td>
<td>29</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td></td>
<td></td>
<td>30</td>
</tr>
<tr>
<td>Write Clock In</td>
<td>WRCLKIN</td>
<td></td>
<td>X</td>
<td>43</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td></td>
<td></td>
<td>44</td>
</tr>
<tr>
<td>Write Clock Out</td>
<td>WCLK</td>
<td></td>
<td>X</td>
<td>47</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td></td>
<td></td>
<td>48</td>
</tr>
<tr>
<td>Write Data</td>
<td>WRDATA</td>
<td></td>
<td>X</td>
<td>35</td>
</tr>
<tr>
<td>Return</td>
<td>GND</td>
<td></td>
<td></td>
<td>36</td>
</tr>
</tbody>
</table>

TABLE 2-3. ADAPTER BOARD/NOVA COMPUTER I/O SIGNAL AND PIN ASSIGNMENTS

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>SIGNAL MNEMONIC</th>
<th>INPUT TO ADAPTER</th>
<th>OUTPUT FROM ADAPTER</th>
<th>CONNECTOR/PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear</td>
<td>CLR</td>
<td>X</td>
<td></td>
<td>A-50</td>
</tr>
<tr>
<td>Data 00</td>
<td>DATA00</td>
<td>X</td>
<td>X</td>
<td>A-62</td>
</tr>
<tr>
<td>01</td>
<td>01</td>
<td>X</td>
<td>X</td>
<td>A-65</td>
</tr>
<tr>
<td>02</td>
<td>02</td>
<td>X</td>
<td>X</td>
<td>A-82</td>
</tr>
<tr>
<td>03</td>
<td>03</td>
<td>X</td>
<td>X</td>
<td>A-73</td>
</tr>
<tr>
<td>04</td>
<td>04</td>
<td>X</td>
<td>X</td>
<td>A-61</td>
</tr>
<tr>
<td>05</td>
<td>05</td>
<td>X</td>
<td>X</td>
<td>A-57</td>
</tr>
<tr>
<td>06</td>
<td>06</td>
<td>X</td>
<td>X</td>
<td>A-95</td>
</tr>
<tr>
<td>07</td>
<td>07</td>
<td>X</td>
<td>X</td>
<td>A-55</td>
</tr>
<tr>
<td>08</td>
<td>08</td>
<td>X</td>
<td>X</td>
<td>A-60</td>
</tr>
<tr>
<td>09</td>
<td>09</td>
<td>X</td>
<td>X</td>
<td>A-63</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>X</td>
<td>X</td>
<td>A-75</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>X</td>
<td>X</td>
<td>A-58</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>X</td>
<td>X</td>
<td>A-59</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>X</td>
<td>X</td>
<td>A-64</td>
</tr>
<tr>
<td>14</td>
<td>14</td>
<td>X</td>
<td>X</td>
<td>A-56</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>X</td>
<td>X</td>
<td>A-66</td>
</tr>
<tr>
<td>Data In A Instruction</td>
<td>DATIA</td>
<td>X</td>
<td></td>
<td>A-44</td>
</tr>
<tr>
<td>Data In B Instruction</td>
<td>DATIB</td>
<td>X</td>
<td></td>
<td>A-42</td>
</tr>
<tr>
<td>Data Out A Instruction</td>
<td>DATOA</td>
<td>X</td>
<td></td>
<td>A-58</td>
</tr>
<tr>
<td>Data Out B Instruction</td>
<td>DATOB</td>
<td>X</td>
<td></td>
<td>A-56</td>
</tr>
<tr>
<td>Data Out C Instruction</td>
<td>DATOC</td>
<td>X</td>
<td></td>
<td>A-48</td>
</tr>
<tr>
<td>Data Channel</td>
<td>DCHA-</td>
<td>X</td>
<td></td>
<td>A-60</td>
</tr>
</tbody>
</table>
### Table 2-3. Adapter Board/NOVA Computer I/O Signal and Pin Assignments (continued)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Signal Mnemonic</th>
<th>Input to Adapter</th>
<th>Output from Adapter</th>
<th>Connector/Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Channel In</td>
<td>DCHI</td>
<td>X</td>
<td></td>
<td>B-37</td>
</tr>
<tr>
<td>Data Channel Mode</td>
<td>DCHM0-</td>
<td>X</td>
<td></td>
<td>B-17</td>
</tr>
<tr>
<td>Data Channel Out</td>
<td>DCHO</td>
<td>X</td>
<td></td>
<td>B-33</td>
</tr>
<tr>
<td>Data Channel Priority In</td>
<td>DCHPIN-</td>
<td>X</td>
<td></td>
<td>A-94</td>
</tr>
<tr>
<td>Data Channel Priority Out</td>
<td>DCHPOT-</td>
<td>X</td>
<td></td>
<td>A-93</td>
</tr>
<tr>
<td>Data Channel Request</td>
<td>DCHR-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device Select 0</td>
<td>DS0-</td>
<td>X</td>
<td></td>
<td>A-72</td>
</tr>
<tr>
<td>1</td>
<td>DS1-</td>
<td>X</td>
<td></td>
<td>A-68</td>
</tr>
<tr>
<td>2</td>
<td>DS2-</td>
<td>X</td>
<td></td>
<td>A-66</td>
</tr>
<tr>
<td>3</td>
<td>DS3-</td>
<td>X</td>
<td></td>
<td>A-46</td>
</tr>
<tr>
<td>4</td>
<td>DS4-</td>
<td>X</td>
<td></td>
<td>A-62</td>
</tr>
<tr>
<td>5</td>
<td>DS5-</td>
<td>X</td>
<td></td>
<td>A-64</td>
</tr>
<tr>
<td>Interrupt Acknowledge</td>
<td>INTA</td>
<td></td>
<td></td>
<td>A-40</td>
</tr>
<tr>
<td>Interrupt Priority In</td>
<td>INTPIN-</td>
<td></td>
<td></td>
<td>A-96</td>
</tr>
<tr>
<td>Interrupt Priority Out</td>
<td>INTPOT-</td>
<td></td>
<td></td>
<td>A-95</td>
</tr>
<tr>
<td>Interrupt Received</td>
<td>INTR-</td>
<td></td>
<td></td>
<td>A-29</td>
</tr>
<tr>
<td>Input/Output Pulse</td>
<td>IOPLS</td>
<td>X</td>
<td></td>
<td>A-74</td>
</tr>
<tr>
<td>Input/Output Reset</td>
<td>IORST</td>
<td>X</td>
<td></td>
<td>A-70</td>
</tr>
<tr>
<td>Mask Out</td>
<td>MSKO-</td>
<td>X</td>
<td></td>
<td>A-38</td>
</tr>
<tr>
<td>Request Enable</td>
<td>RQENB-</td>
<td>X</td>
<td></td>
<td>B-4</td>
</tr>
<tr>
<td>Select Busy</td>
<td>SELB-</td>
<td></td>
<td></td>
<td>A-82</td>
</tr>
<tr>
<td>Select Done</td>
<td>SELD-</td>
<td></td>
<td></td>
<td>A-80</td>
</tr>
<tr>
<td>Start</td>
<td>STRT</td>
<td></td>
<td></td>
<td>A-52</td>
</tr>
</tbody>
</table>

f. Verify proper wiring of "E" pins on formatter for proper disc memory unit according to table 2-4.

g. Verify proper wiring of "E" pins on formatter board for proper sector interlace factor in accordance with tables 2-5 and 2-6.

h. Verify proper wiring of "E" pins on formatter board for proper system size in accordance with table 2-7.

i. Verify proper wiring of "E" pins on formatter board for disc unit address assignments as shown in table 2-8.
j. Verify "E" pins on formatter board for disc unit address assignments as shown in table 2-9.

k. Wire "E" pins on adapter board according to selected device address (unit is shipped for device address 20) as shown in table 2-10.

l. If daisy-chaining of disc memory units is used, remove signal line resistive terminations from PC board of each disc memory unit except from disc memory unit at end cable.

NOTE

It is recommended that disc unit address 0 be connected at the end of the daisy-chain cable assembly. This allows other disc memory units to be removed or connected without changing the system cabling.

---

**TABLE 2-4. 8400/8500 DISC UNIT SELECTION WIRE CONNECTIONS**

<table>
<thead>
<tr>
<th>DISC MEMORY UNIT</th>
<th>STRAPPING</th>
</tr>
</thead>
<tbody>
<tr>
<td>8400</td>
<td>E56 To E57</td>
</tr>
<tr>
<td></td>
<td>E59 To E61</td>
</tr>
<tr>
<td></td>
<td>E58 To E62</td>
</tr>
<tr>
<td>8500</td>
<td>E56 To E59</td>
</tr>
<tr>
<td></td>
<td>E61 To E58</td>
</tr>
<tr>
<td></td>
<td>E62 To E60</td>
</tr>
</tbody>
</table>
### TABLE 2-5. SEQUENTIAL SECTOR INTERLACE WIRE CONNECTIONS

<table>
<thead>
<tr>
<th>FROM</th>
<th>1:1</th>
<th>2:1</th>
<th>4:1</th>
<th>8:1</th>
</tr>
</thead>
<tbody>
<tr>
<td>E19</td>
<td>E40</td>
<td>E37</td>
<td>E32</td>
<td>E31</td>
</tr>
<tr>
<td>E20</td>
<td>E39</td>
<td>E40</td>
<td>E37</td>
<td>E32</td>
</tr>
<tr>
<td>E17</td>
<td>E34</td>
<td>E39</td>
<td>E40</td>
<td>E37</td>
</tr>
<tr>
<td>E18</td>
<td>E33</td>
<td>E34</td>
<td>E39</td>
<td>E40</td>
</tr>
<tr>
<td>E23</td>
<td>E30</td>
<td>E33</td>
<td>E34</td>
<td>E39</td>
</tr>
<tr>
<td>E24</td>
<td>E29</td>
<td>E30</td>
<td>E33</td>
<td>E34</td>
</tr>
<tr>
<td>E21</td>
<td>E31</td>
<td>E29</td>
<td>E30</td>
<td>E33</td>
</tr>
<tr>
<td>E22</td>
<td>E32</td>
<td>E31</td>
<td>E29</td>
<td>E30</td>
</tr>
<tr>
<td>E27</td>
<td>E37</td>
<td>E32</td>
<td>E31</td>
<td>E29</td>
</tr>
</tbody>
</table>

### TABLE 2-6. WIRE CONNECTIONS FOR SECTOR INTERLACE WITH NOVA COMPUTER INTERLEAVING

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>FROM</th>
<th>AMCOMP COMPATIBLE</th>
<th>NOVA COMPATIBLE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1:1</td>
<td>2:1</td>
</tr>
<tr>
<td>LCC5</td>
<td>E29</td>
<td>E51</td>
<td>E51</td>
</tr>
<tr>
<td>LCC4</td>
<td>E30</td>
<td>E52</td>
<td>E52</td>
</tr>
<tr>
<td>LCC6</td>
<td>E31</td>
<td>E50</td>
<td>E50</td>
</tr>
<tr>
<td>LCC7</td>
<td>E32</td>
<td>E49</td>
<td>E19</td>
</tr>
<tr>
<td>LCC3</td>
<td>E33</td>
<td>E18</td>
<td>E23</td>
</tr>
<tr>
<td>LCC2</td>
<td>E34</td>
<td>E17</td>
<td>E18</td>
</tr>
<tr>
<td>LCC8</td>
<td>E37</td>
<td>E23</td>
<td>E24</td>
</tr>
<tr>
<td>LCC1</td>
<td>E39</td>
<td>E20</td>
<td>E17</td>
</tr>
<tr>
<td>LCC0</td>
<td>E40</td>
<td>E19</td>
<td>E20</td>
</tr>
<tr>
<td>BN4</td>
<td>E41</td>
<td>E36</td>
<td>N/C</td>
</tr>
<tr>
<td>BN3</td>
<td>E42</td>
<td>E35</td>
<td>N/C</td>
</tr>
<tr>
<td>BN2</td>
<td>E43</td>
<td>E26</td>
<td>E26</td>
</tr>
<tr>
<td>AN4</td>
<td>E45</td>
<td>E27</td>
<td>N/C</td>
</tr>
<tr>
<td>AN3</td>
<td>E46</td>
<td>E22</td>
<td>E27</td>
</tr>
<tr>
<td>AN2</td>
<td>E47</td>
<td>E21</td>
<td>E22</td>
</tr>
<tr>
<td>AN1</td>
<td>E48</td>
<td>E24</td>
<td>E21</td>
</tr>
<tr>
<td>PUV</td>
<td>E53</td>
<td>E54</td>
<td>E54</td>
</tr>
</tbody>
</table>
### TABLE 2-7. 8400/8500 DISC SIZE WIRE CONNECTIONS

<table>
<thead>
<tr>
<th>DISC SIZE (TRACKS)</th>
<th>8400</th>
<th>8500</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>128</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>16</td>
<td>144</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>32</td>
<td>160</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>48</td>
<td>176</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>64</td>
<td>192</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>80</td>
<td>208</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>96</td>
<td>224</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
<tr>
<td>112</td>
<td>240</td>
<td>E9</td>
<td>E10</td>
<td>E1</td>
</tr>
</tbody>
</table>

### TABLE 2-8. UNIT SELECT ADDRESS WIRE CONNECTIONS

<table>
<thead>
<tr>
<th>UNIT No.</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>E1</td>
<td>E8</td>
</tr>
<tr>
<td>1</td>
<td>E1</td>
<td>E7</td>
</tr>
<tr>
<td>2</td>
<td>E1</td>
<td>E5</td>
</tr>
<tr>
<td>3</td>
<td>E1</td>
<td>E6</td>
</tr>
</tbody>
</table>

### TABLE 2-9. HIGHEST UNIT NUMBER WIRING CONNECTIONS

<table>
<thead>
<tr>
<th>HIGHEST UNIT No. ASSIGNED</th>
<th>TO</th>
<th>FROM</th>
<th>FROM</th>
<th>FROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>E3</td>
<td>E7</td>
<td>E6</td>
<td>E5</td>
</tr>
<tr>
<td>1</td>
<td>E3</td>
<td>E6</td>
<td>E7</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>E3</td>
<td>E7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>NONE</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE**

For multiple units of different size (different number of tracks) but not exceeding two different sizes, the unit having the fewest tracks must be assigned the highest unit number.
TABLE 2-10. DEVICE ADDRESS SELECTION CONNECTIONS

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>FROM</th>
<th>TO</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>E1</td>
<td>E2</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>E1</td>
<td>E3</td>
<td>Cut etch between E1 and E2</td>
</tr>
</tbody>
</table>

2-5 VOLTAGE SELECTION

Line voltages of 100, 120, 220, and 240 volts at an operating frequency of 48 to 62 Hz can be selected through a voltage selector PC board (figure 2-2) located in rear panel of the formatter chassis. To select an operating voltage perform the following steps:

1. Open cover door and rotate fuse-pull to left.

2. Select operating voltage by orienting PC board to position desired voltage on top left side. (Selected voltage should be visible when PC board is installed.)

3. Rotate fuse-pull back into normal position and re-insert fuse into holders, careful to install a fuse with correct value.

2-6 PERFORMANCE VERIFICATION

To verify program operation, refer to chapter 3, paragraph 3-10 and to User's Guide in Appendix A.
Operating voltage is shown in Connector window.

Figure 2-2. Voltage Selecting Connector
Chapter 3

OPERATION AND INTERFACE
3-1 INTRODUCTION

This chapter contains operation and programming considerations, interface input/output signals, and interface signal logic levels. Described in this chapter, under the above major paragraphs, are controller instructions, computer transfer instructions, loading information, and modes of operation.

The basic timing considerations, track selection requirements, write and read timing requirements, and a description of the input/output signals for the interface between the controller and the disc memory units are given in chapter 3 of the AMCOMP Operation and Maintenance Manuals for the disc memory unit.

3-2 OPERATION AND PROGRAMMING CONSIDERATIONS

The operation and programming considerations include controller instructions, computer input/output transfer instructions, automatic and non-automatic loading, and modes of operation.

3-3 CONTROLLER INSTRUCTIONS

The 8011 Disc Controller uses five of the Nova Computer I/O transfer instructions. These instructions are described in the following paragraphs.

3-4 DOA-, DSK (Data Out A-, Disc)

This instruction is as follows: Select the unit, track and sector according to the contents of ac (accumulator) bits 2 through 15 of the instruction as shown in figure 3-1, and perform the function specified by F (bits 8 and 9). The contents of F are as follows:

\[
\begin{align*}
00 & = \text{No operation (NOP)} \\
01 & = \text{Start (READ)} \\
10 & = \text{CLEAR} \\
11 & = \text{Pulse (WRITE)}
\end{align*}
\]
3-5  DOB-, DSK (Data Out B-, Disc)

This instruction (figure 3-2) is as follows: Load the contents of accumulator bits 0 through 15 into the core address counter (accumulator bit 0 should be 0) and perform the function specified by F (bits 8 and 9).

NOTE

If a logical 1 bit is contained in accumulator bit 0, the controller is placed in the diagnostic move.

---

**Figure 3-1. DOA-, DSK Instruction**

**Figure 3-2. DOB-, DSK Instruction**
This instruction reads the status of the disc memory system into accumulator bits 10 through 15 (figure 3-3), clears accumulator bits 0 through 9, and performs the function specified by F (bits 8 and 9). A logical 1 in bits 10 through 15 is decoded as follows:

a. Bit 10 (disc fail). The selected disc becomes not ready or the system is hung during a read or write operation (time out or ready). The setting of this bit clears Busy and sets Done, requesting an interrupt if interrupt disable is clear.

b. Bit 11 (write error). The program has specified write instruction and the selected track-sector is write-protected.

c. Bit 12 (timer error). The data channel, during read or write, has failed to respond in time to a request for access (i.e., because of preemption of the channel by faster devices).

d. Bit 13 (no such disc). The disc or track selected by the program is not available on this system. The setting of this bit clears busy and sets done, requesting an interrupt if interrupt disable is clear.

e. Bit 14 (data error). During a read operation, the cyclic check word or parity bit read from the disc differed from that computed by the controller for the data in the subsector.

f. Bit 15 (error). Bit 10, 11, 12, 13, 14 are a logical 1.

NOTE

The clear, start, or pulse function in an instruction clears all of the flags established by the setting of bits 10 through 15.

![Diagram of instruction and accumulator bits](image_url)

Figure 3-3. DIA-, DSK Instruction
3-7 DIB-, DSK (Data In B-, Disc)

This instruction (figure 3-4) is as follows: Read the present contents of the core address counter into accumulator bits 0 through 15. If the accumulator bit 0 is a logical 1, the unit is in the diagnostic mode. The contents of the core address counter is presented as zeros when this instruction is executed while the system is busy. This instruction can be ordinarily used for diagnostic purposes. Perform the function specified by F (bits 8 and 9).

![Figure 3-4. DIB-, DSK Instruction](image)

3-8 DOC O, DSK (Data Out C, Disc)

This instruction (figure 3-5) is as follows: Select the starting subsector address according to the contents of accumulator bits 0 through 3 and perform the function specified by F in the length according to the contents of accumulator bits 4 through 15. The 12-bit number expresses the length of operation in terms of number of subsectors. It must be a number in 2's complement form. The total number of words transferred is 16 times the specified subsector number.

The DOC instruction extends the capability of the controller beyond that provided by the Data General Disc System. It allows disc addressing to the subsector level. It also allows multiple (1-4096) subsector operation. When all 12 bits of accumulator bits 4 through 15 are specified as zeros, 4096 subsectors will be operated. When the DOC instruction is not executed, the operation is performed as one sector (16 subsectors) operation with disc subsector address starting at 0, which is compatible with the Data General Fixed Head Disc System.

NOTE

- If accumulator bits 4 through 15 are all high, one subsector will be transferred.

- If the DOC instruction is not executed, the system will transfer only one sector (256 words) of data.
The controller has the Nova Computer device code 20, mnemonic DSK, and uses five of the computer I/O transfer instructions. The busy and done flags from the controller are sensed by bits 8 and 9 in the computer skip instructions. The busy and done flags are controlled by the clear, start or pulse function in the instruction. Interrupt disable from the controller is controlled by interrupt priority task bit 9 in the computer. When a second controller is connected to the computer, its device code is 60, mnemonic DSK. If other disc memory units are used, additional codes are assigned.

The clear function in an instruction clears the busy and done flags, and thus terminates data transfers if a track sector is currently being processed. In addition to specifying the function, start and pulse both clear the done flag and set the busy flag. Start selects the read function and pulse selects the write function. Clear, start and pulse each clear the disc memory system status flags: disc fail, write error, data late, no such disc, data error and error.

Ordinarily sector 0, track 0 of disc 0 is reserved for binary loader. If the loader in core is destroyed by program debugging, it can be restored from the disc. The automatic and non-automatic loading procedures are described below.

To bring the loader into memory automatically, proceed as follows:

a. Set device code 20 into DATA switches 10 through 15 at the computer console for disc operation. Set device code 10 into DATA switches for TTY with paper tape operation.

b. If a Nova 1200 or 800 Series Computer with the program load option is being used, position the RESET-STOP switch to RESET position, turn on DATA switch 0, and then position PROGRAM LOAD switch to PROGRAM LOAD position. If a Supernova Computer is being used, position RESET-
STOP switch to RESET position and then position PROGRAM LOAD-CHANNEL start switch to CHANNEL START position.

3-12 Non-Automatic Loading

To bring the loader into memory without automatic loading, proceed as follows:

a. Load bootstrap loader into upper core through the switches.

b. Load binary loader (paper tape) into reader.

c. Set RESET-STOP switch to RESET.

d. Set switches to XX7770. 007770=4K and 777770-32K.

NOTE

If using a high speed reader switch, 0 must be a "1". If using TTY, switch 0 must be a "0".

e. Switch START-CONTINUE to START. (Program will stop at location XX 7777.)

f. Load program tape into reader.

g. START-CONTINUE.

h. Reference program tape listing for starting address and operation of program.

3-13 MODES OF OPERATION

The operation to be performed (read, write, or diagnostic) is specified in the instructions sent to the controller by the Nova Computer. These instructions are the DOA and DOB.

After one read operation, no further DOB instructions need be issued if subsequent operations are to be read operations and are to access consecutive sectors in core memory. For write operations, both the DOA and DOB instructions should be given.

At the completion of each operation, the program should check the status of the disc memory system, and if the data was late or in error, the operation should be repeated. The status should not be checked before starting an operation with a disc; the status is not valid until an operation has been performed.

3-14 Write Operation

When a write operation (pulse) is specified by the instructions from the computer, the controller requests and gains control of the computer data channel and starts transferring words consecutively into a 16-word data buffer. Simultaneously, the controller searches for the sector address on the selected track by comparing the sector address with an incrementing sector counter of the disc. When the specified sector is found, data in the buffer is written on the disc into the first 16-word subsector. The writing operation is
continued until one sector (16 subsectors) of data is transferred, or the specified number of subsectors are transferred (as specified in the DOC instruction). If the DOC instruction is not executed prior to or with the generation of the I/O pulse, one sector (16 subsectors) of data is transferred. Otherwise, the number of subsectors of data transferred is the number of subsectors specified by the DOC instruction.

3-15 Read Operation

When a read operation (start) is specified by the instructions from the computer, the controller searches for the sector address on the selected disc and track by comparing the sector address with the incrementing sector counter of the disc. Data words are then transferred from the disc into the 16-word data buffer. With the first word in the data buffer, the controller then requests and gains use of the data channel for inputting data to the computer. The length of data transfer is the same as that for the write operation.

3-16 Diagnostic Mode of Operation

When the controller is in the diagnostic mode, the read or write operation specified by the computer causes data transfers to be performed only between the computer and the controller.

The controller is placed in the diagnostic mode when a logical 1 is contained in accumulator bit 0 of a DOB instruction from the computer. The controller remains in the diagnostic mode until a logical 0 is contained in accumulator bit 0 in a subsequent DOB instruction from the computer. The DOA instruction that normally specifies the disc, track and sector address is not required in the diagnostic mode. A specified pulse function in the DOB instruction causes 16 words of data to be transferred from the specified core address in the computer to the 16-word buffer in the controller. The contents of the 16-word buffer is then read back to the computer when the computer issues a DOB instruction containing a start function. The contents of the buffer is read back in the logical 1's complement form from which it was written. The diagnostic mode of operation allows 16 words of data to be transferred between the computer and controller for diagnostic purposes without accessing the disc memory.

3-17 INTERFACE INPUT/OUTPUT SIGNALS

The description of the interface signals are divided into two categories: the Nova Computer to the controller and the controller to Nova Computer interface signals. Figure 3-6 contains the signals interfacing the controller (adapter and formatter boards).

3-18 NOVA COMPUTER TO CONTROLLER INTERFACE SIGNALS

The following paragraphs describe the interface signals from the Nova Computer to the 8011 Controller.

3-19 Device Selection (DS0 through DS5)

These signal lines are low in the assertive state. The processor places the device code (bits 10 through 15 of the instruction word) on these signal lines during the execution of an in-out instruction. These signal lines select one of 59 devices (codes 04 through 76) that may be connected to the I/O bus (the controller has the device code 20, mnemonic DSK). Only the selected device responds to control signals generated during the instruction.
NOTE: FOR SIGNAL MNEMONICS SEE TABLES 2.1, 2.2, AND 2.3.

Figure 3-6. Controller Interface Signals
3-20  **Data (DATA 0 through DATA 15)**

These signal lines are low when true and are used to transfer all data and addresses between the processor and controller.

For a programmed output, the processor places the accumulators specified by the instruction on the data lines and then generates DATOA, DATOB, or DATOC to load the data from the lines into the corresponding buffer in the controller of the disc memory system (selected device); or generates MSKO to set up the interrupt disable flags in all of the devices according to the mask on the data lines. For data channel output, the processor places the memory buffer on the data lines and generates signal DCHO to load the contents of the lines into the data register in the controller.

3-21  **Data Out A (DATOA)**

This signal is high when true and is generated by the processor after the accumulator signals have been placed on the data lines in a DOA instruction. DATOA is used to load the address into the unit, track and sector registers on the controller when the disc memory system is the device selected by DS0 through DS5.

3-22  **Data In A (DATIA)**

This signal is high when true and is generated by the processor during a DIA instruction to place the error register in the controller on the data lines when the disc memory system is the device selected by DS0 through DS5.

3-23  **Data Out B (DATOB)**

This signal is high when true and is generated by the processor, after accumulator data has been placed on the data lines in a DOB instruction. DATOB signal loads the data into the core memory address register in the controller when the disc memory system is the device selected by DS0 through DS5.

3-24  **Data In B (DATIB)**

This signal is high when true and is generated by the processor during DIB instruction. DATIB signal places the core memory address register in the controller on the data lines when the disc memory system is the device selected by DS0 through DS5.

3-25  **Data Out C (DATOC)**

This signal is high when true and is generated by the processor after accumulator bits have been placed on the data lines in a DOC instruction. DATOC signal loads the counter and subsector address register in the controller when the disc memory system is the device selected by DS0 through DS5.

3-26  **Start (STRT)**

This signal is high when true and is generated by the processor in a non-skip I/O instruction (DOA, DOB, DOC, etc.) with an S control function (bits 8 and 9 = 01). STRT signal clears done, sets busy, clears the INT REQ flip-flop, and selects a read operation in the controller when the disc memory system is the device selected by DS0 through DS5.
3-27 Clear (CLR)

This signal is high when true and is generated by the processor in a non-skip I/O instruction with a C control function (bits 8 and 9 = 10). CLR clears busy, done and INT REQ flip-flop in the controller when the disc memory system is the device selected by DS0 through DS5.

3-28 I/O Pulse (IOPLS)

This signal is high when true and is generated by the processor in a non-skip I/O instruction with a P control function (bits 8 and 9 = 11). IOPLS selects a write, clears done, sets busy, and clears the INT REQ flip-flop in the controller when the disc memory system is the device selected by DS0 through DS5.

3-29 Request Enable (RQENB)

This signal is low when true and is generated at the beginning of every memory cycle to allow all devices (including the disc memory system) on the I/O bus to request program interrupts or data channel access. In any device, RQENB sets the INT REQ flip-flop if done signal is set and interrupt disable is clear; otherwise, it clears INT REQ flip-flop. In any device connected to the data channel, RQENB sets the DCH REQ flip-flop if the DCH SYNC flip-flop is set; otherwise, it clears DCH REQ.

3-30 Interrupt Priority (INTP)

This signal is low when true and is generated by the processor for transmission serially to the device on the I/O bus. If the INT REQ flip-flop in a device is clear when the device received INTP, the signal is transmitted to the next device.

3-31 Interrupt Acknowledge (INTA)

This signal is high when true and is generated by the processor during the INTA instruction. If a device (including the disc memory system) received INTA while it is also receiving INTP and its INT REQ flip-flop is set, it places its device code on data lines 10 through 15.

3-32 Mask Out (MSKO)

This signal is low when true and is generated by the processor during the MSKO instruction after accumulator bits (data 09) have been placed on the data lines to set up the interrupt disable flags in all devices according to the mask on the lines.

3-33 Data Channel Priority (DCHP)

This signal is low when true and is generated by the processor and transmitted serially to the devices on the I/O bus. If the DCH REQ flip-flop in a device is clear when the device receives the DCHP signal, this signal is transmitted to the next device.

3-34 Data Channel Acknowledge (DCHA)

This signal is low when true and is generated by the processor at the beginning of a data channel cycle. If the controller receives DCHA while it is receiving DCHP and its DCH REQ flip-flop is set, it places the memory address to be used for data channel access on data lines 1 through 15 and sets the DCH SEL flip-flop.
3-35 Data Channel In (DCHI)

This signal is high when true and is generated by the processor for data channel input (DCHMO = logical 1) to place the data register of the controller on the data lines when the disc memory system is selected by DCHA.

3-36 Data Channel Out (DCHO)

This signal is high when true and is generated by the processor for data channel output (DCHMO = logical 0) after the word from memory or the arithmetic result has been placed on the data lines. DCHO signal loads the contents of the lines into the data register of the controller when the disc memory system is selected by DCHA.

3-37 I/O Reset (IORST)

This signal is high when true and is generated by the processor in the IORST instruction or when the console RESET switch is pressed to clear the control flip-flop in all interfaces connected to the I/O bus. This signal is also generated when power is turned on.

3-38 CONTROLLER TO NOVA COMPUTER INTERFACE SIGNALS

The following paragraphs describe the interface signals from the 8010 Controller to the Nova Computer.

3-39 Data (DATA0 through DATA15)

These signal lines are low when true and are used to transfer all data and addresses that are transferred between the processor and the controller.

For a programmed input, the processor generates DATIA or DATIB to place the error register or core memory address register in the controller on the data lines (when the disc memory system is selected by DS0 through DS5), or generates INTA to place the code of the nearest device that is requesting an interrupt on lines 10 through 15. The processor then loads the data from the lines into the accumulator selected by the instruction. To obtain an address for data channel access, the processor generates DCHA to place a memory address from the nearest device that is requesting access on lines 1 through 15 and then loads the address into the memory address register. For data channel input, the processor generates DCHI to place the data buffer of the controller on the data lines (when the disc memory system is the device being serviced), and then loads the contents of the lines into the memory buffer.

3-40 Selected Busy (SELB)

This signal is low when true and is generated by the controller (when the disc memory system is selected by DS0 through DS5) if its busy flag is set.

3-41 Selected Done (SELD)

This signal is low when true and is generated by the controller (when the disc memory system is selected by DS0 through DS5) if its done flag is set.
3-42 **Interrupt Request (INTR)**

This signal is low when true and is generated by any device (including the disc memory system) when its INT REQ flip-flop is set. In the disc controller the INT REQ flip-flop is set when the DONE flip-flop and INT MASK flip-flop are set.

3-43 **Data Channel Request (DCHR)**

This signal is low when true and is generated by any device (including the disc memory system) when its DCH REQ flip-flop is set. This informs the processor that the device is waiting for data channel access.

3-44 **Data Channel Mode (DCHMO)**

This signal is low when true and is generated by the controller when its DCH SEL flip-flop is set to inform the processor of the type of desired data channel cycle. For data in, this signal is low-true; for data out, the signal is high-true.

3-45 **INTERFACE SIGNAL LOGIC LEVELS**

The logic is either 14-pin or 16-pin dual in-line packages, with industrial operating temperatures ranging from 0°C to 70°C. All logic circuits are constructed with TTL integrated circuit chips of the small-scale and medium-scale integration type.

The interface logic used is positive having the following levels:

<table>
<thead>
<tr>
<th>Logical 1 (low-true = active low)</th>
<th>Logical 0 (high-false = active high)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 volts nominal</td>
<td>0.4 volts maximum</td>
</tr>
<tr>
<td>0.4 volts maximum</td>
<td>2.3 volts minimum</td>
</tr>
<tr>
<td>2.3 volts minimum</td>
<td>2.7 volts nominal</td>
</tr>
<tr>
<td>2.7 volts nominal</td>
<td>5.0 volts maximum</td>
</tr>
<tr>
<td>5.0 volts maximum</td>
<td>5.0 volts maximum</td>
</tr>
</tbody>
</table>

**NOTE**

Internal logic levels are contained in chapter 4.
Chapter 4

THEORY OF OPERATION
THEORY OF OPERATION

4-1 INTRODUCTION

This chapter provides logic diagram information, overall theory and circuit descriptions for the 8011 Disc Memory Controller. This includes detailed circuit descriptions of the controller adapter and formatter PC (printed circuit) boards.

4-2 LOGIC DIAGRAM AND SIGNAL INFORMATION

The signals appearing on the adapter and formatter logic boards are listed in table 4-1. The signals from the adapter PC board to Nova Computer are low-true and those from Nova Computer to the adapter PC board are either low-true or high-true, depending upon the particular signal. The signals from/to disc memory unit are low-true.

The low-true signals carry a minus sign at the right end of the signal term (i.e., DSCRDY-), while the high-true signals are presented plainly (i.e., DSCRDY).

NOTE

The interface signals and their logic levels are described in chapter 3; their origin and destination are listed in the tables of chapter 2.

The controller internal logic (between adapter and formatter PC boards) is standard positive having the following levels:

Logic 0 (low) = 0 to +0.4 volts
Logic 1 (high) = 2.3 to +5.0 volts

4-3 KEY TO BASIC SYMBOLOGY

Figure 4-1 shows the gate as well as the JK and D-Type flip-flop symbols together with their truth tables.

4-4 JUMPER CONNECTIONS

The E pins on the formatter PC board are jumpered in order to achieve selection of 8400 or 8500 Disc Memory Unit, disc unit size, sequential sector interlace, sector interlace with Nova Computer interleaving and disc unit (1 through 4) selection. (See chapter 2, tables 2-4 through 2-10.)
<table>
<thead>
<tr>
<th>Mnemonic Term</th>
<th>Signal Definition</th>
<th>Location*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Any Error</td>
<td>Output is negative true for any error output. This includes Read Error, Illegal Address Error, Data Transfer Error, Disc Failure Error, Write Protect Error or Ready Error.</td>
<td>83-2</td>
</tr>
<tr>
<td>AOVFA-</td>
<td>Address Over-Flow A</td>
<td>83-2</td>
</tr>
<tr>
<td>AOVFB-</td>
<td>Address Over-Flow B</td>
<td>83-2</td>
</tr>
<tr>
<td>AOVFE-</td>
<td>Address Over-Flow E</td>
<td>83-2</td>
</tr>
<tr>
<td>BCNT</td>
<td>Bit Count</td>
<td>83-1</td>
</tr>
<tr>
<td>BCNTO</td>
<td>Bit Count Zero</td>
<td>83-1</td>
</tr>
<tr>
<td>BCNT15</td>
<td>Bit Count Fifteen</td>
<td>83-1</td>
</tr>
<tr>
<td>FB00 - BF15</td>
<td>16 Word Buffer, Bit Zero through Bit Fifteen</td>
<td>83-3</td>
</tr>
<tr>
<td>BFEMTY-</td>
<td>Fuffer Empty</td>
<td>83-1, 27-1</td>
</tr>
<tr>
<td>BFEMTY</td>
<td>Fuffer Empty</td>
<td>83-1, 83-5, 27-1, 27-3</td>
</tr>
<tr>
<td>BFFUL</td>
<td>Buffer Full</td>
<td>83-1, 83-5, 27-1, 27-3</td>
</tr>
<tr>
<td>BFLD-</td>
<td>Buffer Load</td>
<td>83-5</td>
</tr>
<tr>
<td>BFLDCNR-</td>
<td>Buffer Load Control Register</td>
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<tr>
<td>BFLDR-</td>
<td>Buffer Load Register</td>
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</tr>
<tr>
<td>BFPSINH</td>
<td>Buffer Pulse Inhibit</td>
<td>83-1, 83-3</td>
</tr>
<tr>
<td>BUFFS</td>
<td>Buffers: Operate during diagnostic mode for 16 Word Transfers</td>
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</tr>
<tr>
<td>BUSY</td>
<td>Busy</td>
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</tr>
<tr>
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<td>Cyclic Code Not Zero Read</td>
<td>83-2, 83-5</td>
</tr>
<tr>
<td>CCYL, CCYL-</td>
<td>Cyclic Code Cycle</td>
<td>83-2, 83-5</td>
</tr>
<tr>
<td>CLR</td>
<td>Clear</td>
<td>27-1</td>
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<tr>
<td>DATA00-</td>
<td>Data Bit 00 through 15 from the Processor</td>
<td>27-2, 27-1</td>
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<tr>
<td>DATA15</td>
<td>Data Bit 15 of the Processor</td>
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<tr>
<td>DATIA</td>
<td>DIA Instruction</td>
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<td>DATIB</td>
<td>DIB Instruction</td>
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<td>DOA Instruction</td>
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<tr>
<td>DATOB</td>
<td>DOB Instruction</td>
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</tr>
<tr>
<td>DATOC</td>
<td>DOC Instruction</td>
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<td>Data Bit 00 through Data Bit 03 from the Adapter Card</td>
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<td>DB00 - DB15</td>
<td>Data Bit 00 through Data Bit 15 from the Adapter Card</td>
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<td>DCHA-</td>
<td>Data Channel Acknowledge</td>
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<td>Data Channel Acknowledge Delay Gated</td>
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<td>DCHBSY</td>
<td>Data Channel Busy</td>
<td>27-2, 27-3</td>
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<tr>
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<td>Data Channel Busy</td>
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<td>DCHI</td>
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<td>DCHIN-</td>
<td>Data Channel In Gated</td>
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<td>DCHMO-</td>
<td>Data Channel Mode</td>
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</tbody>
</table>

*The first two digits refer to the last two digits of the schematic number, third digit refers to sheet number.
<table>
<thead>
<tr>
<th>Mnemonic Term</th>
<th>Signal Definition</th>
<th>Location*</th>
</tr>
</thead>
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<td>Data Channel Out</td>
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<td>DCHR</td>
<td>Data Channel Request</td>
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<td>DOA Instruction</td>
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<td>DOC Instruction</td>
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<td>Data Register Arrival Generated by DCHIN</td>
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<td>Data Register Count Control</td>
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</tr>
<tr>
<td>DRFUL</td>
<td>Data Register Full</td>
<td>83-5, 27-3</td>
</tr>
<tr>
<td>DRGAT</td>
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<td>83-2, 27-1</td>
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<tr>
<td>DSCRDY</td>
<td>Disc Ready</td>
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<tr>
<td>DRSET</td>
<td>Data Register Set</td>
<td>83-3, 83-5</td>
</tr>
<tr>
<td>DRSETPS</td>
<td>Data Register Set Pulse</td>
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<tr>
<td>DRSETBF</td>
<td>Data Register Set Buffer</td>
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</tr>
<tr>
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<tr>
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<td>83-4</td>
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<tr>
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<td>83-2, 83-5, 27-1, 27-3</td>
</tr>
<tr>
<td>ENDSTR</td>
<td>End Strobe</td>
<td>83-1, 83-5, 27-1, 27-3</td>
</tr>
<tr>
<td>EOWD</td>
<td>End of Word</td>
<td>83-1</td>
</tr>
<tr>
<td>INIT</td>
<td>Initiate</td>
<td>83-1, 83-5, 27-1</td>
</tr>
<tr>
<td>INIT-A</td>
<td>Initiate A</td>
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</tr>
<tr>
<td>INIT-C</td>
<td>Initiate C</td>
<td>27-1, 27-2, 27-3</td>
</tr>
<tr>
<td>INTA</td>
<td>Interrupt</td>
<td>27-1</td>
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<tr>
<td>INTACK</td>
<td>Interrupt Acknowledge</td>
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<tr>
<td>INTPIN</td>
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</tr>
<tr>
<td>INTPOT</td>
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<td>27-1</td>
</tr>
<tr>
<td>INTR</td>
<td>Interrupt Received</td>
<td>27-1</td>
</tr>
<tr>
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<td>27-1</td>
</tr>
<tr>
<td>IORST</td>
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</tr>
<tr>
<td>LCC0 - LCC11</td>
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<td>83-4</td>
</tr>
<tr>
<td>LCCA - LCCM</td>
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<td>83-4</td>
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<tr>
<td>LSTWD</td>
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<tr>
<td>MAI N</td>
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<td>27-1, 27-2</td>
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<td>MASET</td>
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<td>MSKO</td>
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<td>PERM ADDRESS</td>
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<td>83-1</td>
</tr>
<tr>
<td>POR</td>
<td>Power ON Reset</td>
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</tr>
<tr>
<td>PTY</td>
<td>Parity Bit</td>
<td>83-2, 83-5</td>
</tr>
<tr>
<td>PTYCYL</td>
<td>Parity Cycle</td>
<td>83-2, 83-4</td>
</tr>
<tr>
<td>PTYCYL-</td>
<td>Parity Cycle</td>
<td>83-5</td>
</tr>
</tbody>
</table>

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# TABLE 4-1. SIGNAL DEFINITION AND MNEMONICS (continued)

<table>
<thead>
<tr>
<th>Mnemonic Term</th>
<th>Signal Definition</th>
<th>Location*</th>
</tr>
</thead>
<tbody>
<tr>
<td>PU</td>
<td>Pull Up</td>
<td>83-2</td>
</tr>
<tr>
<td>RD</td>
<td>Read</td>
<td>27-1, 27-3</td>
</tr>
<tr>
<td>RDDATA,</td>
<td>Read Data</td>
<td>83-1</td>
</tr>
<tr>
<td>RDDATA-</td>
<td>Read Latch</td>
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</tr>
<tr>
<td>RDL, RDL-</td>
<td>Read Operation</td>
<td>83-1, 83-5, 27-1</td>
</tr>
<tr>
<td>RDSC-</td>
<td>Read Sync F/F</td>
<td>83-1</td>
</tr>
<tr>
<td>RDST-</td>
<td>Read Start</td>
<td>27-1</td>
</tr>
<tr>
<td>RQENB, RQENB-</td>
<td>Request Enable</td>
<td>27-1, 27-3</td>
</tr>
<tr>
<td>RSGOA-</td>
<td>Error on drawing S/B RSGO</td>
<td>83-1</td>
</tr>
<tr>
<td>RSGO-</td>
<td>Read Sector Go</td>
<td>83-1, 27-1</td>
</tr>
<tr>
<td>RST-</td>
<td>Reset</td>
<td>83-1, 83-4, 83-5, 27-1, 27-2</td>
</tr>
<tr>
<td>RWOP</td>
<td>Read/Write Operation</td>
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</tr>
<tr>
<td>SA10 - SA13</td>
<td>Subsector Address 0 through 3</td>
<td>83-1, 83-4</td>
</tr>
<tr>
<td>SALOS-</td>
<td>Subsector Address Load One-Shot</td>
<td>83-1, 83-3, 27-1, 27-2</td>
</tr>
<tr>
<td>SARST</td>
<td>Sector Address Reset</td>
<td>83-4</td>
</tr>
<tr>
<td>SARSTA</td>
<td>Should be SARST</td>
<td>83-1</td>
</tr>
<tr>
<td>SCLK</td>
<td>Sector Clock</td>
<td>83-1, 83-5</td>
</tr>
<tr>
<td>SCOPCK</td>
<td>Sector Continue Operation Clock</td>
<td>83-2, 83-5, 27-1, 27-3</td>
</tr>
<tr>
<td>SCSYN</td>
<td>Sector Clock Sync</td>
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</tr>
<tr>
<td>SELB</td>
<td>Select Busy</td>
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</tr>
<tr>
<td>SELD</td>
<td>Select Done</td>
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<tr>
<td>SEQL, SEQL-</td>
<td>Sector Equal</td>
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<tr>
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</tr>
<tr>
<td>SR00 - SR15</td>
<td>Shift Register Bit Zero - Fifteen</td>
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<tr>
<td>SRCI</td>
<td>Shift Register Clock</td>
<td>83-1, 83-3</td>
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<td>SRCWKW</td>
<td>Shift Register Clock Write</td>
<td>83-1, 83-5</td>
</tr>
<tr>
<td>SRL-</td>
<td>Shift Register Load</td>
<td>83-1, 83-3, 83-5</td>
</tr>
<tr>
<td>SRLDENW-</td>
<td>Shift Register Load Enable Write</td>
<td>83-1, 83-3</td>
</tr>
<tr>
<td>SRLKRR-</td>
<td>Shift Register Clock Read</td>
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</tr>
<tr>
<td>STATIN</td>
<td>Status In</td>
<td>83-2, 27-1, 27-2</td>
</tr>
<tr>
<td>STCLD-</td>
<td>Word Transfer Counter Load Used only with a DOC Instruction</td>
<td>27-1, 27-2</td>
</tr>
<tr>
<td>STRT</td>
<td>Start</td>
<td>27-1</td>
</tr>
<tr>
<td>TA0 - TA8</td>
<td>Track Address Zero - Eight</td>
<td>83-4, 83-5, 83-2</td>
</tr>
<tr>
<td>TMERRD-</td>
<td>Timer Error Read</td>
<td>83-1</td>
</tr>
<tr>
<td>TMERWR</td>
<td>Timer Error Write</td>
<td>83-1</td>
</tr>
<tr>
<td>TSASET</td>
<td>Track/Sector Address Set</td>
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</tr>
<tr>
<td>UACHG-</td>
<td>Unit Address Changing</td>
<td>83-1, 83-4</td>
</tr>
<tr>
<td>USEL2</td>
<td>Unit Select Two</td>
<td>83-4</td>
</tr>
<tr>
<td>USEL1</td>
<td>Unit Select One</td>
<td>83-4</td>
</tr>
<tr>
<td>USEL3</td>
<td>Unit Select Three</td>
<td>83-4</td>
</tr>
</tbody>
</table>

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TABLE 4-1. SIGNAL DEFINITION AND MNEMONICS (continued)

<table>
<thead>
<tr>
<th>Mnemonic Term</th>
<th>Signal Definition</th>
<th>Location*</th>
</tr>
</thead>
<tbody>
<tr>
<td>USEL0-</td>
<td>Unit Select Zero</td>
<td>83-4</td>
</tr>
<tr>
<td>WCLK</td>
<td>Write Clock Out</td>
<td>83-1, 83-5</td>
</tr>
<tr>
<td>WCLKDI</td>
<td>Write Clock Out Delay</td>
<td>83-1, 83-5</td>
</tr>
<tr>
<td>WCO-WC3</td>
<td>Word Count Zero - Word Count Three</td>
<td>83-1</td>
</tr>
<tr>
<td>WEO-WE3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRL, WRL-</td>
<td>Write Latch</td>
<td>83-1, 83-5</td>
</tr>
<tr>
<td>WROP</td>
<td>Write Operation</td>
<td>83-1, 83-3, 83-5, 27-1, 27-2, 27-3</td>
</tr>
<tr>
<td>WRITE-</td>
<td>Write</td>
<td>83-5, 83-6</td>
</tr>
<tr>
<td>WRSC, WRSC-</td>
<td>Write Sync flip-flop</td>
<td>83-1</td>
</tr>
<tr>
<td>WRT-</td>
<td>Write to Disc</td>
<td>83-6</td>
</tr>
<tr>
<td>WSGO, WSGO-</td>
<td>Write Sector Go</td>
<td>83-1, 27-1</td>
</tr>
<tr>
<td>WTST-</td>
<td>Write Start</td>
<td>27-1</td>
</tr>
</tbody>
</table>

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4-5 OVERALL SYSTEM THEORY OF OPERATION

The 8011 Disc Memory Controller is normally connected to the Nova Computer I/O bus along with other peripheral devices such as magnetic tape units, paper tape readers, line printers, etc. Each device connected to the I/O bus is assigned a device code (octal) and a mnemonic designation. The controller has device code 20 or 60 with mnemonic DSK. The computer processor selects a device by placing the device code (bits 10 through 15 of the I/O instruction word) on lines D50 through D55 during the execution of an I/O instruction. Only the selected device responds to the control signals generated during the instruction.

4-6 DATA-OUT AND DATA-IN TRANSFERS

For data-out transfers, the controller is selected for operation by the DOA and DOB instructions that are issued by the processor. The DATOA and DATOB signals are sent from the processor to the adapter PC board as a result of the instructions. The IOPLS signal sent from the processor to the PC board adapter, PC board causes the selected busy (SELB) signal from the adapter board to the processor to become true.

The DCHP signal is sent from the processor to the adapter board at the start of the data cycle. When the RQENB signal is sent from the processor to the adapter board, the DCHR signal to the processor becomes true.

The address information placed on the data lines as a result of the DOA instruction is sent to the unit, track and sector registers of the controller. The initial address information of the DOB instruction is sent to the core memory address register on the adapter board. The DATOA signal causes the unit, track and sector registers to be loaded, and the DATOB signal causes the core memory address register to be loaded.

The DCHA signal sent by the processor to the adapter PC board causes the DCHMO signal to the processor to go high, indicating a data-out transfer. This also causes the initial address to be read out from the core memory address register to the processor.
The sector address is applied to the sector equal detection circuit on the formatter board where it is compared with the information from the current sector location counter.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>TABLE</th>
<th>SYMBOL</th>
<th>TABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INVERTER</strong></td>
<td>![Inverter Symbol]</td>
<td><strong>NOR</strong></td>
<td>![NOR Symbol]</td>
</tr>
<tr>
<td>![Inverter Diagram]</td>
<td>$X = \overline{A}$</td>
<td>![NOR Truth Table]</td>
<td>$X = A \oplus B$</td>
</tr>
<tr>
<td><strong>AND</strong></td>
<td>![AND Symbol]</td>
<td><strong>EXCLUSIVE OR</strong></td>
<td>![XOR Symbol]</td>
</tr>
<tr>
<td>![AND Diagram]</td>
<td>$X = AB$</td>
<td>![XOR Truth Table]</td>
<td>$X = AB \oplus \overline{AB}$</td>
</tr>
<tr>
<td><strong>NAND</strong></td>
<td>![NAND Symbol]</td>
<td><strong>D-TYPE FLIP-FLOP</strong></td>
<td>![D-Type Flip-Flop]</td>
</tr>
<tr>
<td>![NAND Diagram]</td>
<td>$X = \overline{AB}$</td>
<td>![D-Type Flip-Flop Truth Table]</td>
<td>![D-Type Flip-Flop Diagram]</td>
</tr>
<tr>
<td><strong>OR</strong></td>
<td>![OR Symbol]</td>
<td><strong>JK FLIP-FLOP</strong></td>
<td>![JK Flip-Flop]</td>
</tr>
<tr>
<td>![OR Diagram]</td>
<td>$X = A \oplus B$</td>
<td>![JK Flip-Flop Truth Table]</td>
<td>![JK Flip-Flop Diagram]</td>
</tr>
</tbody>
</table>

Figure 4-1. Logic Symbols
The data word from the processor is sent through the adapter board to data selectors on the formatter board. It is then transferred through these data selectors to the data register to a 16-word buffer and then to the shift register.

When the sector address applied to the sector equal detection circuit is equal to the sector address on the disc, the data is serially shifted out of the shift register and is written on the disc when the WRITE signal from the formatter board is applied to the disc unit.

At the end of the data-out transfer (256 words) when the last data word has been written, the selected done (SELD) signal from the adapter board to the processor becomes true.

For data-in transfers, the controller is selected for operation and the DOA and DOB instructions are issued by the processor. The STRT signal sent from the processor as a result of one of the instructions is applied to the adapter PC board. This causes the SELB signal to the processor to become true.

The DCHP signal is sent by the processor to the adapter board at the beginning of the data cycle. When the RQENB signal is sent from the processor, the DCHR signal to the processor becomes true. The unit, track and sector address information is loaded into the unit, track and sector registers when the DATOA signal is sent from the processor. The initial address information is loaded into the core memory address register when the DATOB signal is sent from the processor.

The sector address information is applied to the sector equal detection circuit where it is compared with the information from the current location counter. When the addresses are equal, the READ signal to the disc unit becomes true. At approximately 16-bit times later, the first bit of data is read from the disc.

The bits read from the disc are serially shifted into the shift register until a 16-bit word is formed. The data word is then transferred in parallel through the 16-word buffer to the data register through the adapter PC board where it is strobed to the processor when the DATIA signal is sent from the processor to the adapter board.

When the last (256 words) of the data-in transfer has been transferred to the processor, the SELD signal to the processor becomes true.

The preceding paragraphs pertained to sector operation. When subsector operation is used, the word transfer counter is loaded at the start of a data transfer with 12 data bits (04 through 15). These bits define the length of operation in terms of subsectors. A more detailed theory of operation for write and read operations is given in paragraphs 4-57 and 4-58.

4-7 PROGRAM INTERRUPT

When the processor uses a mask to set up the program interrupt, it executes the same sequence as for a data-out transfer, except that it generates MSKI (in place of the DATOA signal) to set up the interrupt disable flags in all devices according to the information on the data lines.

When the controller and the other devices connected to the I/O bus complete an operation, they set their don flag. At the beginning of every memory cycle, the processor generated the request enable (RQENB) signal to allow all devices on the bus to request
program interrupts or channel access. If the done flag of a device is set and its interrupt disable flag is clear, the leading edge of the RQENB pulse is used to set the INT REQ flip-flop to ensure sufficient time for the serial INTP function to be completed before the processor attempts to discover which device has priority. The processor issues INTP IN to a device only if there is no INT REQ flip-flop set in a device closer to the processor on the I/O bus. The closest device that has its INT REQ flip-flop set terminates the INTP signal.

The processor acknowledges an interrupt by generating the INTA signal. If a device receives the INTA signal while it is also receiving the INTP signal and its INT REQ flip-flop is set, it places its device code on DATA 10 through DATA 15 lines to the processor. The processor strobes the data containing the device code into the specified accumulator at the end of the INTA level.

During an interrupt, the processor can also determine which device requires service by sensing the busy or done signals. When the processor is to use the same device again after interrupt, it clears the done signal so that the device does not immediately request an interrupt when the interrupt system is reinitiated and its interrupt disable signal is cleared. When the done signal is cleared, it causes the INT REQ flip-flop to be cleared. This disables the INTR signal, preventing the device from requesting an interrupt.

4-8 DATA CHANNEL REQUESTS

The sequence of events that occur during a data channel request are similar to the events that occur during an interrupt request. Each device connected to the I/O bus has a DCH SYNC flip-flop which controls the logic state of its done signal to the processor. Each device has a DCH REQ flip-flop (data channel request flip-flop) and a net for transmitting the serial priority signal to the next device. When a device receives the input DCHP signal (data channel priority) and its DCH REQ flip-flop is clear, it transmits the DCHP signal to the next device. The first device that has its DCH REQ flip-flop set terminates the DCHP signal. When this flip-flop is set, the next RQENB signal from the processor sets the DCH REQ flip-flop in the device. This causes its DCHP signal to the processor to become true. The DCH REQ flip-flop is set on the leading edge of the RQENB signal to ensure sufficient time for the serial DCHP function to be completed.

When a device is waiting for access to the data channel, the processor generates DCHA after the RQENB signal goes false in the final cycle of an instruction. The leading edge of the DCHA signal sets the DCH SEL flip-flop in the nearest device that is requesting service. This device must be receiving the input DCHP signal and have its DCH REQ flip-flop set. The device that has its DCH SEL flip-flop set places the memory address to be used for data channel access on data lines 1 through 15 to the processor for the duration of the DCHA signal. When the DCHA signal goes false, the processor strobes the address into its memory address register.

When the DCH SEL flip-flop is set in the controller, the DCHMO signal to the processor is enabled. This signal becomes true (low) for a data-in (read) transfer and becomes true (high) for a data-out transfer (write). The DCHA signal that sets the DCH SEL flip-flop also clears the DCH SEL flip-flop in all other devices, thus preventing conflict with other cycles.

The leading edge of the DCHA signal also clears the DCH SYNC flip-flop (done flag). When the next RQENB signal is generated by the processor, the leading edge of the RQENB signal sets request flip-flops in other devices on the I/O bus while it clears
the DCH REQ flip-flop in the device previously having access to the data channel.

When the DCHA signal goes false during a data-in transfer from the controller, the processor generates the DCHI signal and the final instruction cycle is extended while the DCHI signal holds the contents of the data register of the controller on the I/O bus. When the DCHI signal becomes false, the processor strobes the data into its memory buffer and begins the next processor cycle by generating the REQ NB signal which causes the DCHR signal to the processor to go false. During the data-out (write) cycle, the processor stores the data in the addressed memory location.

When the DCHA signal goes false during a data-out transfer to the controller, the processor begins the next cycle by generating the RQENB signal which causes the DCHR signal to become false. During the data-out (write) cycle, the processor retrieves a data word from the addressed memory location and brings it into the memory buffer. The data-out cycle is completed when the processor places the contents of the memory buffer on the data lines to the controller and generates the DCHO signal to load the data word into the controller data register.

4-9 MULTIPLE REQUESTS FOR DATA CHANNEL ACCESS

If the DCH SYNC flip-flop in the device that is being serviced is clear (done signal false) at the leading edge of the RQENB signal in the data channel cycle, the RQENB signal clears the DCH REQ flip-flop in that device. However, if the DCH SYNC flip-flop is already set again (done signal true), the DCH REQ flip-flop stays set. This causes a second data channel access request to be initiated by the device. In either case, the RQENB signal sets the request flip-flops in any other device on the I/O bus that may require service.

If there is a second request from a device, the processor generates a second DCHA signal after completing whatever operations are necessary for the first data channel access. For a data-in transfer, the second DCHA signal is generated when RQENB for the second request becomes false. This occurs preceding the transfer of data. For a data-out transfer, the second DCHA signal is generated following the transfer of data. The second DCHA signal sets the DCH SEL flip-flop in all other devices. The second DCHA signal also initiates the operations necessary to prepare the third transfer of data. Multiple data channel requests occur every other RQENB.

4-10 WRITE OPERATION

A block diagram of a typical write operation is given in figure 4-2. For simplicity, the interrupt signals are not shown. The controller is selected for operation by the processor, and the DOA and DOB instructions and the DOTOA and DATOB signals are generated as a result of the instructions. The IOPLS signal, generated by the processor in accordance with the instruction, is applied to the adapter PC board and sets the WROP flip-flop. This causes the SELB (selected busy) signal to the processor to become true. The DONE flip-flop is reset by the INIT C signal at the same time that the WRIP flip-flop is set. The START signal also becomes true at this time.

The DCHP signal is generated by the processor at the start of the data cycle. When the RQENB signal is generated by the processor, the DCH REQ flip-flop is set, and the DCHR signal to the processor goes low. This also enables the DCH SEL flip-flop. The address information, placed on the data lines as a result of the DOA instruction, is applied through the processor data bus of the adapter board and through the formatter/adapter board common bus to the unit, track and sector registers on the formatter PWBA. The DOB initial address information is applied through the processor data bus to the core memory address register on the adapter board. The unit, track and sector address information is
Figure 4-2. Write Operation Block Diagram
loaded into the unit, track and sector registers when the DATOA signal from the processor causes the TSASET signal to become true. The core memory address register is loaded when the DATOB signal from the processor causes the TSASET signal to become true. The core memory address register is loaded when the DATOB signal from the processor causes the MASET signal to become true. The DCHA signal generated by the processor sets the DCH SEL flip-flop. This causes the DCHADG signal to go low (true) and the DCHMO signal to the processor to go high, indicating a data-out (write) operation. The DCHADG signal is applied to the register on the data processor bus that contains the initial address from the core memory address register. This causes the initial address to be read out to the processor. The low DCHADG signal also presets the DCH BSY flip-flop, enabling data transfer.

When the DOC instruction is used for subsector operation, the subsector address is loaded into the subsector address register when the DATOC signal from the processor causes the STCLD signal to go true, presetting the DOCX flip-flop. For this operation, the contents of accumulator bits 4 through 15 are loaded into the word transfer counter. The 12-bit number expresses the length of operation in terms of numbers of subsectors. This number is a number in two's complement. The total number of words transferred is that which is specified by the subsector number.

The unit track addresses are sent to the disc memory units, and the sector n address is applied to the sector equal detection circuit where it is compared with the information from the current location counter.

The data word from the processor is applied to the data selectros and registers U15, U16, U17, and U18 through the processor data bus and the adapter/formatter PWBA common bus. During the write operation, the WROP signal is high and causes a low input to be applied to the WORD SELECT (pin 10) input. The data selectors and registers are quadruple two-input multiplexers each of which select four input DBO data lines from the formatter/adapter common bus when the WORD SELECT input is low. Each of the data selectors and registers is clocked by the inverted DRSET clock pulse which is derived from the DCHO pulse from the processor. When the data selectors and registers are clocked by the inverted DRSET clock pulse, the DBO data is transferred to data selectros U29, U30, U31, and U32.

Data selectros U29, U30 and U32 are quadruple two-line to one-line data selector/multiplexers. Since the STROBE input of all of these data selectors is connected to ground, the high WROP input to the SELECT terminal of each data selector causes its four DBO input signals to be transferred to its output. This applies the DBO data signals to the 16 word read/write memories U43, U44, U45 and U46. The read/write memories store a total of 16 words of 16 bits per word. The address signals are applied to the memories from the bufferprocessor access counter through the buffer address switch. Since the MEM terminal of each memory is connected to ground, the BFLDPS signal which goes low for each word transferred during a write operation causes the four bits of DBO data at the input of each memory to be written into the 16 word memory at the address established by the buffer address signals. The words are loaded into the memories until the memories are full. With the buffer full and a sector pulse, the WSGO signal goes low. This selects the buffer disc access counter for operation through the buffer address selector switch. The first word is then read out of the memories and appears at the output in the complement form. This causes the DBO data to be transferred to the 4-bit shift registers U57, U58, U59, and U60. The DBO data is loaded into the shift registers by the low SRLD clock when the SRCL clock pulse goes high. When each word is written into the memories the buffer contents counts up. When each word is read from the memories, the counter counts down. During the write operation, the sector bit and word control logic count the number of bits written and generates control signals.
When the sector address applied to the sector equal detection circuit is equal to the selector address on the disc, the write signal flip-flop is conditioned high at the same time that the SRLD signal goes high. The loading of the first word into shift registers U57 through U60 causes the first bit (SROO) to be applied in the complimentary form to the write data logic in the disc interface circuit. This conditions the WRITE DATA flip-flop in accordance with the logical state of the bit. When the WRITE DATA flip-flop is clocked, the WRITE signal flip-flop is also clocked causing the WRITE signal to the disc memory unit to go low. The bit then appears on the write data line to the disc memory unit where it is written on the disc. Timing for the transfer to the write data line is derived from the WRITE CLOCK OUT and SECTOR CLOCK pulses from the disc memory unit.

With each positive pulse to the SRCL input, the data is shifted serially from shift register U60 toward SROO of shift register U57 until all of the 16 bits have been written on the disc. The entire process is repeated using the buffer/disc access counter to read words from the memories and the buffer/processor counter to write words into the memories until one sector (256 words of data) has been written. If the DOC instruction is used, the number of subsectors written is specified by the instruction.

At the beginning of each data channel cycle, the processor issues a DCHA pulse to the adapter PC board. The DCHADG pulses, that clock the word transfer counter, are generated by the DCHA pulses during the write operation. When each word is transferred from the processor, the counter is clocked in the count-up direction. If subsector operation is not used, the counter is programmed to count 256 words (one sector). When 256 words have been transferred, the END flip-flop is set on the adapter board. The END signal is ANDed with BFE MTY signal from the buffer contents counter and generate the ENDWEN signal that is ANDed with the WROP signal and ENDSTR one-shot when it is triggered. When the ENDSTR one-shot times out, it causes a low to high transition at the clock input of the done flip-flop. When the flip-flop is set, the selected done (SELD) signal to the processor goes low (true) and the select busy (SELB) signal goes high (false).

When subsector operation is used, accumulator bits 4 through 15 that are loaded into the word transfer counter determines the length of operation in terms of subsectors.

The DCHADG pulses, that clock the word transfer counter, also clock the core memory address counter in the upward direction. The contents of this counter can be read out to the processor as means of checking the number of words transferred or for diagnostic purposes.

At the end of each subsector, a 16-bit cyclic code word and odd parity bit are generated by the formatter PC board. The 16-bit cyclic code word is generated by a cycle code generator and shifted serially to the data interface circuit. The bits are gated to condition the WRITE DATA flip-flop (WRITE DATA signal to the disc memory unit) by the setting of the CCYL flip-flop that is set after the last word counter generates the LSTWD signal. The odd parity bit is generated by a parity bit generator and is gated to condition the WRITE DATA flip-flop when the PTYCYL flip-flop is set after the 16th bit of the cyclic code word.

4-11 ERRORS IN WRITE MODE

Write Error. When a write operation is initiated by the processor and the selected track-sector is write protected, the ENDER signal goes low (true) and the WPTER flip-flop is set. The ENDER signal sets the done flip-flop, causing the SE LD (selected done) signal to the processor to go low (true). This causes the SELB (selected busy) signal to the processor to go high (false), and the INTR (interrupt request) signal to go low (true) if the INT DSB (interrupt disable) flip-flop is not set. The WPTER and WPTER- signals are applied to
the error register on the formatter/adapter PC board common bus. This sets bit 15 and error bit 11 to a logical 1.

No Such Disc. When the disc or track selected by the processor is not available on the system, the ILAER flip-flop is set, and the ENDER signal goes low (true). The ENDER signal sets the DONE flip-flop, causing the SELD signal to the processor to go low (true) and the SELB signal to go high (false). The true ENDER signal also causes the INTR signal to go low if the INT DSB flip-flop is not set. The ILAER and ILAER- signals are applied to the error register on the formatter/adapter board common bus. This sets bit 15 and error bit 13 to a logical 1.

Disc Fail. If the disc becomes not ready or the system is hung during the write operation, the DSC FAIL flip-flop is set. The ENDER signal goes low (true) if the system is hung. The ENDER signal sets the DONE flip-flop, causing the SELD signal to the processor to go low and the SELB signal to go high. The true ENDER signal also causes the INTR signal to go low (true) if the INT DSB flip-flop is not set. The DISC FAIL and DSC FAIL signals are applied to the error register formatter/adapter PWBA common bus. This sets bit 15 and the 10 error bits to a logical 1.

Data Late. When the data channel fails to respond in time to a request for access, the TMER flip-flop is set. The TMER and TMER signals are applied to the error register on the formatter/adapter board common bus. This sets bit 15 and error bit 12 to a logical 1.

The contents of the error register is read when the processor issues a DIA instruction to read the status of the disc memory system.

4-12 READ OPERATION

A block diagram of a typical read operation is given in figure 4-3. For the sake of simplicity, the interrupt signals are not shown. The 8010 Disc Memory Controller is selected for operation by the processor as described in paragraph 4-3. There are three types of read operations. These consist of read from a disc memory unit, read the status of the controller, and read the contents of the core memory address register. The theory of operation of these three types of read operations is described in paragraphs that follow.

4-13 Read From Disc Memory Unit

The DOA and DOB instructions are issued by the processor, and the STRT signal is generated as a result of one of the instructions and applied to the 8010 adapter. This sets the RDOP flip-flop while causing the START and INIT C and INIT D signals to go low. The INIT C signal resets the DONE flip-flop. The setting of the RDOP flip-flop causes the SELB signal to the processor to go low (true).

The unit, track and sector address information is loaded into the unit, track and sector registers when the DATOA signal from the processor is applied to the Nova adapter PWBA and causes the TSASET signal to go low. The core memory address register is loaded when the DATOB signal from the processor causes the MASET signal to go low.

When subsector operation is used, the subsector address is loaded into the subsector address register when the DATOC signal from the processor causes the STCLD signal to go low, presetting the DOCX flip-flop. The low STCLD signal also loads bits 4 through 15 into the word transfer counter. The 12-bit number expresses the length of the operation in terms of subsectors.
Figure 4-3. Read Operation Block Diagram
The unit select and track address information is sent to the disc memory units, and the sector address information is applied to the sector equal detection circuit where it is compared with the information from the current location counter. When the addresses are equal, the READ signal flip-flop is set and the READ signal to the disc memory unit goes low. At approximately 16 bit times later, the first bit of data is read from the disc.

The first bit of data is applied to the four-bit shift register U60. During the shift operation, the SRLD signal is held high and the first bit of data is entered into U60 when the SRCL clock pulse occurs. The serial shifting process from U57 to U57 is repeated with each clock pulse until shift registers U57 through U60 contain the first data word (16 bits) read from the disc.

During the read operation, the WROP signal is low producing a low input at the SELECT inputs of U29 through U32. This selects the SR data input lines from shift registers U57 through U60. Since the STROBE input of U29 through U32 is grounded, the SR data is transferred in parallel through data selectors U29 through U32 to the input of memories U43 through U46.

Since the MEM input of memories U43 through U46 is grounded and the BFKDR signal goes low when 16 bits are in the shift register, the low signal applied to the WRITE ENABLE input of the memories causes the SR read data to be loaded into the memories since the address is applied from the buffer/disc access counter through the selector switch. When the BFLDR pulse goes high, the buffer disc access counter is advanced, after a delay, to the next higher address.

After the first word is written in the memories, through multiplexers U29 through U32, the buffer/processor access counter is selected and reads the complement of the word from the memory. This applies the word to data selectors U15 through U18. After a delay the buffer/processor access counter is advanced when the first DRSETBF low pulse goes high.

During the read operation the WROP signal is low and causes a high input at the WORD SELECT input of U15 through U18. This selects the BF00 through BF15 inputs from memories U43 through U46. The data is clocked to the outputs of U15 through U18 DRSET pulse that is derived from the first DRSETBF pulse. This pulse is generated as a result of read, buffer registers are empty, and data register not full. The DRSETBF pulses that follow are generated as a result of the data register being emptied by the DCHI signals from the processor. This is where the RQENB, DCHR, DCHPIN and DCHMO should be. If the first DCHI signal does not arrive immediately, loading of the memories still continues. When a word is loaded into the memories, the buffer contents counter counts down. During the read operation, the sector bit and word control logic count the number of bits read and generate control signals.

The outputs from U15 through U18 are applied to the data register on the formatter/adapter PWBA common bus. During the read operation, the DRGAT signal goes low when the RDOP flip-flop is set and DATIA signal is applied from the processor. The low DRGAT signal strobes the data word through the register to the formatter/adapter board common bus. The data word passes through the formatter/adapter PWBA common bus to the data register on the processor data bus. The low DCHIN signal derived from the DCHI signal from the processor strobes the data word through the register to the processor.

The entire read process is repeated for each data word cycle code word and parity bit read from the disc. At the end of each subsector the cyclic code word and the parity bit are read and a read error check is performed. During the read operation, the core memory
address register counter and the word transfer counter are clocked by the DCHADG pulses that are derived from the DCHA pulse from the processor. At the beginning of each data channel cycle, the processor generates at DCHA pulse and applies it to the data channel transfer control circuit on the adapter board. When the length of operation is in terms of sectors, the core memory address register counter provides the count for setting the END flip-flop. The word transfer counter is advanced with each DCHA pulse until 256 words have been transferred. If the BFEMTY signal from the buffer contents counter is high when the 256 count has been reached, the END signal flip-flop is set through its preset input. The END signal is ANDed with the RDOP and DRCNC signals that are caused to be derived from the processor by DCHI signal. When the DCHI signal goes high, the resultant signal sets the DONE flip-flop, and the SELD signal to the processor then goes low.

4-14 ERRORS IN READ MODE

No Such Disc. When the disc or track selected by the processor is not available on the controller, bit 13 is set for a logical 1, SELD signal to the processor goes low, SELB signal to the processor goes high, and an interrupt request is generated by the formatter/controller logic boards in the same manner as for No Such Disc error during a write operation (paragraph 4-11).

Disc Fail. If the disc becomes not ready or the system is hung during a read operation, the DSK FAIL flip-flop is set. The DSK FAIL and DSK FAIL- signals are applied to the error register on the formatter/adapter board common bus. This sets a logical 1 bit in bit 10 of the error bits and also sets a logical 1 in bit 15. The ENDER signal goes low if the system is hung. The ENDER signal sets the DONE flip-flop causing the SELD signal to the processor to go low and the SELB signal to go high. The true ENDER signal also causes the INTR signal to go low if the INT DSB flip-flop is not set.

Data Late. When the data channel fails to respond in time to a request for access during a read operation, the TMER flip-flop is set. The TMER and TMER- signals are applied to the error register on the formatter/adapter board common bus. This sets a bit 15 and error bit 12 to a logical 1.

Data Error. If the cyclic code word or parity bit read from the disc differs from the code word and parity bit computed by the read check circuitry for the data in the sub-sector, the RDER flip-flop is set. The RDER and RDER- signals are applied to the error register on the formatter/adapter board common bus. This sets bit 15 and error bit 14 to a logical 1.

4-15 Read Status of Disc Memory System

The error register on the formatter/controller board common bus contains the errors (if any) from the previous operation. The six errors that the register may contain are described in paragraphs 4-11 and 4-14.

To read the status of the disc memory system, the processor issues a DIA instruction. The DATIA signal applied to the adapter PC board as a result of the instruction causes the STATIN signal to go high (true). The STATIN pulse strobes the contents of the error register through the formatter/adapter board common bus to the processor data bus. On the processor data bus, the inverted STATIN pulse strobes the error bits to the processor.
4-16 Read Contents of Core Memory Address Register

One of the data registers on the processor data bus contains the inputs from the core memory address register on the adapter PC board. The core memory address register bits from the processor. During a write or read operation, the counter is advanced by a DCHADG pulse at the beginning of each data cycle.

To read the contents of the core memory address register, the processor issues a DIB instruction. The DATIB signal, generated by the processor as a result of the instruction, is applied to the adapter board and causes the MAIN signal to go low. The MAIN signal is applied to the register on the data processor bus that contains the inputs from the core memory address register. This causes the contents of the register to be read out to the processor. If the system is busy when the DIB instruction is issued, the contents of the core memory address register is presented as logical 0's.

4-17 DIAGNOSTIC MODE

In the diagnostic mode of operation, the processor issues a DOB instruction containing a logical 1 in accumulator bit 0. This places the controller in the diagnostic mode. The processor then transfers 16 words, using the memories U43 through U46 as described in the write operation in paragraph 4-10. During the diagnostic mode of operation the buffer/processor access counter supplies addresses to the memories through the buffer address switch. The 16 words are then read back to the processor through the data selectors and registers U15 through U18 as described in the read operation of paragraph 4-12. To read the 16 words out of the memories, the write enable input is held high and since the memory enable signal is grounded, the words are read out of the memories when the address signals are applied from the buffer address switch.

4-18 ADAPTER BOARD DETAILED CIRCUIT DESCRIPTION

The following paragraphs describe the logic circuits within the adapter PC board of the controller. The information contained in the descriptions is taken from the schematic diagram 1940027, sheets 1 through 3.

4-19 INITIATION AND DONE CONTROL (1940027, SHEET 1)

The initiation and done control logic contains the logic for selecting the 8010 Disc Memory System for operation and the logic for the various initiation control signals from the processor. It also contains the WROP and DROP flip-flops that control the SELD signal to the processor, the DONE flip-flop that controls the loading of the word transfer counter and subsector address register during subsector operation.

4-20 Device Selection

The DS0- through DS5- signals are applied from the processor to select the 8010 Disc Memory System for operation. To select the disc memory system, DS0- must be high, DS1 must be low, and DS2 through DS5- must be high. This code (010 000) corresponds to octal 20, the code for the disc memory system. With this code applied from the processor, the output from U41-13 goes high. This high output is applied to U15-3 and U16-13, enabling the DATIA and CLR signal gates. This output is also applied to U27-9. If neither the WROP or RDOP flip-flop is set, the input to U27-10 is high. This causes the output from U27-8 to go high. This high output is applied to U3-3, U17-5, U17-13, U17-11, U16-11 and U16-3. This enables the DATOA, DATOB, DATOC, IOPLS, STRT and SATIB signal gates.
The high output from U41-13 is also applied to U5-13 and U5-5, enabling the SELB- and SELD- signal gates.

4-21 Initiation Logic

The IOPLS signal (write operation) applied to U17-9 or the STRT signal (read operation) applied to U16-9 causes the INIT signal at U53-8 to go low, the INIT D signal at U40-12 to go high and the INIT C- signal at U48-8 to go low. The inverted INIT C signal at U48-8 resets the DONE flip-flop at U56-13 causing the SELD- signal to the processor to go high (false). The IOPLS or STRT signal also causes the START signal at U4-11 to go high. The STRT signal generates the RDST- signal that sets the read latch U55-8 and U42-10 signal circuit during a diagnostic read operation.

On the trailing edge of the IOPLS or STRT pulse, the WROP or RDOP flip-flop is set. This causes the SELB signal at U5-11 to go low (true). This signal is applied to the processor to indicate selected busy (busy flag).

During a write operation, the DATOA signal is applied to U3-5. The output at U3-6 goes low, causing the TSASET signal of driver U19-4 to go low. The TSASET- signal is used to load the unit, track and sector address registers with the address contained in the DOA instruction.

During a write operation, the DATOB signal is applied to U17-4. The output MASET- signal at U17-6 goes low. The MASET- signal is used to load the core memory address register with a starting core address contained in the DOB instruction.

When subsector operation is used, the DATOC signal is applied to U17-2 and the STCLD output at U17-12 goes low. The low STCLD output from U17-12 presets the DOCX flip-flop and the DOCXA signal at driver U22-2 goes high. The low output from U17-12 is the STCLD- signal that is applied to the word transfer counter to load bits 4 through 15 of the DOC instruction into the counter (specifying the length of operation in terms of subsectors). The DOCX signal at U56 is used to apply the subsector address register. The DOCX- signal and the START signal are ANDed at U59-11 and used to load the subsector address into the register.

When the status of the disc memory system is ready, the DATIA signal is applied as a result of the DIA instruction to U15-5. The output at U15-6 goes high, causing the STATIN signal at driver U19-2 to go high. The STATIN- signal strobes the contents of the error register on the formatter/adapter common bus to the processor data bus where the STATIN- signal strobes the error data to the processor.

When bits 8 and 9 (F) of the instruction contain a logical 1 (clear function) the signal is applied to U16-1. This causes the clear output at U16-12, and U27-3 to go low. This generates the INIT- signal at U53-8, the INIT-D signal at U40-12 and the INIT-C signal at U48-8. This clears the RDOP, WROP, DOCX, DONE, DCM, REQ and all other flip-flops that are cleared by the INIT signals. This also causes the SELB- signal to the processor to go false (high).

When the IORST signal is generated as a result of the instruction by the processor, or when the console RESET switch is pressed to clear all control flip-flops in all interfaces connected to the I/O bus, or at power turn on, the input to U4-9 goes high. The output from U4-8 goes low, generating the RST- signal. This also causes the output from U27-3 to go low, generating the INIT-, INIT-D and INIT-C signals. This resets all control flip-flops.
Done Control

The DONE flip-flop U56 is set at the end of a write operation or at the end of a read operation, and when a write error (write protect) occurs. No such disc error signal or disc fail error signal occurs during an operation.

At the end of a write operation, the END flip-flop is set on the Nova adapter PWBA. This causes the input to U28-1 to go high. If the BFEMTY signal from the buffer contents counter is high (memory buffer empty), the output from U28-3 goes low, causing a high input at U21-2. Since the WROP signal is high during the write operation, the input to U21-1 is high. If the ENSTR one-shot U64 has been triggered at the end of the parity cycle, the input to U21-13 goes high and the output at U21-12 goes low, enabling the DONE flip-flop input at U56-11. When the ENSTR one-shot times out, the transition from low to high at U56-11 sets the DONE flip-flop.

At the end of a read operation, the END flip-flop is set on the Nova adapter PWBA causing the input to U57-2 to go high. Since the RDOP signal is high during a read operation, the input to U57-1 is high. The DRCNC signal at U57-13 is derived from the DCHI signal from the processor. This causes the output from U57-12 to go low enabling the DONE flip-flop with a low input at its clock input U56-11. When the DCHI signal from the processor goes low (false), the transition from low to high at U56-11 sets the DONE flip-flop.

If a write protect error, no such disc error, or disc fail error occurs during an operation, the ENDER- signal at U15-10 goes low and then goes high, causing a low to high transition at the clock input U56-11 of the DONE flip-flop. This sets the DONE flip-flop.

During a diagnostic write operation, the WROP signal at U42-2 is low and the DIAGM- signal at U43-3 is low. This causes a high output from U42-1 that is applied to U55-4. When the BFFUL signal at U55-5 from the buffer condition decoder goes high at the count of 16, the output from U55-6 goes low, presetting the DONE flip-flop.

Write Sector Go Logic

When the DIAGM signal from the core memory address register is low (not diagnostic mode) and the BFFUL- signal from the buffer condition decoder is low (memory buffer full), the inputs to U42-12 and U42-11 are low. This causes the output from U42-13 to go high. This conditions write sector go flip-flop U49 with a high input at U49-12. If the read sector go flip-flop U49 is not set, the input to U44-5 is low, and since the write sector go flip-flop is reset, the input to U44-6 is also low. This causes the output at U44-4 to go high. When the SCOS (sector clock one-shot) is triggered by the SCSYN- pulse, the SCOPCK signal goes high. The high SCOPCK signal is applied to U57-10 and also causes the write sector go flip-flop U49 to be clocked through gate U20. This causes the WSGO-
signal at U57-8 to go low (true). When the SCOS one-shot times out, the WSGO- signal at U57-8 goes high (false). The write sector go flip-flop is reset by the INIT signal at U41-8 or by the high signal at U41-9 at the end of the write operation when the END and BFEMTY signals are both high. When doing more than one write, the first WSGO is generated by WRSC (low), RDSC (low) and SCSYN (low) which generate SCOS (low); which, in turn, generates SCOPCK (high) which generates WSGO (low). Subsequent WSGO signals are generated by LSTWD (high) followed by CCYL (high), PTYCYL (high), ENDSTR (low), and SCOPCK (high) which generates WSGO (low).

4-25 Read Sector Go Logic

When the RDOP signal at U4-1 (B3) is high and the BFEMTY signal from the buffer contents counter is high, the output from U4-3 goes low. This low output is applied to U42-5. If the DIAGM signal from the core memory address register is low, the read sector go flip-flop U49 is conditioned with a high input at U49-2. If the write sector go flip-flop U49 and the read sector go flip-flop U49 are both reset, the output from U44-4 goes high. When the SCOS one-shot in the end control circuit is triggered by the SCSYN pulse, the SCOPCK signal goes high. The high SCOPCK signal is applied to U57-4 and also causes the read sector go flip-flop to be clocked through gate U20. This causes the RSGO- signal at U57-6 to go low (true). When the SCOS one-shot times out, the RSGO signal goes high (false). The read sector go flip-flop is reset by the low signal at U20-5 at the end of the read operation. Subsequent RSGO signals are generated by LSTWD (high) followed by CCYL (high), PTYCYL (high), ENDSTR (low), and SCOPCK (high) which generates RSGO.

At the start of a diagnostic read operation, the STRT signal from the processor causes the RDST- signal at U55-10 to go low. This sets the latch composed of the two low-true NOR gates U55. This sets the input at U42-8 low. Since the input at U42-9 is low, the BUFFS signal at U42-10 goes high. This programs the buffer contents counter properly for the diagnostic read operation. During all other operations, the BUFFS signal is held low.

4-26 INTERRUPT CONTROL (1940027, SHEET 1)

The Interrupt control logic contains the interrupt mask flip-flop that allows the processor to set up priorities for the program interrupt and the INT REQ internal request flip-flop that generates the INTR- signal to the processor to request a program interrupt or channel access.

4-27 Interrupt Mask

When the processor issues a mask out instruction to set up priorities for the program interrupt, bit 9 of the accumulator bits is used as the mask bit for the 8010 Disc Controller. If the disc controller is not one of the devices having priority for the interrupt, the D09 signal applied to U62-2 of the INT MSK flip-flop is high. When the MSKO- signal is applied from the processor, the output from U2-6 goes high. This sets the INT MSK flip-flop U62, causing the input to U1-13 to go low. This disables the INTR- signal to the processor, since the INT REQ flip-flop U62-9 cannot be set by the RQENB clock pulse.

4-28 Interrupt Request

If the controller is one of the devices having priority for the interrupt, the INT MSK flip-flop is not set. This causes the input of U1-13 to be high. If the DONE flip-flop U56 is set, the input to U1-12 is also high. This conditions the INT REQ flip-flop U62 with a high input at U62-12. When the next RQENB signal is sent from the processor, the INT
REQ flip-flop is set on the leading edge of the RQENB pulse.

The INTPIN signal from the processor is applied to U7-9. This causes a high input at U8-5. If the INT REQ flip-flop U62 is not set, the INPOT signal at U8-6 goes high. This signal is sent to the next device connected on the I/O bus. If the INT REQ flip-flop is set, the INPOT signal at U8-6 goes low disabling priority to all other units on the I/O bus. When the INTA (interrupt acknowledge) signal is applied from the processor, the output from U1-8 goes high; this causes a high input at U53-5. If the INTPIN signal is high at U53-4 and the INT REQ flip-flop is set, the INTACK signal at U53-6 goes low. The INTACK signal is applied to data lines DATA11 to the processor. Since data lines DATA10 and DATA12 through DATA15 are logical 1's, the device code of the disc memory system, 010,000 is sent to the processor. This identifies the disc memory system as the device requesting the interrupt.

4-29 CORE MEMORY ADDRESS REGISTER AND WORD TRANSFER COUNTER

(1940027, Sheet 2)

The core memory address register is a 16-bit binary counter that is loaded with the initial starting address for the operation. During the operation, the counter is advanced by DCHADG pulses when each word is transferred. The contents of the register are read out to the processor at the start of an operation and can be read out at other times as a means of checking the number of words transferred, or for diagnostic purposes.

4-30 Core Memory Address Register

When the DOB instruction is issued by the processor, accumulator bits 0 through 15 (D100 through D115) are applied to the core memory address register. These bits contain the initial starting address for the operation. When the DATOB signal is generated by the processor, the MASET signal goes low. This low signal is applied to pin 1 of each register and loads the 4 bits associated with that register into the register. Since registers U36 through U39 are programmable, the outputs from the registers will assume the state of the input signals. When the DCHADG pulse is generated at the beginning of each data cycle, the input to U58-11 goes low and the output at U58-10 goes high, clocking register U38. The four registers, U36 through U38 are connected as a ripple-through binary counter. A count of 0 to 32,768 words can be transferred.

The outputs from the core memory address register are connected to a register on the processor data bus and are read out to the processor at the beginning of an operation and incremented when the DCHADG pulse occurs. They are also read out to the processor when the processor issues a DIB instruction. If the system is busy when the DIB instruction is issued, the contents of the core memory address register is presented as logical 0's. The setting of the most significant bit in the core memory address register sets the controller in a diagnostic mode of operation. In the diagnostic mode the 16-word buffer is read. There are no data transfers to and from the disc during the diagnostic mode.

The core memory address register is cleared by the RST- signal applied to U27-12, 13 when the IORST pulse is generated by the processor.

4-31 Word Transfer Counter

When subsector operation is used, a DOC instruction is issued by the processor. The starting subsector address is contained in accumulator bits 0 through 3. The length of operation expressed in terms of subsectors is contained in accumulator bits 4 through 15.
At the start of the operation, the START signal at U59-3 goes high when the STRT or IPOL signal is sent from the processor. This clears counters U43, U44, U46 and U48. When the DATOC signal is sent from the processor, the STCLD- signal goes low (true), presetting the DOCX flip-flop. The STCLD- signal is also applied to pin 11 of counters U44, U46 and U48. This loads data bits D04 through D15 into the counters, thereby programming the counters for the specified length of operation. The low STCLD- signal is also applied to U1-4 and causes the SALOS- signal at U1-6 to go low (true). This loads accumulator bits 0 through 3 into the subsector address register on the formatter PC board.

The programming of counters U44, U46, and U48 with bits D04 through D15 allows multiple 1 to 4096 subsectors to be operated. When bits D04 through D15 are low (accumulator bits logical 0), the length of the operation is 4096 subsectors. Since there are 16 words per subsector, 65,536 words can be transferred.

During the operation, counter U43 is advanced with each DCHADG- pulse at the beginning of each data cycle. Since counters U43, U44, and U46 are cascaded in a ripple-through connection, the output at U48-12 goes high at the count programmed by D04 through D15. This clocks the END flip-flop U60 setting the END signal at U60-5 high.

When sector operation is used, the DOC instruction is not executed, and the word transfer counter then counts 256 words (one sector). At this count, the END flip-flop is clocked, setting the END signal at U60-5 high.

4-32 PROCESSOR DATA BUS (1940027, SHEET 2)

The processor data bus connects the adapter PC board to the computer processor. It receives the D00 through D15 signals from the processor, and according to the contents of the signals, routes them to the core memory address register; the unit, track and sector registers; the word transfer counter and subsector register; or the data selectors and registers. It also contains a register that stores the contents of the core memory address register. In addition, it contains a buffer register for the data read from the disc or the data read from the error register on the formatter/adapter common bus.

The D00 through D15 signals from the processor are each applied to an inverter (U10 through U13). When the data lines contain the disc, track and sector address given in the DOA instruction, the address information is applied through the adapter/formatter common bus to the unit, track and sector registers on the formatter PC board.

When the data lines contain the initial address information of the DOB instruction, the address information from the inverters is applied to the registers of the core memory address register.

When the data lines contain the information of the DOC instruction, the inverted D04 through D15 signals are applied to the word transfer counter, and the D00 through D03 signals are applied through the adapter/formatter common bus to the subsector register on the formatter PC board.

When the data lines contain the data to be written, the inverted data from the inverters is applied through the adapter/formatter common bus to the data selectors and registers on the formatter PC board.

The register for the outputs of the core memory address register is composed of NAND gates U23 through U26. At the start of an operation after the core memory address register has been loaded with the initial address, the first DCHADG- pulse is applied to
U14-1. This strobes the initial address from the core memory address register through the NAND gates to the data lines to the processor. When a DIB instruction is issued by the processor, the MAIN- signal at U14-2 goes low. This strobes the present contents of the core memory address through the NAND gates to the data lines to the processor.

When data is read from the disc or when the status of the disc memory system is read, the buffer composed of NAND gates U10 through U13 is used. When the DCHIN- signal at U20-9 goes low, the data is strobed through the NAND gates to the data lines in the processor.

When the status of the disc memory system is read, a DIA instruction is issued by the processor, and the contents of the error register (bits 10 through 15) on the formatter/adapter common bus is strobed by the STATIN signal through the formatter/adapter common bus to NAND gates U10 through U13. The low STATIN- signal at U20-10 strobes the contents of the error register through the NAND gates to the data lines to the processor.

The INTACK- signal at U6-11 goes low when the disc memory system has requested an interrupt and has priority. This causes a logical 1 bit on line DATA11- to the processor. Since data line D10- and data lines D12- through D15- are logical 1's (high), the code 010,000 (octal 20) identifies the disc memory system as the device requesting the interrupt.

4-33 ADAPTER/FORMATTER COMMON BUS (1940027, SHEET 2)

The adapter/formatter common bus contains a buffer that receives the DOO through D15 signals from the processor data bus and a logic circuit that provides the enabling signal for transferring the signals to the formatter/adapter common bus. The adapter/formatter common bus also receives the data read from the disc and the data read from the error register on the formatter/adapter common bus. It inverts this data and applies it to the buffer register on the processor data bus.

When the data is read from the disc, the read signals from the data selectors and registers are strobed through the formatter/adapter common bus to the DB00- through DB15- inputs. Each input signal is terminated by resistive networks and applied to an inverter (U30, U31, U33 and U35). The inverted output signals from the inverters are applied to U10 through U13 and are strobed to the data lines to the processor by DCHIN.

When the status of the disc memory is read, the contents of the error register (bits 10 through 15, DB10- through DB15-) is strobed from the formatter/adapter common bus and processor data bus to the processor. This route is the same as for the read data signals from the formatter/adapter common bus.

4-34 DATA CHANNEL TRANSFER CONTROL (1940027, SHEET 2)

The data channel transfer control logic contains the DCH REQ, DCH SEL and DCH BSY flip-flops. The DCH REQ flip-flops controls the DCHR (data channel request) and DCHPOT (data channel priority out) output signals, and the DCH SEL flip-flop controls the DHADG transfer pulses and DCHMO (data channel mode) output signal. The DCH BSY flip-flop controls the DCH BSY (data channel busy) output signal and the gating of the input DCHI (data channel in) and DCHO (data channel out) signals that generate the DCHI- and DRSETPS signals respectively.

After the WROP (write operation) or RDOP (read operation), the data channel transfer control flip-flop is set and the input to U9-4 or U9-1 goes high. For a write
operation, the DRFUL- signal at U9-5 is set high, and for a read operation the DRFUL signal at U9-2 is set high. This causes the input to U15-1 to go high. Since the DCH BSY flip-flop is reset at this time and the END- signal is high, the inputs to U15-2 and U15-13 are high. This causes the output from U15-12 to go high, conditioning the DCH REQ flip-flop U61 with a high input at U61-2. When the RQENB- signal is applied from the processor at the beginning of the memory cycle, the output from U9-8 goes high. This sets the DCH REQ flip-flop U61-5, causing the CDHR- signal to the processor to go low (true).

The DCHPIN- signal from the processor causes a high input at U5-10. If the DCH REQ flip-flop is not set, the DCHPOT- signal at U5-8 goes low (true). This signal is transmitted to the next device connected on the computer I/O bus. If the DCH REQ flip-flop is set, the DCHPOT- signal remains false giving the controller priority. The output of U59-6 goes high, conditioning the DCH SEL flip-flop U61 with a high input at U61-12 and enabling AND gate U59 with a high input at U59-10.

When the DCHA- signal is applied from the processor at the beginning of the data channel cycle, the output from U2-8 goes high. This sets the DCH SEL flip-flop U61-9 and causes the DCADG- signal at U8-3 to go low. This signal is sent to the processor to indicate a data-out transfer. For a read operation, the RD signal at U8-1 is high, causing the DCHMO- signal to go low. This signal is sent to the processor to indicate a data-in transfer. The low DCHADG- pulse at U58-10 loads the core memory address on the processor data bus into the core memory address register. This causes the initial address to be read out to the processor. The low DCHADG- pulse is also applied to the preset input of U60-10 of the DCH BSY flip-flop U60. This sets U60-9, enabling U21-11 and U21-3. This also causes the DCH BSY signal to go high. This signal is applied to the data register logic on the adapter/formatter common bus. During a write operation this enables the register to transfer data from the processor to the data selectors and registers on the formatter PC board.

During a write operation, the DCHO signal applied from the processor causes the output from U21-6 to go low. This causes the DRSETPS- signal to go low (true). The DRSETPS- signal is applied to the buffer and data register transfer control logic on the formatter PWBA and generates the DRSET pulse that clocks the data into the data selectors and registers. When the DCHO signal goes low (false), the DCH BSY flip-flop is reset. Then the DCHA- signal for the next data word is applied from the processor and the DCHADG- signal presets the DCH BSY flip-flop. This enables gates U21 again for the next DCHO signal from the processor.

During a read operation, the DCHI signal applied from the processor causes the output from U21-8 to go low. This causes the DCHIN signal to go low (true). The DCHIN- signal becomes the DRAVL- signal when it is applied through the adapter/formatter interface. The DRAVL- signal is applied to the buffer and data register transfer control logic on the formatter and generates the DRSET pulse that clocks the read data from the memories into the data selectors and registers. When the DCHA- signal goes low (false), the DCH BSY flip-flop is reset. When the DCHA- signal for the next data word is applied from the processor, the DCHADG- signal presets the DCH BSY flip-flop. This enables gates U21 again for the next DCHI signal from the processor.

4-35 FORMATTER BOARD DETAILED CIRCUIT DESCRIPTION

The following paragraphs describe the logic circuits within the formatter PC board of the controller. The information contained in the descriptions is taken from the schematic diagram 1940083, sheets 1 through 6.
POWER ON RESET (1940083, SHEET 1)

When +5 volts are applied to the formatter board during power turn-on the emitter-base circuit of transistor at U8 (B23) generates a negative pulse in its collector circuit. This pulse is used to reset the SEQLEN flip-flop in the sector equal detection circuit (B3). The negative pulse applied to inverter U13-9 (C4) produces a positive pulse at U13-8. This positive pulse resets the sector and subsector address registers.

READ/WRITE SECTOR CONTROL (1940083, SHEET 1)

The read/write sector control logic provides the control signals required for writing and reading of a sector on the disc.

Write Sector Control

When the WCLK clock pulse at U123-3 (C3) and the SCLK clock pulse at U123-5 are high, the SC SYN pulse at U123-6 goes low, presetting the WR SYN flip-flop U95. At this time, the SCOS one-shot has already been triggered, causing the WSGO- signal at U34-1 to be low and the input to U49-1 to be high. The low WSGO- signal has also caused a low input at U26-1 causing a high input to U49-5. After the time delay of 120 nanoseconds, a low input is applied to U77-3, causing the SRCL signal at U77-6 to go high (refer to the Memory Buffer and Register Loading Circuit Description).

When the SCOS one-shot times out, the WSGO- signal goes high (false). At the same time, the SC SYN signal goes high and the WCLK clock pulse resets the WR SYN flip-flop, causing a high input to be applied to U123-9. The transition from low to high of the WSGO- signal clocks the WR SC flip-flop U110-5. This applies a high input to U124-2.

When the sector address applied to the sector equal detection circuit is equal to the sector on the disc, the SEQL input to U124-13 goes high. If the PERM ADDRESS signal applied to U124-1 is high (address not locked out by disc unit write lockout switches), the WRL flip-flop U110 is conditioned with a high input at U110-12. The transition from low to high of the SC SYN signal clocks the WRL flip-flop. This applies a high input to U123-10, U51-10, and U50-5. The high output from U110-9 is also applied to the WRITE signal flip-flop to condition it with a high input at its D input.

The SRCL signal at U77-6 goes high when the WSGOCK- signal at U49-6 goes low and goes low when the WSGO- signal goes high. The SRCLKW- pulses at U123-8 are generated by the WCLK pulses applied to U123-11. When each SRCLKW- pulse is generated at U123-8, the low input to U77-5 generates the SRCL pulse at U77-6.

The SRLD- signal at U66-6 goes low when the WSGO- signal goes low at U66-3 and goes high when the WSGO- signal goes high. The SRLDENW- signal at U51-8 goes low when 15 bits have been counted by the sector bit and word control circuit. The low input applied to U66-4 and U66-5 at this time causes the SRLD- signal to go low (refer to the Memory Buffer and Register Loading Circuit Description).

When the BFEMTY signal at U50-4 is still high after 15 SRCLKW- pulses have been counted by the sector bit and word control circuit, the inputs to U50-3, 4 and 5 are then high. This causes the TMERWR- signal at U50-6 to go low. When the next SRCLKW- pulse occurs, the TMERWR- signal goes high. This sets the TMER flip-flop in the error circuitry, indicating a data late error (data transfer timing error) since the data from the processor did not arrive in time and caused the BFEMTY signal from the buffer contents counter to remain high (memory buffer empty).
Read Sector Control

When the SCOS one-shot in the end control circuit is triggered, the RSGO- signal goes low, presetting flip-flop U53-5. This also applies a low input to U34-3 and to U26-2. After the time delay established by R16 and C28, the RSGO CK- signal at U49-8 goes low and clocks the bit and word control counter, which is loaded to a programmed count of 15 by the RSGO- signal (refer to the Sector Bit and Word Control Circuit Description).

The presetting of flip-flop U53-5 causes a low input to U90-8. When the sector address is equal to the address from the current location counter, the SEQL- signal at U90-9 goes low. This conditions the RDL flip-flop U95 with a high input at U95-12. The SCSYN- signal at U123-6 goes low when the SCLK and WCLK pulses are high, the low to high transitions at U95-11 clocks the RDL flip-flop U95, causing the RDL output at U95-9 to go high. This high output conditions the READ- signal flip-flop in the disc interface circuit with a high input at its D input. This causes the flip-flop to be set by the WCLK pulse, causing the READ- signal to the disc memory unit to go low (true).

The high RDL signal at U95-9 is also applied to U52-13. When the RCLK (read clock) pulse is applied to U52-2, the RDSC flip-flop U53 is clocked through U14-3. This causes the output from U53-6 to go high. This high output is applied to U52-10. This enables the SRCLKR- pulses at U52-8 which are generated by the RCLK- pulse applied to U52-9.

When 15 read data bits have been shifted into shift registers U57 through U60 in the buffer memory and register loading circuit, the input to U50-1, goes high, and BFLDCNR- signal output at U50-12 goes low. This causes a high input at U51-1. When 16 read data bits have been shifted into shift registers U57 through U60, all inputs to U51 are high, and the BFLDR- signal at U51-6 goes low (refer to the Memory Buffer and Register Loading Circuit Description).

The SRCLKR- pulses from U52-8 are also applied to U77-4 and generate the SRCL clock pulses during the read operation.

The BFLDR- pulse from U51-6 is also applied through inverter U22 to U50-9. If the BFFUL signal at U50-10 is still high at this time, the TMERRD- signal at U50-8 goes low. The low TMERRD- signal presets the TMER flip-flop in the error circuit, indicating a data late error (data transfer timing error), since the DCHI signal from the processor did not arrive in time and caused the BFFUL signal to remain high (memory buffer full).

Reset Circuits

The WRSC flip-flop U110 is reset when the WROP signal at U39-10 goes low, as a result of the resetting of the WROP flip-flop or when the WRL- signal goes low when the WRL flip-flop U110 is set.

The WRL flip-flop U110 and the RDL flip-flop U95 are reset when the INIT- signal at U124-9 goes low at the start of an operation, or when the WROP signal at U124-10 goes low as a result of the resetting of the RDOP or WROP flip-flop, or when the ENDSTR- signal goes low at the end of the write or read operation.

The RDSC flip-flop U53 is reset when the RDOP signal at U53-1 goes low as a result of the resetting of the RDOP flip-flop.
The WRSYN flip-flop U95 is reset when the signal at U95-1 goes low when the track origin signal goes low.

4-41 BIT AND WORD CONTROL COUNTER (1940083, SHEET 1)

The bit and word control counter circuit counts the number of bits transferred during the write and read operations and generates the LSTWD (last word) signal for the subsector. It also provides control signals to the read/write sector control circuit and to the buffer and data register control circuit.

4-42 Write Control

When the WSGO- (D4) signal goes low, 4-bit binary counters U70 and U69 are cleared. During a write operation the RSGO- (D4) signal is high (false). Therefore, U70 and U69 are not loaded with the programmed inputs at A through D. When the WRSC flip-flop is set in the read/write sector control circuit, the low WRSC signal presets flip-flop U53-9. This applies a high input to U69-10 (ENT) and to U54-1.

During the write operation, counters U70 and U69 are clocked by the SRCLKW pulses applied to U55-5 which produce positive pulses at the clock input of U70 and U69. At the count of 12, the inputs to U54-2 and U54-13 go high. This applies a high input to pin 2 of flip-flop U67. The SRCLKW pulses are also applied to U14-4 and produce positive pulses which clock the BFPSINH flip-flop U67. At the count of 13, flip-flop U67-5 is set. The low BFPSINH signal from U67-6 is applied to the buffer and data register transfer control circuit and inhibits the generation of BFLDPS pulses at the count of 13. At the count of 16, the BFPSINH flip-flop is conditioned with a low input at U67-2. When the next SRCLKW pulse occurs, flip-flop U67 is reset.

At the count of 14 SRCLKW pulses, the inputs to U54-11, 9 and 10 go high. This conditions flip-flop U67 with a high input at U67-12. When the 15th SRCLKW pulse occurs, flip-flop U67 is set by the positive pulse from U14-6. The high EOWD signal is applied to the logic in the read/write sector control circuit (refer to the Read/Write Sector Control Circuit Description).

At the count of 16 SRCLKW pulses, the inputs to U56-1, 2, 4 and 5 go low. This applies a high input to U55-9. Since the input to U55-10 is high during the write operation, the BDKO signal at U55-8 goes low when the SRCLKW pulse goes high. The low BCKO signal is applied to U65-1 and resets EOWD flip-flop U67. The low BCKO signal is also applied to the read/write sector control circuit and causes the SRLDENW- and SRLD- signals to go high at this count.

At the count 16 BCNT15 pulses, the outputs from WCO through WC3 go high. These outputs are applied to an AND gate in the cyclic cycle circuit and produce the LSTWD signal that conditions the CCYL flip-flop with a high input at its D input. When the LSTWD signal goes high, the input to U65-12 goes high. Since the WRL flip-flop is set in the read/write sector control circuit, the input to U65-13 is also high. This is a high output from U65-11 and a low input to U54-9 which inhibits the setting of the EOWD flip-flop U67. When the CCYL flip-flop is set in the cyclic cycle circuit after 16 more SRCLKR pulses occur, the input to U90-2 goes high. This inhibits the setting of the EOWD flip-flop U67 until after the 16-bit cyclic code word is written.
4-43 Read Control

When the RSGO- signal goes low at the start of the read operation, the input to counter U70-9 and U69-9 goes low. When the low RSGOCK signal is applied to U55-3, counter U70 is programmed to the count of 15. When the RDSC flip-flop was preset in the read/write sector control circuit, the low RDSC- signal applied to U53-13 reset flip-flop U53. With U70 programmed to 15, the first SRCLKR- pulse applied to U55-4 resets U70 to the count of zero. This causes low inputs at U56-1, 2, 4 and 5 and a high input to U55-9. When the SRCLKR- pulse goes high (false), the BCKO- signal at U55-8 goes low. When the next SRCLKR- pulse occurs, flip-flop U53 is set. This enables counter U69 with a high input at U69-10 and also applies a high input to U54-1.

At the count of 13 SRCLKR- pulses, the output from U54-12 goes high. This conditions the BFPSINH flip-flop U67 with a high input at U67-2. When the next SRCLKR- pulse occurs, flip-flop U67 is set. The low BFPSINH- signal is applied to the buffer and data register transfer control circuit and inhibits the generation of DRSETBF- pulses at this count.

At the count of 15 SRCLKR- pulses, the output from U54-8 goes high. This high output is applied to U55-13. If the RDL flip-flop is set in the read/write sector control circuit, the EOWD flip-flop U67 is preset when the SRCLKR- pulse goes false (high). The high EOWD signal from U67-9 is applied to the read/write sector control circuit and causes the BFLDCNR- signal to go low at this point.

At the count of 16 SRCLKR- pulses, the BCN15 signal at U70-15 goes high. This signal is applied to the read/write sector control circuit and causes the BFLDR- signal to go low when the RCLK clock pulse occurs.

At the count of 17 SRCLKR- pulses, BFLDR- goes high, counter U70 is reset to zero, and the inputs to U56-1, 2, 4 and 5 go low. This causes a high input to U55-9, and the BCKO- signal at U55-8 goes low when the SRCLKR- pulse goes high (false). This applies a low input to U65-1 which resets the EOWD flip-flop U67, causing the BFLDCNR- signal in the read/write sector control circuit to go high.

At the count of 16 BCNT15 pulses, the outputs WC0 through WC3 go high. This produces the LSTWD signal in the same manner as for the write operation. After 15 more SRCLKR- pulses occur, the CCYL flip-flop is set and the input to U90-2 goes high. This inhibits the setting of the EWOD flip-flop until the 16-bit cyclic code word is read.

4-44 DISC/FORMATTER INTERFACE CIRCUIT (1940083, SHEET 1)

The disc/formatter interface logic circuit sends the unit select and track address signals to the disc memory units. It receives the track origin, read clock, write clock out, sector clock-, disc ready-, read data-, and illegal address- signals from the selected disc memory unit and returns the write clock in- signal to the selected disc memory unit.

The disc/formatter interface logic circuit also contains the logic for generating the write-, write data-, and read- signals that are sent to the selected disc memory unit.

The track origin-, sector clock-, write clock out-, read clock-, disc ready-, read data-, and illegal J3-10 per address- signals from the selected disc memory unit are applied through J3-21, J3-23, J3-47, J3-39, J3-2, J3-31 and J3-17, respectively. The signals are inverted and applied to various logic circuits as shown on the schematic.
The formatter/adapter common bus receives the address and write data from the processor through the processor data bus. It applies the address signals to the unit, sector, subsector and track registers and the write data signals to the inputs of data selectors and registers U15 through U18. It also receives the DR00 through DR15 read signals from U15 through U18 and applies them to the processor data bus. In addition, the formatter/adapter common bus contains the 6-bit error register which provides the status of the disc memory system.

**Address and Data Signals**

The address signals (DB00 through DB15) and the write data signals (DB00 through DB15) are applied through electrical connector J1. Each signal line is terminated by a resistive network and applied to an inverter in its associated IC (U1 through U4). When the address given in the DOA instructions is on lines DB00 through DB15, the unit, track and sector address bits are applied to their respective address registers. For subsector operation, the subsector address contained in DB00 through DB03 is applied to a 4-bit register on the formatter/adapter interface. When the DOCX flip-flop is set in the initiation logic circuit, the subsector address bits are applied to the subsector address register U99 in the unit, track and sector address register circuit.

When the write data is on lines DB00 through DB15, the inverted data bits are each applied to their associated input on data selectros and registers U15 through U18.

During a read operation, the DB00 through DR15 input signals from U15 through U18 are applied to the register composed of U1 through U4. When the DATIA signal is applied from the processor, the DRGAT- signal at J2-J3 fall low. This strobes the read data signals to the output lines DB00- through DB15-. Output lines DB00- through DB15- route the signals to the processor via the adapter/formatter common bus and processor data bus.

**Error Register**

The error register is composed of gates U5 and U19. (C6) ILAER (bit 13), RDER (bit 14) and bits 10, 11, 12 and 14 cause a logical 1 in their associated bit in the register when they go high (true). Bit 15 is set to logical 1 when any of the 5 errors occur (refer to the error logic circuit description). When the DATIA signal is applied from the processor, the STATIN signal at J2-25 goes high. This strobes the contents of the error register to output lines DB10- through DB15-. Output lines DB10- through DB15- route the contents of the error register containing the disc memory system status to the processor via the adapter/formatter common bus and the processor data bus.

**Cyclical Cycle, Parity Cycle, and End Control**

The cyclical cycle, parity cycle, and end control logic circuit contains the CCYL flip-flop that is set when the 16-bit cyclical code word is written or read for each subsector of data, the PTYCYL flip-flop that is set when the odd parity bit is written or read for each subsector of data, and the ENDSTR one-shot that is triggered at the end of each subsector.

**During Write Operation**

After 240 bits (15 words) have been written in a subsector, the WCO through WC3 signals at U68-1, 2, 4 and 5 (D8), respectively, go high. This causes the output from
U68-6 to go high, conditioning the CCYL flip-flop U63 with a high input at U63-2. This signal is the LSTWD signal. At this time, the PTYCYL- signal at U104-9 is high, since the PTYCYL flip-flop is reset. The BCNT15- signal at U104-10 is also high, since counter U70 in the sector bit and word control circuit is clocked to zero on the 240th bit count. When counter U70 again counts to 15, the BCNT15- signal at U104-10 goes low, causing the input to U77-11 to go high. When the SRCLKW- pulse for the 255th bit count goes high (false), all inputs to U77 are high. This causes a low output from U77-8 that is applied to the clock input (U63-3) of the CCYL flip-flop U68. When the SRCLKW- pulse for the 256th bit count goes low, the output from U77-8 goes high. The low to high transition at U63-3 sets the CCYL flip-flop U36. The 256th SRCLKW- pulse also clocks counter U70 to zero in the bit and word control circuit, causing the BCNT15- signal to go high and the LSTWD signal at U68-6 to go low.

The high output from U63-5 of the CCYL flip-flop U63 is applied to the disc interface logic circuit to enable the writing of the 16-bit cyclic code word and is also applied to U63-12 of the PTYCYL flip-flop U63. The low output from U63-6 is applied to the disc interface logic circuit to inhibit the writing of data at this time.

When 15 more SRCLKW- pulses have been counted by counter U70 in the bit and word control circuit, the BCNT15- signal at U104-10 goes low. This applies a high input to U77-11, causing a low input to U63-11. When the next SRCLKW- pulse occurs, the PTYCYL flip-flop U63 is set by the low to high transition at U63-11 and the CCYL flip-flop is reset by the low to high transition at U63-3.

The low output from U63-5 of the CCYL flip-flop is applied to U63-12 of the PTYCYL flip-flop U63. The high output from U63-9 is applied to the disc interface logic circuit to enable the writing of the odd party bit. The low output from U63-8 is also applied to the disc interface logic circuit to inhibit the writing of data at this time. The low output from U63-8 is also applied to U104-9, causing a high input to U77-11. This causes a low input to U63-11.

When the next SRCLKW- pulse occurs, the PTYCYL flip-flop U63 is reset by the low to high transition at U63-11. The low output from U63-9 is applied to U64. This triggers the ENDSTR one-shot U64, causing the output from U64-5 to go high and the output from U64-12 to go low. The low output from U64-12 is applied to U104-12, causing the SCOPCK signal at U104-11 to go high. The low output from U64-12 also resets the WRL flip-flop in the read/write sector control circuit, causing the WRITE- signal to be clocked high (false). The high SCOPCK signal at U104-11 is applied to the write sector GO circuit and causes the WSGO- signal to go low. After 200 nanoseconds, one-shot U64 times out, causing the SCOPCK signal to go low. This causes the WSGO- signal to go high.

The sequence described is repeated for each subsector until the end of the operation when the END signal and BFEMTY signal go high (true). This resets the WSGO flip-flop in the write sector start circuit, terminating the operation.

4-50 During Read Operation

The operation of the cyclic cycle, parity cycle, and end control logic circuit during a read operation is similar to the operation during a write operation as explained in the following paragraph.

During the read operation, the LSTWD signal goes high after 241 SRCLKR- pulses have been counted, since counter U70 in the sector bit and control circuit is loaded to a programmed 15 count at the start of the read operation. The SRCLKR- pulses at U77-9
are used in place of the SRCLKW- pulses during the read operation. When the ENDSTR one-shot U64 is triggered, the low output from U64-12 resets the RDL flip-flop in the read/write sector control circuit, causing the READ- signal to be clocked high (false). The high SCOPCK signal at U104-11 is applied to the read sector start circuit and causes the RSGO- signal to go low. After 200 nanoseconds, one-shot U64 times out, causing the SCOPCK signal to go low. This causes the RSGO- signal to go high.

The sequence is repeated for each subsector until the end of the operation when the ENDRD- signal at U57-12 in the done control circuit goes low. This resets the RSGO flip-flop in the read sector start circuit, terminating the operation.

4-51 ERROR LOGIC CIRCUIT (1940083, SHEET 2)

The error logic circuit generates 4 of the 5 error signals that are applied to the error register on the formatter/adapter common bus. These error signals include the disc fail error (bit 10), the write protect error (bit 11), the data transfer timing Error (bit 12) and the illegal address error (bit 13). The read error (bit 14) is generated by the read check error circuit. Bit 15 of the error bits is generated on the formatter/adapter common bus when any of the other errors occur.

4-52 Disc Fail Error

The DSC FAIL flip-flop U25 is set when the disc becomes not ready or when the system is hung during a write or read operation, the WRL flip-flop in the read/write sector control circuit is set when the SEQL signal goes high (true). This applies a low input to U23-4 conditioning U25 with a high input at U25-4. During a read operation, the RDL flip-flop in the read/write sector control circuit is set when the SEQL- signal goes low (true). This applies a low input to U23-4 conditioning U25 with a high input to U25-12. The DSCRDY- signal applied to U25-11 (CLOCK) goes low when the disc is ready. The DSCRDY- signal goes high if there is a loss of ac or dc power, if the dc voltages are below acceptable limits, or if the disc rotational speed is below the reliable operating range. When the DSCRDY- signal goes high, flip-flop U25 is set.

The DSC FAIL flip-flop U25 is also preset if the system is hung during a write or read operation. At the start of a write or read operation, the INIT- signal at U66-13 goes low. This causes a high to low transition at pin 1 of retriggerable TMOUT one-shot U37. This triggers U37, and the output at U37-4 goes low. This low output is applied to U66-10. Since the DSC FAIL flip-flop U25 is reset, the input to U66-9 is high. Since either the WROP (write operation) or RDOP (read operation) is set, the input to U66-11 is high, the output at U66-8 is low, and the input to U25-10 (PRESET) is high.

TMOUT one-shot U37 is a retriggerable one-shot that does not time out if it is retriggered before the time delay established by register R9 and capacitor C6 times out. Before TMOUT U37 times out, either the WSGO- signal (write operation) of the RSGO- signal (read operation) goes low, retriggering U37. The WSGO- signal at U66-2 goes low during a write operation at the start of each subsector. The RSGO- signal at U66-1 goes low during a read operation at the start of each subsector. If the WSGO- signal does not go low in time (300 nanoseconds) during a write operation, or the RSGO- signal does not go low in time (300 nanoseconds) during a read operation because the system is hung, one-shot U37 times out. This causes the input to U66-10 to go high, presetting the DSC FAIL flip-flop U25 with a low input from U22-8. This causes the DSC FAIL signal at U25-9 to go high, and the DSC FAIL- signal at U25-8 to go low.
For either cause of a disc fail error, the high output from U25-9 is applied to U19-10. The low output from U25-8 is applied to U20-9. This causes a logical 1 in 10 of the error bits and also causes a logical 1 in bit 15.

The low output from U22-8 that presets the DSC FAIL flip-flop U25 also is applied to U39-1. This causes the ENDER- signal at U124-6 to go low. This sets the DONE flip-flop, terminating the operation when the DSC FAIL- signal at U66-9 goes low and causes the ENDER- signal to go high. This causes the SELB- (selected busy) signal to the processor to go high (false). This also causes an interrupt request to be generated if the INTDSB flip-flop is reset.

4-53 Write Protect Error

The WPTER flip-flop U109 is preset when the selected track-sector is write protected. When the SCSYN- pulse goes false at the start of a subsector and the SEQL signal is high (true), the inputs to U24-9 and 10 are both high. The resulting high output from U24-8 is applied to U123-13. Since the WRSC flip-flop is set at this time, the input to U123-2 is high. The PERM ADDRESS- signal from the disc at U123-1 goes high when the selected track-sector is write protected. This causes the output from U123-12 to go low, presetting the WPTER flip-flop U109. The high output from U109-8 is applied to U20-11. This causes a logical 1 in bit 15 of the error bits.

The low output from U123-12 is also applied to U124-3. This causes the ENDER- signal at U124-6 to go low. When the SEQL signal at U24-9 goes low (false), the ENDER- signal goes high. This sets the DONE flip-flop, causes the SELB- signal to the processor to go high (false), and causes an interrupt request to be generated if the INTDSB flip-flop is reset.

4-54 Data Transfer Timing Error

The TMER flip-flop U25 is set when the processor has failed to respond in time to a request for data channel access. During a write operation, the TMERWR- signal at U25-3 (CLOCK) goes low (true) when the data from the processor does not arrive in time and causes the BFEMTY signal to remain high, indicating buffer empty (refer to the Read/Write Sector Control Circuit Description). When the TMERWR- signal goes high (false) one SRCLKW- pulse time later, the TMER flip-flop U25 is set.

During a read operation the TMERRD- signal at U25-4 goes low (true) when the processor does not generate the DCHI signal in time and causes the BFFUL signal to remain high, indicating memory buffer full. The low TMERRD- signal presets the TMER flip-flop U25. This causes the TMER signal at U25-5 to go high, and the TMER- signal at U25-6 to go low.

The high output from U25-5 is applied to U5-13 and causes a logical 1 in bit 12 of the error bits. The low output from U25-6 is applied to U21-5 and causes a logical 1 in the bit 15 of the error bits.

4-55 Illegal Address Error

The ILAER flip-flop U109 is set when the disc or track selected by the processor is not available on the system. Pin E2 is jumpered to pins E5 through E8 in accordance with the highest unit number assigned. If the disc unit selected is in the system but the track address is higher than the highest track on the disc, the inputs to U12-2 and 3 go low. This causes a high output from U12-1 and a low input to U23-13. The output at U23-11 then
goes high, causing a high input to U23-1 and U24-13 and a low input to U119-4. The low input to U119-4 inhibits the READ- signal. If the disc unit selected is not in the system, the input to U23-12 goes low, causing the high inputs to U23-1 and U24-13 and the low input to U119-4.

At the beginning of a write or read operation, the INIT-A signal goes low. This presets flip-flop U36. This causes the output from U36-5 to go high, applying a high input to U24-5. Since the RDOP signal is true (high) during both read and write operations, the input to U24-4 is also high. This causes the output from U24-6 to go high, applying a high input to U24-2. Since the ILAER flip-flop is not set at this time, the input to U24-1 is high. This causes the output at U24-3 to go high, applying a high input to U23-2. The output from U23-3 then goes low, presetting the ILAER flip-flop. The high output from U109-5 is applied to U21-4 and causes a logical 1 in bit 15 of the error bits. The low output from U109-6 is applied to U24-4 and causes a logical 1 in bit 15 of the error bits.

The low output from U23-3 is also applied to U124-4 and causes the ENDER- signal at U124-6 to go low (true). When the ENDER- signal to the processor goes high (false), and an interrupt request is generated if the NTDSB flip-flop is reset.

During a read operation, flip-flop U36 is reset at the end of the first subsector when the RDL flip-flop in the read/write sector control circuit. If the system becomes hung and an illegal address occurs, the inputs to U24-12 and 13 go high. This sets the ILAER flip-flop U109 with a high output from U24-11. This causes a logical 1 to be set in bits 10, 13, and 15 of the error bits. This also causes the DONE flip-flop to be set, the SELB- signal to the processor to go high (false), and an interrupt request to be generated if the MSKO flip-flop is reset.

4-56 MEMORY BUFFER AND REGISTER LOADING WRITE AND READ OPERATION (1940083, SHEET 3)

The memory buffer and register loading circuit consists of quadruple two-input multiplexers U15 through U18, quadruple two-line to one-line data selector/multiplexers U29 through U32 and U47, 64-bit read/write memories U43 through U46, 4-bit parallel access shift registers U57 through U60, buffer/disc access counter U61, and buffer/processor access counter U33. This circuit receives the write data from the processor, buffers it, and transfers it in serial form to the disc unit. This circuit also receives the serial read data from the disc, buffers it, and transfers it in parallel form to the processor. The timing diagram for the read and write operations appear in figures 4-4 and 4-5 respectively.

4-57 Write Operation

The DB00 through DB15 write data word from the processor is applied to the data selectors and registers U15 through U18 that are quadruple two-input multiplexers. During the write operation, the WROP signal at U34-11 is high, since the WROP flip-flop is set. This applies a low input to pin 10 (SEL A) of U15 through U18. When the DCHO signal is applied to the data channel transfer control circuit, the DRSETPS- signal goes low. This causes the DRSET signal at U34-9 to go high. This clocks U15 through U18 with a low input, and the DB00 through DB15 signals appear at the outputs of U15 through U18, since they were selected by the low input applied to each SEL A input.

The outputs from U15 through U18 are applied to the inputs of data selectors U29 through U32 that are quadruple two-line to one-line data selector/multiplexers. Since a high input is applied to the SEL input of U29 through U32 and the STR input of U29 through
Figure 4-4. Write Subsector Timing Diagram
U32 is grounded, the inputs from U15 through U18 are selected and appear at the outputs of U29 through U32 and the inputs to memories U43 through U46.

At the start of the write operation, all inputs to NOR gate U20 are high. This causes a low output from U20-12 which is applied to the SELECT input of U47. This selects the outputs of the buffer/processor access counter U33. The BFLDPS- pulses at U48-2 occur as a result of the DCHO signals sent from the processor. This causes a low input at the write enable input of memories U43 through U46. The BFLDPS- pulses are also applied to U48-12 and clock the buffer/processor access counter U33 which is a 4-bit binary counter. When the first BFLDPS- pulse is applied, U33 is reset and the address output from U47-4, 7, 9 and 12 is 0000. When the WRITE ENABLE input of U43 through U46 goes low, the input data to the memories is written at this address. Memories U43 through U46 are 64-bit read/write memories that each store 16, 4-bit words.

The low BFLDPS- pulse applied to U48-12 clocks the 4-bit binary counter U33, and the address output from U33 advances to D001. When the next BFLDPS- pulse is applied, the input data of the next data word is written into the memories at this address. This loading process is repeated until the memory buffer is full. At this point, WSGO- signal goes low, causing the input to U47-1 (SELECT) to go high, selecting the buffer/disc access counter for operation. This also causes the SRLD- signal at the LOAD inputs of shift registers U57 through U60 to go low, and the input to U48-9 to also go low.

At this time, the 4-bit binary counter U61 is reset, and the address output from U47-4, 7, 9 and 12 goes to 0000. Since the write enable input to the memories is now high, the data stored at address 0000 is then read out of the memories in the complemented form and applied to the inputs of shift registers U57 through U60. When the SRCL clock pulse goes high after a short delay, the input data from address 0000 is loaded in parallel into the shift registers.

The low input to U61-2 goes low. When the WSGO- signal goes high, the SRLD- signal goes high. This clocks the 4-bit binary counter U61 so that the address at U47-4, 7, 9 and 12 goes to 0001.

When the SEQL signal in the sector equal detection circuit goes high (true), the WRL flip-flop in the read/write sector control circuit is set. This conditions the write signal flip-flop in the disc interface circuit with a high input at its D input. When shift registers U57 through U60 were loaded, the first bit from SR00 was applied in complemented form to the disc interface logic circuit where it conditioned the write data flip-flop in accordance with the logical state of the bit. When the WCLK pulse occurs and clocks the write data and write flip-flops, the logical state of the bit appears on the WRITE DATA- line and is written on the disc. With each SRCL pulse, the remaining bits of the first data words are shifted in the direction from U60 to U57 out of SR00 and written on the disc in their complemented form. When the last bit of the first data word has been written, the SRLD- signal goes low, and the data word from address 0001 in the memories is loaded in parallel into shift registers U57 through U60 when the SRCL clock pulse goes high. During the time that bits 0 through 11 are shifted to the disc, the next data word is written into the memories at address 0000 using the BFLDPS- signal and the buffer/processor access counter.

The SRLENW signal at U20-2 goes low at the same time that the SRLD- signal goes low, since the low SRLD- signal is generated by the low SRLENW signal. This causes the input to U47-1 to go high, selecting the buffer/disc access counter. When the SRLD- signal goes high 1-1/2 bit times later, U61 is clocked, and the output at U47-4, 7, 9 and 12 goes to 0010.
After the SRLD- signal at the LOAD inputs of shift registers U57 through U60 goes high, the SRCL pulse, which is now generated by the WCLK clock pulses, goes high and the first bit of the second word is shifted out of SR00. The process of reading the data words from the memories, loading them into shift registers, and shifting the bits serially to the disc is repeated for each word written into the memories.

During the write operation, the buffer contents counter, which is a binary count-up/count-down counter, counts up with each BFLD- signal and counts down with each SRLD- signal. The SRCRLW- pulse that generates the SRCL pulses the clock the bits out of the shift register are also applied to an 8-bit binary counter in the bit and word control counter. The counter counts up to 16 bits, 16 words and causes the LSTWD signal (for a subsector) to go true. It also provides control signals to the read/write sector control circuit during the write operation. After the LSTWD signal becomes true, the CCYL flip-flop is set after 16 more SRCRLK- pulses occur. The 16-bit cyclic code word is then written. After the 16th bit has been written, the PTYCYL flip-flop is set. The odd parity bit is then written. When the next SRCRLK- pulse occurs, the PTYCL flip-flop is reset and triggers the ENDSTR one-shot which produces the 200-nanosecond ENDSTR- pulse.

After the 16th subsector is gated the odd parity bit of the final subsector has been written, the buffer contents counter is at a count of zero and the BFEMTY signal goes high (true). The DONE flip-flop is then set (refer to the Initiation and Done Control Circuit Description). A timing diagram for the write operation appears in figure 4-4.

4-58 Read Operation

At approximately 16 bit times after the RSGO signal becomes true, the first bit data read from the disc is applied to pins 2 and 3 of shift register U60. Since the SRLD- signal is high at this time, the bit is shifted into U60 when the SRCL pulse occurs. During the read operation, the SRCL clock pulses are generated by the SRCRLR- pulses that are generated by the RCLK- pulses. The bits are shifted from U60 toward U57 until 16 bits have been shifted into the registers. When the 16 bits have been shifted into U57 through U60 the contents of the register are transferred in parallel on the SR lines to the inputs of data selectors U29 through U32. Since the WROP signal at U34-11 is low during a read operation, a low input is applied to the select inputs of U29 through U32. This selects the SR data inputs from shift registers U57 through U60. Since the strobe inputs of U29 through U32 are grounded, the SR data inputs are applied to the inputs of memories U43 through U46.

The RCLK pulse causes the SR data to be transferred from shift registers U57 through U60, and also causes the BFLDR- signal at U48-1 to go low. This causes a low input at the WRITE ENABLE inputs of memories U43 through U46. Since the BFLDCNR- signal at U20-13 goes low when 15 bits are in shift registers U57 through U60, the outputs from the buffer/disc access counter have already been selected through U47. This causes the SR data to be written into the memories at address 0000.

The low BFLDR- signal causes the outputs from counter U61 to change to 0001. During the writing of words into the memories, the buffer contents counter is advanced when each BFLDR- goes high (false). After the first BFLDR- goes high, the BFEMTY- signal goes high, enabling the DRSETBF- signal circuit in the buffer and data register transfer control logic. At this time, all inputs to U20 are high. This selects the outputs of the buffer/processor counter through U47. This causes the outputs from U47-4, 7, 9 and 12 to go to 0000. This address is applied to the memories and since the WRITE ENABLE inputs are now high, the word stored in address 0000 is read out of the memories in complemented form and applied to the input of data selectors and registers U15 through
Figure 4-5. Read Subsector Timing Diagram
U18. Since the WROP signal at U34-11 is low during the read operation, the high input applied to the select A inputs of U15 through U18 causes the BF data outputs from the memories to the selected. When the first DRSETBF- pulse goes low, the DRSET pulse at U34-9 goes high clocking U15 through U18 and transferring the data to the DR lines to the processor via the formatter/adapter common bus.

The low DRSETBF- pulse applied to U48-13 causes the clocking of counter U33 and causing U33 to advance to 0001. After another data word is transferred from shift register U57 through U60 and written into address 0001 by the buffer/disc access counter, the buffer/processor access counter is again selected and the data from address 0001 is transferred to U15 through U18. If the DCHI signal does not arrive immediately, loading of the memories still continues. When the DRSETBF- pulse is generated as a result of the DCHI signal from the processor, the data from address 0001 is transferred from U15 through U18 to the processor via the formatter/adapter common bus. Counter U33 is then clocked to 0100. In this manner data is alternately transferred from the memories through data selectors U29 through U32 and read out of the memories until the LSTWD signal goes high (true) after 16 words have been read in the subsector. When the LSTWD signal goes true, the CCYL flip-flop is set after 16 more SRCLKR- pulses occur. The cyclic code word is then read. After the cyclic code word is read, the PTYCYL flip-flop is set. The odd parity bit is then read and the read error check is performed and, if a read error has occurred, the RDER signal is generated. However, a read error does not terminate the read operation. When the PTYCL flip-flop is reset, it triggers the ENSTR one-shot which produces the 200 nanosecond ENDSTR- pulse.

During the read operation, the buffer contents counter counts up when each BFLD-pulse goes high (false) and counts down when each DRSETBF- pulse goes high. After the odd parity bit of the final subsector has been read, the buffer contents counter is at a count of zero. The DONE flip-flop is then set (refer to the Initiation and Done Control Circuit Description).

4-59 TRACK AND SECTOR ADDRESS REGISTER LOGIC (1940083, SHEET 4)

The unit, track and sector address register logic circuit contains the registers for loading the unit, track and sector addresses contained in the DOA instruction. The circuit also contains the register loading the subsector address when the DOC instruction is used for subsector operation. In addition, the logic circuit provides the circuitry required to address a maximum of 4096 subsectors during subsector operation.

4-60 Unit Address Selection

The unit address contained in the DOA instruction from the processor (DB03 and DB02 from the formatter/adapter common bus) is applied to U71-10 and 3. When the TSASET- signal at U71-1 goes low as a result of the DATOA signal from the processor, the unit address is loaded into U71. When the disc memory unit selected has address logical 00, the inputs to U71-10 and 3 are low, and the outputs at U71-9 and 2 go low when the TSASET- signal goes low. This causes low inputs at U86-9 and 1 and high inputs to U102-12 and 13. This causes a low output from U102-3 that is applied to J3-15 and selects disc memory unit 0.

When the disc memory unit selected has the address logical 10, the input to U71-3 is low. When the STASET- signal goes low, the output at U71-9 goes high, and the output at U71-2 goes low. This causes a low output from U102-11 that is applied to J3-14 and selects disc memory unit 1.
When the disc memory unit selected has the address logical 01, the input to U71-10 is low, and the input to U71-3 is high. When the STASET- signal goes low, the input to U71-3 is high, and the output at U71-2 goes high. This applies a low input to U86-9 and a high input to U102-5. This causes a low output from U102-6 that is applied to J3-13 and selects disc memory unit 2.

When the disc memory unit selected has the address logical 11, the inputs to U71-10 and 3 are high. When the TSASET- signal goes low, the outputs at U71-9 and 2 go high. This causes high inputs to U102-9 and 10 and a low output from U102-8. This output is applied to J3-12 and selects disc memory unit 3.

The outputs to J15, J14, J13 and J12 are also applied to E pins E8, E5, E6, and E7 respectively, to configure the system in accordance with the number of disc memory units that are to be used (refer to chapter 2).

The information contained in this paragraph is applicable only when multiple memory units are "daisy-chained" in the memory system. The track and unit address register is incremented to a count of 128 (counts of 256 and 512 are selectable). This will cause the unit change flip-flop (U106) to set with TO (track origin) unit change flip-flop. The track and unit address register will be incremented from a track count of 127 to zero and increment the unit address by one. The controller waits for one TO time before looking for SEQL. If the processor changes from one unit to another, the changing of U71 pins 9 or 2 (unit address register) will pulse UACHG- resetting SEQLEN flip-flop inhibiting SEQL for one TO time. When low, the UACHG- signal resets the SEQLEN flip-flop.

4-61 Sector Address Register

The sector address contained in the DOA instruction from the processor (DB11 through DB15 from the formatter/adapter common bus) is applied to U113-15 and U74-9, 10, 1 and 15 respectively. When the TSASET- signal at U113-11 and U74-11 goes low as a result of the DATOA signal from the processor, the sector address is loaded into U113 and U74. When subsector operation is used, the SA10 through SA13 signals from the formatter/adapter PWBA interface are loaded into U99-15, 1, 10 and 9 respectively when the SALOS- signal at U99-11 goes low as a result of the DATOC signal from the processor. The initial sector or subsector address is applied to the sector equal detection circuit (refer to the Sector Equal Detection Logic Circuit Description).

Registers U99, U74 and U113 are 4-bit binary counters cascaded to count to the highest order sector address on a track. When the maximum number of subsectors are to be operated, the operation is as follows: The PTYCYL- signal at U99-5 goes low when the PTYCYL flip-flop is reset at the end of each subsector. When the PTYCYL flip-flop is reset at the end of each subsector, the PTYCYL- signal goes high. This advances counter U99 one count. When U99, U74 and U113 have counted up to the highest sector address on a track, flip-flop U76 is preset by a low output from U104-3. The high output from U76-9 is applied to U92-9. Since the input to U92-10 is high at this time, the output from U92-8 goes low when the track origin signal at U92-12 goes high at the start of the disc revolution. This clocks counter U73 to the next higher track address. When the track origin signal at U92-12 goes low, the output from U92-8 goes high. This resets flip-flop U76. In this manner, the track address register is advanced each time that the highest sector address is reached on the track being operated.

Each time that the track address register is advanced, a low input is applied to U20-4. This causes the HEAD CHANGE- signal at J3-32 to go low (true). The HEAD CHANGE- signal also becomes true at the start of the operation when the initial sector
address is loaded by the TSASET- signal. This causes a low input to U21-9, 10 and 11. When the reset function takes place, the low RST- signal applied to U20-3 also causes the HEAD CHANGE- signal to become true.

During normal operation when the DOC instruction is not used, the length of the operation is one sector (16 subsectors).

4-62 Track Address Register

The track address contained in the DOA instruction from the processor (DB04 through DB10 from the formatter/adapter common bus) is applied to U72-3, 10 and 4, and U73-11, 3, 10 and 4. When TSASET- signal at U73-1 and U72-1 goes low, as a result of the DATOA signal from the processor, the track address is loaded into U72 and U73. Registers U72 and U73 are 4-bit binary counters connected as a ripple-through counter. When the counter is advanced to the count of 127 all inputs to AND gate U75 go high. This enables flip-flop U106 with a high input at U106-12. When the track origin signal becomes false, flip-flop 106 is set, causing a low output from U75-8 which resets the SEQLEN flip-flop in the sector equal detection circuit. The initial track address loaded into U72 and U73 is sent to the disc memory unit on the TAO through TAS lines via electrical connector J3.

The track origin signal which sets U106 also increments the unit address when the track address is at its maximum count. Track address is dependent on the disc size when daisy-chained.

4-63 SECTOR EQUAL DETECTION LOGIC (1940083, SHEET 4)

The sector equal detection logic circuit compares the subsector and/or sector address from the subsector and sector address registers against the output count from the sector counter (current location counter). When the subsector and/or sector address is equal to the output on the sector counter, the SEQL and SEQL- signals are generated.

The sector counter is composed of 4-bit counters U127, U128 and U129 connected as a 12-bit ripple through counter. At the start of each disc revolution, the TO- (track origin) goes low (true) and resets counters U127, U128 and U129. When the TO- signal goes high (false) counters U127, U128 and U129 are cleared. The SCSYN- pulses at U116-9 go low at the beginning of each subsector of data. When each SCSYN- pulse goes high (false), counter U127 is clocked and advanced one count.

There are 16 subsectors in each of the 32 sectors on a track. The subsectors are numbered 0 through 15. The sectors in each track are numbered 0 through 31. When subsector operation is used, the DB00 through DB03 signals applied to register U99 select the subsector starting address and the DB11 through DB15 signals applied to registers U113 and U74 select the sector starting address. When sector operation is used, only the DB11 through DB15 signals are used. The outputs from register U99, U74 and U113 are each applied to a separate input of an exclusive OR gate, U100, U88 and U114.

The outputs from counters U127, U128 and U129 are also each applied to a separate input of an exclusive OR gate (U100, U88 and U114) through E pins E29 through E40. The E pins are wired for the required interlace factor of 1:1, 2:1, 4:1, or 8:1 (refer to chapter 2).

The following theory of operation is given for a selection of subsector 1 of sector 1 as the starting address with an interlace factor of 1:1. When counter U127 has counted 17 SCSYN- pulses, the outputs from U127-5 and U128-5 are high. The high output from
Ul27-5 (LCAA) is connected through E19 and E40 to pin 5 of exclusive OR gate U100. Since subsector 1 is the starting subsector address loaded into U99, the input to U100-4 is high. With high inputs at U100-5 and 4, the output from U100-6 goes low. This low output is inverted by U101, and the output at U101-10 goes high.

The high output from U128-5 (LCEE) is applied through E23 and E30 to pin 2 of exclusive OR gate U88. Since sector 1 is the starting sector address loaded into U74, the input to U88-1 is high. With high inputs at U88-2 and 1, the output at U88-3 goes low. This low output is inverted by U115, and the output at U115-4 goes high.

With high outputs now at U101-10 and U115-4, all outputs from all inverters U101 and U115 connected to U104-4 are then high. Since the SEQLEN flip-flop U76 was set when the TO (track origin) signal went high at the start of the disc revolution, the input to U104-5 is also high. This causes the SEQL- signal at U104-6 to go low, and the SEQL signal at U96-12 to go high, indicating sector equal. The SEQL and SEQL- signals are applied to the logic in the read/write sector control circuit (refer to the Read/Write Sector Control Circuit Description).

When the DSCRDY signal goes low, indicating disc not ready, or the UACHG- signal at U75-8 goes low, or the RST- signal goes low during the reset function, the SEQLEN flip-flop is reset. This inhibits the SEQL and SEQL- signals by applying a low input to U104-5.

**BUFFER AND DATA REGISTER TRANSFER CONTROL (1940083, SHEET 5)**

The buffer and data register transfer control logic circuit generates the BFLDPS- signals that are used to transfer data during the write operation, the DRSETBF- signals that are used to transfer data during the read operation, and the DRSET signals that are used to transfer data during both the write and read operations. It also contains the DRFUL flip-flop which controls the generation of the BFLDPS- and DRSETBF- signals and applies control signals to the data channel transfer control circuit.

**4-65 During Write Operation**

At the beginning of the write operation, the DRFUL flip-flop U38 is reset. When the DCHO signal from the processor is sent to the data channel transfer control circuit, the DRSETPS- signal at U14-13 and U68-13 goes low. This causes the DRSET signal at U14-11 to go high (refer to the memory buffer and register loading circuit description). This also causes the output at U68-8 to go low, applying a low input at the clock input of flip-flop U38. When the DRSETPS- signal goes high (false), flip-flop U38 is set by the low to high transition at its clock input. This enables gate U40 with a high input at U40-5. Since the memory buffer is not full at this time and the WROP flip-flop is set, the inputs to U40-2 and U40-4 are also high. This causes the output from U40-6 to go low and the input to U39-13 to go high. Since neither the cyclic cycle flip-flop or the parity cycle flip-flop is set at this time and the bit and word control counter is not between a count 13 to 16, the output from U54-6 is high. This applies a high input to U39-12. With high inputs at U39-12 and 13, flip-flop U38 is conditioned with a high input at U38-2.

Flip-flop U36 is set on the positive edge of every other WCLKD1 clock pulse applied to its clock input (pin 11). When U36 is set, the high output from U36-9 sets flip-flop U38. This causes the input to U40-1 to go high and the BFLDPS- signal at U40-12 to go low (true). The BFLDPS- signal is applied to the memory buffer and register loading circuit (refer to the Memory Buffer and Register Loading Circuit Description). The low
BFLDPS- signal is also applied to U68-9, causing a low input to the clock (U38-11) of the DRFUL flip-flop U38. When the BFDP- signal goes high (false), the DRFUL flip-flop U38 is reset. In this manner, a BFLDPS- and a DRSET signal are generated for each DCHO signal sent from the processor. After 13 bits have been written in each word, the BFPSINH- signal at U54-4 goes low. This inhibits the BFLDPS- signal until the first bit of the next word has been written. If the memory becomes full, the BFLDPS- signal is inhibited by a low input to U40-3.

When the CCYL flip-flop is set for the writing of the cyclic code word, the input to U54-5 goes low. This inhibits the generation of the BFLDPS- signal. When the PTYCYL flip-flop is set for the writing of the parity bit, the input to U54-5 again goes low. This inhibits the generation of the BFLDPS- signal. Finally, when the ENDSTR one shot is triggered at the end of the subsector, the low input to U54-3 inhibits the BFLDPS- signal until the ENDSTR one-shot times out.

During Read Operation

At the beginning of the read operation, the DRFUL flip-flop, U38, is reset. This causes a high input to U52-5. Since the RDOP flip-flop is set, the input to U52-3 is high. After 16 bits are in shift registers U57 through U60, the BFLD- signal is generated. When the BFEMTY- signal goes high, the buffer contents counter counts up one count. This causes the BFEMTY- signal at U52-4 to go high and the output from U53-6 to go low. This causes a high input to U39-13. Since neither the CCYL or PTYCYL flip-flops are set at this time, the bit and word control counter has not counted to 13 and the ENDSTR one-shot has not been triggered, the output from U54-6 is high and the input to U39-12 is high. With high inputs at U39-12 and 13, flip-flop is conditioned with a high input at U38-2. When flip-flop U36 is set, the high output from U36-9 sets flip-flop U38, and the output from U38-5 goes high. This high output is applied to U40-9. When the WCLKD clock pulse goes low, the DRSETBF- signal at U40-8 goes low. The DDSETBF- signal is applied to the memory buffer and register loading circuit (refer to the Memory Buffer and Register Loading Circuit Description).

The low DRSETBF- signal is also applied to U68-10 and U14-12. The low input to U14-12 causes the DRSET signal at U14-11 to go high (refer to the Memory Buffer and Register Loading Circuit Description). The low input to U68-10 causes the output from U68-8 to go low. This applies a low input to the clock input (pin 11) of the DRFUL flip-flop U38. When the DRSETBF- signal goes high (false), the low to high transition at U38-11 sets the DRFUL flip-flop U38.

When the DCHI signal is sent from the processor, the DRAVL- signal at U68-12 goes low. This causes a low input to U38-11. When the DRAVL- signal goes high (false), the low to high transition at U38-11 resets the DRFUL flip-flop U38. Another DRSETBF- signal is then generated in the manner previously described.

When each DRAVL- signal is applied to U68-12, a DRSETBF- signal is generated. When the sector bit and word control counter has counted to 14 bits, the input of U54-4 goes low, inhibiting the DRSETBF- signal until the second bit of the next word. When the CCYL flip-flop is set for the reading of the parity bit, the input to U54-5 goes low. This again inhibits the generation of the DRSETBF- signal. Finally, when the ENDSTR one-shot is triggered at the end of the subsector, the low input to U54-3 inhibits the DRSETBF- signal until the ENDSTR one-shot times out.
The buffer contents counter is composed of 4-bit up/down binary counters U42 and U41 and associated logic circuitry connected as a 5-bit up/down binary counter. The counter counts up one count when each data word is written into memory buffers U43 through U46 and counts down one count when each word is read out of memory buffers U43 through U46. The buffer condition decoder is composed of U12-13 and U13-12. The buffer condition decoder detects a full condition memory buffers U43 through U46 by decoding the outputs from the counter logic.

4-68  During Write Operation

At the beginning of the write operation, counter U42 is loaded to a programmed 15 count by the low INIT-A signal applied to U42-11. Since the BUFFS signal at U41-15 is high only the diagnostic read mode, counter U41 is programmed to zero by the INIT-A signal applied to U41-11.

The BLDF- signal applied to U6-13 goes low when each word is written into memory buffers U43 through U46. When the BFLD- signal goes false U42-5 goes high. This causes U42 to count up one count (reset to zero count), since the input at U42-4 is high at this time. Since the carry from U42-12 was applied to U41-5 when counter U42 was programmed to 15, the output from U41-3 goes high when U42 counts up. The output from U41-3 is inverted by U13 and applied to U12-12 and to various control circuits on the Nova adapter BWBA and formatter PWBA. As additional words are written into the memory buffers, counter U42 is advanced when each BFLD- pulse goes high. When the WSGO signal goes low, the SRLD signal goes low, and the first word is read out of the memory buffers and loaded in parallel into shift registers U57 through U60.

When the SRLD- signal at U65-4 goes low to high it applies a high input to U42-4. Since the input to U42-5 is high at this time, counter U42 counts down one count. Another word is then written into the memory buffers, and counter U42 counts up one count as previously described. The next word is then transferred to the shift registers, and counter U42 counts down one count as previously described. This sequence continues until only one word is left to be read out from the memory buffers. At this point, counter U42 has counted down to zero, and the borrow output from U42-13 is applied to U41-4. When the next SRLD- pulse goes high (false), counter U42 outputs go to the count of 15, and counter U41 output U41-3 goes low. Since the BFEMTY- signal is U41-3, the BFEMTY signal is then low and the BFEMTY signal at U13-10 is then high, indicating buffer empty.

4-69  Buffer Condition Decoder

When memory buffers U43 through U46 are full (contain 16 words), the full condition is detected by the buffer condition decoder composed of NAND gate U12 and inverter U13. When the buffer contents counter has counted up to 16, the outputs from U42-3, 2, 6 and 7 go high and the output from U41-3 is high. This caused the outputs from U28-6 and U13-10 to go low. These low outputs are applied to U12-11 and U12-12 respectively. This causes the BFFUL signal at U12-13 to go high and the BFFUL- signal at U12-2 to go low, indicating a buffer full condition. The BFFUL and BFFUL- signals are applied to various control circuits on the Nova adapter PWBA and formatter PWBA.
During Read Operation

During a read operation, counters U42 and U41 operate in a similar manner to their operation during a write operation, except that the DRSETBF- signal at U65-5 is used for the count-down function instead of the SRLD- signal at U65-4. The BFLD- signal at U6-13 is also used for the count-up function during a read operation. As each word is read from the disc and written into memory buffers U43 and U46, counter U42 is advanced one count when the BFLD- pulse goes high (false). As each word is read out of the buffer memories and transferred to the processor, counter U42 counts down one count when the DRSETBF- signal goes high. The final count down of the buffer contents counter is the same as during a write operation.

During Diagnostic Read Operation

At the start of a diagnostic read operation, the BUFFS signal at U41-15 goes high. When the INIT-A signal is applied to U42-11 and U41-11, counter U42 is loaded to a programmed 15 count and counter U41 is loaded to a programmed 1. This is required because a diagnostic read operation may be performed without a preceding diagnostic write operation, since the readout from memory buffers U43 through U46 is non-destructive. In this case the buffer contents counter would be in the empty condition with the output from U41-3 low. Loading counters U41 to a programmed 1 count places the buffer contents counter in the full condition.

CYCLIC CODE GENERATOR, PARITY BIT GENERATOR AND READ CHECK ERROR CIRCUITS (1940083, SHEET 5)

The cyclic code generator generates the 16-bit cyclic code word that is written at the end of each subsector of data. The parity bit generator generates the odd parity bit that is written after the cyclic code word at the end of each subsector of data.

When the cyclic code word and the odd parity bit are read at the end of each subsector, they are compared against a cyclic code word and odd parity bit that is generated by the cyclic code generator and parity bit generator for the 16 words of data that have been read. If the cyclic code words or odd parity bits differ, the RDER (read error) signal is generated by the read check error circuit.

During Write Operation

At the start of each subsector, the SCLK signal at U80-9 and U80-10 (A20) goes high. This causes the output from U80-8 to go low, presetting the PTY flip-flop U79 and clearing shift registers U84, U97 and U82 and flip-flops U94 and U93.

When the subsector and/or sector address is equal to the outputs from the sector counter (current location counter), the WRL flip-flop is set in the read/write sector control circuit. This causes the WRL signal at U112-4 (C20) to go high. The WR DATA signal at U112-5 goes high each time a logical 1 bit is written and goes low each time a logical 0 bit is written.

The output from U112-6 is applied to U98-2 and to U90-1. The output from U98-3 is determined by the logical state of the signal at U112-4 and the state (set or reset) of flip-flop U93-9. The output from U98-3 is applied to pins 2 and 3 of 4-bit shift register U84 and to exclusive OR gates U98. The output from U98-8 conditions U94-12 with a high or low input, depending upon the state of flip-flop U94-5 and the output from U98-3. The
output from U98-11 conditions U93-12 with a high or low input, depending upon the state of flip-flop U93-5 and the output from U98-3.

The three shift registers U84, U97 and U82 (A20, B20) and the four flip-flops U94 and U93 (A19) are clocked by the trailing edge of the SRCLKW- pulses applied from U80-11. The inputs to shift register U84 are shifted in the direction from QA toward QD with each SRCLKW- pulse. The output from QD (U84-12) is a complemented output that is applied to exclusive OR gate U98-5. The output from U98-6 depends upon the logical state of the signal at U112-5 and the logical state of the output from U84-12. Shift registers U97 and U82 also shift in the direction from QA toward QD with each SRCLKW- pulse and provide complemented outputs at QD.

When the last data word is written, the CCYL flip-flop in Sheet 2 (C8) is set. The 16 bits of the cyclic code word are then written, shifting the bits in a direction from QA to QD in U84 (sheet 5, B20) toward flip-flop U93-9 (CCG16). Each time that flip-flop U93-9 is set, the CCG16- output from U93-8 goes low. This writes a logical 1 bit in the cyclic code word, since the CCG16- signal is applied to the AND/OR invert circuit that conditions the write data-signal flip-flop. Each time the flip-flop U93-9 is reset, a logical 0 bit is written in the cyclic code word.

The parity flip-flop U79 (A19) changes state with each logical 1 bit (high input) applied to U112-5. If there was an odd number of logical 1 bits written in the subsector (including the cyclic code word), flip-flop U79 will be in the reset state when the parity bit is to be written (after the PTYCYL flip-flop is set in the cyclic cycle, parity cycle, and end control circuit in sheet 5). This causes a logical 0 to be written (odd parity) since the low PTY- output from U79-6 is applied to the AND/OR invert circuit that conditions the write data-signal flip-flop. The cyclic code word has the characteristic that if an even number of logical 1 data bits are written in the subsector it will have odd parity and if an odd number of logical 1 bits are written in the subsector it will have an even parity.

During Read Operation And Read Check Error

During a read operation, the RDL signal at U112 (C20) goes high when the RDL flip-flop is set in the read/write sector control circuit. The RD DATA signal at U112-3 goes high when each logical 1 bit is read from the disc. The operation of the circuit is the same as during a write operation, except that the SRCLKR- pulses at U80-13 are used in place of the SRCLKW- pulses at U80-12 (A20).

When the last data word is read in the subsector, the CCYL in sheet 2 (CB) flip-flop is set. The cyclic code word is then read. If the cyclic code word generated by the cyclic code generator for the data bits read in the subsector is the same as the cyclic code word read from the disc, the outputs from U83-6, U83-8, and U81-6 are high and the CCGNZR signal at U92-6 goes low. If any of the outputs are low, the CCGNZR signal at U92-6 goes high. This output is applied to U77-13 (sheet 2, D8). Since the BCNT15 signal at U77-2 (D8) and the CCYL signal at U77-1 are high at this time, flip-flop U79 is conditioned with a high input of U79-12. When the SRCLKR- pulse occurs, flip-flop U79 is set. This causes the RDER signal at U79-9 to go high, indicating a CRC error (D6). The RDER signal is applied to the error register on the formatter/adapter common bus and causes a logical 1 in bit 15 of the error bits.

When the PTYCYL flip-flop (C8) is set, the input to U78-4 goes high. If the PTY flip-flop U79 (A18) is set at this time, the input of U78-5 (D8) is high. This conditions flip-flop U79 with a high input to U79-12 (D7). When the SRCLKR- (D8) pulse occurs, flip-flop U79 is set. This causes the RDER signal at U79-9 to go high indicating a parity error,
since the PTY signal at U78-5 (D8) should have been low if an odd number of logical 1 bits were read in the subsector.

In either case of a read check error, the low output from U79-8 (D7) is applied to U79-9 and inhibits any additional clocking of flip-flop U79.

4-75 Disc Interface Signals

The WRITE flip-flop U122 (B17) is conditioned with a high input at U122-2 when the WRITE flip-flop is set in the read/write sector control circuit (C2). This occurs when the sector address is equal to the outputs from the sector counter in the sector equal detection circuit and causes the SEQL signal to go high (true). At this time the WRL- signal at U108-1 and 13 (B18) goes low. Since the CCYL and PTYL flip-flops are reset at this time, three of the four inputs to NOR gate U108 of AND/OR invert gates U108 are low. If the SR00 signal at U108-4 is low, the output from U108-8 goes high, conditioning flip-flop U122 with a high input at U122-12. If a SR00 signal at U108-4 is high, the output from 108-8 goes low, conditioning flip-flop U122 with a high input at U122-12. The WRITE flip-flop U122 is reset by either the power on reset (POR) signal from sheet 6 or initiate A (INIT-A) signal from the adapter board. When the WCLK signal occurs, it causes the output from U122-5 to go high, causing the WRITE signal to go low. This is used in power cycling feature contained in the description of sheet 6. Depending upon the logical state of the signal at U108-4, the write data- signal at J3-35 goes either low or high.

During the writing of the cyclic code word, the CCYL signal at U108-3 goes high, and the CCYL signal at U108-5 goes low. This again produces low inputs at three of the four inputs to NOR gate U108. Depending upon the logical state of the CCG16 signal at U108-2, the write data- signal goes either low or high.

When the odd parity bit is written, the PTYCYL signal at U108-10 goes high. This again produces low inputs at three of the four inputs to NOR gate U108. Depending upon the logical state of the PTY- signal at U108-9, the write data- signal goes either low or high when the WCLK clock pulse occurs.

The READ flip-flop U106 is conditioned with a high input at U106-2 when the RDL flip-flop is set in the read/write sector control circuit. This occurs when the sector address is equal to the outputs from the sector counter in the sector equal detection circuit and causes the SEQL- signal to go true (low). When the WCLK clock pulse occurs, flip-flop U106 is set. This causes the input to U19-5 to go high. If the address for the read operation is legal, the input to U19-4 is high. This causes the read- signal to the disc memory unit at J3-27 to go low (true).

4-76 POWER CYCLING (1940083, SHEET 6)

If there is a power loss the voltage is detected early enough so that a protective action is taken before the circuit elements lose their normal bias voltage. This is done through power on reset (POR) signal (B22) and WRITE signal (B17).

When power on reset (POR) signal detects a voltage of less than 4.2 volts over 50 ± 10 µsec, it resets the disc WRITE flip-flop U122 (B17). The output WRITE causes the Q7 (D23) to clamp on the write circuit and force it to its nonactive state. When the voltage source becomes greater than 4.50 volts for over 100 ± 30 msec, the write circuit is enabled.
Chapter 5

MAINTENANCE
MAINTENANCE

5-1 INTRODUCTION

This chapter provides troubleshooting procedures confined in replacing the PC boards and/or the power supply.

5-2 TROUBLESHOOTING TOOLS

The tools needed for such limited troubleshooting are as follows:

1. Digital volt-ohmmeter.
2. Standard field service tool kit

5-3 TROUBLESHOOTING PROCEDURES

If all equipment external to the controller are functioning properly, the following outline is used to isolate a malfunction via board level of maintenance.

a. Verify that all cables are connected according to figure 2-1. Make sure that cable connectors are properly seated.

b. Verify that the adapter board is plugged into the Nova computer I/O slot.

c. Verify that the power switch on the assembly formatter assembly front panel is in the ON position and that the fuse located at the rear of the chassis is installed and functioning.

d. Remove top cover from formatter assembly chassis. With the volt-ohmmeter, check for +5 volts at the J4-5 on the formatter PC board. Voltage should be:

\[ 5 \text{ volts} \pm 1\% \text{ (with J4 connected)} \]

If voltage is not within the above values, make the adjustment according to the following step.

e. Remove formatter PC board hold-down clamp by removing two screws. Rotate the front of the hinged PC board upward. The adjustment pot can be accessed through the round hole located inside the chassis in the back right-hand corner. If power supply cannot be adjusted according to specification,
it must be replaced according to paragraph 5–4 and the defective power supply routed for repair.

f. If the malfunction is not isolated by the steps above, replace the formatter PC board and run diagnostics to check it out. If problem persists, replace adapter PC board. Again run diagnostics. If a defective board is found, route it for repair. If problem remains, the malfunction is likely located in the external equipment or in defective cable.

5–4 POWER SUPPLY REMOVAL AND REPLACEMENT

The following steps may be used in order to remove and replace the power supply.

a. Remove both top and bottom chassis covers from formatter assembly.

b. Unplug J4 connector from formatter PC board.

c. Unplug both J1 and J2 connectors located in power supply.

d. Remove four screws from bottom of chassis to free power supply.

e. Remove power supply from chassis and route for repair.

f. Reverse above steps to install new power supply.

g. Check new power supply according to the procedure described in step d of paragraph 5–3.
Chapter 6

DRAWINGS AND PARTS LISTS
DRAWINGS AND PARTS LISTS

6-1 INTRODUCTION

This chapter contains the drawings required to maintain the 8011 Disc Memory Controller. A list of replaceable parts is also included.

6-2 DRAWINGS

Table 6-1 lists the drawings contained in this chapter. These are assembly schematic and wiring diagrams. The partial drawing tree in figure 6-1 shows the order in which the drawings apply to the controller.

<table>
<thead>
<tr>
<th>DRAWING No.</th>
<th>DRAWING TITLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1040027</td>
<td>Adapter PC Board Assembly</td>
</tr>
<tr>
<td>1940027</td>
<td>Adapter PC Board Schematic</td>
</tr>
<tr>
<td>1040083</td>
<td>Formatter PC Board Assembly</td>
</tr>
<tr>
<td>1940083</td>
<td>Formatter PC Board Schematic</td>
</tr>
<tr>
<td>1020129</td>
<td>Formatter Assy</td>
</tr>
<tr>
<td>1940080</td>
<td>Connector Interface Board</td>
</tr>
<tr>
<td>1940081</td>
<td>Connector Interface Board</td>
</tr>
<tr>
<td>1930025</td>
<td>System Interconnect Diagram</td>
</tr>
<tr>
<td>1060019</td>
<td>Cable Assembly</td>
</tr>
<tr>
<td>1060024</td>
<td>CPU A Cable Assembly</td>
</tr>
<tr>
<td>1060025</td>
<td>CPU B Cable Assembly</td>
</tr>
<tr>
<td>1020093</td>
<td>Rear Panel Assembly</td>
</tr>
<tr>
<td>1930003</td>
<td>Power Supply Wiring Diagram</td>
</tr>
</tbody>
</table>

6-3 PARTS LIST

A list of replaceable parts for the adapter and formatter PC boards is given in table 6-2.
NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL PART & ASSEMBLY DASH NUMBERS ARE -01.

Figure 6-1. 8011 Disc Memory Controller Drawing Tree (Partial)
<table>
<thead>
<tr>
<th>AMCOMP PART No.</th>
<th>DESCRIPTION/LOCATION</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADAPTER PC BOARD COMPONENTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1040027</td>
<td>Adapter PC Board Assembly</td>
<td>1</td>
</tr>
<tr>
<td>04122221-01</td>
<td>Res. Fxd, 220 ohms, 1/2 w, 5%/R7, R8, R11, R13, R16, R17, R19, R24, R33, R36, R37, R39, R41, R44, R46, R47, R49, R52, R54, R55, R57, R60, R62, R63, R65, R68, R70, R72, R76, R80</td>
<td>30</td>
</tr>
<tr>
<td>04122331-01</td>
<td>Res. Fxd, 330 ohms, 1/2 w, 5%/R6, R9, R10, R14, R15, R18, R20, R23, R34, R35, R40, R38, R42, R43, R45, R48, R50, R51, R53, R58, R59, R56, R61, R64, R66, R67, R69, R71, R75, R79</td>
<td>30</td>
</tr>
<tr>
<td>04122102-01</td>
<td>Res. Fxd, 1K ohms, 1/2 w, 5%/R1, R2, R3, R4, R5, R12, R21, R22, R25, R26, R27, R28, R29, R30, R31, R32, R73, R74, R77, R78, R81</td>
<td>21</td>
</tr>
<tr>
<td>01400101-27</td>
<td>Cap. Fxd., Cer., 100 pf, 100v, 10%/C1 through C15</td>
<td>15</td>
</tr>
<tr>
<td>01400106-01</td>
<td>Cap. Fxd., Cer., .01 μf/C18 through C71</td>
<td>54</td>
</tr>
<tr>
<td>01383201-01</td>
<td>Cap. Fxd., Mica 200 pf, 500v, 5%/C16</td>
<td>1</td>
</tr>
<tr>
<td>01400109-21</td>
<td>Cap. Fxd., Mold Cer. 470 pf, 200v, 5%/C17</td>
<td>1</td>
</tr>
<tr>
<td>01200104-03</td>
<td>Cap. Fxd., Tant. 15 μf, 10v, 20%/C72 through C77</td>
<td>6</td>
</tr>
<tr>
<td>03201101-01</td>
<td>I.C., 14 pins, 7400/U2, U4, U9, U28, U55</td>
<td>5</td>
</tr>
<tr>
<td>03201142-01</td>
<td>I.C., 14 pins, 7402/U41, U42</td>
<td>2</td>
</tr>
<tr>
<td>03201109-01</td>
<td>I.C., 14 pins, 7410/U3, U16, U17, U21, U53, U57</td>
<td>6</td>
</tr>
<tr>
<td>03201123-01</td>
<td>I.C., 14 pins, 7474/U49, U54, U56, U60, U61, U62</td>
<td>6</td>
</tr>
<tr>
<td>03201104-01</td>
<td>I.C., 14 pins, 7404/U7, U18, U40, U53</td>
<td>4</td>
</tr>
<tr>
<td>03201118-01</td>
<td>I.C., 14 pins, 7473/U14</td>
<td>1</td>
</tr>
<tr>
<td>03201134-01</td>
<td>I.C., 16 pins, 74193/U43, U44, U46, U48</td>
<td>4</td>
</tr>
<tr>
<td>03201111-01</td>
<td>I.C., 14 pins, 74H11/U15</td>
<td>1</td>
</tr>
<tr>
<td>03201108-01</td>
<td>I.C., 14 pins, 7408/U1, U20, U27, U59</td>
<td>4</td>
</tr>
<tr>
<td>03201119-01</td>
<td>I.C., 14 pins, 7438/U5, U8, U23, U24, U25, U26</td>
<td>6</td>
</tr>
<tr>
<td>03201128-01</td>
<td>I.C., 14 pins, 74197/U36, U37, U38, U39</td>
<td>4</td>
</tr>
<tr>
<td>03201114-01</td>
<td>I.C., 14 pins, 7417/U6, U19, U22</td>
<td>3</td>
</tr>
<tr>
<td>03100111-02</td>
<td>I.C., 16 pins, 75138/U30, U31, U33, U35</td>
<td>4</td>
</tr>
<tr>
<td>03201138-01</td>
<td>I.C., 16 pins, DS8838/U10, U11, U12, U13</td>
<td>4</td>
</tr>
<tr>
<td><strong>FORMATTER PC BOARD COMPONENTS</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1040083</td>
<td>Formatter PC Board Assembly</td>
<td>1</td>
</tr>
<tr>
<td>07100898-40</td>
<td>Connector, 50-pin/J1, J2, J3</td>
<td>3</td>
</tr>
</tbody>
</table>
### TABLE 6-2. REPLACEABLE PARTS LIST (continued)

<table>
<thead>
<tr>
<th>AMCOMP PART No.</th>
<th>DESCRIPTION/LOCATION</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FORMATTER PC BOARD COMPONENTS (continued)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>47080101-01</td>
<td>Header Assembly, 10-pin, right angle/J4</td>
<td>1</td>
</tr>
<tr>
<td>04122100-01</td>
<td>Res., 10 ohms, 1/4 w, 5%/R91</td>
<td>1</td>
</tr>
<tr>
<td>04122220-01</td>
<td>Res., 22 ohms, 1/4 w, 5%/R69</td>
<td>1</td>
</tr>
<tr>
<td>04122101-01</td>
<td>Res., 100 ohms, 1/4 w, 5%/R1</td>
<td>1</td>
</tr>
<tr>
<td>04122151-01</td>
<td>Res., 150 ohms, 1/4 w, 5%/R2, R17, R21, R37, R68, R81</td>
<td>6</td>
</tr>
<tr>
<td>04122221-01</td>
<td>Res., 220 ohms, 1/4 w, 5%/R46, R53, R72, R75, R92</td>
<td>5</td>
</tr>
<tr>
<td>04122271-01</td>
<td>Res., 270 ohms, 1/4 w, 5%/R79</td>
<td>1</td>
</tr>
<tr>
<td>04122331-01</td>
<td>Res., 330 ohms, 1/4 w, 5%/R45, R52</td>
<td>2</td>
</tr>
<tr>
<td>04122471-01</td>
<td>Res., 470 ohms, 1/4 w, 5%/R67</td>
<td>1</td>
</tr>
<tr>
<td>04122511-01</td>
<td>Res., 510 ohms, 1/4 w, 5%/R11, R14, R23 through R31, R34, R35, R36, R43, R56</td>
<td>18</td>
</tr>
<tr>
<td>04122561-01</td>
<td>Res., 560 ohms, 1/4 w, 5%/R71, R78, R88, R90</td>
<td>4</td>
</tr>
<tr>
<td>04122621-01</td>
<td>Res., 620 ohms, 1/4 w, 5%/R83</td>
<td>1</td>
</tr>
<tr>
<td>04122102-01</td>
<td>Res., 1K ohms, 1/4 w, 5%/R6, R7, R15, R18, R19, R33</td>
<td>27</td>
</tr>
<tr>
<td>04122122-01</td>
<td>Res., 2.2K ohms, 1/4 w, 5%/R74, R76, R89, R96</td>
<td>4</td>
</tr>
<tr>
<td>04122222-01</td>
<td>Res., 2.2K ohms, 1/4 w, 5%/R74, R76, R89, R96</td>
<td>4</td>
</tr>
<tr>
<td>04122272-01</td>
<td>Res., 2.7K ohms, 1/4 w, 5%/R98</td>
<td>1</td>
</tr>
<tr>
<td>04122472-01</td>
<td>Res., 4.7K ohms, 1/4 w, 5%/R87, R93, R94</td>
<td>3</td>
</tr>
<tr>
<td>04122510-01</td>
<td>Res., 51 ohms, 1/4 w, 5%/R69</td>
<td>1</td>
</tr>
<tr>
<td>04122622-01</td>
<td>Res., 6.2K ohms, 1/4 w, 5%/R10</td>
<td>1</td>
</tr>
<tr>
<td>04122822-01</td>
<td>Res., 8.2K ohms, 1/4 w, 5%/R16, R40, R41</td>
<td>3</td>
</tr>
<tr>
<td>04122103-01</td>
<td>Res., 10K ohms, 1/4 w, 5%/R82</td>
<td>1</td>
</tr>
<tr>
<td>04122123-01</td>
<td>Res., 12K ohms, 1/4 w, 5%/R85</td>
<td>1</td>
</tr>
<tr>
<td>04122393-01</td>
<td>Res., 39K ohms, 1/4 w, 5%/R9</td>
<td>1</td>
</tr>
<tr>
<td>04122623-01</td>
<td>Res., 62K ohms, 1/4 w, 5%/R73</td>
<td>1</td>
</tr>
<tr>
<td>04444502-01</td>
<td>Res., Variable, 5K/R70</td>
<td>1</td>
</tr>
<tr>
<td>04551331-01</td>
<td>Res., Net Dip, 330/RN2, RN5, RN7, RN9, RN11, RN13, RN15, RN3</td>
<td>8</td>
</tr>
<tr>
<td>04551221-01</td>
<td>Res., Net Dip, 220/RN1, RN4, RN6, RN8, RN10, RN12, RN14, RN16</td>
<td>8</td>
</tr>
<tr>
<td>02100914-03</td>
<td>Diode, IN914B/CR1-CR3, CR5-CR10</td>
<td>9</td>
</tr>
<tr>
<td>02100102-01</td>
<td>Diode, IN4454/CR4</td>
<td>1</td>
</tr>
<tr>
<td>05100104-01</td>
<td>Transistor, 2N3646/Q5-Q8</td>
<td>4</td>
</tr>
<tr>
<td>01383101-01</td>
<td>Cap., 100 pf, 500v, 5%/C59, C60, C28</td>
<td>3</td>
</tr>
<tr>
<td>01400109-16</td>
<td>Cap., 180 pf, 200v/C31</td>
<td>1</td>
</tr>
<tr>
<td>01383221-01</td>
<td>Cap., 220 pf, 500v, 5%/C33, C40, C57</td>
<td>3</td>
</tr>
<tr>
<td>01383201-01</td>
<td>Cap., 200 pf, 500v, 5%/C1, C2</td>
<td>2</td>
</tr>
<tr>
<td>01400101-52</td>
<td>Cap., 1000 pf/C19, C72</td>
<td>2</td>
</tr>
<tr>
<td>01400106-01</td>
<td>Cap., 01 µf, 16v/C8-C14, C17, C18, C20-C26,</td>
<td>94</td>
</tr>
</tbody>
</table>
## TABLE 6-2. REPLACEABLE PARTS LIST (continued)

<table>
<thead>
<tr>
<th>AMCOMP PART No.</th>
<th>DESCRIPTION/LOCATION</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>FORMATTER PC BOARD COMPONENTS (continued)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C30-C32, C34-C39, C43-C50, C53, C54, C55, C56, C58, C61, C62, C63, C64, C65, C68, C69, C70, C71, C73-C81, C84-C95, C98-C108, C111-C125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01200102-17 Cap., 2.2 µf, 20v/C128</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>01200104-04 Cap., 22 µf/C6</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>01225226-01 Cap., 22 µf, 15v, 20%/C7, C15, C16, C27, C29, C41, C42, C51, C52, C66, C67, C82, C83, C96, C97, C109, C110</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>01200103-31 Cap., 33 µf, 35v/C132</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>01200102-37 Cap., 100 µf, 20v/C129, C130</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>01225107-01 Cap., 100 µf, 20v/C3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201101-01 I.C., 14 pins, 7400/U78</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201142-01 I.C., 14 pins, 7402/U12, U90</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>03201130-01 I.C., 16 pins, 7445/U117</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201123-01 I.C., 14 pins, 7474/U25, U36, U53, U76, U79, U106, U122</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>03201102-01 I.C., 14 pins, 74H00/U14, U23, U104</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>03201104-01 I.C., 14 pins, 7404/U13, U22, U34, U86, U96, U116</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>03201120-01 I.C., 14 pins, 74H51/U112</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201110-01 I.C., 14 pins, 74H10/U20, U40, U50, U52, U55, U77, U123</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>03201105-01 I.C., 14 pins, 74H04/U105, U118, U119</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>03201107-01 I.C., 14 pins, 7405/U35, U101, U115</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>03201118-01 I.C., 14 pins, 7437/U80</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201124-01 I.C., 14 pins, 74H74/U38, U63, U67, U93, U94, U95, U109, U110</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>03201112-01 I.C., 14 pins, 7413/U49</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201134-01 I.C., 16 pins, 74193/U4, U42, U74, U99, U113</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>03201111-01 I.C., 14 pins, 74H11/U21, U54, U66, U75, U124</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>03201116-01 I.C., 14 pins, 74H21/U68, U87</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>03201108-01 I.C., 14 pins, 74H8/U24, U39, U48, U65, U85</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>03201121-01 I.C., 14 pins, 74H54/U108</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>03201133-01 I.C., 16 pins, 74161/U33, U69, U70, U61</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>03201139-01 I.C., 16 pins, 74123/U37, U64</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>03201122-01 I.C., 14 pins, 74H20/U28, U92</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>03201140-01 I.C., 16 pins, 7489/U43, U44, U45, U46</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>03201125-01 I.C., 14 pins, 7486/U88, U100, U114</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>03201143-01 I.C., 16 pins, 74157/U29, U30, U31, U32, U47</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>03201117-01 I.C., 14 pins, 7425/U56, U81, U83</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>03201119-01 I.C., 14 pins, 7438/U5, U19, U26, U102, U107, U120, U121</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>03201128-01 I.C., 14 pins, 74197/U71, U72, U73, U127, U128, U129</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>03201113-01 I.C., 14 pins, 7416/U7</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>AMCOMP PART No.</td>
<td>DESCRIPTION/LOCATION</td>
<td>QUANTITY</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------------------------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>03201114-01</td>
<td>I.C., 14 pins, 7417/U6, U11, U62, U103</td>
<td>4</td>
</tr>
<tr>
<td>03201115-01</td>
<td>I.C., 14 pins, 74S20/U51</td>
<td></td>
</tr>
<tr>
<td>03201126-01</td>
<td>I.C., 14 pins, 74S86/U89, U91, U98</td>
<td>3</td>
</tr>
<tr>
<td>03100111-02</td>
<td>I.C., 16 pins, 75138/U1, U2, U3, U4</td>
<td>4</td>
</tr>
<tr>
<td>03201144-01</td>
<td>I.C., 16 pins, 74195/U57, U58, U59, U60, U82, U84, U97</td>
<td>7</td>
</tr>
<tr>
<td>03201150-01</td>
<td>I.C., 16 pins, 74283/U130</td>
<td>1</td>
</tr>
<tr>
<td>03201135-01</td>
<td>I.C., 16 pins, 74298/U15, U16, U17, U18</td>
<td>4</td>
</tr>
<tr>
<td>03000102-01</td>
<td>I.C., 14 pins, 3046/U8</td>
<td>1</td>
</tr>
<tr>
<td>47210002-01</td>
<td>Wire-Wrap Pin/E1-E62</td>
<td></td>
</tr>
</tbody>
</table>
NOTES:
1. WORKMANSHIP SHALL COMPLY WITH QA-000000-00
2. IDENTIFY WITH APPROPRIATE ASY/PART NO.
3. MAXIMUM COMPONENT LEAD PROTECTION ON CIRCUIT SIDE OF BOARD SHALL BE .060

REVISIONS

PRE-PRCD RELEASE 0000-00
SE.E:... 00.03 02.02
S12.E 03 02
REVISiO PER 0122

DESCRIPTION REFERENCE SYMBOL
ADAPTER PWBA
1040027
NOTES

1. THIS ASSEMBLY SHALL BE IDENTIFIED BY ITS M/L NO. 100129-01
   P/N 100300.

2. WORKMANSHIP TO COMPLY WITH QA 100000-00.
### Wire Lead List

**NOTES:**
1. Connect as follows: P1/1 to P2/1, etc. thru P1/50 to P2/50.
2. Workmanship shall comply with QA100000-00.
3. Identify with Assy No 1060015-01 & Rev.

<table>
<thead>
<tr>
<th>ITEM</th>
<th>NO.</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
<th>REF DES</th>
<th>MFR</th>
<th>PART NO.</th>
<th>CODE</th>
<th>QTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>029-100</td>
<td>LABEL, ADHESIVE, BACK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>082-054</td>
<td>LOCK SCREW ASSY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>085-033</td>
<td>CABLE, FLAT, 50 CONDUCT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>088-020</td>
<td>BOOT, TELESCOPING</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>089-053</td>
<td>SHELL JUNCTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>089-052</td>
<td>CONNECTOR, 50 PIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>089-051</td>
<td>CONNECTOR, 50 PIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**List of Material**

**NOTICE**

- Unless noted, dimensions are in inches.
- Tolerance is ±0.005 unless noted.
- Standard tolerance unless noted.
- Use caution when handling.

- **DATE**: 10/11/77
- **APPRO**: 10/11/77

**Title**: CABLE ASSY, CPU CONTROLLER

**Scale**: 1/16" = 1" (0001"

**Drawing No.**: 1060019

**Drawn By**: P. M. L

**Comment**: Do not scale one.

**APP**: 10/11/77

**Signature**: P. M. L

**Drawing Completion**: 10/11/77

---

**Diagram**

- Pin 1
- Grooved Side
- Red Stripe
- Grooved Side

---

**Data Disc Incorporated**

**Incorporated Page A of 5**

---

**Printed on Ola'° NO. IO00001**

---
**WIRE LEAD LIST**

<table>
<thead>
<tr>
<th>ITEM</th>
<th>NO.</th>
<th>FROM</th>
<th>TO</th>
<th>REMARKS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>1</td>
<td>MARKER 63 VEL</td>
<td>TP</td>
<td>(CCYL-)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>MARKER 71 VEL</td>
<td>TP</td>
<td>(SCRPK)</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
<td>MARKER 75 VEL</td>
<td>TP</td>
<td>(ENDER)</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>MARKER 78 VEL</td>
<td>TP</td>
<td>(O'Brien)</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>MARKER 81 VEL</td>
<td>TP</td>
<td>(STATIN)</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
<td>MARKER 83 VEL</td>
<td>TP</td>
<td>(TSASSET)</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>MARKER 85 VEL</td>
<td>TP</td>
<td>(GALOS-)</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td></td>
<td>MARKER 85 VEL</td>
<td>TP</td>
<td>(DOCK)</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td></td>
<td>MARKER 87 VEL</td>
<td>TP</td>
<td>(RA1-)</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>37</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
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</tr>
<tr>
<td>40</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td></td>
<td>MARKER 40 VEL</td>
<td>TP</td>
<td>(BUFFS)</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46</td>
<td></td>
<td>GND</td>
<td>BPU</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. ATTACH WIRE MARKER TO SIGNAL END (YELLOW WIRE) OF EACH TWISTED PAIR AND AS WIRE LEAD LIST. TYPE IN CHARACTERS AS SHOWN.
2. WORKMANSHIP SHALL COMPLY WITH 9A100000-00.
3. IDENTIFY WITH ASSY NO. 1060024-01 & LATEST REV. THIS Dwg.

**FUNCTION**

- MARKER PLATES: CABLE IDENT.
- LABEL, SELF ADHESIVE.
- WIRE, GOLD TIP, 26G, BPU/VEL.
- TIE WRAP.
- TUBING, SHRINK.
- SCREW JACK, FEMALE.
- CONNECTOR, 50 PIN.

**LIST OF MATERIAL**

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>DESCRIPTION</th>
<th>REF DES</th>
<th>CODE IDENT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**REMARKS**

20.00 ± 0.05

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**NOTICE**

- NOTICE DETAILED MATERIAL LIST IS NOT SCALE DRAWING AND NOT CONSTRUCTIVE OF THE COMPLETE DRAWING. USE DRAWING NO. FOR CONSTRUCTION.

**SIGNATURE**

- DATE: 1/5/86

---

**PRODUCT DATA**

- NAME: CPU ASSY
- MODEL: CAFL ASSY, CPU A
- SCALE: 1/10
- SHEET: 1 OF 1
WIRE LEAD LIST

NOTES:
1. ATTACH WIRE MARKER TO SIGNAL END (YELLOW WIRE), OF EACH TWISTED PAIR, AS PER WIRE LEAD LIST.
2. TYPE IN CHARACTERS AS SHOWN.
3. WORKMANSHIP SHALL COMPLY WITH GA/100000-00
4. IDENTIFY WITH ASSY NO. 1060002-01 & LATEST REV.

![Diagram of wire lead list]

LIST OF MATERIAL

<table>
<thead>
<tr>
<th>NO.</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>069-055</td>
<td>CONNECTOR, 50 PIN</td>
</tr>
<tr>
<td>2</td>
<td>229-116</td>
<td>LABEL, SELF ADHESIVE</td>
</tr>
<tr>
<td>3</td>
<td>192-007</td>
<td>WIRE, SOLID, TPR, 2C, BLUE/ YELLOW</td>
</tr>
<tr>
<td>4</td>
<td>015-000</td>
<td>TIE WRAP</td>
</tr>
<tr>
<td>5</td>
<td>192-201</td>
<td>TUBING, SHRINK</td>
</tr>
<tr>
<td>6</td>
<td>089-207</td>
<td>SCREW JACK, FEMALE</td>
</tr>
<tr>
<td>7</td>
<td>229-176</td>
<td>MARKER PLATE, CABLE IDENT</td>
</tr>
</tbody>
</table>

NOTICE UNLESS NOTED SIGNATURE DATE

ATTACH WIRE MARKER TO SIGNAL END (YELLOW WIRE), OF EACH TWISTED PAIR, AS PER WIRE LEAD LIST.

WORKMANSHIP SHALL COMPLY WITH GA/100000-00

IDENTIFY WITH ASSY NO. 1060002-01 & LATEST REV.

DRAWING NO. 100000-00

DATE APPD.

SIGNATURE

DATE

TITLE

REVISION

INTEGRATED CIRCUIT ASSY, CPU B

CABLE ASSY, CPU B
<table>
<thead>
<tr>
<th>ITEM REQD</th>
<th>WIRE NO.</th>
<th>GAGE</th>
<th>COND</th>
<th>FROM</th>
<th>STA</th>
<th>COMP</th>
<th>PIN</th>
<th>STA</th>
<th>TO</th>
<th>REMARKS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITEM</td>
<td>45</td>
<td>LM</td>
<td></td>
<td>MARKER 60</td>
<td>YEL</td>
<td>TP</td>
<td>WRAP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>46</td>
<td>GND</td>
<td></td>
<td>BLU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ITEM</td>
<td>47</td>
<td>GND</td>
<td></td>
<td>MARKER 60</td>
<td>YEL</td>
<td>TP</td>
<td>WRAP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>48</td>
<td>GND</td>
<td></td>
<td>BLU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTICE**

UNLESS NOTED ON DRAWING, USE MTS-101, METAL LAUGER WIRE, COPPER ALLOY, SHIELDED, SOLDERABLE, IN ACCORDANCE WITH DRAWING 0000/0000.

DATE APPD: _ _ _ _

SIGNATURE: _ _ _ _

FILE DATED: _ _ _ _

COMP. PIN: _ _ _ _

SCALE: _ _ _ _

APPLICATION: _ _ _ _

CODE: _ _ _ _

MFR. PART NO.: _ _ _ _

IDENT: _ _ _ _

QTY REQD: _ _ _ _

**LIST OF MATERIAL**

**DATA DISC INCORPORATED**

Palo Alto, Calif.

---

RELEASE LEVEL = ENGR 2 LIMITED 1 PROD 1

REV. LEVEL = CABLE ASSY. CPU 'B' 

SIGNATURE: _ _ _ _

DATE APPD: _ _ _ _

APPROVED BY: _ _ _ _

DATE: _ _ _ _

REVISIONS

**LIST OF MATERIAL**

**DATA DISC INCORPORATED**

Palo Alto, Calif.

---

RELEASE LEVEL = ENGR 2 LIMITED 1 PROD 1

REV. LEVEL = CABLE ASSY. CPU 'B' 

SIGNATURE: _ _ _ _

DATE APPD: _ _ _ _

APPROVED BY: _ _ _ _

DATE: _ _ _ _

REVISIONS

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Palo Alto, Calif.

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SIGNATURE: _ _ _ _

DATE APPD: _ _ _ _

APPROVED BY: _ _ _ _

DATE: _ _ _ _

REVISIONS

**LIST OF MATERIAL**

**DATA DISC INCORPORATED**

Palo Alto, Calif.
NOTES:

1. IDENTIFY WITH ASSY PART NO. 1020093-02 AND CURRENT M/L REVISION PER 10500010.

ROUTE HARNESS AND CONNECTOR P1 THRU P3 THRU 10" X 20" CUTOUT IN ITEM I AS SHOWN.

ROUTE HARNESS AND CONNECTORS P4 & P5 THRU 10" X 20" CUTOUT IN ITEM I AS SHOWN.

ROUTE HARNESS AND CONNECTORS P1 & P2 THRU UPPER SLOT IN ITEM B AS SHOWN AND CONNECT P1 & P2 WITH J1 & J2, RESPECTIVELY.

IDENTIFY WITH ASSY PART NO. 1020093-02 AND CURRENT M/L REVISION PER 10500010.
APPENDIX A

USER'S GUIDE

FOR

8010 DISC MEMORY SYSTEM DIAGNOSTIC PROGRAM
A-1  INTRODUCTION

The 8010 Disc System Diagnostic Program is a maintenance program designed to test the AMCOMP 8010 Disc Memory System. Minimum machine requirements include a standard Nova processor with 8K of read/write memory, an AMCOMP 8010 Disc Memory System, and a teletype. Sufficient flexibility has been designed into this program to allow a wide range of disc system testing. The user may choose test functions as widely varied as looping on single bit exercises suitable for scope loops, to large scale data transfer and verification. The program consists of five different tests and numerous options. Combinations of these tests and options are selectable from the Nova's front panel data switches and the teletype such that the user may never have to directly alter the processor's memory.

A-2  LOADING AND STARTING

The medium of the AMCOMP 8010 Disc System Diagnostic Program load module is paper tape. This paper tape may be loaded from either the teletype or a high speed paper tape reader. In either case the program will be loaded using the Data General Binary Loader program which is loaded by the Data General Bootstrap Loader. The Data General Nova Processor User's Guide should be referred to for a complete description of these loaders. Once the program is successfully loaded it may be started by executing location 2. This may be accomplished by setting all the data switches except switch 14, which must be up, downward, then engaging the STOP, RESET and START switches in turn. The program will respond by prompting the user for the disc system device address by printing on the teletype the message:

8010 DISC SYSTEM TEST PROGRAM
TYPE 2 DIGIT DISK DEVICE CODE (20 OR 60)

The user should respond to this promptly by entering the disc system device address on the teletype. A response must always be 2 digits since the program waits for the second digit. A response other than 20 or 60 will cause the second half of the above message to be repeated. An improper response, i.e., a 60 for a system with a device address of 20 or vice versa, will cause multiple errors when executing test 1 of this program and the error message SOFTWARE TIMEOUT when executing any other test. Once the device code has been accepted by the program the message SET DATA SWITCHES-CONTINUE is printed on the teletype. In response to this message the user should select the desired options by manipulating the Nova's front panel data switches then depressing the CONTINUE switch which is also located on the Nova's front panel.
A-3 SWITCH FUNCTION AND SETTING

All 16 of the Nova's front panel data switches are used in this program. The switches are active (1) in their up position, and inactive (0) when depressed. Their assignments are as follows:

SWITCH

0 = Print instructions/Abort current test
1 = Halt on error
2 = Print test 4 cycle count
3 = Loop on selected test

4, 5, 6 Test selection
0 0 0 Tests 1 thru 4
0 0 1 Test 1 discrete controller tests
0 1 0 Test 2 diagnostic mode test
0 1 1 Test 3 sizing test
1 0 0 Data transfer (sector) test
1 0 1 Data transfer (subsector) test
1 1 0 Tests 1, 2 and 4
1 1 1 Tests 2 and 4

7 = Read only
8 = Write only
9 = Data error print inhibit
10 = Status error print inhibit
11 = End of test and test ID print inhibit
12 = 2 Reads per write inhibit

13, 14, 15 Select data pattern
0 0 0 Use all data patterns
0 0 1 Use random pattern
0 1 0 Use incrementing pattern
0 1 1 Use track/sector as pattern
1 0 0 Use worst case pattern (16142)
1 0 1 Use all ones
1 1 0 Use all zeroes
1 1 1 User selected pattern

SWITCH 0

The program instructions are printed if and when the program finds switch 0 to be in the up position when the CONTINUE switch has been depressed after the program has printed SET DATA SWITCHES - CONTINUE. These instructions are almost identical to the above description of the switch functions. In order to actually exercise any of the tests of this program the user must depress switch 0. If in the course of actually running any of the tests available in this program switch 0 is found to be set, the test being run will be aborted and the message SET DATA SWITCHES - CONTINUE will be printed. At this time the user may reselect the desired options, then restart the program by depressing CONTINUE.
SWITCH 1

If an error such as discrete test error, status error, data error, or software timeout error occurs during the running of any of the tests available in this program, and the program finds switch 1 to be set, the program will halt. This feature is useful when hardware conditions demand that the software does nothing to cover up a problem once a spurious hardware anomaly has been detected.

SWITCH 2

When, during the running of any of the tests of this program switch 2 is found to be set, the program will print the cycle count. The cycle count is set to zero at the start of the program (when the program prints SET DATA SWITCHES - CONTINUE) and incremented at the end of Test 4.

SWITCH 3

This switch may be used to cause the program to repeatedly execute a single test or a sub-test. As the program starts any of the tests, it determines whether switch 3 is set. If the switch is found to be set the program will demand the test dependent looping parameters from the user. If switch 3 is found to be set as test 1 is started, the program will print the message LOOP ON RNT# on the teletype. The user may then enter on the teletype a number, ranging from 1 to 53, corresponding to the desired test routine number. The program will then repeatedly execute only this desired sub-test for as long as switch 3 remains set. If switch 3 is found to be set when test 2 or test 3 is started, the program will execute repeatedly the particular test without a prompt message. If switch 3 is found to be set as test 4 is started the program will prompt the user with the message START SECTOR. The user should then enter the disc system disc/track/sector address (in octal) where the user desires test 4 to start its exercise. Next the program prompts the user with the message END SECTOR to which the user responds with the disc system disc/track/sector address (in octal) where he desires test 4 to end its exercise. The acceptable range of addresses is from a single sector (the desired start and end addresses are the identical) to all the sectors of the disc system. If switch 3 is found to be set when test 5 is started the program will again prompt the user with the messages START SECTOR then END SECTOR then START SUB SECTOR then END SUB SECTOR then NO. OF SUB SECTORS. To each of these messages the user must respond with the desired value. The acceptable range of values is from a single sub sector to the entire disc system. The number of sub sectors refers to the number of sub sectors that will be transferred per transfer and may be any value from 1 to 20 octal.

SWITCHES 4, 5, and 6

The user sets these switches to select the desired test or tests as detailed above. These switches are examined by the program when it is started (when the program has printed SET DATA SWITCHES - CONTINUE) and at the end of each test that is being looped on.

SWITCH 7

When set this switch causes the program to enter a read-only mode. This switch is ignored by tests 1 and 3. The user must ensure that the data read and the data expected to be read are identical; otherwise continuous data errors will result. The disc system should be written with a specific data pattern before read-only mode. This pattern should be the same with the one data was entered if data compare validity is desired by the user.
SWITCH 8

When set this switch causes the program to enter a write-only mode. This switch is ignored by tests 1 and 3.

SWITCH 9

This switch is examined by the program only once a data compare error has occurred. If the switch is found to be set no teletype print of the error condition is made. Otherwise a printout results as detailed as that in the error messages section of this manual.

SWITCH 10

This switch is examined by the program only once a status error has been detected by the program. No teletype print of the error is made if this switch is found to be set. Otherwise a printout results as detailed as that in the error messages section of this manual.

SWITCH 11

When set this switch inhibits the test identification and end of test messages that would otherwise be printed on the teletype as each test is started or completed.

SWITCH 12

The setting of this switch causes the program to issue only one read command to the disc system for each write command. With this switch reset, two read commands are issued for each write.

SWITCHES 13, 14 and 15

The setting of these switches determines the data pattern, as detailed above, used for the data transfer tests. These switches are ignored by tests 1 and 3, and while a data transfer cycle is in progress, i.e., while the program is in the process of writing or reading the disc, the pattern will not be changed even though the user alters the setting of these data switches.

A-4 TEST DESCRIPTIONS

TEST 1 - DISCRETE CONTROLLER TESTS

Test 1 is composed of a series of 43 very short, basic tests which exercise control and status bits between the CPU and the disc system controller. Interrupts are forced and acknowledged and the core location counter is written to and read back. No actual data is transferred.

TEST 2 - CPU TO CONTROLLER DATA PATH TEST

Test 2 writes 16 words of data to the controller in diagnostic mode then reads that data back and compares it to what was written. The data is read back complemented so the program must recompelment it before the actual compare is done. All data patterns may be used by this test.
TEST 3 - DISC SYSTEM SIZING TEST

Test 3 determines the size of the disc system and verifies that the sizing options have been properly strapped in the hardware. The program does this by writing to the first sector of a track of the disc system and examining the status returned by the system after the write. If the status indicates that the track just written to is write-protected, an appropriate error message is printed. The program attempts to write to all four discs in the system and prints the last valid address or a NO DISC MESSAGE for each disc. Once the last valid address has been determined for a disc and that address is found to be less than the maximum address of a disc, the program will continue to write to the remaining possible tracks of that disc ensuring that all these writes raise the NO-SUCH-DISC status bit, otherwise an error message is printed.

TEST 4 - DATA TRANSFER SECTOR

Test 4 writes to the entire disc system, or to the portion of the disc system selected by the user through the looping option and the current data pattern, one sector at a time. When the write is completed the portion of the disc system that was written to is read and the data is compared to what was written. Each sector is read twice unless data switch 12 is set.

TEST 5 - DATA TRANSFER SUBSECTOR

Test 5 writes to the entire disc system, or the portion of the disc system selected by the user through the looping option and the current data pattern, one subsector at a time. When the write is completed the portion of the disc system that was written to is read and the data is compared to what was written. Each subsector is read twice unless data switch 12 is set. If the user chooses to exercise the looping option of test 5, the user must also select the number of subsectors that will be written or read on each data transfer.

A-5 DATA PATTERNS

ZEROES

The zeroes pattern consists of words of data with all data bits reset.

ONES

The ones pattern consists of words of data with all data bits set.

WORST CASE

The worst case pattern consists of words containing the pattern 16142 octal.

TRACK/SECTOR

The track/sector pattern consists of words of data containing the disc system address of where that pattern will be written.

INCREMENTING

The incrementing pattern consists of words of data each of which is incremented by one from the preceding word. The first word is zero, the next 1, and the next 2,
up to a maximum depending on the size of the portion of the disc system being written to. Once the data word is incremented to where it contains all ones, the next data word will again be all zeroes.

**RANDOM**

The random pattern consists of words of data with bits unpredictably set or reset. The pattern is generated from a one word seed which is manipulated to form a data word. The next data word uses the last data word as the seed. This method allows the same "random" pattern to be generated repeatedly if that were desired. Ordinarily the program will alter the seed word on each pass ensuring a new and different random pattern.

**ERROR MESSAGES**

The program prints 2 main types of error messages: status errors and data compare errors. The format for status error is as follows:

\[\text{STER SS D TTT SS XXX CY}\]

This is a status error message. The STER indicates that a status error occurred. The SS is the actual status the program received in octal. The D TTT SS indicate the disc system address at which the error occurred. D is the disc number, TTT is the track and SS is the sector. The XXX is the cycle count the program was on when the error occurred. The CY identifies the cycle count which is printed only when the program is executing test 4.

\[\text{N:RD- PPPPPP WT- PPPPPP ADRS: D TTT SS WWW XXX CY}\]

This format is a data compare error. The N is either a 1 or a 2 indicating whether the error occurred on the first or second read. RD- PPPPPP represents the data that was read in octal, WT- PPPPPP represents the data that was written, the expected data. The D TTT SS represent the disc system address as it does for status errors. The WWW is the word position in the sector or subsector in octal where the error was detected. The XXX CY again represents the cycle count which is printed only when the program is executing test 4.

The format of test 1 errors is as follows:

\[\text{ER# NNN}\]

This is the format of test 1 error. The NNN corresponds to the number of the sub-test that detected the error.

Test 3 will print the message SIZING ERROR if on any particular disc attempting to write to a track address greater than the last valid address does not result in a NO SUCH DISC status.

The error message SOFTWARE TIMEOUT is recorded whenever DONE is not asserted by the disc system approximately 2/3 of second after an I/O instruction causing data transfer, has been issued to it.
Test 1 Sub-Test Detailed Descriptions

The 43 sub-tests that make up Test 1 are identified by their run sequence number in octal.

Sub-Test 01

This sub-test selects device 0 via a SKPBZ instruction. An error indicates that the disc controller is asserting BUSY when it should not.

Sub-Test 02

This sub-test selects device 0 via a SKPDZ instruction. An error indicates that the disc controller is asserting DONE when it should not.

Sub-Test 03

This sub-test clears the disc controller with a NIOC instruction, does an I/O reset via an IORST instruction then checks to see if the disc controller is busy. An error indicates that the disc controller BUSY signal is asserted when it should not be.

Sub-Test 04

This sub-test clears the disc controller with a NIOC instruction, does an I/O reset via an IORST instruction and then checks to see if the disc controller is done. An error indicates that the disc controller DONE signal is asserted when it should not be.

Sub-Test 05

This sub-test issues a NIO instruction to the disc controller then checks to see if BUSY signal is asserted. An error condition indicates that BUSY was asserted without a "S" or "P" pulse.

Sub-Test 06

This sub-test issues a "P" pulse via a NIOP instruction to device 0. It then checks to see if the disc controller asserts BUSY signal. An error condition indicates that the disc controller asserted BUSY in response to a "P" pulse to a device not the disc.

Sub-Test 07

This sub-test issues a "S" pulse via a NIOS instruction to device 0. It then checks to see if the disc controller asserts BUSY signal. An error condition indicates that the disc controller asserted BUSY in response to an "S" pulse to a device not the disc.

Sub-Test 10

This sub-test sets the disc BUSY signal via an NIOP instruction to the disc. It then issues a clear via an NIOC instruction to the disc and issues an IORST. An error condition indicates that the disc BUSY signal failed to clear from neither a "C" pulse nor a I/O reset.
Sub-Test 11

This sub-test sets the disc BUSY signal via an NIOP instruction to the disc and issues an IORST. An error condition indicates that the disc BUSY signal failed to clear from an I/O reset.

Sub-Test 12

This sub-test sets the disc BUSY signal via an NIOP instruction to the disc and issues a clear via an NIOC instruction to the disc. An error condition indicates that the disc BUSY signal failed to clear from a "C" pulse.

Sub-Test 13

This sub-test sets the disc BUSY signal via a DOBP instruction to the disc. An error condition indicates that BUSY failed to set.

Sub-Test 14

This sub-test sets the disc BUSY signal via a DOBS instruction to the disc. The disc is then reset via an NIOC instruction. An error condition indicates that BUSY failed to set.

Sub-Test 15

This sub-test sets the disc BUSY signal via a DOBP instruction to the disc. The disc is then issued an NIO instruction without a "C" pulse. An error condition indicates that the disc was cleared via a NIO instruction without a "C" pulse.

Sub-Test 16

This sub-test sets the disc BUSY signal via a DOBP instruction to the disc. A NIOC instruction is then issued to device 0. An error condition indicates that disc BUSY signal was cleared via an NIOC instruction to a device other than the disc.

Sub-Test 17

This sub-test enables the CPU interrupt system and issues an interrupt acknowledge instruction to which no device should respond. An error condition indicates that an interrupt occurred without the disc DONE signal being set.

Sub-Test 20

This sub-test disables all device interrupts by issuing a MSKO instruction with an argument of all ones. The CPU interrupt system is then enabled which it would be unless an interrupt occurred. An error condition indicates that an interrupt occurred although all device interrupts, including the disc, are disabled.

Sub-Test 21

This sub-test repeats a portion of sub-test 20 by enabling the CPU interrupt system testing to see if an interrupt has occurred. An error condition indicates that the disc interrupt request remained set after the IORST instruction, which is part of every sub test, was issued.
Sub-Test 22

This sub-test issues an interrupt acknowledge instruction. An error condition indicates that the disc responded to the interrupt acknowledge without the disc interrupt request being set.

Sub-Test 23

This sub-test loads the core location counter with all zeroes. An IORST instruction is then issued and the CLC is read back via a DIB instruction. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 24

This sub-test loads the core location counter with all ones. An IORST instruction is then issued and the CLC is read back via a DIB instruction. An error condition indicates that something other than all ones was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 25

This sub-test loads the core location counter with all zeroes, then reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 26

This sub-test loads the core location counter with all zeroes, then loads it with an octal 010421 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (010421).

Sub-Test 27

This sub-test loads the core location counter with all zeroes, then loads it with an octal 021042 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (021042).

Sub-Test 30

This sub-test loads the core location counter with all zeroes, then loads it with an octal 042104 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (042104).

Sub-Test 31

This sub-test loads the core location counter with all zeroes, then loads it with an octal 104210 and again loads it with all zeroes and reads it back. An error condition indicates that something other than all zeroes was read back. AC0 contains the data read back and AC1 contains the data written (104210).
Sub-Test 32

This sub-test loads the core location counter with all ones, then reads it back. An error condition indicates that something other than all ones was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 33

This sub-test loads the core location counter with all ones and issues a "P" pulse. It then attempts to read back the equivalent of the CLC of device 0. An error condition indicates that data was read back from the CLC when the disc was not selected.

Sub-Test 34

This sub-test loads the core location counter with all ones and issues a "S" pulse. It then attempts to read back the equivalent of the CLC of device 0. An error condition indicates that data was read back from the CLC when the disc was not selected.

Sub-Test 35

This sub-test issues an instruction to load the core location counter with all ones to the CPU as the device. The CLC of the disc is then read back. An error condition indicates that the disc accepted the data (loaded the CLC) when it was not selected.

Sub-Test 36

This sub-test write all ones to the disc core location counter. It then reads the disc CLC back and ANDs that data with an octal 377. An error condition indicates that bits 8 - 15 were not read back correctly.

Sub-Test 37

This sub-test write all ones to the disc core location counter. It then reads the disc CLC back and ANDs that data with an octal 377 and complements it. An error condition indicates that bits 1 - 7 were not read back correctly.

Sub-Test 40

This sub-test loads the core location counter with all ones, then reads it back. An error condition indicates that something other than all ones was read back. AC0 contains the data read back and AC1 contains the data written.

Sub-Test 41

This sub-test selects disc 0, track 0, sector 0 via a DOAP instruction to the disc. The status of the disc system is then read via a DIA instruction. An error condition indicates that the NO-SUCH-Disc status bit (bit 13) was set.

Sub-Test 42

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read. An error condition indicates that the WRITE-ERROR bit (bit 11) was set.
Sub-Test 43

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read via a DIAC instruction which clears the status. An error condition indicates that the WRITE-ERROR bit (bit 11) remained set.

Sub-Test 44

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read via a DIAC instruction which clears the status. An error condition indicates that the ERROR bit (bit 15) remained set.

Sub-Test 45

This sub-test issues a read command to the disc via a DOBS instruction. The status of the disc system is then read via a DIAC instruction which clears the status. An error condition indicates that the DATA-LATE bit (bit 12) remained set.

Sub-Test 46

This sub-test issues a write command to the disc via a DOBP instruction. It then issues a DIC instruction to device 0. An error condition indicates that a DIC to a device other than the disc produced a response from the disc system.

Sub-Test 49

This sub-test issues a write command to the disc system. It then issues a NIOC to device 21 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 21.

Sub-Test 50

This sub-test issues a write command to the disc system. It then issues a NIOC to device 22 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 22.

Sub-Test 51

This sub-test issues a write command to the disc system. It then issues a NIOC to device 24 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 24.

Sub-Test 52

This sub-test issues a write command to the disc system. It then issues a NIOC to device 30 and tests to see if the disc system remains busy. An error condition indicates that the disc system responded to the device selection of device 30.

Sub-Test 53

This sub-test is designed to assure that the CLC register is capable of counting. A maximum length (65536 words) write is unitiated from memory location zero. This should cause the CLC to be set to a logical zero, then incremented until it overflows, resulting in its being set to a zero. An error condition indicates that the contents of the
CLC that were read back after the write command had set DONE, was something other than zero. AC0 contains the starting memory location; AC1 contains the status of the disc system after the write; AC2 contains the contents of the CLC after the write; and AC3 contains what was output in the DOC instruction.

Sub-Test 54

This sub-test also assures that the CLC register is capable of counting. The above test (53) expects the setting of the CLC to be the same before and after the write command. This sub-test is executed since a completely non-incrementing CLC would produce the same results. In this sub-test only 65520 words are written from memory location zero. This will cause the CLC to set to an octal 77760 after the write command. An error condition indicates that the contents of the CLC that were read back after the write command had set DONE, was something other than 77760. AC0 contains the expected contents of the CLC; AC1 contains the status of the disc system after the write; AC2 contains the contents of the CLC after the write; and AC3 contains what was output in the DOC instruction.

A-7 DISC CONTROL DIAGNOSTIC

The following pages contain the software diagnostic program for the 8011 Disc Memory Controller.
TYPE 8011 DISK CONTROL DIAGNOSTIC

ABSTRACT

TYPE 8011 DISK CONTROL DIAGNOSTIC IS A MAINTENANCE PROGRAM DESIGNED TO TEST THE TYPE 8010 DISK MEMORY SYSTEM

MACHINE REQUIREMENTS

STANDARD NOVA PROCESSOR

4K READ/WRITE MEMORY

DATA DISC 8010 DISK MEMORY SYSTEM

TELETYPE

SWITCH SETTINGS

SWITCH 0(1) PRINT INSTRUCTIONS/ABORT CURRENT TEST

HALT / LOOP OPTIONS

SWITCH 1(1) HALT ON ERROR

SWITCH 2(1) PRINT CYCLE COUNT

SWITCH 3(1) LOOP ON SELECTED TEST

TEST SELECTION

SWITCH 4(1) SELECT TEST

SWITCH 5(1) SELECT TEST

SWITCH 6(1) SELECT TEST

TESTS

0 0 0 TESTS 1 THRU 4
0 0 1 TEST 1 DISCRETE CONTROLLER TESTS
0 1 0 TEST 2 DIAGNOSTIC MODE TEST
0 1 1 TEST 3 SIZE TEST
1 0 0 TEST 4 DATA TRANSFER (SECTOR)
1 0 1 TEST 5 DATA TRANSFER (SUB-SECTOR)
1 1 0 TESTS 1, 2 AND 4
1 1 1 TESTS 2 AND 4

READ-ONLY

WRITE-ONLY

DATA ERROR PRINT INHIBIT

STATUS ERROR PRINT INHIBIT

END OF TEST AND TEST ID PRINT INHIBIT

2 READS PER WRITE

SELECT THE DATA PATTERN

SELECT THE DATA PATTERN

SELECT THE DATA PATTERN

SELECT THE DATA PATTERN

SELECT THE DATA PATTERN
OPERATING PROCEDURE

LOAD THE PROGRAM VIA THE BINARY LOADER

GET SWITCHES TO 000002
PRESS RESET
PRESS START
THE PROGRAM WILL IDENTIFY ITSELF ON THE TELETYPE
AND REQUEST THE DISK DEVICE CODE TO WHICH A 20 OR
60 MUST BE ENTERED TO INDICATE THE DISC MEMORY
SYSTEM TO BE TESTED. THE PROGRAM WILL NEXT REQUEST
THAT THE DATA SWITCHES BE SET TO THEIR DESIRED SETTINGS
THEN HALT. THE USER SHOULD THEN SET THE DATA SWITCHES
AND DEPRESS CONTINUE.

THE PROGRAM WILL RUN UNTIL MANUALLY STOPPED
OR AN ERROR IS DETECTED. AT THE END OF EACH
TEST THE MESSAGE "END OF TEST" IS PRINTED.

PROGRAM OUTPUT/ERROR DESCRIPTION
IF A MALFUNCTION IS DETECTED THE PROGRAM
WILL, DEPENDING ON THE SWITCH SETTING, PRINT
AN ERROR MESSAGE, HALT, CONTINUE, OR LOOP ON
THE ERROR.

PROGRAM DESCRIPTION/THEORY OF OPERATION
TEST 1 IS MADE UP OF 43 TEST STEPS WHICH TEST
THE SETTING AND RESETTING OF THE CONTROLLER STATUS
BITS UNDER VARIOUS CONDITIONS. NO DATA TRANSFER
TAKES PLACE.
TEST 2 TESTS DIAGNOSTIC MODE. DATA IS TRANSFERRRED FROM
THE CPU TO THE CONTROLLER AND READ BACK IMMEDIATELY.
NO DATA TRANSFER TAKES PLACE BETWEEN THE CONTROLLER
AND THE DISC.
TEST 3 DETERMINES THE SIZE AND THE WRITE PROTECTED TRACKS
OF THE DISC. THE FIRST SECTOR OF EACH TRACK IS WRITTEN TO
AND THE STATUS OF THE DISC SYSTEM IMMEDIATELY AFTER EACH
WRITE IS READ AND EXAMINED.
TEST 4 TRANSFERS DATA TO AND FROM THE DISC ON A SECTOR
BY SECTOR BASIS.
TEST 5 TRANSFERS DATA TO AND FROM THE DISC ON A SUB-SECTOR BASIS BY USING THE DOC INSTRUCTIONS.

7. RESTRICTIONS/MISC

7.1 WHEN THE DIAGNOSTIC IS RUNNING NO OTHER CONTROL MAY REQUEST THE DISK DRIVE.

7.2 THE DISK DRIVE LOGIC MUST RESPOND TO SELECTING OF DRIVE 0.

LOC 2

SUB 0.0.SKP

HIGH SPEED CHANNEL

JMP 0.+1

DUSR = 020

IBUF = 10000

O8UF = 14000

PASS: 0

TINRET: 0

LOADR: 0

WCTR: 0

DRET: 0

DEVICE: 0

MAV: 0

Cl44: 144

c 12: 12

XXITR: 1TR

FIRST: T01 ;FAB FOR PROGRAM

LAST: ECODE ;MODIFICATION

ICRLF: CRLF

IMESS: MESS

TYPIN: DCODE

SETUP: ENTER

CYCLE

ER: ERR

EHALT=JSR

;
<table>
<thead>
<tr>
<th>Line</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>00266</td>
<td>004000</td>
</tr>
<tr>
<td>2</td>
<td>00267</td>
<td>003400</td>
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<tr>
<td>3</td>
<td>00270</td>
<td>003430</td>
</tr>
<tr>
<td>4</td>
<td>00271</td>
<td>000330</td>
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<tr>
<td>5</td>
<td>00272</td>
<td>000037</td>
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<tr>
<td>6</td>
<td>00273</td>
<td>000240</td>
</tr>
<tr>
<td>7</td>
<td>00274</td>
<td>000300</td>
</tr>
<tr>
<td>8</td>
<td>00275</td>
<td>000070</td>
</tr>
<tr>
<td>9</td>
<td>00276</td>
<td>000087</td>
</tr>
<tr>
<td>10</td>
<td>00277</td>
<td>002518</td>
</tr>
<tr>
<td>11</td>
<td>00300</td>
<td>002575</td>
</tr>
<tr>
<td>12</td>
<td>00301</td>
<td>005460</td>
</tr>
<tr>
<td>13</td>
<td>00302</td>
<td>000000</td>
</tr>
<tr>
<td>14</td>
<td>00303</td>
<td>000000</td>
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<tr>
<td>15</td>
<td>00304</td>
<td>000000</td>
</tr>
<tr>
<td>16</td>
<td>00305</td>
<td>000000</td>
</tr>
<tr>
<td>17</td>
<td>00306</td>
<td>000000</td>
</tr>
<tr>
<td>18</td>
<td>00307</td>
<td>000000</td>
</tr>
<tr>
<td>19</td>
<td>00318</td>
<td>000000</td>
</tr>
<tr>
<td>20</td>
<td>00311</td>
<td>004373</td>
</tr>
<tr>
<td>21</td>
<td>00312</td>
<td>005354</td>
</tr>
<tr>
<td>22</td>
<td>00313</td>
<td>077760</td>
</tr>
<tr>
<td>23</td>
<td>00314</td>
<td>000055</td>
</tr>
<tr>
<td>24</td>
<td></td>
<td></td>
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<td>25</td>
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<td></td>
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<td>26</td>
<td></td>
<td></td>
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<tr>
<td>27</td>
<td>00037</td>
<td>000000</td>
</tr>
<tr>
<td>28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>00377</td>
<td>000085</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
START OF DIAGNOSTIC

; TELL OPERATOR TO LOCK DISK DRIVE.

; FORM A ONE

; READ THE DATA SWITCHES

; GET A ONE

; GET TWO DIGITS

; ERROR
LDA 1,CSN ; GET MAX TEST NO.
SUBZ 1,CSN 1,2,SNC
JMP MIA
NEG 2,2 ; DECREMENT COUNT
COM 2,2
STA 2,ERNO ; SET POTENTIAL ERROR NUMBER
INC 2,2
LDA 1,TTBL ; ADDRESS OF TEST TABLE
ADD 1,2 ; ADD TO ENTERED NUMBER
JMP MIA:0,2 ; JUMP TO DESIRED TEST

TTBL: MIA
T01
T02
T03
T04
T05
T06
T07
T08
T09
T10
T11
T12
T13
T14
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T57
T58

;
MOV 0,0 ; FORM A ZERO

SUB 0,0 ; RESET ERROR NUMBER

JSR @SETUP ; SELECT DEVICE ZERO. TEST FOR NOT BUSY

SKPBZ 0 ; IF EHALT THE CONTROLLER IS ASSERTING

EHALT ; BUSY AND SHOULD NOT BE.

JSR @LOOP ;

JSR @SETUP ; SAME AS TEST 01 TESTING

SKPBZ 0 ; DONE INSTEAD OF BUSY

EHALT ;

JSR @LOOP ;

JSR @SETUP ; DISK BUSY FLOP STUCK (1).

NIOD DSK ;

IORST DSK ; DISK BUSY (1), ASSERTED

JSR @LOOP ;

JSR @SETUP ; DISK DONE FLOP STUCK (1)

NIOD DSK ;

IORST DSK ; DISK DONE (1). ASSERTED

JSR @LOOP ;

JSR @SETUP ; SELECTING THE DISK

NIOD DSK ; WITHOUT A *S* OR *C* PULSE

SKPBZ DSK ; SET DISK BUSY

EHALT ;

JSR @LOOP ;

JSR @SETUP ; A *P* PULSE TO A

NIOP 0 ; DEVICE NOT THE DISK

SKPBZ DSK ; SET DISK BUSY.

EHALT ;

JSR @LOOP ;

JSR @SETUP ; A *S* PULSE TO A

NIOS 0 ; DEVICE NOT THE DISK

SKPBZ DSK ; SET DISK BUSY.

EHALT ;

JSR @LOOP ;

JSR @SETUP ; DISK BUSY FLOP FAILED

NIOP DSK ; TO CLEAR VIA A *C*.

NIOD DSK ; PULSE OR I/O RESET.

IORST DSK ;

EHALT ;

JSR @LOOP ;

JSR @SETUP ; DISK BUSY FLOP FAILED

NIOP DSK ; TO CLEAR VIA A 1/O RESET.
00623 063520 SKPBZ DSK
00624 066071 EHALT
00625 066070 JSR @LOOP

00626 066067 T12: JSR @SETUP ; DISK BUSY FLOP FAILED
00627 066320 NIDP DSK ; TO CLEAR VIA A "C"
00630 066020 NIDC DSK ; PULSE.
00631 066520 SKPBZ DSK
00632 066071 EHALT
00633 066070 JSR @LOOP

00634 066067 T13: JSR @SETUP ; A "P" PULSE FAILED
00635 020170 LDA 0.1DBUF ; TO SET DISK BUSY FLOP.
00636 066320 DDBP 0.DSK
00637 066520 SKPBZ DSK
00640 066071 EHALT
00641 066070 JSR @LOOP

00642 066067 T14: JSR @SETUP ; A "S" PULSE FAILED
00643 020170 LDA 0.1DBUF ; TO SET DISK BUSY FLOP.
00644 126400 SUB 1.1
00645 066120 DDBS 0.DSK
00646 066520 SKPBZ DSK
00647 126400 ADC 1.1
00650 066020 NIDC DSK
00651 125805 MDV 1.1.SHR
00652 066071 EHALT
00653 066070 JSR @LOOP

00654 066067 T15: JSR @SETUP ; THE DSK BUSY FLOP
00655 020170 LDA 0.1DBUF ; WAS CLEARED VIA A
00656 066320 DDBP 0.DSK ; "MID" INSTRUCTION WITH-
00657 066020 NID DSK ; OUT A "C" PULSE.
00658 066520 SKPBZ DSK
00661 066071 EHALT
00662 066070 JSR @LOOP

00663 066067 T16: JSR @SETUP ; THE DSK BUSY FLOP
00664 020170 LDA 0.1DBUF ; WAS CLEARED VIA A
00665 066320 DDBP 0.DSK ; "C" PULSE WITHOUT
00666 066020 NIDC 0 ; THE DISK BEING SELECTED.
00667 066520 SKPBZ DSK
00670 066071 EHALT
00671 066070 JSR @LOOP

00672 102620 SUBZR 0.0 ; SET LOCATION
00673 046001 STA 0.1 ; FOR INTERRUPTS

00674 066067 T17: JSR @SETUP ; A INTERRUPT OCCURRED
00675 0660177 NIDOS CPU ; WITHOUT DSK DONE FLOP
00676 061477 INTA 0 ; BEING SET.
00677 101004 MOV 0.0.SZR
00678 006403 JMP +3
00679 066347 SKPBZ CPU
00682 066071 EHALT
00683 066070 JSR @LOOP

00684 066067 T20: JSR @SETUP ; THE DSK INT REQ
I 00705 102000 ADC B.0 : FLOP IS SET.
2 00706 062077 MSKD B
3 00707 060177 MSKD CPU
4 00710 101000 MOV B.0
5 00711 063477 SKPB0 CPU
6 00712 006071 EHALT
7 00713 006070 JSR LOOP
8 00714 005067 T21: JSR SETUP : THE DSK INT REQ
9 00715 064177 NIOS CPU : FLOP IS SET.
10 00716 101000 MOV B.0
11 00717 063477 SKPB0 CPU
12 00720 006071 EHALT
13 00721 006070 JSR LOOP
14 00722 006067 T22: JSR SETUP : THE DSK INT REQ FLOP
15 00723 061477 INTA B IS NOT SET. YET INTA
16 00724 101004 MOV B.0.SZR : READS BACK A BYTE.
17 00725 006071 EHALT
18 00726 006070 JSR LOOP
19 00727 006067 T23: JSR SETUP : THE CORE LOCATION COUNTER
20 00728 126408 SUB 1.1 (CLC) WAS LOADED TO 0
21 00730 062020 DOB 1.DSK : THEN RESET VIA 10RST.
22 00732 062677 1DRST : JSRB READ BITS BACK.
23 00733 061428 DIB B.DSK : CHECK AC0 FOR READ
24 00734 101004 MOV B.0.SZR : CHECK AC1 FOR WRITTEN
25 00735 006071 EHALT
26 00736 006070 JSR LOOP
27 00737 006067 T24: JSR SETUP : THE CORE LOCATION COUNTER
28 00740 126220 ADCZHR 1.1 (CLC) WAS LOADED WITH
29 00741 066020 DOB 1.DSK : ALL BITS. THEN CLEARED
30 00742 062677 1DRST : VIA A 1/0 RESET PULSE.
31 00743 061428 DIB B.DSK : CHECK AC0 FOR READ
32 00744 101004 MOV B.0.SZR : CHECK AC1 FOR WRITTEN
33 00745 006071 EHALT
34 00746 006070 JSR LOOP
35 00747 006067 T25: JSR SETUP : LOAD THE CLC REGISTER
36 00750 126008 SUB 1.1 : WITH ZEROS. CHECK VIA
37 00751 065028 DOB 1.DSK : A DIB INSTRUCTION.
38 00752 061428 DIB B.DSK : ANY BIT SET IN AC0 15
39 00753 101004 MOV B.0.SZR : IN ERROR.
40 00754 006071 EHALT
41 00755 006070 JSR LOOP
42 00756 005067 T26: JSR SETUP : LOAD THE CLC REGISTER
43 00757 102408 SUB B.0 : MAGIC TEST #1
44 00758 062020 DOB B.DSK
45 00760 062407 LDA 1.C0104: *B10421
46 00762 065028 DOB 1.DSK : AC1 WRITTEN
47 00763 063028 DOB B.DSK : AC0 READ
48 00764 061428 DIB B.DSK
49 00765 101004 MOV B.0.SZR
50 00766 006071 EHALT
51 00767 006070 JSR LOOP
I.e0110 006076 T27: JSR @SETUP ;LOAD THE CLC REGISTER
2 ee1?1 10240e SUB 0,0 ;MAGIC TEST 2
3 00772 062020 DOB 0, DSK
4 00773 024075 LDA 1, C0210 :021042
5 00774 066020 DOB 1, DSK ;AC I WRITTEN
6 00775 065020 DOB 0, DSK ;ACO READ
7 00776 061420 DIB 0, DSK
8 00777 101004 MOV 0,0,SNR
9 01000 006071 EHALT
10 01001 006076 JSR @LOOP
11 00778 062020 DOB 0, DSK
12 00779 066020 DOB 1, DSK ;ACO READ
13 00780 061420 DIB 0, DSK
14 00781 101004 MOV 0,0,SNR
15 01002 006076 JSR @SETUP ;LOAD THE CLC REGISTER
16 01003 102400 SUB 0,0 ;MAGIC TEST 3
17 01004 062020 DOB 0, DSK
18 01005 024076 LDA 1, C0421 :042104
19 01006 066020 DOB 1, DSK ;AC I WRITTEN
20 01007 065020 DOB 0, DSK ;ACO READ
21 01008 061420 DIB 0, DSK
22 01009 101004 MOV 0,0,SNR
23 01010 006071 EHALT
24 01011 006070 JSR @LOOP
25 01012 006076 JSR @SETUP ;LOAD CLC WITH
26 01013 102400 SUB 0,0 ;MAGIC TEST 4
27 01014 062020 DOB 0, DSK
28 01015 024077 LDA 1, C0421 :042104
29 01016 066020 DOB 1, DSK ;AC I WRITTEN
30 01017 065020 DOB 0, DSK ;ACO READ
31 01018 061420 DIB 0, DSK
32 01019 101004 MOV 0,0,SNR
33 01020 006071 EHALT
34 01021 006070 JSR @LOOP
35 01022 006076 JSR @SETUP ;DSK DATIB ASSERTED
36 01023 126000 ABC 1,1 ;ALL ONES AND TRY
37 01024 066020 DOB 1, DSK ;TO READ SOME BACK.
38 01025 061420 DIB 0, DSK ;ACI WRITTEN
39 01026 101005 MOV 0,0,SNR ;ACO READ
40 01027 006071 EHALT
41 01028 006070 JSR @LOOP
42 01029 006076 JSR @SETUP ;DSK DATIB ASSERTED
43 01030 126000 ABC 1,1 ;WITHOUT DSK SELECT.
44 01031 062320 DOBP 0, DSK
45 01032 065400 DIB 1,0
46 01033 166415 SUB 0,1,SNR
47 01034 006071 EHALT
48 01035 006070 JSR @LOOP
49 01036 102220 ADCZ 0,0 ;ACO READ
50 01037 066120 DOBS 1, DSK ;AC 1, SNR
51 01038 061400 DIB 0, DSK
52 01039 005400 MOV 0,0,SNR
53 01040 066120 DOBS 1, DSK ;AC 1, SNR
54 01041 061400 DIB 0, DSK
55 01042 005400 MOV 0,0,SNR
56 01043 006071 EHALT
57 01044 006070 JSR @LOOP
PAGE 13

1 01054 006067 T35: JSR @SETUP ; DSK DATOB ASSERTED
2 01055 126220 ADCZR 1.1 ; WITHOUT DSK SELECT
3 01056 066077 DOB 1. CPU ; AC I WRITTEN
4 01057 061420 DIB 0. DSK ; AC 0 READ
5 01058 106415 SUB* 0. 1.SNR
6 01059 006071 EHALT
7 01060 006070 JSR @LOOP
8
9 01061 006067 T36: JSR @SETUP ; THE CLC REGISTER FAILED
10 01062 102000 ADC 1. ; TO READ BACK BITS
11 01063 066020 DOB 0. DSK 18-15.
12 01064 061420 DIB 0. DSK
13 01065 123415 LDA 1.XX377
14 01066 123415 AND* 1. 1.SNR
15 01067 006071 EHALT
16 01068 006070 JSR @LOOP
17
18 01069 006067 T37: JSR @SETUP ; THE CLC REGISTER FAILED
19 01070 102001 ADC 0. ; TO READ BACK BITS 1-7
20 01071 000377 XX377: 377
21 01072 066020 DOB 0. DSK
22 01073 061420 DIB 0. DSK
23 01074 123415 LDA 1.XX377
24 01075 123415 AND* 1. 1.SNR
25 01076 006071 EHALT
26 01077 006070 JSR @LOOP
27
28 01078 006067 T38: JSR @SETUP ; LOAD CLC WITH ALL
29 01079 126200 ADC 1.1 ; ONES, CHECK THEM AS
30 01080 066020 DOB 1. DSK ; READ BACK.
31 01081 061420 DIB 0. DSK ; ACI WRITTEN
32 01082 123415 LDA 1.XX377
33 01083 123415 AND* 1. 1.SNR ; AC0 READ
34 01084 006071 EHALT
35 01085 006070 JSR @LOOP
36
37 01086 006067 T39: JSR @SETUP ; DISK SELECT ERROR IS SET
38 01087 102000 SUB 0. 0 ; SELECTING DISC 0.
39 01088 066020 DDAP 0. DSK ; TRACK 0. SECTOR 0.
40 01089 063520 SKPBZ DSK ; SET NO-SUCH-DISC BIT
41 01090 060777 JMP -1
42 01091 060420 DIA 0. DSK
43 01092 024100 LDA 1.C4
44 01093 107414 AND* 0.1.SZR
45 01094 006071 EHALT
46 01095 006070 JSR @LOOP
47
48 01096 006067 T40: JSR @SETUP ; WRITE LOCK STATUS
49 01097 020100 LDA 0.C77K ; IS SET WITHOUT WRITE COMMAND
50 01098 062120 DOB 0. DSK
51 01099 061420 DIB 0. DSK
52 01100 063520 SKPBZ DSK
53 01101 060777 JMP -1
54 01102 060420 DIA 0. DSK
55 01103 024100 LDA 1.C4
56 01104 107414 AND* 0.1.SZR
57 01105 006071 EHALT
58 01106 006070 JSR @LOOP
I01140 006067 T43: JSR @SETUP ; WRITE LOCK STATUS
2 01141 026117 LDA 0.C77K ; SHOULD NOT SET ON
3 01142 062120 DOBS 0.DSK ; JA READ OPERATION.
4 01143 063520 SKPBZ DSK
5 01144 066777 JMP .-1
6 01145 066220 D!AC 0.DSK
7 01146 024120 LDA 1.C20
8 01147 107414 AND# 0.1.5ZR
9 01148 006071 EHALT
10 01149 006070 JSR @LOOP
11
12 01150 006067 T44: JSR @SETUP ; DISK DATA ERROR BIT
13 01151 020101 LDA 0.C140K ; IS SET.
14 01152 062120 DOBS 0.DSK
15 01153 062620 DIAC 0.DSK
16 01154 006071 EHALT
17 01155 006070 JSR @LOOP
18
19 01156 024104 LDA 1.C20
20 01157 107414 AHD• 0.LSZR
21 01158 006071 EHALT
22 01159 006070 JSR @LOOP
23
24 01160 006067 T45: JSR @SETUP ; DISK DCH LATE ERROR
25 01161 020101 LDA 0.C140K ; BIT IS SET.
26 01162 062120 DOBS 0.DSK
27 01163 062620 DIAC 0.DSK
28 01164 006071 EHALT
29 01165 006070 JSR @LOOP
30
31 01166 006067 T46: JSR @SETUP ; COMMAND IS WRITE
32 01167 102620 SUBZR 0.0 ; MAINT MODE: THIS TEST
33 01168 062320 DOBP 0.DSK ; INSURES THAT A DIC
34 01169 0175076400 DIC 3.0 ; INSTRUCTION TO A DEVICE
35 01170 0176101000 MOV 0.0 ; OTHER THAN THE DISK
36 01171 0177076480 DIC 3.0 ; WILL NOT PRODUCE
37 01172 0120068420 DIO 0.DSK ; (DISK DATAC) A MAINTENANCE
38 01173 01201024102 LDA 1.C20 ; FEATURE OF THE DISK.
39 01174 01202107414 AND# 0.1.5ZR
40 01175 0120306071 EHALT
41 01176 01204006070 JSR @LOOP
42
43 01177 01205006070 T47: JSR @SETUP ; CHECK DEVICE SELECTION
44 01178 01206102620 SUBZR 0.0
45 01179 01207062320 DOBP 0.DSK
46 01180 01210060221 NIOC 21
47 01181 01211063420 SKPBZ DSK
48 01182 01212006071 EHALT
49 01183 01213006070 JSR @LOOP
50
51 01184 01214006070 T50: JSR @SETUP ; CHECK DEVICE SELECTION
52 01185 01215102620 SUBZR 0.0
53 01186 01216062320 DOBP 0.DSK
54 01187 01217060221 NIOC 22
55 01188 01220063420 SKPBZ DSK
56 01189 01221006071 EHALT
57 01190 01222006070 JSR @LOOP
58
59 01191 01223006070 T51: JSR @SETUP ; CHECK DEVICE SELECTION
I 01224 102620 SUBZR 0.0
2 01225 062320 DOBP 0.DSK
3 01226 060224 NIOC 24
4 01227 063420 SKPN DSK
5 01230 006071 EHALT
6 01231 006070 JSR @LOOP
7
8 01232 006067 T52: JSR @SETUP ; CHECK DEVICE SELECTION
9 01233 102620 SUBZR 0.0
10 01234 062320 DOBP 0.DSK
11 01235 060230 NIOC 30
12 01236 063420 SKPN DSK
13 01237 006071 EHALT
14 01240 006067 T53: JSR @SETUP ; CHECK THAT CLC REGISTER CAN INCREMENT
15
16 01241 006067 T54: JSR @SETUP ; CHECK THAT CLC REGISTER CAN INCREMENT
17 01242 176400 SUB 3.3 ; FORM A ZERO
18 01243 102400 SUB 0.0 ;
19 01244 062020 DOB 0.DSK ; CORE ADDRESS ZERO
20 01245 071420 DIB 2.DSK ; GET THE CLC REGISTER
21 01246 020313 LDA 0.T54C ; GET THE EXPECTED CLC CONTENTS
22 01247 112434 SUBZ 0.2.SZR ; COMPARE TO ACTUAL
23
24 01250 064420 DIA 1.DSK ; GET DISC STATUS
25 01251 071420 DIB 0.0 ;
26 01252 151004 MOV 2.2.SZR ; ZERO IMPLIES CLC WRAPPED ALL AROUND IS OK
27 01253 006071 EHALT ; ON ERROR AC 0 CONTAINS CORE ADDRESS OF WRITE
28 START... AC1 CONTAINS DISC SYSTEM STATUS. AC2 CONTAINS THE CLC REGISTER CONTENTS AFTER THE WRITE.
29 AC3 CONTAINS INITIAL CLC CONTENTS.
30 01254 006070 JSR @LOOP
31
32 01255 006067 T55: JSR @SETUP ; CHECK THAT CLC CAN INCREMENT
33 01256 034110 LDA 3.3 ; GET A ONE
34 01257 102400 SUB 0.0 ; FORM A ZERO
35 01258 062020 DOB 0.DSK ; USE MEMORY ADDRESS OF ZERO
36 01259 077320 DOCP 3.DSK ; DOC OF 1 WRITES LOTS
37 01260 063620 SKPDN DSK ; WAIT FOR DONE
38 01261 000777 JMP . - 1
39 01264 064420 DIA 1.DSK ; GET DISC STATUS
40 01265 071420 DIB 2.0 ; GET THE CLC
41 01266 020313 LDA 0.T54C ; GET THE EXPECTED CLC CONTENTS
42 01267 112434 SUBZ 0.2.SZR ; COMPARE TO ACTUAL
43 01270 006071 EHALT ; ON ERROR AC0 CONTAINS EXPECTED CLC CONTENTS
44 AC1 CONTAINS DISC SYSTEM STATUS
45 AC2 CONTAINS CLC CONTENTS
46 AC3 CONTAINS DOC OUTPUT REGISTER
47 01271 006078 JSR @LOOP
48
49 01272 074477 READS 3 ; READ THE DATA SWITCHES
50 01273 030150 LDA 2.0;CIN ; INHIBIT EOT PRINT BIT
51 01274 173404 AND 3.2.SZR ; SEE IF SET
52 01275 000404 JMP TIUU ; YES NO PRINT
53
54 01276 006064 JSR @ICRLL ; CARRIAGE RETURN LINE FEED
55 01277 006065 JSR @IMESS ; MESSAGE
56 01300 003735 !PASS
; TEST 2 HANDLER
;
; 1. GENERATE 16 HALFWORD PATTERN IN OBUF
; 2. SEND DOB OF OBUF PLUS BIT 0 + PULSE TO WRITE TO CONTROLLER
; 3. SEND DOB OF IBUF PLUS BIT 0 + START TO READ FROM CONTROLLER
; 4. COMPLEMENT IBUF
; 5. COMPARE IBUF, OBUF
;
; USE LOC. 20 AUTO

01303 034111 MODE2: LDA 3.C2 ; GET A TWO
01304 054166 STA 3.MODE ; SET CURRENT MODE
01305 176548 SUB 3.3 ; FORM A ZERO
01306 054550 STA 3.M27 ; RESET 1-2 READ FLAG
01307 054261 STA 3.6FLG ; ALLOW PATTERN CHANGE
01308 054246 STA 3.INCE ; INITIALIZE INCREMENTING PATTERN
01309 034216 LDA 3.SSEED ; GET INITIAL SEED
01310 034110 LDA 3.C1 ; GET A ONE
01311 054217 STA 3.CSEED ; INITIALIZE SEED
01312 034110 LDA 3.C1 ; GET A ONE
01313 054217 STA 3.CUKPT ; INITIALIZE PATTERN
01314 054215 STA 3.EOCIN ; PRINT INHIBIT BIT
01315 074477 READS 3 ; READ THE DATA SWITCHES
01316 060484 AND 3.2.SZR ; MASK SWITCHES
01317 054777 JMP M2B

01320 060664 JSR @ICRLF ; CARRIAGE RETURN LINE FEED
01321 050065 JSR @MESS ; MESSAGE
01322 004403 MOD2M
01323 004203 MOD2M
01324 006213 M2B: JSR @IPTRN ; GENERATE PATTERN
01325 000020 C10: 20 ; OF 16 WORDS
01326 014000 OBUF ; IN OUTPUT BUFFER
01327 000000 0 ; TRACK ADDRESS
01328 074477 MOD2B: READS 3 ; READ THE DATA SWITCHES
01329 030144 LDA 2.RDONLY ; READ ONLY BIT
01330 035484 AND 3.2.SZR ; MASK THE SWITCHES
01331 004421 JMP M2RD

01334 030134 LDA 2.M1 ; TIME OUT VALUE
01335 056302 STA 2.WCNTR ; SET COUNTER
01336 052480 SUB 2.2 ; FORM A ZERO
01337 058306 STA 2.WFLG ; INDICATE WRITE
01338 028167 LDA 0.1OBUF ; ADDRESS OF OUTPUT BUFFER
01339 024222 LDA 1.DMBIT ;
01340 044261 STA 1.WFLG ; INHIBIT PATTERN CHANGE
01341 123000 ADD 1.0 ;
01342 062320 DOBP 0.DSK ; WRITE TO CNTRL
01343 059520 SKPDN DSK ; WAIT FOR DONE
01344 060591 JSR @WLP

01346 074477 READS 3
01347 030145 LDA 2.WONLY ; GET WRITE ONLY BIT
01348 035484 AND 3.2 ; MASK WITH SWITCHES
01349 151864 MOV 2.2.SZR ; SEE IF SET
01350 060755 JMP M2D2B

A-28
01354 102400 M2RD: SUB 0.0 ; FORM A ZERO
01355 040246 STA 0.INC ; INITIALIZE INCREMENT
01356 101400 INC 0.0 ; FORM A ONE
01357 040306 STA 0.RWLG ; INDICATE READ
01358 101400 INC 0.0 ; FORM A ONE
01359 040306 STA 0.RWLG ; INDICATE READ
01360 020216 LDA 0.SSEED ; INITIAL SEED
01361 040217 STA 0.CSEED ; INITIALIZE SEED
01362 020170 LDA 0.IIBUF ; ADDRESS OF INPUT BUFFER
01363 024222 LDA 1.DMBIT ;
01364 123000 ADD L0
01365 062120 DOSS 0.DSK ; READ FROM CONTROLLER
01366 030115 LDA 2.M20 ; MINUS 16
01367 034170 LDA 3.IIBUF ; ADDRESS OF INPUT BUFFER
01368 174400 NEG 3.3 ; DECREMENT
01369 054020 STA 3.20 ; SET POINTERS
01370 054021 STA 3.21 ; SET POINTERS
01371 022020 CMP 0.20 ; GET WORD
01372 174000 COM 3.3 ; COMPLEMENT
01373 054020 STA 3.20 ; SET POINTERS
01374 054021 STA 3.21 ; SET POINTERS
01375 100000 LDA 2.M20 ; MINUS 16
01376 042021 STA 0.21 ; STORE IT BACK
01377 151404 INC 2.5ZR
01378 000774 JMP M2RD ; READ THE DATA SWITCHES
01379 030151 LDA 2.RD2WR ; SEE IF NOT 2 READS PER WRITE
01380 174305 AND 3.2.SHR ;
01381 060432 JMP M2CRD ; SECOND READ
01382 030135 M2C: LDA 2.PRINS ; ABORT TEST BIT
01383 173404 AND 3.2.SZR ; MASK SWITCHES
01384 002214 JMP @ISTRT ; GO TO BEGINNING
01385 074477 READS 3 ; READS 3
01386 030137 LDA 2.LPERS ; PRINT CYCLE COUNT SWITCH
01387 173404 AND 3.2.SHR ;
01388 060244 JSR @IPC2 ; YES PRINT CYCLE COUNT
01389 074477 READS 3
01390 030140 LDA 2.LPTST ; GET LOOP ON TEST BIT
01391 173404 AND 3.2.SZR ; MASK SWITCHES
01392 000440 JMP @M20UT ; YES LOOP
01393 030150 LDA 2.DPALL ; MASK OF PATTERN DATA SWITCHES
01394 173405 AND 3.2.SHR ; SEE IF 0 SELECTED
01395 000425 JMP @P2NX ; YES DO ALL PATTERNS
01396 030150 M2EXT: LDA 2.EOCIN ; END OF TEST PRINT INHIBIT ?
01397 173404 AND 3.2.SZR ; SEE IF SET
01398 020217 M2OUT: LDA 0.CSEED ; GET CURRENT SEED
01399 006864 JSR @ICRLF ; CARRIAGE RETURN
01399 086865 JSR @IMESS ; MESSAGE
01400 083735 IPASS
01401 020217 M2OUT: LDA 0.CSEED ; GET CURRENT SEED
STA 0. SSLED ; USE AS INITIAL SEED
SUB 0. 0 ; FORM A ZERO
STA 0. SWFLG ; ALLOW PATTERN CHANGE
JMP 0. +1
EDIAG

M2RD: LDA 0. M22 ; SECOND READ FLAG
MOV 0. 0. 5ZR ; SEE IF SET
JMP M2C2 ; YES
ISZ M22 ; OTHERWISE SET IT
JMP M2RD ; DO SECOND READ
SUB 0. 0 ; FORM A ZERO
STA 0. M22 ; RESET SECOND READ FLAG
JMP M2C ; CONTINUE TEST

P2NX: SUB 0. 0 ; FORM A ZERO
STA 0. PATF ; RESET PATTERN PER TRACK SWITCH
STA 0. SWFLG ; RESET PATTERN CHANGE INHIBIT
LDA 0. CURPT ; GET THE CURRENT PATTERN CODE
LDA 1. C1 ; GET A ONE
SUB 0. 1. SZR ; SEE IF CODE EQUAL 1
P2NX2: JMP M2B ; NO DO TEST WITH NEXT PATTERN
JMP M2EXT ; YES ALL DONE

M2B2: LDA 0. CSEED ; GET THE CURRENT SEED
STA 0. SSEED ; USE AS INITIAL SEED
SUB 0. 0 ; FORM A ZERO
STA 0. SWFLG ; ALLOW PATTERN CHANGE
JMP P2NX2
<table>
<thead>
<tr>
<th>Line</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>01471</td>
<td>034116 MODE3: LDA 3,C3; GET A THREE</td>
</tr>
<tr>
<td>14</td>
<td>01472</td>
<td>054166 STA 3,MODE; SET CURRENT MODE</td>
</tr>
<tr>
<td>15</td>
<td>01473</td>
<td>074477 READS 3; READ THE DATA SWITCHES</td>
</tr>
<tr>
<td>16</td>
<td>01474</td>
<td>030150 LDA 2,E0CIN; PRINT INHIBIT BIT</td>
</tr>
<tr>
<td>17</td>
<td>01475</td>
<td>173404 AND 3,2,SZR; MASK THE SWITCHES</td>
</tr>
<tr>
<td>18</td>
<td>01476</td>
<td>000404 JMP M3B</td>
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<td></td>
<td></td>
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<tr>
<td>19</td>
<td>01477</td>
<td>000604 JSR @ICRLF; CARRIAGE RETURN LINE FEED</td>
</tr>
<tr>
<td>20</td>
<td>01500</td>
<td>000665 JSR @MESS; MESSAGE</td>
</tr>
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<td>21</td>
<td>01581</td>
<td>004042 MOD3M</td>
</tr>
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<td>22</td>
<td>01582</td>
<td>020167 LDA 0,IOBUF; GET BUFFER ADDRESS</td>
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<td>23</td>
<td>01583</td>
<td>126400 SUB 1,1; START WITH 0</td>
</tr>
<tr>
<td>24</td>
<td>01584</td>
<td>044257 STA 1,MOD3T; INITIALIZE TRACK ADDRESS</td>
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<tr>
<td>25</td>
<td>01585</td>
<td>044477 STA 1,DSKH; INITIALIZE DISC NUMBER</td>
</tr>
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<td>26</td>
<td>01586</td>
<td>030134 MOD3C: LDA 2,M1; TIME OUT VALUE</td>
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<td>27</td>
<td>01587</td>
<td>050302 STA 2,WCNTR; SET COUNTER</td>
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<td>28</td>
<td>01589</td>
<td>152408 SUB 2,2; FORM A ZERO</td>
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<td>29</td>
<td>01590</td>
<td>050306 STA 2,RFULG; INDICATE WRITE</td>
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<td>30</td>
<td>01592</td>
<td>056520 DDA 1,DSK; SET SECT ADDRESS</td>
</tr>
<tr>
<td>31</td>
<td>01593</td>
<td>062320 DOBP 0,DSK; SET BUFFER ADDRESS AND WRITE TO DISC</td>
</tr>
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<td>32</td>
<td>01594</td>
<td>063620 SKPDN DSK; WAIT FOR DONE</td>
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<td>33</td>
<td>01595</td>
<td>063631 JSR @IULP;</td>
</tr>
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<td>34</td>
<td>01596</td>
<td>070420 DIA 2,DSK; READ THE STATUS</td>
</tr>
<tr>
<td>35</td>
<td>01597</td>
<td>050204 STA 2,STERS; SAVE THE STATUS</td>
</tr>
<tr>
<td>36</td>
<td>01598</td>
<td>044205 STA 1,STS; T/S FOE STATUS ROUTINE</td>
</tr>
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<td>37</td>
<td>01599</td>
<td>034104 LDA 3,DSSFAL; GET DISC FAIL BIT</td>
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<tr>
<td>38</td>
<td>01600</td>
<td>157405 AND 2,3,SR;</td>
</tr>
<tr>
<td>39</td>
<td>01601</td>
<td>000403 JMP M3D</td>
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<td>40</td>
<td>01602</td>
<td>000503 JSR @1STER; PRINT STATUS</td>
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<tr>
<td>41</td>
<td>01603</td>
<td>000572 JMP M3H; GO TO NEXT TRACK</td>
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<tr>
<td>42</td>
<td>01604</td>
<td>034161 M3O: LDA 3,MSDIS; GET NO SUCH DISC BIT</td>
</tr>
<tr>
<td>43</td>
<td>01605</td>
<td>057404 AND 2,3,SR; AND TO STATUS</td>
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<tr>
<td>44</td>
<td>01606</td>
<td>004667 JMP MOD3B</td>
</tr>
<tr>
<td>45</td>
<td>01607</td>
<td>034163 LDA 3,WRERR; GET A WRITE ERROR BIT</td>
</tr>
<tr>
<td>46</td>
<td>01608</td>
<td>157404 AND 2,3,SR; MASK STATUS</td>
</tr>
<tr>
<td>47</td>
<td>01609</td>
<td>000576 JMP MOD3D; YES REPORT IT</td>
</tr>
<tr>
<td>48</td>
<td>01610</td>
<td>074477 READS 3; READ THE DATA SWITCHES</td>
</tr>
<tr>
<td>49</td>
<td>01611</td>
<td>030135 LDA 2,PRINS; GET THE ABORT BIT</td>
</tr>
<tr>
<td>50</td>
<td>01612</td>
<td>173404 AND 3,2,SR; MASK TO SWITCHES</td>
</tr>
<tr>
<td>51</td>
<td>01613</td>
<td>002214 JMP @1STRT;</td>
</tr>
<tr>
<td>52</td>
<td>01614</td>
<td>030137 LDA 2,LPERS; PRINT CYCLE COUNT SWITCH</td>
</tr>
<tr>
<td>53</td>
<td>01615</td>
<td>173404 AND 3,2,SR; SEE IF SET</td>
</tr>
<tr>
<td>54</td>
<td>01616</td>
<td>006244 JSR @IPCT2; PRINT CYCLE COUNT</td>
</tr>
</tbody>
</table>
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2 01543 034432 M3P: LDA 3, M3INC ; GET SECTOR ADDRESS INCREMENT
3 01544 167000 ADD 3, i
4 01545 044257 STA 1, MOD3T ; SAVE CURRENT TRACK ADDRESS
5 01546 020432 LDA 0, DSKM ; GET CURRENT DISK NUMBER
6 01547 034251 LDA 3, ISCO ; ADDRESS OF DISC TABLE
7 01548 117000 ADD 0, 3 ; FORM POINTER INTO TABLE
8 01549 021000 LDA 0, 0, 3 ; GET CURRENT DISC CODE
9 01550 131000 MOV 1, 2 ; CURRENT ADDRESS
10 01551 034242 LDA 3, DSC3 ; MASK OF DISC BITS
11 01552 173000 AND 3, 2 ; MASK TO CURRENT DISC
12 01553 012415 SUB 0, 2, SNR ; SEE IF INCREMENTED PAST CURRENT DISC
13 01554 000730 JMP MOD3C ; NO CONTINUE TO NEXT TRACK
14 01555 000444 JMP M3N ; YES PRINT LAST ADDRESS MESSAGE
15
16
17 01556 074477 M3G: READS 3 ; READ THE DATA SWITCHES
18 01557 030150 LDA 2, EOCIN ; END OF TEST PRINT INHIBIT ?
19 01558 173404 AND 3, 2, SZR ; SEE IF SET
20 01559 000405 JMP M3OUT ; YES
21
22 01560 006064 JSR @ICRLF ; CARRAGE RETURN LINE FEED
23 01561 006065 JSR @IMESS ; MESSAGE
24 01562 003735 IPASS
25
26 01563 074477 READS 3 ; READ THE DATA SWITCHES
27 01564 030140 M3OUT: LDA 2, LPTST ; GET LOOP ON TEST BIT
28 01565 173404 AND 3, 2, SZR ; MASK SWITCHES
29 01566 000710 JMP M3B ; YES LOOP
30
31 01567 002401 JMP @.T1
32 01568 004134 EDIAG
33
34 01569 008040 M3INC: 40
35 01570 007777 TSMSK: 7777
36
37 01571 000000 DSC0: 0
38 01572 010000 DSCI: 10000
39 01573 020000 DSC2: 20000
40 01574 030000 DSC3: 30000
41
42 01575 010000 DSINC: 10000
43 01576 000000 DSKM: 0
44 01577 044220 DSKM: .TXTE \ DISC }
45 01578 051711
46 01579 129303
47 01580 000240
48 01581 047240 MODSM: .TXTE \ NO DISC }
49 01582 128317
50 01583 144504
51 01584 141523
52 01585 128248
53 01586 000000
54
55 01587 044257 MOD3B: STA 1, MOD3T ; SAVE CURRENT ADDRESS
56 01588 020756 LDA 0, TSMSK ; MASK FOR TRACK AND SECTOR
57 01589 007415 AND 0, 1, SNR ; SEE IF ANYTHING THIS DISC
58 01590 000526 JMP M3E ; NOTHING
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2 01623 12400 M3H: NEG 1,1; FORM LAST VALID ADDRESS
3 01624 12400 COM 1,1; READ DATA SWITCHES
4 01625 044257 STA 1.MOD3T; SAVE ADDRESS
5 01626 044174 STA 1.MXSEC; SET MAXIMUM SECTOR
6 01627 074477 READS 3; READ DATA SWITCHES
7 01630 030158 LDA 2.EOCIN
8 01631 173400 AND 3.2.SZR; SEE IF SET
9 01632 000416 JMP M3C
10 01633 006064 JSR @XH; CARRIAGE RETURN, LINE FEED
11 01634 006065 JSR @IMESS; PRINT MESSAGE
12 01635 003723 LASTV
13 01636 024257 LDA 1.MOD3T; GET SAVVED ADDRESS
14 01637 034737 LDA 3.TSMSK; TRACK SECTOR MASK
15 01640 167400 AND 3.1; MASK OUT DISC ADDRESS
16 01641 096297 JSR @IPDOT; PRINT ADDRESS
17 01642 006606 M3K: JSR @IMESS; MESSAGE
18 01643 001605 DSKM
19 01644 030123 LDA 2.C60; ASCII ZERO
20 01645 020737 LDA 0.DSKH; CURRENT DISC
21 01646 143000 ADD 2.0; FORM DISC NO. IN ASCII
22 01647 006210 JSR @ICHAR; PRINT IT
23
24 01650 024257 M3C: LDA 1.MOD3T; GET LAST ADDRESS
25 01651 034725 LDA 3.TSMSK; MAX TRACK PER DISC
26 01652 167400 AND 3.1; MASK TO TRACK/SECTOR
27 01653 166415 SUB* 3.1.SNR; SEE IF MAX FOR THIS DISC
28 01654 000443 JMP M3H
29 01655 024257 LDA 1.MOD3T
30 01656 125400 INC 1.1; OTHERWISE GO TO NEXT TRACK OF THIS DISC
31 01657 020716 STA 0.M3INC; GET TRACK INCREMENT
32 01660 187000 ADD 0.1; SET FOR NEXT TRACK
33 01661 020167 LDA 0.IDBUS; BUFFER ADDRESS
34 01662 030134 M3I: LDA 2.MI; TIME OUT VALUE
35 01663 050302 STA 2.WCNTR; SET COUNTER
36 01664 152400 SUB 2.2; FORM A ZERO
37 01665 050306 STA 2.RFLG; INDICATE WRITE
38 01666 065020 DDA 1.DSK; SET SECTOR ADDRESS
39 01667 062328 DBBP 0.DSK; SET BUFFER ADDRESS AND WRITE TO DISK
40 01670 063620 SAMP DSK; WAIT FOR DONE
41 01671 006381 JSR @IULP
42
43 01672 070420 DIA 2.DSK; SET DISK SYSTEM STATUS
44 01673 050204 STA 2.SFR; SAVE THE STATUS
45 01674 044205 STA 1.SFR; SAVE T/S FOR STATUS ROUTINE
46 01675 034164 LDA 3.DSFLAG; GET THE DISK FAIL BIT
47 01676 173404 AND 3.2.SR; SEE IF SET
48 01677 086203 JSR @ISTER; YES PRINT ERROR
49 01678 030204 LDA 2.STER; RESTORE STATUS
50 01679 034416 LDA 3.MDIS; GET NO SUCH DISC BIT
51 01680 173405 AND 3.2.SN; SHOULD BE SET
52 01681 006464 JMP M3J; OTHERWISE ERROR
53
54 01684 034671 LDA 3.M3INC; ADDRESS INCREMENT
55 01685 167000 ADD 3.1; FORM NEXT TRACK ADDRESS
56 01686 024476 LDA 0.DSKM; GET THE CURRENT DISC NUMBER
57 01687 034251 LDA 3.IDS0; ADDRESS OF TABLE
58 01688 117000 ADD 0.3; FORM POINTER INTO TABLE
13711 021400 LDA 0.0.3 ; GET CURRENT DISC CODE
13712 131000 MOV 1.2 ; CURRENT ADDRESS
13713 034667 LDA 3.DSC3 ; DISC BITS IN ADDRESS
13714 173400 AND 3.2 ; MASK ADDRESS TO DISC
13715 12405 sub 0.2.SNR ; SEE IF STILL EQUAL
13716 000744 JMP M31 ; DO NEXT TRACK THIS DISC
13717 010665 M3H: ISZ DSKN ; INCREMENT CURRENT DISC NO.
13718 030664 LDA 2.DSKN ; GET CURRENT DISC NO.
13719 034100 LDA 3.C4 ; GET A FOUR
13720 156415 ADD 2.3.SNR WHEN FOUR WE ARE DONE
13721 030635 JMP M3G ; OTHERWISE CONTINUE
13722 134251 LDA 3.IDSC0 ; ADDRESS OF TABLE
13723 157000 ADD 2.5 ; FORM DINTER INTO TABLE
13724 025400 LDA 1.0.3 ; GET NEXT DISC ADDRESS
13725 044257 STA 1.MOD3T SAVE CURRENT ADDRESS
13726 002256 M3L: JMP @I M3
13727 006064 JSR @ICRLF CARRIAGE RETURN LINE FEED
13728 006065 JSR @I MESS MESSAGE
13729 001611 NODSM
13730 030123 M3M: LDA 2.C60 ASCII ZERO
13731 020621 LDA 0.DSKN ; CURRENT DISC NO.
13732 002214 JMP @ISTRT TO THE BEGINNING
13733 173404 AND 3.2.SZR SEE IF SET
13734 002214 JMP @ISTRT TO THE BEGINNING
13735 030150 LDA 2.EOCIN SEE IF INHIBIT SET
13736 173404 AND 3.2.SZR SEE IF SET
13737 000770 JMP M3L CONTINUE
13738 006064 JSR @ICRLF CARRIAGE RETURN LINE FEED
13739 006065 JSR @I MESS MESSAGE
13740 003065 WP ROM
13741 006207 JSR @I PCRT PRINT IT
13742 002260 JMP @IPCP
13743 006064 JSR @ICRLF CARRIAGE RETURN LINE FEED
13744 006065 JSR @I MESS MESSAGE
13745 001611 NODSM
13746 030123 M3M: LDA 2.C60 ASCII ZERO
13747 020621 LDA 0.DSKN ; CURRENT DISC NO.
13748 002214 JMP @ISTRT TO THE BEGINNING
13749 173404 AND 3.2.SZR SEE IF SET
13750 002214 JMP @ISTRT TO THE BEGINNING
13751 030150 LDA 2.EOCIN SEE IF INHIBIT SET
13752 173404 AND 3.2.SZR SEE IF SET
13753 000731 JMP M3H IF INHIBITED JUST CONTINUE
13754 074477 M3E: READS 3 ; READ THE DATA SWITCHES
13755 038135 LDA 2.PRINS ; ABORT BIT
13756 173404 AND 3.2.SZR SEE IF SET
13757 002214 JMP @ISTRT TO THE BEGINNING
13758 030150 LDA 2.EOCIN SEE IF INHIBIT SET
13759 173404 AND 3.2.SZR SEE IF SET
13760 000731 JMP M3H IF INHIBITED JUST CONTINUE
13761 006064 JSR @ICRLF CARRIAGE RETURN LINE FEED
13762 006065 JSR @I MESS MESSAGE
13763 001611 NODSM
13764 030123 M3M: LDA 2.C60 ASCII ZERO
13765 020621 LDA 0.DSKN ; CURRENT DISC NO.
13766 002214 JMP @ISTRT TO THE BEGINNING
13767 030150 LDA 2.EOCIN SEE IF INHIBIT SET
13768 173404 AND 3.2.SZR SEE IF SET
13769 002214 JMP @ISTRT TO THE BEGINNING
13770 030135 LDA 2.PRINS ; ABORT BIT
13771 173404 AND 3.2.SZR SEE IF SET
13772 002214 JMP @ISTRT TO THE BEGINNING
13773 030150 LDA 2.EOCIN SEE IF INHIBIT ERROR PRINT
13774 173404 AND 3.2.SZR SEE IF SET
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1 01775 000722 JMP M3H ; DO NEXT DISC
2 01776 0006064 JSR @ICRLF ; CARRIAGE RETURN LINE FEED
3 01777 0006065 JSR @IMESS ; MESSAGE
4 02000 0028094 SZERM ; SIZING ERROR
5 02001 0006065 JSR @IMESS ; PRINT DISC
6 02002 001605 DSKM
7 02003 000757 JMP M3M ; DISC NUMBER
8
9 02004 144523 SZERM: .TXTE ISIZING ERROR !
10 02005 144532
11 02006 043516
12 02007 142640
13 02008 151322
14 02009 151317
15 02010 120240
16 02011 000000
17
TEST 4 DATA TRANSFER SECTORS

LDA 3.C4 ; GET A FOUR
STA 3.MODE ; SET CURRENT MODE
SUB 3 ; FORM A ZERO
STA 3.SFFLG ; RESET PATTERN SELECT INHIBIT
STA 3.INCE ; ZERO INCREMENT START
STA 3.DISKAD+1 ; RESET 1-2 READ FLAG
LDA 3.C1 ; GET A ONE
STA 3.CURP1 ; INITIAL PATTERN
READS 3 ; READ THE DATA SWITCHES
LDA 3.EDCN ; PRINT INHIBIT BIT
AND 3.2.SZP ; MASK THE SWITCHES

JSR @ICRF ; CARRIAGE RETURN LINE FEED
JSR @IMES ; MESSAGE
MOD4M
READS 3 ; READ THE DATA SWITCHES

LDA 0.MXSEC ; GET MAX SECTOR ADDRESS
STA 0.MSEC ; SET END TEST ADDRESS
SUB 0.B ; FORM A ZERO
STA 0.LOWSEC ; SET LOW SECTOR ADDRESS
STA 0.M4CTS ;
MOD4A: READS 3 ; READ DATA SWITCHES
LDA 0.DCN ; GET THE READ ONLY BIT
AND 3.2.SZP ; MASK TO SWITCH SETTING

JSR @PTRN ; GENERATE TEST PATTERN
40
JSR @ICRF ; CARRIAGE RETURN LINE FEED

LDA 0.MACTS ; GET START SECTOR ADDRESS
STA 0.M1 ; TIME OUT VALUE
STA 0.WCNRTR ; SET COUNTER
SUB 0.B ; FORM A ZERO
STA 0.SFFLG ; INDICATE WRITE

DOA 1.DSK ; SEND IT TO THE CONTROLLER
STA 1.M4CTS ; SAVE CURRENT ADDRESS
LDA 2.IOBUF ; BUFFER ADDRESS
STA 2.SFFLG ; NO MORE PATTERN CHANGE
DBP 2.DSK ; START WRITE

JSR @WLP ; WAIT FOR DONE
<table>
<thead>
<tr>
<th>Line</th>
<th>Line Number</th>
<th>Operation</th>
<th>Register</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>02072</td>
<td>DIA</td>
<td>00.DSK</td>
<td>READ THE STATUS</td>
</tr>
<tr>
<td>2</td>
<td>02073</td>
<td>STA</td>
<td>00.STERS</td>
<td>SAVE STATUS</td>
</tr>
<tr>
<td>3</td>
<td>02074</td>
<td>STA</td>
<td>01.STTS</td>
<td>SAVE T/S FOR STATUS ROUTINE</td>
</tr>
<tr>
<td>4</td>
<td>02075</td>
<td>LDA</td>
<td>02.ERROR</td>
<td>GET THE ERROR Bit</td>
</tr>
<tr>
<td>5</td>
<td>02076</td>
<td>AND</td>
<td>02.SZR</td>
<td>MASK THE STATUS</td>
</tr>
<tr>
<td>6</td>
<td>02077</td>
<td>JSR</td>
<td>00.ISTER</td>
<td>STATUS ERROR</td>
</tr>
<tr>
<td>7</td>
<td>02100</td>
<td>READS</td>
<td>3</td>
<td>READ THE DATA SWITCHES</td>
</tr>
<tr>
<td>8</td>
<td>02101</td>
<td>LDA</td>
<td>03.PRINS</td>
<td>GET THE ABORT BIT</td>
</tr>
<tr>
<td>9</td>
<td>02102</td>
<td>AND</td>
<td>03.SZR</td>
<td>MASK TO SWITCHES</td>
</tr>
<tr>
<td>10</td>
<td>02103</td>
<td>JMP</td>
<td>00.ISTRT</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>02104</td>
<td>LDA</td>
<td>02.LPERS</td>
<td>PRINT CYCLE COUNT SWITCH</td>
</tr>
<tr>
<td>12</td>
<td>02105</td>
<td>AND</td>
<td>02.SZR</td>
<td>SEE IF SET</td>
</tr>
<tr>
<td>13</td>
<td>02106</td>
<td>JSR</td>
<td>00.IPC2</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>02107</td>
<td>READS</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>02110</td>
<td>LDA</td>
<td>01.8745</td>
<td>GET CURRENT ADDRESS</td>
</tr>
<tr>
<td>16</td>
<td>02111</td>
<td>LDA</td>
<td>01.M4CTS</td>
<td>INCREMENT TRACK/SECTOR ADDRESS</td>
</tr>
<tr>
<td>17</td>
<td>02112</td>
<td>LDA</td>
<td>02.HISEC</td>
<td>GET MAX TRACK/SECTOR</td>
</tr>
<tr>
<td>18</td>
<td>02113</td>
<td>SUBZ</td>
<td>02.SHC</td>
<td>SUBTRACT CURRENT</td>
</tr>
<tr>
<td>19</td>
<td>02114</td>
<td>JMP</td>
<td>00.M4N</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>02115</td>
<td>LDA</td>
<td>02.PATE</td>
<td>SEE IF PATTERN PER TRACK SET</td>
</tr>
<tr>
<td>21</td>
<td>02116</td>
<td>MOV</td>
<td>00.SNR</td>
<td>SEE IF SET</td>
</tr>
<tr>
<td>22</td>
<td>02117</td>
<td>JMP</td>
<td>00.M4LP</td>
<td>GENERATE NEXT PATTERN</td>
</tr>
<tr>
<td>23</td>
<td>02118</td>
<td>JMP</td>
<td>00.MOD4B</td>
<td>DO NEXT WRITE</td>
</tr>
<tr>
<td>24</td>
<td>02119</td>
<td>JMP</td>
<td>00.MOD4W</td>
<td>YES DO WRITE ONLY</td>
</tr>
<tr>
<td>25</td>
<td>02120</td>
<td>JMP</td>
<td>00.M4N</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>02121</td>
<td>LDA</td>
<td>02.WRONLY</td>
<td>GET THE WRITE ONLY BIT</td>
</tr>
<tr>
<td>27</td>
<td>02122</td>
<td>AND</td>
<td>02.SZR</td>
<td>MASK THE SWITCH Setting</td>
</tr>
<tr>
<td>28</td>
<td>02123</td>
<td>JMP</td>
<td>00.MOD4W</td>
<td>YES DO WRITE ONLY</td>
</tr>
<tr>
<td>29</td>
<td>02124</td>
<td>JSR</td>
<td>00.9ULP</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>02125</td>
<td>DIA</td>
<td>00.DSK</td>
<td>READ THE STATUS</td>
</tr>
<tr>
<td>31</td>
<td>02126</td>
<td>STA</td>
<td>00.STERS</td>
<td>SAVE STATUS</td>
</tr>
<tr>
<td>32</td>
<td>02127</td>
<td>STA</td>
<td>01.STTS</td>
<td>SAVE T/S FOR STATUS ROUTINE</td>
</tr>
<tr>
<td>33</td>
<td>02128</td>
<td>LDA</td>
<td>02.ERROR</td>
<td>GET THE ERROR Bit</td>
</tr>
<tr>
<td>34</td>
<td>02129</td>
<td>AND</td>
<td>02.SZR</td>
<td>MASK THE STATUS</td>
</tr>
<tr>
<td>35</td>
<td>02130</td>
<td>MOV</td>
<td>00.2</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>02131</td>
<td>LDA</td>
<td>02.WRONLY</td>
<td>GET THE WRITE ONLY BIT</td>
</tr>
<tr>
<td>37</td>
<td>02132</td>
<td>DOR</td>
<td>02.DSK</td>
<td>SEND IT TO CONTROLLER</td>
</tr>
<tr>
<td>38</td>
<td>02133</td>
<td>STA</td>
<td>02.DSKAD</td>
<td>SAVE CURRENT ADDRESS</td>
</tr>
<tr>
<td>39</td>
<td>02134</td>
<td>LDA</td>
<td>02.11BUF</td>
<td>INPUT BUFFER</td>
</tr>
<tr>
<td>40</td>
<td>02135</td>
<td>DOB</td>
<td>02.DSK</td>
<td>READ THE SECTOR</td>
</tr>
<tr>
<td>41</td>
<td>02136</td>
<td>SKPDN</td>
<td>00.DSK</td>
<td>WAIT FOR DONE</td>
</tr>
<tr>
<td>42</td>
<td>02137</td>
<td>JSR</td>
<td>00.9ULP</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The above code snippet represents a portion of a computer program written in assembly language. It appears to be part of a larger context, possibly related to data handling or file operations. The comments and labels indicate various steps such as reading status, saving status, checking error bits, and handling different types of operations like reads and writes. The specific context or system this code is intended for is not explicitly clear from the snippet alone.
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1 02152 006212 JSR #1COMP : COMPARE DATA
2 02153 000400 #800 ; NO. OF WORDS
3 02154 014000 OBUP ; DATA WRITTEN
4 02155 018000 IBUF ; DATA READ
5 02156 000000 DSKAD: 0 ; CURRENT TRACK/SECTOR
6 02157 000000 0 ; FIRST/SECOND FLAG

7
8 02160 074477 READS 3 ; READ THE DATA SWITCHES
9 02161 030135 LDA 2,PRINS ; GET THE ABORT BIT
10 02162 173404 AND 3,2.SZR ; MASK TO SWITCHES
11 02163 002214 JMP #1STRT
12 02164 030137 LDA 2,LPERS ; PRINT CYCLE COUNT
13 02165 173404 AND 3,2.SZR ; SEE IF SET
14 02166 006244 JSR #1PCT2 ; PRINT CYCLE COUNT
15 02167 074477 READS 3
16
17 02170 030151 LDA 2,RD2UR ; 2 READS PER WRITE BIT
18 02171 173405 AND 3,2.SNR ; MASK SWITCHES
19 02172 000464 JMP CSRDL ; SECOND READ
20
21 02173 024763 M4NX: LDA 1,DSKAD ; GET THE LAST READ TRACK/SECTOR
22 02174 125400 INC 1,1 ; INCREMENT ADDRESS
23 02175 030173 LDA 2,HISEC ; GET THE MAX TRACK/SECTOR
24 02176 132423 SUBZ 1,2.SNC ; SEE IF EQUAL
25 02177 000430 JMP MOD4D
26 27
28 02200 000731 JMP M4RLP ; READ NEXT SECTOR
29
30 ; GET THE LOOP PARAMETERS
31
32 02201 006064 MOD4LP: JSR #1CRLF ; CARRIAGE RETURN LINE FEED
33 02202 005065 JSR #1MESS ; MESSAGE
34 02203 003010 SECP
35 02204 152400 SUB 2,2 ; GET CHARACTERS
36 02205 006220 JSR #1T4IN ; READ THE TELETYPE
37 02206 000773 JMP MOD4LP ; ERROR
38 02207 050172 STA 2,LOWSEC ; SET THE START SECTOR ADDRESS
39 02208 050645 STA 2,M4CTS
40
41 02211 006064 M4M: JSR #1CRLF ; CARRIAGE RETURN LINE FEED
42 02212 005065 JSR #1MESS ; MESSAGE
43 02213 003020 ESCP
44 02214 152400 SUB 2,2 ; GET CHARACTERS
45 02215 006220 JSR #1T4IN ; READ THE TELETYPE
46 02216 000773 JMP M4M ; ERROR
47 02217 050173 STA 2,HISEC ; SET END SECTOR ADDRESS
48 02218 050173 LDA 1,LOWSEC ; GET THE LOW
49 02219 046416 SUB 2,1.SNC ; SEE IF HI EQUALS LOW
50 02220 000622 JMP MOD4A ; YES ITS OK
51 02221 146412 SUB 2,1.SEC ; OTHERWISE HI MUST BE GRATER
52 02222 000256 JMP MOD4LP ; IF NOT TRY AGAIN
53 02223 000457 JMP M4P
54
55 02226 000616 M4O: JMP MOD4A ; LINKAGE
56
57
58 ; READS COMPLETED FIND WHAT TO DO NEXT

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PAGE 2B

MOD4D: READS 3 : READ THE DATA SWITCHES
MOD4W: LDA 2.LPTST : CHECK FOR LOOP ON TEST
AND 3.2.SZR : MASK TO DATA SWITCHES
JMP M4P : YES REPEAT THE TEST

READS 3 : READ THE DATA SWITCHES
LDA 2.DPALL : MASK OF PATTERN SELECT SWITCHES
AND 3.2.SNR : SEE IF ALL PATTERNS SELECTED
JMP P4NX : YES

M4EXT: READS 3 : READ DATA SWITCHES
LDA 2.EOCIN : END OF TEST PRINT INHIBIT ?
AND 3.2.SZR : SEE IF SET
JMP M4OUT : YES
JSR @ICRLF : CARRIAGE RETURN LINE FEED
JSR IMESS : MESSAGE

M40UT: LDA 2.PRINS GET THE ABORT BIT
AND 3.2.SZR MASK TO SWITCHES
JMP alSTRT
ISZ T4CY INCREMENT CYCLE COUNT
JSR IJ .
EDIAG
CSRD: LDA l.DSKAD ; GET CURRENT ADDRESS
LDA 2.DSKAD+1 : GET SECOND READ FLAG
JMP CSR02 : YES
ISZ DSKAD+1 SET SECOND READ FLAG
LDA 3.PATE GET PATTERN PER TRACK SWITCH
STA 3.PATES SAVE IT
SUB 3.3 FORM A ZERO
STA 3.PATE RESET PATE FOR SECOND READ
JMP M4RLP DO THE SECOND READ
CSRD2: SUB 2.2 FORM A ZERO
STA 3.PATE GET THE SAVED PATE
STA 3.PATE ;
JMP M4NX
P4NX: SUB 0.0 FORM A ZERO
STA 0.PATE ; RESET PATTERN PER TRACK SWITCH
STA 0.SWFLG ALLOW PATTERN CHANGE
LDA 0.CURPT GET A ONE
SUB 0.1.SNR SEE IF A ONE
JMP M4EXT YES ALL DONE
LDA 0.LOWSEC : GET START SECTOR
M4P: LDA 0.WM4 USE AS CURRENT SECTOR
SUB 0.0 FORM A ZERO
STA 0.INCE START INCREMENT WITH ZERO
STA 0.SWFLG ALLOW PATTERN CHANGE
<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>02311 040233</td>
<td>STA 0.PATE : RESET PATTERN PER TRACK</td>
</tr>
<tr>
<td>2</td>
<td>02312 020216</td>
<td>LDA 0.SSEED : GET INITIAL SEED</td>
</tr>
<tr>
<td>3</td>
<td>02313 040217</td>
<td>STA 0.CSEED : USE AS CURRENT SEED</td>
</tr>
<tr>
<td>4</td>
<td>02314 000712</td>
<td>JMP .M40</td>
</tr>
</tbody>
</table>
TEST 5 DATA TRANSFER SUB SECTORS

02315 173000 MSAA: ADD 3.2 ; FORM SUB SECTOR DECREMENT
02316 124000 NEG 1.1 ; DECREMENT COUNT
02317 124000 COM 1.1
02320 000444 JMP MSAC

02321 034112 MODES: LDA 3.CS ; GET A FIVE
02322 054166 STA 3.MODE ; SET CURRENT MODE
02323 176400 SUB 3.3 ; FORM A ZERO
02324 054261 STA 3.SWFLG ; RESET SELECT PATTERN INHIBIT
02325 054246 STA 3.INCE ; START INCREMENT WITH ZERO
02326 056262 STA 3.WMS2 ; RESET 1-2 READ FLAG
02327 034110 LDA 3.CI ; GET A ONE
02328 054215 STA 3.CURPT ; CURRENT PATTERN CODE
02329 054177 STA 3.NSSC ; DEFAULT NO. OF SUB SECTORS
02330 074477 READS 3 ; READ THE DATA SWITCHES
02331 030150 LDA 2.EDC ; PRINT INHIBIT BT
02332 173404 AND 3.2.SZR ; MASK THE SWITCHES
02333 000404 JMP MSB

02336 006064 JSR 1CRLF ; CARRIAGE RETURN LINE FEED
02337 006085 JSR 1MESS ; MESSAGE
02340 046235 MOD5A: LDA 1.LOWSEC ; GET START SECTOR
02341 044425 STA 1.M5
02342 046235 STA 1.M5CT
02343 024177 LDA l.NSSC ; NUMBER OF SUB SECTOR
02346 040173 STA l.MSSC ; GET MAX SUB SECTOR
02347 020176 LDA l.HSSC ; SET START TEST ADDRESS
02348 040227 STA l.HSSEC ; SET END SUB SECTOR
02351 018200 SUB 0.0 ; FORM A ZERO
02352 040172 STA 0.LOWSEC ; SET START TEST ADDRESS
02353 040226 STA 0.LSSEC ; SET START SUB SECTOR
02354 024172 MOD5A: LDA 1.LOWSEC ; GET START SECTOR
02355 046235 STA 1.W1MS
02356 044425 STA 1.MSC
02357 024177 LDA 1.NSSC ; NUMBER OF SUB SECTOR
02360 124400 NEG 1.1 ; DECREMENT IT
02361 124000 COM 1.1
02362 034120 LDA 3.2C0 ; WORD COUNT INCREMENT
02363 030120 LDA 2.2C0 ; BASIC WORD COUNT
02364 125004 MOV 1.1.SZR ; SEE IF ZERO YET
02365 000730 JMP MSAA ; NO
02366 058413 STA 2.MODA
02367 050564 STA 2.M5AB ; SET WORD COUNT
02370 052264 STA 2.WMSAD

02371 074477 MOD5B: READS 3
02372 030144 LDA 2.RDONLY ; GET THE READ ONLY BIT
02373 173400 AND 3.2 ; MASK TO SWITCH SETTING
02374 151004 MOV 2.2.SZR ; SEE IF SET
I 02375 000513 JMP MOD5R YES DO READ ONLY
3 02376 030217 LDA 2,CSEED GET CURRENT SEED
4 02377 050216 STA 2,SEED USE AS INITIAL SEED

5
6
7 02400 006213 JSR wIPTRN GENERATE TEST PATTERN
8 02401 000020 MODA: 20 NO. OF WORDS
9 02402 014000 OBUF OUT BUFFER
10 02403 000000 M5CT: 0 CURRENT TRACK/SECTOR ADDRESS

11
12 02404 024172 M5WA: LDA 1,LOWSEC GET THE START SECTOR ADDRESS
13 02405 030236 LDA 2,SSONE INITIAL SUB SECTOR ADDRESS
14 02406 050261 STA 2,SUFLG NO MORE PATTERN CHANGE
15 02407 034256 LDA 3,LSSEC GET THE START SUB SECTOR
16 02410 020177 LDA 0,NSSC NUMBER OF SUB SECTORS
17 02411 100400 NEG 0,0 DECREMENT
18 02412 100000 COM 0,0
19 02413 112400 SUB 0,2
20 02414 173520 MOVZS 3,3 SHIFT TO HI BYTE
21 02415 177120 ADDZL 3,3 SHIFT 2 MORE BITS
22 02416 177120 ADDZL 3,3 SHIFT 2 MORE BITS
23 02417 173000 ADD 3,2 FORM START SUB SECTOR ADDRESS

24
25 02420 020134 MSWLP: LDA 0,M1 TIME OUT VALUE
26 02421 040302 STA 0,WCNTR SET COUNTER
27 02422 163404 AND 0,3,SZRS MASK TO SWITCHES
28 02423 040306 STA 0,RUFLG INDICATE WRITE
29 02424 065028 DOA 1,DSK SEND IT TO THE CONTROLLER
30 02425 034167 LDA 3,IOBUF BUFFER ADDRESS
31 02426 076828 DDB 3,DSK START WRITE
32 02427 073328 DDCF 2,DSK WRITE A SUB SECTOR
33 02430 063620 SKPDN DSK WAIT FOR DONE
34 02431 006301 JSR 0,MSLP

35
36 02432 006420 DIA 0,DSK READ THE STATUS
37 02433 040204 STA 0,STERS
38 02434 044205 STA 1,STTS SAVE T/S FOR STATUS ROUTINE
39 02435 034157 LDA 3,ERROR GET THE ERROR BIT
40 02436 117400 AND 0,3 MASK THE STATUS
41 02437 175804 MOV 3,3,SZR SEE IF ERROR BIT SET
42 02440 005203 JSR 0,ISTER STA US ERROR
43
44 02441 074477 READS 3 READ THE DATA SWITCHES
45 02442 020139 LDA 0,PRINS GET THE ABORT BIT
46 02443 163404 AND 3,0,SZR MASK TO SWITCHES
47 02444 002214 JMP 0,ISTRT

48
49 02445 030137 LDA 2,LPERS PRINT CYCLE COUNT?
50 02446 173404 AND 3,2,SZR SEE IF SET
51 02447 006244 JSR 0,IPCT2 PRINT CYCLE COUNT
52
53 02450 020177 LDA 0, NSSC GET NO. OF SUB SECTORS
54 02451 040200 STA 0,WRK1 SAVE IT
55 02452 102400 SUB 0,2 FORM A ZERO
56 02453 034237 LDA 3,SSINC SUB SECTOR INCREMENT
57 02454 163600 ADD 3,0
58 02455 014200 DSZ 0,WRK1 DECREMENT COUNT
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02456  000776  JMP  AD  ; REPEAT
1 02457 113022  ADDZ  0.2.SZC  ;
2 02458 000411  JMP  MSL  ;
3 02461 034227  LDA  3.LSSEC  ; GET MAX SUB SECTOR
4 02462 175320  MOVZS  3.3  ; SHIFT TO HI BYTE
5 02463 177120  ADDZL  3.3  ; SHIFT 2 MORE BITS
6 02464 177120  ADDZL  3.3  ; SHIFT 2 MORE BITS
7 02465 020236  LDA  0.SSOHE  ; SEE IF MAX YET
8 02466 117000  ADD  0.3  ; FORM MAX SUB SECTOR ADDRESS
9 02467 156422  SUBZ  2.3.SZC  ;
10 02468 125400  M5L:  IHC
11 02469 030236  LDA  2.SSOHE  ; RESET SUB SECTOR ADDRESS
12 02470 034226  LDA  3.LSSEC  ; GET THE START SUB SECTOR
13 02471 175320  MOVZS  3.3  ; SHIFT TO HI BYTE
14 02472 177120  ADDZL  3.3  ; SHIFT 2 MORE BITS
15 02473 177120  ADDZL  3.3  ; SHIFT 2 MORE BITS
16 02474 173000  ADD  3.2  ; FORM START SUB SECTOR ADDRESS
17 02475 101400  HEG  0.0  ;
18 02476 122424  SUBZ  1.0.SZR  ; SUBTRACT CURRENT
19 02477 126400  HOD5R:  SUB
20 02478 044216  STA  1.LOWSEC  ; GET START TRACK/SECTOR ADDRESS
21 02479 044217  STA  1.CSEED  ; USE AS CURRENT SEED
22 02480 044218  STA  1.HISEC  ; GET MAX TRACK/SECTOR
23 02481 020173  LDA  0.HISEC  ;
24 02482 101400  HEG  0.0  ;
25 02483 122424  SUBZ  1.0.SZR  ;
26 02484 074477  READS  3  ; READ DATA SWITCHES
27 02485 030145  LDA  2.WROHLY  ; GET THE WRITE ONLY BIT
28 02486 173404  AND  3.2.SZR  ; MASK THE SWITCH SETTING
29 02487 022625  JMP  @IMSW  ; YES DO WRITE ONLY
30 02488 020134  H5RLP:  LDA  0.M1  ; TIME OUT VALUE
31 02489 040302  STA  0.WCNR  ; SET COUNTER
32 02490 020110  LDA  0.C1  ; GET A ONE
33 02491 040306  STA  0.RUFLG  ; INDICATE READ
34 02492 065020  DOA  1.DSK  ; SEND IT TO CONTROLLER
35 02493 076020  DOB  3.DSK  ; READ THE SECTOR
36 02494 073120  DOC5  2.DSK
37 02495 063620  SKPDN  DSK  ; WAIT FOR DONE
38 02496 066301  JSR  @WLP
2 02541 060420 DIA 0.DSK ; READ THE STATUS
3 02542 040204 STA 0.STERS ; SAVE STATUS
4 02543 044205 STA 1.STTS ; SAVE T/S FOR STAGE ROUTINE
5 02544 034157 LDA 3.ERROR ; GET THE ERROR BIT
6 02545 117400 AND 0.3 ; MASK THE STATUS
7 02546 175804 MOV 3.3.SZS ; SEE IF ERROR BIT SET
8 02547 006203 JSR @ISTERS ; STATUS ERROR
9 02550 044406 STA 1.DSKS ; SAVE CURRENT TRACK/SECTOR
10 02551 050252 STA 2.DSK6 ; SAVE CURRENT SUB SECTOR
11 02552 006212 JSR @ICOMP ; COMPARE DATA
12 02553 000026 MSAB: 2B ; NO. OF WORDS
13 02554 014000 OBuf ; DATA WRITTEN
14 02555 010000 IBuf ; DATA READ
15 02556 000000 DSK5 : 0 ; CURRENT TRACK/SECTOR
16 02557 000000 MS2: 0 ; FIRST/SECOND FLAG
17 02560 074477 READS 3 ; READ THE DATA SWITCHES
18 02561 030135 LDA 2.PRINS ; GET THE ABORT BIT
19 02562 173404 AND 3.2.SZR ; MASK TO SWITCHES
20 02563 002214 JMP @ISTRT
21 02564 030137 LDA 2.LPERS ; PRINT CYCLE COUNT ?
22 02565 173404 AND 3.2.SZR ; SEE IF SET
23 02566 006244 JSR @PCT2 ; PRINT CYCLE COUNT
24 02567 074477 READS 3
25 02570 024766 LDA 1.DSK5 ; RESTORE SECTOR ADDRESS
26 02571 035252 LDA 2.DSK6 ; RESTOR SUB SECTOR
27 02572 020151 LDA 0.RD2WR ; 2 READS PER WRITE
28 02573 163405 AND 3.0.SNR ; SEE IF SET
29 02574 000057 JMP MSS ; DO SECOND READ
30 02575 020177 MSQ: LDA 0.NSSC ; NO. OF SUB SECTOR
31 02576 040200 STA 3.WRK1 ; SAVE IT
32 02577 102400 SUB 0.0 ; FORM A ZERO
33 02578 034237 LDA 3.SSINC ; SUB SECTOR INCREMENT
34 02579 163000 ADD 3.0 ;
35 02580 014200 DSZ WRK1 ; DECREMENT COUNT
36 02581 000776 JMP .-2
37 02582 113022 ADDZ 0.2.SZC
38 02583 008411 JMP MSS ;
39 02584 034227 LDA 3.HISEC ; GET MAX SUB SECTOR
40 02585 175320 MOVZS 3.3 ; SHIFT TO HI BYTE
41 02586 032207 ADDZL 3.3 ; SHIFT 2 MORE BITS
42 02587 177120 ADDZL 3.3 ; SHIFT 2 MORE BITS
43 02588 020236 LDA 0.SSONE ; ONE SUB SECTOR
44 02589 117000 ADD 0.3 ; FORM MAX SUB SECTOR ADDRESS
45 02590 156422 SUBZ 2.3.SZC ; SAVE IF MAX YET
46 02591 000712 JMP MSRLP
47 02592 034173 LDA 3.HISEC ; GET THE MAX TRACK/SECTOR
48 02593 136425 SUBZ 1.3.SNR ; SEE IF EQUAL
49 02594 000500 JMP MOD5D
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1 02621 125400 MSR: INC 1.1 : INCREMENT CURRENT TRACK/SECTOR
2 02622 030236 LDA 2.550NE : INITIAL SUB SECTOR ADDRESS
3 02623 034226 LDA 3.55SEC : GET THE START SUB SECTOR
4 02624 175320 MOVZS 3.3 : SHIFT TO HI BYTE
5 02625 177120 ADDZL 3.3 : SHIFT 2 MORE BITS
6 02626 177120 ADDZL 3.3 : SHIFT 2 MORE BITS
7 02627 173000 ADD 3.2 FORM START SUB SECTOR ADDRESS
8 02630 000677 M5V: JMP M5RLP READ NEXT SECTOR
9
10
11
12 02631 006064 MOD5LP: JSR @ICRLF : CARRIAGE RETURN LINE FEED
13 02632 006065 JSR @IMESS : MESSAGE
14 02633 003010 SECP
15 02634 152400 SUB 2.2 : GET CHARACTERS
16 02635 006220 JSR @IT4IN : READ THE TTY
17 02636 000773 JMP MOD5LP : ERROR
18 02637 050173 STA 2.LOWSEC : SET THE START SECTOR ADDRESS
19
20 02640 006064 M50: JSR @ICRLF : CARRIAGE RETURN LINE FEED
21 02641 006065 JSR @IMESS : MESSAGE
22 02642 003020 ESCP
23 02643 152400 SUB 2.2 : GET CHARACTERS
24 02644 006220 JSR @IT4IN : READ THE TTY
25 02645 000773 JMP MOD5LP : ERROR
26 02646 024172 LDA 1.LOUSEC : GET LOW SECTOR ADDRESS
27 02647 146415 SUB 2.1.SNR : SEE IF EQUAL
28 02648 000403 JMP M5U : EQUAL IS OK
29 02649 146432 SUB 2.1.SZC : HI SEC SHOULD BE GREATER
30 02650 000757 JMP MOD5LP : OTHERWISE TRY AGAIN
31 02653 050173 STA 2.HISEC : SET HI SECTOR ADDRESS
32
33 02654 006064 M5K: JSR @ICRLF : CARRIAGE RETURN LINE FEED
34 02655 006065 JSR @IMESS : MESSAGE
35 02656 003027 SSEC
36 02657 152400 SUB 2.2 : GET CHARACTERS
37 02658 006220 JSR @IT4IN : READ TTY
38 02660 000773 JMP M5K : ERROR
39 02662 050227 STA 2.LSSEC : SET START SUB SECTOR
40
41 02663 006064 M5N: JSR @ICRLF : CARRIAGE RETURN LINE FEED
42 02664 006065 JSR @IMESS : MESSAGE
43 02665 003041 SESC
44 02666 152400 SUB 2.2 : GET CHARACTERS
45 02667 006220 JSR @IT4IN : READ THE TTY
46 02668 000773 JMP M5N : ERROR
47 02669 024226 LDA 1.LSSEC : GET LOW SUB SECTOR
48 02670 146415 SUB 2.1.SNR : SEE IF EQUAL
49 02671 000403 JMP M5P : EQUAL OK
50 02672 146432 SUB 2.1.SZC : HI MUST BE GREATER
51 02673 006064 M5P: JSR @ICRLF : CARRIAGE RETURN LINE FEED
52 02674 006065 JSR @IMESS : MESSAGE
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1 02704 003052 02705 152400 02706 006220 02707 008773 02710 151005 02711 008072 02712 024120 02713 146433 02714 000773 02715 050177 02716 002401 02717 002354

2 02704 NO SUB SECTORS MESSAGE 02705 GET CHARACTERS 02706 READ TTY 02707 TRY AGAIN IF ERROR 02710 SEE IF ZERO 02711 RESET ALL ON ZERO 02712 MAX SUB SECTOR 02713 IF GRATER 02714 YES NO GOOD

3 02706 SUB SECTOR 02707 READ TTY 02708 TRY AGAIN IF ERROR 02709 RETRY THE TEST 02710 ALL PATTERNS SELECTED 02711 YES 02712 YES

4 02708 LDA I.C20 02709 MAX SUB SECTOR 02710 SEE IF GRATER 02711 ALL PATTERNS SELECTED 02712 YES

5 02711 LDA I.PATE 02712 GET PATTERN PER SECTOR

6 02712 MOV 3.3.SNR 02713 SET

7 02713 LDA 2.PATE 02714 GET THE PATTERN

8 02714 LDA 0.TATR 02715 SECOND READ FLAG

9 02715 MOV 0.0.SZ 02716 SEE IF SET

10 02716 JMP 0.1.M5 02717 SET

11 02717 LDA 0.PATE 02718 GET THE PATTERN PR TRACK SWITCH

12 02718 LDA 0.ATR 02719 SET
L3/0B/76
1 02760 040234 STA B.PATES; SAVE IT
2 02761 102400 SUB B.0; FORM A ZERO
3 02762 040233 STA B.PATE; RESET PATTERN PER TRACK FOR SECOND READ
4 02763 086645 JMP MSV; DO THE SECOND READ
5 02764 020234 MST: LDA B. PATES; GET THE PATTERN SWITCH
6 02765 040233 STA B.PATE
7 02766 102400 SUB B.0; FORM A ZERO
8 02767 042262 STA B.1 IM52; reset second read flag
9 02768 002388 JMP @IM50; read next sub sector
10 02769 102400 P5NX: SUB B.0; FORM A ZERO
11 02770 040233 STA B.PATE; RESET PATTERN PER TRACK SWITCH
12 02771 040261 STA B.SWFLG; ALLOW PATTERN CHANGE
13 02772 020215 LDA B.CURPT; GET CURRENT PATTERN CODE
14 02773 040217 STA B.CSEED; USE AS CURRENT SEED
15 02774 002240 JMP MD5
16 02775 102400 M5Y: SUB B.0; FORM A ZERO
17 02776 040261 STA B.SWFLG; ALLOW PATTERN CHANGE
18 02777 020216 LDA B.SSEED; GET INITIAL SEED
19 02778 000000 ECODE: 0
20 02779 007300 JMP M5EXT; YES
21 02780 047305 ESCP: .TXTE !START SECTOR !
22 02781 000000 .RDX 0
23 02782 047305 SESCP: .TXTE !END SUB SECTOR !
24 02783 047305 SECP: .TXTE !START SECTOR !
25 02784 000000 .RDX 0
26 02785 047305 SESCP: .TXTE !END SECTOR !
27 02786 000000 .RDX 0
28 02787 047305 SESCP: .TXTE !END SECTOR !
29 02788 000000 .RDX 0
30 02789 047305 SESCP: .TXTE !END SECTOR !
31 02790 000000 .RDX 0
32 02791 047305 SESCP: .TXTE !END SUB SECTOR !
33 02792 000000 .RDX 0
34 02793 047305 SESCP: .TXTE !END SECTOR !
35 02794 000000 .RDX 0
36 02795 047305 SESCP: .TXTE !END SECTOR !
37 02796 000000 .RDX 0
38 02797 047305 SESCP: .TXTE !END SECTOR !
39 02798 000000 .RDX 0
40 02799 047305 SESCP: .TXTE !END SECTOR !
41 02800 000000 .RDX 0
42 02801 047305 SESCP: .TXTE !END SECTOR !
43 02802 000000 .RDX 0
44 02803 047305 SESCP: .TXTE !END SECTOR !
45 02804 000000 .RDX 0
46 02805 047305 SESCP: .TXTE !END SECTOR !
47 02806 000000 .RDX 0
48 02807 047305 SESCP: .TXTE !END SECTOR !
49 02808 000000 .RDX 0
50 02809 047305 SESCP: .TXTE !END SECTOR !
51 02810 000000 .RDX 0
52 02811 047305 SESCP: .TXTE !END SECTOR !
53 02812 000000 .RDX 0
54 02813 047305 SESCP: .TXTE !END SECTOR !
55 02814 000000 .RDX 0
56 02815 047305 SESCP: .TXTE !END SECTOR !
57 02816 000000 .RDX 0
58 02817 047305 SESCP: .TXTE !END SECTOR !
59 02818 000000 .RDX 0
60 02819 047305 SESCP: .TXTE !END SECTOR !
<table>
<thead>
<tr>
<th>Page</th>
<th>Time</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>120104</td>
<td>TXTE 15SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>2</td>
<td>120523</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>3</td>
<td>120102</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>4</td>
<td>142523</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>5</td>
<td>152383</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>6</td>
<td>151317</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>7</td>
<td>120240</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>8</td>
<td>000000</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>9</td>
<td>147516</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>10</td>
<td>120856</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>11</td>
<td>143517</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>12</td>
<td>051640</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>13</td>
<td>041123</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>14</td>
<td>051640</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>15</td>
<td>141705</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>16</td>
<td>147724</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>17</td>
<td>051722</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>18</td>
<td>120240</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>19</td>
<td>000000</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>20</td>
<td>142523</td>
<td>TXTE 19SXY: OF SUB SECTORS</td>
</tr>
<tr>
<td>21</td>
<td>151327</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>22</td>
<td>152311</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>23</td>
<td>120305</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>24</td>
<td>151120</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>25</td>
<td>152317</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>26</td>
<td>141705</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>27</td>
<td>120324</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>28</td>
<td>042101</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>29</td>
<td>151104</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>30</td>
<td>051705</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>31</td>
<td>120123</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>32</td>
<td>120240</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>33</td>
<td>000000</td>
<td>TXTE WRITE PROTECT ADDRESS</td>
</tr>
<tr>
<td>34</td>
<td>142523</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>35</td>
<td>120324</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>36</td>
<td>040504</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>37</td>
<td>040724</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>38</td>
<td>051640</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>39</td>
<td>144727</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>40</td>
<td>141724</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>41</td>
<td>145210</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>42</td>
<td>120123</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>43</td>
<td>120855</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>44</td>
<td>147724</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>45</td>
<td>144724</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>46</td>
<td>142523</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>47</td>
<td>000000</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>48</td>
<td>042104</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>49</td>
<td>051640</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>50</td>
<td>142510</td>
<td>TXTE SET DATA SWITCHES - CONTINUE</td>
</tr>
<tr>
<td>51</td>
<td>040504</td>
<td>TXTE DATA SWITCHES</td>
</tr>
<tr>
<td>52</td>
<td>040724</td>
<td>TXTE DATA SWITCHES</td>
</tr>
<tr>
<td>53</td>
<td>051640</td>
<td>TXTE DATA SWITCHES</td>
</tr>
<tr>
<td>54</td>
<td>144724</td>
<td>TXTE DATA SWITCHES</td>
</tr>
<tr>
<td>55</td>
<td>141724</td>
<td>TXTE DATA SWITCHES</td>
</tr>
<tr>
<td>56</td>
<td>142510</td>
<td>TXTE DATA SWITCHES</td>
</tr>
</tbody>
</table>
I03213 137275
2 03214 152240
3 03215 051705
4 03216 051724
5 03217 130640
6 03220 152240
7 03221 151110
8 03222 120125
9 03223 120264
10 03224 000000
11
12 03225 120060 INST8: RXTE 10 0 1 -> TEST 1 DISCRETE CONTROLLER TESTS!
13 03226 120060
14 03227 120261
15 03230 137275
16 03231 152240
17 03232 051705
18 03233 120324
19 03234 120261
20 03235 144504
21 03236 141523
22 03237 142722
23 03238 142724
24 03241 141648
25 03242 047317
26 03243 151324
27 03244 146317
28 03245 142714
29 03246 120322
30 03247 142724
31 03250 152123
32 03251 120123
33 03252 000000
34
35 03253 120060 INST9: RXTE 10 1 0 -> TEST 2 DIAGNOSTIC MODE!
36 03254 120261
37 03255 120060
38 03256 137275
39 03257 152240
40 03260 051705
41 03261 120244
42 03262 120262
43 03263 144504
44 03264 043501
45 03265 147516
46 03266 152123
47 03267 141711
48 03270 046640
49 03271 042317
50 03272 120305
51 03273 000000
52
53 03274 120060 INSTA: RXTE 10 1 1 -> TEST 3 SIZE/WRITE PROTECT!
54 03275 120261
55 03276 120261
56 03277 137275
57 03280 152240
58 03281 051705
13 08 76

1 03302 120324
2 03303 120663
3 03304 145523
4 03305 142532
5 03306 153657
6 03307 144722
7 03310 142724
8 03311 050240
9 03312 147722
10 03313 142724
11 03314 152303
12 03315 000240
13
14 03316 120261
INSTD: .TXTE 11 0 0 => TEST 4 DATA TRANSFER (SECTOR)

15
16 03320 120060
17 03321 137275
18 03322 152240
19 03323 051705
20 03324 120324
21 03325 120264
22 03326 040504
23 03327 040724
24 03328 152240
25 03329 040722
26 03332 051516
27 03333 142706
28 03334 120322
29 03335 051450
30 03336 141705
31 03337 147724
32 03340 142722
33 03341 000240
34
35 03342 120261
INSTD: .TXTE 11 0 0 => TEST 5 DATA TRANSFER (SUB SECTOR)

36
37 03343 120060
38 03344 120261
39 03345 137275
40 03346 152240
41 03347 051705
42 03350 120324
43 03351 120065
44 03352 040504
45 03353 040724
46 03354 152240
47 03355 040722
48 03356 051516
49 03357 142706
50 03360 120322
51 03361 051450
52 03362 041125
53 03363 051640
54 03364 141705
55 03365 147724
56 03366 124722
57 03367 000240
58 03370 120261
INSTD: .TXTE 11 1 0 => TESTS 1, 2 AND 4
1 03371 120261
2 03372 120262
3 03373 137275
4 03374 152240
5 03375 051705
6 03376 051724
7 03377 130640
8 03400 120254
9 03401 120262
10 03402 647101
11 03403 120104
12 03404 120264
13 03405 000000
14
15 03406 120261
16 03407 120261
17 03410 120261
18 03411 137275
19 03412 152240
20 03413 051705
21 03414 051724
22 03415 131248
23 03416 040648
24 03417 042116
25 03420 132240
26 03421 000240
27
28 03422 120267
29 03423 142722
30 03424 042101
31 03425 147648
32 03426 146116
33 03427 120131
34 03430 000000
35
36 03431 120270
37 03432 151327
38 03433 152311
39 03434 120385
40 03435 047317
41 03436 054714
42 03437 000240
43
44 03440 120071
45 03441 047311
46 03442 144510
47 03443 144582
48 03444 128524
49 03445 049504
50 03446 040724
51 03447 142648
52 03450 151322
53 03451 151317
54 03452 059248
55 03453 144722
56 03454 152116
57 03455 000240
58
INST: .TXTE 10 INHIBIT STATUS ERROR PRINT !

INST: .TXTE 11 INHIBIT END OF TEST PRINT !

INST: .TXTE 12 TWO READS PER WRITE INHIBIT !

INST: .TXTE 13, 14, 15 SELECT DATA PATTERN !
<table>
<thead>
<tr>
<th>Index</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>03633 151234</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>03634 141581</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>03635 127513</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>03636 142523</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>03637 152303</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>03638 151317</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>03639 146640</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>03640 128104</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>03641 150000</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>03642 03643</td>
<td>WORST CASE</td>
</tr>
<tr>
<td>11</td>
<td>03644 130640</td>
<td>INSTQ: .TXTE ! 1 0 0 -&gt; WORST CASE !</td>
</tr>
<tr>
<td>12</td>
<td>03645 128240</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>03646 038240</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>03647 128240</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>03648 038240</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>03649 136640</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>03650 136640</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>03651 136640</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>03652 136640</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>03653 147727</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>03654 051722</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>03655 128324</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>03656 040703</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>03657 142523</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>03658 000000</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>03659 130640</td>
<td>INST: .TXTE ! 1 0 1 -&gt; ONES !</td>
</tr>
<tr>
<td>27</td>
<td>03660 128240</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>03661 030240</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>03662 128240</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>03663 136640</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>03664 136640</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>03665 136640</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>03666 136640</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>03667 128276</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>03668 047317</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>03669 051705</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>03670 000240</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>03671 130640</td>
<td>INST: .TXTE ! 1 1 0 -&gt; ZEROES !</td>
</tr>
<tr>
<td>39</td>
<td>03672 128240</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>03673 136640</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>03674 136640</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>03675 136640</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>03676 128240</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>03677 030240</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>03678 136640</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>03679 128276</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>03680 142532</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>03681 147722</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>03682 051705</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>03683 000240</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>03684 130640</td>
<td>INST: .TXTE ! 1 1 1 -&gt; SELECTABLE !</td>
</tr>
<tr>
<td>52</td>
<td>03685 128240</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>03686 136640</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>03687 128240</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>03688 136640</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>03689 128276</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>03690 142523</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>03691 142714</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>03692 152303</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>03693 041101</td>
<td></td>
</tr>
<tr>
<td>Page 45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13/08/76</td>
<td></td>
<td></td>
</tr>
<tr>
<td>03721</td>
<td>142714</td>
<td></td>
</tr>
<tr>
<td>03722</td>
<td>000240</td>
<td></td>
</tr>
<tr>
<td>03723</td>
<td>040714</td>
<td></td>
</tr>
<tr>
<td>03724</td>
<td>152123</td>
<td></td>
</tr>
<tr>
<td>03725</td>
<td>053240</td>
<td></td>
</tr>
<tr>
<td>03726</td>
<td>146101</td>
<td></td>
</tr>
<tr>
<td>03727</td>
<td>042311</td>
<td></td>
</tr>
<tr>
<td>03728</td>
<td>040640</td>
<td></td>
</tr>
<tr>
<td>03729</td>
<td>042104</td>
<td></td>
</tr>
<tr>
<td>03730</td>
<td>042722</td>
<td></td>
</tr>
<tr>
<td>03731</td>
<td>051523</td>
<td></td>
</tr>
<tr>
<td>03732</td>
<td>000240</td>
<td></td>
</tr>
<tr>
<td>03733</td>
<td>026705</td>
<td></td>
</tr>
<tr>
<td>03734</td>
<td>120324</td>
<td></td>
</tr>
<tr>
<td>03735</td>
<td>142520</td>
<td></td>
</tr>
<tr>
<td>03736</td>
<td>131240</td>
<td></td>
</tr>
<tr>
<td>03737</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03738</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03739</td>
<td>042240</td>
<td></td>
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<tr>
<td>03740</td>
<td>042240</td>
<td></td>
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<tr>
<td>03741</td>
<td>042240</td>
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<td>03742</td>
<td>042240</td>
<td></td>
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<td>03743</td>
<td>042240</td>
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<td>03744</td>
<td>042240</td>
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<td>03745</td>
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<tr>
<td>03746</td>
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<td></td>
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<tr>
<td>03747</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03748</td>
<td>042240</td>
<td></td>
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<tr>
<td>03749</td>
<td>042240</td>
<td></td>
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<tr>
<td>03750</td>
<td>042240</td>
<td></td>
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<tr>
<td>03751</td>
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<td>03752</td>
<td>042240</td>
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<td>03753</td>
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<td>03754</td>
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<td>03755</td>
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<td>03756</td>
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<td>03757</td>
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<td>03758</td>
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<td>03759</td>
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<td>03760</td>
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<td>03762</td>
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<td>03763</td>
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<td>03764</td>
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<td>03765</td>
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<tr>
<td>03766</td>
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<td></td>
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<tr>
<td>03767</td>
<td>042240</td>
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<td>03768</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03769</td>
<td>042240</td>
<td></td>
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<tr>
<td>03770</td>
<td>042240</td>
<td></td>
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<tr>
<td>03771</td>
<td>042240</td>
<td></td>
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<tr>
<td>03772</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03773</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03774</td>
<td>042240</td>
<td></td>
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<tr>
<td>03775</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03776</td>
<td>042240</td>
<td></td>
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<tr>
<td>03777</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03778</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03779</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03780</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03781</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03782</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03783</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03784</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03785</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03786</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03787</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03788</td>
<td>042240</td>
<td></td>
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<tr>
<td>03789</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03790</td>
<td>042240</td>
<td></td>
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<td>03791</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03792</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03793</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03794</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03795</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03796</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03797</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03798</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03799</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03800</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03801</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03802</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03803</td>
<td>042240</td>
<td></td>
</tr>
<tr>
<td>03804</td>
<td>042240</td>
<td></td>
</tr>
</tbody>
</table>
MOD1M: DISCRETE CONTROLLER TESTS!
MOD2M: CPU-CONTROLLER DATA PATH TEST!
MOD3M: DISC SIZE TEST!
MOD4M: DATA PATH TEST (SECTOR)
MOD5M: DATA PATH TEST (SUB-SECTOR)
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1 04071 152101
2 04072 120118
3 04073 14724
4 04074 152123
5 04075 024240
6 04076 052523
7 04077 026502
8 04100 142523
9 04101 152303
10 04102 151317
11 04103 000000
12
13 04104 147714 THOM: .TXTE !LOOP ON RNT •
14 04105 050317
15 04106 147640
16 04107 120116
17 04110 047322
18 04111 120324
19 04112 120243
20 04113 000000
21
22 04114 047305 EPSM: .TXTE !END OF CYCLE !
23 04115 120104
24 04116 143317
25 04117 141640
26 04118 141531
27 04121 142714
28 04122 000000
29
30 04123 147523 TMSG: .TXTE !SOFTWARE TIMEOUT !
31 04124 152306
32 04125 040727
33 04126 142722
34 04127 152240
35 04130 047111
36 04131 147705
37 04132 152125
38 04133 000000
39
40 04134 024166 EDIA: LDA 1, MODE
41 04135 181000 EOC2: MOV O, O ;ITERATE TEST.
42 04136 030156 LBA 2, MODAL ;ALL MODE SWITCHES
43 04137 074477 READS 3 ;READ THE DATA SWITHCES
44 04138 173400 AND 3.2 ;SEE WHICH RE SET
45 04139 153328 MOVZS 2.2 ;SUAP BYTES
46 04140 151220 MOVZR 2.2 ;SHIFT BITS TO LOW ORDER
47 04141 024224 EOC4: LDA 1, 11MOD ;ADDRESS OF MODE TABLE
48 04144 133000 ADD 1.2 ;FORM POINTER INTO TABLE
49 04145 030000 JMP @0.2 ;JUMP TO CURRENT MODE
50
51 04146 084156 IMODE: MODE0 ;TESTS 1 THRU 4
52 04147 084430 MAXE1 ;TEST 1
53 04150 083103 MODE2 ;TEST 2
54 04151 081471 MODE3 ;TEST 3
55 04152 082914 MODE4 ;TEST 4
56 04153 083221 MODE5 ;TEST 5
57 04154 084167 MODE6 ;TESTS 1, 2 AND 4
I04155 004206 MODE7 : TESTS 2 AND 4

4 04156 010166 MODE8: ISZ MODE : INCREMENT MODE
5 04157 030166 LDA 2.MODE : GET THE MODE
6 04160 024112 LDA 1.C5 : MAX TEST NO.
7 04161 132432 SUBZ+ 1.2.SZC : SEE IF GREATER THAN MAX
8 04162 000402 JMP EPMS : YES END OF PASS
9 04163 000760 JMP EOC4

10 04164 152400 EPMS: SUB 2.2 : GET A ZERO
12 04165 050166 STA 2.MODE : SET MODE
13 04166 000755 JMP EOC4

15 04167 030166 MODE6: LDA 2.MODE : GET CURRENT MODE
16 04170 020110 LDA 0,C1 : GET A ONE
18 04172 034100 LDA 3.C4 : GET A FOUR
19 04173 112415 SUB+ 0.2.SNR : SEE IF CURRENTLY 1
20 04174 000405 JMP M6A YES
21 04175 132415 SUB+ 1.2.SHR : SEE IF CURRENTLY 2
22 04176 000406 JMP M6B YES
23 04177 111000 MOV 0.2 : OTHERWISE MUST BE FOUR
24 04200 000402 JMP M6C SET TO 1
25 04201 151400 M6A: INC 2.2 : FORM A TWO
27 04202 050166 M6C: STA 2.MODE : SET NEXT MODE
28 04203 000740 JMP EOC4 GO TO NEXT TEST
29 04204 133000 M6B: ADD 1.2 : FORM A FOUR
30 04205 000775 JMP M6C

33 04206 030166 MODE7: LDA 2.MODE : GET THE CURRENT MODE
34 04207 024111 LDA 1.C2 : GET A TWO
35 04210 132415 SUB+ 1.2.SNR : SEE IF CURRENTLY 2
36 04211 000403 JMP M7A
37 04212 030111 LDA 2.C2 : GET A TWO
38 04213 000767 JMP M6C : GO TO TEST
40 04215 000402 JMP M6C : GO TO TEST
41 04216 054054 DCODE: STA 3.DRET :SET THE I/O INST
42 04217 062677 IORST :DEVICE CODES.
43 04218 060664 JSR #ICRLF
45 04219 080655 JSR #IMESS
46 04220 03761 DEVNUM
47 04221 030107 LDA 2.C2000
48 04222 004450 SHFL: JSR TIN :TYPE INPUT
50 04223 034121 LDA 3.C70
52 04226 116032 ADCZ+ 0.3.SZB
53 04227 034122 LDA 3.CM6B
54 04230 117046 ADDO 0.3.SEZ
55 04231 000767 JMP DCODE+2 : NOT A DIGIT
56 04232 151120 MOVZL 2.2
57 04233 153120 ADDZL 2.2
58 04234 173803 ADD 3.2.SNC :ASSEMBLE 2 DIGITS
59 04235 000767 JMP SHFL
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1 04236 024120 LDA 1.C20
2 04237 020123 LDA 0.C60
3 04240 146414 SUB 2.1.SZR
4 04240 142415 SUB 2.ELSNR
5 04241 10 101 l MOV+ 0.0.SKP
6 04242 01Hl755 JMP DCPDE+2
7 04244 050055 STA 2.DEV!CE
8 04245 030062 DEVCD: LDA 2.FJRST ;MODIFY I/O !MST
9 04246 021000 LDA 0.2.BETWEEN FIRST
10 04247 024124 LDA 1.C1600 ;AND LAST.
11 04250 123400 AND 1.0
12 04251 106414 SUB+ 0.J.SZR
13 04252 000414 JMP DEV1 ;NOT I/O
14 04254 021000 LDA 0.0.2
15 04255 024126 LDA 1.C77
16 04256 123400 AND 1.0
17 04257 106415 SUB+ 0.1.SNR
18 04258 000407 JMP DEVI ;CPU INST
19 04259 021000 LDA 0.0.2
20 04260 024127 LDA 1.C77
21 04261 151400 DEVI: INC 2.2
22 04262 024123 LDA 0.0.2
23 04263 123400 ADD 1.0
24 04264 024054 LDA 1.DEVICE
25 04265 041000 STA 0.0.2
26 04266 151400 TIN: STA 3.TINRET;TYPE INPUT
27 04267 063610 SHFL: JSR TIN GET A CHARACTER
28 04268 063511 LDA 3.c713 MASK
29 04269 163400 ADCZ+ 0.3.SZC ???
30 04270 061311 LOA 3.cM60
31 04271 17046 ADDO 0.3.SE<'. ???
32 04272 000407 JMP TIN1 NOT A DIGIT
33 04273 002054 JMP @TINRET
34 04274 054051 T41N: STA 3.TRET;SAVE RETURN ADDRESS
35 04275 063610 JKST: SET THE WORLD
36 04276 063511 JSK TIN: GET A CHARACTER
37 04277 063511 JSK 3.37E20
38 04278 061311 JSK 3.33E00
39 04279 163400 JSK 3.33E00
40 04280 063511 JSK 3.33E00
41 04281 063511 JSK 3.33E00
42 04282 063511 JSK 3.33E00
43 04283 063511 JSK 3.33E00
44 04284 063511 JSK 3.33E00
45 04285 063511 JSK 3.33E00
46 04286 063511 JSK 3.33E00
47 04287 063511 JSK 3.33E00
48 04288 063511 JSK 3.33E00
49 04289 063511 JSK 3.33E00
50 04290 063511 JSK 3.33E00
51 04291 063511 JSK 3.33E00
52 04292 063511 JSK 3.33E00
53 04293 063511 JSK 3.33E00
54 04294 063511 JSK 3.33E00
55 04295 063511 JSK 3.33E00
56 04296 063511 JSK 3.33E00
57 04297 063511 JSK 3.33E00
58 04298 063511 JSK 3.33E00
59 04299 063511 JSK 3.33E00
60 04300 063511 JSK 3.33E00
61 04301 063511 JSK 3.33E00
62 04302 063511 JSK 3.33E00
63 04303 063511 JSK 3.33E00
64 04304 063511 JSK 3.33E00
65 04305 063511 JSK 3.33E00
66 04306 063511 JSK 3.33E00
67 04307 063511 JSK 3.33E00
68 04308 063511 JSK 3.33E00
69 04309 063511 JSK 3.33E00
70 04310 063511 JSK 3.33E00
71 04311 063511 JSK 3.33E00
72 04312 063511 JSK 3.33E00
73 04313 063511 JSK 3.33E00
74 04314 116032 HACZ+ 0.3.35ZC
75 04315 034122 LDA 3.35E00
76 04316 117046 ADD0 0.3.35ZC
77 04317 008408 JMP T4IM ;NOT A DIGIT

ROUTE TO READ SOME DIGITS FROM TELETYPewriter
1 04320 151120 MOVZL 2,2
2 04321 153120 ADDZL 2,2 : SHIFT
3 04322 173003 ADD 3,2.5NC : ASSEMBLE DIGIT
4 04323 000767 JMP SH4FL : GET NEXT DIGIT
5
6 04324 010406 T4OUT: ISZ TRET : FORM NO ERROR RETURN ADDRESS
7 04325 002405 JMP ??TRET : RETURN
8
9 04326 034405 T4IM: LDA 3,CR : CARRIAGE RETURN CHARACTER
10 04327 116404 SUB 0,3.5ZR : SEE IF LAST CHAR A CR
11 04328 002402 JMP ??TRET : NO MUST BE ERROR
12 04330 000773 JMP T4OUT : OTHERWISE NORMAL EXIT
13
14 04332 000000 TRET: 0
15 04333 000015 CR: 15
ROUTINE TO PRINT STATUS ERROR

04334 054310 STA: STA 3.Stars; SAVE RETURN REGISTER
04335 044526 STA 1.SAVE1; SAVE AC 1
04336 050528 STA 2.SAVE2; SAVE AC 2
04337 074477 READS 3; READ DATA SWITCHES
04340 030147 LDA 2.STERIN; STATUS ERROR PRINT INHIBIT BIT
04341 173404 AND 3.2.SER; MASK THE SWITCHES
04342 000516 JMP SRTN; NO PRINT SO RETURN
04343 006064 JSR @ICRLF; CARRIAGE RETURN LINE FEED
04344 006065 JSR @IMESS; MESSAGE
04345 004467 STERM

04346 020306 LDA 0.RWFLG; GET THE READ/WRITE FLAG
04347 101005 MOV 0,0.SHR; SEE IF SET
04350 000404 JMP V,0; SRTN SEE IF SET
04351 006065 JSR @IMESS; PRINT MESSAGE
04352 000403 SRDM; RD

04353 000403 JMP SRT2

04354 006065 JSR @IMESS; MESSAGE
04355 004475 SUTM; UT

04356 030123 STER2: LDA 2.C60; GET AN ASCII 0
04357 020204 LDA 0.STERS; GET THE STATUS
04358 024505 LDA 1.STMK1; FIRST CHARACTER MASK
04361 123620 ANDZR 1.0; MASK TO STATUS
04362 101220 MOVZR 0.0; SHIFT
04363 101220 MOVZR 0.0; SHIFT TO LOW ORDER
04364 143000 ADD 2.0; FORM ASCII CHARACTER
04365 006210 JSR @ICHAR; PRINT THE CHARACTER
04366 020204 LDA 0.STERS; RELoad STATUS
04367 024477 LDA 1.STMK2; MASK FOR SECOND CHARACTER
04370 123400 AND 1.0; ISOLATE 2ND CHARACTER BITS
04371 143000 ADD 2.0; FORM ASCII CHARACTER
04372 006210 JSR @ICHAR; PRINT THE CHARACTER

04373 020273 STP: LDA 0.CBLK; ASCII BLANK
04374 006210 JSR @ICHAR; PRINT IT
04375 030122 LDA 2.C60; ASCII 0
04376 020205 LDA 0.STTS; GET SAVE T/S
04377 024265 LDA 1.DMSK; MASK TO DISC NO. BITS
04400 123700 ANDS 1.0; MASK IT
04401 101220 MOVZR 0.0; SHIFT
04402 101220 MOVZR 0.0; SHIFT
04403 101220 MOVZR 0.0; SHIFT
04404 101220 MOVZR 0.0; SHIFT
04405 143000 ADD 2.0; FORM ASCII
04406 006210 JSR @ICHAR; PRINT IT
1 04407 020273 LDA 0.CBLK ; ASCII BLANK
2 04410 006210 JSR wICAR ; PRINT IT

PRINT TRACK

1 04411 020205 LDA 0.STTS ; GET THE SAVE T/S
2 04412 024266 LDA 1.TMSK1 ; MASK TO HI CHARACTER
3 04413 123700 ANDS 1.0 ; AND IT TO MASK
4 04414 101220 MOVZR 0.0 ; SHIFT IT
5 04415 101220 MOVZR 0.0 ; SHIFT
6 04416 101220 MOVZR 0.0 ; SHIFT
7 04417 143000 ADD 2.0 ; FORM ASCII
8 04420 006210 JSR wICAR ; PRINT IT

PRINT TRACK

1 04421 020205 LDA 0.STTS ; GET THE SAVE T/S
2 04422 024267 LDA 1.TMSK2 ; MASK FOR SECOND CHARACTER
3 04423 123700 ANDS 1.0 ; MASK
4 04424 143000 ADD 2.0 ; FORM ASCII
5 04425 006210 JSR wICAR ; PRINT IT

PRINT SECTOR

1 04426 020205 LDA 0.STTS ; GET THE SAVE T/S
2 04427 024270 LDA 1.TMSK3 ; MASK TO LO CHARACTER
3 04430 123620 ANDZR 1.0 ; MASK
4 04431 101220 MOVZR 0.0 ; SHIFT
5 04432 101220 MOVZR 0.0 ; SHIFT
6 04433 101220 MOVZR 0.0 ; SHIFT
7 04434 101220 MOVZR 0.0 ; SHIFT
8 04435 143000 ADD 2.0 ; FORM ASCII
9 04436 006210 JSR wICAR ; PRINT IT
10 04437 020273 LDA 0.CBLK ; ASCII BLANK
11 04440 006210 JSR wICAR ; PRINT IT

PRINT SECTOR

1 04441 020205 LDA 0.STTS ; GET THE SAVE T/S
2 04442 024271 LDA 1.TMSK1 ; SECTOR MASK
3 04443 123620 ANDZ 1.0 ; MASK
4 04444 101220 MOVZR 0.0 ; SHIFT
5 04445 101220 MOVZR 0.0 ; SHIFT
6 04446 143000 ADD 2.0 ; FORM ASCII
7 04447 006210 JSR wICAR ; PRINT IT

PRINT SECTOR

1 04450 020205 LDA 0.STTS ; GET THE SAVE T/S
2 04451 024272 LDA 1.TMSK2 ; SECTOR MASK
3 04452 123400 AND 1.0 ; MASK
4 04453 143000 ADD 2.0 ; FORM ASCII
5 04454 006210 JSR wICAR ; PRINT IT
6 04455 020273 LDA 0.CBLK ; ASCII BLANK
7 04456 006210 JSR wICAR ; PRINT IT

PRINT SECTOR

1 04457 006243 JSR wIPCNT ; PRINT CYCLE COUNT
2 04460 024403 SRTN: LDA 1.SAVE1 ; RESTORE AC 1
3 04461 030403 LDA 2.SAVE2 ; RESTORE 2
4 04462 002310 JMP wSTARS ; RETURN

SAVE1: 0
5 04463 000000 SAVE2: 0

1 04465 000870 STMK1: 70
2 04466 00087 STMK2: 7
3
4 04467 152123 STEM: .TXTE ISTER !
5 04470 151320 .STERN: .TXTE ! RD !
6 04471 009240 .STERN: .TXTE ! RD !
7 04472 151240 SPM: .TXTE ! RD !
8 04473 120104 .STERN: .TXTE ! RD !
9 04474 000240 .STERN: .TXTE ! RD !
10 04475 136460 SPM: .TXTE ! RD !
11 04476 120324 .STERN: .TXTE ! RD !
12 04477 000240 .STERN: .TXTE ! RD !
13
14 04500 054430 ENTER: STA 3.LOOPR LOOP ITERATE RETURN
15 04501 074477 READS 3 READ THE DATA SWITCHES
16 04502 030135 LDA 2.PRINT TEST ABORT SWITCH
17 04503 173404 AND 3.2.SZR MASK SWITCHES
18 04504 082214 JMP @ISTRT ABORT
19 04505 030137 LDA 2.LPERS PRINT CYCLE COUNT
20 04506 173404 AND 3.2.SZR SEE IF SET
21 04507 096244 JSR @IPCT2 PRINT CYCLE COUNT
22 04508 034410 LDA 3.ITR THIS ROUTINE INITIALIZES
23 04509 054410 STA 3.ITRCT EACH TEST
24 04510 000165 ISZ ERRNO INCREMENT ERROR NUMBER
25 04511 054400 SUB 3.3
26 04512 054406 STA 3.ESWIT
27 04513 054406 STA 3.ERCT
28 04514 062677 IORST I/O RESET
29 04515 062411 JMP @LOOPR
30 04516 000144 ITR: 144
31 04517 000000 ITRCT: 0
32 04518 000000 ERRCT: 0
33 04519 000000 ESWIT: 0
34 04520 000000 ERR: STA 3.RETURN ; ERROR SUBROUTINE
35 04521 000000 SAV2: 0
36 04522 000000 SAV1: 0
37 04523 000000 SAV0: 0
38 04524 000000 LOOPR: 0
39 04525 000000 CYCLE: STA 3.RETURN: END OF TEST ITERATION
40 04526 000000 SAV2: 0
41 04527 000000 SAV1: 0
42 04528 000000 SAV0: 0
43 04529 000000 LOOPR: 0
44 04530 000000 CYCLE: STA 3.RETURN: END OF TEST ITERATION
45 04531 054773 READS 3 READ THE DATA SWITCHES
46 04532 050773 STA 2.SAV2 ROUTINE
47 04533 074477 READS 3 READ THE DATA SWITCHES
48 04534 062677 IORST I/O RESET
49 04535 082214 JMP @ISTRT
50 04536 030135 LDA 2.PRINT ABORT SET?
51 04537 173404 AND 3.2.SZR MASK SWITCHES
52 04538 082214 JMP @ISTRT
53 04539 030137 LDA 2.LPERS SEE IF LOOP ON TEST
54 04540 173404 AND 3.2.SZR MASK SWITCHES
55 04541 030137 LDA 2.LPERS SEE IF LOOP ON TEST
56 04542 002766 JMP @LOOPR ;(1) LOOP ROUTINE
57 04543 002761 JMP @RETURN ;(0) PROCEED TO NEXT TEST
58 04544 054773 ERR: STA 3.RETURN ; ERROR SUBROUTINE
59 04545 058760 STA 2.SAV2
60 04546 044760 STA 1.SAV
I 04547 048760 STA B.SAV0
2 04550 000487 JMP ERR1
3 04551 038754 ERET: LDA 2.SAV2 ;RESTORE ACS
4 04552 024754 LDA 1.SAV1
5 04553 028754 LDA 0.SAV0
6 04554 018747 ERHRT: ISZ ERR01 ;COUNT
7 04555 101000 MOV B,0 ;ERRORS, I/O RESET
8 04556 002746 JMP @RETURN ;EXIT
9
10 04557 034745 ERR1: LDA 3.RETURN;ERROR, C(3)•PC
11 04560 054742 STA 3.ESWIT
12 04561 074477 READS 3
13 04562 030146 LDA 2.DERRIN PRINT INHIBIT BIT
14 04563 173405 AND 3.2.SRIN MASK
15 04564 004406 JSR EPRINT PRINT THE ERROR
16 04565 074477 READS 3
17 04566 030136 LDA 2.ERHTS HALT ON ERROR BIT
18 04567 173404 AND 3.2.SZS MASK SWITCHES
19 04568 000411 JMP ERR3
20 04571 000760 JMP ERR1

21 04572 054730 EPRINT: STA 3.ESWIT ;ERROR MESSAGE PRINTER
22 04573 006064 JSR @ICRLF ;PRINT CARRIAGE
23 04574 004606 JSR @MESS ;AND HEADER
24 04575 004606 HEADER
25 04576 024165 LDA 1.ERROR
26 04577 085207 JSR @IPORT ;NO. OF ERROR
27 04580 002722 JMP @ESWIT ;RETURN TO CALL
28
29 30 04601 028726 ERR3: LDA 0.SAV0 ;RESTORE AC 0
31 04602 024724 LDA 1.SAV1 ;RESTORE AC 1
32 04603 038722 LDA 2.SAV2 ;RESTORE AC 2
33 04604 063077 HALT
34 04605 000747 JMP ERHRT ;RETURN
35
36 04606 151305 HEADER: .TSTE !ER+ !
37 04607 126243
38 04610 000000
; ROUTINE TO GENERATE DATA PATTERN
; CALLING SEQUENCE:
; JSR @!PATRN
; DC NUMBER OF WORDS
; DC ADDRESS OF BUFFER
; DC CURRENT TRACK/SECTOR ADDRESS
; DC FIRST/SECOND READ FLAG
; EXAMINE DATA SWITCHES 13, 14, 15 TO DETERMINE THE PATTERN.
; PATTERNS ARE:
; 13, 14, 15
; 0 0 0 ALL PATTERNS
; 0 0 1 RANDOM
; 0 1 0 INCREMENTING
; 1 0 0 WORST CASE
; 1 0 1 ONES
; 1 1 0 ZEROS
; 1 1 1 SELECTABLE
; PATRN: STA 3,PRTN ;SAVE RETURN
; 3,SWFLG : SEE IF PATTERN CHANGE IS INHIBITED
; JMP PCUR ; YES
; READS 3: GET DATA SWITCHES
; LDA 2,DPALL
; AND 3.2: MASK DP SWITCHES
; LDA 1,IPTbl : ADDRESS OF PATTERN HANDLERS TABLE
; ADD 1.2: ADD TO SWITCHES
; JMP @0.2: JUMP
; PAT4: LDA 3,IP4F :GET CURRENT PATTERN CODE
; PATBL: AL PAT
; RANPAT
; INCPAT
; IDPAT
; WCPAT
; ONEPAT
; ZERPAT
; SLPAT
; ALPAT: LDA 0,PATE ;GET PATTERN PER SECTOR FLAG
; MOV 0.0,SRZ: SEE IF SET
; JMP ALP2: IF SET REPEAT PATTERN
; DSZ CURPT : DECREMENT CURRENT PATTERNS
; JMP ALP2
; LDA 0.C6: GET A SIX
; STA 0,CURPT
; JMP ALP2: LDA 1,IPTbl : ADDRESS OF PATTERN HANDLERS TABLE
1 04646 133000 ADD 1.2 ADD TO SWITCH SETTING
2 04647 003000 JMP 08.2
3
4 04650 028112 ONEPAT: LDA 0. C5 GET A ONE
5 04651 049215 STA 0.CURPT SET CURRENT PATTERN
6 04652 028134 LDA 0. C1 GET A ONE
7 04653 034510 PAT1: LDA 3.PRTN GET THE NUMBER OF WORDS
8 04654 025400 LDA 1.0.3 SAVE IT
9 04655 044585 STA 1.CNTR DECREMENT COUNTER
10 04656 031401 LDA 2.1.3 GET THE BUFFER ADDRESS
11 04657 041000 PAT2: STA 0.0.2 STORE IN BUFFER
12 04660 151400 INC 2.2 INCREMENT BUFFER POINTER
13 04661 014501 DSZ CNTR DECREMENT COUNTER
14 04662 000775 JMP PAT2:
15 04663 001403 JMP 3.3 RETURN
16
17 04664 028113 ZERPAT: LDA 0. C6 GET A TWO
18 04665 049215 STA 0.CURPT SET CURRENT PATTERN
19 04666 012400 SUB 0.0 GET A ZERO
20 04667 000764 JMP PAT1 STORE IN BUFFER
21
22 04670 028111 INC PAT: LDA 0. C2 GET A THREE
23 04671 049215 STA 0.CURPT SET CURRENT PATTERN
24 04672 049233 STA 0.PATE SET PATTERN PER TRACK
25 04673 028246 LDA 0.INC START W ZERO
26 04674 034467 LDA 3.PRTN GET # OF WORDS
27 04675 025400 LDA 1.0.3 SAVE IT
28 04676 031401 LDA 2.1.3 GET BUFFER ADDRESS
29 04677 044463 STA 1.CNTR SET THE COUNTER
30
31 04700 041000 INC2: STA 0.0.2 STORE PATTERN
32 04701 101400 INC 0.0 INCREMENT PATTERN
33 04702 151400 INC 2.2 INCREMENT STORE POINTER
34 04703 014457 DSZ CNTR DECREMENT COUNTER
35 04704 000774 JMP INC2
36 04705 001403 JMP 3.3 RETURN
37
38 04707 028110 RANPAT: LDA 0. C1 GET A FOUR
39 04710 049215 STA 0.CURPT SET CURRENT PATTERN
40 04711 048233 STA 0.PATE SET PATTERN PER TRACK
41 04712 034451 LDA 3.PRTN GET # OF WORDS
42 04713 025400 LDA 1.0.3 SAVE IT
43 04714 031401 LDA 2.1.3 GET BUFFER ADDRESS
44 04715 044445 STA 1.CNTR SET COUNTER
45 04716 018217 LDA 0.CSEED INCREMENT CURRENT SEED
46 04717 000841 JMP 0.0.1 MANIPULATE SEED
47 04720 028217 LDA 0.CSEED GET CURRENT SEED
48
49 50 04721 105120 RAMP2: MOVZL 0.1 MANIPULATE SEED
51 04722 127120 ADDZL 1.1
52 04723 123120 ADDZL 1.0
53 04724 041000 STA 0.0.2 STORE PATTERN
54 04725 151400 INC 2.2 INCREMENT BUFFER POINTER
55 04726 014434 DSZ CNTR DECREMENT COUNTER
56 04727 000772 JMP RAMP2
57 04730 001403 JMP 3.3 RETURN
58
04731 020100  WCPAT:  LDA 0,C4 ; GET A FIVE
04732 040215  STA 0,CURPT ; SET CURRENT PATTERN
04733 020431  LDA 0,WCPT ; GET WC PATTERN
04734 000717  JMP PAT1

04735 020116  DCPAT:  LDA 0,C3 ; GET A SIX
04736 040215  STA 0,CURPT ; SET CURRENT PATTERN
04737 034424  LDA 3,PRTN ; GET POINTER
04738 021402  LDA 0,2,3 ; GET CURRENT TRACK/SECTOR
04739 04734 024110  LDA 1,C1 ; GET A ONE
04740 044233  STA 0,PAT1 ; SET PATTERN PER SECTOR SWITCH
04741 000710  JMP PAT1

04742 020114  SLPAT:  LDA 0,C7 ; GET A SEVEN
04743 040215  STA 0,CURPT ; SET CURRENT PATTERN
04744 020250  LDA 0,SELPT ; SEE IF PATTERN SELECTED
04745 101004  MOV 0,0,SRZ ;
04746 000710  JMP PAT1
04747 004765  JSR @UNIX READ THE TTY
04748 000766  JMP PAT ERROR
04749 050250  STA 2,SELPT ; SAVE THE PATTERN
04750 000672  JMP PAT1

04751 000000  CNTR 0
04752 000000  PRTN 0
04753 016142  WCPT 16142
04754 040520  SLPM .TXTE !PATTERN ? !
04755 152400  SUB 2,2 ; GET SOME CHARACTERS
04756 006220  JSR @IT4IN READ THE TTY
04757 000766  JMP PAT ERROR
04758 141000  MOV 2,0 ;
04759 000672  JMP PAT1

04760 000000  CNTR 0
04761 000000  PRTN 0
04762 016142  WCPT 16142
04763 040520  SLPM .TXTE !PATTERN ? !
ROUTINE TO COMPARE DATA PATTERN

CALLING SEQUENCE:

JSR IICOMP
DC NUMBER OF WORDS
DC OBUF WRITE BUFFER ADDRESS
DC IBUF READ BUFFER ADDRESS
DC TRACK/SECTOR CURRENT TRACK/SECTOR
DC FIRST/SECOND 0 -> FIRST READ, 1 -> SECOND READ

04773 054303 COMP: STA 3.CRTN : SAVE RETURN REGISTER
04774 020377 LDA 0.ERCS : CONSECUTIVE ERROR COUNTER
04775 040307 STA 0.ERCN : SET COUNTER
04776 020233 LDA 0.ERCN : GET THE PATTERN PER SECTOR SWITCH
04777 034303 LDA 3.CRTN : SAYE RETURN REGISTER
04778 102400 COMB: SUB 0.0 FORM A ZERO
04779 040304 STA 0.POSS : INITIALIZE POSITION
04780 101400 INC 0.0 : INCREMENT
04781 031401 LDA 2.0.3 : GET THE NUMBER OF WORDS
04782 050305 STA 2.CCNTR : SET THE COUNTER
04783 022020 CLOP: LDA 0.1120 GET A WORD FROM WRITE BUFFER
04784 026021 LDA 1.1121 GET A WORD FROM READ BUFFER
04785 131000 MOV 0.0 : SAVE
04786 010304 CONW: ISZ POSS INCREMENT POSITION
04787 014305 DSZ CCHTR OTHERWISE DECREMENT COUNTER
04788 000766 JMP CLOP GET THE NEXT WORD
I 05042 034303 LDA 3, CRTN ; GET RETURN ADDRESS
2 05043 001405 JMP 5,3 ; RETURN

5 05044 038146 CERRL: LDA 2, DERIN ; DATA ERROR PRINT INHIBIT BIT
6 05045 074477 READS 3, ; READ THE DATA SWITCHES
7 05046 173484 AND 3,2,5ZR ; MASK THE BITS
8 05047 000770 JMP CONW ; IF SET NO PRINT
9 05050 030135 LDA 2, PRINS ; SEE IF ABORT SET
10 05051 173484 AND 3,2,5ZR ;
11 05052 002214 JMP #1STRT ; YES ABORT
12 05053 014307 DSZ ERN ; DECREMENT CONSEQ. ERROR COUNT
13 05054 000462 JMP 0.2 ; PRINT ERROR
14 05055 009762 JMP CONW ; DONT PRINT ERROR
15 05056 006064 JSR #ICRLF ; CARRIAGE RETURN LINE FEED
16 05057 034303 LDA 3, CRTN ; GET POINTER
17 05060 021404 LDA 0,4,3 ; FIRST/SECOND FLAG
18 05051 024123 LDA 1,60 ; ASCII ZERO
19 05062 125408 INC 1,1 ;
20 05063 123808 ADD 1,0 ; FORM ASCII CHARACTER
21 05064 006210 JSR #ICCHAR ; PRINT THE FLAG
22 05065 006065 JSR #IMESS ; MESSAGE
23 05066 005254 CERML ;
25 05067 030021 LDA 2,21 ; GET THE BUFFER POINTER
26 05070 025000 LDA 1,6,2 ; GET WORD FORM BUFFER
27 05071 050021 STA 2,21 ; RESET INDEX
28 05072 006207 JSR #IPDCF ; PRINT THE WORD
29 05073 006665 JSR #IMESS ; MESSAGE
30 05074 005264 EXPM ;
31 05075 030020 LDA 2,20 ; WRITE BUFFER POINTER
32 05076 025000 LDA 1,6,2 ; GET WORD FROM BUFFER
33 05077 050020 STA 2,20 ; RESET INDEX
34 05100 006207 JSR #IPDCF ; PRINT THE WORD
35 05101 006065 JSR #IMESS ; MESSAGE
36 05102 005257 ADRL ;
38 38 PRINT DISC
40 05103 030123 LDA 2,60 ; GET ASCII ZERO
41 05104 034303 LDA 3, CRTN ; POINTER
42 05105 001405 LDA 0,3,3 ; TRACK/SECTOR
43 05106 024265 LDA 1,6MSK ; MASK TO DISC BITS
44 05107 123700 ANDS 1,0 ; MASK TO T/S
45 05110 101220 MOVZ 0.0 ; SHIFT BITS
46 05111 011220 MOVZ 0.0 ; SHIFT BITS
47 05112 011220 MOVZ 0.0 ; SHIFT BITS
48 05113 011220 MOVZ 0.0 ; SHIFT BITS
49 05114 143000 ADD 2.0 ; FORM ASCII
50 05115 006210 JSR #ICCHAR ; PRINT DISC NO.
51 05116 020273 LDA 0,CBLK ; A SPACE
52 05117 006210 JSR #ICCHAR ; PRINT IT
53 54 PRINT TRACK
56 05120 034303 LDA 3, CRTN ; GET PRINTER
57 05121 021403 LDA 0,3,3 ; GET THE TRACK/SECTOR
58 05122 024266 LDA 1,TMSK ; MASK TO FIRST CHARACTER
ANDS 1.0 ; MSK ADDRESSES
2 05124 101220 MOVZR 0.0 ; SHIFT
3 05125 101220 MOVZR 0.0 ; SHIFT
4 05126 101220 MOVZR 0.0 ; SHIFT
5 05127 143000 ADD 2.0 ; FORM ASCII
6 05130 006210 JSR @ICHR ; PRINT FIRST CHARACTER
7 05131 034303 LDA 3.CRTN ; RESTORE POINTER
8 05132 021403 LDA 0.3.3 ; GET TRACK/SECTOR
9 05133 024267 LDA 1.TMSK2 ; MASK TO SECOND CHARACTER
10 05134 123700 ANDS 1.0 ; MASK TO ADDRESS
11 05135 143000 ADD 2.0 ; FORM ASCII
12 05136 006210 JSR @ICHR ; PRINT SECOND CHARACTER
13 05137 034303 LDA 3.CRTN ; RESTORE POINTER
14 05138 021403 LDA 0.3.3 ; GET TRACK/SECTOR
15 05139 024270 LDA 1.TMSK3 ; GET MASK
16 05140 101220 MOVZR 0.0 ; SHIFT
17 05141 101220 MOVZR 0.0 ; SHIFT
18 05142 101220 MOVZR 0.0 ; SHIFT
19 05143 101220 MOVZR 0.0 ; SHIFT
20 05144 101220 MOVZR 0.0 ; SHIFT
21 05145 101220 MOVZR 0.0 ; SHIFT
22 05146 101220 MOVZR 0.0 ; SHIFT
23 05147 143000 ADD 2.0 ; FORM ASCII
24 05148 006210 JSR @ICHR ; PRINT THE THIRD CHARACTER
25 05151 020273 LDA 0.CBLK ; SPACE
26 05152 006210 JSR @ICHR ; PRINT IT
27 05153 034303 LDA 3.CRTN ; RESTORE POINTER
28 05154 021403 LDA 0.3.3 ; GET TRACK/SECTOR
29 05155 024271 LDA 1.TMSK1 ; MASK
30 05156 123620 ANDZR 1.0 ; MASK TRACK ADDRESS
31 05157 101220 MOVZR 0.0 ; SHIFT
32 05158 101220 MOVZR 0.0 ; SHIFT
33 05159 101220 MOVZR 0.0 ; SHIFT
34 05160 101220 MOVZR 0.0 ; SHIFT
35 05161 143000 ADD 2.0 ; FORM ASCII
36 05162 006210 JSR @ICHR ; PRINT THE CHARACTER
37 05163 034303 LDA 3.CRTN ; RESTORE POINTER
38 05164 021403 LDA 0.3.3 ; GET TRACK/SECTOR ADDRESS
39 05165 024272 LDA 1.TMSK2 ; MASK TO SECOND CHARACTER
40 05166 123300 AND 1.0 ; MASK TO ADDRESS
41 05167 143000 ADD 2.0 ; FORM ASCII
42 05168 006210 JSR @ICHR ; PRINT THE CHARACTER
43 05171 020273 LDA 0.CBLK ; SPACE
44 05172 006210 JSR @ICHR ; PRINT IT
45 05173 020304 LDA 0.POSS ; GET THE POSITION
46 05174 024274 LDA 1.PMSK1 ; MASK TO FIRST CHARACTER
47 05175 123520 ANDZL 1.0 ; MASK
48 05176 101320 MOVZL 0.0 ; SHIFT
49 05177 101320 MOVZS 0.0 ; SHIFT
50 05178 143000 ADD 2.0 ; FORM ASCII
51 05180 006210 JSR @ICHR ; PRINT THE FIRST CHARACTER
52 05181 020304 LDA 0.POSS ; GET THE POSITION
53 05182 024274 LDA 1.PMSK1 ; MASK TO FIRST CHARACTER
54 05183 123520 ANDZL 1.0 ; MASK
55 05184 101320 MOVZL 0.0 ; SHIFT
56 05185 101320 MOVZS 0.0 ; SHIFT
57 05186 143000 ADD 2.0 ; FORM ASCII
58 05188 006210 JSR @ICHR ; PRINT THE FIRST CHARACTER
59 05189 020304 LDA 0.POSS ; GET THE POSITION
LDA 1,PMSK2 : MASK TO SECOND CHARACTER
ANDZ 1.0 : MASK
MOVR 0.0 : SHIFT
MOVR 0.0 : SHIFT
ADD 2.0 : FORM ASCII
JSR #ICHAR : PRINT THE SECOND CHARACTER
LDA 0.POSS : GET THE POSITION
LDA 1,PMSK3 : MASK TO THIRD CHARACTER
ADD 1.0
ADD 2.0 : FORM ASCII
ADD 2.0 FORM ASCII
JSR #ICHAR : PRINT THE CHARACTER
LDA 0.CBLK : SPACE
JSR #ICHAR : PRINT IT

PRINT PATTERN
LDA 0.CURPT : GET CURRENT PATTERN CODE
NEG 0.0 : NEG IT
NEG 0.0 : DECREMENT PATTERN CODE
ADDZL 0.0 : MULTIPLY BY FOUR
LDA 1.IDONE : ADDRESS OF TABLE
ADD 1.0 : FORM ADDRESS OF MESSAGE
STA 0.MSAD : STORE MESSAGE POINTER
JSR #IMESS : MESSAGE
MSAD: 0

PRINT CYCLE COUNT IF TEST 4
LDA 0.MODE : GET THE CURRENT MODE
LDA 1.64 : SEE IF TEST 4
SUB 1.0.SNR : SUBTRACT 1
JSR #IPCNT : PRINT CYCLE COUNT
READS 3 : READ THE DATA SWITCHES
LDA 2.ERHLTS : HALT ON ERROR SET ?
AND 3.2.SNR :
JMP #ICONW

LDA 3.21 : GET BUFFER POINTER
STA 3.21 : RESET INDEX
LDA 3.20 : GET WRITE BUFFER POINTER
LDA 3.20 : GET WORD FOR DISPLAY
STA 3.20 : RESET INDEX
LDA 2.POSS : POSITION
LDA 3.CRTN : GET POINTER
LDA 3.24 : TRACK-SECTOR FOR DISPLAY
HALT
JMP #ICONW : CONTINUE

CERM: .TXTE 1:RD- !
ADRM: .TXTE 1:ADRS: !
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1 05260 151104
2 05261 035123
3 05262 129248
4 05263 000000
5
6 05264 153640 EXPM: .TXTE ! UT-!
7 05265 026724
8 05266 000240
9
10
11 05267 120240 ONEM: .TXTE ! RAN!
12 05270 040722
13 05271 128016
14 05272 000000
15
16 05273 120240 ZERM: .TXTE ! INC!
17 05274 047311
18 05275 128303
19 05276 000000
20
21 05277 120240 SECm: .TXTE ! SEC!
22 05300 145223
23 05301 128303
24 05302 000000
25
26 05303 120240 INCM: .TXTE ! WOR!
27 05304 147727
28 05305 128322
29 05306 000000
30
31 05307 120240 RM: .TXTE ! ONE!
32 05310 047317
33 05311 128305
34 05312 000000
35
36 05313 120240 WORM: .TXTE ! ZER!
37 05314 142532
38 05315 128322
39 05316 000000
40
41 05317 120240 SELM: .TXTE ! SEL!
42 05320 142523
43 05321 128314
44 05322 000000
45
46
47
48 05323 054446 PCNT: STA 3,PCRTN ; SAVE RETURN ADDRESS
49 05324 024242 LDA 1,T4CY ; GET THE COUNT
50 05325 005286 JSR 01PDEc ; PRINT IT
51 05326 006065 JSR 0IMESS ; MESSAGE
52 05327 005331 CYM
53 05330 002441 JMP 0PCRTN ; RETURN
54
55 05331 141640 CYM: .TXTE ! CY!
56 05332 128131
57 05333 000240
58
PCT2: STA 3.PRTN: SAVE RETURN
3 05334 054436  STA 0.P05
4 05335 044436  STA 1.P15
5 05336 054436  STA 2.P25
6 05340 006064  JSR 0.106: CARRIAGE RETURN LINE FEED
7 8 05341 020306  LDA 0.RDFLG: GET THE READ/WRITE FLAG
9 05342 181905  MOV 0.0:SNR: 0 FOR WRITE
10 05343 000040  JMP PWT2: WRITE MESSAGE
11 05344 000665  JSR 0.IMESS: MESSAGE
12 05345 004472  SRPM
13 05346 000463  JMP PCT3: CONTINUE
14 15 05347 000605  PWT2: JSR 0.IMESS: MESSAGE
16 05350 004475  SWTM
17 18 05351 020312  PCT3: LDA 0.IPRT: CONTINUE ADDRESS
19 05352 040310  STA 0.STARS: PRINT RETURN
20 05355 002318  JMP 0.ISTP: PRINT ADDRESS
21 22 05354 020215  PRT: LDA 0.CURPT: GET CURRENT PATTERN CODE
23 24 05355 100400  NEG 0.0: NEG IT
25 05356 100600  COM 0.0: DECREMENT PATTERN CODE
26 05357 103120  ADD2L 0.0: MULTIPLY BY FOUR
27 28 05360 024247  LDA 1.10NE: ADDRESS OF TABLE
29 05361 125060  ADD 1.0: FORM ADDRESS OF MESSAGE
30 05362 040402  STA 0.HSD2: STORE MESSAGE POINTER
31 05363 000665  JSR 0.IMESS: MESSAGE
32 33 05364 000000  MSAD2: 0
34 35 05365 028406  LDA 0.P05
36 37 05366 024406  LDA 1.P15
38 05367 030406  LDA 2.P25
39 05370 002402  JMP 0.PRTM: RETURN
40 41 05371 000000  PRTN: 0
42 39 05372 000000  P2RTN: 0
43 40 05373 000000  P05: 0
44 41 05374 000000  P15: 0
45 42 05375 000000  P25: 0
46 47 05376 054423  PIN: STA 3.PRTN: SAVE RETURN ADDRESS
48 05377 126400  SUB 1.1: FORM A ZERO
49 05400 044231  STA 1.INPTR: INITIALIZE TABLE POINTER
50 05401 000664  PINLP: JSR 0.106: CARRIAGE RETURN LINE FEED
51 52 05402 030135  LDA 2.PRINS: GET THE ABORT BIT
53 05403 074477  READS 3: READ THE DATA SWITCHES
54 55 05404 173405  AND 3.2.SNR: MASK SWITCHES
56 05405 002414  JMP 0.PRTN: RETURN
57 58 05406 024231  LDA 1.INPTR: GET TABLE POINTER
59 60 05407 038230  LDA 2.INTB: ADDRESS OF TABLE
61 62 05410 137000  ADD 1.2: FORM POINTER INTO TABLE
63 64 05411 025000  LDA 1.0.2: GET CURRENT MESSAGE ADDRESS
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1 05412 135085 MOV 1,3,SNR = ZERO IS END OF TABLE
2 05413 002406 JMP @PRTN = RETURN
3 05414 044482 STA 1,.+2 = STORE AS CALL
4 05415 006065 JSR @MESS = MESSAGE
5 05416 000000 0
6 05417 010231 ISZ INPTR = INCREMENT TABLE POINTER
7 05420 000671 JMP PINLP

8
9 05421 008000 PRTN: 0
10
11 05422 003111 INTR: INST1
12 05423 003131 INST2
13 05424 003141 INST3
14 05425 003152 INST4
15 05426 003165 INST5
16 05427 003175 INST6
17 05430 003210 INST7
18 05431 003225 INST8
19 05432 003253 INST9
20 05433 003274 INSTA
21 05434 003316 INSTB
22 05435 003342 INSTC
23 05436 003370 INSTD
24 05437 003406 INSTE
25 05440 003422 INSTF
26 05441 003431 INSTG
27 05442 003448 INSTH
28 05443 003465 INSTI
29 05444 003476 INSTJ
30 05445 003515 INSTK
31 05446 003535 INSTL
32 05447 003555 INSTM
33 05450 003573 INSTN
34 05451 003606 INSTO
35 05452 003624 INSTP
36 05453 003644 INSTQ
37 05454 003661 INSTR
38 05455 003673 INSTS
39 05456 003706 INSTT
40 05457 000000 0 = END OF TABLE

41
42
43
44
45
46
47 05460 014302 WLP: DSZ WCNTR = DECREMENT COUNTER
48 05461 001776 JMP -2,3 = RETURN IF NOT ZERO
49
50 05462 004817 STA 0,RSW0 = SAVE 0
51 05463 004417 STA 1,RSW1 = SAVE 1
52 05464 058417 STA 2,RSW2 = SAVE 2
53 05465 054417 STA 3,WRTN = SAVE RETURN
54 05466 074477 READS 3
55 05467 038150 LDA 2,EQCN = SEE IF PRINT INHIBITED
56 05470 173484 AND 3.2,SR
57 05471 008484 JMP WLP2 = YES
58
59
60
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1 05472 006054 JSR @ICRLF : OTHERWISE TIMEOUT OCCURRED
2 05473 006055 JSR @IMESS : MESSAGE
3 05474 004123 TMSG
4 
5 05475 024004 ULP2 LDH 0.RSUO : RESTORE 0
6 05476 024004 LDA 1.RSU1 : RESTORE 1
7 05477 030404 LDA 2.RSU2 : RESTORE 2
8 05500 002404 JMP @WRTH : RETURN
9 
10 05501 000000 RSWO : 0
11 05502 000000 RSU1 : 0
12 05503 000000 RSW2 : 0
13 05504 000000 WRTH : 0
14 
15 05505 054545 MESS : STA 3.MESSR : PRINT A TEXT MESSAGE
16 05506 010544 ISZ MESSR
17 05507 031400 LDA 2.0.3 ;C(2) POINTS TO MESSAGE
18 05510 024541 LDA 1.0.377 ;A 8 BIT MASK
19 05511 021000 LDA 0.0.0.2 ;C(2)=DATA WORD
20 05512 125112 MOVL 1.1.5ZC
21 05513 123701 ANDS 1.0.SKP
22 05514 123401 AND 1.0.SKP ;C(0)=DATA CHARACTER RIGHT
23 05515 151400 INC 2.2 ;INC TO NEXT WORD
24 05516 124800 COM 1.1 ;FLIP MASK
25 05517 004452 JSR CHAR ;PRINT
26 05520 000771 JMP MESS+4 ;JMP THE OTHER
27 05521 002531 JMP @MESSR ;LAST
28 
29 05522 029525 ZDCT : LDA 0.CH240
30 05523 101881 MOV 0.0.5KP
31 
32 05524 020123 PCT : LDA 0.680
33 05525 080433 LDA 2.OCTAB ;PRINT C(1) IN OCTAL
34 05526 000433 JMP ++3
35 05527 030441 PDEC : LDA 2.DECTB ;PRINT C(1) IN DECIMAL
36 05530 028517 STA 0.CH240 ;SUPPRESS LEADING ZEROS
37 05531 054447 STA 3.RADRET ;BOTH ENTRIES PRINT NUMBER
38 05532 040445 STA 0.ZSUPP ;THEN TAB TO NEXT POSITION
39 05533 050401 STA 2.+1
40 05534 000000 DEOCT : LDA 2.TABLE ;INSTRUCTION
41 05535 010777 JSZ ,1
42 05536 034444 LDA 1.RADRET ;SETUP 'TAB' AT END
43 05537 028503 LDA 0.CHTAB
44 05540 151005 MOV 2.2.5KW ;IF TABLE ENTRY 0
45 05541 008440 JMP CHAR ;EXIT WITH TAB
46 05542 034435 LDA 3.ZSUPP ;ZEROS SUPPRESS STUF
47 05543 102400 SUB 0.0
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1 05544 146512 DECOT: SUBL 2,1.SZC
2 05545 000405 JMP DECP
3 05546 146400 SUB 2,1 FORM THE DIGIT
4 05547 034123 LDA 3.C60
5 05548 101400 INC 0,0
6 05549 000773 JMP DECOT
7 05550 151225 DECP: MOVZR 2,2.SNR
8 05551 034123 LDA 3.C60
9 05552 054423 STA 3.ZSUPP: C(0)*DIGIT
10 05553 163000 ADD 0,0 MAKE ADCII
11 05554 004423 JSR CHAR PRINT
12 05555 000755 JMP DECOCT GET NEXT DIGIT

13 05556 030425 OCTAB: LDA 2.+1+.-DECOCT
14 05557 100000 100000
15 05558 001000 10000
16 05559 000100 100
17 05560 000010 10
18 05561 000001 1
19 05562 000000 0

20 05563 000812 .RDx 10
21 05564 001750 1000
22 05565 000144 100
23 05566 000012 10
24 05567 000001 1
25 05568 000000 0
26 05569 000812 .RDx 8
27 05570 000000 ZSUPP: 0
28 05571 000000 RADRET: 0

29 05572 054442 CHAR: STA 3.CHRET PRINT C(0) RIGHT
30 05573 001305 MOVZX 0,0.SNR RETURN +2 IF NULL
31 05574 001401 JMP 1,3
32 05575 040440 STA 0.CHSAV
33 05576 163484 AND 0,0.SZR
34 05577 000775 JMP .+3
35 05578 000000 SUBCR 3,3 COMPUTE THE PARITY
36 05579 176668 SUBCR 3,3 COMBINE PARITY WITH CHAR
37 05580 054442 CHAR1: LDA 3.CH1TAB IS THIS A TAB
38 05581 054442 SUB 0,3.SN
39 05582 054442 JMP .+3 YES
40 05583 000403 JMP .+3 NO PRINT IT
41 05584 000000 JMP @CHRET EXIT
42 05585 000775 AND 0,3.SN
43 05586 000000 JMP @CHRET SIMULATE A TAB
44 05587 000000 JMP @CHRET VIA 1 TO 8 SPACES
45 05588 000000 LDA 0.CHSAV
46 05589 163388 ADXS 3,0
47 05590 000000 LDA 0.CH1TAB
48 05591 000000 LDA 0.CH1TAB
49 05592 000000 LDA 0.CH1TAB
50 05593 000000 LDA 0.CH1TAB
51 05594 000000 LDA 0.CH1TAB
52 05595 000000 LDA 0.CH1TAB
53 05596 000000 LDA 0.CH1TAB
54 05597 000000 LDA 0.CH1TAB
55 05598 000000 LDA 0.CH1TAB
56 05599 000000 LDA 0.CH1TAB
57 05600 000000 LDA 0.CH1TAB
58 05601 000000 LDA 0.CH1TAB
59 05602 000000 LDA 0.CH1TAB
60 05603 000000 LDA 0.CH1TAB
61 05604 000000 LDA 0.CH1TAB
62 05605 000000 LDA 0.CH1TAB
63 05606 000000 LDA 0.CH1TAB
64 05607 000000 LDA 0.CH1TAB
65 05608 000000 LDA 0.CH1TAB
66 05609 000000 LDA 0.CH1TAB
67 05610 000000 LDA 0.CH1TAB
68 05611 000000 LDA 0.CH1TAB
69 05612 000000 LDA 0.CH1TAB
70 05613 000000 LDA 0.CH1TAB
71 05614 000000 LDA 0.CH1TAB
72 05615 000000 LDA 0.CH1TAB
73 05616 000000 LDA 0.CH1TAB
74 05617 000000 LDA 0.CH1TAB
75 05618 000000 LDA 0.CH1TAB
76 05619 000000 LDA 0.CH1TAB
77 05620 000000 LDA 0.CH1TAB
78 05621 000000 LDA 0.CH1TAB
79 05622 000000 LDA 0.CH1TAB
80 05623 000000 LDA 0.CH1TAB
81 05624 000000 LDA 0.CH1TAB
82 05625 000000 LDA 0.CH1TAB
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1 05626 084425 JSR TYPE
2 05627 000772 JMP -.6
3
4 05630 054420 CRLF: STA 3.CRLFR ;SAVE RETURN
5 05631 020410 LDA 0.C215
6 05632 00474F JSR CHAR :PRINT CHAPRIAGE AND LF
7 05633 020405 LDA 0.C212
8 05634 004745 JSR CHAR
9 05635 022400 SUB 0.0
10 05636 04040T STA 0.CHORZ :CLEAR MORZ POSITION
11 05637 002411 JMP @CRLFR ;EXIT
12
13 05640 080212 C212: 212
14 05641 000215 C215: 215
15 05642 000001 CHTAB: 1
16 05643 000000 CHRET: 0
17 05644 000000 CHSRV: 0
18 05645 000000 CHORZ: 0
19 05646 000007 CHARZ: 7
20 05647 000240 CH240: 240
21 05650 000000 CRLFR: 0
22 05651 000177 C377: 377
23 05652 000000 MESSR: 0
24 05653 054406 TYPE: STA 3.TYPRET;TYPE THE C(EJ)R I/F
25 05654 010771 ISZ CHORZ
26 05655 063511 SKPBZ TTO
27 05656 000777 JMP .-1
28 05657 061111 DOAS 0.TTO
29 05658 002401 JMP @TYPRET
30 05659 000000 TYPRET: 0
31 .END
<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>VALUE</th>
<th>DEFINED REFERENCES</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD</td>
<td>002454</td>
<td>31:57 32:01</td>
</tr>
<tr>
<td>ADRM</td>
<td>005257</td>
<td>61:58 59:36</td>
</tr>
<tr>
<td>ALP1</td>
<td>004644</td>
<td>55:57 55:54</td>
</tr>
<tr>
<td>ALP2</td>
<td>004635</td>
<td>55:50 55:40</td>
</tr>
<tr>
<td>BAC</td>
<td>005811</td>
<td>58:32 58:26</td>
</tr>
<tr>
<td>CB210</td>
<td>000075</td>
<td>3:47 12:04</td>
</tr>
<tr>
<td>CB421</td>
<td>000076</td>
<td>3:48 12:15</td>
</tr>
<tr>
<td>C0600</td>
<td>000125</td>
<td>4:13 49:13</td>
</tr>
<tr>
<td>C10</td>
<td>000084</td>
<td>3:54 14:25</td>
</tr>
<tr>
<td>C100</td>
<td>000133</td>
<td>4:19</td>
</tr>
<tr>
<td>C1042</td>
<td>000077</td>
<td>3:49 12:26</td>
</tr>
<tr>
<td>C12</td>
<td>000060</td>
<td>3:31</td>
</tr>
<tr>
<td>C140X</td>
<td>000101</td>
<td>3:51 14:13 14:22</td>
</tr>
<tr>
<td>C144</td>
<td>000057</td>
<td>3:30</td>
</tr>
<tr>
<td>C16</td>
<td>001325</td>
<td>17:32</td>
</tr>
<tr>
<td>C1600</td>
<td>000124</td>
<td>4:12 49:11</td>
</tr>
<tr>
<td>C177</td>
<td>000132</td>
<td>4:10 49:41</td>
</tr>
<tr>
<td>C1777</td>
<td>000127</td>
<td>4:15 49:22</td>
</tr>
<tr>
<td>C20</td>
<td>000120</td>
<td>4:08 13:54 14:07 38:47 38:49 35:07 49:01</td>
</tr>
<tr>
<td>C200</td>
<td>000102</td>
<td>3:52 14:37</td>
</tr>
<tr>
<td>C2000</td>
<td>000107</td>
<td>3:57 49:47</td>
</tr>
<tr>
<td>C212</td>
<td>005640</td>
<td>67:13 67:07</td>
</tr>
<tr>
<td>C215</td>
<td>005641</td>
<td>67:14 67:05</td>
</tr>
<tr>
<td>C3</td>
<td>000116</td>
<td>4:06 20:13 57:06</td>
</tr>
<tr>
<td>C377</td>
<td>005651</td>
<td>67:22 65:29</td>
</tr>
<tr>
<td>C40K</td>
<td>000073</td>
<td>3:45</td>
</tr>
<tr>
<td>C44</td>
<td>000131</td>
<td>4:17</td>
</tr>
<tr>
<td>C5</td>
<td>000112</td>
<td>4:02 38:11 48:06 56:04</td>
</tr>
<tr>
<td>C54</td>
<td>000103</td>
<td>3:53</td>
</tr>
<tr>
<td>C55</td>
<td>000314</td>
<td>6:23 8:01</td>
</tr>
<tr>
<td>C6</td>
<td>000113</td>
<td>4:03 55:55 56:17</td>
</tr>
<tr>
<td>C7</td>
<td>000114</td>
<td>4:04 57:14</td>
</tr>
<tr>
<td>C70</td>
<td>000121</td>
<td>4:09 49:50 49:54</td>
</tr>
<tr>
<td>C7367</td>
<td>000130</td>
<td>4:16</td>
</tr>
<tr>
<td>C77</td>
<td>000126</td>
<td>4:14 49:17</td>
</tr>
<tr>
<td>C77K</td>
<td>000117</td>
<td>4:07 13:49 14:02</td>
</tr>
<tr>
<td>CCNTN</td>
<td>000305</td>
<td>6:16 58:46 58:57</td>
</tr>
<tr>
<td>CERM</td>
<td>005254</td>
<td>61:54 59:23</td>
</tr>
<tr>
<td>CERR</td>
<td>005044</td>
<td>59:05 58:53</td>
</tr>
<tr>
<td>CH240</td>
<td>005647</td>
<td>67:20 65:40 65:47 66:50</td>
</tr>
<tr>
<td>CHAH</td>
<td>000072</td>
<td>3:44 3:16</td>
</tr>
<tr>
<td>CHAR</td>
<td>005614</td>
<td>66:48</td>
</tr>
<tr>
<td>CHAR1</td>
<td>005614</td>
<td>66:48</td>
</tr>
<tr>
<td>CHAR2</td>
<td>005646</td>
<td>67:19 66:55</td>
</tr>
<tr>
<td>CHBACK</td>
<td>005645</td>
<td>67:18 66:54 67:10 67:25</td>
</tr>
<tr>
<td>CHFET</td>
<td>005643</td>
<td>67:16 66:36 66:52 66:57</td>
</tr>
<tr>
<td>CHSHA3</td>
<td>005644</td>
<td>67:17 66:39 66:45</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED REFERENCES</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>-------------------</td>
</tr>
<tr>
<td>CHAB</td>
<td>005442</td>
<td>67:15 65:54 66:48</td>
</tr>
<tr>
<td>CLOP</td>
<td>00627</td>
<td>58:48 58:58</td>
</tr>
<tr>
<td>CMP</td>
<td>00132</td>
<td>41:10 49:52 49:56</td>
</tr>
<tr>
<td>CNTR</td>
<td>00194</td>
<td>13:18 18:22</td>
</tr>
<tr>
<td>CO04</td>
<td>00024</td>
<td>31:46 11:51</td>
</tr>
<tr>
<td>COMH</td>
<td>00504</td>
<td>58:36 58:21</td>
</tr>
<tr>
<td>COMP</td>
<td>00477</td>
<td>58:16 51:15</td>
</tr>
<tr>
<td>CROM</td>
<td>00557</td>
<td>50:56 54:42 59:08 59:14</td>
</tr>
<tr>
<td>CRLF</td>
<td>00520</td>
<td>67:04 3:36</td>
</tr>
<tr>
<td>CRTP</td>
<td>00559</td>
<td>67:21 67:04 67:11</td>
</tr>
<tr>
<td>CSRD</td>
<td>00425</td>
<td>28:31 27:20</td>
</tr>
<tr>
<td>CSRD2</td>
<td>00723</td>
<td>29:41 29:34</td>
</tr>
<tr>
<td>CURSE</td>
<td>00021</td>
<td>5:06</td>
</tr>
<tr>
<td>CYCLE</td>
<td>00451</td>
<td>53:44 3:48</td>
</tr>
<tr>
<td>CYM</td>
<td>00531</td>
<td>62:55 62:52</td>
</tr>
<tr>
<td>DAREP</td>
<td>00016</td>
<td>4:46</td>
</tr>
<tr>
<td>DALAT</td>
<td>00016</td>
<td>4:48</td>
</tr>
<tr>
<td>DECD</td>
<td>00421</td>
<td>40:42 3:30 48:54 49:06</td>
</tr>
<tr>
<td>DECH</td>
<td>00554</td>
<td>66:01 66:06</td>
</tr>
<tr>
<td>DECP</td>
<td>00552</td>
<td>66:07 66:02</td>
</tr>
<tr>
<td>DECR</td>
<td>00570</td>
<td>66:23 65:46</td>
</tr>
<tr>
<td>DERIN</td>
<td>00040</td>
<td>4:33 54:13 59:05</td>
</tr>
<tr>
<td>DEVI1</td>
<td>00427</td>
<td>49:20 49:15 49:20</td>
</tr>
<tr>
<td>DEVCD</td>
<td>00425</td>
<td>49:09 49:31</td>
</tr>
<tr>
<td>DEVIE</td>
<td>00025</td>
<td>3:20 49:07 49:24</td>
</tr>
<tr>
<td>DEVHU</td>
<td>00371</td>
<td>45:39 48:46</td>
</tr>
<tr>
<td>DIAH</td>
<td>00003</td>
<td>0:00 0:00 3:10</td>
</tr>
<tr>
<td>DMBT</td>
<td>00034</td>
<td>5:23 17:46 18:00</td>
</tr>
<tr>
<td>DMSK</td>
<td>00035</td>
<td>5:50 51:51 59:43</td>
</tr>
<tr>
<td>DPALL</td>
<td>00017</td>
<td>4:40 18:46 20:03 35:22 55:29</td>
</tr>
<tr>
<td>DPAT1</td>
<td>00052</td>
<td>4:37</td>
</tr>
<tr>
<td>DPAT2</td>
<td>00053</td>
<td>4:38</td>
</tr>
<tr>
<td>DPC1</td>
<td>00115</td>
<td>4:37</td>
</tr>
<tr>
<td>DPC2</td>
<td>00154</td>
<td>4:39</td>
</tr>
<tr>
<td>DRET</td>
<td>00054</td>
<td>3:27 48:42 49:32</td>
</tr>
<tr>
<td>DSC0</td>
<td>00157</td>
<td>21:37 5:46</td>
</tr>
<tr>
<td>DSC1</td>
<td>00160</td>
<td>21:38</td>
</tr>
<tr>
<td>DSC2</td>
<td>00161</td>
<td>21:39</td>
</tr>
<tr>
<td>DSC3</td>
<td>00162</td>
<td>21:40 21:10 23:08</td>
</tr>
<tr>
<td>DSFAL</td>
<td>00018</td>
<td>4:50 20:39 22:46</td>
</tr>
<tr>
<td>DSINC</td>
<td>00163</td>
<td>21:42</td>
</tr>
<tr>
<td>DSK5</td>
<td>00256</td>
<td>33:16 33:13 33:16 33:30 35:40 35:48</td>
</tr>
<tr>
<td>DSK6</td>
<td>00252</td>
<td>5:47 33:11 33:13 35:41 35:49</td>
</tr>
<tr>
<td>DSKM</td>
<td>00169</td>
<td>21:44 22:10 24:06</td>
</tr>
<tr>
<td>DSKM</td>
<td>00169</td>
<td>21:44 22:10 24:06</td>
</tr>
<tr>
<td>DSKM</td>
<td>00169</td>
<td>21:44 22:10 24:06</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE DEFINED REFERENCES</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>--------------------------</td>
<td></td>
</tr>
<tr>
<td>ECODE</td>
<td>003007 36:28 3:34</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9:53 10:18 10:30 10:43</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:27 15:45</td>
<td></td>
</tr>
<tr>
<td>ENTER</td>
<td>004500 53:17 3:39</td>
<td></td>
</tr>
<tr>
<td>EOC2</td>
<td>004135 47:42</td>
<td></td>
</tr>
<tr>
<td></td>
<td>64:55</td>
<td></td>
</tr>
<tr>
<td>EPMS</td>
<td>004164 48:11 48:20</td>
<td></td>
</tr>
<tr>
<td>EPRI</td>
<td>004572 54:22 54:15</td>
<td></td>
</tr>
<tr>
<td>EPSM</td>
<td>00414 47:22</td>
<td></td>
</tr>
<tr>
<td>ER</td>
<td>000071 3:41 3:42</td>
<td></td>
</tr>
<tr>
<td>ERC5</td>
<td>000377 6:29 58:17 58:26</td>
<td></td>
</tr>
<tr>
<td>ERCH</td>
<td>000307 6:18 58:18 58:27 59:12</td>
<td></td>
</tr>
<tr>
<td>ERH</td>
<td>004551 54:03 54:20</td>
<td></td>
</tr>
<tr>
<td>ERHL</td>
<td>000136 4:25 54:17 61:37</td>
<td></td>
</tr>
<tr>
<td>ERHRT</td>
<td>004554 54:06 54:34</td>
<td></td>
</tr>
<tr>
<td>ERNO</td>
<td>000165 4:52 7:17 8:06 9:03 53:27 54:26</td>
<td></td>
</tr>
<tr>
<td>ERR</td>
<td>004544 53:56 3:41</td>
<td></td>
</tr>
<tr>
<td>ERR1</td>
<td>004557 54:10 54:02</td>
<td></td>
</tr>
<tr>
<td>ERR3</td>
<td>004601 54:30 54:19</td>
<td></td>
</tr>
<tr>
<td>ERRCT</td>
<td>004523 53:37 53:38 54:86</td>
<td></td>
</tr>
<tr>
<td>ERROR</td>
<td>000157 4:45 26:54 26:54 31:39 33:05</td>
<td></td>
</tr>
<tr>
<td>ESCP</td>
<td>003020 36:39 27:43 34:22</td>
<td></td>
</tr>
<tr>
<td>ESUIT</td>
<td>004522 53:36 53:29 54:11 54:25 54:28</td>
<td></td>
</tr>
<tr>
<td>EXPM</td>
<td>005264 62:06 59:30</td>
<td></td>
</tr>
<tr>
<td>FIRST</td>
<td>000062 3:33 49:09</td>
<td></td>
</tr>
<tr>
<td>HERE</td>
<td>004606 54:36 54:25</td>
<td></td>
</tr>
<tr>
<td>HISSC</td>
<td>000176 5:03 30:36 30:52</td>
<td></td>
</tr>
<tr>
<td>HSSEC</td>
<td>000227 5:20 30:37 32:25 33:46 34:55</td>
<td></td>
</tr>
<tr>
<td>ICOMP</td>
<td>000212 5:15 10:23 27:10 35:12</td>
<td></td>
</tr>
<tr>
<td>ICONU</td>
<td>000245 5:42 61:39 61:51</td>
<td></td>
</tr>
<tr>
<td>ICRLF</td>
<td>000064 3:36 7:07 7:12 7:42 7:53 15:56 17:20 18:54</td>
<td></td>
</tr>
<tr>
<td></td>
<td>34:41 34:57 35:37 48:44 51:15 54:23 57:19</td>
<td></td>
</tr>
<tr>
<td></td>
<td>59:15 63:16 65:50 65:81</td>
<td></td>
</tr>
<tr>
<td>IDPAT</td>
<td>004735 57:06 55:43</td>
<td></td>
</tr>
<tr>
<td>IDSCB</td>
<td>000251 5:46 21:06 22:57 23:13</td>
<td></td>
</tr>
<tr>
<td>IDEIA</td>
<td>000262 5:07</td>
<td></td>
</tr>
<tr>
<td>IEOC2</td>
<td>000225 5:26 7:29</td>
<td></td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED REFERENCES</td>
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<td>--------</td>
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</tr>
<tr>
<td>I U100</td>
<td>00024</td>
<td>32:54</td>
</tr>
<tr>
<td>I U101</td>
<td>00028</td>
<td>5:25 47:148</td>
</tr>
<tr>
<td>I M2</td>
<td>00025</td>
<td>5:29 63:56</td>
</tr>
<tr>
<td>I N3</td>
<td>00026</td>
<td>5:51 23:17</td>
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<tr>
<td>I N3E</td>
<td>00026</td>
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<tr>
<td>I N4</td>
<td>00025</td>
<td>5:48 26:55</td>
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<tr>
<td>I N5</td>
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<td>5:34 30:42</td>
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<td>I N6</td>
<td>00026</td>
<td>5:55 30:16 35:54 35:57 36:09</td>
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<tr>
<td>I N6A</td>
<td>00024</td>
<td>5:49 30:32</td>
</tr>
<tr>
<td>I N6B</td>
<td>00026</td>
<td>5:57 30:53</td>
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<tr>
<td>I N6C</td>
<td>00025</td>
<td>5:58 32:12 32:24</td>
</tr>
<tr>
<td>I N6D</td>
<td>00026</td>
<td>6:11 36:10</td>
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<tr>
<td>I N6E</td>
<td>00027</td>
<td>6:18</td>
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<tr>
<td>I N6F</td>
<td>00026</td>
<td>5:16 32:29</td>
</tr>
<tr>
<td>I M20</td>
<td>00028</td>
<td>7:37 36:25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>34:21 34:34 34:42 34:58 35:31 40:45 51:16 51:23</td>
</tr>
<tr>
<td>IMOE</td>
<td>00416</td>
<td>47:52 5:25</td>
</tr>
<tr>
<td>IMOH</td>
<td>00041</td>
<td>5:38 35:39 35:50</td>
</tr>
<tr>
<td>IMGZ</td>
<td>00478</td>
<td>56:31 56:35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>36:20 56:125 56:36</td>
</tr>
<tr>
<td>IHCH</td>
<td>00538</td>
<td>62:26</td>
</tr>
<tr>
<td>IHCP</td>
<td>00467</td>
<td>56:22 55:42</td>
</tr>
<tr>
<td>INPT</td>
<td>00031</td>
<td>5:30 63:49 63:55 64:06</td>
</tr>
<tr>
<td>INST</td>
<td>00512</td>
<td>37:53 64:11</td>
</tr>
<tr>
<td>INST2</td>
<td>00513</td>
<td>38:04 64:12</td>
</tr>
<tr>
<td>INST3</td>
<td>00514</td>
<td>38:13 64:13</td>
</tr>
<tr>
<td>INST4</td>
<td>00515</td>
<td>38:23 64:14</td>
</tr>
<tr>
<td>INST5</td>
<td>00516</td>
<td>38:35 64:15</td>
</tr>
<tr>
<td>INST6</td>
<td>00517</td>
<td>38:44 64:16</td>
</tr>
<tr>
<td>INST7</td>
<td>00518</td>
<td>38:56 64:17</td>
</tr>
<tr>
<td>INST8</td>
<td>00520</td>
<td>39:12 64:18</td>
</tr>
<tr>
<td>INST9</td>
<td>00525</td>
<td>39:35 64:19</td>
</tr>
<tr>
<td>INSTG</td>
<td>00424</td>
<td>39:53 64:20</td>
</tr>
<tr>
<td>INSTR</td>
<td>00116</td>
<td>40:14 64:21</td>
</tr>
<tr>
<td>INSTD</td>
<td>00316</td>
<td>40:14 64:22</td>
</tr>
<tr>
<td>INTE</td>
<td>00342</td>
<td>40:14 64:23</td>
</tr>
<tr>
<td>INTEQ</td>
<td>00370</td>
<td>40:58 64:23</td>
</tr>
<tr>
<td>INTEZ</td>
<td>00376</td>
<td>41:15 64:24</td>
</tr>
<tr>
<td>INTEI</td>
<td>00422</td>
<td>41:28 64:25</td>
</tr>
<tr>
<td>INTEJ</td>
<td>00471</td>
<td>41:36 64:26</td>
</tr>
<tr>
<td>INTEK</td>
<td>00540</td>
<td>41:44 64:27</td>
</tr>
<tr>
<td>INTEH</td>
<td>00545</td>
<td>42:01 64:28</td>
</tr>
<tr>
<td>INTEL</td>
<td>00546</td>
<td>42:18 64:29</td>
</tr>
<tr>
<td>INTEM</td>
<td>00547</td>
<td>42:34 64:30</td>
</tr>
<tr>
<td>INTEM</td>
<td>00548</td>
<td>42:51 64:31</td>
</tr>
<tr>
<td>INTEO</td>
<td>00555</td>
<td>43:10 64:32</td>
</tr>
<tr>
<td>INTEQ</td>
<td>00556</td>
<td>43:25 64:33</td>
</tr>
<tr>
<td>INTEH</td>
<td>00560</td>
<td>43:37 64:34</td>
</tr>
<tr>
<td>INTEJ</td>
<td>00564</td>
<td>43:52 64:35</td>
</tr>
<tr>
<td>INTEI</td>
<td>00569</td>
<td>44:11 64:36</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED REFERENCES</td>
</tr>
<tr>
<td>--------</td>
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<td>---------------------</td>
</tr>
<tr>
<td>M2C</td>
<td>001413</td>
<td>19:14</td>
</tr>
<tr>
<td>M2C2</td>
<td>001451</td>
<td>19:09</td>
</tr>
<tr>
<td>M2CRD</td>
<td>001444</td>
<td>18:33</td>
</tr>
<tr>
<td>M2EXT</td>
<td>001439</td>
<td>19:23</td>
</tr>
<tr>
<td>M2OUT</td>
<td>001436</td>
<td>18:52</td>
</tr>
<tr>
<td>M2RD</td>
<td>001354</td>
<td>19:11</td>
</tr>
<tr>
<td>M3B</td>
<td>001502</td>
<td>21:29</td>
</tr>
<tr>
<td>M3C</td>
<td>001650</td>
<td>22:09</td>
</tr>
<tr>
<td>M3E</td>
<td>001750</td>
<td>21:58</td>
</tr>
<tr>
<td>M3G</td>
<td>001568</td>
<td>23:12</td>
</tr>
<tr>
<td>M3H</td>
<td>001717</td>
<td>28:43</td>
</tr>
<tr>
<td>M3I</td>
<td>001662</td>
<td>23:06</td>
</tr>
<tr>
<td>M3INC</td>
<td>001575</td>
<td>22:02</td>
</tr>
<tr>
<td>M3J</td>
<td>001767</td>
<td>22:52</td>
</tr>
<tr>
<td>M3K</td>
<td>001642</td>
<td>22:17</td>
</tr>
<tr>
<td>M3L</td>
<td>001739</td>
<td>23:27</td>
</tr>
<tr>
<td>M3M</td>
<td>001762</td>
<td>24:07</td>
</tr>
<tr>
<td>M3N</td>
<td>001623</td>
<td>21:14</td>
</tr>
<tr>
<td>M3D</td>
<td>001526</td>
<td>20:41</td>
</tr>
<tr>
<td>M3OUT</td>
<td>001579</td>
<td>20:19</td>
</tr>
<tr>
<td>M3P</td>
<td>001543</td>
<td>21:02</td>
</tr>
<tr>
<td>M4B</td>
<td>002833</td>
<td>25:17</td>
</tr>
<tr>
<td>M4CTS</td>
<td>002855</td>
<td>25:46</td>
</tr>
<tr>
<td>M4EXT</td>
<td>002237</td>
<td>25:31</td>
</tr>
<tr>
<td>M4H</td>
<td>002211</td>
<td>27:46</td>
</tr>
<tr>
<td>M4N</td>
<td>002212</td>
<td>26:21</td>
</tr>
<tr>
<td>M4X</td>
<td>002173</td>
<td>28:45</td>
</tr>
<tr>
<td>M4P</td>
<td>002226</td>
<td>29:04</td>
</tr>
<tr>
<td>M4UT</td>
<td>002298</td>
<td>28:16</td>
</tr>
<tr>
<td>M4RLP</td>
<td>002131</td>
<td>28:06</td>
</tr>
<tr>
<td>M4ULP</td>
<td>002957</td>
<td>26:25</td>
</tr>
<tr>
<td>M52</td>
<td>002557</td>
<td>5:55</td>
</tr>
<tr>
<td>M5A</td>
<td>002315</td>
<td>30:50</td>
</tr>
<tr>
<td>M5A0</td>
<td>002553</td>
<td>30:52</td>
</tr>
<tr>
<td>M5AC</td>
<td>002364</td>
<td>30:09</td>
</tr>
<tr>
<td>M5D</td>
<td>002745</td>
<td>3:57</td>
</tr>
<tr>
<td>M5B</td>
<td>002341</td>
<td>30:23</td>
</tr>
<tr>
<td>M5CPP</td>
<td>002747</td>
<td>5:50</td>
</tr>
<tr>
<td>M5CT</td>
<td>002483</td>
<td>30:43</td>
</tr>
<tr>
<td>M5CTS</td>
<td>002747</td>
<td>34:46</td>
</tr>
<tr>
<td>M5EXT</td>
<td>002726</td>
<td>36:18</td>
</tr>
<tr>
<td>M5K</td>
<td>002654</td>
<td>34:38</td>
</tr>
<tr>
<td>M5L</td>
<td>002471</td>
<td>34:51</td>
</tr>
<tr>
<td>M5M</td>
<td>002616</td>
<td>34:54</td>
</tr>
<tr>
<td>M5N</td>
<td>002663</td>
<td>34:46</td>
</tr>
<tr>
<td>M5D</td>
<td>002648</td>
<td>34:25</td>
</tr>
<tr>
<td>M5P</td>
<td>002676</td>
<td>34:49</td>
</tr>
<tr>
<td>M5Q</td>
<td>002575</td>
<td>6:11</td>
</tr>
<tr>
<td>M5R</td>
<td>002621</td>
<td>34:81</td>
</tr>
<tr>
<td>M5RLP</td>
<td>002627</td>
<td>33:53</td>
</tr>
<tr>
<td>M5S</td>
<td>002753</td>
<td>33:34</td>
</tr>
<tr>
<td>M5T</td>
<td>002764</td>
<td>35:56</td>
</tr>
<tr>
<td>M5U</td>
<td>002653</td>
<td>34:20</td>
</tr>
<tr>
<td>M5V</td>
<td>002630</td>
<td>36:04</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>INSTR</td>
<td>003661</td>
<td>44:25</td>
</tr>
<tr>
<td>INSTR5</td>
<td>003673</td>
<td>44:36</td>
</tr>
<tr>
<td>INSTR6</td>
<td>003706</td>
<td>44:40</td>
</tr>
<tr>
<td>INTRA</td>
<td>005422</td>
<td>64:11</td>
</tr>
<tr>
<td>IOBUF</td>
<td>006167</td>
<td>45:12</td>
</tr>
<tr>
<td>IXE</td>
<td>006247</td>
<td>51:44</td>
</tr>
<tr>
<td>IPECS</td>
<td>007735</td>
<td>45:17</td>
</tr>
<tr>
<td>IPCH1</td>
<td>008243</td>
<td>51:48</td>
</tr>
<tr>
<td>IPCT1</td>
<td>008244</td>
<td>51:41</td>
</tr>
<tr>
<td>IPDCT</td>
<td>008266</td>
<td>51:11</td>
</tr>
<tr>
<td>IOBUF</td>
<td>002322</td>
<td>51:31</td>
</tr>
<tr>
<td>IPDCT</td>
<td>002307</td>
<td>51:12</td>
</tr>
<tr>
<td>IPRT</td>
<td>003112</td>
<td>51:24</td>
</tr>
<tr>
<td>ITPB</td>
<td>002223</td>
<td>51:24</td>
</tr>
<tr>
<td>ITPH1</td>
<td>002213</td>
<td>51:16</td>
</tr>
<tr>
<td>ISTEP</td>
<td>002033</td>
<td>51:09</td>
</tr>
<tr>
<td>ISTP</td>
<td>003111</td>
<td>61:20</td>
</tr>
<tr>
<td>IST1</td>
<td>006141</td>
<td>51:17</td>
</tr>
<tr>
<td>IT4IN</td>
<td>006220</td>
<td>51:21</td>
</tr>
<tr>
<td>ITR</td>
<td>004520</td>
<td>53:34</td>
</tr>
<tr>
<td>ITRCT</td>
<td>004521</td>
<td>53:35</td>
</tr>
<tr>
<td>ITRIPB</td>
<td>002221</td>
<td>51:22</td>
</tr>
<tr>
<td>ITRIPH</td>
<td>003111</td>
<td>51:14</td>
</tr>
<tr>
<td>LILP</td>
<td>003801</td>
<td>61:12</td>
</tr>
<tr>
<td>LAST</td>
<td>000663</td>
<td>3:14</td>
</tr>
<tr>
<td>LASTV</td>
<td>003793</td>
<td>45:18</td>
</tr>
<tr>
<td>LOADR</td>
<td>000552</td>
<td>3:25</td>
</tr>
<tr>
<td>LOOP</td>
<td>006678</td>
<td>3:48</td>
</tr>
<tr>
<td>LOOPR</td>
<td>004520</td>
<td>53:42</td>
</tr>
<tr>
<td>LOWE</td>
<td>000172</td>
<td>4:17</td>
</tr>
<tr>
<td>LOWSS</td>
<td>000175</td>
<td>5:02</td>
</tr>
<tr>
<td>LPEPS</td>
<td>000137</td>
<td>4:26</td>
</tr>
<tr>
<td>LPTST</td>
<td>000148</td>
<td>4:27</td>
</tr>
<tr>
<td>LSEC</td>
<td>000226</td>
<td>5:27</td>
</tr>
<tr>
<td>ML</td>
<td>000134</td>
<td>4:28</td>
</tr>
<tr>
<td>ML2</td>
<td>000165</td>
<td>3:15</td>
</tr>
<tr>
<td>ML6</td>
<td>000166</td>
<td>3:56</td>
</tr>
<tr>
<td>ML10</td>
<td>000446</td>
<td>7:53</td>
</tr>
<tr>
<td>ML11</td>
<td>000444</td>
<td>7:48</td>
</tr>
<tr>
<td>ML25</td>
<td>000115</td>
<td>4:05</td>
</tr>
<tr>
<td>ML27</td>
<td>000148</td>
<td>4:27</td>
</tr>
<tr>
<td>ML32</td>
<td>000132</td>
<td>4:28</td>
</tr>
<tr>
<td>ML22</td>
<td>000164</td>
<td>4:125</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>MSUA</td>
<td>002404</td>
<td>31:12</td>
</tr>
<tr>
<td>MSULP</td>
<td>002420</td>
<td>31:25</td>
</tr>
<tr>
<td>MSY</td>
<td>003800</td>
<td>36:19</td>
</tr>
<tr>
<td>MSZ</td>
<td>002702</td>
<td>34:57</td>
</tr>
<tr>
<td>M6A</td>
<td>004201</td>
<td>48:26</td>
</tr>
<tr>
<td>M6B</td>
<td>004204</td>
<td>48:30</td>
</tr>
<tr>
<td>M7A</td>
<td>004214</td>
<td>48:39</td>
</tr>
<tr>
<td>MESS</td>
<td>005505</td>
<td>65:26</td>
</tr>
<tr>
<td>MESR</td>
<td>005652</td>
<td>67:23</td>
</tr>
<tr>
<td>MOD1M</td>
<td>004006</td>
<td>46:04</td>
</tr>
<tr>
<td>MOD1S</td>
<td>000141</td>
<td>4:28</td>
</tr>
<tr>
<td>MOD2B</td>
<td>001330</td>
<td>17:36</td>
</tr>
<tr>
<td>MOD2H</td>
<td>004823</td>
<td>46:18</td>
</tr>
<tr>
<td>MOD2S</td>
<td>000142</td>
<td>4:29</td>
</tr>
<tr>
<td>MOD3B</td>
<td>001617</td>
<td>21:55</td>
</tr>
<tr>
<td>MOD3C</td>
<td>001500</td>
<td>28:27</td>
</tr>
<tr>
<td>MOD3D</td>
<td>001731</td>
<td>23:28</td>
</tr>
<tr>
<td>MOD3H</td>
<td>004042</td>
<td>46:34</td>
</tr>
<tr>
<td>MOD3S</td>
<td>000143</td>
<td>4:30</td>
</tr>
<tr>
<td>MOD4A</td>
<td>002044</td>
<td>25:32</td>
</tr>
<tr>
<td>MOD4B</td>
<td>002052</td>
<td>25:41</td>
</tr>
<tr>
<td>MOD4H</td>
<td>002227</td>
<td>26:02</td>
</tr>
<tr>
<td>MOD4M</td>
<td>004052</td>
<td>46:43</td>
</tr>
<tr>
<td>MOD4R</td>
<td>002124</td>
<td>26:35</td>
</tr>
<tr>
<td>MOD4U</td>
<td>002230</td>
<td>28:04</td>
</tr>
<tr>
<td>MOD5A</td>
<td>003544</td>
<td>38:49</td>
</tr>
<tr>
<td>MOD5B</td>
<td>002371</td>
<td>38:55</td>
</tr>
<tr>
<td>MOD5S</td>
<td>002720</td>
<td>35:16</td>
</tr>
<tr>
<td>MOD5L</td>
<td>002631</td>
<td>34:12</td>
</tr>
<tr>
<td>MOD5M</td>
<td>004666</td>
<td>46:56</td>
</tr>
<tr>
<td>MOD5R</td>
<td>002510</td>
<td>32:33</td>
</tr>
<tr>
<td>MOD5U</td>
<td>002721</td>
<td>35:18</td>
</tr>
<tr>
<td>MODH</td>
<td>002461</td>
<td>31:00</td>
</tr>
<tr>
<td>MOD8L</td>
<td>000156</td>
<td>4:41</td>
</tr>
<tr>
<td>MODE0</td>
<td>004156</td>
<td>48:04</td>
</tr>
<tr>
<td>MODE1</td>
<td>000430</td>
<td>7:37</td>
</tr>
<tr>
<td>MODE2</td>
<td>001303</td>
<td>17:13</td>
</tr>
<tr>
<td>MODE3</td>
<td>001471</td>
<td>28:13</td>
</tr>
<tr>
<td>MODE4</td>
<td>002014</td>
<td>25:06</td>
</tr>
<tr>
<td>MODE5</td>
<td>002321</td>
<td>38:11</td>
</tr>
<tr>
<td>MODE6</td>
<td>004167</td>
<td>48:15</td>
</tr>
<tr>
<td>MODE7</td>
<td>004286</td>
<td>48:33</td>
</tr>
<tr>
<td>MSDAD</td>
<td>005230</td>
<td>61:27</td>
</tr>
<tr>
<td>MSDAD2</td>
<td>005364</td>
<td>63:32</td>
</tr>
<tr>
<td>MSAX</td>
<td>000056</td>
<td>3:29</td>
</tr>
<tr>
<td>MXSEC</td>
<td>000174</td>
<td>5:01</td>
</tr>
<tr>
<td>MODMM</td>
<td>001611</td>
<td>21:48</td>
</tr>
<tr>
<td>NSD1S</td>
<td>000161</td>
<td>4:47</td>
</tr>
<tr>
<td>NSSC</td>
<td>000177</td>
<td>5:04</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>HSSCM</td>
<td>003052</td>
<td>37:10</td>
</tr>
<tr>
<td>HUC</td>
<td>005010</td>
<td>58:31</td>
</tr>
<tr>
<td>OCTAB</td>
<td>005560</td>
<td>66:14</td>
</tr>
<tr>
<td>DNEA</td>
<td>005267</td>
<td>62:11</td>
</tr>
<tr>
<td>OMEPA</td>
<td>004650</td>
<td>56:04</td>
</tr>
<tr>
<td>POS</td>
<td>005373</td>
<td>63:48</td>
</tr>
<tr>
<td>P15</td>
<td>005374</td>
<td>63:41</td>
</tr>
<tr>
<td>P2H</td>
<td>004544</td>
<td>19:16</td>
</tr>
<tr>
<td>P2HX</td>
<td>004162</td>
<td>19:22</td>
</tr>
<tr>
<td>P2TH</td>
<td>005372</td>
<td>63:39</td>
</tr>
<tr>
<td>P2S</td>
<td>005376</td>
<td>63:42</td>
</tr>
<tr>
<td>P4X</td>
<td>002275</td>
<td>20:47</td>
</tr>
<tr>
<td>PSH</td>
<td>002771</td>
<td>36:12</td>
</tr>
<tr>
<td>PWS</td>
<td>000050</td>
<td>3:23</td>
</tr>
<tr>
<td>PAT1</td>
<td>004653</td>
<td>56:07</td>
</tr>
<tr>
<td>PAT2</td>
<td>004657</td>
<td>56:11</td>
</tr>
<tr>
<td>PAT4</td>
<td>004620</td>
<td>55:31</td>
</tr>
<tr>
<td>PATBL</td>
<td>004625</td>
<td>55:40</td>
</tr>
<tr>
<td>PATRN</td>
<td>004611</td>
<td>55:23</td>
</tr>
<tr>
<td>PCHNT</td>
<td>005328</td>
<td>62:48</td>
</tr>
<tr>
<td>PCHRN</td>
<td>005371</td>
<td>63:10</td>
</tr>
<tr>
<td>PCT2</td>
<td>005334</td>
<td>63:12</td>
</tr>
<tr>
<td>PCT3</td>
<td>005251</td>
<td>63:18</td>
</tr>
<tr>
<td>PCCUR</td>
<td>004623</td>
<td>55:36</td>
</tr>
<tr>
<td>PSEC</td>
<td>005527</td>
<td>65:46</td>
</tr>
<tr>
<td>PINLP</td>
<td>005481</td>
<td>64:50</td>
</tr>
<tr>
<td>PINS</td>
<td>005376</td>
<td>63:47</td>
</tr>
<tr>
<td>PRTH</td>
<td>005421</td>
<td>64:09</td>
</tr>
<tr>
<td>PMSK1</td>
<td>000274</td>
<td>6:07</td>
</tr>
<tr>
<td>PMSK2</td>
<td>000275</td>
<td>6:08</td>
</tr>
<tr>
<td>PMSK3</td>
<td>000276</td>
<td>6:09</td>
</tr>
<tr>
<td>PCT</td>
<td>005524</td>
<td>65:44</td>
</tr>
<tr>
<td>POSS</td>
<td>000304</td>
<td>6:15</td>
</tr>
<tr>
<td>PRT</td>
<td>005354</td>
<td>63:24</td>
</tr>
<tr>
<td>PKTN</td>
<td>004763</td>
<td>57:31</td>
</tr>
<tr>
<td>PWT</td>
<td>004354</td>
<td>51:20</td>
</tr>
<tr>
<td>PWT2</td>
<td>005347</td>
<td>63:15</td>
</tr>
<tr>
<td>RAPRE</td>
<td>005600</td>
<td>66:34</td>
</tr>
<tr>
<td>RAINP</td>
<td>004707</td>
<td>56:39</td>
</tr>
<tr>
<td>R2U2</td>
<td>000151</td>
<td>4:36</td>
</tr>
<tr>
<td>RDLN</td>
<td>000144</td>
<td>4:34</td>
</tr>
<tr>
<td>RETUR</td>
<td>004524</td>
<td>53:30</td>
</tr>
<tr>
<td>RSU0</td>
<td>005501</td>
<td>65:10</td>
</tr>
<tr>
<td>RSU1</td>
<td>005502</td>
<td>65:11</td>
</tr>
<tr>
<td>RSU2</td>
<td>005503</td>
<td>65:12</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>SAV0</td>
<td>004527</td>
<td>53:41</td>
</tr>
<tr>
<td>SAV1</td>
<td>004526</td>
<td>53:48</td>
</tr>
<tr>
<td>SAV2</td>
<td>004525</td>
<td>53:39</td>
</tr>
<tr>
<td>SAVE1</td>
<td>004463</td>
<td>52:57</td>
</tr>
<tr>
<td>SAVE2</td>
<td>004464</td>
<td>52:58</td>
</tr>
<tr>
<td>SECH</td>
<td>005277</td>
<td>62:21</td>
</tr>
<tr>
<td>SELH</td>
<td>005317</td>
<td>62:41</td>
</tr>
<tr>
<td>SELPT</td>
<td>008250</td>
<td>5:45</td>
</tr>
<tr>
<td>SESCP</td>
<td>003041</td>
<td>36:58</td>
</tr>
<tr>
<td>SH4FL</td>
<td>004312</td>
<td>49:33</td>
</tr>
<tr>
<td>SHFL</td>
<td>004224</td>
<td>49:49</td>
</tr>
<tr>
<td>SLPAT</td>
<td>004744</td>
<td>57:14</td>
</tr>
<tr>
<td>SLPH</td>
<td>004765</td>
<td>57:33</td>
</tr>
<tr>
<td>SMSK1</td>
<td>000271</td>
<td>6:04</td>
</tr>
<tr>
<td>SMSK2</td>
<td>000272</td>
<td>6:05</td>
</tr>
<tr>
<td>SODI</td>
<td>004472</td>
<td>53:08</td>
</tr>
<tr>
<td>SRTN</td>
<td>004460</td>
<td>52:53</td>
</tr>
<tr>
<td>SSEC</td>
<td>003027</td>
<td>36:47</td>
</tr>
<tr>
<td>S1NC</td>
<td>000237</td>
<td>5:30</td>
</tr>
<tr>
<td>SDOHE</td>
<td>000236</td>
<td>5:35</td>
</tr>
<tr>
<td>SSWH1</td>
<td>003182</td>
<td>37:36</td>
</tr>
<tr>
<td>SAAE</td>
<td>004334</td>
<td>51:07</td>
</tr>
<tr>
<td>SARR</td>
<td>000310</td>
<td>6:18</td>
</tr>
<tr>
<td>STE1</td>
<td>000147</td>
<td>4:34</td>
</tr>
<tr>
<td>STF1</td>
<td>004467</td>
<td>53:04</td>
</tr>
<tr>
<td>STMK1</td>
<td>004465</td>
<td>53:01</td>
</tr>
<tr>
<td>STMK2</td>
<td>004466</td>
<td>53:02</td>
</tr>
<tr>
<td>STP</td>
<td>004373</td>
<td>50:47</td>
</tr>
<tr>
<td>STRT</td>
<td>000484</td>
<td>7:12</td>
</tr>
<tr>
<td>STTS</td>
<td>000285</td>
<td>5:10</td>
</tr>
<tr>
<td>SUTN</td>
<td>004475</td>
<td>53:12</td>
</tr>
<tr>
<td>SZER</td>
<td>002084</td>
<td>24:09</td>
</tr>
<tr>
<td>T01</td>
<td>000543</td>
<td>9:01</td>
</tr>
<tr>
<td>T02</td>
<td>000552</td>
<td>9:11</td>
</tr>
<tr>
<td>T03</td>
<td>000556</td>
<td>9:16</td>
</tr>
<tr>
<td>T04</td>
<td>000564</td>
<td>9:23</td>
</tr>
<tr>
<td>T05</td>
<td>000572</td>
<td>9:30</td>
</tr>
<tr>
<td>T06</td>
<td>000577</td>
<td>9:36</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>----------</td>
</tr>
<tr>
<td>T07</td>
<td>000604</td>
<td>9:42</td>
</tr>
<tr>
<td>T10</td>
<td>000511</td>
<td>9:48</td>
</tr>
<tr>
<td>T11</td>
<td>000620</td>
<td>9:56</td>
</tr>
<tr>
<td>T12</td>
<td>000626</td>
<td>10:05</td>
</tr>
<tr>
<td>T13</td>
<td>000634</td>
<td>10:12</td>
</tr>
<tr>
<td>T14</td>
<td>000642</td>
<td>10:19</td>
</tr>
<tr>
<td>T15</td>
<td>000654</td>
<td>10:30</td>
</tr>
<tr>
<td>T16</td>
<td>000663</td>
<td>10:38</td>
</tr>
<tr>
<td>T17</td>
<td>000674</td>
<td>10:49</td>
</tr>
<tr>
<td>T1OUT</td>
<td>001301</td>
<td>16:01</td>
</tr>
<tr>
<td>T20</td>
<td>000704</td>
<td>10:50</td>
</tr>
<tr>
<td>T21</td>
<td>000714</td>
<td>11:09</td>
</tr>
<tr>
<td>T22</td>
<td>000722</td>
<td>11:16</td>
</tr>
<tr>
<td>T23</td>
<td>000727</td>
<td>11:22</td>
</tr>
<tr>
<td>T24</td>
<td>000737</td>
<td>11:31</td>
</tr>
<tr>
<td>T25</td>
<td>000747</td>
<td>11:40</td>
</tr>
<tr>
<td>T26</td>
<td>000756</td>
<td>11:48</td>
</tr>
<tr>
<td>T27</td>
<td>000770</td>
<td>12:01</td>
</tr>
<tr>
<td>T30</td>
<td>001302</td>
<td>12:12</td>
</tr>
<tr>
<td>T31</td>
<td>001814</td>
<td>12:23</td>
</tr>
<tr>
<td>T32</td>
<td>001026</td>
<td>12:34</td>
</tr>
<tr>
<td>T33</td>
<td>001035</td>
<td>12:42</td>
</tr>
<tr>
<td>T34</td>
<td>001044</td>
<td>12:50</td>
</tr>
<tr>
<td>T35</td>
<td>001054</td>
<td>13:01</td>
</tr>
<tr>
<td>T36</td>
<td>001063</td>
<td>13:09</td>
</tr>
<tr>
<td>T37</td>
<td>001073</td>
<td>13:18</td>
</tr>
<tr>
<td>T40</td>
<td>001105</td>
<td>13:29</td>
</tr>
<tr>
<td>T41</td>
<td>001114</td>
<td>13:37</td>
</tr>
<tr>
<td>T42</td>
<td>001126</td>
<td>13:46</td>
</tr>
<tr>
<td>T43</td>
<td>001140</td>
<td>14:01</td>
</tr>
<tr>
<td>T44</td>
<td>001152</td>
<td>14:12</td>
</tr>
<tr>
<td>T45</td>
<td>001162</td>
<td>14:21</td>
</tr>
<tr>
<td>T46</td>
<td>001172</td>
<td>14:30</td>
</tr>
<tr>
<td>T47</td>
<td>001205</td>
<td>14:42</td>
</tr>
<tr>
<td>T4CY</td>
<td>000242</td>
<td>5:39</td>
</tr>
<tr>
<td>T4IM</td>
<td>000426</td>
<td>50:09</td>
</tr>
<tr>
<td>T4IN</td>
<td>000451</td>
<td>49:51</td>
</tr>
<tr>
<td>T4OUT</td>
<td>000452</td>
<td>50:06</td>
</tr>
<tr>
<td>T50</td>
<td>001214</td>
<td>14:50</td>
</tr>
<tr>
<td>T51</td>
<td>001223</td>
<td>14:58</td>
</tr>
<tr>
<td>T52</td>
<td>001232</td>
<td>15:08</td>
</tr>
<tr>
<td>T53</td>
<td>001241</td>
<td>15:16</td>
</tr>
<tr>
<td>T54</td>
<td>001255</td>
<td>15:33</td>
</tr>
<tr>
<td>T54C</td>
<td>000313</td>
<td>6:22</td>
</tr>
<tr>
<td>TAC</td>
<td>000512</td>
<td>58:33</td>
</tr>
<tr>
<td>TIN</td>
<td>000474</td>
<td>49:34</td>
</tr>
<tr>
<td>TINRE</td>
<td>000051</td>
<td>3:24</td>
</tr>
<tr>
<td>TMSG</td>
<td>000423</td>
<td>47:30</td>
</tr>
<tr>
<td>TMSK1</td>
<td>000266</td>
<td>6:01</td>
</tr>
<tr>
<td>TMSK2</td>
<td>000267</td>
<td>6:02</td>
</tr>
<tr>
<td>TMSK3</td>
<td>000270</td>
<td>6:03</td>
</tr>
<tr>
<td>TNON</td>
<td>000404</td>
<td>47:13</td>
</tr>
<tr>
<td>TRET</td>
<td>000432</td>
<td>50:14</td>
</tr>
<tr>
<td>TRKAD</td>
<td>000171</td>
<td>4:55</td>
</tr>
<tr>
<td>TSHSK</td>
<td>001576</td>
<td>21:35</td>
</tr>
<tr>
<td>SYMBOL</td>
<td>VALUE</td>
<td>DEFINED</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>TTBL</td>
<td>000466</td>
<td>8:12</td>
</tr>
<tr>
<td>TYPE</td>
<td>005653</td>
<td>67:24</td>
</tr>
<tr>
<td>TYPIN</td>
<td>006666</td>
<td>3:38</td>
</tr>
<tr>
<td>TYPRE</td>
<td>005661</td>
<td>67:38</td>
</tr>
<tr>
<td>WCPAT</td>
<td>004731</td>
<td>57:01</td>
</tr>
<tr>
<td>WCPT</td>
<td>004764</td>
<td>57:32</td>
</tr>
<tr>
<td>WCCTR</td>
<td>006653</td>
<td>3:26</td>
</tr>
<tr>
<td>WLP</td>
<td>005460</td>
<td>64:47</td>
</tr>
<tr>
<td>WLP2</td>
<td>005475</td>
<td>65:05</td>
</tr>
<tr>
<td>WDRM</td>
<td>005313</td>
<td>62:36</td>
</tr>
<tr>
<td>WRERR</td>
<td>000163</td>
<td>4:49</td>
</tr>
<tr>
<td>WRL</td>
<td>000280</td>
<td>5:05</td>
</tr>
<tr>
<td>WRLNL</td>
<td>000145</td>
<td>4:12</td>
</tr>
<tr>
<td>WRTC</td>
<td>005504</td>
<td>65:13</td>
</tr>
<tr>
<td>ZERM</td>
<td>005273</td>
<td>62:16</td>
</tr>
<tr>
<td>ZERPA</td>
<td>004664</td>
<td>56:17</td>
</tr>
<tr>
<td>ZOCT</td>
<td>005522</td>
<td>65:40</td>
</tr>
<tr>
<td>ZSUPP</td>
<td>005577</td>
<td>66:33</td>
</tr>
</tbody>
</table>
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AMCOMP, INC.

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