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UNDERSTANDING BIT-ERROR-RATE TESTING

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN

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MAY 9, 1991

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A PREVIEW OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE

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While HP's high-performance plastic optocouplers may all look alike, the similarity is only skin deep.

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There is a better way.
Extraordinary disc drives require extraordinary parts.
Today's disc drives are smaller in size and larger in capacity than ever before due to advances in component technology. By designing and manufacturing most of the components ourselves—a concept called vertical integration—we can control the technology, cost, availability and quality of these critical parts.

Technically speaking, no one builds more advanced thin-film discs and recording heads than Seagate. These core technologies help us put 3 gigabytes of storage in a box the size of a toaster. And because we design our own components, we can bring our new products to market faster.

Of course, a key consideration in building our own parts is the cost. By controlling the manufacturing process down to the component level, we can have a significant impact on the cost of our finished products. The end-result is a better value for the customer without sacrificing quality or performance.

In terms of availability, it's important to know that Seagate shipped over 7 million disc drives last year alone. With volumes like these, building our own components helps us avoid the parts shortages that often plague other disc drive manufacturers.

Most importantly, vertical integration allows us to maximize the quality of every component we produce. With the industry's most advanced equipment and testing techniques, we consistently turn out components and finished products that are beyond reproach.

Obviously, it takes an extraordinary capital investment to pursue this strategy. But the disc drive companies who control their critical component production will be better able to control their own destinies, as well as those of their customers.

For more information on our complete line of high-performance disc storage products, contact your authorized Seagate distributor. Or call Seagate at 800-468-DISC, or 408-438-6550.
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• Designing with a new combination RAM and PLD
• PIPS Special Section: Power, Interconnections, Passives, Switches & Relays
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  Computing EIA-standard component values
  Selecting the proper shielded connector
  Controlling the taper of variable resistors
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  Technology Advances

Correction: In the Special Report “High-resolution ADCs up dynamic range in more applications,” Apr. 11, p. 65, we neglected to mention that the Micro Networks MN6400 family of 16-bit ADCs also guarantees 16-bit differential and integral linearity, as well as no-missing-code operation, over its operating-temperature range. Ed.

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial Achievement Awards

Cover: Jook Leung

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IN THE TIME IT TAKES COULD ROUTE THE WO

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At Xilinx we invented the FPGA. And we've led the industry ever since. With the fastest, highest-performance FPGAs available anywhere.
Today, we offer system clock speeds of 60 MHz.
We're also the first programmable logic company to offer you on-board RAM.
Making our newest FPGAs ideal for everything from FIFOs to register stacks.
What's more, we're the only programmable logic company that provides you with on-chip wide decode.
And that's just the beginning.
Because as formidable as our hardware may seem, it's only half the story.

Our new push-button software makes programming other logic devices seem positively tedious.

NEW ENHANCED SOFTWARE PROVIDES PUSH BUTTON SOLUTION.
Device speed alone doesn't determine the fastest, highest-performance logic device.
When you're designing, the clock on the wall is every bit as important as the clock speed of the chip.
So to make Xilinx FPGAs even faster and easier to program, we've redesigned our software.
This is no mere upgrade. It's a major rewrite.
Our new version of XACT now comes with 200 soft macros. And fifty hard macros.
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With greater than 90% gate utilization.

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**IF AT FIRST YOU DON'T SUCCEED, IT'S EASY TO TRY AGAIN.**

As you well know, when you're designing a system, changes keep coming fast and furious. Which is why Xilinx FPGAs are designed to be reprogrammed quickly an unlimited number of times.

And not only do our FPGAs save you an enormous amount of time early on, they also save you time later when you need to make those "last minute" enhancements.

It's one more way we make it easier for you to get your product to market as fast as possible. First time. Every time.

![Graph showing elapsed time for 100% routing](chart)

**GETTING AN EDGE OVER YOUR COMPETITORS IS JUST A PHONE CALL AWAY.**

If you've read this far, you could have already placed and routed one of our FPGAs.

So don't delay. No other programmable logic company can offer you the many exclusive features of Xilinx FPGAs.

Call 1-800-255-7778. Or in California, 408-559-7778. And we'll send you more information on how our FPGAs can give you the competitive edge.

But you'd better hurry. Some of your competitors have already finished reading this ad.

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The Programmable Gate Array Company®

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• Calibration and Engineering Unit conversion
• Higher resolution: >0.1% accuracy
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• Anti-Aliasing Filter
• Programmable Gain Amplifier
• No programming required
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CIRCLE 86
You'll like the feeling of our new digital troubleshooting scope.

Now there's a 100 MHz digital scope that handles just like analog.

Digital oscilloscopes have certain advantages that are hard to overlook. But for troubleshooting, many engineers still prefer analog scopes. Simply because they like the way they handle.

The HP 54600 changes that. It looks like a 100 MHz analog scope. All primary functions are controlled directly with dedicated knobs. And it feels like one.

The display responds instantly to the slightest control change. But when it comes to troubleshooting, the HP 54600's digital performance leaves analog and hybrid scopes in the dust. At millisecond sweep speeds, the display doesn't even flicker. Low-rep-rate signals are easy to see without a hood. It has all the advantages that only a true digital scope can provide. Like storage, high-accuracy, pre-trigger viewing, hard copy output, and programming. And since it's one of HP's basic instruments, the HP 54600 gives you all this performance at a very affordable price. Only $2,395* for a 2-channel scope; $2,895* for the 4-channel version.

So, if you need the power of a digital scope, but like the feel of analog, call 1-800-752-0900. Ask for Ext. 2282, and find out how well the HP 54600 handles your troubleshooting needs.

There is a better way.

* U.S. Prices only.
† In Canada, call 1-800-387-3867, Dept. 428.
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MACH
Fastest High Density CMOS PLDs
At 15ns

PALCE16V8H-10
Fast Universal CMOS PLD Family
At 10ns

PAL1668-5
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At 5ns
### Whatever kind of PLD you need, the fastest comes from AMD.

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Not surprising—because AMD invented the PAL® device. That's why we know programmables better. And offer you the most choices of the best devices.

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For more speed, along with low power consumption, try our new 10- and 15-nanosecond CMOS PLDs. Use our 16V8-10s and 20V8-10s anywhere you'd use a GAL® device. Or choose the ever-popular AMD-invented 22V10, at 15ns.

Faster still are our seventh generation bipolar PAL devices. Complete families of 16L8-5s, 20L8-5s, and the 22V10-10s. And for real speed freaks, we're now shipping a 4.5ns bipolar PAL device—the world's fastest TTL programmable logic.

Along with all this speed, we're providing equally fast delivery. In quantity. In fact, we deliver more programmable logic devices than all our competitors combined.

For details, call AMD now at **1-800-222-9323**. And let nothing stand between you and your need for speed.

---

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
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</tbody>
</table>

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**Advanced Micro Devices**

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CIRCLE 149
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Kit provides serial interface to IBM PC for quick prototyping. Board also supports displays up to 240 x 128 pixels. Interface to 6 soft keys or 4 x 4 key matrix.

Kit also includes:

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CIRCLE 107

EDITORIAL

REMINISCING ABOUT A NEW COMPUTER

Recently, the thought struck me as to why, about 20 years ago when radios became so inexpensive, some stations didn’t offer free fixed-tuned radios to select listeners. The result would have been a captive, high-quality audience. The marketing concept is somewhat akin to giving away a razor, but selling the razor blades. Because such radios would be tuned to only one station, they would not need a variable tuning capacitor, reducing their cost even further. The radio broadcasters, after all, made their money on commercials—the software—while the hardware was only the vehicle necessary to complete the transaction.

I was reminded of these thoughts by Hewlett-Packard’s introduction of its $699 Model 95LX pocket computer, which includes a built-in copy of Lotus 1-2-3. I recently bought a copy of Lotus 1-2-3 for somewhere around $300, but there’s still the tiresome task of shifting out of my word-processing program and into Lotus 1-2-3 whenever I want to do some budget work rather than editorial work. Now, for not a heck of a lot more, I could have a dedicated piece of hardware to run that program anytime or anywhere (the computer weighs 11 oz. and measures 6.3 x 3.4 x 1 in.). I would want to do so.

The fact that I (taking the role of a typical computer user) would even consider buying a computer to run a single software program shows how far the computer industry has come since the original IBM PC was launched about a decade ago. The HP computer will do other things besides run the Lotus program—it has a calculator function, phone and address storage, and handles text—but the point is that even if it did not, it would still be an interesting, single-function package.

This is by no means a pitch for HP or its new computer. Only the market can, and will, decide whether this is the right product at the right time in the highly competitive pocket-computer market. But it does highlight some basic, ongoing trends in the electronics industry.

For one, it demonstrates software’s relatively constant value while hardware costs continue to decline (nevertheless recognizing the obvious necessity of having the hardware to run the software). Looked at another way, it also demonstrates the importance of identifying a customer need before committing to the design and manufacture of a product. And finally, it demonstrates how smart design teams can better exploit the flexibility of VLSI to tailor hardware to solve those specific user problems.

Stephen E. Acquaviva

Editor-in-Chief
dc to 2000 MHz amplifier series

Unbelievable, until now...tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

NOTE: Minimum gain at highest frequency point and over full temperature range.

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

SPECIFICATIONS

<table>
<thead>
<tr>
<th>MODEL</th>
<th>FREQ. MHz</th>
<th>GAIN, dB</th>
<th>• MAX. NF</th>
<th>PRICE $</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAR-1</td>
<td>DC-1000</td>
<td>18.5</td>
<td>13.0</td>
<td>0</td>
</tr>
<tr>
<td>MAR-2</td>
<td>DC-2000</td>
<td>13</td>
<td>12.5</td>
<td>11</td>
</tr>
<tr>
<td>MAR-3</td>
<td>DC-2000</td>
<td>13</td>
<td>12.5</td>
<td>10.5</td>
</tr>
<tr>
<td>MAR-4</td>
<td>DC-1000</td>
<td>8.2</td>
<td>8.0</td>
<td>7.0</td>
</tr>
<tr>
<td>MAR-6</td>
<td>DC-2000</td>
<td>20</td>
<td>16</td>
<td>11</td>
</tr>
<tr>
<td>MAR-7</td>
<td>DC-2000</td>
<td>13.5</td>
<td>12.5</td>
<td>10.5</td>
</tr>
<tr>
<td>MAR-8</td>
<td>DC-1000</td>
<td>33</td>
<td>23</td>
<td>—</td>
</tr>
</tbody>
</table>

NOTE: Minimum gain at highest frequency point and over full temperature range.

- 1dB Gain Compression
- 1+4dBm 1 to 2 GHz

designers amplifier kit, DAK-2
5 of each model, total 35 amplifiers only $59.95

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

<table>
<thead>
<tr>
<th>Size (mils)</th>
<th>Tolerance</th>
<th>Temperature Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>80 x 50</td>
<td>5%</td>
<td>NPO</td>
<td>10.22, 47.68, 100, 220, 470, 680, 1000 pf</td>
</tr>
<tr>
<td>80 x 50</td>
<td>10%</td>
<td>X7R</td>
<td>2200, 4700, 6800, 10,000 pf</td>
</tr>
<tr>
<td>120 x 60</td>
<td>10%</td>
<td>X7R</td>
<td>0.022, 0.047, 0.068, 1µf</td>
</tr>
</tbody>
</table>

† Minimum Order 50 per Value

Designers kit, KCAP-1, 50 pieces of each capacitor value, only $99.95

Mini-Circuits
A Division of Scientific Components Corporation
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Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620158

CIRCLE 173
You're looking at the biggest news in signal sources in years: two new families of pulse generators from Tektronix.

You can already see one reason why Tek's new pulse generators are stirring up so much interest: their what-you-see-is-what-you-get user interface vastly simplifies your life.

Now you can stop piecing the big picture together from one-line LEDs, blinking error lights and trial-and-error iteration. Tek's new scope-like display lets you set up and modify a whole set of parameters at once, with a true representation of your pulses and instant, visual feedback.

You name your application and logic technology: Tek has a signal source to match. For the first time, you can choose channel capacities from one to six channels, or rep rates from 50 MHz to a remarkable 600 MHz. Choose tools designed for logic, fast logic, or mixed technologies. Vary transition times from 200 ps to 10 ms. Test complex timing relationships with ease.

Add to all this our popular pulse generator plug-ins from Tek TM500/
5000 modular instrumentation, and you can see why we're making waves!

Easier to use, more precise and more expandable, Tek's new pulse generators are doing for signal sources what DSOs have done for measurements.

Contact your Tek sales office for a demonstration, or call for more information.

1-800-426-2200

One company measures up.
These VCXO’s are used to replace a distorted incoming reference signal (e.g., 1.544 MHz, T1), with a stable crystal-controlled signal of the same or any multiple frequency, from 1 to 67 MHz.

With MF VCXO’s, since the specification is computer-tested over the full operating temperatures, you can be assured that the specified frequency-deviation is what you get for capture range.

<table>
<thead>
<tr>
<th>Control Voltage</th>
<th>Deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2001</td>
<td>0.3 to 10V ±175 ppm</td>
</tr>
<tr>
<td>M2002</td>
<td>0.3 to 4V ±75 ppm</td>
</tr>
<tr>
<td>M2003</td>
<td>0.3 to 10V ±175-300 ppm</td>
</tr>
<tr>
<td>M2004</td>
<td>0.3 to 4V ±125 ppm</td>
</tr>
<tr>
<td>M2005</td>
<td>1.0 to 4V ±75-300 ppm</td>
</tr>
<tr>
<td>M2006</td>
<td>0 to 5V ±150 ppm</td>
</tr>
<tr>
<td>M2007</td>
<td>0.5 to 4.5V ±125-250 ppm</td>
</tr>
</tbody>
</table>

**PHASE-LOCKED LOOP-VCXO’S**

Series M2010, M2015

This is the complete loop, including the phase-comparator and the VCXO, in just one package. Add the dividers to match the frequencies. Oscillators from 10 to 30 MHz.

**Frequency Range**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>M2010</td>
<td>±125 ppm</td>
</tr>
<tr>
<td>M2015</td>
<td>±150 ppm</td>
</tr>
</tbody>
</table>

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**EUROPE IS GETTING READY FOR HDTV**

Regular high-definition TV picture transmissions in Europe are probably still several years off, but the television industry—TV set makers, studio-equipment manufacturers, broadcasters, and program producers—is getting set for the new TV era that begins in 1995.

By now, the Europeans have buried all hopes for a global HDTV standard. The Japanese, who were the first to demonstrate the new medium to a broad audience during the 1988 Olympics in Seoul, have their MUSE (multiple sub-Nyquist encoding) standard, an 1125-line/50-Hz system that’s incompatible with existing TV sets. The U.S. favors an 1150-line/60-Hz-compatible system, and American companies are now investigating digital HDTV transmissions. Will the Europeans, who have opted for the 1250-line/50-Hz HD-MAC (high-definition multiplexed analog components) standard, follow suit and also go digital?

"Unless something dramatic happens, Europe won’t see digital HDTV by the mid-1990s," says Sönke Mehrgardt, technical director, ITT Semiconductors Group, Freiburg, Germany. "Work on the HD-MAC standard has gathered such momentum that it cannot be stopped to pursue another approach."

Development of HD-MAC is a truly pan-European effort. Major participants in the 6-year, $600-million project, called Eureka 95, are Philips of the Netherlands, France’s Thomson, Nokia of Finland, and Broadcast Television Systems, a joint venture of Philips and Germany’s Robert Bosch. The first three firms are designing, among other things, the HDTV receivers with the new 16:9 picture format. BTS, of Darmstadt, Germany, is building the studio and program production equipment.

About 35 other companies, universities, and research institutes in 10 countries, are involved in various aspects of HDTV. Philips heads the project.

Eureka 95 is now well into its second phase, which will last until the end of 1992. After that, the industry will gear up for volume production of HDTV equipment—receivers, video-disk players, professional cameras, video-tape recorders, mixers, and the like—conforming to the 1250-line/50-Hz European standard. By 1995, the HDTV infrastructure will be in place and the 16:9 sets will be ready for consumers to buy. Significantly, the HD-MAC system is compatible with present TV technology. This means that today’s receivers can still be used. But, of course, there won’t be the high-definition pictures of HDTV.

Meanwhile, trial HDTV broadcasts have been held in several countries using HD-MAC signals sent over a direct satellite-transmission path. The industry is preparing for large-scale trials next year. These will be held during the 1992 Winter Olympics in Albertville, France; the Summer Olympics in Barcelona, Spain; and the World Exhibition in Seville, Spain. Viewers will see, on pre-production HDTV receivers installed at public demonstration centers throughout Europe, from 8 to 10 hours of sports and cultural programs a day.

Pointing to Europe’s progress in HDTV since 1986, when the first tentative engineering research proposals were made, Peter Bögel, a Philips executive and president of the Eureka 95 directorate, says "although we haven’t yet delivered as much HDTV equipment to studios as the Japanese have, we’re on an equal footing as far as system quality is concerned, and even ahead when it comes to transmission quality.”

Europe’s HDTV project is advancing not only TV-receiver and studio-equipment design, it’s also pushing chip technology. At ITT Semiconductors, which is designing half of the HDTV receiver’s signal-processing circuitry, engineers have come up with an HD-MAC decoder that integrates more than 200,000 transistors. This already accounts for half of the company’s share. The firm is now delivering the decoder chips as samples to Philips, Thomson, and Nokia for application in the pre-production HDTV receivers they’re building.
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**low pass dc to 1200MHz**

<table>
<thead>
<tr>
<th>MODEL</th>
<th>PASSBAND, MHz (loss&lt;1dB)</th>
<th>f00, MHz (loss&lt;3dB)</th>
<th>STOP BAND, MHz (loss&gt;20dB)</th>
<th>VSWR</th>
<th>PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLP-10</td>
<td>DC-11</td>
<td>14</td>
<td>19</td>
<td>24</td>
<td>200</td>
</tr>
<tr>
<td>PLP-21</td>
<td>DC-22</td>
<td>24.5</td>
<td>32</td>
<td>41</td>
<td>200</td>
</tr>
<tr>
<td>PLP-30</td>
<td>DC-32</td>
<td>36</td>
<td>47</td>
<td>61</td>
<td>200</td>
</tr>
<tr>
<td>PLP-50</td>
<td>DC-48</td>
<td>55</td>
<td>70</td>
<td>90</td>
<td>200</td>
</tr>
<tr>
<td>PLP-70</td>
<td>DC-60</td>
<td>70</td>
<td>90</td>
<td>110</td>
<td>200</td>
</tr>
<tr>
<td>PLP-100</td>
<td>DC-98</td>
<td>108</td>
<td>146</td>
<td>189</td>
<td>400</td>
</tr>
<tr>
<td>PLP-150</td>
<td>DC-140</td>
<td>155</td>
<td>210</td>
<td>300</td>
<td>600</td>
</tr>
<tr>
<td>PLP-200</td>
<td>DC-190</td>
<td>210</td>
<td>290</td>
<td>390</td>
<td>800</td>
</tr>
<tr>
<td>PLP-250</td>
<td>DC-225</td>
<td>250</td>
<td>330</td>
<td>420</td>
<td>1200</td>
</tr>
<tr>
<td>PLP-300</td>
<td>DC-270</td>
<td>297</td>
<td>410</td>
<td>550</td>
<td>1200</td>
</tr>
<tr>
<td>PLP-450</td>
<td>DC-400</td>
<td>440</td>
<td>580</td>
<td>980</td>
<td>1200</td>
</tr>
<tr>
<td>PLP-550</td>
<td>DC-530</td>
<td>570</td>
<td>750</td>
<td>920</td>
<td>1200</td>
</tr>
<tr>
<td>PLP-750</td>
<td>DC-700</td>
<td>770</td>
<td>1000</td>
<td>1300</td>
<td>2000</td>
</tr>
<tr>
<td>PLP-800</td>
<td>DC-720</td>
<td>800</td>
<td>1080</td>
<td>1400</td>
<td>2000</td>
</tr>
<tr>
<td>PLP-1000</td>
<td>DC-900</td>
<td>900</td>
<td>1620</td>
<td>2100</td>
<td>2500</td>
</tr>
</tbody>
</table>

**high pass dc to 2500MHz**

<table>
<thead>
<tr>
<th>MODEL</th>
<th>PASSBAND, MHz (loss&lt;1dB)</th>
<th>f00, MHz (loss&lt;3dB)</th>
<th>STOP BAND, MHz (loss&gt;20dB)</th>
<th>VSWR</th>
<th>PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHP-50</td>
<td>41</td>
<td>200</td>
<td>26</td>
<td>20</td>
<td>1.5</td>
</tr>
<tr>
<td>PHP-100</td>
<td>90</td>
<td>400</td>
<td>55</td>
<td>40</td>
<td>1.8</td>
</tr>
<tr>
<td>PHP-150</td>
<td>133</td>
<td>600</td>
<td>90</td>
<td>70</td>
<td>1.8</td>
</tr>
<tr>
<td>PHP-175</td>
<td>160</td>
<td>800</td>
<td>105</td>
<td>70</td>
<td>1.8</td>
</tr>
<tr>
<td>PHP-200</td>
<td>185</td>
<td>800</td>
<td>116</td>
<td>90</td>
<td>1.8</td>
</tr>
<tr>
<td>PHP-250</td>
<td>225</td>
<td>1200</td>
<td>150</td>
<td>100</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-300</td>
<td>290</td>
<td>1200</td>
<td>190</td>
<td>145</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-400</td>
<td>395</td>
<td>1600</td>
<td>290</td>
<td>210</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-500</td>
<td>500</td>
<td>1600</td>
<td>365</td>
<td>290</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-600</td>
<td>600</td>
<td>1600</td>
<td>440</td>
<td>340</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-700</td>
<td>700</td>
<td>1800</td>
<td>520</td>
<td>420</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-800</td>
<td>800</td>
<td>2000</td>
<td>570</td>
<td>445</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-900</td>
<td>900</td>
<td>2100</td>
<td>650</td>
<td>520</td>
<td>1.9</td>
</tr>
<tr>
<td>PHP-1000</td>
<td>1000</td>
<td>2200</td>
<td>720</td>
<td>550</td>
<td>1.9</td>
</tr>
</tbody>
</table>

**bandpass 20 to 70MHz**

<table>
<thead>
<tr>
<th>MODEL</th>
<th>CENTER FREQ MHz</th>
<th>PASS BAND, MHz (loss&lt;1dB)</th>
<th>STOP BAND, MHz (loss&gt;10dB)</th>
<th>VSWR</th>
<th>PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBF-10</td>
<td>10.7</td>
<td>9.5-11.5</td>
<td>7.5</td>
<td>15</td>
<td>6.5</td>
</tr>
<tr>
<td>PBF-21.4</td>
<td>21.4</td>
<td>19.3-23.6</td>
<td>15.5</td>
<td>29</td>
<td>3.0</td>
</tr>
<tr>
<td>PBF-30</td>
<td>30.0</td>
<td>27.0-33.0</td>
<td>22</td>
<td>40</td>
<td>3.2</td>
</tr>
<tr>
<td>PBF-40</td>
<td>40.0</td>
<td>37.0-51.0</td>
<td>44</td>
<td>79</td>
<td>4.6</td>
</tr>
<tr>
<td>PBF-50</td>
<td>50.0</td>
<td>40.0-70.0</td>
<td>51</td>
<td>94</td>
<td>4.9</td>
</tr>
</tbody>
</table>

**narrowband IF**

<table>
<thead>
<tr>
<th>MODEL</th>
<th>CENTER FREQ MHz</th>
<th>PASS BAND, MHz</th>
<th>STOP BAND, MHz</th>
<th>STOP BAND, MHz</th>
<th>VSWR</th>
<th>PRICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB-10.7</td>
<td>10.7</td>
<td>9.5-11.5</td>
<td>7.5</td>
<td>15</td>
<td>6.5</td>
<td>50-1000</td>
</tr>
<tr>
<td>PB-21.4</td>
<td>21.4</td>
<td>19.3-23.6</td>
<td>15.5</td>
<td>29</td>
<td>3.0</td>
<td>800-1000</td>
</tr>
<tr>
<td>PB-30</td>
<td>30.0</td>
<td>27.0-33.0</td>
<td>22</td>
<td>40</td>
<td>3.2</td>
<td>99-1000</td>
</tr>
<tr>
<td>PB-40</td>
<td>40.0</td>
<td>37.0-51.0</td>
<td>44</td>
<td>79</td>
<td>4.6</td>
<td>190-1000</td>
</tr>
<tr>
<td>PB-50</td>
<td>50.0</td>
<td>40.0-70.0</td>
<td>51</td>
<td>94</td>
<td>4.9</td>
<td>193-1000</td>
</tr>
</tbody>
</table>

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SOFTWARE MANAGES VHDL SOURCE-CODE CREATION

A complete design environment that creates and manages source code in a VHDL-based design methodology promises to simplify the designer's job. The VHDL Design Assistant, from Ascent Technology Inc., San Jose, Calif., consists of three programs that provide design management, a VHDL specific source editor, and a source browser. The browser views a VHDL design as a data base and permits various inquiries that assist designers in understanding and maintaining VHDL designs on a logical level. The software employs built-in knowledge of the language standard to ease text and graphics creation, as well as assisting the analysis, maintenance, and documentation tasks in a typical product. The Source Manager portion of the software manages a design on a larger file and library basis. It supports the notion of design sets, a concept that precisely captures all sources required for a particular design. The Source Editor offers a mixed-structure/text-editing mode to create and modify the VHDL sources. The first release of the software is slated for late this quarter. Other software modules that will be released later include a state-machine editor, a Petri-net editor, and a VHDL architecture editor.

LIGHT BEAM ACCELERATES PATTERN RECOGNITION

A system that compares up to 1000 stored images with a video scene in just 1 second promises better robotic vision, improved security, and more-accurate weapon systems. Initially developed for missile-guidance systems, the acousto-optic image correlator compares images and determines whether or not a designated pattern or target is within all of the images. When a match occurs, it provides a simple dot representation of the match on a CRT. Researchers at Sandia National Laboratories, Albuquerque, N.M., have developed a functioning model of this hybrid optical processor prototype that stores up to 256 digitized patterns (templates)—representations of different objects or the same object in different rotations and sizes. To perform the comparison, the processor performs millions of multiplications in parallel to determine the closest match. Employing optics for the correlator improves the speed because of the inherent parallelism of optics and the high information capacity of light. Furthermore, the optics enable the system to be very compact while consuming only about 100 W—about 1/10 the power of an all-electronic system that might come close in throughput, but would fill an entire room with equipment. Images are captured with a video camera and compared by scanning them into the correlator using an acousto-optic device. Templates are stored in memory and introduced into the processor by a laser-diode array. The image propagates along the length of the acousto-optic device, and during propagation is compared with the reference template. The signal is then re-imaged onto a charge-coupled device sensor array and displayed on a monitor. A white dot indicates the presence and location of a match. Contact K. Terry Stalker, (505) 844-8143.

SUPERCOMPUTER SETS NEW SPEED RECORD

Scientists running the Linpack benchmark routine on the massively parallel Connection Machine-2 (CM-2) from Thinking Machines Corp., Cambridge, Mass., have achieved computing speeds of 5200 MFLOPS. The benchmark is the standard by which supercomputing speed has been measured since the early 1980s. Thinking Machines claims this establishes a new speed record for conventional supercomputers. The CM-2 utilizes 64,000 processors. The scientists say that later this year the same results will come from a Fortran 90 program.

RECEIVER TAKES GPS NAVIGATION IN HAND

A palm-size Global Positioning System receiver, relying on gallium arsenide chips and application-specific I Cs, could find its way into consumer electronic products by the end of the year. Rockwell Communications Systems' 2.6-by-4.0-in. NavCor V module has five channels, enabling it to take a reading accurate to within 25 m in about 30 seconds. That compares with the two minutes it takes a typical two-channel receiver, says the Dallas company, a division of Rockwell International. Aimed at OEMs, the module consists of four custom I Cs and four memory chips. By adding an antenna, LED readout, application processor, and more memory to the module, engineers can develop a compact auto, truck, or marine navigation system. The NavCore V receiver could also be used in a handheld navigation device for cyclists and hikers. The module’s front end is a gallium arsenide receiver RF/IF that packs 1291 components into a 1/8-in.² space. Rockwell’s DSP chip has 250,000 tran-
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sisters. The receiver, which sells for $450 in small quantities, is scheduled for delivery in the fourth quarter. Sales of the module, which was developed from a military GPS product, could reach $1 billion in four years, the company says. SVT

UNITRODE, MOTOROLA JOIN FOR WAFER BONDING

When direct-wafer bonding was first described at an IEDM conference about five years ago, it sounded so easy: Hold the oxide surfaces of two wafers together with light pressure at 700°C in an oxygen atmosphere. With this technique, you could build low-cost silicon-on-insulator (SOI) starting material that’s ideal for high-voltage ICs. Bond the silicon surfaces and costly, thick epitaxial layers need not be grown for high-voltage discrete parts. However, only Toshiba and Unitrode presently offer devices built from bonded wafers. Now Unitrode Corp., Billerica, Mass., and Motorola, Phoenix, Ariz., have joined forces in a technology partnership to develop a proprietary technique to manufacture direct-bonded wafers. Their goal is to develop a facility that can supply both companies with these wafers for further processing. Additional applications for the technology include VLSI circuits, power and high-voltage ICs, fast analog ICs, and a variety of analog and mixed-signal ICs and sensors. The technology not only raises device performance, but also increases design flexibility, speed, and packing density (particularly for bipolar devices). FG

LAMINATE MATERIAL IS ENVIRONMENTALLY CLEAN

A new paper phenolic copper-clad laminate for use in pc-board fabrication offers a number of advantages over materials now available for pc-board manufacture. Developed at the Industrial Laminates Group of the Philips Plastics and Metalware Factories Div. in the Netherlands, the LC470 laminate is friendly to the environment because it’s free from antimony (Sb), chlorine (Cl), and bromine (Br). This contrasts with the material FR2 that contains such chemicals, which companies around the world have been marketing for more than 20 years. The absence of Sb, Cl, and Br in LC470 leads to a drastic reduction of harmful pollution when waste material is disposed of or burned. Pressure against pollution is growing, and in some European countries, environmental activists are clamoring for manufacturers of end-user equipment—for example, TV sets—to take back the equipment at the end of its life-cycle for disposal. An additional feature of LC470 is that, when heated, it doesn’t give off the irritating smell of present laminates. What’s more, the new Philips laminate can be cold-punched, which means that manufacturers of pc boards need not worry about expansion and shrinkage of the material when punching. The Dutch company expects approval by Underwriters Laboratories (UL) in the U.S. by the end of May. JG

28-PIN PGA PACKAGE CONTAINS MIL MEMORIES

A low-profile, 28-pin grid-array package has been developed for avionics and military EEPROMs ranging in density from 16 to 256 kbits. The package, built by Seeq Technology Inc., San Jose, Calif., has been qualified to MIL-STD-883C Rev C requirements, and its outline has been submitted to JEDEC for standardization. Its dimensions are 0.550 by 0.650 in.; height from the pc board is typically 0.141 in. including standoff. The hermetically sealed PGA uses a solder-sealed gold lid for high-vibration and high-shock environments. Call Rich Norris at (408) 432-7400, ext. 5040. DM

MIXED-SIGNAL ASICS GET 0.7µM 2-POLY CMOS

By moving from a single- to a double-polysilicon CMOS process for its 0.7-µm mixed-signal standard-cell library, NCR, Fort Collins, Colo., more than doubled the performance of its analog cells over those built on its single-polysilicon 1.5-µm process. This double-polysilicon submicron analog process exhibits lower capacitive parasitics, which in turn permits greater operational efficiency in the analog portion of a mixed-signal IC. As a result, future cells in the library can include 5-MHz bandwidth rail-to-rail op amps; 2-µs settling time, rail-to-rail, voltage-output 8-bit DACs; and 5-µs 8-bit successive-approximation ADCs. NCR’s process requires only one mask step more than its single-polysilicon process, yet it can build 80-MHz video DACs and 125-MHz clock synthesizers. Essentially, the process achieves mixed-signal performance levels associated with bipolar and biCMOS processes, but at significantly lower cost. All new analog cells will be added to NCR’s kit-part program, which permits customer breadboarding with DIP packages. The cells will be added to its CAE/CAD-tool library as well. For additional information, call 1-(800) 334-5454. FG
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<table>
<thead>
<tr>
<th>Hardware</th>
<th>Price</th>
<th>MFLOPS</th>
<th>SPECmarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWERstation 320H</td>
<td>$17,972</td>
<td>11.7</td>
<td>32.4</td>
</tr>
<tr>
<td>SPARCstation 2</td>
<td>$14,995</td>
<td>4.2</td>
<td>21.0</td>
</tr>
<tr>
<td>DECstation 5000</td>
<td>$19,395</td>
<td>3.7</td>
<td>18.5</td>
</tr>
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CIRCLE 93

For the Power Seeker.
OVERHAULED TRANSPUTER ARCHITECTURE UPS THROUGHPUT TO OVER 200 MIPS, 25 MFLOPS

The latest generation of processor chips can be likened to the body-builder stereotype—big, powerful, and good for crunching numbers, but limited when it comes to communicating. That analogy forms the foundation of both the old as well as the latest Transputer family members developed by Inmos Ltd., Bristol, U.K. According to Inmos, a processor should be finely balanced between multiple-task processing power and communications, as did the first generations of Transputers with their multiple serial ports, on-chip RAM, and integer and floating-point units.

Not only does the just-disclosed T-9000 Transputer achieve such a balance, but it does so with a vengeance, delivering between 200 and 250 MIPS and 25 MFLOPS of processing horsepower along with four 100-Mbit/s on-chip communication links (see the figure). Target applications include real-time video imaging for high-definition television, industrial inspection, and multimedia office systems.

A T-9000 could transport and simultaneously process up to four image transmission channels with a combined bandwidth of 80 Mbytes/s, and at the same time carry out such tasks as image compression, edge detection, or color conversion. Telecommunications usage covers areas like network protocol conversion and multiplexing. One such example is a network interface card that can multiplex 10 Ethernet channels onto a fiber distributed data interface (FDDI) wide-area network.

To obtain the multi-hundred MIPS throughput, designers at Inmos redesigned the Transputer's internal microarchitecture, exploiting architectural enhancements, instruction parallelism, and silicon-processing improvements developed over the last few years. The chip will employ a submicron three-metal-layer CMOS process that the company has already qualified for other products.

Presently, Inmos has the T-9000, which will be encased in a 208-pad leadless ceramic surface-mounted package, running as a series of "breadboard" modules and simulations. The first complete chips will be sampled in the next quarter, with production slated for the first quarter of 1992. But even with the major redesign, software compatibility with previous Transputer family members was kept intact. And Inmos designers retained the phase-locked clock-multiplication scheme that generates a high-speed 50-MHz clock on chip, from a simple 5-MHz off-chip synchronization clock signal. That helps keep pc-board layout requirements very simple.

The process can still reach higher speeds according to Ian Pearson, Inmos technical director. He claims that future versions will be able to internally clock at up to 70 MHz. In the meantime, one of the working silicon "subcomponents" belonging to the T-9000 is its on-chip memory—16 kbytes of fast static RAM. The RAM can be configured via software to form either a very efficient low-power cache or main program memory, or partitioned as half and half.

The RAM is organized as four independent banks of 4 kbytes each, and each bank can be accessed independently and simultaneously in one 20-ns clock cycle. When configured as a fully associative cache, a bank holds 256 words, with each line containing four words. The cache operates in a write-back mode with random replacement for fast throughput and high hit rate while keeping power consumption down to a minimum. According to Clive Dyson, project design team leader, the memory can deliver data to the chip's pipelined processor at an aggregate rate of up to 800 Mbytes/s using its four 32-bit buses.

The pipeline needs data at that rate. It has five stages, each with its own local workspace memory and cache. A 32-instruction fetch-ahead buffer and instruction grouper feeds the pipeline. The grouper is implemented in hardware with a hardwired lookup table. The table lets it know which of the instructions waiting execution can be grouped together for simultaneous processing.

"The grouper puts together groups of instructions that require the same number of clock cycles to execute," explains Dyson. "Best case is four instructions per group. Further along the pipe, two such groups can themselves be grouped for a maximum of eight instruction executions per cycle."

Two independent arithmetic processors take over at the end of the pipe—one for 32-bit integer operations, the other for full IEEE-754-compliant 64-bit floating-point math. Floating-point 32- or 64-bit additions require just two cycles. Similarly, just two cycles are needed for 32-bit multiplications. Multiplying two 64-bit numbers adds one clock cycle, while...
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32-bit division and square-root operations each require eight clock cycles. A "virility" benchmark done by the company shows that just one processor can run a 1024-point, double-precision, floating-point, complex fast Fourier transform in 2 ms. This is accomplished using a program written in a high-level language, such as Fortran, compiled and run without any special tuning.

Blazing pipeline and calculation speed aren't compromised by communications, Dyson asserts, because a dedicated virtual communications processor takes care of routine interconnection chores, like labeling packets, interrogating processes awaiting for input data, setting up a process to receive fresh data, and looking after hand-shaking between processes. The four communications links each require just four pins and drive 100-Ω transmission lines. Signals can be sent over distances of up to 10 m for board-to-board or inter-rack communications.

Each of the serial links on the T-9000 can be set up to service up to 64,000 duplex "virtual" channels using a packet-multiplexing protocol, thus allowing an almost unlimited number of communication processes to be concurrently executing. The links are designed to directly interconnect the processors to give full linear scalability.

"System processing power increases in direct proportion to the number of CPUs used," says Paul Strzelecki, marketing director. That rule, he claims, holds true even for systems with thousands of processor nodes.

The chip's main functional blocks interconnected by what Dyson terms a "crossbar" network of 32-bit buses. He depicts it as four vertical buses that interconnect the four on-chip memory segments with the memory interface. A CPU pipeline, a virtual communication processor, and a hardware system scheduler cross-connect with all four main buses, each with their own 32-bit buses.

Other external connections include two more communications links for system control, and an event or interrupt pin. The control links are completely separate from the program communications links. They provide an independent communications network that can be used to load code, carry out hardware debugging, monitor a running system for errors, and perform diagnostic functions. Another system simplifier included on the chip is a programmable memory interface that allows the chip to handle any or all of four memory types—DRAM, SRAM, VRAM and EPROM. Using external drives, the processor can address up to 4 Gbytes. The interface can address up to 8 Mbytes of low-cost two- or four-wait-state DRAM without external buffering.

Programming has been made simple too, claims Strzelecki. Because the processor is binary-compatible with earlier Transputers, it can deliver a tenfold performance boost over older Transputers when running existing software. New compilers, though, that can take full advantage of the new chip's abilities, are available for C, C++, Fortran, and Ada programming languages. A Postscript compiler is also available. Contact Paul Strzelecki at Inmos U.K., (44) 0628 890900, or Inmos U.S. at (602) 867-6100.

DAVE BURSKY AND PETER FLETCHER

ADVANCED CIRCUIT/PROCESS LETS HIGH-SIDE MOSFET/IGBT DRIVER IC ALSO SENSE CURRENT

Advancements in circuit techniques and processing have allowed International Rectifier Corp., El Segundo, Calif., to develop high- and low-side driver ICs that not only offer undervoltage-lockout protection, but a number of other self-protection features. One of the features involves the ability to sense, and thus limit, switch current. The high-side (IR2125) driver is fabricated on a 500-V CMOS/DMOS process that builds bipolar and CMOS transistors; the low-side driver is fabricated on a similar 20-V process (see the figure). While the circuit shown is driving a current-sensing FET, a standard FET or an IGBT can also be driven.

The pair represent the second and third members of IR's family of MOSFET drivers, which started with the IR2110. Also built on the 500-V process, the IR2110 provides both low- and high-side drive, but switch protection is limited to undervoltage-lockout protection. The new power MOSFETs and their insulated-gate bipolar- transistor (IGBT) kin are finding much use in large, off-line, switching power supplies and motor-control systems that use half- and full-bridge circuits (see "Chips/Pulse Transformer Build HV High-Side Drivers," p.36).

To turn on a high-side FET switch, its gate must be pulled 10 to 20 V above its source, which, when the FET is on, is essentially at the high-voltage rail. As a result, the high-side drive for each FET must operate from a floating 10-to-20-V supply (Vb, pin 8) whose minus terminal is tied to that FET's source. The driver must increase the 5-V, TTL/CMOS input control signal (pin 2) to between 10 and 20 V, then level-shift it so logic low is at the potential of the FET's source (Vb, pin 5). Low-side drivers need only increase the amplitude of the drive signal.

The IR2125 employs a bootstrap supply for its floating drive voltage Vb. That voltage is developed from the chip's power rail Vcc (pin 1), using the bootstrap diode and capacitor as the FET switch turns off and on. On- and off-chip circuits, operating at high voltage, are highlighted in the figure.

The input logic-control signal feeds a comparator with hysteresis, which in turn feeds a pulse generator through the shutdown latch. If Vcc is below 8 V or above 20 V, which is the over/undervoltage (OV/UV) detector's typical trip point, the circuit shuts off the FET switch by blocking the input signal in the
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The pulse generator puts out narrow On and Off pulses triggered respectively by the input signal's rising and falling edges. A pair of 500-V n-channel DMOSFETs shift the pulses to the level of the floating rail. There they Set and Reset an RS latch working off the rail.

A second UV/OV detector locks the latch if the bootstrap supply exceeds its high or low limits (if gate voltage is too high, it kills the FET; if too low, the FET can go into a linear operating region resulting in excessive power dissipation). The latch feeds a predriver and a CMOS buffer that puts out peak currents of 1 A in pull-up and 2 A in pull-down modes. Driving a capacitance of 3300 pF, the buffer typically provides rise and fall times of 43 and 27 ns, respectively.

When the voltage across the user-selected current-sense resistor exceeds the 230-mV threshold of the current-sense comparator, the comparator fires. After a 500-ns delay (to avoid false triggering by spikes when the FET switches), switch S between the predriver and the buffer moves to the output of a linear amplifier, forming a negative-feedback loop composed of a buffer, FET switch, and amplifier. The gate-drive voltage \( V_{\text{out}} \) settles to a lower value, which limits the FET's current to its original preset value.

The output of the 500-ns delay is also downshifted to the low-voltage level by a circuit like that of the upshifters. However, it uses 500-V p-channel (instead of n-channel) FETs to drive the latch. The output of the latch feeds the error-timing circuits. These circuits and the error comparator perform a number of FET-switch protection functions, including linear-mode timing. If the FET is shorted, they determine the type of short (hard or pulsed), perform cycle-by-cycle external shutdown, and provide a status output flag on pin 3. With the exception of level-shifting circuits and the need for a floating supply, the high- and low-side switches are functionally similar.

The drivers come in 8-pin plastic DIPs rated for operation from -40 to +150°C. In quantities of 1000, the IR2125 goes for $4.80 each. The IR2121 costs $2.48 each in similar quantities. For additional information, call Arnold Alderman, 1-(800) 245-5549.

FRANK GOODENOUGH

**CHIPS/PULSE TRANSFORMER BUILD HV HIGH-SIDE DRIVERS**

Though low-side driver ICs for power MOSFETs and insulated-gate bipolar transistors (IGBTs) continue to grow in numbers, high-side drivers needed in full- and half-bridge plus many control applications are few and far between. Moreover, those becoming commercially available are limited to a differential input-to-output rating of a few hundred volts because of the semiconductor process on which they're fabricated (see "Advanced Circuit/Process Lets High-Side MOSFET/IGBT Driver IC Also Sense Current," p. 34).
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But in many applications, particularly motor controls and uninterruptible power supplies (UPSs), the FET switches run directly off the rectified ac lines. For reliable performance, they require drive circuits that supply up to several thousand volts of input-to-output true galvanic isolation. No one wants to see even a tiny fraction of those voltages sneak into a host computer. However, until now, only complex, costly, and relatively unreliable multi-device discrete solutions have done the job.

To answer that problem, Unitrode Integrated Circuits Corp., Merrimack, N.H., developed a high-side-driver chip set that transfers the isolation job to a single, inexpensive (under 35 cents each in volume), small pulse transformer. One chip, the UC3724, sits at input-control-signal (logic) potential. The other, the UC3725, floats at the FET's source voltage $V_s$. That is, the chip's "ground" pin is connected to the FET's source pin (see the figure).

The transformer carries both the On-Off command for the FET switch and continuous operating power for the high-side chip, while providing isolation limited only by its insulation. Neither IC "sees" the high voltage. As a result, the ICs can be built on a low-cost 40-V bipolar process. Power transfer goes on regardless of whether or not commands are being transmitted. Many alternative techniques that generate floating high-side drive power require that the supply be "refreshed" (by switching action at some minimum rate) when...
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TECHNOLOGY ADVANCES

functional switching isn't underway. Otherwise a startup time is required.

The UC3724 (called an isolated drive transmitter by Unitrode) consists of a duty-cycle modulated fixed-frequency (to about 600 kHz) rectangular-wave oscillator. The carrier carries the power for the UC3725 driver; its modulation carries the command signal. The TTL input to the transmitter (V\text{tr}, pin 7) switches the oscillator's duty cycle between two possible formats (for example, between 30-70% and 70-30%). That is, when the TTL input is logic low, each oscillator output cycle is duty cycle between two logic high 30% of its period, each oscillator cycle is logic low, each oscillator output cycle is duty cycle between two logic high 30% of its period, and logic low 70% of the time. When the input is logic high, each oscillator cycle is high 70% of its period, and low 30%.

Usually, when a train of rectangular pulses with other than 50% duty cycle (such as those just described) is passed through a transformer, the average magnetizing current isn't zero and the transformer's core will saturate. This oscillator's unique design prevents such saturation by ensuring that its magnetizing current decreases to zero between each output cycle. Average voltage across the transformer is always zero, even under the transient conditions caused by input command changes, so core saturation is virtually impossible.

After passing through the transformer, the portions of the waveform with different duty cycles are level-shifted relative to each other, and to \( \pm V_{cc} \) (see the waveforms). The duty-cycle comparator in the UC3725 driver examines the waveform \( V_{A-B} \) (between A, pin 7; and B, pin 8), and in just one cycle detects the level shift. It creates \( V_{out} \) (pin 2), a 10- to-15-V version of the TTL input signal. The Schottky-diode bridge rectifies the carrier to provide chip power. A second comparator with programmable off time (at pins 4 and 5) can implement overcurrent protection. The enable input (pin 6) adds additional control and protection flexibility.

The retriggerable one-shot's pulse width (set by \( R_t \) and \( C_t \)) creates 1/3 of the oscillator's total period, and the transformer core's reset time creates 2/3 of the its period. Working together, they form a free-running multivibrator. Assume the one-shot has been triggered by the output of one of the zero-current detectors (a comparator). The full supply voltage is applied to the transformer primary; one output (assume A) is high, the other (B) is low. Transformer magnetizing current in the primary winding rises linearly at a rate \( \frac{dV}{dt} \) determined by the inductance and the applied voltage:

\[
\frac{dV}{dt} = \frac{-V_A - V_B}{L_{primary}} (A/s)
\]

When the one-shot times out, the logic circuits switch the low output (B) high with \( S_3 \) (letting its catch diode conduct), and the high output (A) to \( V_{cc}/2 \) with \( S_1 \). The action puts half the supply voltage across the primary in the reverse direction. Power is only transferred to the secondary circuit when full voltage is across the primary, during which time its current is a composite of both load and magnetizing current.

Because the load current is interrupted when the polarity is reversed and halved, only a decreasing magnetizing current flows. It falls at half the rate at which it's increased, thus taking twice as long to drop to zero. This resets the core and prevents its saturation. Output A's zero-current detector senses zero magnetizing current and triggers the one-shot, initiating another oscillator cycle. If a continuous high is commanded, the waveforms driving outputs A and B are interchanged, again reversing the magnetizing current.

When the input command is changed, the existing oscillator cycle terminates, the A and B outputs are reversed, and a new oscillator cycle is initiated. Full voltage is applied across the primary for detection by the driver chip. Although the oscillator cycle is terminated without allowing the core to reset, there's no danger of saturation since reversing the outputs forces the magnetizing current to pass through zero before increasing in the opposite direction. Because the one-shot cycle was terminated early (by the change in command), the magnetizing current is actually less than the current for a full cycle, thereby reducing its fall time and the oscillator period.

Both chips in the set come in 8-pin DIPs. In quantities of 1000, pricing starts at $1.75 each for the commercial-grade versions of the UC3724 and UC3725. For additional information, call Joe Pappalardo at (603) 424-2410.

FRANK GOODENOUGH

SIMPLE LIQUID-PHASE EPITAXIAL PROCESS YIELDS 22.3% EFFICIENT GaAs SOLAR CELLS

In worldwide solar-cell development efforts, the name of the game is high efficiency at low cost. That is, getting the most from the solar-to-electrical energy conversion process at a practical cost level. Now, as part of a government-funded project, researchers at the Fraunhofer Institute for Solar Energy Systems in Freiburg, Germany, have fabricated gallium arsenide solar cells with 22.3% efficiencies with a simple process.

A small production run of 35 laboratory-type GaAs cells, which use a relatively simple technology, showed good yields. The 1-cm\(^2\) cells were checked in with efficiencies that were fairly constant between 20% and 22%.

Although the highest for a research group in Europe, the efficiency of 22.3% is by no means a world record, the Fraiberg institute says. The highest reported figure for GaAs solar cells is 25.7%, and it was achieved by a group at the Solar Energy Research Institute (SERI) in Denver, Colo. However, the 0.25-cm\(^2\) SERI cells were made with a relatively expensive layer-tiencing a metal organic chemical-vapor-deposition (MOCVD)
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process.
The Fraunhofer cells, by contrast, use a simpler and environmentally cleaner process based on liquid-phase epitaxy. The institute thinks that the 22.3% efficiency for its cells isn't the limit achievable with this process. By optimizing the cell construction, it hopes to push the efficiency to 23%.

After silicon, GaAs is the second most important material for high-efficiency solar cells. Compared to silicon, though, GaAs has higher light absorption. Therefore, the thickness of the cell's active area need be only a few nanometers. For silicon-based solar cells, on the other hand, that thickness must be from 60X to 100X higher. Other advantages that GaAs has over silicon is that its theoretical-limit efficiency is higher. Also, GaAs cells can operate at higher temperatures as they exist, such as when the sunlight is concentrated onto the cell. Furthermore, because they're less sensitive to cosmic rays, GaAs cells can be used to supply energy to satellites in outer space.

For terrestrial photovoltaic applications, GaAs is an interesting material for tandem and concentrator solar-cell systems. Tandem systems consist of two cells, one atop the other. Each cell is adapted to a different solar-spectrum region so that sunlight can be better exploited than is possible with one cell.

In concentrator systems, a mirror or lens arrangement focuses the sunlight onto the cell. This scheme calls for just a fraction of the cell area that's needed for non-concentrating solar-cell systems.

Currently, the Fraunhofer institute is refining its liquid-phase epitaxy technique so that it can be used to fabricate cells larger than 1 cm² and in larger production runs. Other work involves experiments in depositing GaAs onto silicon and germanium substrates, also by epitaxial methods.

This work aims at lighter and less expensive GaAs solar cells. Also, by cutting GaAs material consumption to a minimum, any environmental damage is limited. The environment is further protected because GaAs solar cells are used only for special applications—for example, in satellites and in concentrator-cell systems.

The four-year development effort at the Fraunhofer Institute for Solar Energy Systems (the work ends in 1992) is fully financed under a $3 million contract from the German Ministry for Research and Technology. The institute is carrying out its work in cooperation with research groups in the industry and at the University of Stuttgart, Germany.

JOHN GOSCH
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REMEMBER WHEN SQUARE WAVES WERE SQUARE?

Typical Digital Waveform, circa 1990
Clock rate > 100 MHz
Rise/Fall Time < 0.5 nsec.
Equivalent microwave signal > 1GHz

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1. Three internal register files, a motion estimator, multiplier-accumulators, and ALUs are among the major functional units of Integrated Information Technology’s Vision Processor. The chip is powered by a 16-bit RISC engine.

PAPERS FROM OVER 30 COUNTRIES DESCRIBE THE LATEST IN ANALOG AND DIGITAL ASICs AND DESIGN SOFTWARE.

CICC ACCENTS GLOBAL ASIC TECHNOLOGY

Lisa Maliniak

With ASICs permeating every area of electronics, the Custom Integrated Circuits Conference (CICC) is distinguishing itself as an important international industry event. This year’s conference offers the latest ASIC technology from all over the world, with more than 170 papers, almost half of which are from 30 countries outside the United States. The conference, being held in San Diego, May 12–15, covers a wide swath of technology: design automation; digital-signal-processing applications; fabrication technology; device, circuit, and system modeling and simulation; analog circuits; telecommunications applications; interfaces and packaging; and design-for-test. Many of the devices described are standard ICs developed by semiconductor manufacturers, which highlights the growing trend toward using ASIC methodologies to create commercial chips (see "IC design adopts ASIC techniques," p. 48).

A session on new hardware products spotlights high-speed, high-density, low-power, CMOS field-programmable gate arrays (FPGAs) based on an antifuse technology called ViaLink. The technique, developed by QuickLogic Corp., Santa Clara, Calif., fabricates devices using a direct metal-to-metal program-
Worldwide competition in electronic markets is forcing standard-IC developers to adopt ASIC design techniques. These techniques include capturing designs at the gate level or higher, using synthesis to map higher levels of design into library elements, and using chip-level timing simulation and analysis. These techniques let chip designers focus on functionality and floor plan, while leaving the specific implementation and layout details to the software. Although these methods make it easier for standard-part designers to quickly frame and finish chip designs, custom integrated-circuit design techniques are still critical for creating cell libraries.

ASIC design techniques improve productivity and time to market, but they don't remove the market pressures on the off-the-shelf products. Standard-part die must be as small as possible to improve yield and minimize manufacturing cost. They must also operate as fast as possible to be competitive. Consequently, custom IC design is more focused on creating fast, dense circuit blocks for the libraries that support the ASIC techniques.

Custom design of digital libraries involves using some manual editing techniques. This may mean "polygon pushing" for ultra-dense cells like dynamic random-access memories. Alternatively, compilers and symbolic layout editors may be utilized for blocks with a higher percentage of digital logic circuitry.

Comprehensive verification and characterization of the library cells is also included in custom design. Characterization supplies the performance data that allows ASIC design tools to make the best trade-offs when using and laying out the cells.

IC design tools are changing to reflect their new cell-level responsibilities. Most important is complete integration of the tools used to create and verify the cells. Layout tools must be meshed with simulation tools to speed the iterations of cell layouts needed to balance multiple parameters, such as speed, power, and size. Custom cell design can't slow down the higher-level processes, like synthesis and automatic layout.

Tool integration also extends into system-level design and analysis. With systems implemented largely on dense chips, it's important to use the chip design database for system simulation and analysis. For example, cell characterization data is the basis for chip-wide timing results, which can then be applied quickly and accurately to system-level timing analysis. Integration of the IC tools within the system-level design environment augments the design-cycle reductions of the ASIC techniques.

These custom design capabilities rely heavily on the integrated-circuit design database technology. Specifically, integrating the chip and system tools is a result of object-oriented programming techniques. In this case, the design environment can rely on the database to automatically keep track of library cells, their many views (graphical, physical, and electrical), and instances of where the cells are used within the entire system design.

IC manufacturers still need IC design tools that can deliver the economics required for standard parts, namely small die size for economical manufacturing. At the same time, however, these IC design tools must support some of the characteristics typically associated with ASIC design tools, like high-level synthesis, design reuse, process independence, and a place within the context of systems design. With this capability in place, designers of digital integrated circuits can adopt the techniques that improve both their productivity and their design's competitiveness.

Contributed by Peter Rip, vice president of marketing for the IC Group at Mentor Graphics Corp., Wilsonville, Ore.
neled arrays to improve the performance. First, the sea-of-gates architecture enables macros to be placed closer together, yielding shorter net lengths. Also, the FET currents were cut in half, reducing the power dissipation by a factor of two. Finally, process improvements, including a gate-length reduction from 0.8 µm to 0.6 µm, produced a 30% overall speed improvement.

The architecture consists of a continuous array of core cells surrounded by I/O buffers and pads. Megacells are placed in columns, with unused columns used for vertical routing tracks. Megacells can span multiple columns, which reduces both area and interconnect capacitance. Clock distribution is accomplished with a fixed clock tree.

Neural networks are the subject of a paper being presented in the FPGA architecture and applications session. The paper, from the IBM Almaden Research Center, San Jose, Calif., describes Ganglion, the hardware implementation of an interconnected, digital, feed-forward artificial neural net on one VME card. Ganglion, which relies heavily on FPGAs, performs 4.8 billion interconnections/s. The system makes novel use of the reprogrammability of FPGAs to reconfigure and adapt to different problems.

Ganglion designers strove for rapid prototyping and low cost for limited card production. They built most of the system from Xilinx programmable gate arrays. The Xilinx reconfigurable arrays furnished density without the cost and lengthy design cycles of full-custom circuits.

**HIDDEN LAYERS**

The network has one hidden layer. The input layer consists of twelve channels, the hidden layer has fourteen units, and the output layer contains four units. Units of different layers are fully interconnected.

The input layer doesn't do any processing, but simply buffers the input data. Units in the other layers first form a weighted sum of their inputs. Eight-bit unsigned inputs are multiplied by 8-bit signed integer weights to produce 16-bit signed products.

The twelve products and a 16-bit signed, unit-specific bias value are accumulated into a 20-bit result.

Next, the 20-bit sum gets scaled to an 11-bit value. It's then passed through an arbitrary activation function that's implemented as a look-up table in a 2-kbyte PROM, producing each unit's 8-bit output.

British Telecom Research Laboratories, Martlesham Heath, United Kingdom, is also presenting a paper on neural networks. The paper details a CMOS integrated circuit that implements very-large, digital, multilayer perceptron neural networks. A back-propagation algorithm helps with on-chip training, and using pseudo-random noise allows for training with coarsely quantized weight values.

The chip, which is fabricated using a 0.7-µm double-metal CMOS process, measures 9 mm by 11 mm. It has 750,000 transistors and contains eight 20-MHz neural processors. Target performance exceeds 20,000 MIPS for a 1000-neuron network. That type of speed will support complex networks that are trained and used in real-time image- and signal-processing applications.

Pseudo-random noise generators allow for training with reduced word-length weights; a noise component is added to weight-update values during training. Independent, automatic weight ranging and scaling at each neural processor prevents weight saturation.

Each of the eight neural processor on the chip have 8 kbits of associated weight storage. The storage can be configured as 512-by-16-bit or 1024-by-8-bit weights. Neural processors can have 8192 connections by selecting different memory blocks. Unused processors on the same chip are bypassed completely. This feature is also used to exclude faulty elements to improve yield.

The basic structure of the device is a linear array of neural processors that can be cascaded to form large networks. Network configuration and layer boundaries are defined at initialization. Each processor acts autonomously, synchronized by a global clock.

Forward relaxation is achieved by passing the input data serially through the network. When the input arrives at each neuron, it's multiplied by the appropriate connection weight and the result is added to the accumulator. After all the inputs have been presented to each neuron in that layer, the accumulated sum of input-weight products is applied to a sigmoidal, nonlinear activation function to produce the inputs for the network's next layer. This process continues until the final layer is reached. At this point, the values produced are the output values of the net. They are serially clocked out of the network, passing unchanged through any unused neurons.

Real-time image processing is the focus of a paper from Integrated In-
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formation Technology, Santa Clara, Calif., which describes a 50-MHz chip called the Vision Processor. It’s a microcoded motion video compression and decompression digital-signal-processing (DSP) chip. The Vision Processor is suitable for many consumer and desktop multimedia applications. Every second, the digital processor can perform $8 \times 10^8$ 16-bit multiply, shift, and accumulate operations; $8 \times 10^8$ pixel absolute-difference operations or $4 \times 10^8$ 16-bit addition-subtraction operations; and $8 \times 10^8$ sum-of-difference operations.

Vision Processor’s major functional units are three multiported internal register files, parallel reconfigurable ALUs, a motion estimator, parallel MACs, a RISC engine, address generators, and an I/O controller (Fig. 1). External static RAMs are used for microcode reconfigurability. To reduce the number of microcode pins, the code is double-pumped at twice the chip’s operating frequency. By changing the microcode, users can easily implement many current and future video-compression standards.

Four parallel 16-by-16-bit multipliers and 24-bit accumulators meet the computational requirements of the discrete cosine transform. The multiplier-accumulators can also be used for general filtering operations, which include rounding and overflow-clamping stages. Multiple shifters perform efficient block floating-point operations.

The 16-bit RISC engine has only eight instructions. These instructions perform many serial operations of the compression algorithms that aren’t suited for the parallel structure of the main datapath. The RISC processor can run in parallel with the main datapath.

Also aimed at high-speed computing is an 80-MFLOPS 64-bit microprocessor for parallel-computing applications, which executes two instructions during its 25-ns cycle time, including the combination of 64-bit floating-point add and multiply instructions. The chip, which was developed at the Semiconductor Research Center at Matsushita Electric Industrial Co. Ltd., Osaka, Japan, has five independent execution units.

Three factors are largely responsible for the 80-MFLOPS performance. First, the device was built from a two-instruction-parallel type of superscalar architecture that includes a five-stage pipeline. Also, a path-selection structure improves the operation speed of floating-point arithmetic units. Finally, the I/O bottleneck common in these chips was relieved by on-chip data and instruction caches, plus double-size instruction and data ports.

The well-oiled pipeline keeps instructions flowing (Fig. 2). In the first stage of the five-stage pipeline, two instructions are fetched from the instruction cache. They’re loaded into two instruction registers of the instruction decoder and pipeline scheduler at the beginning of the second stage. They’re then decoded into control signals for the execution units or two register files, floating-point register, and pointer register. In the third and fourth stage, each instruction is executed by one or two of the five execution units. The fifth stage is assigned to write-back operation of the results to register files.

**DATA CONVERSION**

In a session focusing on data-conversion circuits, a paper jointly written by Vanguard Semiconductor, Milpitas, Calif., and California Micro Devices, Tempe, Ariz., explains a 12-bit video biCMOS track-and-hold amplifier that uses analog calibration. A charge-cancellation circuit combined with feedthrough suppression in a closed-loop architecture results in 12-bit accuracy. For a 4-V full-scale input voltage and 50-Ω output load, the track-and-hold settles to within 1 mV of its final value in 42 ns.

Also in that session, researchers from Tektronix Inc., Beaverton, Ore., describe a 10-bit, 75 Msample/s analog-to-digital converter. The converter uses multiple subranging digitizers to eliminate metastable states and increase sample speed. It measures 4.3 mm by 6.6 mm, and dissipates 2.5 W from a 5-V supply. The device consists of input buffer amplifiers, two 9-bit dual-rank ADCs, a 5-bit flash ADC, error-correction logic, and multiplexing circuitry (Fig. 3). The 9-bit converters use a high-speed, low-gain subranging topology. Two quantizers are offset so that an active region of one converter overlaps a digital-to-analog converter cutoff zone of the second converter. A multiplexer selects the active converter for a given sample, producing the five least-significant bits of the system. This architecture elimi-
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CIRCLE 98
rades possible metastable states due to DAC switchpoints.

A 5-bit flash converter provides the five most-significant bits of the system. It also provides information used by the multiplexer to select between the two 9-bit converters. Data from those converters is used to detect and correct any error in the least-significant bit of the 5-bit first-rank flash.

A 50-MHz variable-gain amplifier is the subject of a paper being presented by the Integrated Circuits and Systems Lab at the University of Calif., Los Angeles. The CMOS device attains a 30-dB range of variable gain with a 50-MHz bandwidth, requires one 5-V supply, and dissipates 150 mW. Applications for the variable-gain amplifier include disk-drive read channels.

In the analog-circuit applications session, a paper from Texas Instruments, Villeneuve-Loubet, France, summarizes new design techniques and measured performances of a 5-V CMOS line circuit that uses oversampled audio converters and a dc-feed controller. It includes 96-dB DACs and 100-dB ADCs. The ADC is a second-order switched-capacitor delta-sigma modulator sampled at 2.048 MHz. The oversampled DAC is embedded in a switched-capacitor low-pass filter.

The dc-feed controller synthesizes adjustable line characteristics. It sets line battery voltage and feed impedance. A line-interface circuit feeds the controller with a scaled-down line voltage, and converts controller-output voltage into the dc-feed current.

Possible approaches to IC reliability simulation are the topic of another paper from the University of California. This paper, which is from the Electronics Research Lab in Berkeley, uses the Berkeley Reliability Simulation Tool (Bert) to illustrate the issues. Bert considers such factors as hot carriers, oxide time-dependent dielectric breakdown, and electromigration. Additional reliability models for bipolar transistor degradation and ESD protection circuits are being implemented into the simulation tool.

The tool simulates circuit reliability and failure rate with the speed of typical Spice simulations. Consequently, design-for-reliability adds only a small effort to the routine process of design for performance. The reliability models must be simple, yet accurate and general enough to pinpoint major reliability weak spots in a circuit. They must also predict at least the relative reliability changes in what-if design procedures.

**Weak Points**

Bert can simulate the waveforms after hot-carrier induced degradation; the failure rate due to oxide wear-out, including the effect of any proposed burn-in; the failure rate due to electromigration; or issue a mixed-signal device are explained as an example of a framework that meshes analog testing with digital DFT. The schemes are multiplexer-based DFT, analog-bus-based DFT, and scan-path-based DFT. In the analog test mode, the various configurations of multiplexers and switches employed in the three schemes are manipulated by the control signals to test analog macros.

AT&T Bell Laboratories, Princeton, N.J., also addresses test in a paper describing the architecture of the Gentest Sequential Test Generator. Gentest creates test vectors for sequential circuits described at the net-list level, without the need for such testability features as scan. For moderate-size circuits (30k–50k gates), the overhead of such techniques is unacceptable. With Gentest, test generation requires no designer involvement.

There are four major enhancements to the algorithm beyond other test generators. First, the Split data structure reduces the complexity of the choice process by dealing with two 3-value algebras (for the good and fault machine), instead of one 9-value algebra. Also, Gentest’s Back algorithm employs a drivability measure that orders outputs and fault-propagation paths to guide the test generator in driving a fault effect to an output. In addition, a set of flip-flop functional-level models handles different clocking regimens. Finally, the Proofs fault-simulation algorithm picks up faults detected as a by-product of the vectors generated for the target fault. The algorithm works by keeping differences between faulty machines, not just between the faulty machine and the good machine. Consequently, the good-machine state doesn't have to be stored, saving a considerable amount of memory. The Proofs algorithm was measured running ten times faster the concurrent fault simulation.

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**How Valuable?**

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<thead>
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<th>Circle</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGHLY</td>
<td>Highly</td>
<td>529</td>
</tr>
<tr>
<td>MODERATELY</td>
<td>Moderately</td>
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CIRCLE 157 FOR LITERATURE
Most electronic loads require stiff dc-voltage sources, typically regulated to within ±5%. A wide range of power supplies do a fine job meeting that need, as long as the load changes slowly. These supplies also work well for fast transients whose magnitudes represent only a small percentage of the total rated supply current.

But with system-clock speeds climbing beyond 50 MHz, and an increasing number of applications featuring pulsed-load current slew rates that exceed 5 to 100 A/µs, today’s power supplies can hardly keep up. Vicor feels it now has an answer to this problem with a newly developed family of modular dc-dc converters called TachoMods. The TachoMods are based on the company’s earlier VI-200 family.

The new converters guarantee that during a 10-to-90% load change, at 200 A/µs, the maximum voltage deviation at the point of load is less than ±5%. The TachoMods eliminate the effects of parasitic inductances by removing capacitance from the converter’s output filter. A patent has been applied for this technique. The more common TachoMod specifications are similar to those of the other VI-200 family members (see the table). Dynamic-response specifications, however, put the TachoMods in a class by themselves.

Internal and external parasitic inductances prevent conventional switching power supplies from handling rapidly switching high-current loads. That is, they can’t keep the supply rail’s voltage—at the load or sometimes at the terminal—even close to the required limits. Such loads can be found on large high-speed computer memory boards containing several hundred CMOS DRAMs; in large, high-resolution video CRT displays; and in radar transmitters and laser drivers.

In a conventional supply, only the output capacitor handles fast changes. The feedback loop and its voltage source are left to handle slow changes.

For years, radar systems have needed sup-
plies like the TachoMods. It has appeared more recently in systems where high-power lasers are driving optical-fiber transmission lines. And it's just now rearing its ugly head in computers. Though the TachoMod was developed for computer applications, it should be a boon to anyone with a large and fast pulsed load that's located more than a few microseconds from the load's voltage rail.

CPU, memory, and related pc boards are contained in one or more racks in traditional computer systems. The power supply, on the other hand, resides in a corner where someone found space for it as the rest of the system was being finished. The dynamic performance of such equipment is truly limited by the transient response of its power system. This includes the power supply's output impedance as a function of frequency, the reactance of the cable connecting the supply with the computer's pc boards, and the reactance of the power-distribution runs on the boards themselves.

**Purge Parasites**

Even now, to reduce the parasitic resistances and reactances typically occurring between the regulator and the pc board, distributed power systems are replacing a single, massive switching regulator. In addition, the transient response of the power supply itself has been improved by raising switching frequencies to over 1 MHz, which in turn can quicken the control-loop's response time. However, even the best distributed-power architectures haven't kept up with the transient-response needs of new and next-generation systems.

Raising switching speeds has made it possible to improve loop response. However, the core issue is now the parasitic inductance created by the converter's output pins and the metal traces between the converter module and the load—high-speed logic or memory devices that often completely cover a 2-ft.-by-2-ft. board.

The traditional solution has been to populate the pc board with large numbers of low-ESR (equivalent-series-resistance) capacitors with one or more located at each chip. These capacitors (usually tantalum) are expensive, they take up valuable board space, and don't have a reputation for reliability. Now, with Vicor's TachoMod, a virtually instantaneous load change by a multitude of computer chips is no longer inconsistent with tight voltage regulation at every chip site.

The heart of typical switching power supplies and board-mounted dc-dc converters consists of switching circuitry that delivers pulses of voltage, V_s, to a choke input LC filter (Fig. 1). The supply’s breakpoint frequency

$$\frac{1}{2\pi V L C}$$

is set well below the converter's switching frequency. The filter delivers the average value of the pulsating waveform to the load connected across the filter and attenuates the waveform's large, time-varying component, essentially eliminating the ripple from the dc output voltage. The circuit's controller senses the voltage across the load and maintains it at a constant average value, within limits, as the source and load change.

The filter's capacitor also stores energy to minimize output-voltage variation in response to sudden load-current changes. In principle, the peak-voltage change in response to large load-current changes can be controlled by correctly sizing the ca-
capacitor. It's typically not an easy task because parasitic inductance lies between the capacitor and the load. The value of this parasitic inductance depends on the geometry of the connections between the capacitor and the converter's terminals, and the connections between the terminals and the load. Inductance \( L_p \) lies inside the converter's terminals, and the inductance \( L_1 \) lies outside the converter, inductance \( L_p + L_1 \), multiplied by the current's rate of change \( (L \, di/dt) \), develops across \( L_p + L_1 \). Because the voltage across the capacitor can't change instantaneously, the voltage at the load is reduced by the voltage drop across the inductances. That drop can be significant. For example, a \( di/dt \) of 20 A/\( \mu \)s produces a 2-V drop across 100 nH. In a 5-V system, that represents a 40% drop in voltage. A more acceptable voltage change of 0.1 V (2%) demands a total parasitic inductance of less than 5 nH, which is less than the inductance produced by a 0.1-in.-diameter loop of wire.

As noted earlier, the traditional technique used to "hold up" the voltage at the load consists of adding massive amounts of "bypass capacitance" across it, as close to the load as possible. This approach may appear to address the problem, but it creates three more. First, increasing the total filter capacitance degrades the response time of the converter. Second, too much capacitance may also cause closed-loop converter instability. Finally, if small amounts of external capacitance are used, a rapid change in load current causes the load voltage to ring. Ringing associated with the circuit loop formed by the external and internal capacitors and the parasitic inductances can be large enough in amplitude (relative to the nominal load voltage) to potentially interfere with system operation or even damage devices.

**INSIDE OUTSIDE**

Vicor's new proprietary power-distribution architecture, as noted earlier, removes the output capacitor and relies on small amounts of bypass capacitance at one or more load sites (Fig. 2). Now all of the parasitic inductances are, in effect, lumped into the filter's inductance (of which they represent only a small part), and they actually perform some of the filtering. Because the current flow's rate of change is no longer limited in the parasitic inductances, external capacitance at the load can be charged rapidly.

The value of the external capacitance need only be enough to eliminate the ripple and limit the maximum output-voltage deviation associated with worst-case load changes. In most computer-logic, or memory-board, applications, the new converters can rely on the energy stored in the distributed capacitors found on the boards. A static load current of 10 to 100 \( \mu \)F/A represents a good rule of thumb for estimating capacitor size.

A number of examples can illustrate the savings in capacitor usage offered by these converters. A typical 100-W, pulse-width-modulator design operating at 50 kHz is one such example. The following additional assumptions should be made:

1. The converter has an output voltage of 5 V, a filter inductor of 50 \( \mu \)H, and the output must be kept within 0.2 V (4%), for a 20-A instantaneous step-current change. About 10,000 \( \mu \)F of capacitance would be needed to "hold up" the voltage. The minimum output would occur about 200 \( \mu \)s after the current step. That much capacitance would reduce the converter's first breakpoint frequency to

---

**TachoMod SPECIFICATIONS**

(Unless noted otherwise, specifications are at a baseplate temperature of 25°C, nominal line voltage, and 75% load current.)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output set-point accuracy</td>
<td>±1%</td>
</tr>
<tr>
<td>Line and load regulation</td>
<td>±0.5% maximum</td>
</tr>
<tr>
<td>Drift with temperature</td>
<td>0.02%/°C</td>
</tr>
<tr>
<td>Efficiency</td>
<td>88% to 90%</td>
</tr>
<tr>
<td>Input isolation to baseplate</td>
<td>3750 V rms minimum</td>
</tr>
<tr>
<td>Output isolation to baseplate</td>
<td>500 V rms minimum</td>
</tr>
<tr>
<td>No-load dissipation</td>
<td>2 W maximum</td>
</tr>
<tr>
<td>Dimensions</td>
<td>4.6 in. x 2.4 in. x 0.5 in.</td>
</tr>
<tr>
<td>Operating temperature (baseplate)</td>
<td>0°C to 85°C</td>
</tr>
<tr>
<td>Nominal dc input-voltage ranges</td>
<td>12, 24, 36, 48, 150, 300 V</td>
</tr>
<tr>
<td>Nominal dc output voltages</td>
<td>2.95 V</td>
</tr>
<tr>
<td>Output-power ratings (power rating determines current rating)</td>
<td>50, 75, 100, 150, and 200 W</td>
</tr>
</tbody>
</table>

---

**3. WHEN SUBJECTED TO 3-TO-27 A load changes slewed at 20 A/\( \mu \)s (the top waveform in figures a through c), a bench supply's output changed 56% and took 2.8 ms to settle (a, bottom), and a fast-response module's output changed 26% and took 3.2 ms to settle (b, bottom). The TachoMod's output, on the other hand, changed just over 4%, settling in 0.8 ms (c, bottom). Note the change of scale in the bottom waveform of (c).**
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225 Hz. Maximum rate of current change through the inductor would be a mere 0.1 A/µs.

By moving to a zero-current switching converter (such as a standard VI-200 module) running at about 1 MHz, the inductor drops (by a factor of 25) to 2 µH and the capacitor (by a factor of 5) to 2000 µF. For a similar step-sized load change, the maximum voltage deviation would occur within 8 µs of the change, the first breakpoint is at 2.5 kHz, and the current can slew at 2.5 A/µs. Finally, by moving to a TachoMod also switching at 1 MHz and still employing 2000 µF of capacitance (but at the load), the maximum deviation runs a mere 0.005 V (0.1%) and occurs in a quick 1 µs. That’s about the settling time expected from a pretty good IC op amp for a modest 10-mA output-current change (for a detailed analysis of these converter architectures and their calculations, ask Vicor for a copy of “Beyond Distributed Power” by Jay Prager, their vice president of system engineering).

THE REAL WORLD

These calculations are theoretical approximations. Translating these calculations into a pc board filled with, say, 200 CMOS DRAMs, using a TachoMod can eliminate the need for nearly 100 tantalum capacitors. Translated into dollars, eliminating the capacitors can drop the board’s power-system cost from about $1.00 a watt to about 75 cents a watt. That doesn’t take into account the value of the space saved, which, of course, can be used to hold more ICs. As noted earlier, the low-ESR tantalum capacitors don’t have a reputation for reliability. When they fail, they usually short out, putting a heavy strain on the power module while shutting down the system. The VI-200 series modules, on the other hand, have demonstrated in-the-field mean-time-between-failures of a million hours.

So now you have the world’s fastest-settling power converter—how do you prove it to yourself, or to potential customers? It becomes a particularly difficult task for distributed load applications, such as logic and memory boards. Here’s the proof: To build a “convincer,” Vicor’s senior application engineer, Charles Skoolicas, loaded a multilayer pc board, 12-in. wide by 18-in. long, with 21 power MOSFET “cells,”

THE CONVINCER

To demonstrate and test their fast-responding TachoMod dc-dc converters, Vicor designed a special-purpose analog computer. Essentially a simulator, this continuously variable, high-speed, dynamic distributed load is built on a 2-ft.² multilayer pc board. It consists of 21 programmable cells and a socket for a VI-200 family converter module. Each cell consists of an IRFR110 power MOSFET rated at 100 V and 5 A, programming circuitry to drive the FET’s gate, and current-sensing circuits. Hooked to a supply, the simulator board’s loads change at rates of up to 420 A/µs.

A VI-200 series module (original or TachoMod) is plugged into the socket in the upper left-hand corner and a dc-voltage source is applied to terminals on its left. Because the converter’s basic specification is for a 10%-to-90% load change, a 10% dc preload (a resistor) is added externally at terminals on the top edge. The preload will vary with the output-current and voltage ratings of the particular module being tested.

Pulse generators are connected to bus A and/or B (top right-hand corner). The amplitude of the generator waveforms applied to the MOSFET gates represents the set point of a feedback loop that controls the current’s magnitude through each FET at between 0 and 5 A. The current waveform duplicates the gate-voltage waveform. Dip switches at each cell select a drive signal from bus A, bus B, both, or neither. Consequently, each cell’s current can be set from 0 to 5 A. By selecting from 0 to 21 cells, up to 105-A pulsed, or 27-A steady state, can be programmed.

This board isn’t a one-of-a-kind marketing tool. It will be put into customers’ hands, for module evaluation, incoming inspection, and test. Provisions have been made on the board for adding capacitors that represent those found in specific applications.
leaving just enough room to plug in a Vicor module. Each cell is a program­ mable, 0-to-5-A load. The complete board can provide pulsed dynamic load changes up to a maximum of 125 A at over 400 A/μs. (see “The con­ vincer,” p. 65).

To demonstrate the TachoMod’s dynamic capability, the board was used to compare the performance of a typical switching bench supply and a standard VI-230-CV module (48-V dc input, 5-V output, at 150 W and 30 A) with a similarly rated TachoMod (VI-230-CV-TM). In each of three cases (Figs. 3a, 3b, and 3c), the load was changed from 3 to 27 A at 20 A/μs, which is the top waveform in each figure. All of the voltage waveforms were taken at the cell in the lower right-hand corner of the board (as far away as possible from the supply terminals).

The bench supply was connected to the board’s preload terminals with about a foot of wire. Its output changed 2.5 V pk-pk, and took 2.8 ms to settle back to 5 V. The standard Vicor module changed 1.32 V pk-pk and settled in 3.2 ms. The Tacho­ Mod’s output varied a mere 216 mV (note change of vertical scale), or about 4.3%, and it settled in 0.8 ms.

**SPECIFICATIONS**

TachoMOD specifications need a little comment. TachoMODs are available with virtually any standard dc output voltage (2, 3.3, 5, 12, 15, 24, 28, 48 V); other outputs are available on request. Input-voltage ranges are specified with three numbers: the input dc voltage representing the minimum expected ac-line voltage, the dc voltage representing the nominal ac-line voltage, and the dc voltage representing the maximum expected ac-line voltage. For example, modules specified for a nominal 12-V input are rated with inputs between 10 and 20 V. Two types of 24-V input modules are available, those that meet their specifications from 21 to 32 V and those that can handle 18 to 36 V at the input. The 48-V-input modules for telecommunications are similar; one class handles 42- to 60-V inputs, the other handles 36 to 76 V. At the high-voltage end, modules running off the rectified 115- and 220-V ac lines produce 100 to 200 V and 200 to 400 V, respectively.

**PRICE AND AVAILABILITY**

Pricing for the TachoMod modules, in quantities of 100, ranges from $90 each to $150 each, depending on power rating. Small quantities are available from stock. Vicor Corp., 23 Frontage Rd., Andover, MA 01810; Renee Catalano Lucas, (508) 470­ 2900.

**HOW VALUABLE?**

- HIGHLY
- MODERATELY
- SLIGHTLY

---

**Small Company's New Golf Ball Flies Too Far; Could Obsolete Many Golf Courses**

Pro Hits 400-Yard Tee Shots During Test Round

Want To Shoot An Eagle or Two?

By Mike Henson

MERIDEN, CT — A small golf company in Connecticut has created a new, super ball that flies like a U-2, puts with the steady roll of a cue ball and bites the green on approach shots like a dropped cat. But don’t look for it on weekend TV. Long-hitting pros could make a joke out of some of golf’s finest courses with it. One pro who tested the ball drove it 400 yards, reaching the green on all but the longest par-fours. Scientific tests by an independent lab using a hitting machine prove the ball out-distances major brands dramatically.

The ball’s extraordinary distance comes partly from a revolutionary new dimple design that keeps the ball aloft longer. But there’s also a secret change in the core that makes it rise faster off the clubhead. Another change reduces air drag. The result is a ball that gains altitude quickly, then sails like a glider. None of the changes is noticeable in the ball itself.

Despite this extraordinary performance the company has a problem. A spokesman put it this way: “In golf you need endorsements and TV publicity. This is what gets you in the pro shops and stores where 95% of all golf products are sold. Unless the pros use your ball on TV, you’re virtually locked out of these outlets.

TV advertising is too expensive to buy on your own, at least for us. “Now, you’ve seen how far this ball can fly. Can you imagine a pro using it on TV and eagle-ing par-fours? It would turn the course into a par-three, and real men don’t play par-three’s. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There’s more to golf than tournaments, you know.”

The company guarantees a golfer a prompt refund if the new ball doesn’t cut five to ten strokes off his or her average score. Simply return the balls — new or used — to the address below. “No one else would dare do that,” boasted the company’s director.

If you would like an eagle or two, here’s your best chance yet. Write your name and address and “Code Name S” (the ball’s R&D name) on a piece of paper and send it along with a check (or your credit card number and expiration date) to National Golf Center (Dept. S-58), 500 S. Broad St., Meriden, CT 06450. Or phone 203-238-2712, 8-8 Eastern time. No P.O. boxes, all shipments are UPS. One dozen “S” balls cost $24.95 (plus $3.00 shipping & handling), two to five dozen are only $22.00 each, six dozen are only $109.00. You save $55.70 ordering six. Shipping is free on two or more dozen. Specify white or Hi-Vision yellow.

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ANALOG INPUTS

<table>
<thead>
<tr>
<th></th>
<th>DT2831</th>
<th>DT2835</th>
<th>DT2831-G</th>
<th>DT2838</th>
<th>DT2837</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>50KHz</td>
<td>50KHz</td>
<td>250KHz</td>
<td>30KHz</td>
<td>30KHz</td>
</tr>
<tr>
<td>Gain</td>
<td>1,2,4,8</td>
<td>1,2,4,8</td>
<td>1,2,4,8</td>
<td>1,2,4,8</td>
<td>1,2,4,8</td>
</tr>
<tr>
<td></td>
<td>1,10,100,500</td>
<td>1,2,4,8</td>
<td>1,2,4,8</td>
<td>1,10,100,500</td>
<td></td>
</tr>
</tbody>
</table>

ANALOG OUTPUTS

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Throughput</td>
<td>130KHz</td>
<td>130KHz</td>
<td>130KHz</td>
<td>100KHz</td>
<td>100KHz</td>
</tr>
</tbody>
</table>

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CIRCLE 112
To properly evaluate digital transmission systems, users must understand their BER tester's specifications.

A critical element in a digital transmission system is how error-free its transmissions are. This measurement is made by a bit-error-rate tester (BERT), which replaces one or more of the system’s components during a test transmission. A BERT must be able to mimic normal and stress conditions and must not be the first component to fail when the system is stressed. Moreover, a BERT’s data pattern and clock quality typically differ from those of the system under test. Consequently, users must know how to obtain and understand these important specifications to ensure an accurate picture of their system’s capabilities.

A digital transmission system includes a data source—such as computer memory, a voice digitizer, or a multiplexer—that originates a digital signal, D (Fig. 1). A clock source produces a clock signal, C, that times the occurrence of each bit in the digital signal. A driver, which may be a power amplifier, a laser diode, an RF modulator, or a tape head, prepares the signal for the system under test. The system under test can be a transmission line with repeaters, or an optical fiber link, microwave radio link, or digital tape recorder. The received signal, F, exhibits the noise and pulse dispersion that the transmission system adds to the digital signal.

If the noise and distortion are within limits, the decision circuit can correctly decide whether the original bit was a 1 or a 0. The circuit does this by comparing F (at sampling instants determined by clock signal G) with a threshold halfway between the two levels (Fig. 1, again). If no errors are made in the decision process, H is a delayed replica of the original data signal D. A clock-
recovery circuit generates G from information in data signal F.

A malfunction in any system component can cause the recovered data to differ from the original data. The primary job of a BERT is to determine the system's error rate rather than to isolate the faulty component. But for the sake of convenience, the BERT may replace the clock source in the transmitter or the receiver. In this case, some fault isolation may be possible by comparing the performance of the system clock sources with that of the BERT. But for the comparison to be meaningful, users must understand the timing jitter specifications of both units.

To measure the system's error rate, the test set performs one or more of the following pairs of functions: data-pattern generation and error monitoring, clock generation and recovery, and jitter generation and measurement. Which functions are used depends on how the BERT is connected in the system.

The simplest measuring technique is to replace the system's data source with the BERT's data-pattern generator and have the BERT receiver monitor the recovered signal for errors (Fig. 2a). Data signal D then becomes D'. The data-pattern generator can mimic typical traffic by creating pseudorandom patterns, or it can stress the system by outputting fixed patterns stored in memory.

**Supplying Data Patterns**

To monitor the transmission, the BERT receiver generates its own data pattern, H', which is the same as the desired data, D'. The BERT receiver compares the received signal, H, with H', and looks for errors. The tester records the total number of errors, the ratio of errors to bits (the bit error rate), the number of "errored" seconds (ES), and the ratio of ES to total seconds.

To make a valid comparison, the BERT receiver must synchronize H' with H. Accomplishing synchronization depends on whether the data is a fixed or pseudorandom pattern.

Sometimes it's convenient for the BERT to supply its own clock signals for its transmitter and/or its receiver. For instance, the system clock may be unavailable in a field situation, or the test engineer may want to avoid the trouble of providing and phasing the clock at the BERT receiver. In this case, the BERT's transmitter clock is C', and its receiver clock is G' (Fig. 2b). In laboratory applications, it's common for the BERT to provide a wide range of clock frequencies.

The BERT's clock source and clock-recovery circuit must be as good as their counterparts in the system under test. The source must introduce negligible timing jitter, because phase jitter in C' causes phase jitter in the recovered clock signal, G, relative to the received data signal, F. Likewise, the BERT's clock-recovery circuit must tolerate at least as much jitter as the system's recovery circuit without causing errors. Clock-source phase jitter and receiver jitter tolerance are discussed in detail later in this article.

Although the BERT clock source should be essentially jitter-free to test the digital transmission system under normal conditions, users may wish to stress the system at times. In
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that case, the BERT must generate controlled jitter. To do so, some BERTs have a jitter generator that can sinusoidally modulate the phase of the clock source (Fig. 2b, again).

On the receive end, the BERT monitors the effect of the controlled jitter in two ways: First it looks for an increased error rate, then it measures the jitter remaining in the recovered data. The second measurement yields the system’s jitter-transmission system. The most general scheme is a repeating pattern stored in memory has a period of $T = 2\pi / f_t$, where $f_t$ is the bit rate. For example, if $f_t = 32$ kHz and $f_c = 1$ Gbit/s, the fixed data pattern must be at least $N = 1$ Gbit/s/32 kHz = 31,200 bits long.

Users can create different stress

**TABLE 1: DATA PATTERNS FOR NOISE MARGIN STRESSING**

<table>
<thead>
<tr>
<th>Pattern A</th>
<th>Pattern B</th>
<th>Margin reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1101101101101101</td>
<td>1101101101101101</td>
<td>0 %</td>
</tr>
<tr>
<td>1001101101101101</td>
<td>1101101101101101</td>
<td>12.5</td>
</tr>
<tr>
<td>1001101101101101</td>
<td>1101101101101101</td>
<td>25.0</td>
</tr>
<tr>
<td>1001101101101101</td>
<td>1101101101101101</td>
<td>50.0</td>
</tr>
</tbody>
</table>

For example, if $f_t = 32$ kHz and $f_c = 1$ Gbit/s, the fixed data pattern must be at least $N = 1$ Gbit/s/32 kHz = 31,200 bits long.
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levels by combining the above patterns with patterns that have an equal number of 1s and 0s, thus causing no stress in a system with ac coupling. For example, the pattern 11001100 won't change the content or noise margin. By combining various amounts of this balanced pattern with the previous unbalanced patterns, users can stress the system to varying degrees, up to 50% (Table 1). Other patterns, such as 10000011000000, stress the noise margin by more than 50%, but they also stress the clock-recovery circuit, which may be undesirable.

Users who want to stress the clock-recovery circuit can do so by varying the transition density. This is because the system's receiver gets its information from the received data signal. For nonreturn-to-zero data, the clock information is in the data transitions. Random data contains an equal number of 0-to-1 and 1-to-0 transitions, and a clock-recovery circuit is usually designed to expect this 50% transition density. The circuit may have trouble with either a greater or a lesser density.

The simplest fixed pattern with a 50% transition density is again 11001100. The patterns in Table 1 that stress noise margin by varying the balance of 1s and 0s also maintain a 50% transition density. Similarly, patterns that stress the clock-recovery circuit by varying transition density should keep the 1s and 0s in balance (Table 2).

As the transition density is increased or decreased from 50%, the bandwidth, $f_p$, the better the tracking and the less the phase error, $\theta_e$. To analyze this relationship, the circuit's transfer function $H(jw)$ can be used, where $j$ is the imaginary unit and $w$ is the frequency. The transfer function describes how the circuit responds to different frequencies. A typical transfer function is given by:

$$H(jw) = \frac{1}{1 + jwT}$$

where $T$ is the time constant of the circuit. The frequency $f_p$ is the frequency at which the magnitude of the transfer function is equal to 1.

To keep the clock edge in the center of the eye pattern, the clock recovery circuit tries to track $\theta_e$. The wider the circuit's bandwidth, $f_p$, the better the tracking and the less the phase errors, $\theta_e$. To analyze this relationship, the circuit's transfer function $H(jw)$ can be used, where $j$ is the imaginary unit and $w$ is the frequency. The transfer function describes how the circuit responds to different frequencies. A typical transfer function is given by:

$$H(jw) = \frac{1}{1 + jwT}$$

where $T$ is the time constant of the circuit. The frequency $f_p$ is the frequency at which the magnitude of the transfer function is equal to 1.  

A. IF THE BERT MANUFACTURER doesn't supply information on clock-source jitter, users can find $\Phi_{\theta_e}$, the spectral density of the clock-source jitter, bottom. First, they measure the source's power spectral density, $\Phi_{\nu}$, top. Then they divide that curve by the clock signal power, $P_c$, middle.

**DESIGN APPLICATIONS**

**BIT-ERROR-RATE TESTING**

Test engineers can characterize a clock source's phase jitter, $\theta_e$, by using a spectrum analyzer to measure $\Phi_{\nu}$, which is the source's power spectral density at voltage $\nu$. The amount of phase jitter is indicated by the width of the spectrum about the clock frequency, $f_c$. In a typical example, the peak spectral density is about −30 dBm/Hz (Fig. A, top). Most spectrum analyzers display power spectral density directly in dBm/Hz. From $\Phi_{\nu}$, users can calculate the clock-source phase's spectral density, $\Phi_{\theta_e}(f)$, and from this determine the rms value of the phase error, $\theta_e$. The first step is to divide $\Phi_{\nu}$ by the clock signal power, $P_c$, which is commonly called the carrier power because jitter is phase modulation. If $P_c$ is 10 dBm, the division reduces the peak spectral density to about −40 dBc/Hz (Fig. A, middle). The units change because the level is now relative to the carrier.

Finally, $\Phi_{\theta_e}$, the spectral density of the clock phase, is obtained by shifting $\Phi_{\nu}/P_c$ so its peak is at the origin (Fig. A, bottom). The relationship is $\Phi_{\theta_e}(f_m) = \Phi_{\nu}(f)/P_c$, where $f_m$ is the offset frequency from the carrier frequency, $f_c$; that is, $f_m = f - f_c$. The units dBc/Hz now have the interpretation $10\log(\text{rad}^2/\text{Hz})$. For example, $10\log(\text{rad}^2/\text{Hz}) = -90$ corresponds to $10^{-9}$ rad^2/Hz.
clock-recovery circuit will fail and the error rate will become significant. A well-designed clock recovery will typically tolerate transition densities between 100% and 25% without causing errors.

**DATA PATTERNS STORED**

Fixed patterns can also be designed to simulate valid line formats in telecommunications. One such format is DS2, the third level in the North American digital hierarchy at 6.312 Mbit/s. The DS2 frame is 1176 bytes long, organized into 24 groups of 49 bits. The first bit in each group of 49 is a framing bit or a control bit, and the rest are data bits. A BERT transmitter can generate such a pattern to test terminal equipment that looks for the framing and control bits.

Fixed data patterns are stored in the BERT transmitter. User-defined patterns are stored in RAM, and manufacturer-provided patterns are stored in ROM. For example, the Microwave Logic gigaBERT-660 offers 4980-bit and 19,440-bit SONET frame patterns on ROM as options.

The BERT receiver must be programmed to produce the same data pattern as the transmitter. The receiver synchronizes its pattern, H', to the received data pattern, H, on the basis of error rate. If the error rate is greater than some set level, say $10^{-2}$, H' is shifted one bit by dropping a clock pulse. This continues until the synchronization is achieved, as indicated by an error rate less than $10^{-2}$.

Another type of pattern, a pseudo-random bit sequence (PRBS), simulates live traffic. A PRBS has all of the properties of a random sequence but is periodic. A fixed pattern could be programmed to produce a PRBS, but a simple circuit can generate a pattern millions of bits long with only 20 to 30 bits of memory. Common pattern lengths are $N = 2^n - 1$, $2^{23} - 1$, and $2^{63} - 1$.

PRBS patterns can stress the noise margin and the clock recovery as fixed patterns do. But it’s done randomly, somewhat like live traffic. When averaged over the whole sequence, the number of 1s and 0s is almost equal (actually different by one), and transition density is 50%. Over a short term, though, the averages can be very different, stressing both noise margin and clock recovery for periods of time.

To stress the noise margin, the PRBS spectrum must have components below the coupling circuit’s cutoff frequency, $f_c$. For example, a 23-stage PRBS generator with a bit rate, $f_b$, of 44.7 Mbits/s has a pattern length of $2^{23} - 1 = 8,388,607$ bits. The fundamental frequency, $f_f$, is $f_b / 8,388,607 = 5.33$ Hz. If $f_L = 32$ kHz, thousands of the pattern’s spectral components are removed. The fraction of power removed is given by $\pi f_f / f_c$, and the square root of that figure is the rms error as a fraction of the signal level:

$$\text{rms error} = \sqrt{\pi f_f / f_c} = 0.047.$$  

This error appears as Gaussian noise with an rms value that is 4.7% of the noise margin. The more spectral components below the cutoff frequency, the more Gaussian the...
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noise is. However, if the PRBS pattern length was $2^7 - 1$, the fundamental would be 350 kHz, which is greater than $f_L$. The noise margin wouldn't be stressed, and the formula for RMS error wouldn't hold.

Similarly, a PRBS pattern will stress the clock-recovery circuit if the pattern's fundamental is within the circuit's bandwidth, $f_B$. If it is, the pattern introduces random jitter in the recovered clock. The jitter's magnitude depends on $f_B$ and on offsets within the circuit. The RMS jitter isn't a function of the PRBS pattern length, but the peak jitter increases with pattern length.

### EXAMINING JITTER

An important factor in a data transmission system is jitter. Ideally, all clock and data signals in the system have a constant frequency with no phase modulation. In practice, a clock source has some phase modulation, or jitter, and noise and imperfect equalization introduce additional jitter. The following discussion examines clock-source jitter alone, assuming that noise and distortion contribute no jitter.

If the received data waveform, $F$, is viewed on an oscilloscope synchronized to that data, the 1s and 0s overlap to produce an "eye" pattern (Fig. 4). If the transmitter clock source has phase jitter $\theta_i$, the received data signal, $F$, has the same jitter. But the eye pattern doesn't display this jitter because the scope is synchronized to the data.

In general, $\theta_o$, which is the phase of the recovered clock signal, $G$, cannot track $\theta_i$ exactly, so some phase error ($\theta_o - \theta_i$) exists between the clock and the data. With the oscilloscope synchronized to the data, this error is seen as a broadening of the recovered clock's trace. The trace's width is the peak-to-peak value of the phase error jitter.

Phase error can cause a problem when the clock's rising edge samples the received data to see if it's above or below the threshold. If the phase error is too great, the rising clock edge approaches the sides of the data eye pattern, and the transmission system's decision circuit makes errors. If $\Phi_{th}(f)$ and $f_B$ are known, the RMS phase error can be calculated:

$$\theta_{e \text{ rms}} = \sqrt{\frac{\pi}{2}} f_B \Phi_{th}(f_B)$$  \hspace{1cm} (1)

where $\Phi_{th}(f_B)$ is the spectral density of the clock-source phase jitter (see "Measuring clock source jitter," p. 76.) BERT manufacturers sometimes specify the clock's single-sideband noise density, $\Phi_{n}(f)$, at an offset frequency of 10 kHz, which is also the value of $\Phi_{th}(10 \text{ kHz})$. From this figure, the value of $\Phi_{th}(f_B)$ can be approximated by:

$$\Phi_{th}(f_B) = \frac{(10 \text{ kHz})^2}{f_B^2} \Phi_{th}(10 \text{ kHz})$$

For example, if $\Phi_{th}(f + 10 \text{ kHz})$ is -84 dBc/Hz, then:

$$\Phi_{th}(10 \text{ kHz}) = 10^{-84/10} = 2.5 \times 10^{-9} \text{ rad}^2/\text{Hz}$$

and for $f_B = 16 \text{ kHz}$,

$$\Phi_{th}(f_B) = \frac{(10 \text{ kHz})^2}{16 \text{ kHz}^2} \times 2.5 \times 10^{-9}$$

$$= 10^{-9} \text{ rad}^2/\text{Hz}$$

If the BERT manufacturer supplies no information on clock-source jitter, the user must measure the spectral density.

Once $f_B$ and $\Phi_{th}(f_B)$ are known, the RMS phase error $\theta_{e \text{ rms}}$ can be calculated from Equation 1. Typical spectral density for the Microwave Logic gigabERT-660 clock source at $f_c = 70$ MHz and $f_B = 16 \text{ kHz}$ is $10^{-9} \text{ rad}^2/\text{Hz}$. For these specifications, Equation 1 yields an RMS phase error of 0.005 rad, or about 0.0008 UI (unit intervals), where 1 UI = $2\pi$ rad. Because the width of the eye pattern in this example is on the order of 1 UI, the phase error has a negligible effect on system performance.

### JITTER TOLERANCE

In general, the noise and imperfect equalization of the transmission system itself introduce much more jitter than the clock source does. If the jitter, $\theta_o$, of the received data exceeds the receiver's jitter tolerance, the receiver will begin making errors. When the BERT is recovering its...
own clock, the instrument receiver's jitter tolerance must be greater than the system receiver's for all waveforms. Otherwise, the BERT will report an incorrectly high error rate.

It's impossible to check all waveforms. Fortunately, however, if the BERT receiver has a higher jitter tolerance for sinusoidal jitter at all jitter frequencies, \( f_m \), then it has a higher jitter tolerance for all jitter waveforms.

The maximum data phase jitter, \( \theta_{e_{\text{max}}} \), that a receiver can tolerate depends on the maximum phase error, \( \theta_{e_{\text{max}}} \), between the data and the clock that the receiver can tolerate. The first failure may be the setup time when the decision circuit samples the data with the clock.

Or the clock-recovery circuit may fail to maintain lock if \( \theta_{e_{\text{rms}}} \) is too great. In any case, \( \theta_{e_{\text{max}}} \) is generally between 0.3 and 1.0 UI peak-to-peak. If the system's \( \theta_{e_{\text{max}}} \) is unknown, it can be measured.

The transfer function from \( \theta_{e} \) to \( \theta_{e_{\text{rms}}} \) is:

\[
|\frac{\theta_{e}}{\theta_{e_{\text{rms}}}}| = \frac{f_m}{(f_m^2 + f_B^2)^{1/2}}
\]

where \( f_m \) is the frequency of the sinusoidal jitter (Fig. 5). Then the maximum data jitter a receiver can tolerate is

\[
\theta_{e_{\text{rms}}} = \frac{\theta_{e_{\text{max}}}}{|\frac{\theta_{e}}{\theta_{e_{\text{rms}}}}|}
\]

Below \( f_B \), \( \theta_{e_{\text{max}}} \) descends at one decade per decade. Above that frequency (where the clock recovery can't follow the data jitter), \( \theta_{e_{\text{max}}} = \theta_{e_{\text{max}}}. \)

For proper operation, the BERT receiver's jitter tolerance curve must lie above that of the system receiver. The plot in Fig. 5 shows that this condition is satisfied if the BERT receiver has a larger \( f_B \) and larger \( \theta_{e_{\text{max}}} \) than the system receiver. The plot offers a quick and simple check if these parameters are known.

If not, the jitter tolerance curves must be measured using a calibrated jitter generator, which some BERTs provide.

A BERT designed to supply jitter has a sinusoidal generator that modulates the clock phase (Fig. 2b, again). Both the frequency, \( f_m \), and the amplitude, \( A \), of the phase are selectable over certain ranges. CCITT Recommendation 0.171 specifies the minimum ranges, which depend on the bit rate of the system under test.

The range of \( f_m \) is from \( f_l \) to \( f_4 \), and the range of the amplitude depends on \( f_m \). At low frequencies, the bit-error-rate tester must generate higher amplitudes than are needed at high frequencies (Fig. 6).

The BERT's jitter generation and jitter measurement specifications should be somewhat higher than the maximum jitter that a system can typically tolerate. As a result, a BERT with jitter generation can find a receiver's \( \theta_{e_{\text{max}}} \) by setting \( f_m = f_l \) and increasing \( A \) until the receiver begins to make errors. In addition, the clock-recovery bandwidth, \( f_B \), can be estimated by lowering \( f_m \) until the jitter tolerance begins to exceed \( \theta_{e_{\text{max}}}. \)

**BERT Affects Accuracy**

Several BERT characteristics can affect the accuracy of system measurements. For instance, a BERT transmitter may have a very jittery clock source, such as an open-loop voltage-controlled oscillator. If so, the system will have a higher error rate or less margin than when the system's clock source is used. Measuring the clock-source spectral density and calculating \( \theta_{e_{\text{rms}}} \) will uncov-
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er this problem.

Another snag may be that a BERT receiver has a very narrowband clock-recovery circuit, such as a crystal-controlled phase-locked loop. The small $f_b$ will probably make the BERT less tolerant of jitter than the system it’s testing. In high-jitter situations, therefore, the BERT will report a higher bit error rate than the actual rate. A BERT transmitter with jitter generation can measure its own receiver’s jitter tolerance and that of the system to see which is greater.

The question of whether a BERT data pattern fairly represents live traffic is more difficult to answer. Experience indicates that long PRBS patterns (N greater than 14) stress the system more than most live traffic does. But it’s the rare traffic with unusually stressing patterns that is most interesting. Therefore, the best users can do is to anticipate these patterns and generate them with fixed patterns from the BERT transmitter.

References

Dan Wolaver, a consulting electrical engineer, received a BSEE from Rensselaer Polytechnic Institute, Troy, N.Y., and an MSEE and PhD from Massachusetts Institute of Technology, Cambridge.

James Hanley, vice president of marketing at Microwave Logic, received BSEE and MSEE degrees from the University of Illinois, Urbana.

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CIRCLE 181
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Abilities to Handle Video Clock Rates up to 75 MHz and Providing Noninterlaced-Monitor Refresh Rates up to 70 Hz, a VGA-Level Video Controller Developed by Western Digital Corp., Irvine, Calif., Provides IBM XGA-Compatible Images. The WD90C30 not only produces 1024-by-768-pixel images with up to 256 colors, but can also supply up to 65,536 colors with standard VGA resolutions of 640-by-480 pixels. To ensure high-speed video-data transfers, the chip will offer a 16- or 32-bit memory-interface option and can support fonts with 6 to 16 dots and 132-column text modes. An eight-level-deep FIFO buffer on the memory interface offers some elasticity so that data can be fed into the controller at the bus’ maximum rate. When combined with a clock synthesizer (such as the ISC90C63 from ICS Inc.), some wide-word DRAMs, and a palette digital-to-analog converter, a compact board, or a display block can be implemented with less than half-a-dozen chips. Contact John Burger, (714) 932-7312.

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Because All Applications Don’t Require Floating-Point Math, Intel Corp., Santa Clara, Calif., Has Opted to Remove the Floating-Point Math Unit on its 80486 Microprocessor. That Enables the Company to Reduce the Chip Price Considerably and Offer System Designers a More Price-Competitive Performance Upgrade to the 80386DX. The 486SX Still Offers the Full 32-bit Bus Structure of the Standard 486, Unlike the Reduced Bus 386SX, Which Has a 16-bit Data Bus Rather Than the 386DX’s Full 32-bit Bus. To Add Floating-point Capability to Systems that Incorporate the 486SX, Intel Designers Created the 487SX. During System Design, Intel Suggests that an Upgrade Site/socket be Allocated on the PC Board So That the 487SX Can Be Plugged In. The 487SX, However, Is Nothing More Than a Full 486DX Processor with a New Package. The 486SX Will Initially Be Offered in 20-MHz Versions, Which Makes It Possible for the Chip to Deliver, at a Lower Cost, a Throughput About 135% That of a 33-MHz Intel 386DX CPU with External Cache. In Lots of 1000, the 486SX Sells for $258, While the 487SX Has a Suggested Retail Price of $799 in Single-unit Lots. For More Information, Contact Intel at (408) 765-8080.
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The PC as an EDA platform: Is the PC up to the task?

Compared to workstations, the biggest difference is not raw computing power, but the available EDA software.

BY JOHN DURBETAKI
OrCAD, 3175 N.W. Aloclek Dr., Hillsboro, OR 97124; (503) 690-9881.

As technology races forward at dizzying speeds, every aspect of the design process is being challenged. Even though designs are becoming more complex, there’s pressure for engineers to reduce design cycles. As this trend continues, today’s engineer must ask himself, “Are the electronic-design-automation (EDA) tools, and specifically personal computers, up to the task?” The answer is a qualified yes: The PC is extremely well-suited in certain areas.

Determining what PCs can and can’t handle isn’t a function of performance, but rather a function of whether the EDA applications software exists and if the particular application can handle the design complexity. In addition to the applications’ basic capabilities, the requirements of the design environment must be reviewed to determine workgroup needs, individual needs, and management needs. The design environment can be specified only with a thorough understanding of all the competing needs.

For example, consider three broad categories of design tasks: IC design, ASIC design, and board design (Fig. 1). Each category can also be partitioned by design complexity: simple and complex. The terms simple and complex cover all aspects of the design category, such as component or gate count, operating conditions, and technology. They also generally reflect the dividing line between the EDA tool requirements in specific areas.

The characteristics of each area in the figure are meant to be general, even though some specific values have been assigned. For instance, a small gate-count IC in an exotic new technology might require using tools typically employed for complex design. Similarly, some tools usually associated with simple designs may be used to design a more complex system by partitioning the design into subsystems. As with any analysis of an object and its boundary conditions, each situation must be carefully reviewed to determine the tools best suited for its design.

Now consider the relative share of design starts in each of the three categories. This reveals a strong dominance of design classification by design category (Fig. 2). For instance, most IC designs are complex because simple designs are probably more quickly and correctly implemented as ASICs. Moreover, the dominance in ASIC designs is shifting toward complex designs as greater integration occurs and better tools become available. Simple designs dominate in the board area because component densities aren’t growing faster than the tools and technology can handle. In addition, as greater integration occurs in the IC and ASIC areas, the component count may actually decline.

Many more board designs than IC and ASIC designs exist. Although the number of IC and ASIC designs is currently growing at a higher rate than board designs, this rate will begin to slow down. After all, every IC and ASIC must be placed on a board at some point. Considering that many designs contain no ASICs or custom ICs, the relationship between PCB, IC, and ASIC designs will stabilize at a 75% to 25% ratio.

Different tools exist for simple and complex IC, ASIC, and board design because there’s no such thing as a universal EDA tool. Even though the tool suppliers would like everyone to believe their tools can do it all, reality is that they can’t. Just as a Swiss Army knife can remove a splinter from a finger, yet wouldn’t be recommended for open heart surgery, a tool that’s designed for board layout isn’t suited for IC layout. Conversely, a tool supporting the development of a 1-million transistor IC uses a database that exceeds the needs of the designer of a wall thermostat. Similarly, an analog simulator is a poor choice of tool to check the logical function of a PLD design. Tools are specialized so that they may perform the task demanded of them with a greater degree of precision, performance, or quality. As tasks become more sophisticated, tools become less generalized.

Today, the computing platform is split into two broad categories—personal computers and workstations. The
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*Average force for 121-pin package
designing for systems

The PC as an EDA Platform

Distinction between the two isn't the processor, operating system, graphics support, memory, or supplier, but rather in the way the machine is used. A PC is used by an individual in primarily singular tasks. It may communicate to other PCs or storage areas, but these actions are to support the user's work as an individual. On the other hand, the workstation basically performs group-related tasks. The group interaction of the members is supported by the environment, both hardware and software. Integrating group activities occurs throughout the entire relationship of the group members, and often must occur in real time.

Until recently, categorizing a particular platform as a PC or a workstation was fairly simple. A PC was a rather limited computing platform that had small storage facilities and limited graphics capabilities, supported little of the intensive numerical analysis required by engineering professionals, and had fairly basic software applications often designed to cope with the platform's limitations. It was designed for the masses, supported by the masses, and used by many sectors of the work force. Primarily it was used in offices, laboratories, and engineering communities.

A workstation, on the other hand, was considered to be a much more capable machine. Workstations supported higher computing throughput in numerical analysis and other areas, had larger storage facilities, used virtual operating environments, and had sophisticated applications. Workstations were more expensive than PCs, often by thousands of dollars. In addition, they were designed to be used by the highly computer literate, had applications and operating environments that were complicated and required extensive training, and more often than not were a resource shared among many individuals.

Today, however, these easily recognized traits no longer distinguish the computing platforms. There's little difference in MIPS or MFLOPS between each of the major CPU architectures used today. What difference exists is easily stamped out by the performance differences attributed to the EDA application software. There are machines marketed as PCs and others as workstations that all use the same CPU chip, such as the Apple Macintosh, the Atari Amiga, and the HP/Apollo workstation. In addition, both can be configured with large hard disks, tape backup systems, CD ROM drives, and network interfaces.

Large strides have been made toward better operating environments and graphical user interfaces. Graphics support on PCs has improved in both resolution and drawing performance. On both the PC and the workstation, better human interfaces simplify the human-machine interaction. Examples of this are Windows on the IBM-compatible PC and Open Look on the Sun Sparcstation.

Also, the price difference is negligible between comparably featured systems. While PCs are still generally less expensive than workstations, the price differential between PCs and workstations has closed rapidly and the trend is expected to continue.

The most important factor in determining the hardware required to support design automation is the application software. If an application supports various platforms and configurations, then the range of choice is set. If an application doesn't support the hardware available to the designer, then either the hardware must change, the applications under consideration must change, the vendor of the desired application must be convinced to support the available hardware, or the design and/or design process must change. Most often the last choice is made because there isn't enough money to buy more hardware. Few, if any, reasonable alternative applications are available, and even if the vendor is convinced to support the designer's available hardware, the project time constraints don't allow the designer wait for the application.

Today, PCs can do every task needed for simple board design (Fig. 3). In fact, they can handle the design of most simple ASICs, and a little bit of the complex area in all of the categories. Therefore, the answer that yes, the PC can handle EDA tasks, is qualified based on the type of problem being tackled. For instance, no designer doing a complex ASIC would use a PC today because no EDA software tools are equal to the task.

Generally speaking, the PC has enough horsepower to do most, but not all, electronic design tasks. For instance, a Spice simulation of a 1-million-transistor IC can't be done on a PC. That type of job probably can't even be done on a workstation, but would need the power of a bigger computer. The difference between the PC and the workstation, however, is that the workstation has a link to that bigger computer and the PC generally doesn't.

The chart in Fig. 3 shows which machine dominates in each category of design tasks. For example, workstations can be used to design simple boards even though PCs dominate that area. Today, it's primarily software that situates particular platform-application combinations. Just a few years ago, the hardware would have been the determining factor because PCs had characteristically small resources and low performance, especially to support EDA tools.

A major demand placed on the hardware and software tools stems from the particular design category of the six that were previously discussed. In IC and ASIC design, especially in complex designs, integration occurs throughout the design. A great deal of integration, however, occurs at the end of the design. ASIC and IC integration means connecting various circuits at the transistor level within a product that isn't easily modified. In board design, which

<table>
<thead>
<tr>
<th></th>
<th>IC</th>
<th>ASIC</th>
<th>Board</th>
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<tr>
<td>Complex</td>
<td>80%</td>
<td>40%</td>
<td>20%</td>
</tr>
<tr>
<td>Simple</td>
<td>20%</td>
<td>60%</td>
<td>80%</td>
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<td></td>
<td>15%</td>
<td>85%</td>
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2. The percentages of design starts in each category shows a strong dominance of design classification by design category.
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The conference is structured such that the first day, July 8th, will provide 10 four-hour tutorials 5 in the morning and 5 in the afternoon. The remaining 2 days will present, in 3 parallel technical session tracks, over 100 speakers describing innovative design approaches to implementing high performance desktop and portable systems.

Coffee break refreshments as well as lunches are included in the conference registration. Vendor exhibits showing the latest components for system designers will be open for 2 hours starting at noon on Tuesday & Wednesday. A reception in the exhibit area will be held Tuesday evening.

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**Monday, July 8th - TUTORIALS - (1 through 5; 8:00 AM - 12:00 PM) (6 through 10; 1:00 PM - 5:00 PM)**

**TUTORIAL 1**

Basic Approaches to PC Caches

Intel Corp.

**TUTORIAL 2**

Portable System Design Issues

Intel Corp.

**TUTORIAL 3**

Multifunction Peripherals

National Semiconductor

**TUTORIAL 4**

Basics of SCSI-1 & SCSI-2

NCR Corp.

**TUTORIAL 5**

Designing with High Speed PLD

Intel Corp.

**TUTORIAL 6**

BIOS Design Award Software

Award Software

**TUTORIAL 7**

Powerful Technology Gates Energy Products

Gates Energy Products

**TUTORIAL 8**

Data/Image compression

Oak Technologies & Adv. Hardware Architectures

**TUTORIAL 9**

Integrating SCSI with CAM

Ballard Synergy

**TUTORIAL 10**

Bringing Technology to Market

Regis McKenna, Inc.

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**Tuesday, July 9th, 8:00 AM - OPENING KEYNOTE and TECHNICAL SESSIONS - Beyond the Single Chip PC - Gordon Campbell, CEO, Chips & Technologies Inc.**

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**TRACK I**

- DISPLAY BASICS - CRT Display Technology Directions; Advances in Video RAM Architectures; Advances in RAMDACs and Color Palettes; Where to Put Intelligence in Graphics.

- HIGH PERFORMANCE DISPLAY CONTROLLERS - Understanding VGA Benchmarks; Implementing Advanced Features in VGA Systems; VRAM-Based Ultra-VGA Controllers; Bringing Workstation Graphics to PCs; Implementing 3D Graphics on a PC Add-In Card.

Above papers by: AT&T Microelectronics; Chips and Technologies; National Semiconductor; Cypress; National; NCR; Oak Technology; Toshiba

**TRACK II**

- MOTHERBOARD DESIGN ISSUES - PC Chip Set Market Trends: Challenges and Opportunities; Designing High-Integration EISA Motherboards; Implement Compact EISA-Based Systems; A CPU-Speed-Independent Micro Channel Motherboard.

- BIOS AND SYSTEM PERFORMANCE ISSUES - BIOS Architectural Support for New Chip Sets; Hash Memory: The Ideal BIOS Storage Device; Memory Subsystem Architectural Options; An Algorithm for Dynamic Memory Management; A New Enhanced-Mode DRAM for PC-based Workstations; Smaller, Faster, Cheaper, and Hotter: Thermal Problems and Cooling Solutions.

Above papers by: Intel; NMB; Opti; Phoenix; Toshiba

**TRACK III**

- BATTERY-POWERED SYSTEM ISSUES - Designing Low Voltage Systems; Battery Technology: Current Status and Projections; Clock Synthesis for Laptops; Battery System Management.

- LAPTOP SYSTEM DESIGN APPROACHES - ROM BIOS: The Best Place for Laptop Power Management; BIOS Modifications/Enhancements for Transparent Power Management for the 386SL; Power Management in Laptop Computers; Power Management in Portable Computers; Managing Power in Systems Based on the AM386DXL; Implementing High-Performance Laptops.

Above papers by: AMD; AT&T Microelectronics; Avens; Benchmark Microelectronics; Gates Energy Products; Intel; Phoenix; Toshiba

12:00PM through 2:00PM LUNCH AND EXHIBITS OPEN

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**TUTORIAL 11**

ACCELERATING GRAPHICS - Accelerating 3D Graphics on a PC; Implement an Accelerated Windows Graphics Controller; Apply Multiple Processors to Accelerate GUIs; Accelerate GUIs With Smart Bus Control.

- MULTIMEDIA HARDWARE APPROACHES - Adding Video to PC Graphics; Low-Cost Approaches to Video Compression; Integrating DSP into PC Systems; Developing Application Processors for Multimedia; Implementing Systems with DVI Technology.

Above papers by: Chips and Technologies; Intel; Imnos; Philips Components (Signetics); TI; Spectrum Signal Processing; Weitek.

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5:00PM EXHIBITOR RECEPTION/EXHIBITS OPEN

Technical Sessions continued on next page

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5:00PM EXHIBITOR RECEPTION/EXHIBITS OPEN

Technical Sessions continued on next page

REGISTRATION APPLICATION FORM
(For use at Registration Desk)

**A $50 processing fee will be charged for registrations cancelled before June 23, 1991. No refunds after June 23.**

**# Deduct 10% from the total cost if registering 5 or more persons from one company with one company check. This option voids all other discounts.**

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Monday, June 10th, 8:00 AM - OPENING KEYNOTE and TECHNICAL SESSIONS -
"The 10 PCs You’ll Never See" - Mike Aymar, VP & General Manager, Microcomputer Div., Intel Corp.

**TRACK I**
- FLAT PANEL BASICS
  - Flat Panel Design Options; Flat Panel Displays for Handheld/Low-end Portable; Controlling Full-Color VGA Flat Panels.
- DEALING WITH GUIs
  - A High-Speed Video Digitizer for the Apple Macintosh; System Software Needs of the new Operating Environments: OS/2 and Windows; Designing a CAD Toolkit to Run Under Windows; Developing FAX Communication Interfaces Under Windows; Creating Multi-function User Interfaces; Controlling Instruments Through Windows.

Above papers by: Chips and Technologies; Gebala Systems; Information Associates; QuickLogic; Logical Services; National Semiconductor; Phoenix Technologies; Stanford Resources.

**TRACK II**
- EXPANSION-BUS ISSUES
  - EISA Addon Card Design - Shaking the AT Mentality; System Design Issues for Intelligent EISA/MCA Cards; A RISC-based I/O Processor for PC Architectures; Increasing I/O Performance in PC Architectures; An Extended Local Bus Architecture for Better System Performance.
- HIGH-PERFORMANCE SYSTEM ISSUES
  - Clock Distribution for High-Performance PCs; Care and Breeding of High-Speed Clocks; Applying System-Level Simulation When Designing ASIC Based PC Systems; Streamlining High-Speed System Design With Transmission Line Analysis; Computer-Aided Prototyping For Concurrent PC System Design.

Above papers by: Bull-Microl; Chips and Technologies; EliteGroup Computer Systems; Intel; Quantic Laboratories; QuickTurn Systems; Silicon Systems; Texas Instruments; VLSI Technology.

**TRACK III**
- NETWORKING
  - Putting FDDI on a PCAT Half-Card For Single Attachment Stations; Interface Ethernet to the EISA Bus; Customizing a LAN Controller For a Single-Chip Solution; Direct Bus Mastering in PCs Improves LAN Performance; Take Advantage of Specialty Memories When Building LAN Interfaces.
- DATA COMMUNICATIONS AND MASS STORAGE
  - Employ Serial Packet Controllers for Flexible Protocol Control; Designing Appletalk-Compatible Serial Interfaces; Large Capacity Back-up Systems for Networked PCs/Workstations; Magnetic and Optical Drive Technology; Current Status and Future Directions; Flash Memory: The Optimal Technology for Solid-State Disks; SCSI RAID Subsystems for Redundant, High-Performance Mass Storage.

Above papers by: AMD; Intel; Integrated Device Technology; Mixtor; NCR; Plus Logic; PureData Research/USA; R-Byte; Silicon Systems; Zilog.

FOR MORE PROGRAM INFORMATION CONTACT: Dave Bursky, Chairman SVPC’91 Technical Program. Voice: 408/441-0550, Email: 76366.553@Compuserve.com

FOR EXHIBITION CONTACT: Ken Majlthia, General Chairman SVPC’91 Voice: 408/924-3930, FAX: 408/997-8265, Email:majlthia@calstate.bitnet
includes system design using a number of boards, integration occurs primarily at the beginning of the design cycle. Here, the interfaces between the boards or subsystems are defined. Some integration occurs at the end when the completed subsystems are connected and verified, but most integration is at the beginning.

When the work group requires real-time integration of the design, as in the case of complex IC and ASIC designs, highly integrated hardware and software tools are needed to improve productivity because the group’s interaction has such a great impact on the design, schedule, performance, quality, and other aspects. When the group is small, or when the design contains a defined module-interface specification, group interaction has a much smaller impact than individual productivity.

This doesn’t mean that group- and personal-oriented tools, both hardware and software, shouldn’t be employed in some areas of design. After all, it’s not the tool that determines which type of tool should be used, but rather the task to be accomplished. Tools are often thought of as the end rather than the means to the end, perhaps because they were so difficult to operate. The design process and its relationship to the tools is changing, however, as the hardware and software tools change.

What, then, is needed for the PC to start handling more complex tasks? The applications, operating systems, and network software have to change. They must all move toward supporting a group work environment. For example, the network software must let the applications talk to each other across the network in a sophisticated manner. Today, the PC is inappropriate for handling some tasks because they aren’t individual-oriented tasks.

Some tasks are group-oriented because of how the system is put together, and how the people who work at developing that system interact. A multitasking operating environment is needed for group-oriented design because it lets people share work and information. This is possible on the PC today, but there’s much room for improvement. Also, large design groups need to interact with the database. And designers need more than just the ability to run an application; they need to develop new applications and to run applications that may require more computing resources than they have on their desk.

For these reasons, the network is becoming just as important as the computer. Each designer needs his own machine, but must interact with all of the other individuals. This setup requires an operating system with interconnectivity and interfacing, requirements that DOS doesn’t handle well. DOS is a one-person, one-machine, one-task system. Windows 3.0, considered by many to be the successor to DOS, is a step in the right direction but presently isn’t up to task to solve all of the problems with DOS. For example, to use the 32-bit operating mode of the 80386 and 80486, the application developer must resort to using clumsy and often poor-performing DOS extenders to fit 32-bit applications into a 16-bit operating environment. Therefore, when the application developer is faced with large data spaces, natural and native support for this problem aren’t available. Fortunately, this PC limitation occurs only in the complex, not the simple, design area.

Frameworks are important to this discussion because they manage the design process and the applications used in those processes. Applications are the key to making the PC succeed as an EDA platform. Therefore, the more that the framework and the applications can remove the burden of the tedious tasks, (such as integrating and interfacing tools), the more the productivity is enhanced. Frameworks, of course, need time to mature and develop. It’s such a large and complicated task that the industry can’t develop a solution all at once. Using the goals and standards now being developed by the CAD Framework Initiative, implementation will be many years away.

Although things like frameworks are the means to the end, they certainly aren’t the end. And there are more tasks to be solved beyond those the frameworks will solve. One set of tools can’t meet the needs of both group- and personal-oriented environments now, but large strides have been and will continue to be made toward both group and individual productivity. The goal is being approached from a number of different angles. Rapid progress will continue as long as standards and practices allow room for experimentation and change. This sounds quite disconcerting to the users that endure every change. It would be wonderful if anyone could design the product that doesn’t need to change, but it hasn’t happened yet and it’s not likely to happen. But all isn’t as discouraging as this last statement indicates. The progress made in design automation has shown many improvements. Future design environments will see just as dramatic improvements.

John Durbetaki, chief executive officer of OrCAD, received a BEE from the Georgia Institute of Technology, Atlanta.
Build A Speedy Low-Cost Graphics Accelerator In Hardware

An Efficient Design Puts Repetitive Functions In Hardware For Fast Operation.

By Phil Mattison

VLSI Technology Inc., 8375 S. River Pkwy., Tempe, AZ 85284; (602) 752-6174; Fax (602) 752-6000.

The surging popularity of user-friendly interfaces with bit-mapped graphics continues to push designers to improve graphics performance and trim hardware cost. And, thanks to technology advances, the chips that induce graphics in workstations and PCs keep growing more powerful, more compact, and less expensive. These hardware developments mean that designers can build a high-performance, low-cost graphics subsystem using off-the-shelf components, such as VLSI Technology’s Raster-Op ALU chip, and a graphics controller, like Texas Instruments’ TMS34061 chip.

Understanding today’s graphics hardware depends on knowing some graphics history. Early PC graphics adapters, such as the Color Graphics Adapter (CGA), were simple bit-mapped display controllers without hardware-assisted drawing functions. To speed certain drawing operations, the Enhanced Graphics Adapter (EGA) incorporated bit-masking and color-compare functions.

The Video Graphics Array (VGA) went a step further by arbitrating automatically between CPU and CRT controller access to display memory. This arbitration relieved the software of polling for a vertical retrace interval, thus avoiding “snow” on the display caused by CPU access during active video intervals. This did little to improve performance, however, because the processor still had to wait for a retrace interval.

The first departure from this architecture came with IBM’s 8514A chip, the first truly independent graphics coprocessor. The 8514A coprocessor includes a line-drawing engine, which implements Bresenham’s line-drawing algorithm in hardware, as well as automatic bit-block transfers (BitBLTs). Texas Instruments’ 34010 family supplies similar functions but with more flexibility. The 34010’s low-level graphics functions are programmable while the 8514A has a fixed function set. Both chips can operate independently of the host CPU. If software exploits this capability, the independent operation can afford parallel processing. Unfortunately, the 8514A’s software drivers don’t take advantage of independent operation—they simply wait for each operation to finish.

To attain independent operation, designers use a wide variety of schemes in non-PC graphics subsystems, from window priority controllers to completely independent display list processors. To supply more display-memory bandwidth to the CPU, many makers of after-market, or clone, VGA equipment added FIFO data buffers and dual-port video DRAM, among other components.

Designers of graphics subsystems must make trade-offs between cost and performance. Analyzing the software that drives the system is the best way to identify graphics functions for which hardware enhancement yields the greatest performance increase relative to cost. Highly repetitive low-level functions are usually the best candidates for hardware enhancement. In the single-user world, the most common graphics-related applications are computer-aided design and desktop publishing.

The most routine graphics operations are line drawing and BitBLTs. Almost any bit-mapped screen display can be drawn using these two operations, and the algorithms for their implementation are well-defined. Of course, other more specialized drawing operations exist, such as ellipses or circles and arcs (actually just special cases of the ellipse). These are less common, and although the ellipse algorithm isn’t much more complex than the line-drawing algorithm, it can be implemented using short line segments.

If there’s no special hardware to enhance drawing operations, the two factors that have the most effect on drawing speed are the efficiency of the drawing algorithm and display memory’s accessibility to the CPU. As noted, CPU accessibility was already addressed in many after-market VGA products. The venerable basic drawing algorithms are probably about as refined as they’re ever likely to be.
Line drawing is almost always implemented using Bresenham's algorithm, which involves calculating a pair of increment/decrement values and an initial accumulator value, and then stepping a pointer along the X or Y axis. A pixel is plotted at each location, and depending on the value in the accumulator, the other axis pointer is advanced.

The accumulator is incremented or decremented depending on whether the minor axis pointer was incremented. The relative frequency with which the value in the accumulator crosses zero determines the line's slope. Lines can be plotted at any angle this way. Horizontal and vertical lines represent the trivial case of moving a pointer along only one axis. With this algorithm, the only highly repetitive operations are integer addition to calculate the next address in the display memory, the actual data transfers, and shifting to modify the correct display memory appears simply as a drawing engine. Another common operation is the BitBlt, which simply involves moving memory words from one rectangular region to another and possibly combining or modifying them. This may be completely within display memory or between display memory and some other memory, such as CPU memory. In many cases, display memory appears simply as a special area within the CPU address space, so there's nothing unique about such transfers. If the boundaries of the source and/or destination regions of a BitBlt don't fall on memory word boundaries, it becomes necessary to concatenate and shift the data, and possibly mask it at the boundaries.

It may be desirable to perform logical operations between source and destination data, which introduces other special cases that must be handled. Here the programmer is faced with a trade-off. If the BitBlt is to be implemented as one routine, it's necessary to place some kind of selection procedure within the innermost loop so that the right operation is performed. Even if this is only an indirect jump, the performance may suffer because it's so repetitive. The other alternative is a complete BitBlt routine for each function desired, but that's at the cost of memory space and flexibility. A third alternative—self-modifying code—is generally shunned these days because of its nasty debugging nature.

BitBlt is probably the best candidate for hardware acceleration because it affects the maximum number of pixels. To draw a diagonal line across a rectangle M by N pixels requires modifying only the number of pixels in the major axis. A BitBlt requires modifying a number of pixels equal to M times N. Naturally, the extent to which hardware enhancement is used depends on the intended market. If a designer wants to fill the entire gap between high-end PC systems and low-end workstations, the obvious target is

### TABLE 1.

<table>
<thead>
<tr>
<th>Strobe</th>
<th>Width</th>
<th>Op-Count</th>
<th>Row</th>
<th>Column</th>
<th>Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>LS</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>LD</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AO</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>LS</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>LD</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>AO</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>none</td>
</tr>
<tr>
<td>LS</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>none</td>
</tr>
<tr>
<td>LD</td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>none</td>
</tr>
<tr>
<td>AO</td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>4</td>
<td>none</td>
</tr>
<tr>
<td>LS</td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>4</td>
<td>none</td>
</tr>
<tr>
<td>LD</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>AO</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>LS</td>
<td>3</td>
<td>3</td>
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<td>2</td>
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<tr>
<td>LD</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AO</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>and so forth</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### TABLE 2.

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Source</th>
<th>Destination</th>
<th>Function bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 (LSB)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 (MSB)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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<td>0</td>
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<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1 (MSB)</td>
</tr>
</tbody>
</table>
the mid-range point for both price and performance. A more rational tactic is to improve performance as much as possible with a minimal increase in cost.

The more software functions are moved into hardware, the less performance gain is available from each hardware dollar. When implemented in hardware, only the simplest, most repetitive functions can offer significant performance gains without major cost increases. A good example is the character generator incorporated into even the most primitive display adapters. Only in recent years has the traditional hardware character generator been considered inadequate for many applications. Interestingly, the BitBLT function replaces the hardware character generator.

The BitBLT algorithm for a rectangle with corners at \((X_1,Y_1)\) and \((X_2,Y_2)\) looks something like this:

1. Calculate horizontal word count: \(\text{Abs}(X_2-X_1)/\text{word width}\)
2. Determine shift value: \(\text{Remainder}(\text{Abs}(X_{source}-X_{destination})/\text{word width})\)
3. Set right and left mask values (for nonaligned boundaries)
4. For each row,
   - Concatenate first- and second-source memory words
   - Shift concatenated data
   - Mask shifted source data
   - Combine source with destination data using desired function
   - Write new destination word

The mask-1 register masks the first word in a scan, and the mask-2 register masks the last word in a scan. The relationship between the width register and the op counter that controls the mask registers goes as follows:

At the beginning of the destination strobe, the op counter is compared with the width register. If they're equal, mask 1 will be applied to the destination data on the next output, and the op counter will be decremented. If the op counter is zero, mask 2 will be applied to both the destination data on the next output and the op counter loaded with the value in the width register.

In all other cases, the op counter will be decremented, but no mask will be applied to subsequent output. The width register should be programmed with the number of words to be transferred for the scan line, including masked words, minus one.

The op counter should be initialized to the same value. The sequence for a block of data four words wide, first and last words masked, second and third words unmasked is illustrated in Table 1.

The only remaining register that requires initialization is the function decoder. The internal ALU is actually a group of 16 one-of-eight selectors, controlled by bits from the source, pattern, and destination registers. The desired output for any given combination is programmed by setting a one or zero in the appropriate bit of the function register. For example, to implement the function \((\text{source + destination}) \times \text{pattern}\), the truth table would be used (Table 2).

The value programmed into the function register then would be \(\text{E}0\) hex. If the pattern in this example was alternating ones and zeros (say \(5555\) hex) and inverted on each successive scan, the net effect would be to combine the source and destination images and convert any solid pixel areas to a sort of halftone. A typical programming technique is to define the required function values in advance for each type of BitBLT anticipated and simply to select the function codes from a table as needed.
For intermediate memory words,
Concatenate next and previous source memory words
Shift concatenated data
Combine source with destination using desired function
Write new destination word
Concatenate previous and last source memory words
Shift concatenated data
Mask shifted source data
Combine source with destination data using desired function
Write new destination word

The inner loop handles one scan line at a time, and the outer loop steps through all of the scan lines in the block. Each scan line presents three possible cases: the first and last bytes, which may or may not have to be masked; and the intermediate bytes, which are simply shifted for alignment and written to or combined with the destination.

Much more complex is a general-purpose routine that handles copying over the destination and logical combinations, such as AND, OR, XOR. It also incorporates a second source of data for such things as background patterns. Using multiple bit planes as separate image planes or as encoders for color information further compounds the complexity.

A good hardware solution should implement the algorithm's inner loop so that the most repetitive operations are done with the most speed. A high-speed data path is necessary so that the system can use the full bandwidth of display memory. The hardware should apply masking at the boundaries automatically because this decision process is part of the algorithm's inner loop. As always in hardware design, including more functionality involves a trade-off between flexibility and complexity. As a result, designers must carefully consider the potential applications.

The VLSI Raster-Op chips incorporate most of the inner loop from the sample algorithm. Generating source and destination addresses must be done externally and can be implemented in software or with relatively simple hardware. Address generation is left as an external function because of the wide variety of memory schemes that could be used in any given display system.

In BitBLT data flow, source and destination data words are written into the chip's internal registers, and the ALU...
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output data is written back to the destination region (Fig. 1). Pattern data may be stored in an internal register, as in the VL16160 single Raster-Op ALU chip. Or it may be read from a separate block of memory, as in the VL82C164 Quad Raster-Op chip. Both ICs have direct strobes to all registers that transfer data to or from memory, eliminating the typical delays of address decoding. Both have an internal word counter that automatically activates masking at the beginning and end of a scan-line transfer.

The counter, which instantly concatenates and shifts source data to align with the destination, transfers data left-to-right or right-to-left. This enables a source block to be transferred to an overlapping destination without corrupting the source. Both can do a bit-wise combination of source, pattern, and destination data using any of 256 possible three-operand Boolean functions. Therefore, 256 functions are possible because a three-input truth table has eight possible states, and the output for each state can be defined as either true or false, thus $2^8 = 256$.

In a design example of a graphics subsystem, a single-plane, two-color display can be implemented using the VL16160 single Raster-Op ALU for simplicity (Fig. 2). The scheme could easily be expanded to use multiple bit planes and one or more VL82C164 Quad Raster-Op chips. The TMS34061 video controller was selected because it can generate X-Y addresses automatically for display memory. The control logic, which can be implemented in a programmable logic array, contains a simple sequencer to control display-memory access during BitBLT operations. Each cycle consists of source-read, destination-read, and destination-write operations.

The ALU handles data manipulation, such as shifting, masking, and logical operations. The TMS34061 video controller generates source addresses, and the host CPU calculates destination addresses. This is because in X-Y addressing mode, the TMS34061 chip updates the address after each access automatically, and the destination requires a read-modify-write operation. The modify portion of the cycle actually occurs within the VL16160, so the CPU need execute only a read, immediately followed by a write, to the same location.

The control logic must generate signals to govern the following operations: host register access to the VL16160 and the TMS34061; host access to display memory; host indirect X-Y access to display memory (where the video controller generates the address); and BitBLT cycle sequencing. The first three are fairly simple and consist primarily of address decoding. The BitBLT cycle sequencer, once started, successively generates one X-Y indirect cycle followed by two host direct cycles.

The video controller's three inputs (FS0-2) select what type of access is to be performed during a read or write cycle. The control logic simply generates the correct access code for each cycle in sequence. The video controller would ordinarily require some sort of external register or logic to generate this code anyway. So it's fairly simple to expand it into a three-step sequencer. The Raster-Op chip has a set of address lines (A0-3) that select which register to access when the CPU programs the chip. The chip also has a set of direct strobe signals (LSSTB, LDSTB, and AOSTB) that access the source input register, the destination input register, and the ALU output, respectively.

The video controller uses one Read Write input signal with a separate strobe, while the Raster-Op chip has separate Read and Write strobes. All of these signals, plus Chip Selects on both chips, should be generated by the control logic. Exactly how this is implemented depends somewhat on the type of host CPU. However, here are a few guidelines for the BitBLT cycle where the host, Raster-Op, and video controller must interact.

To initiate a BitBLT operation, a code is latched in the
control logic to indicate register access. The Raster-Op and video controller are then programmed for the intended operation. This involves setting the mask registers, op counter, and width register in the Raster-Op, and initializing the X-Y addressing registers in the video controller (see “Programming the Raster-Op chip,” p. 102).

Another code is then written to the control logic register to initialize the BitBLT cycle sequencer. The BitBLT then proceeds as follows: The CPU reads a word from display memory. The control logic causes the video controller to execute an X-Y indirect read from the source region defined by the X-Y address, and then increments the address. When the Ready signal from the video controller indicates the data is valid, it's strobed into the Raster-Op source register. The CPU then reads another word from display memory. The control logic causes the video controller to execute a CPU direct read from the destination word defined by the CPU address.

When the Ready signal from the video controller indicates the data is valid, it's strobed into the Raster-Op destination register. The CPU then writes a word to display memory at the same address. The control logic causes the video controller to execute a CPU direct write to the destination region defined by the CPU address. But it blocks the data from the CPU by disabling the 245 transceiver, enabling the output of the Raster-Op ALU instead. This read-write operation occurs at the same address in the destination. As a result, any read-modify-write instruction of the host CPU can be used, such as a register to memory add instruction. A row of pixels can, therefore, be processed by a very tight program loop. The loop would consist of a read from any display-memory address followed by an auto-increment or auto-decrement read-modify-write instruction to the destination address.

At the end of each row, the source and destination addresses are adjusted for the beginning of the next row. The BitBLT software algorithm would now look more like the following:

Calculate horizontal word count: \( \text{Abs}(X2-X1) / \text{word width} \)

Determine shift value: \( \text{Remainder}(\text{Abs}(X\text{source}-X\text{destination}) / \text{word width}) \)

Set right and left mask values (for nonaligned boundaries)

Store calculated values into Raster-Op chip

Initialize video controller mode registers

For each row,

Set initial destination pointer

For each memory word,

Read (any) display location

Read-modify-write destination word (Auto Increment/Decrement)

The design example uses the CPU to direct display-memory access but does the data manipulation in the Raster-Op ALU and part of the address generation in the video controller. As a result, the hardware can be very simple yet offer a significant speed increase over a strictly software implementation. A functional block diagram shows how control logic coordinates the CPU, video controller, and Raster-Op ALU (Fig. 3).

Three memory cycles make up the three-step BitBLT cycle (Fig. 4). The clock isn't shown because the actual number of clock cycles between events depends on the system's operating speed. The TMS34061 operates synchronously, so the clock speed must be defined in terms of the video controller's requirements. The VL16C160 is an asynchronous device. So if its minimum timing requirements aren't violated, signal timings can be more flexible, and therefore easily adapted to the video controller. An active high CPURDY signal tells the CPU when each memory cycle is finished.

Depending on the processor, another handshake protocol may be required. The Address Latch Enable (ALE) signal, a required input to the 34061 video controller, initiates each memory cycle. RDY/Hold, an output from the 34061 controller, indicates the end of each video DRAM cycle. The timing diagram shows back-to-back memory cycles that can be realized if the host CPU keeps the destination address in one of its registers and if it has a large enough instruction pipeline, or operates out of cache memory.

Unfortunately, the design example neglects one consideration. Much development for IBM-compatible PC graphics has been swayed by the need to remain compatible with a large base of existing software. But more and more users realize that older software can't fully exploit the computing power of today's machines. Speed and efficiency of graphical representation makes up a bigger part of the total useful computing power of a given machine.

Many users are bewildered by the growing numbers of hardware variations caused by the lack (or breakdown) of standardization. Designers of new equipment had to conform to de-facto standards while pressure for innovation kept increasing. Changes are in the wind, though.

And when the dust finally settles, the landscape will doubtlessly be dotted with various systems. They won't necessarily be compatible but will be targeted to their intended markets. The design example would require special drivers or fully custom software to realize its potential. This, however, would make it only marginally useful in the standard PC-compatible environment. Fortunately, as the horizon continues to broaden, hardware solutions like this will find niches.

Phil Mattison, product development engineer at VLSI Technology's Logic Products Div. studied computer science at Arizona State University and business administration at the University of Phoenix.
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For life-like 3-dimensional imaging, Cirrus Logic color LCD controllers offer technology leadership for your color products. With direct support for the latest active-matrix color LCD panels. Our controller chips do more than support your panel’s color capabilities — they enhance it with full VGA color support and a fuller color palette. To give you color so good it competes with CRT quality.

Our monochrome solutions give you displays that PC Magazine called “the stars of our VGA color-mapping tests”** with up to 64 shades of gray. And with a lower dot clock rate, your power consumption is lower than other solutions for longer battery operation.

Cirrus Logic LCD controllers are fully compatible with the popular PC video standards and will work with LCD, plasma, or electroluminescent displays.

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*Gold Crown Club Points are awarded for rooms purchased at the regular rate. Points will not
be awarded for discounted room rates.

CIRCLE 1

PC DESIGN PRODUCTS

DSP BOARD PEAKS AT 25 MFLOPS
Based on AT&T's DSP32C floating-point digital-signal processor, the AC5-AO DSP board offers a peak performance of 25 MFLOPS. Built with an ISA interface, the board includes 64 kbytes of zero wait-state RAM. It's I/O mapped and uses an on-board DMA controller to achieve ISA bus transfer rates as high as 2.5 Mbytes/s. For added flexibility, the AC5-AO features a daughterboard area that can accommodate various standard or custom daughterboard options. These include data acquisition, a serial interface, and a Codec. A 25-MHz version of the AC5-AO costs $1195 and is available now from stock. Daughterboards start at $95. Software development tools are also available.

Communication Automation and Control Inc.
1642 Union Blvd., Suite 200
Allentown, PA 18103
(215) 776-6669

INDUSTRIAL CHASSIS FEATURE 200-W SUPPLIES
A family of low-priced industrial chassis for PC-based data-acquisition and control systems features a 200-W power supply and 18-gauge steel construction. They also include a four-layer backplane that accepts any PC/XT/AT-compatible half-size card. The chassis can be either rack or panel mounted. The family includes the CH4516, CH4512, CH4510, and CH4506. They contain 16, 12, 10, and 6 slots, respectively. Prices range from $325 to $449, with a full-card option available for $100.

Ann Arbor Technologies Corp.
P.O. Box 3083
Ann Arbor, MI 48106
(313) 995-1360

CIRCLE 554
**9600-BPS MODEM COSTS UNDER $700**

The 9600etc/e external modem uses the CCITT V.32 full-duplex protocol for 9600-bps communication, V.42 error control, and V.42bis data compression—all available for just $699. By adopting the V.32 modulation, the modem ensures complete compatibility with a growing installed base of 9600-bps modems. Combining V.32 protocol with V.42bis enables the 9600etc/e to transmit and receive data at speeds up to 38,400 bps while still maintaining 100% accuracy. In addition, the modem is fully backward compatible, with modems following 4800-, 2400-, 1200-, and 300-bps standards. It contains push-button access to frequently used commands, such as speed select, modem diagnostics, auto answer, and data mode.

ATI Technologies Inc.
3761 Victoria Park Ave.
Scarborough, Ontario, Canada M1W 3S2
(416) 756-0718
►CIRCLE 555

**ADD TWO SERIAL PORTS TO A PC**

Users can now get two additional serial ports for modems, printers, terminals, or other peripherals. The Comm+232 board is a two-channel serial I/O interface for IBM PC/XT/AT and compatible computers. The board is designed specifically for users of Microsoft Windows 3.0, which allows for four communications ports.

The board has selectable addresses and a special switch-port feature that enables it to emulate two COM1 or COM2 serial ports for software requiring either of those two ports.

The switch-port software is also included. The Comm+232 is priced at $169 and is available immediately from stock.

Sealevel Systems Inc.
P.O. Box 1808
107 S. Pendleton St.
Easley, SC 29640
(803) 855-1581
►CIRCLE 556

---

**The Right Choice Could Save You $25,000.**

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HTBasic is a state-of-the-art language which gives you a number of advanced scientific/engineering features not found in other BASIC packages.

Features such as data acquisition and IEEE-488/RS-232 instrument control syntax, COMPLEX arithmetic, matrix mathematics, complete HP-style graphics, a comprehensive on-line help facility, and many more, add up to increased productivity for all levels of users.

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(801) 224-6550 Fax (801) 224-0355

CIRCLE 155

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risks associated with new product introductions.

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DC-DC Converter Transformers

PC DESIGN PRODUCTS

▼ OPTICAL MOUSE SLIMS DOWN CONSIDERABLY
An extremely small, lightweight, and accurate mouse is now available for IBM PCs and compatibles. The Little Mouse has a base resolution of 300 counts/in., variable to 30,000 counts/in. It's compatible with Microsoft and PS/2 protocols and works with Windows 3.0.

The accuracy of the two-button mouse comes from its built-in M-5 optical technology. There are no moving parts, and no cleaning, maintenance, or adjustment is ever required. The input device has an MTBF of more than 20 years. It comes bundled with four “mouseable” software applications. The Little Mouse sells for $149.95 and is available now.

Mouse Systems Corp.
47505 Seabridge Dr.
Fremont, CA 94538
(415) 656-1117
► CIRCLE 557

▼ TRANSFER DATA 100 TIMES FASTER ON A 386-BASED PC
Using the CoStar AT bus accelerator-coprocessor board with 80386-based PCs, applications can run up to 100 times faster than without the board. The accelerator's interface architecture effectively overcomes the data-transfer bottleneck that's typically associated with the AT bus.

The CoStar couples an Intel i860 RISC microprocessor to the existing 386SX chip. This combination enables the PC to run math-intensive scientific and engineering applications that previously required a supercomputer. The board permits data-transfer rates up to 33 Mbytes/ s and it's optimized to allow both CPUs to run at their maximum speed at all times. The high speed can also be attributed to the board's efficient virtual-memory capabilities and the high-speed local memory. Available now, the CoStar ranges in price from $3995 to $5995, depending on the processor speed (33 or 40 MHz) and the amount of memory included with the board.

TekStar Systems Corp.
P.O. Box 585
2415 Parrow Rd.
Middleton, WI 53562
(608) 836-7890
► CIRCLE 558

▼ REMOVABLE HARD DISK BOLSTERS SECURITY
Designed for security-sensitive computer applications or for multiple users sharing one system, the Data Express 5-1/4-in. removable hard disk drive fits into a standard half-height drive slot. The drive supports most standard interfaces, including AT, SCSI, and ESDI. The Data Express comes with a receiving frame that installs into the drive slot and a drive carrier that acts as a removable drawer within the receiving frame. A 3-1/2-in. drive can also be mounted in the drive carrier. The drive has a maximum storage capacity of 450 Mbytes, suitng it for any type of PC or workstation. Prices for the Data Express subsystem start at $315.

Kingston Technology Corp.
3023 S. Harbor Blvd.
Santa Ana, CA 92704
(714) 545-6887
► CIRCLE 559

▼ TURN GRAPHICS INTO NUMBERS
Designed for the Apple Macintosh, digiMatic is a tool that actually turns graphics into numbers. The software converts any graphical information into useful, editable numerical data quickly and easily using the computer’s mouse. The extracted data can then be saved as tab-delimited text or in the Mac’s PICT2 format for use in other programs. The tool automatically maps the screen size of any monitor in pixel units, giving programmers rapid determination of window and region coordinates for pasting into code and resources. The digiMatic software, which runs on any Macintosh computer, sells for $229.

FE! Software
4855 Finlay St.
Richmond, VA 23231
(804) 222-2215
► CIRCLE 560
IDEAS FOR DESIGN

VOLTAGE LIMITER IS ADJUSTABLE

MICHAEL J. ENGLISH
National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.

This circuit limits signal levels to specific amplitudes without using Zener diodes (a). The circuit's V-I characteristic resembles a circuit containing Zeners connected back-to-back (b). Adding two diodes removes the 8 V pk-pk limitation (c). By replacing the three resistors of the original circuit (a) with two fixed resistors and two potentiometers, users can easily adjust the limiting level (d).

SIGNAL BANDPASS FILTERS

STÉPHANE GATZKEL
Aurel Bueche University, Geneva, Switzerland.

Simple equivalent circuits of common discrete ceramic capacitors and film resistors can greatly enhance the accuracy of Spice simulations when frequencies exceed 1 MHz or the transient step interval is less than 1 µs. One equivalent circuit is for a 1/4-W film resistor (Fig. 1a). The model includes shunt capacitance and equivalent series inductance (ESL) effects. The ESL and capacitance are more products of the package size than resistor value, so the nominal values shown work for all values of 1/4-W composition or film resistors.

In a second circuit representing a ceramic capacitor, the ESL and equivalent series resistance effects are simulated (Fig. 2a). The nominal values given are good for small 100-pF types up to 0.2-in., 1-µF square types, with little loss in accuracy. PSpice net lists are generated for the two subcircuits (Figs. 1b and 2b).

The impedance characteristics of...
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2 KHz to 8 GHz from $10.45

With over 300 models, from 2-way to 48-way, 0°, 90° and 180°, a variety of pin and connector packages, 50 and 75 ohm, covering 2KHz to 8000MHz, Mini-Circuits offers the world's largest selection of off-the-shelf power splitter/combiners. So why compromise your systems design when you can select the power splitter/combiner that closely matches your specific package and frequency band requirements at lowest cost and with immediate delivery.

And we will handle your "special" needs, such as wider bandwidth, higher isolation, intermixed connectors, etc. courteously with rapid turnaround time.

Of course, all units come with our one-year guarantee.

1. EQUIVALENT TO A 1/4-W FILM RESISTOR, this circuit includes shunt capacitance and equivalent series inductance (ESL) effects (a). The higher values of resistance tend to be capacitive while the lower values act inductive at high frequencies (b).

The two macromodels for several values of resistance compare favorably with actual network-analyzer measurements on real parts. The resistors look either inductive or capacitive, depending on their value. Higher resistor values tend to be capacitive, while the lower values act inductive at high frequencies. Capacitors appear capacitive until their self-resonance point, then they become inductive.

Both models assume about a 0.1-in. lead length. If the layout has longer trace runs to the components, about 10 nH/in. of lead length should be added. It’s most convenient to use these models as subcircuits. PSpice has a parameter-passing feature that can be employed with subcircuits to pass the actual capacitor or resistor value to the subcircuit. The subcircuits can be used with standard Berkeley Spice by making a separate subcircuit for each component value handled in the simulation.

2. THIS CERAMIC CAPACITOR MODEL is simulated with the ESL and equivalent series resistance effects (a). The model’s characteristic impedance compares favorably with actual network analyzer results on real parts (b).
MAXI/PC PUTS A FRIENDLY FACE ON PCB CAD

Unlike some people, you'll be smiling when you see how easy to use new MAXI/PC is. A new, proactive user interface saves you hundreds of keystrokes in a typical design because it anticipates your next move and logically defaults to the most likely action. MAXI/PC's OSF/Motif® style interface has clear, logical menus integrated across all functions. It's easy to learn and much easier and more productive to use than the competition.

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MAXI/PC gives you an incredible amount of design power for the money. Rich with features, it's capable of handling multi-layer, double-sided, surface mount boards. You get schematic capture, layout, automatic routing, and manufacturing outputs. All backed by a 30 day, no questions, money back guarantee. All for $995.

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- Automatic part/component replacement
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Racal-Redac is the only EDA vendor to offer a smooth growth path, with data migration from MAXI/PC, to the more powerful PC-based CADSTAR, to high end, workstation-based VISULA EDA. Make yourself smile, get MAXI/PC.

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Fax: (508) 692-4725

CIRCLE 111
If you're trapped trying to design ASICs with vendor-specific tools, it's time to make a break— for Oki. Because at Oki, we take a "customer-friendly" approach to ASIC design by supporting the range of industry-standard tools you're used to working with.

Verilog, for example, is our in-house simulator, providing high-quality customer-to-Oki and Oki-to-customer design interface. So you enjoy shorter design and verification cycles and the assurance that your design will work.

Is your ASIC design platform workstation- or PC-based? No matter. With Oki, you get across-the-board hardware, software, and operating system support for DAZIX, Mentor, Valid, Viewlogic, and others.

Just choose the environment you're familiar with, and start designing. There's no relearning effort required.

If you're ready to escape the limitations of vendor-favored tools, Oki is ready to set you free—with complete design support: 24-hour, fully-equipped, state-of-the-art design centers. Customer-compatible tools. A true 0.8µm drawn family of SOGs for next-generation products. Industry-standard JEDEC metric packages. Data books, design guides, and more.

Make a break for the design freedom you've been longing for. Call 1-800-OKI-6994.

Apollo, Cadence, DAZIX, DEC, Digital, DNIX, DOMAIN, GED, HP, IDEA, LOGICIAN, Mentor Graphics, PC-DOS, RapidSM, Sun, Sun OS, Synopsys, ULTRIX, Valid, ValidSIM, Verilog, Viewlogic, and Workview are trademarks of others.
## ASIC Tools?

### Oki ASIC Design Tool Support

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<thead>
<tr>
<th>Vendor</th>
<th>Platform</th>
<th>O.S. &amp; Application</th>
<th>Design Kits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cadence</td>
<td>Sun-4</td>
<td>Sun OS 4.0.1, Verilog 1.5C</td>
<td>SDG: 0.8µm</td>
</tr>
<tr>
<td>DAZIX</td>
<td>LOGICIAN</td>
<td>SUN-3, SUN OS 4.0.1</td>
<td>GA: 1.2µm, 0.8µm, 0.6µm</td>
</tr>
<tr>
<td></td>
<td>Sun-4</td>
<td>Digital Application 6.1, Digital Application 6.3</td>
<td>SC: 1.2µm, 1.0µm</td>
</tr>
<tr>
<td>Mentor</td>
<td>HP/Apollo</td>
<td>GRAPHICS, DOMAIN/OS 10.1</td>
<td>GA: 1.2µm, 1.0µm, 0.8µm</td>
</tr>
<tr>
<td></td>
<td>Sun-4</td>
<td>IDEAS, IDEA Series 7.0</td>
<td>SC: 1.0µm, 1.2µm</td>
</tr>
<tr>
<td>Synopsys</td>
<td>Sun-4</td>
<td>OASIS, OASIS 4.0.3</td>
<td>SDG: 1.0µm, 0.8µm, 0.6µm</td>
</tr>
<tr>
<td></td>
<td>Sun-3</td>
<td>Interface to Mentor, Valid, Viewlogic</td>
<td></td>
</tr>
<tr>
<td>Valid</td>
<td>Sun-4</td>
<td>SUN OS 4.0.1, GED, ValidSIM, RapidSIM</td>
<td>GA: 1.2µm, 0.8µm, 0.6µm</td>
</tr>
<tr>
<td></td>
<td>Sun-3</td>
<td>GED, ValidSIM, RapidSIM</td>
<td>SC: 1.5µm, 1.2µm</td>
</tr>
<tr>
<td>DEC Station</td>
<td>ULTRIX</td>
<td>3100, ValidSIM, GED</td>
<td>GA: 1.2µm, 0.8µm, 0.6µm</td>
</tr>
<tr>
<td>Viewlogic</td>
<td>Sun-4</td>
<td>SUN OS 4.0.3, Workview 4.0</td>
<td>GA: 1.2µm, 0.8µm, 0.6µm</td>
</tr>
<tr>
<td>PC386</td>
<td>DOS 3.3</td>
<td>Workview 4.0</td>
<td>GA: 1.2µm, 0.8µm, 0.6µm</td>
</tr>
</tbody>
</table>

**OKI Semiconductor**

785 North Mary Avenue
Sunnyvale, CA 94086-2909

CIRCLE 128
When developing BIOS for PC/XT (ISA) systems, having a 64-kbyte block of nonvolatile memory above DOS DRAM would be useful. One low-cost approach to obtaining this block is to remove one chip of a 64-kbyte block of memory while leaving an identical block above intact. Many full motherboard versions of the PC/XT are configured as:

- 4th bank - 64 kbytes
- 3rd bank - 64 kbytes
- 2nd bank - 256 kbytes
- 1st bank - 256 kbytes

When the third bank of 64-kbyte chips is disabled by removing one chip from its bank (not a parity chip), the fourth bank is still refreshed as though nothing had happened. Upon boot up, the resident BIOS checks memory and hands the system over to DOS as a 512-kbyte DRAM machine. Thus, the fourth bank of DRAM is available as pseudo-static RAM and can be read from or written to using a DOS version that contains the Debug program. It will survive all but a power reset.

When the prototype BIOS is compiled, assembled, linked, and turned into a binary image, the Debug program should be used to load and jump to the new BIOS. Using this method, EPROMs need only be burned to replace the resident BIOS after the many revisions produce an acceptable BIOS. The time-consuming task of burning EPROMs for each cycle of the BIOS development is thus avoided. This concept of having memory available above DOS DRAM applies equally well for any embedded control program that requires less than 64 kbytes of executable code.

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Almost everything about Sun Microsystems’ future workstations is under wraps.

Everything, that is, except that Sun is using Mentor Graphics IC design tools to create revolutionary chips with record levels of performance.

Workstation details will have to wait for the product announcements, which won’t be long since Mentor Graphics IC design solutions accelerate the entire IC design process — from concept to layout to verification. These solutions boost productivity to help market leaders like Sun stay one step ahead of their competition.

Mentor Graphics delivers the most powerful tools and the most flexible design environment, all created to the industry’s most stringent software standards. The proof of our technology leadership lies in hundreds of CMOS, bipolar and GaAs chips and tens of thousands of custom and ASIC library cells. Created by organizations like Apple Computer, Motorola DSP Operations, Thomson TMS, Texas Instruments, and, of course, Sun. All using Mentor Graphics IC design tools.

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MARKET FACTS

Process-control jobs are absorbing more and smart pressure transmitters. As a consequence, the market is booming for these smart devices, which include self-diagnostics, electronic re-ranging, and, for some, digital outputs. Prices are dropping too—some smart devices now go for less than traditional transmitters. These predictions come from Venture Development Corp.

The Natick, Mass., market researcher says the total U.S. market for pressure sensors, transmitters, and switches amounted to $1.05 billion last year. In terms of market segments, the pressure-switch sector shipped $233.7 million worth of product last year. The pressure transducer and transmitter sectors combined for a total of $827.9 million. Another $13.6 million in switches was exported; $280.5 million worth of transducers and transmitters was shipped last year.

Smart devices snared 30% of the market in 1990, up from 20% the year before. And the market for smart transmitters is expected to grow 12.2% a year over the next five years. U.S. sales of pressure transmitters for process control amounted to $312.4 million last year. About half of the pressure transmitters used variable capacitance. Another 10% of the transmitters relied on ion-implanted semiconductors with this figure expected to increase; nonetheless, semiconductors can be used only in jobs below 150°C (300°F).

EYECATCHER

As ICs get smaller and faster, their packaging is changing. Multichip modules will account for $18 billion in revenues in 1995, forecasts market researcher Dataquest. By the year 2000, MCMs will house one-third of ICs while throughholes will account for just 3%.

WHERE PRESSURE SENSORS ARE GOING

<table>
<thead>
<tr>
<th>Component pressure sensors</th>
<th>$80.4 million</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure switches</td>
<td>$233.7 million</td>
</tr>
<tr>
<td>Non-process pressure transducers</td>
<td>$425.3 million</td>
</tr>
<tr>
<td>Process pressure transmitters</td>
<td>$312.4 million</td>
</tr>
</tbody>
</table>

1990 U.S. consumption $1051.6 million

Source: Venture Development Corp.

DID YOU KNOW?

... that world semiconductor shipments should increase 12.5% this year, on the heels of a scant 1.5% increase in 1990. The world market should amount to $55.7 billion in 1991. Part of the momentum comes from countries like Hong Kong, where electronics exports are expected to increase 7% in 1991, compared with 5% last year. Orders are up 10% compared with the same period last year.

SIA, Hong Kong Economic & Trade Office

... that the typical U.S. manufacturer invests 20 to 25% of its operating budget finding and fixing mistakes.

BusinessWeek

... that in fiscal 1988, the U.S. spent 0.2% of its research funds on industrial technology, compared with 4.8% by Japan, and 14.5% by West Germany. That year, the U.S. spent 65.6% of its research money on defense, compared with 48% by Japan and 12.5% by West Germany.

U.S. Council on Competitiveness Report

... that 26% of U.S. companies reported having computer viruses on their PCs as of January. In the same quarter of last year, about 10% of companies reported a computer virus.

Certus International Corp.

... worldwide, compatible high-definition TV should be a reality by the year 2010, according to 70% of engineers surveyed by the Gallup Organization for the IEEE. About 38% said that superconductivity would find practical application in power and transportation by 2010.
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One of the H4C Series' system-level design features is the Customer Defined Architecture. CDA enables versatile, efficient system-level design in which large, fully-diffused architectural blocks like RAM, and in the future, microprocessors and arithmetic functions, are embedded in the Array. High-speed, user-configurable RAMs are structured to easily integrate with user-defined BIST circuitry. Optimized SRAM is available in several hundred thousand single and dual port configurations of up to 256K bits.

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Which technical books are the most popular in Silicon Valley?

**ELECTRONICS:**

**COMPUTER SCIENCE:**

This list is compiled for *Electronic Design*’s Quick Look section by Stacey’s Bookstore, 219 University Ave., Palo Alto, CA 94301; phone (415) 326-0681; fax (415) 326-0693.

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**QUICK NEWS: THE PROFESSION**

**American Engineer**, a newsletter from the American Engineering Association, aims to boost engineers’ status as professionals and promote engineering employment. The AEA has a goal of 50,000 members by the end of the year. Regular membership is $20; professional membership, $50; and sponsoring membership, $100. All members receive a copy of *American Engineer*, the AEA’s monthly publication, which has articles on employment and publishes engineers’ opinions. For more information or to join, contact the AEA, P. O. Box 820473, Ft. Worth, TX 76180-0473.

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**KMET’S KORNER**

...Perspectives on Time-to-Market

**BY RON KMETOVICZ**
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458, fax (408) 253-6085

Now that the team has modeled its concurrently engineered new product-development effort, how does it know if the plan is any good? To help answer this question, I’ve developed a graphical technique that’s very useful.

To apply the technique, you simply sort the project’s database and arrange task information by completion date. In effect, you produce a to-do list for the entire project from the task data, arranged by the date work should be completed. The next step is to produce a graph of this information called the KMET chart. The chart is produced by having time on the X-axis and cumulative task completion on the Y-axis (see the figure).

In the chart, 63 tasks exist over about 61 weeks. Besides cumulative task count over time, the graph provides key milestone information and, possibly most important, discloses information about the underlying network through the slope of the line. The entire plan is graphically summarized on a single piece of paper. As you review the figure, can you see problems with the plan being represented by this chart?

In the next column, I’ll discuss using the KMET chart as a plan analysis and decision-making tool. In the meantime, produce a KMET chart of your own for a project you have in a database and then study the results.

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**QUICK NEWS: EDUCATION**

More than other occupations, engineering is a learning profession. Engineers have to become and remain students. Rapid changes in technology amplify the need to keep learning. Courses on videotape can be rented or purchased. One source is the Office of Continuing Engineering Education at the University of Illinois in Urbana-Champaign. Each course has a recommended text; printed notes supplement many courses. Courses may be previewed free for two weeks. Write for a free catalog to the Office of Continuing Education, University of Illinois at Urbana-Champaign, 422 Engineering Hall, 1308 W. Green St., Urbana, IL 61801; (217) 333-6634.
**NAME THE LEADING VENDORS OF 32-BIT CISC MICROPROCESSORS**

- **Motorola**: 68.6%
- **Intel**: 70.8%
- **National Semiconductor/Fairchild**: 69.6%
- **Texas Instruments**: 62.7%

Legend:
- Yellow: Current 32-bit CISC users
- Red: Plan to use 32-bit CISC in next 12 months
- Blue: All users, designers

Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

**OFFERS YOU CAN'T REFUSE**

- **PLDshell**, a software tool for programmable logic design, is free from Intel Corp. The software supports Intel's microcomputer PLDs and other standard devices. PLDshell is a menu-driven shell under which editors, compilers, and programmer software can be run. The software also includes the company's integrated compiler, PLDasm, which compiles designs for microcomputer PLDs using an expanded syntax compatible with PALASM2. PLDasm, which can import other design files, has functional simulation to enable engineers to spot design mistakes early.

Available at the end of this month, PLDshell can be obtained by calling a local Intel sales office or the company's literature center at (800) 548-4725. Or write for Intel Literature Packet IP78, P.O. Box 7641, Mount Prospect, IL 60056-7641. Outside the U.S., contact the nearest Intel sales office.

- **Johns Hopkins University** is offering a $10,000 grand prize for the best ideas, systems, devices, or computer programs to help disabled people. In addition, more than 100 other awards will be given. The contest categories are employment, independent living, education, and leisure. As a follow up to the competition, the university will act as a liaison with manufacturers to have winning entries commercially produced and into the hands of those who need them.

Entry deadline is Aug. 23, 1991. For more information, write to Personal Computing to Assist Persons with Disabilities, P.O. Box 1200, Laurel, MD 20723.

- **Free disk** demonstrates software that can specify, modify, and check timing requirements for digital circuits. With Chronology Corp.'s TimingDesigner, engineers can solve timing design problems by creating and analyzing timing diagrams. These diagrams, created before a schematic is drawn, can save many hours in the design phase and help avoid costly design errors that crop up when manufacturing begins. Contact the company at 2849 152nd Ave., Redmond, WA 98052-5516; (202) 869-4227.


- **Free seminars** on designing with Intel Corp.'s 80186 embedded processors will be held in two dozen U.S. cities from May 21 to June 27. Design examples will be given for a low-cost 16-bit external bus 80186 SA/SB. Seminars run from 9 a.m. to 12:30 p.m. For cities and dates, call (800) 548-4725.
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What's All This "SMWISICDI" Stuff, Anyhow?

A long time ago, I went out to dinner with Dave Ludwig, an old friend of mine from Massachusetts. We went to a fancy Italian restaurant. After we had ordered our entrees, the waiter asked, "Would you like a salad? I declined, but Dave said he would like one. "What would you like in your salad?" I asked, "Would you like a salad?" Dave said lettuce and tomatoes.

In a few minutes the salad arrived. Yes, it had lettuce and tomatoes. It had three kinds of lettuce, and tomatoes and chick-peas and croutons and onion slices and green onions and Italian cherry peppers and slices of hard-boiled egg, and three kinds of salad dressing on the side. I sat there with barely suppressed astonishment, and Dave just sat there with a quiet, resigned smile. After the waiter departed, Dave explained: There was no point in complaining or griping or hollering, because at the best, the manager or the headwaiter would just come over and say, "Hey, you don't have to eat anything you don't want, and you don't have to pay for anything you don't want, so, what's your complaint? Show Me Where It Says I Can't Do It." And he explained that he was an aficionado of these kinds of stories, which we will of course abbreviate to "SMWISICDI."

He pulled a faded clipping from his pocket. The newspaper story was about the advantages of home ownership. "If you own your own home, you can play the piano at midnight." I thought about it. I said, "Dave, I can't play the piano worth a darn. But this story says that I can play the piano at midnight if I own my own house."

Dave smiled and agreed. "You just think you can't play the piano. But, have you ever tried at midnight?" I had to admit that I had not. But, one of these days, I will try playing at midnight, to see if I'm any better than at any other time. What I suspect is that at 12:00:02, I'll suddenly be a rotten pianist again.

Now I, too, have gotten interested in SMWISICDI stories. In fact, last week I mailed 5 ounces of SMWISICDI stories and clippings to Dave. For example, I clipped out a story about how the Israeli Army solved the problem of what to do when Palestinians throw stones at the soldiers. The Israeli Military invented an automated stone thrower to retaliate. An eye for an eye, a tooth for a tooth—and a rock for a rock? What if Jack Anderson got wind of this, and confronted the Joint Chiefs of Staff? They would just tell him, "Show Me Where It Says I Can't Do It."

Last week, Wanda Garrett, our senior applications engineer for amplifiers and regulators, got a phone call from an unhappy customer. He had used one of our ICs to design a switching regulator, and it didn't work well at all. The output had glitches and burps and excessive ripple and noise. The regulation was poor, the loop stability was rotten, and the efficiency wasn't even very good.

After a lot of inquiry, Wanda discovered that this person had built up the switcher on one of those solderless breadboards. OHHH!! Patiently, Wanda explained, that is exactly what you expect when you use one of those solderless beasts. The inductances are awful, the capacitances will cause crosstalk between adjacent buses, and if you try to build a switching-type regulator, of course it will work badly. And the customer replied, "SMWISICDI."

Now, Wanda was a little taken aback. She had to admit, of all the things that we might have told people they should not expect to work, this was one that we didn't specifically warn against. But, to put the shoe on the other foot, she asked, "Where does it say you can do this?" And the customer replied that in the solderless breadboard's promotional brochure, it says, "Ideal for high-frequency and high-speed/low-noise circuits."

Wanda observed that was probably not quite true—neither for linear circuits, fast digital circuits, fast ADCs, nor switches. Then she pointed out to the customer that the LM2575 data sheet does spell out: "As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients that cause problems. For minimum stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. Single-point grounding or ground-plane construction should be used for best results."

So we really did tell every customer that you need a good layout, right in the data sheet. Of course, if the customer believes that solderless breadboards are really great for high-frequency circuits, then we have a problem—which Wanda was able to resolve and explain. The solderless breadboards do cause many troubles.

First of all, most fast ICs, whether linear or digital, require a good ceramic power-supply bypass capacitor, right close to the IC. But with those long buses inside a solderless breadboard, it's hard to get a bypass capaci-
tor with less than 3 or 4 inches of loop. That won't help a switcher or any other fast circuit. Then, the capacitance between adjacent buses—typically 2 to 4 pF, depending on the size—is going to cause stray coupling that will probably make the circuit unhappy. That's my experience. Furthermore, when you have a switching transistor turning off, its collector or drain can easily slew at 600 V/μs or more. If your "catch" diode is spaced more than an inch from the inductor and transistor, the L di/dt can cause dozens of volts of overshoot, which may overstress the switching transistor (exceeding its voltage ratings), not to mention generating some horrible spikes in the air.

And those white slabs—they are not Teflon. They aren't polystyrene or polyethylene, either. They are made of nylon, or something similar, so the leakage can be pretty bad on a warm or humid day. Even worse, if you push a whole lot of wires into those little solderless connectors, the little scraps of solder will get scraped off until there's a whole pile of solder scraps hidden inside. Then they can start making intermittent short-circuits between adjacent buses—won't that be fun to troubleshoot.

So Wanda explained all of these reasons not to use a solderless breadboard for making a switcher. She sent the customer a little PC board that was neat and compact to help him get a prototype of the circuit working—one of the LM2575 "Simple Switchers." Note, we normally think that these "Simple Switchers" cannot miss—they're very easy to apply. But, if you try to build it on a solderless breadboard, even a simple circuit can be hurt—ruined—by the strays of a poor layout. Simple, yes. But foolproof and tolerant of a truly bad layout? No.

Then she warned the rest of us Applications Engineers that customers might be having trouble when using solderless breadboards, ultimately complaining "SMWISICDL." I'm just passing on this warning to you readers.

Finally, Wanda said she was going to try to put a disclaimer in our linear databooks and applications handbooks, that the "solderless breadboards" are unsuitable for any applications other than medium-speed, medium-impedance-level, and medium-precision circuits. It may sound silly, but I know that she'll find a way to put in a caution flag where it's appropriate. I mean, Wanda is the Czarina of Linear Data Books. She can put anything she wants in there. Show Me Where It Says She Can't Do It!

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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As the need for digital-signal-processing (DSP) functions within a desktop computer increases, so does the need for closely coupling the host CPU with coprocessor cards and digital-signal processors on motherboards. This increased DSP need is caused by a host CPU having to handle everything from modem communications to multimedia presentations. Tight coupling, however, may limit system expandability and may not even let the DSP chip use the system’s resources.

By adding a second system bus dubbed the Media-Link, Spectrum Signal Processing overcomes the bottlenecks in most DSP systems. The new bus forms a high-speed interconnection system that permits DSP chips, a host processor, and I/O peripherals to communicate together over a high-speed bus, independent of the host-system bus. As a result, multiple processors can be inter-
connected to form systems in which processing power or I/O functions can be added to, much as memory is added to a computer. Media-Link also allows multiple processors from different manufacturers to communicate over a common link.

The heart of Media-Link is a custom chip designed by Spectrum called the Media-Link Controller (MLC), which transfers 16-bit-wide data at sustained rates of 66 Mbytes/s. In addition to controlling the interconnection scheme, the first version of the chip matches the control signals of a host Intel 80386 32-bit processor, or the Texas Instruments 32-bit TMS320C31 floating-point DSP chip (selectable via a control pin). The on-chip logic permits a direct connection to the desired processor and keeps the interface very simple—a two-chip solution results if no off-chip memory is needed. The noncompeting message-passing communication protocol used by the chip provides predictable responses for real-time applications—a critical requirement for many industrial control or measurement systems.

Any subsystems connected to an MLC can access the resources of any other system tied into the 25-line (16 data and 9 control lines) Media-Link bus. Consequently, if multiple processor nodes are interconnected, any or all nodes can share a hard-disk drive that may reside on the host-processor node, or a peripheral that may be located at another node. That allows each block to communicate with any other as if all processor blocks are peers, rather than master/slave units.

Two MLCs can be directly connected to each other over their CMOS interface buses if the propagation delay between the two chips, after accounting for loading impedances, is much less than the duty cycle of the Media-Link clock. To increase the distance between MLCs, or the number of MLCs that can be interconnected, bus-transceiver-logic (BTL) buffers should be used to create a Media-Link backplane. The BTL transceivers allow data to be transferred across the backplane at higher data rates than TTL circuits, without the reflection propagation delays that are normally associated with a TTL bus.

The bus thus provides a high-speed interprocessor communication path that allows data to be copied from a source processor’s memory or I/O space to a destination processor’s memory or I/O space. The transfers are done under the control of the MLCs, which put their respective host processors into a hold state, and then take over control of their host processor’s buses. Once the two MLCs control the buses, they will transfer data from the source processor’s memory or I/O space to the destination processor’s memory or I/O space.

The MLC will be incorporated into a family of board-level products, the first of which, the DSP/PC, will be a combination digital-signal processor and personal-computer equivalent. The MLC will also be sold as a standalone component.

The DSP/PC is a single-board computer intended for PC/AT industry-standard-architecture (ISA) passive backplanes. The card includes standard peripheral interfaces for hard- and floppy-disk drives, a keyboard, and a serial port, as well as a real-time operating system and Microsoft Windows 3.0 drivers for quick startup and relatively easy programming.

All data-transfer overheads are managed by the MLC. That leaves the host and DSP nodes to go about processing data independent of each other. Based on the memory-to-memory transfer of packetized data...

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**Diagram:**

- **TMS320C31 floating-point digital-signal processor**
- **Media-Link controller**
- **BTL transceivers**
- **Media-Link controller**
- **Cache**
- **8 Mbytes (system DRAM)**
- **16-bit ISA-bus interface**
- **Optional 80387**
- **25-MHz 80386**
- **2 Mbytes (static RAM)**
- **Serial port**
- **10 Mbytes/s**
- **66 Mbytes/s**
- **SCSI controller**
- **SCSI connector**
- **Floppy-disk drive connector**
- **Floppy-disk controller**
- **Keyboard, communications, printer, and interface logic**
- **Serial I/O**
- **Keyboard**, **communications**, **printer**, and **interface logic**

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2. **THIS 80386-BASED PC/AT CARD** with floating-point DSP capability employs two Media-Link Controller chips, so that the DSP chip can talk to the PC. The two controller chips on the DSP/PC card also provide a 66-Mbyte/s gateway for further expansion.
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CIRCLE 92
Features are particularly handy for than most commercial buses, like the one chip need not share the memory a single-board ISA computer system. They also let each DSP chip have as ed ISA, VMEbus, and Multibus II. A

The on-chip logic handles all func- involve tying a host computer to mul­
termination, and error detection. These features are particularly handy for real-time applications of DSP chips. They also let each DSP chip have as much local static RAM as needed— one chip need not share the memory with another.

The MLC, which is a two-port de­vice, ties a CPU or DSP chip to the Media-Link bus. The MLC thus serves as the common gateway to the bus. When a data transfer oc­curs, the originating processor sets up a description block with the pa­rameters of the data to be sent, in­cluding the destination processor, a pointer to the data, and the length of the data block. The MLC is then acti­vated, the processor bus stops, and the data is transferred to the destina­tion processor under control of the MLC’s DMA circuitry. The destina­tion MLC then responds, notifying its processor that data has been re­ceived, as well as the data’s origin, location, and length.

The custom MLC chip keeps sys­tem component count to a mini­mum—all that’s needed is the MLC, the digital-signal processor, and the desired off-chip memory and peripheral functions. In addition to the CMOS logic used for the MLC, the bus interface is implemented with backplane transceiver logic so that data rates over the bus can keep up with the data rates for real-time full-motion video—an essential element of a multimedia system. The chip (and thus any board that includes it) should support real-time DSP operating systems, such as the open-sign­al-processor architecture (OSPA) from Spectron Microsystems Inc., Santa Barbara, Calif., and the Windows 3.0 user interface. A number of off-the-shelf applications, written under OSPA, will soon be released for fax, modem, JPEG (Joint Photographic Experts Group), and MUSICAM (masking pattern adaptive universal subband integrated coding and -multiplexing) control. MUSICAM is the audio portion of MPEG (Moving Picture Expert Group).

A typical MLC chip application will involve tying a host computer to mul­tiple DSP chips, maximizing system throughput. At 66 Mbytes/s, the transfer rate of Media-Link is faster than most commercial buses, like the PC/AT ISA, Micro Channel, extend­ed ISA, VMEbus, and Multibus II. A typical host system might consist of a single-board ISA computer system with a CPU, a DSP chip, and two MLC chips (Fig. 2).

The computer portion incorporates a 32-bit PC-compatible proces­sor, such as an 80386 (and optional 80387), with 8 Mbytes of dynamic RAM and cache. It also contains an MLC chip, a BIOS ROM, a dual flopp­py-disk controller, and a Small Com­puter System Interface controller. In addition, a real-time clock, key­board, parallel, and dual serial inter­faces are included. The DSP portion might consist of the 320C31 DSP chip, up to 2 Mbytes of local static RAM, a serial port, and a local expan­sion bus, the DSP-Link. Spectrum has provided DSP-Link for several years as an inexpensive way to add medium-speed (10-Mbyte/s) peripheral functions. The two MLC chips are connected directly to each other; they don’t have to communicate through the BTL buffers. The 66­Mbyte/s bus is tapped off the chip-to-chip connections, with BTL trans­ceivers supplying the high-speed buffering.

Able to run any PC software, the DSP/PC card can operate as a DOS­compatible system running Micro­soft Windows 3.0, while the DSP chip could run the SPOX operating system developed by Spectrum Micro­systems. The SPOX system is one el­ement of Spectrum’s OSPA, a frame­work for DSP applications that the company is trying to establish as a standard software interface. Applications developed under OSPA will run unaltered on Media-Link-based hardware. Some application soft­ware packages now being developed include multimedia programs for JPEG and MUSICAM, a Windows 3.0 interface, and AutoCAD.

To handle some of the multimedia applications, Spectrum defined a multimedia adapter that combines a VGA graphics output plus a TMS320C31 DSP chip with analog-to-di­gital and digital-to-analog converters for audio input and output. The card will plug into the ISA bus and pro­vides a Media-Link expansion bus. Also coming is a Media-Link DSP expansion card that contains four ad­ditional TMS320C31s, each with up to 1 Mbyte of local static RAM. The card provides up to 132 MFLOPS of computing power.

Additional hardware being de­veloped at Spectrum includes a 386 motherboard adapter that permits users to retrofit exiting PC/AT 386 motherboards with Media-Link ca­pability. The adapter plugs into the 80386 socket and the 80386 drops into a socket on the adapter card. That gives the MLC access to all of the CPU’s signals and enables the con­troller to provide a local 66-Mbyte/s bus. A Media-Link prototyping card that contains the 320C31 portion of the DSP/PC card is also in the works. It has a prototyping area instead of the 80386 PC/AT logic.

**Price and Availability**

Samples of the Media-Link controller chip will be available in the early fourth quarter. The chip, to come in a 144-lead plastic quad-sidet flat package, will sell for about $50 in 1000-unit lots. For large­volume users, licenses to manufacture the chip can be purchased. The DSP/PC 80386­based card will be available in the same time frame, debuting at about $3500 in small quantities. The other cards will be released in the fourth quarter of this year and through the first half of 1992. Soft­ware from Spectrum will be available in the fourth quarter of this year.

**How Valuable?**

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**CIRCLE**


[512] **Spectrum Microsystems Inc., 600 Ward Dr., Santa Barbara, Calif., 93111; David Wong, (805) 967-9563. CIRCLE 512**

**E L E C T R O N I C  D E S I G N**

MAY 9, 1991
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The result has been a number of object-oriented, icon-based programming tools that let designers concentrate more on the test at hand and less on the programming task. The Hewlett-Packard visual engineering environment (VEE) software takes this concept to the ultimate level, completely freeing users from the need to know any high-level-language syntax, semantics, or rules. Designers merely link the HP VEE icons into an intuitive block diagram on the display. The software then executes the completed block diagram (see the figure).

The VEE consists of two products aimed at a wide range of computer-aided prototyping, experimentation, and testing. HP VEE-Engine is general-purpose software that analyzes and presents data either collected from a file or generated mathematically. An expanded version, HP VEE-Test, is intended specifically for instrument control. It includes icons that allow data collection from more than 170 HP instruments, as well as from non-HP instru-
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<td>R90</td>
<td></td>
<td>R87</td>
<td></td>
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<tr>
<td>R79</td>
<td></td>
<td>R88</td>
<td></td>
</tr>
<tr>
<td>R72</td>
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<td>R89</td>
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<tr>
<td>R75</td>
<td></td>
<td>R29</td>
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<tr>
<td>R80</td>
<td></td>
<td>R85</td>
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<td>R86</td>
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☐ Bill my company and include postage and handling charges. My purchase order is enclosed.

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*U.S. prices only CIRCLE 189

Now, high-speed AGC is easier than ABC.

Take the new CLC520, add ±5V and two resistors, and you have a total high-speed AGC solution for fast variable-gain applications. 160MHz small-signal and 100MHz gain-control bandwidth—with a 40dB range from max. gain—give you a very flexible solution in a single 14-pin DIP.

CIRCLE 190

Modular amplifiers... ready to go.

For bench or system use, this family of de-coupled modular amplifiers gives you complete amplifier solutions. Including PMT amps, cable drivers, post-amps, very-low-distortion amps, or amps with gain and I/O impedances that you can select.

CIRCLE 191

** ENGINEERING SOFTWARE **

HP tried to make the VEE software as easy as possible to use, while still maintaining functionality. The result is a comprehensive set of icons chosen to simplify data collection, analysis, and presentation. Users choose from among engineering elements, such as virtual sources, accumulators, and timers, and then define the data flow by linking these elements into a block diagram. All icons are named, making them easy to recognize and intuitive to use.

“Overhead” steps are eliminated. For example, the details of creating, appending, opening, reading, writing, and closing a file are handled transparently by the VEE software, rather than requiring a separate icon for each operation. In addition, the procedure for sending sequences of strings and numbers to an instrument is simplified. Instead of converting all numbers to strings and concatenating the whole sequence, users specify the numbers and strings in one transaction. The VEE-Test then converts and concatenates the numbers automatically.

To further help users who are unfamiliar with programming techniques, HP VEE accommodates a large number of interchangeable data types. In addition, all objects accept any data type without user intervention. For instance, users can supply a time-domain waveform to a spectrum-display icon, which needs frequency-domain data. HP VEE will automatically run a fast Fourier transform on the input to make the conversion.

Users can collect data from HP-UX files, standard in (a Unix communication method), communication programs, and programs written in C, Pascal, and Fortran (HP-UX is based on and fully complies with AT&T's Unix system). HP VEE-Test accepts data from HP Basic/UX programs and named pipes (Unix data transfer techniques), in addition to instruments. During setup or when external sources are unavailable, the software's internal data generators can supply simulation signals. The HP-IB (IEEE-488), RS-232, and general-purpose input-output (GPIO) interfaces are supported.

Analysis icons include most math functions, calculus, regression analysis, probability, statistics, and others. Some of the engineering functions available are FFTs, data filtering, digital-signal processing, and distributions.

To increase flexibility in more complex applications, HP VEE has several flow-control objects, including repeat and conditional objects. Moreover, standard objects can be grouped into customized modules called UserObjects. Users can choose from XY or Y plots, strip or polar charts, complex planes, waveforms, and several frequency plots to present their data.

In the debugging mode, four features help users troubleshoot their applications. Line Probe shows which objects are connected by a specific line, as well as the type and value of data flowing through the line. Show Data Flow and Show Execution Flow allow users to see the data flow or the sequence in which objects are executed. Finally, users can set breakpoints at specified points to stop execution for examination.

The completed application can be viewed in two ways. The detail view shows every icon. The panel view lets users display only a desired subset of icons—input and output devices, for example. This feature creates a simplified interface that can be secured to prevent unauthorized access.

HP VEE-Engine and VEE-Test run on HP 9000 Series 300 or 400 systems with HP-UX 7.0 and X Windows. Minimum RAM needed is 8 Mbytes.

** PRICE AND AVAILABILITY **

HP VEE-Engine (HP E2100A), the general-purpose analysis and presentation software, costs $895. HP VEE-Test (HP E2110A), which adds instrument I/O and control functions, is priced at $5000. Delivery is in 4 weeks. Hewlett-Packard Co., Measurement Systems Operation, P.O. Box 301, Loveland, CO 80539; (800) 752-0900.

CIRCLE 513

** HOW VALUABLE? **

HIGHLY 547
MODERATELY 548
SLIGHTLY 549
Introducing the wave of the future. The industry’s first and only low-noise GAL devices.

Silencing device noise with our new GAL® Quiet Series™ family.

The tide of events for CMOS-based logic is sure to change course with the introduction of our new GAL Quiet Series devices. Because now you can design in high-speed logic devices without having to design out noise.

Through our advanced proprietary circuitry, we keep noise to a bare minimum. Our GTO™ (Graduated Turn-on Output) circuit, which retards the output buffers, results in smoother edge rates, diminished output undershoot, and greatly reduced ground bounce (V_{OLP} max of 1.5V).

What’s more, these devices utilize unique ground and power buses, which effectively isolate inputs from output noise and improve dynamic threshold.

Minimizing system noise.

Not only will our high-speed GAL QS devices improve your system performance, they’ll reduce your overall system noise. And that means extraneous noises like Electromagnetic Interference (EMI), crosstalk, and ringing, the effects of which often result in false clocking.

Delivering higher speeds at 1/2 and 1/4 the power.

What more would you want in a GAL device other than high speed and low noise? Our answer is less. That’s why we offer reduced-power versions of our 15ns devices. Which means now you can get half- and quarter-power GAL devices — in either 20- or 24-pin DIP and PLCC packages — that draw a max I_{CC} of 90mA and 55mA respectively at 15MHz.

Building on our Quiet Series heritage.

When we designed our low-noise GAL devices we talked to the experts. National’s team of ACMOS logic designers. After all, they invented FACT Quiet Series, which is globally accepted as the quiet standard. And now standard on our new GAL devices.

Riding the crest with National.

For samples, call or write us today. And find out why our new GAL Quiet Series devices are making waves.

1-800-NAE-SEMI, Ext. 125
National Semiconductor Corp.
P.O. Box 7643
Mt. Prospect, IL 60056-7643

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<thead>
<tr>
<th></th>
<th>V_{OLP}</th>
<th>V_{OHV}</th>
<th>V_{IL}</th>
<th>V_{OH}</th>
</tr>
</thead>
<tbody>
<tr>
<td>National</td>
<td>1.18</td>
<td>-.62</td>
<td>1.40</td>
<td>1.78</td>
</tr>
<tr>
<td>Competitor A</td>
<td>2.06</td>
<td>-.66</td>
<td>1.10</td>
<td>1.83</td>
</tr>
<tr>
<td>Competitor B</td>
<td>1.58</td>
<td>-.66</td>
<td>1.39</td>
<td>1.62</td>
</tr>
<tr>
<td>Competitor C</td>
<td>1.46</td>
<td>-1.08</td>
<td>1.09</td>
<td>1.56</td>
</tr>
</tbody>
</table>

*V_{OLP}—Dynamic Input threshold low **V_{OH}—Dynamic Input threshold high

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NEW PRODUCTS

SECOND-GENERATION MAX FAMILY BOOSTS DENSITY FIVEFOLD DAVE BURSKY

With multiple architectural enhancements put to work, the Max 7000 family of ultraviolet-erasable programmable-logic devices gives designers from 4000 to 40,000 available gates—up to five times more than most other high-density programmable chips. Furthermore, not only will the chips offer some of the highest complexities for PLDs, but they’ll have some of the shortest logic-propagation delays—as short as 15 ns from one input, through the array, and to an output for complex parts. In all, Altera plans to offer ten members in the family, with pin counts ranging from 68 to an industry high of 288 pins for PLDs.

To achieve the short delays and permit global clock speeds of 70 MHz, designers developed a low-skew programmable interconnect array that keeps skew to less than 2 ns. They also developed an enhanced macrocell that supports complex logic functions with up to 32 product terms. In addition, the macrocell library and design tools enable users to select various speed and power options for the cells to optimize the logic path during chip configuration. This power-saver feature allows individual logic macrocells to operate at full power with the shortest delay, or at one quarter the power with moderate speed (the speed penalty is less than 10 ns). Because only speed-critical paths need to run at full power, company designers estimate this can reduce overall chip power consumption by 20 to 50%.

The macrocells include a new logic structure Altera refers to as parallel logic expanders. Expanders permit complex logic functions to be implemented without incurring significant additional gate delays. Macrocells can borrow product terms from adjacent macrocells when complex functions of more than 5 product terms are needed. Incremental delays to build the complex functions are less than 2 ns per macrocell.

One key aspect to improving the overall array speed was the removal of the EPROM configuration elements from the direct signal path. By removing them, signal propagation delays are shortened by more than 10 ns when compared to the previous Max 5000 family. Between any two logic array blocks, there’s only a fixed delay, which is unlike the Max 5000, which had a variable routing delay.

In the array’s I/O control block, the I/O pins are decoupled from the macrocells so that the I/O pin and macrocell can be used independently of each other. Configurable registers in the macrocell can be set as D, T, S-R or J-K flip-flops, and have a programmable Clock Enable line. Global control signals feeding the register include Clock, Clear, and Output Enable.

In some speed comparisons of circuit functions implemented in the already available Max 5000 series and the forthcoming Max 7000 series, Altera examined the performance of four blocks—a 16-bit counter, a 16-bit adder, a 16:1 multiplexer, and a 16-bit decoder. The counter exhibited a 40% speed improvement, while the other three showed a 120 to 140% speed boost when implemented with the Max 7000 devices.

Software support for the Max 7000 series will be provided by the company’s Max+Plus II design software package that operates on a PC under Microsoft’s Windows 3.0 graphical environment. Data entry can be done through schematics, waveforms, or Altera’s hardware-description language. As part of the toolset, a compiler can automatically minimize the logic and synthesize an optimal fit of the design to the Max architecture.

Max 7000 series devices will come in a reprogrammable, windowed, ceramic package, and in a one-time-programmable plastic package. Depending on chip pin count, the package options include PGAs, PLCCs, and PQFPs. The first two devices—the 10,000-gate EPM7256 and the 4000-gate EPM7096—will be sampled in the fourth quarter of this year, with the others to follow during 1992.

Altera Corp., 2610 Orchard Parkway, San Jose, CA 95134; Stan Kopee, (408) 984-2800. CIRCLE 301

ELECTRONIC DESIGN
MAY 9, 1991
A pair of additions to the Am29000 family of 32-bit RISC processors gives designers both higher-performance and lower-cost options for applications employing the RISC CPUs. For higher-performance, Advanced Micro Devices created the 29030, which replaces the small branch-target-cache (BTC) memory with an 8-kbyte instruction cache. Not only does that improve processing throughput, but it eliminates one of the three 32-bit buses the original 29000 requires. That, in turn, allows the chip to be housed in a smaller (144-lead PGA or PQFP) and less-costly package. The other chip, the 29035, is pin-compatible with the 29030, but has only half the cache (4 kbytes). That cache is also simpler: It's direct-mapped rather than two-way set-associative to reduce chip complexity, thus lowering the price.

The BTC was replaced with the two-way set-associative 8-kbyte instruction cache to reduce the number of off-chip instruction accesses needed for programs or program loops that exceeded the size of the BTC on the older chip. The cache is accessed in the same pipeline stage as was the BTC. As a result, instruction response timing is identical to that in the previous chips. The store array, tag array, and valid array portions of the cache are all accessible under program control. That permits all entries to be read or written to ease testing or allow specific patterns to be preloaded. A control register also enables the cache to be left unlocked or be locked when portions of the contents must be write-protected, or be enabled or disabled. Half or all of the cache can be locked. When half is locked, the other half becomes a direct-mapped cache suitable for applications that require time-critical code to always be cached.

The bus protocol of the 29030 was designed to run with clock frequencies of more than 50 MHz, but without requiring large amounts of high-speed external memory. To ease system design, the input clock can be a TTL signal with a duty cycle that can range from a 30:70 to a 70:30 ratio and runs at the same frequency as the internal clock frequency of the processor. A proprietary clocking scheme allows the chip to use high-frequency clocks without undue silicon costs. A bidirectional Memory Clock signal on the processor is used as the timing marker for all setup and hold requirements for memory accesses. The signal can be either a copy of the Input Clock signal or a divide-by-2 version of the Input Clock signal, based on the state of a Division control pin. Consequently, the memory bus can be run at either full clock speed, or at half the speed (for example, when a 25-MHz system is upgraded with a 50-MHz CPU module, and the memory subsystem must stay at the older clock rate).

Some new protocols are adopted by the 29030 for single and burst-mode accesses. Those activities are controlled by the Request and Burst signal pins which are used together to indicate which of four different accesses is being performed on external memory. Additional support for narrow ROM, Page mode, and interleaved memory gives designers more flexibility for optimizing system cost. An output line also gives the outside world a signal to indicate whether or not the processor is performing an 8- or 16-bit access. The CPU also knows how many bytes or 16-bit words to transfer.

As part of the new bus structure on the 29030, AMD designers included support for the JTAG IEEE P1149.1 standard for boundary-scan testing, to aid in system board testing. Future extensions of boundary-scan technology will make even more extensive use of the boundary-scan test features for internal testing, so that a high level of fault coverage can be obtained.

Initial versions of the 29030 will run at external clock frequencies of 25 MHz. The simpler 29035 will initially come in 16- and 20-MHz versions and will only be available in the 144-lead quad-sided flat package. In lots of 1000, the PGA 25-MHz version of the 29030 sells for $147, the 33-MHz version will go for $184, and a 40-MHz version will be released in the latter half of this year. Pricing for the 16-MHz version of the 29035 goes for just $76 each in 1000-unit lots. Samples of the 25-MHz 29030 are available from stock, while samples of the 29035 will be available in the third quarter.

Advanced Micro Devices Inc., 5204 E. Ben White Blvd., Austin, TX 78741; (512) 462-4840. CIRCLE 302
Midrange-Density FPGAs Deliver More Features

Right on the heels of Altera's Max 7000 family of high-density PLDs comes a family of high-density field-programmable gate arrays. The QuickLogic family of pASIC chips will range in usable gate counts from about 500 to 4000, with minimum pin-in-to-pin-out propagation delays of about 15 ns, with most of that time consumed by the I/O buffers. Internally, such functions as 8-bit counters can run at over 100 MHz, and larger 16- or 32-bit counters can hit 90 MHz and higher. In contrast, the company claims most other FPGAs can't obtain counter speeds of more than about 50 MHz.

The CMOS logic typically consumes just 25 mW during standby, and about 1 W when clocked at full speed. The programming approach employed is based on a new, antifuse programming element that requires much less area than the structure employed by Actel Corp., the only other company that employs antifuses. The resulting areas of the pASIC chips are much smaller than those of similar capacity from Actel.

Not only are the fuses smaller, but their resistances are lower—just 50 Ω (typical) versus several hundred. That low resistance value and the small size also help keep circuit performance high and power consumption low. Parasitic losses can be kept to a minimum. The ViaLink fuse material is deposited into small window regions (vias) etched in the dielectric layer that separates the two metal interconnection layers. When a programming voltage is applied to the two metal layers, a short-circuit path is formed in the filled-in window region between the two conductors.

Each pASIC consists of a regular array of logic cells, with each containing the equivalent of 30 gate-array gates, of which 12 can be used in any typical application. Contained in each cell are AND gates, multiplexers, and a register element, all interconnected by the metallization grids and the ViaLink antifuses. Logic functions up to 14 inputs wide, including arithmetic, counter, data path, state-machine and "glue"-type gates, can all be implemented.

In the QL8X12, one of the smaller arrays in the family, there are 96 cells, or 1152 usable gates. The chip is referred to as a 1000-gate device. The chip comes in a 68-lead package. In the design stage are two other chips, the QL12X16 and the QL16X24, which pack 192 and 384 logic cells, respectively. The first comes in an 84-lead package, while the largest one employs a 160-lead package. The 192-cell chip packs about 2000 equivalent gates, while the 384-cell chip has about 4000 equivalent gates. All chips have built-in serial-scan-path circuitry to ease the testing problem and allow automatic-test-vector generation.

A set of design tools—the pASIC Toolkit 3.0—support the development of configuration patterns. The tools run under the Microsoft Windows 3.0 graphical user interface on PCs. Circuit designs can be captured with ECS, a graphical schematic-entry tool from the CAD/CAM Group Inc., Cupertino, Calif., and simulated with X-SIM a tool from Silicon Automation Systems Inc., San Jose, Calif. Both tools are included in the toolkit.

A design library with over 200 macrocells covers most frequently used blocks, including popular 7400-series TTL. The SpDE (seamless ASIC design environment) has an open, ASCII interface that allows third-party tools to easily be added. In addition, QuickLogic plans to port their tools to the Sun SparcStation family. The toolkit also includes automatic placement and routing software, a physical viewer/editor, a delay modeler, and a device programmer, all for $3995.

Samples of the 1000-gate QL8X12 will be ready in the third quarter, with full production slated for the fourth quarter. In 1000-unit lots, the chip will sell for $75 each.

QuickLogic Inc., 2933 Bunker Hill Lane, Santa Clara, CA 95054; David Laws, (408) 987-2000. CIRCLE 303
Upgrades for Mentor, OrCAD and Viewlogic

SUSIE Concurrent Designer™ has been upgraded with interfaces to Mentor™, OrCAD™ and Viewlogic™. This allows these popular data entry tools to work directly with the real-time SUSIE simulator. This new capability allows these popular data entry tools to work directly with the real-time SUSIE simulator. Designs take only seconds to load. Operating in real time, SUSIE allows for instant design and test vector modifications without any compilations. All changes to JEDEC, hex files, FPGA designs, IC technologies, etc., can be performed while simulation is in progress. Equipped with a software accelerator, SUSIE allows the designer to select any design section and simulate at a speed that is totally independent of the design size. This has created a renewed user confidence about board level simulation.

The SUSIE simulator is an excellent upgrade of Mentor, OrCAD and Viewlogic CAE tools that pays for itself typically within the first sixty days. CIRCLE 101

FPGA Competition Shifts to CAE Tools

With more entrants into the FPGA field, the product differentiation is becoming vague. For this reason, the new FPGA vendors stress the design environment and applications over the architecture of their devices. For example, while older FPGA vendors still push the $9,000 to $12,000 development systems, there are rumors that newer entrants, like PLUS LOGIC, will be announcing highly advanced simulation tools for under $500. Even more important, these new CAE tools will take only hours to learn and will be easy to use due to their real-time interactive operation. Also, simulation of multiple FPGAs at the board level in excess of 200,000 gates will be possible with optional software.

Xilinx™, ACTEL™ Forge Ahead

With a growth rate of over 50% per year, field programmable gate arrays (FPGAs) have drawn so much attention from semiconductor vendors that most of them will have FPGA parts ready by the end of 1991. However, it is expected that Xilinx and Actel will retain their technological leadership, particularly now that designing with these parts has become quick and simple. Thanks to real-time SUSIE development tools from ALDEC one can simulate these parts at chip and board level with an accuracy of 10 picoseconds. Since SUSIE allows for selective circuit simulation, you can simulate the FPGA parts cell-by-cell, section-by-section, IC-by-IC and/or any combination thereof. This dramatically speeds design development over the previously employed methods. CIRCLE 102

Cost - A Leading CAE Factor

With purse strings still tight, many CAE vendors find that their lower cost products are moving faster. Designers are particularly buying products that automatically create design documentation, handle archives and do other basic chores at affordable prices. For example, SUSIE simulator ($995) which allows designers to save, print, and archive design revisions, test vector files, error conditions, etc., is being purchased in greater numbers. Perceiving this shift to low-cost CAE environments, some workstation CAE vendors are talking to the PC CAE vendors about tool integration and licensing. This recession has considerably helped high performance PC-based CAE to gain ground on the expensive workstation-based CAE tools.

Real Cost of CAE Tools

Experienced CAE users are much more careful in selecting CAE tools than novices. While novices look primarily at price and features, the experienced users focus mainly on ease of use, because the database built around any CAE tool may quickly represent ten times the value of the CAE purchase price. Tools that work in real-time save the most. They save at least four to ten times more than those working in batch mode because: they are free of any software compilations and designers are much more effective when they debug designs in real-time. SUSIE, the logic simulator that is resold by most CAE vendors, is the only existing real-time simulator. It provides the most cost effective design environment available today. CIRCLE 105
The chip, jointly developed by Fujitsu and AFE Displays Ltd., Birmingham, U.K., operates at clock rates of 40 MHz and offloads the host processor from the graphics computations.

The graphics processor can support 8, 24, or 48 bits/pixel, including a 16-bit Z buffer and an 8-bit transparency buffer, and addresses a 56-Mbyte memory space. Image maps of up to 4096-by-4096 pixels can be supported by the large memory space. Direct interfaces for either video RAMs or standard dynamic RAMs enable the designer to effect various cost/performance trade-offs. An on-chip programmable video-timing controller handles just about any CRT parameter, and supplies the synchronization and blanking control signals.

Triple on-chip FIFO buffers keep all of the video data buffered so that both the host-system and video-RAM interfaces can operate at maximum transfer rates. When running at 40 MHz, the chip can transfer 32 Mpix/s (8-bit pixels) for BitBLTs and 200 Mpix/s for screen fills. Development tools for the GSP include a software emulator, both 2D and 3D graphics libraries, C source examples, example X-windows software, and Sun’s low-level graphics library, and an S-bus evaluation board for use on Sun SparcStation platforms. Samples of the chip sell for $300 in 100-unit quantities and are available immediately.

**Fujitsu Microelectronics Inc., Advanced Products Div., 77 Rio Robles, San Jose, CA 95134-1807; Martin Booth, (408) 456-1160.**

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The new L3R000A CPU module as well as the L3R230 enhanced read/write buffer chip, the L3R010A floating-point coprocessor, and dual caches, each comprising 64 kbytes of fast SRAM (double the size of caches in the RPM3310). Enhanced features of the L3R000A MIPs RISC processor include hardware cache invalidation control. That feature simplifies the implementation of multiprocessor systems and helps ensure cache integrity.

Using 3.5-in.² modules can greatly simplify system design because they eliminate many of the complex timing concerns associated with implementing RISC-based systems. At 33 MHz, the subsystem dissipates about 25 W and requires an airflow of 150 linear ft./min. to keep the ambient to 50°C.

In addition to the 33- and 40-MHz modules, LSI will also sell the enhanced R/W buffer chip, the L3R230. That chip contains a nine-word write buffer, full-priority generation, multiprocessor support, and a reset-initialization controller. An optional byte-gathering feature is also included. Furthermore, the chip incorporates a Block-Match capability that lets it resolve read/write conflicts quickly. Block sizes can be programmed for 4 to 32 words.

Prices for the 33- and 40-MHz versions of the RPM3300 in 100-unit lots are $2375 and $3165, respectively. Prices for the 33- and 40-MHz versions of the chip sell for $240 and $264 each, respectively, in 5000-unit quantities.

And, to simplify Sparc-based graphics systems or any other system requiring high-performance 2D graphics, Weitek designed the W8720, a highly integrated graphics controller. The chip packs local buffer memory and video-control logic, as well as hard-wired support for such functions as polygon fills, bit-block transfers, and logical raster operations. Speed can be improved about tenfold by using the W8720 instead of the dumb frame-buffer 2D color graphics typically implemented on other Sparc-based systems. The chip comes in a 208-lead quad-sidied flat package and sells for $160 in 1000-unit lots.

**Weitek Corp., 1060 E. Arques Ave., Sunnyvale, CA 94086; (408) 739-8400.**

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**NEW PRODUCTS**

**ENHANCED SPARC CPU PACKS FPU, CUTS SPACE**

Merging a floating-point math unit on the same chip as the Sparc integer unit lets the W8701 Sparc processor chip from Weitek replace two-chip combo (integer plus floating-point) units. The W8701 chip implements version 7.0 of the Sparc architecture while maintaining software compatibility with other Sparc processors. Versions of the chip are available for clock speeds of 25, 33, and 40 MHz.

A 136-register, general-purpose register file allows the W8701 integer plus floating-point unit to implement eight sets of register windows plus eight nonwindowed global registers. Also on the chip are 32, 32-bit floating-point registers that can be paired to hold 16 double-precision numbers. The chip will be housed in a 207-pin PGA package. The 33- and 40-MHz versions of the chip sell for $240 and $264 each, respectively, in 5000-unit quantities.

**This module implements version 7.0 of the Sparc architecture while maintaining software compatibility with other Sparc processors.**

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**ENHANCED CPU MODULE PUSHES RISC TO 40 MHZ**

The second-generation RISC CPU module from LSI Logic, the Ngine RPM3310, gives system designers a complete CPU, cache, and floating-point subsystem that can run at clock speeds of 33 or 40 MHz. At those speeds, the module delivers throughputs of 27 and 35 MIPS, respectively. The RPM3310 is also pin-compatible with the 20- or 25-MHz RPM3300 module released last year.

The 3330 incorporates the LR3000A CPU as well as the LR3230 enhanced read/write buffer chip, the LR3010A floating-point coprocessor, and dual caches, each comprising 64 kbytes of fast SRAM (double the size of caches in the RPM3310). Enhanced features of the LR3000A MIPS RISC processor include hardware cache invalidation control. That feature simplifies the implementation of multiprocessor systems and helps ensure cache integrity.

Using 3.5-in.² modules can greatly simplify system design because they eliminate many of the complex timing concerns associated with implementing RISC-based systems. At 33 MHz, the subsystem dissipates about 25 W and requires an airflow of 150 linear ft./min. to keep the ambient to 50°C.

In addition to the 33- and 40-MHz modules, LSI will also sell the enhanced R/W buffer chip, the LR3230. That chip contains a nine-word write buffer, full-priority generation, multiprocessor support, and a reset-initialization controller. An optional byte-gathering feature is also included. Furthermore, the chip incorporates a Block-Match capability that lets it resolve read/write conflicts quickly. Block sizes can be programmed for 4 to 32 words.

Prices for the 33- and 40-MHz versions of the RPM3300 in 100-unit lots are $2375 and $3165, respectively. Prices for the 33- and 40-MHz versions of the chip sell for $240 and $264 each, respectively, in 5000-unit quantities.

And, to simplify Sparc-based graphics systems or any other system requiring high-performance 2D graphics, Weitek designed the W8720, a highly integrated graphics controller. The chip packs local buffer memory and video-control logic, as well as hard-wired support for such functions as polygon fills, bit-block transfers, and logical raster operations. Speed can be improved about tenfold by using the W8720 instead of the dumb frame-buffer 2D color graphics typically implemented on other Sparc-based systems. The chip comes in a 208-lead quad-sidied flat package and sells for $160 in 1000-unit lots.

**Weitek Corp., 1060 E. Arques Ave., Sunnyvale, CA 94086; (408) 739-8400.**

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**ENHANCED SPARC CPU PACKS FPU, CUTS SPACE**

Merging a floating-point math unit on the same chip as the Sparc integer unit lets the W8701 Sparc processor chip from Weitek replace two-chip combo (integer plus floating-point) units. The W8701 chip implements version 7.0 of the Sparc architecture while maintaining software compatibility with other Sparc processors. Versions of the chip are available for clock speeds of 25, 33, and 40 MHz.

A 136-register, general-purpose register file allows the W8701 integer plus floating-point unit to implement eight sets of register windows plus eight nonwindowed global registers. Also on the chip are 32, 32-bit floating-point registers that can be paired to hold 16 double-precision numbers. The chip will be housed in a 207-pin PGA package. The 33- and 40-MHz versions of the chip sell for $240 and $264 each, respectively, in 5000-unit quantities.

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**Weitek Corp., 1060 E. Arques Ave., Sunnyvale, CA 94086; (408) 739-8400.**
IEEE-488

Control any IEEE-488 (HP-IB, GP-IB) device with our cards, cables, and software for the PC/AT/386, EISA, MicroChannel, and NuBus.

30-MHZ CONTROLLER BOOSTS 8-BIT SYSTEMS

A 30-MHz version of the popular 80C51 microcontroller meets the increasing demand for greater processing speed in embedded-controller applications. Up to now, the maximum clock frequency for an 80C51 has been 24 MHz. Together with the 80C51’s existing features—such as comprehensive bit handling, instruction set, two 16-bit timer/counters, and binary and BCD arithmetic—the 30-MHz clock frequency suits the PCB80C51BH-5-30 for a wide range of low-cost, high-performance embedded-control applications. The new microcontroller executes nearly 60% of its instructions in 0.4 μs, and 40% of them in 0.8 μs. Multiply and divide instructions execute in just 1.6 μs. At full speed, the device consumes 44 mA at 5.5 V. Power-down and idle modes reduce current consumption to 10.8 mA/μs and 50 μA, respectively. Samples of the PCB80C51BH-5-30 are available now, and volume quantities can be delivered within 10 weeks. The device costs about $3.50 each in quantities of 10,000.

Philips Components, Signetics Company, 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Kate Douglas, (408) 991-5076.

30-MHZ CONTROLLER BOOSTS 8-BIT SYSTEMS

The popular GAL16V8, an electrically erasable programmable-logic device that can emulate most types of 20-pin PLDs, is now available in a very-low-power version. It has a maximum supply current of only 27 mA that consumes only one-eighth the power of bipolar programmable-array-logic parts. The new GAL16V8S-20EB1 has a maximum propagation time of 20 ns. The low-power consumption is achieved by using an optimized single-polysilicon single-metal CMOS EEPROM process that’s simpler and more reliable than the processes used by other gate-array logic makers. Other benefits of the new process are a threefold improvement in electrostatic-discharge protection, increased data retention, and better switching-noise immunity. Available now, the GAL16V8S-20EB1 offers preload and power-on reset of all registers, a 100% final-programming yield, and data retention exceeding 20 years.

SGS-Thomson Microelectronics, 1-20014 Agrate Brianza, Italy; (0039) 39-6555-597.

FAST LOGIC SEQUENCER RUNS AT 62 MHZ

The fastest programmable-logic sequencer released by Philips-Signetics, the PLUS405-55, can be clocked at up to 62 MHz—about 20% faster than previously released sequencers from the company. A speed upgrade to the company’s PLUS405 architecture, the 28-pin chip has 16 inputs and 8 J-K registered outputs. It accepts two external clock sources, and has two Complement Arrays so that If-Then-Else transitions can be implemented with one product term. The chip also has an asynchronous-register-initialization feature that allows each register to be individually programmed to generate a specific Preset-Reset pattern, allowing the chip to be asynchronously initialized to any known condition. The sequencer is supported by both the Snap tool package offered by the company and a simpler software package, Slice, that does entry-level implementation. In 1000-unit lots, the plastic DIP version of the chip sells for $17.65.

Philips Components, Signetics Company, 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Kate Douglas, (408) 991-5076.

TRIMS IC COUNT/SPACE

A second-generation chip set for extended-industry-standard-architecture (EISA)-based motherboards, the 82350DT is a superset of Intel’s 82350 chip set released in 1990. The new set lets system designers assemble an EISA system with 43 devices—less than half the number needed for the first chip set—on an 8.5-by-12-in. board. This reduced chip count and thus cost, coupled with the simultaneous release of the reduced-cost 80486SX CPU, will let system designers implement low-cost EISA-based systems. The chip set's modular architecture enables the same platform to be used for 386DX, 486DX, or 486SX CPUs. The 82350DT consists of three of the original chips—the integrated system peripheral, the EISA bus controller, and the EISA bus buffer—plus a DRAM controller, an advanced data-path circuit, and a local I/O controller. In 1000-unit lots, the chip set sells for $200.

Intel Corp., 3063 Bowers Ave., Santa Clara, CA 95052-8131; (408) 765-8800.

Free: Informative catalog 800-234-4232 Applications help (617) 273-1818

CIRCLE 87

EISA CHIP SET

TRIMS IC COUNT/SPACE
The FS700 LORAN-C frequency standard

10 MHz cesium stability

$4950

Cesium long term stability at a fraction of the cost

Better long-term stability than rubidium

Not dependent on ionosphere position changes, unlike WWV

Complete northern hemisphere coverage, unlike GPS.

The FS700 LORAN-C frequency standard provides the optimum, cost-effective solution for frequency management and calibration applications. Four 10 MHz outputs from built-in distribution amplifiers provide cesium standard long-term stability of $10^{-12}$, with short-term stability of $10^{-10}$ ($10^{-11}$ optional). Reception is guaranteed in North America, Europe and Asia.

Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ±360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.
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CIRCLE 83

New Products
DIGITAL ICS

Standard-Cell Family Includes V-Series CPU

Although standard-cell vendors are plentiful, the CB-C7 standard-cell family from NEC is the only one, aside from Intel, offering 8086- and 8088-compatible CPU cores (the V20H and V30H, respectively). Employing a 0.8-µm (drawn) CMOS fabrication process, the cells can be combined to deliver chips with complexities of up to 180,000 gates and as many as 350 I/O lines.

Typical gates have propagation delays of 340 ps and dissipate just 8 µW/gate/MHz. Two implementation options will be available with CB-C7. The first offers the shortest turnaround time (about 6 weeks), and places the standard cells on a sea-of-gates array. Although not as dense as a full-custom chip, only metal-mask-related layers need be fabricated to complete the design. If customers can wait two weeks longer, a fully customized and smaller chip can be created.

The CB-C7 cell library is compatible with the company’s previously released CMOS-7 library, and thus provides a direct migration path for existing designs. Many popular standard "mega" functions are included in the library—the 8086- and 8088-compatible CPUs, a programmable DMA controller, USART, interval timer, system bus controller, and a 765-type floppy-disk controller. Also available are compilers to generate custom-sized blocks of RAM and ROM.

Supporting the chip designer is NEC’s OpenCAD Design System, which offers a complete front-to-back unified design environment based on popular commercial design tools, as well as a few proprietary tools. Initial prices for the chips will range from 0.06 to 0.1 cents/usable gate, depending on complexity, package, and quantity. The libraries are available immediately and designs will be accepted for production in the third quarter of this year.

NEC Electronics Inc., 401 Ellis St., Mountain View, CA 94043; Al Chiang, (415) 965-6539.

Dave Bursky

Crosspoint Switch Moves NRZ Data Fast

Letting data flow through it at 1.2 Gbits/s for non-return-to-zero-coded signals, a 32-by-32 crosspoint switch can also be used in groups of four without any additional support components to implement 64-by-64 crosspoint switches. The S2024 Crossbow switch, developed by Applied Microcircuits, also offers full broadcast capability. This capability permits any of its 32 input lines to be connected independently to any or all of its 32 output lines.

Although the chip is implemented internally with 10K-family ECL circuits, all addressing inputs and control lines are TTL-compatible to simplify the interfacing to microprocessors. A complete reconfiguration of the data-flow paths requires only 4 ns, and the reconfiguring does not disturb existing switch operations.

The chip has transparent and synchronous operating modes, providing maximum flexibility across a wide range of applications. The transparent mode allows the full-speed, 1.2-Gbit/s throughput, while the synchronous mode drops the data rate to half that figure—to 600 Mbits/s.

The high data rates suit the chip well for handling many diverse applications: digital video, digital demultiplexing, microwave or fiber-optic data distribution, data communications and telecommunications switching, and high-speed automatic test equipment.

The 9-W power consumption of the S2024 switch may seem high, but that dissipation figure is still only about half the power of the best alternative solutions. Finally, clock inputs for the chip can be set as single-ended or differential.

Housed in either a 251-lead pin-grid array package or a 196-lead chip-carrier version sells for $389 each.

Applied Microcircuits Corp., 6195 Lusk Blvd., San Diego, CA 92121; Mike Orenich, (619) 550-9333.

Dave Bursky
CHIP SET POWERS V.32 MODEMS IN LAPTOPS AND PORTABLES

Modem and personal-computer designers can now track a V.32 modem into their designs by using a three-chip, surfacemountable data pump that typically consumes just 450 mW while operating and 50 mW in the sleep mode. The DSP16A-V32 chip set from AT&T Microelectronics consists of the company's 16-bit fixed-point DSP16A digital-signal processor, the T7525 linear codec, and an interface controller. V.32 is a 2- or 4-wire full-duplex telecommunication standard for public-switched or private networks. Housed in a 28-pin SOJ package, the T7525 linear codec on the telephone-line side of the data pump serves as the analog front end and has 12-bit linearity that provides over 60 dB of echo cancellation from a digital echo canceler. The ROM-coded DSP16A performs signal-processing and control functions required to implement V.32 performance specifications. Interfaces to a V.24 TAD and telephone functions, and the T7525 linear codec on the telephone-line side of the data pump serves as the analog front end and has 12-bit linearity that provides over 60 dB of echo cancellation from a digital echo canceler. The ROM-coded DSP16A performs signal-processing and control functions required to implement V.32 performance specifications. Interfaces to a V.24 speech compression, storage, and other functions for featurephones and cordless telephones, the D6005 chip set from DSP Group stores telephone messages on solid-state memory. This approach breaks away from conventional telephone answering devices (TADS) that use audio tape to store messages.

The chip set consists of the D6005-11 digital-signal processor that executes speech compression, storage, and other TAD and telephone functions, and the D6005-71 ASIC to handle the memory and host interface. It also consists of the D0000-26 codec for analog-to-digital and digital-to-analog signal conversions, and from 1 to 16 audio-grade RAMs (ARAMs) for message storage.

The D6005 chip set has the capability to address up to 16 Mbits of memory, which is equivalent to 26 minutes of storage time or 60-30-second messages. Other features include instantaneous message retrieval, playback, and repeat; message skip and offset; selective erasure; date and time stamping; and voice-activated recording.

Like cassette-based TADs, products designed with the D6005 chip set can also have such features as a secret mailbox, private incoming messages, message-transfer capability, multiple outgoing messages, and voice instructions.

To support featurephones and cordless telephones, the D6005 chip set offers dual-tone multifrequency (DTMF) receive and transmit capability, permitting remote activation of all TAD functions from a cordless telephone. Remote TAD operation is also supported by the D6005 chip set's near-end echo-cancellation capability.

The digital-signal processor, ASIC, and codec circuits have a total maximum power dissipation of 1.09 W. The D6005 chip set, with a complement of four ARAMs (7 minutes of recording time), is available now for under $30 each in quantities of 10,000.

AT&T Microelectronics, Dept. 52AL300240, 555 Union Blvd., Al- lenstown, PA 18103; (800) 372-2417.

MILT LEONARD

CHIP SET IMPLEMENTS TAPELESS TELEPHONE-ANSWERING MACHINES

In addition to performing all of the functions for featurephones and cordless telephones, the D6005 chip set from DSP Group stores telephone messages on solid-state memory. This approach breaks away from conventional telephone answering devices (TADS) that use audio tape to store messages.

The chip set consists of the D6005-11 digital-signal processor that executes speech compression, storage, and other TAD and telephone functions, and the D6005-71 ASIC to handle the memory and host interface. It also consists of the D0000-26 codec for analog-to-digital and digital-to-analog signal conversions, and from 1 to 16 audio-grade RAMs (ARAMs) for message storage.

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AT&T Microelectronics, Dept. 52AL300240, 555 Union Blvd., Al- lenstown, PA 18103; (800) 372-2417.

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We’ll send you the real block diagram.

CIRCLE 138
NEW PRODUCTS

ADC WITH 574 FOOTPRINT SAMPLES
AND CONVERTS SIGNAL IN 10 µS

FRANK GOODENOUGH

The standard 574 analog-to-digital converter, originated by Analog Devices a dozen years ago, is now available in various forms with many specifications from, at last count, nine suppliers. The original device required two chips and for years was only available in ceramic packages. With their latest version—the AD1674—Analog Devices is now topping all known 574-type ADCs in both price and performance.

At $18 each in hundreds, the ADC goes for 80% of a basic AD574A and 70% of an AD674A. However, conversion times of the AD574A and AD674A run a minimum of 35 and 15 µs, respectively. The AD1674 does it in 10 µs—a conversion rate of 100 kHz. And, unlike previous versions, a user-transparent, true sample-and-hold amplifier (SHA) sits on the ADC’s front end. The ADC’s conversion rate is the SHA’s sampling rate. The SHA’s 1-MHz bandwidth ensures 12-bit operation to Nyquist frequencies. Its unique circuit was the subject of a technical presentation at this year’s International Solid State Circuits Conference (ELECTRONIC DESIGN, Feb. 14, p. 68).

Like most sampling ADCs, dynamic (ac) specifications are provided, and guaranteed at that. Not only does the AD1674 maintain the 574’s footprint, but works with all current 574 software operating in the standalone mode. While operating in the full-control mode, minor timing changes are needed.

All 574 family converters are general-purpose ADCs designed to run off ±15-V or ±12-V rails plus a 5-V digital line. Other family traits include user selection of one of four input-voltage ranges (±5, ±10, 0-10, and 0-20 V) by pin-strapping, and a parallel three-state digital output, which is software-programmable to provide any mix of three 4-bit nibbles. As a result, it adapts easily to a wide range of signals and to 4-, 8- or 16-bit microprocessor buses.

Devices for all three standard-temperature ranges are available with an integral nonlinearity (INL) over temperature of ±1 LSB maximum. Prime grades for the commercial and extended-industrial range offer ±1/2-LSB INL maximum. All five grades guarantee no-missing-code operation to 12 bits over temperature.

The lower-grade commercial AD1674J, over temperature and in a 28-pin plastic double-width DIP, offers a sampling rate of 100 kHz minimum, a 10-kHz minimum input signal, maximum offset drift of ±2 LSBs, maximum full-scale error of ±6 LSBs, and maximum signal-to-(noise + distortion) (s/(n + d)) ratio of 69 dB (11.2 bits). Total harmonic distortion (THD) is −82 dB (13.3 bits) maximum, peak harmonic component is −82 dB (13.3 bits) maximum, and intermodulation distortion (IMD) is −80 dB maximum (with 9.08- and 9.58-kHz inputs). Power dissipation is 575 mW maximum.

If a SHA is needed ahead of a 12-bit ADC, such as the 3-µs AD7672, the AD1674’s SHA—the AD781—is available in an 8-pin miniDIP. The hold capacitor is on-chip. Its acquisition time is just 700 ns maximum to 0.01%, and aperture jitter is just 75 ps maximum.

Unlike most SHAs, dynamic specifications are provided. While sampling at 500 kHz and with a 10-kHz input, THD runs −80 dB maximum, and s/(n + d) ratio runs −72 dB. Typical THD (while sampling 10-, 50- and 100-kHz inputs) runs −90, −73, and −68 dB, respectively. Sampling similar signals, typical s/(n + d) runs 78, 73, and 67 dB, respectively. IMD usually runs −77 dB.

Pricing for the AD1674, in hundreds, ranges from $18 to $70 each. In similar quantities, the commercial-grade AD781 can be had for $6 each, the extended-industrial grade for $7.40 each, and the mil-grade SHA for $20 each. Small quantities of each are available from stock.

Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; Applications Engineering, (617) 937-1428

CIRCLE 315
Minimize EMI During PCB layout before you build it!

Get your product to market fast and save time and money in the process! Now you can optimize your circuit boards early in the design cycle before hardware prototyping with a simulation tool developed by Bell-Northern Research for Northern Telecom. As a complement to the circuit board design system CBDS, PCP EMSIM allows designers to select, position and route components for minimum EMI emissions, decreasing the risk of failing government regulations, such as FCC, CISPR and VCCI.

Optimizing component selection, placement, and routing using PCP EMSIM enables you to reduce EMI before costly hardware prototyping. Scanning the revised prototype board on EMSCAN confirms the reduction in EMI, which is again verified by open field tests.

Come and see PCP EMSIM & EMSCAN at Booth 1361 at the Design Automation Conference 28th Conference.
16-PIN IC LOOKS LIKE 4 VIDEO OP AMPS FEEDING A MULTIPLEXER

Cramping four video op amps, each with its own functional pair of differential inputs, a multiplexer to connect one of them to an output, two address inputs for the multiplexer, plus an enable/disable input, may seem topologically impossible. Not for the Harris HA-2444. As a black box, this device looks like four op amps connected to a four-input analog multiplexer, offering a high-impedance state in which none of the op amps are connected to the output. Unlike similar devices that are limited strictly to multiplexing, each op amp can be given its own unique feedback circuitry to control gain, bandwidth, or function (see the figure). For example, one op amp can sum (linearly mix) several signals, a second can perform integration, while the third and fourth act as a comparator and buffer. The high-impedance output state permits multiple HA-2444s to be wire-ORed (connected in parallel) when more than four signals must be conditioned and multiplexed.

Small-signal (±100-mV) unity-gain bandwidth is typically 45 MHz. Open-loop gain at dc typically runs 76 dB. Operating from ±15-V rails, the output can put ±11 V across 1 kΩ and ±2 V across a more typical 75-Ω video load. Reflecting a 120-V/µs minimum slew rate is full-power bandwidth of 3.8 MHz minimum. At a gain of 1, gain is flat within ±0.12 dB to 10 MHz for a 200-mV rms input. Typical differential gain and phase run 0.05% and 0.05°, respectively. Chrominance gain and luminance delay run 0.1 dB and 7 ns, respectively. An enabled HA-2444 switches from one channel to another in a maximum of 100 ns. The application of an enable pulse connects a selected channel to the output in a similar time. Applications range from simple video-channel selection to use as a programmable-gain amplifier with four selectable gains for one signal.

Harris Semiconductor, P. O. Box 883, Melbourne, FL 32901; (800) 4-HARRIS, ext. 1221. FRANK GOODENOUGH

HIGH-SPEED ANALOG ARRAYS GET MACROS

If a relatively small, high-speed, semicustom analog IC at low cost is needed, a dielectrically isolated Sipex SP2000 tile array may be the way to go. The company is now announcing a library of over 25 macros and two new tiles, creating a family of three: the SP2100/04/07 with 4, 12, and 20 tiles, and 26, 46, and 54 bonding pads, respectively. Each tile holds 16 vertical npn and 16 vertical pnp small-signal transistors with fβ of 1000 and 600 MHz, respectively. Each array also contains additional (larger), vertical npns and pnp transistors (currents to 100 mA), as well as thin-film resistors, capacitors, and conventional and Zener diodes. Each transistor is isolated in its own silicon-dioxide tub, and good vertical npn transistors are available; thus, designers can design circuits on the arrays without worrying about dc and ac parasitics or working with only npn transistors. Macros, which take from one to two tiles, include general-purpose, precision, wide-band (300-MHz), and high-gain (125-dB) op amps; multiplexing amplifiers; sampling amplifiers; comparators; and analog multiplexers. Also included are references, charge pumps, and even logic gates. By year's end, most macros will be available as kit parts for breadboarding. Typical NRE cost runs under $19,000 and includes prototypes in about 8 weeks after completion of design and layout.

Sipex Corp., 22 Linnell Circle, Billerica, MA 01821; Tim Maniwa, (408) 942-4484. CIRCLE 317

DIP HOLDS 4 OP AMPS PLUS A REFERENCE

The TDC4614 is designed to create up to four precision low-impedance voltage sources. This 16-pin DIP contains four, independent 324-type op amps plus an adjustable output (1.2 to 6.3 V) bandgap reference. Its cohort, the TDC4611, contains just one op amp and a reference in an 8- or 14-pin DIP. Many flash ADCs offer improved linearity if one or more taps on their resistive divider are each driven by a precision voltage, a natural application for the TDC4614. Many additional flash and other types of ADCs require a positive and a negative reference. Alternatively, the IC can provide any mix of four different positive or negative reference voltages for any mix of DACs or ADCs. Available in commercial and military grades, pricing starts at $1.20 each for the commercial TDC4611 and $1.75 each for the TDC4614, both in quantities of 100.

TRW LSI Products Inc., P. O. Box 2472, La Jolla, CA 92038; Dan Watson (619) 457-1000. CIRCLE 319

8-BIT ADCS SAMPLE 300-KHZ SINE WAVES

Designed to replace their original 10-year-old, industry-standard ADC0820, National Semiconductor's new families of 8-bit ADCs and data-acquisition systems convert in 500 ns. Of more importance, because they're truly sampling converters, they offer a typical full-power bandwidth of 300 kHz. That is, they can sample and digitize a 300-kHz sine wave. At their heart lies a patented, 8-bit/500-nS ADC employing a multistep architecture. The ADC08061/162/068 family offers 1, 2, 4, and 8 signal input channels, respectively, followed by a multiplexer (except for the single-channel unit), a sample-and-hold amplifier, and an ADC. The ADC08161/162/164/168 are identical devices, except that all have a 2.5-V bandgap reference. Four grades provide total unadjusted errors of ±1 and ±1/2 LSB for both industrial and military use. Packaging includes: 20-pin PLCCs, DIPs, and wide-body SOICs for the 4-channel unit; a sample-and-hold amplifier, and an ADC. The ADC08161/162/164/168 are identical devices, except that all have a 2.5-V bandgap reference. Four grades provide total unadjusted errors of ±1 and ±1/2 LSB for both industrial and military use. Packaging includes: 20-pin PLCCs, DIPs, and wide-body SOICs for the 4-channel device; and 28-pin PLCCs, DIPs, and wide-body SOICs for the 8-channel unit. In quantities of 100, the ADC starts at $8.90 each.

National Semiconductor Corp., P. O. Box 58990 Santa Clara, CA 95052-5890; Kay Hoang, (408) 721-2392. CIRCLE 319

158 ELECTRONIC DESIGN MAY 9, 1991
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CIRCLE 133 FOR LITERATURE
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TIMING-DIAGRAM SOFTWARE ADDS
TEST-VECTOR GENERATION

The Test Vector Generator is the newest enhancement to the dV/dt Timing Diagram Accelerator, a pre-schematic-capture tool that lets designers create timing diagrams. With Test Vector Generator, designers can convert dV/dt waveforms to various programmable-logic-device (PLD) test-vector formats, and can convert test vectors into dV/dt waveforms.

Currently, the Test Vector Generator will translate into the following PLD formats: Data I/O's Abel, Capo Computing Systems' MacAbel, Logical Devices' CPLD, Accel Technologies' TangoPLD, OrCAD's Orcad/PLD, AMD's Palasm, and Ovation's Scheme PLD. Other PLD formats will be added.

Users create test vectors by first establishing dV/dt standard-format test-vector files. Using the conversion utility, they then convert the standard vectors to the PLD format of choice. Also, dV/dt Timing Diagram Accelerator can import dV/dt standard-format test-vector files to create waveforms on the screen. Users can customize test-vector format outputs with the necessary file specifications in the Test Vector Generator manual.

The dV/dt Test Vector Generator runs on PCs and Macintosh computers. It's shipping now for $495, or for $995 when bundled with the Timing Diagram Accelerator.

Doctor Design Inc., 5415 Obertin Dr., San Diego, CA 92121; (619) 457-4545.

LISA MALINIAK

PCB SCREENING TOOL CHECKS
FOR SIGNAL INTEGRITY

Version 2.0 of the BoardScan PCB-board screener from Quantic Laboratories now calculates signal-integrity parameters. BoardScan is a circuit-simulation tool that screens pc boards and determines critical nets where crosstalk and signal-integrity problems are likely to occur. The signal-integrity calculations uncover complications due to such factors as time delays, overshoots, undershoots, settling time, noise margins, and functional violations.

BoardScan features an interactive database facility that lets users add, delete, substitute, and browse through the component library within the user interface. The component library includes over 4000 components covering a range of logic technologies, such as Fast and HCT.

Crosstalk between nets is calculated with a high-order boundary-element field solution. Routed nets are coupled automatically, and the crosstalk values are detailed in a net report. Users input circuits to the screener through an interface file that's already integrated with tools from such companies as Mentor Graphics, Rascal-Redac, and Valid Logic Systems.

Once BoardScan identifies the critical nets, they can be further analyzed by the company's Greenfield Version 3.0 system-level simulator. Greenfield can simulate circuits with multiconductor, coupled, transmission lines. It includes a schematic and graphics editor for interconnection and editing of system components.

Both BoardScan Version 2.0 and Greenfield Version 3.0 run on a variety of Unix platforms. Pricing for BoardScan and Greenfield starts at $17,000 and $24,500, respectively.

Quantic Laboratories Inc., Suite 200, 281 McDermot Ave., Winnipeg, Manitoba, Canada R3B 0G9; (204) 943-2552.

LISA MALINIAK

IMPROVED SOFTWARE EASES BOARD DESIGN

The newest release of the Auto-Board System features enhancements that ease the task of board design. Schematic capture was improved with pull-down menus for invoking edit commands and inserting symbols. In addition, a reorganized symbol library has multiple-section parts that can be inserted as a unit and then moved individually. The layout and routing module now has forward annotation for recognizing new parts added to the schematic or net list, and a viewport that lists parts for selection during placement.

Auto-Board System was restructured so that placement and routing tools can be added incrementally. It runs on PCs and Macintosh computers, and costs between $295 and $3200.


LISA MALINIAK

FPGA DESIGN SOFTWARE RUNS UNDER WINDOWS 3.0

The pASIC Toolkit 3.0 is a set of tools for designing, simulating, programming, and testing QuickLogic field-programmable gate arrays on a PC. It combines the Engineering Capture System from the CAD/CAM Group and the X-Sim simulator from Silicon Automation Systems with the pASIC architecture-optimized tools from QuickLogic. All of the software runs under Microsoft Windows 3.0. The toolkit contains all of the software and hardware needed to build custom designs with QuickLogic's devices, except for the personal computer. A notebook-sized Designer Programmer performs both device programming and functional testing with ATVG and user-generated vectors. Cables, connectors, and an antistatic wrist strap are also included. The pASIC Toolkit 3.0 is shipping now for $3995.


LISA MALINIAK

Correction: On page 109 of our March 14 issue, the phone number of Lewis Systems Inc., Irving, Texas was incorrectly listed. The number should have read (214) 438-2177.
NEW PRODUCTS

COMPUTER-AIDED ENGINEERING

UPGRADE KIT BOOSTS MODELER’S PERFORMANCE

Users can push the speed of their Logic Modeling LM-1000 hardware modelers with an upgrade kit from the company. The upgrade improves the speed of the LM-1000 by up to a factor of six, enabling a large number of designers to run more complex simulations and faster fault simulations. The kit consists of a 68040-based CPU board and software. An improved network server helps boost overall performance, and a larger CPU memory increases fault-simulation capacity by as much as a factor of ten. In addition, the new software includes enhanced hardware-modeling algorithms. LM-1000 users can install the upgrade in the field. With the upgrade, the LM-1000 becomes identical to the company’s new LM-1200 modeler. The upgrade kit will be available in June for $19,000.

MODEL E R’S PERFORMANCE ENHANCED

The improved 4.05 version of PSpice now offers more features, including Sun network licensing and pulse-width-modulator models. Parts sessions can be frozen and rerun at a later time. In addition, the number of states for digital simulation has increased from 28 to 246,528. This is due to the increase in the number of input levels from three to five, and an increase in the number of output strengths from 4 to 64. Optional power-supply pins were added to all of the parts in the digital library, giving users the ability to have more than one power supply in the circuit. The PSpice software runs on personal computers, Macintosh computers, and several Unix workstations. Pricing ranges from $950 to $5400, depending on the platform. Such options as digital simulation are sold separately.

ALTERA PLD SOFTWARE RUNS ON SUN COMPUTERS

Users of Altera’s erasable, programmable-logic devices (EPLDs) can now do their designs on a Sun workstation. The PLS-SN software is a set of EPLD design tools for the Sun Sparcstation and Sun 3 computers. In addition, Altera has an agreement with Valid Logic Systems to provide an EDIF-based interface between the Altera tools and Valid’s digital design environment. PLS-SN contains the Altera programmable logic-synthesis technology and a bidirectional EDIF 2.0 interface. Users can input a design with a variety of workstation-based schematic-entry tools. Also, they can use the Altera HDL to input a design behaviorally employing any workstation text editor. System-level verification is performed with an EDIF net list that has post-synthesis routing and delay information. This file can be read by any standard EDIF net-list reader. PLS-SN includes the Max+Plus compiler, EDIF net-list reader and writer, and simulation libraries for Valid Logic Systems and Viewlogic Systems. It’s shipping now for $9995.

ABEL DESIGN SOFTWARE OFFERS COMPLETE FPGA SOLUTION

Designers working with field-programmable gate arrays (FPGAs) can use ABEL-FPGA design software from project start to finish. The software, which is based on the ABEL design software, offers design entry, optimization, device fitting, and logic synthesis for all current FPGAs.

FPGA-specific capabilities include a DOS extended parser for handling the arrays’ larger logic modules. Also, extended ABEL-HDL features generate place-and-route constraints for FPGA architectures. Optimization features include criteria for net-list generation based on specific FPGA architectures. New menu features support the FPGA design flow.

ABEL-FPGA is built around device fitters, which are optimization programs that manipulate logic descriptions to best use specific device characteristics. In addition to the traditional pin and node assignments, macrocell configuration, and control-term configurations done by all fitters, the ABEL-FPGA device fitters automatically perform logic transformation, logic partitioning, and signal placement and routing tasks.

Behavioral entry can take the form of state machines, high-level equations, or truth tables. The software’s output includes vendor-specific net lists and vendor-specific constraint files. As a result, the same design can be migrated between multiple FPGA vendors. In addition, ABEL-FPGA automatically creates schematic symbols that can be used with schematic-capture tools to integrate the ABEL-designed behavioral models into the rest of the system design.

ABEL-FPGA costs $7995 for the IBM/XT and /AT, Compaq 386, IBM PS/2 Models 70 and 80, and compatible sites. Site licensing and box-of-5 and box-of-10 quantities are available. Delivery is in 2 to 4 weeks.

Data 1/0 Corp., 10266 Willows Rd., N.E., Redmond, WA 98052-9746; (206) 815-6441. CIRCLE 376

JOHN NOVELLINO

PSpice ADDS FEATURES FOR BETTER ANALYSIS

The improved 4.05 version of PSpice now offers more features, including Sun network licensing and pulse-width-modulator models. Parts sessions can be frozen and rerun at a later time. In addition, the number of states for digital simulation has increased from 28 to 246,528. This is due to the increase in the number of input levels from three to five, and an increase in the number of output strengths from 4 to 64. Optional power-supply pins were added to all of the parts in the digital library, giving users the ability to have more than one power supply in the circuit. The PSpice software runs on personal computers, Macintosh computers, and several Unix workstations. Pricing ranges from $950 to $5400, depending on the platform. Such options as digital simulation are sold separately.

MicroSim Corp., 20 Fairbanks, Irvine, CA 92718; (800) 245-3022 or (714) 770-3022. CIRCLE 375

ENHANCEMENTS EMERGE FOR SUSIE SIMULATOR

The ICMaker software from Aldec is a real-time VHDL-model generator that quickly creates new IC models by modifying the timing parameters of existing VHDL IC models. The models are then used with the company’s Susie logic simulator. ICMaker is shipping now for $995. The company is also announcing an EDIF interface between the Susie 6.0 simulator and Mentor-generated schematics. Susie 6.0 and the Mentor interface are being sold together for $9995. Finally, XNF/VT is a Xilinx cell library that allows for real-time simulation of multiple Xilinx parts at the system level using the Susie 6.0 simulator. The cell library is written in VHDL. With XNF/VT and Susie 6.0, users can display cells from different Xilinx parts on the same screen. In addition, users can observe in real time how a change in one cell affects the operation of cells in other Xilinx parts. The XNF/VT cell library includes the 2000, 3000, and 4000 series parts. It’s shipping now for $10295.

Aldec Co., 3525 Old Conejo Rd., Newbury Park, CA 91320; (805) 499-8867. CIRCLE 378

JOHN NOVELLINO

ELECTRONIC DESIGN 161

MAY 9, 1991
A full spectrum of choices.

<table>
<thead>
<tr>
<th>Device</th>
<th>Organization</th>
<th>Speed (ns)</th>
<th>Package</th>
<th>Micron Part #</th>
<th>Availability</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Meg DRAM</td>
<td>x4*</td>
<td>70 – 100</td>
<td>DIP, ZIP, SOJ</td>
<td>MT4C4256</td>
<td>Now</td>
<td>VGA 8514</td>
</tr>
<tr>
<td></td>
<td>x16*</td>
<td>80 – 100</td>
<td>ZIP, SOJ</td>
<td>MT4C1664/65/70</td>
<td>Now</td>
<td>Super VGA 540*</td>
</tr>
<tr>
<td>4 Meg DRAM</td>
<td>x16*</td>
<td>60 – 100</td>
<td>SOJ, TSOP</td>
<td>MT4C16256/7</td>
<td>Samp. Q4 '91; Prod. 1H '92</td>
<td>XGA MAC* Workstation Multimedia</td>
</tr>
<tr>
<td>256k VRAM</td>
<td>x4</td>
<td>100 – 120</td>
<td>DIP, ZIP</td>
<td>MT4C2064</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td>1 Meg VRAM</td>
<td>x4</td>
<td>80 – 120</td>
<td>ZIP, SOJ</td>
<td>MT4C20255/6</td>
<td>4255 Now; 4256 Q4 '91</td>
<td></td>
</tr>
<tr>
<td></td>
<td>x8</td>
<td>80 – 120</td>
<td>ZIP, SOJ</td>
<td>MT4C20127/8</td>
<td>8127 Now; 8128 Q4 '91</td>
<td></td>
</tr>
<tr>
<td>2 Meg VRAM</td>
<td>x8</td>
<td>70 – 100</td>
<td>SOJ</td>
<td>MT4C32256</td>
<td>Samp. Q4 '91; Prod. 1H '92</td>
<td></td>
</tr>
<tr>
<td>1 Meg Triple-Port DRAM</td>
<td>x4</td>
<td>80 – 120</td>
<td>SOJ</td>
<td>MT4C32257/8</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td></td>
<td>x8</td>
<td>80 – 120</td>
<td>PLCC</td>
<td>MT4C328128/9</td>
<td>Now</td>
<td></td>
</tr>
</tbody>
</table>

*Also in low power versions.
RF TESTERS EVALUATE EUROPEAN CELLULAR PHONE SYSTEMS

The HP 8922A transceiver test set and HP 8922B base-station test set are multifunction instruments aimed at the new Pan-European digital cellular telephone system. The HP 8922A contains all instrumentation needed to test the RF characteristics of the system's mobile units. The HP 8922B adds the ability to synchronize base stations to system clocks, as well as a large memory and state machine, which are needed to test base stations.

For transmitter measurements, the testers have a frequency-agile local oscillator, coherent data demodulator, pulse demodulator, FM demodulator, and pulse-power meter. A global-method analyzer tests phase and frequency. Modulation-spectrum measurements are made by a fully synchronized spectrum analyzer. The instruments use high-speed DSP algorithms for fast results.

In addition to these system-specific functions, the testers have several general-purpose instruments. They include a digital oscilloscope, CW frequency counter and power meter, ac voltmeter, 1-kHz distortion meter, audio-frequency counter, and synthesized audio source.

DEVELOPMENT SYSTEMS OFFER VERSATILITY

A family of microprocessor emulation and development systems offers hardware and software solutions for developers of various microprocessor-based systems. The low-cost Zaxpak 1000 products, which are based on the ICD emulator series, run in standalone mode or under control of most personal computers or workstations. The high-performance Zaxpak 2000 systems are based on the ERX line of emulators, which include a PC/AT bus interface. The Zaxpak 2000 Plus adds its own 386SX 16-MHz host to the 2000-series hardware. Systems come with an emulator, cables, and required software. For Ethernet environments, the Axi- spak includes Ethernet interface hardware and software. Zaxpak systems are available for immediate delivery at prices starting at about $8700.

SOFTWARE WRITES CODE FOR PC INSTRUMENTS

Working together with Burr-Brown's PCI-2002S-1 general-purpose software drivers, the SmartCoder software package simplifies programming of custom data-monitoring applications. The software supports all of the company's PC/XT/AT Personal Computer Instrumentation (PCI) boards, carriers, and modules. Users need not know the internal details of the hardware or the function of the drivers. Instead, they select menu items that represent information about the application and the installed hardware. SmartCoder then writes source code that initializes the hardware, configures the channels, and performs the needed analog, digital, and counter-timer tasks. SmartCoder is available from stock on 3-1/2- or 5-1/4-in. diskettes at a price of $95.

TEST SOFTWARE OFFERS VERY-HIGH FAULT COVERAGE

The CX-Test software combines with CrossCheck's patented on-chip test structures to efficiently create fully testable ASICs without the performance and functionality trade-offs typical of ASIC test development. With the fault simulation and test vectors supplied by CX-Test, typical fault coverage is 95% to 99%, depending on the ASIC design.

The software works with all types of designs, including synchronous and asynchronous, and chips with RAM or ROM. Gate counts of 10,000 to 100,000 are accommodated. CrossCheck says that CX-Test speeds test-writing time by a factor of 30 to 50 times, compared with other development methods. In addition to the commonly used stuck-at-zero and stuck-at-one faults, CX-Test covers actual manufacturing defects that may escape detection by other test techniques. These defects include open and shorted FETs, open and shorted interconnects, and bridging nets.

The CrossCheck approach to testability fits transparently into the ASIC design flow, requiring no change in established methodologies or tools and no insertion of dedicated test logic into the design. The ASIC manufacturer embeds the on-chip test structures in the base array and library without any intervention by the designer. CX-Test is designed to integrate into popular CAE environments. Presently, the software is available for use with Verilog from Cadence Design Systems and LSim from LSI Logic Corp. The release of CX-Test follows the recent introduction of LSI Logic's FastTest family of 100K HCMOS gate arrays, which are based on the CrossCheck embedded test structures.

Initially, CX-Test will be available in the ASIC design centers of chip makers that are CrossCheck partners. It's available now at LSI Logic design centers. Call Bill Alexander at (408) 433-4554. CrossCheck is scheduled to market CX-Test directly to ASIC designers during the second half of 1991.

JOHN NOVELLINO
A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

20 Fairbanks • Irvine, CA 92718 USA • FAX (714) 455-0554
ECL Clock Oscillator Is First With Enable/Disable

Until now, unlike HCMOS and TTL types, ECL clock oscillators have been unable to perform tristate functions. But the M1900 ECL crystal oscillator offers a tristate enable/disable function that lets the clock be shut off by logic control.

The M1900 oscillator’s enable/disable function is activated by logic levels on an input pin. Activation of this pin is achieved by applying a logic “1,” which turns off the oscillator. At the same time, this causes the device’s output pin to be ECL logic “0.” An external ECL signal may then be applied to the tester by the oscillator output node, which will follow the tester. Because of the wired-OR capability of ECL logic, this achieves the same effect as the HCMOS tristate.

In many applications, the clocking speed must be changed by selecting one or two or more active clock oscillators on a board. In TTL and HCMOS, this is done by tristating. ECL applications have in the past had to use AND/OR gates for this function. But with the M1900 oscillator, the outputs of several oscillators may be tied together while only one is enabled. The M1900 oscillator comes in frequencies from 10 MHz to 225 MHz. Packaging is a four-pin, dual-in-line metal case. Delivery is from stock. Call for pricing.

New Products

64-Megabit CMOS SRAMs

Big Memory, Small Package!!

Here’s 64-Megabits of CMOS SRAM memory we’ve just packed into a 120-pin 3” x 3.5” x 0.32” ceramic flatpack. Just right for designs that need a lot of memory, space is scarce, and temperature is a factor.

Look at these key features:
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  120mA Operating Current
  1mA Data Retention Current
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• Temperature Ranges
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  Industrial: —40°C to +85°C

• Screening and Burn In to Military Standards Are Available Options
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And, if you’re after non-volatile memory, we have that too. We have an 8-Megabit Flash PROM in a 34-pin package, and we’re working on a new 128-Megabit Flash PROM in a 3” x 3.5” flatpack. We also have a large selection of SRAMs and EEPROMs to fit almost every memory size and package requirement.

More? Yes, much more. We’re designing memory systems in the terabit regions, and if you’re looking for a complex single-package system, a supercomputer array, or a totally defined multi-package management information system, give us a call. Your imagination or ours, we’ll make it happen.

White Technology, Inc.
A wholly owned subsidiary of Bower Instrument Corporation
4246 E. Wool Street • Phoenix, Arizona 85040
Tel: (602) 437-1520 • FAX (602) 437-9120

64-Megabit CMOS SRAM

DT2404 display comes with an RS-232 interface and power supply. Other features include bottom-line scrolling and an audible-alarm option. Pricing is $800 per unit. Small quantities are delivered from stock.

Telegenic Inc., P.O. Box 5550, Cherry Hill, NJ 08034; (800) 424-5220.
DENSE, HIGH-REL DC-DC CONVERTER SPORTS CURRENT-SHARING ABILITY

Until now, true high-reliability dc-dc converters have been available only in power levels below 70 W. For higher-power applications, designers have had to settle for "pseudo-military" or "ruggedized industrial" converters that don't span the full military-temperature range and can't pass military qualification. Interpoint's MFL series, however, is a true high-rel unit that uses current-sharing to nearly triple the power range for military/aerospace-grade dc-dc converters.

Thanks to a high-frequency pulse-width-modulation design, Interpoint claims a record power density for its individual MFL converters—up to 40 W/in.². Case measurements are 3 by 1.5 in., with a height of just 0.385 in. The parts are designed for either 28- or 270-V dc input (per MIL-STD-704D), and provide outputs of 5, 12, 15, 28, ±12, or ±15 V at up to 65 W per unit. The modules' input range is 16 to 40 V dc.

The 65-W rating is within the ballpark of other regulators. What sets the MFL Series apart is its current-sharing capability. Three MFL units in parallel generate about 200 W of output power. Typical series performance includes up to 85% efficiency, up to 50 dB of audio rejection, and line and load regulation of 15 mV. Without external components, the converters meet MIL-STD-461C CS01 and CS02 susceptibility standards. With companion EMI filters, they meet MIL-STD-461C CE03 emission limits.

Prices start at $690 in lots of 100. Availability begins May 30.

Interpoint Corp., P.O. Box 97005, Redmond, WA 98073-9705; (206) 882-3100. CIRCLE 334

LOW-NOISE SUPPLIES PRESENT DUAL RANGES

LOW-NOISE SUPPLIES PRESENT DUAL RANGES

LEDs. List prices are $300 each. Units are available now.

Hewlett-Packard Co., 19301 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. CIRCLE 336

40-W SUPPLY OFFERS THREE OUTPUTS

A 40-W, triple-output supply measuring just 3 by 5 by 1.35 in. has been added to the International MAP family. The line now offers 27 models in a power range spanning 40 to 130 W. The MAP40-3000 has outputs of ±5 V at ±3 A, ±12 V at ±2.5 A, and ±12 V at ±0.5 A. Automatic ac-input selection permits worldwide operation over the range of 90 to 264 V ac. Onboard FCC and VDE filtering meet the Class B conducted-emissions requirements. The supply features tight load regulation of ±0.5% for the main output and ±1% for the others. Output noise and ripple is less than 1% peak to peak over a 20-MHz bandwidth. Pricing varies with quantity ordered. Delivery is from stock.

Power-One Inc., 740 Calle Plano, Camarillo, CA 93010-5853; (805) 987-8741. CIRCLE 339

TINY POWER MODULES RUN FROM +5-V INPUT

Two series of power modules deliver highly reliable power to digital and communications applications. The 112- and 113-Series modules are non-isolated switching regulators that operate from a +5-V dc input. Output voltages of +12, 15, and 25 V are provided by the 112-Series units, while outputs of ±5, 12, 15, and 130 V make up the 113-Series units. Minimal external filtering components are required. In lots of 100, the price is $28.60 per module. Samples are available now.

AT&T Microelectronics, Power Systems Business Unit, 3000 Skyline Dr., Mesquite, TX 75149; (800) 526-7819. CIRCLE 337

MODULZ GIVE 3.3 V OUT FOR 7-TO-35-V IN

Have some of your CMOS ICs moved to 3.3 V, thus requiring a stiff, clean, 3.3-V bus to run them off? If you possess a 7- to 35-V source, Modupower's MP7008 can provide up to 1 A of line- and load-regulated 3.3 V. The MP7104 supplies the same current at a regulated 3.3 V from a 4.5-to-10-V rail. These low-cost, 1.5×1×0.5-in. encapsulated modules are non-isolated dc-dc converters that offer high efficiency (over 80%). Unlike most other modules, these offer self-protection in the form of current-limiting and thermal shutdown. In addition, a shutdown pin, usually connected to ground, is provided. In the case of an external fault detected by a watchdog circuit, or to reduce power, pulling the pin to 5 V reduces the output voltage to zero and the quiescent current to 500 µA. Initial voltage is within 5% of 3.3 V and regulation is within ±5% over specified line and load changes. Quiescent current is 20 mA and output ripple is 50 mV pk-pk. In quantities of 1000, the converters run $1.15 each.

Modupower Inc., 374 Turquoise St., Milpitas, CA 95035; Art Fury, (408) 263-6115. CIRCLE 338
EMPLOYMENT OPPORTUNITIES

ELECTRONIC-ELECTRICAL ENGINEERS. Nationwide Design/Project/ QC/Mfg., Power, Software/Systems, Controls, Circuits, Equipment, Test, Communications, etc. Contact: John Longberry, Longberry Employment, 913 Main Place, P.O. Box 471, Niles, OH 44446. (216) 652-5871.

CONSULTANTS

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- BSEE's (no EET degrees) with 5 years current RF (UHF/VHF) experience specifically in a.m. receivers and multichannel synthesized f.m. transmitters. Small stowable antenna design is highly desirable. U.S. citizenship required for clearance.

- BSME's (no MET degrees) with 2 to 5 years current experience in the design of injection molded plastic, die cast metal, and stamped metal parts for a high volume/low cost manufacturer. Solid experience in finite element analysis (FEA) and knowledge of design for assembly (DFA) concepts is highly preferable. Tooling vendor interface and production floor support backgrounds are necessary. U.S. citizenship is required for clearance.

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SPARTON DEFENSE ELECTRONICS
ATTN: Mr. John S. Gould, Employment Manager
5612 Johnson Lake Road
DeLeon Springs, Florida 32130

BUSINESS SERVICES

LITERATURE

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ELECTRONIC DESIGN

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So, for the strength and security of the largest 1-Meg SRAM family, look to Sony. You’ll find us at Sony Corporation of America, Component Products Company, 10833 Valley View St., Cypress, CA 90630. For details, call us at (714) 229-4190, FAX us at (714) 229-4285, or write to us “Attn: Communications.”

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