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Process merges tungsten deposition and etchback
Submicron biCMOS packs 300 kga/Chip

X-Window gets true colors simultaneously
Instant gate arrays have wiring configured by laser
GaAs comes of age in low-cost satellite downconverter

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The ins and outs of designing with DSP chips
Using new delta-sigma d-a converters
First details on new mixed-signal simulators
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CIRCLE 109

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Noyce on Education
It's already been a couple of months since Robert Noyce died in Austin, Texas, where he moved to direct operations at Sematech, the consortium for semiconductor manufacturing technology. Noyce's last interview may have been one of his most profound, published in the July/August, 1990 issue of Intel Corp.'s house organ "Microcomputer Solutions." Here he noted, among other things, "We need to decide now whether we are going to make an investment in education. The outcome of that decision will be with us for the next 40 to 50 years."

Few will deny that Robert Noyce earned the right to predict for the next 40 to 50 years. His achievements—as the co-inventor with TI's Jack Kilby of the integrated circuit and as a co-founder of both Fairchild Semiconductor and Intel Corp.—will be with us for at least that long. And his comments on education, albeit posthumously recorded, are again right on target.

With all due respect to the leaders of the American education system, we believe that few experts exist in the process of education—at least not as expert in the same sense that Noyce was an expert in semiconductor technology. Education is not a rigorous science, as is physics—cause and effect in people are not as predictable as, say, the movement of electrons in a conductor or semiconductor. Just about the only common link between the two disciplines is that, in today's world, there won't be much progress without large upfront investments. But successful education programs involve more than money. The home and community environment must actively support the education process, and there must be a promise of employment opportunity when the education is completed.

The tributes to Noyce have been offered, the eulogies have been delivered. What could possibly remain to be said? Perhaps nothing need be said. Perhaps what's needed is action.

Stephen E. Scrupski
Editor-in-Chief
dc to 2000 MHz amplifier series

SPECIFICATIONS

<table>
<thead>
<tr>
<th>MODEL</th>
<th>FREQ. MHz</th>
<th>GAIN, dB</th>
<th>MAX NF</th>
<th>PRICE $</th>
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<td>MAR-1</td>
<td>DC-1000</td>
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<td>0 5.0 0.99 (100)</td>
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<td>-3 6.5 1.50 (25)</td>
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<tr>
<td>MAR-8</td>
<td>DC-1000</td>
<td>33 23 19 10</td>
<td>35 5.0 1.90 (25)</td>
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</tbody>
</table>

NOTE: Minimum gain at highest frequency point and over full temperature range.

Unbelievable, until now... tiny monolithic wideband amplifiers for as low as 99 cents. These rugged 0.085 in. diam., plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-A, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1.

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.

<table>
<thead>
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<td>X7R</td>
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<tr>
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<td>10%</td>
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<tr>
<td>120 x 60</td>
<td>10%</td>
<td>X7R</td>
<td>022, 047, 068, 1µf</td>
</tr>
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Minimum Order 50 per Value

Designers kit, KCAP-1, 50 pieces of each capacitor value, only $99.95

Designers amplifier kit, DAK-2
5 of each model, total 35 amplifiers only $59.95

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CIRCLE 104
TECHNOLOGY BRIEFING

GRAPHICS MATURE, BUT AT WHAT PRICE?

Displays on graphics workstations are nearing the point where the improvements in resolution are no longer easily noticeable by the human eye. On the other hand, monitor manufacturers are struggling to keep up with rapidly rising pixel refresh rates now possible with higher-speed ICs. However, such performance improvements—higher resolution and faster refresh rates—are expensive. The question is: How much will users pay for this high performance? Makers of high-end graphics systems will be looking for conclusive evidence, one way or the other, as they display their wares at the Siggraph '90 Computer Graphics Conference, August 6th to the 10th, in Dallas, Texas.

In today's market, a 1280-by-1024 monitor's cost (about $3000) is about the most users seem willing to spend on a display. Units with a resolution as high as 2048-by-2048 pixels are available, but they still cost much more: up to $50,000 with today's technology, primarily because of expensive CRT technology. As manufacturers begin to supply users with alternative, potentially lower-cost technologies, such as color LCD, high-res display prices should start to drop. This may even put added pressure on CRT developers to innovate lower-cost CRT technology.

Consequently, the next few years will see only those users who need high resolution move to 2048-by-2048 displays. Rather than higher resolution, the most significant improvements probably will be refinements in CRT design to improve overall display quality and convenience (such as flat, thin displays, shorter depths, etc.), or in high-resolution flat-panel screens, making them larger (greater than 15-in.-diagonal) at an affordable price.

For example, Dolch Computer Systems, San Jose, Calif., developed a mere 10-in. display with a resolution of 640 by 480, which represents a solid starting point for the active-matrix LCD technology. Using a thin-film transistor (TFT) method, the Dolch VGA-compatible display is a step above standard electroluminescent or gas-plasma displays. It boasts a contrast ratio of 100 to 1, five times that of conventional LCDs and a typical response time of just 40 ms, compared with the LCD's usual specs of 300 ms.

One key issue facing graphic-workstation designers is integrating different data-handling functions, such as image processing, volume rendering, and interactive graphics. Users typically would prefer to perform all of their graphic analyses on one system, rather than jump from one specialized system to another to get the optimum data-displaying method. Because the need for visualization and the amount of data that requires the integrated technologies has grown so rapidly, workstation makers had to turn integration from wishful thinking into reality.

Another issue to be discussed at Siggraph involves tuning up the graphics processing system. Producing graphics involves more than just displaying an image. Many imaging requirements reside in a "graphics" environment in order to offload the CPU from graphic-specific tasks. As a result, it's free to handle memory and move data around quickly. The graphics processor then performs the graphics-oriented operations, such as zooming, panning, rotations, and clipping. Users are now finding that the bottleneck once located in the processor has shifted. Statistics indicate that up to 80% of computing time is spent processing I/O information to disks, peripherals, or to the graphics subsystem. The standard solution of increasing the processing power won't help ease the bottleneck. Therefore, it's likely that vendors will now focus their resources on increasing I/O performance. I/O specifications will be highlighted instead of the MIPS that are always tossed about. And because the high number of MIPS can't be utilized effectively, those numbers may be leveling off.
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**Low Pass dc to 1200MHz**

<table>
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**High Pass dc to 2500MHz**

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<td>PHP-100</td>
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**Bandpass 20 to 70MHz**

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<tr>
<th>MODEL NO.</th>
<th>CENTER FREQ. MHz</th>
<th>PASS BAND, MHz (loss &lt;1dB)</th>
<th>STOP BAND, MHz (loss &gt;10dB)</th>
<th>VSWR, 1.5 typ. band typ.</th>
<th>PRICE $</th>
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<tbody>
<tr>
<td>PIF-21.4</td>
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<td>PIF-30</td>
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**Narrowband IF**

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<th>STOP BAND, MHz (loss &gt;10dB)</th>
<th>VSWR</th>
<th>PRICE $</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBP-10.7</td>
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<tr>
<td>PBP-21.4</td>
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<td>21.4</td>
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<td>21.4</td>
<td></td>
</tr>
</tbody>
</table>

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1-MINUTE OPINIONS

Is the IEEE truly serving its membership?

I've been an IEEE member for 12-plus years now, with no regrets at all. There is a lot of voluntary work involved, so you can't complain too much. Some of the publications are great; I have a large pile that I haven't read through. There are a lot of academic papers—I would like to see more practical examples that I can immediately come to grips with and apply in my work. James D. Traill, Tokyo, Japan.

For a not-for-profit organization with so many volunteers in different societies, I believe IEEE is serving its membership. I do not mean that there is no room for improvement. However, in the local chapter that I belonged to, there are so many workshops and seminars—from how to grow in your own profession to how to start your own business. A lot of time and energy has been put in by those volunteer organizers. It is a self-service organization. I don't think it is fair to lay back and say that it didn't serve me well enough. Janpu Hou, Bridgewater, N. J.

What is the goal of the IEEE? Is it to help distribute information and push forward technology? I think that these are the goals of the IEEE and the IEEE is doing fine on these goals. I do not feel that the IEEE needs to be a union for engineers; nor should there be a union for engineers. Richard Lokken, Milwaukee, Wis.

Instead of surveys and public opinion polls, which seem to have the intent of IEEE bashing, you would serve your engineering readers better by sending your writers out to report the actions taken by IEEE PACE groups.

How can your readers know that despite any hearsay resulting from the previous reputation of the IEEE, that there are volunteers working within the IEEE structure to help the “working” engineers, including the unemployed? The tone set by your magazine in both "1-Minute Opinion?" and the career survey is such that it debases the efforts of the IEEE volunteers.

In addition to the EA, the IEEE has on-line services for jobs. It has a national network, plus local BBS services, which on Long Island include a message area: "jobs for LL engineers." A number of IEEE volunteers have been fighting what they call ESP—engineering shortage propaganda. We have other groups—the Consultants Network, the Retired Engineers, and the group that I chair: the Small Business Development Group for engineering entrepreneurs and engineer-owned businesses.

Remember, the IEEE is a volunteer organization. Anyone with a complaint about what the IEEE does (or does not do) needs only to become an active member to be able to participate with us in improving the member services. Marlene S. Farber, East Meadow, L. I.

What's your opinion on the IEEE? ... or how about the importance of analog design skills. ... or the quality of today's EE graduates. See the table of contents (p. 5) for a complete list of questions and fax your opinions to (201) 393-0637. Or mail your opinions to Quick Look, Electronic Design, 611 Route 46 W, Hasbrouck Heights, NJ 07604.

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CAE SURVEY

Which systems do you use for automated design (including CAE or CAD), 1990 vs. 1989?

<table>
<thead>
<tr>
<th>System Type</th>
<th>1990 Percentage</th>
<th>1989 Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standalone PCs</td>
<td>71.1%</td>
<td>72.9%</td>
</tr>
<tr>
<td>Standalone engineering</td>
<td>52.7%</td>
<td>43.2%</td>
</tr>
<tr>
<td>Multiuser workstation networks</td>
<td>45.2%</td>
<td>37.2%</td>
</tr>
<tr>
<td>PC networks</td>
<td>44.9%</td>
<td>33.7%</td>
</tr>
<tr>
<td>Minicomputer host systems</td>
<td>32.7%</td>
<td>28.0%</td>
</tr>
<tr>
<td>Mainframe host systems</td>
<td>23.8%</td>
<td>22.5%</td>
</tr>
</tbody>
</table>

Source: Survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

HOT PC PRODUCTS

With line powering, a compact, 2400-baud modem works without an ac adapter or internal batteries. The Stowaway 2400 modem from Vocal Technologies Ltd. instead derives power from its serial port connection to a computer and from the phone line, which is how conventional telephones operate. Compatible with the AT command set, the modem, which has dimensions of 2.2 in. by 3 in., slides easily into a shirt pocket or the pouch for a laptop or notebook computer.

Because it can be tucked behind other equipment and doesn't need to be monitored, the modem also may find use in embedded applications. The Stowaway 2400, which sells for $295, is available from Vocal Technologies, 3032 Scott Blvd., Santa Clara, CA 95054; phone (408) 980-5181; fax (408) 980-8709.
Which technical books are the most popular in Silicon Valley?

**ELECTRONICS**

5. **Art of Electronics**. Paul Horowitz, Winifred Hill. Cambridge University Press. $49.50.

From Stacey's Bookstore, 219 University, Palo Alto, CA 94301; (415) 326-0681.

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TECHNOLOGY NEWSLETTER

MOLDING COMPOUNDS HASTEN IC DEMISE
An important cause in the degradation of the intermetallic region of the gold-wire-to-aluminum-bonding-pad interface has been identified in several types of IC devices. In a paper presented at the International Reliability Physics Symposium in New Orleans in March, it was reported that antimony trioxide—a common component of semiconductor molding compounds—is the overriding factor in causing “ball lift,” leading to a near-complete loss of bond strength. The test results, reported by scientists from Dexter Electronic Materials, Olean, N.Y., contrast sharply with earlier reports that antimony trioxide improves wire-bond reliability in dry environments. Dexter disclosed that the commonly used substance actually weakens many molding compounds. Using ion-seaeveng additives with specific types of flame retardants solves the problem. Dexter's scientists believe that their test procedures will help screen molding compounds and benefit many applications. DM

ASIC MAKERS PROMOTE STANDARD TEST PORT
Several leading ASIC suppliers have formed a specification group to enhance and promote a standard test-access port for on-chip test structures developed by CrossCheck Technology Inc., San Jose, Calif. The group's first meeting discussed how to improve and extend the test circuitry while ensuring compatibility with independently developed application software tools, such as fault-simulation and automatic-test-pattern-generation (ATPG) programs. With a standard port, ASIC designers could use the same application software to design ASICs with different suppliers. Members include Fujitsu Ltd., Harris Semiconductor Corp., LSI Logic Corp., and Raytheon Co. The group, all of which are licensees of CrossCheck technology, decided that the test port should be usable as a standalone port or with the IEEE-1149.1 test-access port for board testing. The patented test structure is a grid with many test points embedded in the ASIC's base array. Using the grid and specially developed ATPG software, designers can get faster high fault coverage than with conventional techniques. JN

SERVER BRINGS BACK MINI MEMORIES
The recently announced VAX 4000 model 300 “server” from Maynard, Mass.-based Digital Equipment Corp., closely resembles the mimicomputer of yesteryear. The VAX is the first that DEC designed and optimized specifically for client-server operation, coming on the heels of the company's proclamation that client-server computing will rule in the 1990s. Fully compatible with other members of the VAX family, the server can utilize the extensive library of existing application software. The pedestal-enclosure machine occupies less than 20 ft.² and doesn't require any special air conditioning or a separate computer room. Systems start at $127,000. The server, as well other products, were announced at DECWorld '90. RN

SMART MODELS RUN SIMULATIONS WITH MAX
Board-level simulation with the Max family of erasable programmable logic chips from Altera Corp., San Jose, Calif., has just become possible thanks to behavioral software models created for the EPLDs. The simulation models, called SmartModels, from Logic Automation Inc., Beaverton, Ore., enable designers to simulate the EPLDs as standalone devices and simulate the entire system, into which the EPLDs are inserted. One option available for the models is a “window” feature that allows designers to view some of the inner workings of the EPLDs. With the window viewports, designers can set breakpoints, single-step through instructions, change register values, and group various registers or bits together to form a cluster that can be observed as one entity. SmartModels will be available next quarter for the four current Max family members, and for two soon-to-be-released additions to the Max EPLD family. Contact Rick Denker at Logic Automation, (503) 690-6900. DB

HDTV'S FIRST IMPACT TO HIT COMPUTER INDUSTRY
ACM Siggraph, the Association of Computing Machinery's Special Interest Group on Computer Graphics, forecasts a greater emphasis on computer graphics applications as high-definition television (HDTV) shifts into niche markets. According to ACM's report, "HDTV & the Quest for Virtual Reality," HDTV will influence the evolution of desktop workstations significantly. According to the study, HDTV and workstation designers must replace bulky CRT screens with flat-panel displays, and adapt to higher-capacity communications channels. The study examines the current state of HDTV hardware and the probable future direction of the technology and its marketplace. The study, which was recorded on videotape, serves as a buying and planning guide for users with...
production and closed-circuit applications. It offers manufacturers, programmers, and educators a thought-provoking analysis and forecast of the HDTV movement. Also, the debate on standards, program delivery, and interactivity is addressed. The report was released at the Siggraph '90 conference. For information on obtaining the tape, call (800) 523-5503. RN

SPICE MODEL CREATES BETTER GaAs ICs

By correcting several deficiencies in existing models, a new Spice model allows designers to more accurately represent GaAs metal-semiconductor field-effect transistors (MESFETs). For instance, in most existing Spice models (like Raytheon-Statz Spice models), the correct drain conductance can be predicted only for a small range of drain current values. The new model, developed by TriQuint Semiconductor Inc., Beaverton, Ore., rectifies this problem by making pinch-off voltage a function of drain voltage, and by correcting self-heating more efficiently. It also incorporates several features unique to GaAs technology, and more accurately predicts small-signal parameters over many bias conditions. As a result, the improved model delivers more realistic results for gain compression and other nonlinear parameters. The model is available now to TriQuint customers, and may soon be included with commercial Spice programs. For more information, call (503) 644-3535. LG

MEGABIT FLASH EPROM PERFORMS SECTOR ERASE

Unlike the simple flash memory chips that just erase the entire chip, a 1-Mbit flash memory’s space divided into 128 sectors of 1 kbyte each. Each sector of the 128-kword-by-8-bit memory from Philips Components-Signetics Corp., Sunnyvale, Calif., can be erased and rewritten independently. The entire chip can also be erased, as is the case with the simpler chips. The 48F010 is the first flash memory chip from Philips-Signetics to come as a result of a technology-sharing agreement inked between Seeq Technology Inc., San Jose, Calif., and Philips in the fall of 1989. Philips is an alternate source for the previously released Seeq megabit flash memory. Data in the 48F010 can be read in 200, 250, or 300 ns (depending on the speed grade), and can be stored in just 0.5 ms/byte. The 48F010 requires a 12-V supply for the erase/program cycle and can endure 100 such cycles; screening can yield units with 1000-cycle ratings. Future chip versions will be able to endure up to 10,000 erase-program cycles. DB

PROCESS Merges Tungsten DEPOSITION, EThBACK

An integrated metallization system to create interconnections, or vias, between metal layers in multilayer ICs has been developed to reduce wafer-processing cycle time and particle-induced defects. The system, developed by Applied Materials Inc., Santa Clara, Calif., combines chemical vapor deposition (CVD) of tungsten with tungsten etchback and maintains the wafer under vacuum throughout the processing sequence to avoid airborne contaminants. After receiving the CVD tungsten deposition, the wafer is then transferred to the etchback chamber where a magnetically enhanced reactive ion etching removes the tungsten blanket at a rate greater than 7000 A/min, but leaves tungsten in the contacts or via holes. At this point, the etch system removes any residual tungsten and the adhesion layer on the oxide surface using a highly selective overetch step. To prevent plug recess, the system—called the Precision 5000 WCVD—uses an endpoint-detection scheme based on multiline optical emission. This detects the interface between the blanket tungsten film and the underlying adhesion layer. ML

SUBMICRON BiCMOS Packs 300 KGates/Chip

A next-generation biCMOS process with drawn features as small as 0.8 µm makes it possible to pack 300,000 gates on a chip. Up to 120,000 ECL gates (including embedded RAMs), or 200,000 to 300,000 biCMOS gates, as well as mixed ECL, TTL, or CMOS I/Os can be integrated. Dubbed ABIC IV (advanced biCMOS IV) by its creator, National Semiconductor Corp., Santa Clara, Calif., the process can implement loaded ECL gates with delays as short as 50 ps biCMOS gates with delays of less than 200 ps, and CMOS gates with loaded delays of about 400 ps. The process employs twin buried layers and double-diffused npn transistors to get 15-GHz cutoff frequencies for the bipolar devices. In addition, contactless self-aligned structures with polysilicon sidewall silicidation are used. Silicide also coats the source, drain, gate, base, and emitter regions to reduce contact resistances. Short polysilicon local interconnections are also silicided. Tungsten plugs are used in the dielectric contact holes between metal layers so that subsequent metal layers are deposited on planar surfaces, thus eliminating step-coverage problems. With the planar layers, four levels of metal can be used for device interconnections, resulting in high wiring densities. DB
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- VSBRAM-EC1: Features include "extra-bit" EDC and dual 64-bit caches for simultaneous transfer capabilities. Dual-ported for the VMEbus and VSB subsystem bus, the VSBRAM-EC1 is available in 2 to 64 MB densities.

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Offer expires October 31, 1990.
X-WINDOWS GETS TRUE COLORS SIMULTANEOUSLY

Thanks to a RAMDAC with a unique architecture and a virtual-resource scheme, X-window terminals can now have true colors simultaneously for all windows. The RAMDAC, dubbed the Bt463, was developed jointly by Brooktree Corp., San Diego, Calif., and Digital Equipment Corp., Maynard, Mass. The chip's virtual-resource scheme enables each X-terminal window to have its own color map and the associated pixel data that's structured uniquely by the graphics chip without any color degradation.

The Bt463 operates at 110 to 170 MHz and is the first commercially available monolithic IC that offers a high-resolution true-color palette (see the figure). According to Brooktree, the device's mapping functions are completely different from any other RAMDAC's, and is the key to its performance.

The chip's lookup tables have enough storage space to switch between a full eight-plane pseudo-color and a full 24-plane true-color display. By adding the pixel-mapping function, called window-type tables, the lookup table can be subdivided into 16 smaller tables, depending on the window types being supported. The window-type tables offer the ability to switch on a pixel-by-pixel basis for different visual types (gray-scale, true-color, or pseudo-color). In addition, they make it possible for a window to be set at any depth. For example, one window can have a 24-plane true-color format, another a 12-plane true-color format, and still another an 8-plane pseudo-color or gray-scale format.

The Bt463 is constructed so that each residing application can have control over its own lookup table. Before the Bt463, the application that last touched the lookup table (the application on top) would modify the table. This confused all of the other applications running on the screen at that time.

At 170 MHz, the chip can achieve 1/2-pixel resolution—at 110 MHz, that equates to 1/4-pixel resolution. The chip, which contains a standard microprocessor interface, isn't designed exclusively for DEC hardware. It isn't X-window specific either, just window specific.

The chip's pixel ports are reconfigurable on a pixel-by-pixel basis, offering the flexibility for multiple display modes. The reconfigurability feature also makes the frame buffer more efficient because the same buffer can be used for pseudo- and true color.

The RAMDAC lets DEC—one of the key instigators behind the X-window software standard—promote the graphical user interface as a standard more easily.

RICHARD NASS

INSTANT GATE ARRAYS HAVE WIRING CONFIGURED BY LASER

A proprietary laser-patterning process has been developed that eliminates many drawbacks of other fast-turnaround patterning schemes. It also lets premetalized gate arrays be configured in minutes. By predefining a two-level metal X-Y matrix of wiring above the gate array, Chip Express Corp., Santa Clara, Calif., can pattern both layers at the same time, thus eliminating processing steps of other fast-turnaround gate arrays.

That promises to reduce the turnaround time for gate arrays to 1 to 5 days. Although the scheme can theoretically work with almost any gate array, its key is the custom X-Y wiring grid for each array family. However, to ensure no hitches on the first product release, the company, along with International Microelectronic Products Inc., San Jose, Calif., developed its own family of gate arrays with predeposited metalization grids. The CMOS arrays have 3000, 6000, and 10,000 gates, and typical loaded gate delays of 500 ps.

Because the grid sits atop a standard chip, the company expects utilization to be near that of fully mask-configured arrays. To "instant" program a gate array, the base array is coated with metal. The metal is then patterned to form the first-level grid, an oxide insulating layer is deposited, and the second metal level is deposited and patterned. Tiny window regions are next etched away in the oxide regions formed between the grid of second-layer metal lines, to expose the programming points on the first metal layer (see the figure, p.36, left port).

For accurate laser positioning and minimal vaporized aluminum-wiring redepositing, a thin, proprietary antireflection material is deposited over the chip surface. Wafers can then be stockpiled for configuration at any time. An array is configured under the proprietary Quick laser-micromachining system. About an hour later (for up to 12,000-gate arrays), a configured chip
emerges (see the figure, right part).

Post-processing removes the antireflection coating and any redeposited aluminum. A sealant cap layer is used to protect the chip. Chips can then be tested with customer test vectors and then delivered.

All of this works well for a few chip samples with a turnaround of 1 to 5 days. However, when a few dozen to a few hundred chips, there are two alternatives through IMP. The first is the OneMask production option, which allows all metal lines to be patterned in a single etch step. Most double-level-metal arrays require four mask steps to custom-create the two wiring layers, resulting in a much longer processing cycle. For major production volumes, the second option lets IMP create custom metal masks for the Chip Express arrays to further optimize performance. For either option, customers can deal directly with IMP.

Chip Express doesn’t plan to sell its laser system initially, but hopes to become a “service house,” making possible designs in either of two modes. Customers can provide a circuit netlist and test vectors created with the library of macrocells supplied by Chip Express and standard tools from popular workstation vendors. Chip Express will then do the layout (a fuse cut list) and supply post-layout parameters for final simulation before signing off.

Alternatively, customers can purchase the layout software tools from the company and do all placement and routing. Then they just supply a final approved fuse pattern and test vectors.

Contact Adi Gamon, (408) 988-2445.

DAVE BURSKY

**GAAS COMES OF AGE IN LOW-COST DOWNCONVERTER**

Gallium arsenide’s days as a bridesmaid may finally be over. For years, proponents of GaAs technology have predicted that the material’s time was just around the corner. It took longer than originally thought to turn that corner, but Anadigics Inc., has done so. The Warren, N.J., company is producing more than 70,000 GaAs downconverter ICs a month to fulfill a 1-million-piece order from British Satellite Broadcasting. This is the largest production run of any GaAs IC. The Anadigics low-noise block downconverter is mounted in the Ku-band antenna’s feedhorn. The circuit drops the incoming 11.7-to-12.5-GHz signal to 950-to-1750 MHz, a frequency range than can be sent through coaxial cable to the indoor direct-broadcast satellite (DBS) receiver. The downconverter and a preceding two-stage low-noise amplifier also boost the signal by 50 dB (see the figure). The Anadigics IC replaces more than 50 discrete components used in older-generation downconverters.

To win the British Satellite order, Anadigics had to come up with a way to produce large numbers of GaAs ICs with a higher yield and lower price than is typical for the GaAs industry. To do that, the company bought moderately priced, commercially available equipment and modified it to fit the project’s needs. Production technology was also improved to increase yields.

Furthermore, the company developed a quick-turn design cycle that went from mask tape to device to evaluation in just 2 weeks. The whole cycle requires only 4 weeks, compared with a typical 16 weeks.

The chip was packaged in a modified TO-5 can that costs less than $1, rather than the $10 or more for a specialized microwave package. In fact, the whole chip sells for under $8. The discrete components being replaced cost from $5.50 to $7, depending on quantity.

However, the IC also permits a smaller and simpler antenna, reduces manufacturing and test costs, and improves reliability and consistency.

The 12-GHz Ku-band transponders, which have transmitters in the 100-W range, make it possible for home receivers to use antennas of less than 1 m and costing about $500. This compares with C-band systems in the U.S. with 3-m antennas and price tags of $1500 and up.

JOHN NOVELLINO
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Device Technology
CIRCLE 131
A 1983 concept that's still an innovation - Ericsson component power

If you've only just discovered the economy, reliability and flexibility of component power, don't worry. Even some power supply manufacturers think it's new!

In fact, component power concept - using very efficient, high frequency DC/DC converters as complete power 'components' for distributed power architecture - was introduced by Ericsson way back in 1983. And EriPower™ modules have since been proven in thousands of applications worldwide.

The first product, the PKA 25 to 40 Watt converter, set the standard and is still the market leader by far. Using hybrid construction and 300 kHz switching it's the world's smallest converter to offer full power operation at 85°C. And with ceramic capacitors for filtering and effective thermal management design, it has a demonstrated MTBF of over 200 years!

This same concept applies to the 15 and 18 Watt PKC. With a footprint smaller than a credit card, these sub-miniature converters offer the unique option of In-Card low profile mounting. The mechanical design allows the center of the module to rest in a slot in the PCB, giving a maximum height of just 8.5mm. The PKA and PKC can be easily paralleled for higher power applications and they make ideal components for n+1 parallel redundancy applications.

If your product demands innovative power supplies, yet needs the security of well proven solutions from a reliable source, call Ericsson. And let our technology lead help maintain yours.
One of the most difficult aspects of high-speed system design is distributing minimal-skew high-speed clock signals across one or several circuit boards. Often, board designs have to be "tuned" by adding inverter strings or delay lines to reduce clock skews. Such tuning lowers the maximum performance because the board must operate with worst-case trims. Yet another problem is distributing high-speed clock signals across multiple circuit boards so that the clocks can all be synchronized.

Although ECL systems have dealt with both issues for years, the latest crop of high-speed TTL-compatible systems now face this same problem as clock speeds go to 33 or 50 MHz and beyond. A 5-ns clock skew across a large board or system caused by improper buffering or system design could detract as much as 20% from the throughput in systems that run at 40 MHz.

By trimming the clock skew between clock output lines to less than 500 ps, most skew-related performance degradations can be eliminated. A pair of gallium-arsenide-based timing support chips, the GA1110 and 1210 from Gazelle Microcircuits, accomplish just that. They offer flexible and programmable control of timing-signal edges for systems with clock frequencies of 25, 33, 40, or 50 MHz, or with double-frequency clocks of up to 100 MHz.

The GA1110 can generate as many as five TTL clock signals that are phase- and frequency-synchronized to a master clock, adjust the clock edges in 2-ns steps, and buffer the clock signals for distribution. The GA1210 generates multiple output-clock signals at double the input frequency. Those clocks are also phase-aligned to the input clock.

In its basic configuration, the GA1110 serves as a multiple-output, zero-skew clock buffer. Inputs and outputs are all TTL compatible, with each...
output able to deliver symmetric waveforms with an output drive of \( \pm 24 \text{ mA} \). Output lines can be paralleled if higher drive currents are needed. The chip generates five identical phase-aligned output clock signals, as well as one 180° phase-aligned output clock, from a periodic reference clock (Fig. 1). Both the phase and frequency relationships of the output clocks to the input clock are controlled by the circuit through an on-chip phase-locked loop (PLL) that operates at about 500 MHz.

Proprietary PLL circuitry, similar to that employed in the company’s previously released Hot Rod serial communication circuits, eliminates the need for any external components to support internal phase locking at up to 500 MHz. That makes the GA1110 very simple to use. A sixth clock output serves as the feedback signal to the PLL and synchronizes the outputs to the input clock. Multichip clock chains and clock trees can now be easily configured thanks to the tight skew control.

There’s no requirement, however, that the external feedback connection be directly hardwired from an output pin to the feedback input (FBIN) pin. Additional logic can be inserted in the feedback path as long as the signal arriving at the FBIN pin is derived directly from one of the output pins, and it maintains the output pin’s frequency. The internal PLL will adjust the output clocks to ensure zero phase delay between the FBIN and CLKIN signals. This feature is very handy when custom chips must be synchronized to the system clock. There’s one caveat, though: The signal at the FBIN pin must stay continuous (it can’t be a gated or conditional signal) to ensure synchronization.

A pair of active-high control signals, S1 and S0, combined with the feedback of an output clock signal to the FBIN, enables users to select any of 14 timing relationships between the five output clocks (Table 1). Consequently, the clock edges can be placed in precise, digitally-controlled 2-ns increments (+ or −) relative to the input and feedback clock phase. In systems where clocks must be sequential, or where wiring-trace and loading mismatches develop, the chip can supply the early or late clocks. When the chip is powered up, or the system clock is reset, the PLL requires a short time period (\( T_{sync} \)) to lock onto the signal.

In a typical system, designers may require several low-skew outputs, one early clock, one late clock, and one inverted clock. Such a system can be satisfied by setting S1 low, S0 high, and connecting Q0, Q1, or Q4 to the FBIN input (row 3 of table 1). The result is that Q0, Q1, and Q4 will be phase-aligned to the input clock, Q3 provides the early clock (by one 2-ns increment), Q2 delivers the late clock (also by one 2-ns step), and Q5 supplies the inverted clock.

Output clock signals are generated with 50/50 duty cycles, even if the input clock isn’t completely symmetrical. Ratios of up to 75/25 for the input clock can be handled. Housed in a standard 16-pin DIP, the chip has three pins assigned for power and another three serve as ground lines. As a result, it permits more than adequate power-supply bypassing to eliminate noise. The chip operates from a 5-V supply and typically draws about 120 mA. Working either in conjunction with the GA1110 or as a standalone circuit, the GA1210 delivers multiple

**Table 1: Timing Options for the GA1110**

<table>
<thead>
<tr>
<th>Configuration number</th>
<th>Select pins</th>
<th>Outputs fed to feedback input pin</th>
<th>Output phase shift</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>S0</td>
<td>Q0, Q1, Q2, Q3, or Q4</td>
<td>Q0, Q1, Q2, Q3, Q4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0, 1</td>
<td>0, 0, 0, 0, 1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0, Q1, or Q4</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>Q2</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>Q3</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>Q4</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>Q5</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>Q0, Q2, or Q3</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>Q1</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>Q4</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>0</td>
<td>Q5</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
<td>0</td>
<td>Q0</td>
</tr>
<tr>
<td>12</td>
<td>0</td>
<td>0</td>
<td>Q1 or Q2</td>
</tr>
<tr>
<td>13</td>
<td>0</td>
<td>0</td>
<td>Q3 or Q4</td>
</tr>
<tr>
<td>14</td>
<td>0</td>
<td>0</td>
<td>Q5</td>
</tr>
</tbody>
</table>

Notes: 1. \( i \) represents the incremental phase-shift adjustment (2 ns) 2. A 0 phase shift indicates the output is aligned to the clock input 3. A negative phase indicates the output precedes the input clock 4. A positive phase indicates the output follows the input clock 5. I indicates an inverted version of the input clock
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CIRCLE 91

CLOCK GENERATOR CIRCUITS

TABLE 2: OUTPUT CHOICES FOR THE GA1210

<table>
<thead>
<tr>
<th>Control pins</th>
<th>Clock output lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable 2-phase clocking</td>
<td>Invert Q1 output</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Notes: 1. 1X is an output clock, a phase-aligned copy of the input clock signal.
2. (I) indicates inverted version of 1X clock (180° out of phase)
3. 2X is an output clock, a phase-aligned double-frequency copy of the input clock signal.
4. PH1 and PH2 are the first and second of two clock phases, synchronous to the input clock.

low-skew clock signals that are twice the frequency of the input clock, which can be as high as 50 MHz (Fig. 2). The chip also generates several 1X clocks, one of which is fed back to the FBIN input so that the PLL can maintain synchronization.

All of the generated clocks (up to 100 MHz) are phase-aligned to the periodic clock input. Such a circuit solves the problem of distributing high-frequency clock signals in large systems. A low-frequency clock of 50 MHz or less can be distributed to each board and then doubled on the board by a GA1210, so that 50-to-100-MHz clocks can time on that particular card.

Several different configurations can be set up on the chip to accommodate various system requirements through the Enable 2-phase Clocking (EN2) and Invert Q1 (INV1) control pins (Table 2). In addition to supplying the 2X clock, the chip can be configured to generate non-overlapping two-phase clocks.

As with the GA1110, the clock multiplier accepts a master-clock input frequency from 25 to 50 MHz, has a maximum skew of 500 ps between outputs, recreates a 50/50 duty cycle on each output, and can drive up to 24 mA on each output line. The GA1210 also comes in a 16-pin DIP, and includes triple power and ground lines to minimize noise.

PRICE AND AVAILABILITY
The GA1110 and 1210, which come in 16-pin DIPs, are immediately available. The commercial-temperature-range versions of the 25- and 33-MHz speed grades sell for $28.50 in 1000-unit quantities. The higher-speed grades will be sampled next quarter.

Gazelle Microcircuits Inc., 2300 Owen St., Santa Clara, CA 95054; Bob Gunn, (408) 982-0900.

CIRCLE 511

HOW VALUABLE?
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HIGHLY 547
MODERATELY 548
SLIGHTLY 549

2. GENERATING CLOCK INPUTS that are 2X or 1X multiples of the input clock, the GA1210 clock circuit can use its high-frequency PLL to synchronize the output clock signals to the input clock.
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functions include timers, counters, serial ports, and parallel I/O ports.

Additional support functions becoming popular include interrupt controllers, large register files, and DMA controllers. Furthermore, manufacturers have created specialized I/O functions that include complex timer modules, pulse-width modulators, analog-to-digital and digital-to-analog converters (ADCs and DACs), and others for automotive system, telecommunication, consumer-equipment, and computer-peripheral applications.

On the whole, the older NMOS controllers have given way to CMOS. However, for applications that aren't power-critical, NMOS 8-bit controllers are still viable and cost slightly less than the newer CMOS chips. NMOS-device choices are somewhat limited to older- or first-generation architectures—the MCS-48 and 51 families originated by Intel Corp., Chandler, Ariz.; the 6805 series from Motorola Inc., Austin, Texas; and the Z8 from Zilog Inc., Campbell, Calif.; among others.

One way manufacturers can cut chip cost is to design a simple processor that performs its operations with minimum hardware by time-sharing the silicon resources. In previous designs, that approach worked because processor throughputs could handle the expected applications.

Today's demanding applications, however, require much higher performance. As a result, controller makers are taking two approaches to meet the customer's needs. The simplest approach is to up the clock fre-
frequency that the controller runs at. Over the past few years, clock frequencies have crept from 8 MHz up to 16 MHz, and later this year some suppliers expect to ship controllers that run at 20 MHz and beyond. Unfortunately, elevated clock frequency creates several problems—testing the chips at the higher speeds, potentially reduced yields of higher-speed devices (and thus a higher device price), and more generated radio-frequency interference caused by higher clock frequencies.

Alternatively, more silicon can be used to address the throughput issue. The processor’s time-shared internal architecture can be restructured to a more parallel structure that enables multiple operations to be done in one clock cycle.

Many original low-cost 8-bit processors, such as the 80C51 family from Intel Corp.; the 68HC05 series from Motorola Inc.; the TMS7000 series from Texas Instruments Inc., Dallas; and the Z8 family from Zilog Inc.; require 8 to 12 clock cycles (1 to 2 µs) for one instruction to execute. In contrast, some of the latest 8-bit controllers—such as the H8 processors from Hitachi Semiconductor Inc., Brisbane, Calif.; and the K series chips from NEC Electronics Inc., Mountain View, Calif.; and the TMS370 family from TI—require just a few cycles (less than 500 ns) to complete an instruction. Consequently, for a much lower clock rate, the processor can perform the same work. The drawback is that more silicon area is needed for the more efficient processor core, increasing chip cost.

Today’s workhorse processors, the 8-bit microcontrollers, come in a dazzling array of configurations. A well-established family, such as Intel’s 80C51, which has several licensed alternate sources, contains more than two dozen commercial versions from Intel; Advanced Micro Devices Inc., Austin, Texas; Oki Semiconductor Inc., Sunnyvale, Calif.; Philips-Signetics Corp., Sunnyvale; Siemens Corp., Santa Clara, Calif.; and others.

The original CMOS versions in the MCS-51 family include the 80C51 with 4 kbytes of ROM and 128 bytes of RAM, and the 80C52, which includes 8 kbytes of ROM and 256 bytes of RAM. UV EPROM and ROM-less versions of both chips are also available. Other 80C51 resources include a pair of 16-bit timer-counters, a full-duplex serial port, 32 bidirectional I/O lines (four 8-bit ports), and a five-source interrupt structure with two priority levels. The C52 adds one more timer-counter and its interrupt source.

Intel’s latest offering is the 87C51FC, which offers the largest on-chip program storage in the MCS-51 family: 32 kbytes of EPROM, doubling the memory of the company’s previous version—the 87C51FB. Along with the expanded program memory, the chip packs an array of programmable counters with five I/O channels to handle complex timing applications with minimum CPU overhead. Either a windowed ceramic package or a one-time-programmable (OTP) plastic package can house the chip.

Additional 87C51FC resources include 256 bytes of RAM, a serial I/O port, three 16-bit timer-counters, and a two-level program lock to guard against software piracy. A simpler version of the chip, the 87C54, eliminates the complex counter array to trim the price. The chips are designed to handle some of the complex operations in automotive control systems, and can operate over a −40 to +125°C temperature range at either 12 or 16 MHz.

The 80C515, packing 48 I/O lines, a 16-bit watchdog timer, three additional 16-bit counter-timers, a full-duplex serial port, an 8-bit ADC, as well as 8 kbytes of ROM and 256 bytes of RAM, is an extended-I/O version of the 80C51 offered by AMD and Siemens. Housed in a 68-lead PLCC, the controller’s ADC has eight multiplexed inputs and performs a conversion in 13 µs. When operating at 12 MHz, the controller executes most commands in about 1 µs. Higher-speed 16-MHz units are also available.

AMD and Siemens went in different directions for additional control-
timer-counter, one 16-bit compare timer, one 16-bit reload-capture-compare register, four 16-bit capture-compare registers, eight 16-bit compare registers, the ability to perform concurrent compare operations, and up to 21 channels of compare outputs. The multiplication-division block tackles the math-intensive applications and delivers results on 32-bit numbers in just 4 to 6 µs.

In addition to the MCS-51-compatible chips, Siemens just signed a deal with SGS-Thomson Inc., Phoenix, Ariz., to alternate source and jointly develop future versions of SGS's S-series microcontrollers. The ST8 series from SGS is based on a core CPU that can address up to 32 kbytes of program memory and a 6-bit stack pointer (future versions will increase the pointer to 8 bits to address up to 256 kbytes). The first two processors in the family, the ST8108 and 81E08, pack 8 kbytes of ROM and EPROM, respectively, 176 bytes of RAM, timers and serial I/O ports, as well as bidirectional I/O ports. Future members will include EEPROMS, ADCs, DACs, and other functions. SGS also has two other families, the ST6 to tackle the low-end applications, and the ST9 to handle the most complex 8-bit applications.

Tackling I/O-intensive applications, Philips-Signetics created an extended I/O processor—the 83C51—which offers seven 8-bit I/O ports in a 68-lead PLCC version. One unique port includes a "mailbox" feature that makes it possible for the port to serve as an I/O port or as a control and status register. The chip packs the same amount of RAM and ROM as the original 80C51.

A more complex version of the same chip—the 83C552—starts with the 80C52 memory and adds six byte-wide parallel ports, a 10-bit 8-channel ADC, two pulse-width-modulated (PWM) outputs, and an inter-IC bus serial port for chip-to-chip communications (see the figure). Also available are an EPROM version, and a version without the ADC and PWM outputs and with only four ports.

Very large memories on a version similar to what Intel included on the 877C51FC are also on the horizon. Philips-Signetics plans to offer the 83C528 with 32 kbytes of EPROM and 512 bytes of RAM. In addition, the company will have two versions—the 83C053 and 054—both of which pack 192 bytes of RAM, and 8 or 16 kbytes of EPROM, respectively. These two chips are aimed at TV remote-control subsystems and pack a separate 128-byte display RAM and three digital video outputs.

Going in the low-cost and minimal-I/O direction, Philips-Signetics slimmed down the 80C51, creating the 83C751. It comes in a 24-pin skinny DIP (300-mils wide) and packs 19 I/O lines, one counter-timer, a single-level interrupt structure, 2 kbytes of ROM, and 64 bytes of RAM. A slightly larger version—the 83C752—comes in a 28-lead DIP or PLCC, and packs the same memory and counter-timer, but has three parallel ports (two 8-bit and one 5-bit parallel ports), an inter-IC serial interface, one PWM output with timer, and a five-channel 8-bit ADC. Both chips can't use off-chip memory.

Philips-Signetics is also upgrading its 80C51 direct-equivalent controllers so that they can operate at 20

- **VDD**
- **VSS**
- Pulse-width-modulated output 0
- Pulse-width-modulated output 1
- Analog VSS
- Analog VDD
- Strobe ADC
- ADC inputs 0-7
- Serial data A
- Serial data L
- Program memory (8 kbytes of ROM)
- Data memory (256 bytes of RAM)
- Dual pulse-width modulator
- ADC
- Serial inter-IC port
- 8-bit internal bus
- Four 16-bit capture latches
- Timer 2 16-bit timer-event counter
- Three 16-bit comparators with registers
- Comparator output selection
- Watchdog timer 3
- Port 5
- Port 4
- Capture inputs 0-31
- Timer 2
- Reset timer 2
- Comparator outputs
- Reset
- Enable watchdog

**ONE OF** the most complex microcontrollers based on the 80C51 processor core is the PCB80C552 from Philips-Signetics. It packs an eight-channel ADC, a pair of PWM outputs, a pair of serial ports, multiple timer-counters, and a large number of I/O lines.

---

**E L E C T R O N I C  D E S I G N**

**A U G U S T 9 , 1 9 9 0**
and 24 MHz. The 24-MHz unit becomes the fastest C51 controller available from any source and can execute typical commands in just 500 ns. The company hopes to be the first supplier to include EEPROM on an 80C51-based controller. Plans are underway to create the 83C851, an 80C51 with 256 bytes of EEPROM. One alternative to EEPROM for the 80C51 is a battery-backed version offered by Dallas Semiconductor Corp., Dallas, Texas. By embedding a long-lifetime battery-backed RAM in the same package as an 80C51-equivalent controller, Dallas devised a controller that can retain data for about 10 years, if used in accordance with its data sheet.

Although many C51-based CMOS controllers can operate at voltages down to about 2.5 V, even lower operating-voltage requirements led designers at Philips-Signetics to create another version of the C51—the 83C5410. The CL410 was designed with static CMOS logic and can operate with supply levels of just 1.5 V, or draw less than 1 mA when operated at 3 V and 3 MHz.

As prolific as the MCS-51 family is thanks to its multiple suppliers, Motorola has limited alternate sources to its low-to-mid-range 68HC05 architecture microcontrollers, establishing itself as a sole-source for its mid-to-high-end 8-bit family—the 68HC11 series. However, that hasn’t limited the proliferation of the 68HC05 controllers. Nearly two dozen versions of the 68HC05 already exist, with a few of these alternate-sourced by Harris Semiconductor Corp., Melbourne, Fla. (an outgrowth of Harris’s acquisition of RCA Corp., the original licensee of the Motorola processors). The chips’ typical instruction execution time is about 1 µs and contain a similar software structure to the original 6800 microprocessor.

Needless to say, a wide variety of memory, I/O, and control functions are available in the processor family, and more “standard” versions are planned by both Harris and Motorola. To create so many versions, Motorola implemented a customer-specific adaption program that tries to match similar customer requests with similar features and then to turn all of the requests into a common piece of silicon that can be offered commercially. The company also expects to add such capabilities as handling high voltages for display driving or high-current outputs to directly drive small motors.

For more demanding applications, Motorola offers the 68HC11 family, the first microcontrollers to offer RAM, ROM, and EEPROM on one chip. The original HC11 processor packed 256 bytes of RAM, 512 bytes of EEPROM, and 8 kbytes of ROM, as well as a timer, both simple and complex serial ports, multiple parallel I/O ports, an 8-channel ADC, and a watchdog timer. One forthcoming HC11 processor will include no ROM, but will offer demultiplexed address and data lines, 1 kbyte of RAM, and 512 bytes of EEPROM—the 68HC11F1. Additional processors with larger on-chip memories are also in development.

The HC11 processors execute a superset of the original 6800 and 6801 instruction sets and include the ability to tie the dual 8-bit accumulators together and perform 16-bit arithmetic operations without looping. The simplest version in the family is the 68HC11D3, which contains just a 4-kbyte ROM, 192 bytes of RAM, and comes in a 40-pin DIP. Memory capacities for large programs are also available—the HC11E9 packs 12 kbytes of ROM, 512 bytes of EEPROM, and 512 bytes of RAM.

Also offering two families of 8-bit microcontrollers, TI developed the TMS7000 series to tackle what it considers low-to-mid-range applications, and the TMS370 series to handle the mid-range to high-end applications. About a dozen versions of the TMS7000 processor exist, all offering performance levels competitive with the MCS-51 and 68HC05 families. The TMS7000 chips pack up to 4 kbytes of ROM or EPROM, 128 or 256 bytes of RAM, timers, serial ports, and up to 32 I/O lines. One CMOS processor, the 70C42, operates from as low as 2.5 V and as high as 6 V. At the low value, the chip must run at a much-reduced clock frequency—800 kHz, maximum—rather than the 5 to 6 MHz when powered by a 5- or 6-V supply.

Employing a more complex CPU core, the TMS370 series chips compete more with the 68HC11 and the K-series from NEC Electronics. TI actually divided its 370 family into several sub-families, which total close to two dozen choices. The sub-families consist of the 370Cx10, Cx3x, and Cx5x series. The Cx10 aims at the lower end of the higher-performance range, the Cx3x for slightly more complex applications, and the Cx5x solves the high-I/O and large memory needs of the most challenging applications.

Various members of the Cx10 series offer up to 4 kbytes of program ROM or EEPROM, 128 bytes of RAM, another 256 bytes of data EEPROM, a counter-timer and a watchdog timer, a serial port, and up to 22 I/O lines. More formidable applications might use the Cx5x processors, which pack up to 16 kbytes of ROM or EPROM, or 4 kbytes of EEPROM, as well as 256 or 512 bytes of RAM, 256 or 512 bytes of data EEPROM, an 8-channel ADC, two counter-timers plus a watchdog timer, two serial ports, and up to 55 I/O lines.

Some of the most recent family members include versions that operate at clock frequencies as high as 20 MHz. They add on-chip functions such as a multichannel ADC, or a multi-output complex timer array that can offload the Cx32 core processor, much like the timing array Intel and Siemens included in their 80C51-based controllers. The programmable acquisition and control timer module provides six capture inputs, eight timer-controlled outputs with PWM capability, up to 20 configurable comparison lines, a watchdog timer, and a full serial port.

With ROM capacities of 2 or 4 kbytes, Zilog’s NMOS Z8 family gives customers about a dozen variations with pin counts ranging from 28 to 64 leads. All of the chips in the Z8600 family pack 124 bytes of RAM, either 1 or 4 external interrupt inputs, two timers, and in most versions, both an asynchronous serial port and another simpler, synchro-
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ELECTRONIC DESIGN REPORT
EMBEDDED CONTROLLERS

ous serial port. The CMOS Z8 family includes over 15 processors that have as few as 18 and as many as 40 pins. On-chip memory ranges from 2 to 8 kbytes of ROM or EPROM, while RAM is either 124 or 236 bytes.

Several Z8 versions are designed to retain data when the power supply dips as low as 2 V, and they can operate from 3 to 5.5 V with clock speeds of 2, 8, or 12 MHz. When running at 12 MHz, the average instruction executes in about 1 µs. Some also include analog comparators to perform level-sensing operations and programmable timers with programmable prescalers (the Z86C08, 09, 30, and the ROM-less C90).

The company's older NMOS Super 8 processor will soon be converted to CMOS, thus reducing power, possibly increasing the on-chip ROM to 16 kbytes, the RAM to 512 bytes, and improving performance. The NMOS version packs many resources—a DMA controller, high-performance math instructions and commands to support threaded-code languages such as Forth, a large 128-kbyte address space, a complex interrupt-service unit that responds to an interrupt in just 600 ns, a pair of counter-timers, a full-duplex serial port, and 40 parallel I/O lines.

One version of the Z8, the Z86C27, is optimized for television control, and contains an 8-kbyte RAM, 256 bytes of ROM, a separate 180-byte character RAM, 4-kbyte character ROM, and 13 PWM outputs with 6 or 8-bit resolution (except for one that offers 14-bit resolution). The chip also includes some analog comparators, a pair of counter-timers, 36 parallel I/O lines, and fast-responding interrupt control logic.

Future members of the Z8 family will tackle such applications as hard-disk control, thanks to a separate ALU that accelerates multiplication and division operations, thus improving response times in servo control loops.

In addition to offering an alternate source to the old Intel MSC-48 family, Mitsubishi America Inc., Sunnyvale, has a family of over thirty 8-bit controllers in its proprietary M50XXX and M37XXX families that are software-compatible with the 6500 family instruction-set processors. On-chip ROM ranges from 3 to 16 kbytes on the smallest to largest units, with RAM growing from a minimum of 96 bytes to 512 bytes at its maximum.

Minimum instruction execution times range from about 2.5 µs when a 3.2 MHz clock is employed, to just 670 ns when the chips run from a 12-MHz clock. The 6502 processor core is also used by NCR Corp., Colorado Springs, Colo., to create custom custom microcontrollers, while Rockwell International, Newport Beach, Calif. has developed a single-chip controller with 2 kbytes of RAM and 64 bytes of RAM.

Depending on the chip in Mitsubishi's family, there can be from 14 to 48 I/O lines, asynchronous or synchronous serial ports, ADCs, DACs, PWM outputs, counter-timers, and special features including vacuum-fluorescent or liquid-crystal display drivers, telephone-tone generators, or variable-threshold comparators. A complex chip, the M37499M2, combines the controller, 192 bytes of dual-ported RAM, 320 bytes of normal RAM, 4 kbytes of ROM, three full-duplex serial ports, an 8-bit timer, and two byte-wide I/O ports.

Targeting the high-throughput applications, the K-series processors from NEC offer designers highly efficient CPUs. The company currently has close to 20 devices defined and in production, with more to be released before year's end. In the K2 family, versions are available with ROMs as large as 1 kbyte and ROMs or EPROMs of up to 32 kbytes. As with the Motorola 68HC11, NEC offers one type that packs 16 kbytes of ROM, 512 bytes of RAM and 512 bytes of EEPROM—the uPD78244.

The K-series is crafted for speed—at 12 MHz the K2 chips execute instructions in 333 ns—about half the time required by the 68HC11 or TMS370 controllers. Due later this year are 16-MHz versions that cut the instruction cycle time to 250 ns. Serial I/O ports, counter timers, and multichannel ADCs and DACs are common on most devices in the K series. One carryover from the previous uPD7800 family of 8-bit control}-
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Transportation emerges as the next catalyst for electronic component technology.

JOHN GYORKI AND MILT LEONARD

THE ELECTRONICS industry is undergoing a fundamental change, spurred on by new applications in vehicles. Automakers in the 1990s will increasingly depend on electronics to meet ever more strict safety and emissions standards. Moreover, manufacturers now see auto electronics technology as a means of getting a competitive edge. The result: Innovative applications in ride control, entertainment, and driving aids have already been developed, and indications are that the best is yet to come. The next phase of automobile development will treat the auto as a total integrated system which will rely on substantially higher levels of computer speed and memory.

Experts feel that automotive applications may stimulate the demand for electronics in the 1990s as the PC did in the early 1980s. Electronics companies that supply European and Japanese automakers may benefit in particular. The reason is that these car builders tend to buy electronic components from outside suppliers. The Big Three automakers in Detroit, on the other hand, tend to obtain most of their electronics from internal divisions.

TRENDS AND PROJECTIONS

According to Roger Grace Associates, a San Francisco-based consulting firm, automakers’ increasing dependence on electronic solutions (along with a growing automotive market) will boost the worldwide automotive electronics market from an estimated $12.5 billion in 1987 to $35 billion by 1995. Growth for North American auto electronics is equally dramatic. Where a 1970 model car from Ford Motor Co. contained about $25 worth of electronics, the electronic content per vehicle of 1984 models averaged $585. Projections for 1995 indicate a jump to $1,500 per vehicle, and to $2,000 by the end of the decade. Similarly, Chrysler Corp. estimates a jump from an average $350 for a 1988 model to about $1,400 for a 1992 model. The increased emphasis on automotive electronics is also reflected in a study conducted by The University of Michigan at Ann Arbor. The Delphi V study reports that electronics will represent 20% of a car’s total value by the year 2000.

Another study by Dataquest Inc., a San Jose-based market research and consulting firm, divides an estimated $2.6 billion electronics market for the North American passenger-car industry into application areas. Most expenditures (40%) will go toward power-train controls such as ignition systems, emission control, and engine and transmission control. Vehicle controls will comprise another 19%, followed closely by the safety, comfort, and convenience (SCC) aspects of automotive design, which will consume 17% of the market. Currently the fastest growing segment of the automotive market, SCC includes keyless entry, automatic climate control, memory seats, and antiskid...
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ELECTRONIC FUEL INJECTION

Electronic fuel injection (EFI) computers basically control engine air-fuel (A/F) ratios to handle changing conditions. For example, a ratio of 14.7/1 is optimal for cruise conditions, but a richer mixture is needed for cold start and wide open throttle (WOT). Similarly, a leaner mixture is required for decelerations; sometimes the fuel is totally cut-off on deceleration.

Sensors give the EFI controller information about the volume of air inducted so it can calculate the precise amount of fuel to be injected. Direct-measuring mass air-flow sensors were not readily available for use in early EFI systems. Rather, a so-called speed density system was employed that measured engine speed, manifold vacuum, and inducted air temperature. Mass air intake could only be interpolated from these secondary measurements. Inaccuracies resulted and had to be corrected.

However, Bosch of Germany recently developed an advanced mass airflow sensor that overcomes such drawbacks. The air meters use either a hot wire or hot film as the sensing element. Inducted air tends to cool the heated resistance element as it passes. The idea is to adjust current through the element to keep it at a constant temperature. The amount of current flow is proportional to airflow and, thus, serves as a measure of inducted air mass.

Exhaust emission and fuel economy requirements have forced engine designers to constantly improve fuel-management techniques. For example, systems are being designed to learn and adapt to changing driving conditions and engine parameters. New solutions to internal-combustion engine-management problems include injection valves with split spray jets for engines containing four valves per cylinder, hot wire mass airflow meters, and highly integrated electronic ignition systems.

Two basic types of EFI systems are widely used. The first is called multiport injection where each cylinder has a separate fuel injector. The other is single-point injection where one main injector sits in the throttle body.

The Mono-Jetronic system by Bosch uses a simple single-point, throttlebody injection system (TBI). Gasoline is injected through a single solenoid-operated valve located above the throttle valve. This thoroughly atomizes fuel at the point of maximum air velocity.

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**EFI System functional diagram**

THE LH-JETRONICS system with hot-wire airflow sensor is one of the most advanced EFI systems available for passenger cars. Earlier systems, such as the L-Jetronic, contained a moving vane (pushed by the airflow) connected to a position-sensing potentiometer.

Like most other EFI systems, the LH-Jetronic fuel system is controlled by solenoid-operated injector valves. The pressure drop at the injector nozzle (metering point) is held constant with a pressure regulator. Thus, the injected volume of fuel depends solely on the opening period of the injector valves as calculated by the electronic control unit.
The TBI system consists of a throttle valve, injection valve, pressure regulator, throttle valve potentiometer, temperature sensor, and throttle valve servomotor. Because of the compact and low-profile design, the throttle body can mount directly on the intake manifold.

Fuel-injection control and exhaust gas optimization is handled by an intelligent system, called Alpha-n control. This is a self-adaptive controller that monitors the exhaust gas (Lambda) sensor, throttle valve angle, and engine speed. These inputs determine the fuel-control schedule, also known as the engine map.

The computer monitors exhaust gas composition and stores the data in memory. Next, it calculates an optimum operating point, outputs a new fuel-injection signal, then rechecks the exhaust ahead of the catalytic converter. The external surface of a ZrO₂ ceramic sensing element protrudes into the exhaust gas flow and the inner surface is exposed to outside air. The ZrO₂ electrodes generate a small voltage that is proportional to the ratio of residual oxygen in the exhaust gas to oxygen in ambient air. When the ratio changes, the output voltage also changes.

The electronic control unit uses the Lambda output voltage as a factor in adjusting the air-fuel ratio. The exhaust gas composition is kept at a level that is optimum for treatment by the catalyst.

The Lambda sensor can only operate when the exhaust gas and manifold exceed 900°C. On some engines, the time for Lambda sensor warm-up is prohibitive so a self-heating sensor was developed. This permits closed-loop control within 30 s of starting and during idle.

braking. Driver information systems, such as digital gages, service reminders, trip and navigation computers, and CRT and head-up displays, will account for another 14%, and entertainment and body systems, such as multiplexing and lighting will comprise the rest.

**NEAR-TERM BENEFITS**

New car models showcase advanced electronic control systems from the power train throughout the chassis. For example, General Motors Corp. plans to equip all luxury and full-size 1991 cars with ABS (antilock braking systems), which will become standard on all models by 1994. A typical ABS combines wheel-speed sensors, microcontrollers, and brake-pressure modulators to apply pulsed brake pressure at each wheel without brake lockup.

Using many of the same components as ABS, traction control minimizes wheel slippage during vehicle acceleration. The front-wheel drive of the 1990 Cadillac Allante has a 2-stage antislip system made by Robert Bosch GmbH of Stuttgart, West Germany. The system combines front-axle traction control with Bosch's four-wheel ABS. Cadillac's 1992 Eldorado and Seville are expected to be similarly equipped. Other U.S. cars expected to have traction control next year are the Lincoln Town Car from Ford Motor Co. and the New Yorker Fifth Avenue and Imperial from Chrysler Corp.

Active suspension improves vehicular handling and safety by changing the damping force of shock absorbers according to driving conditions. European and Japanese auto suppliers are leading the technology with systems that respond to such variables as road surface, axle load, wheel turning angle, and even side loads caused by wind.

The list goes on with antitheft and security systems. GM's PASS-Key (personalized automotive security system) has an ignition key with an embedded resistor code which is read by electronic sensors in the ignition lock cylinder. If an
improper key is inserted, the system disables the starting and fuel systems. In a more aggressive system by Ford, opening the door turns on the horn, blinks the lights, and disables the starter coil when the dome light is lit by opening the door.

With the number of in-vehicle control modules doubling to over 60 during the past ten years, the size and weight of wire harnesses that interconnect these functions has increased dramatically. To reduce the complexity of such links, U.S. carmakers are turning to multiplexed designs. These use a microprocessor to send pulse-width-modulated commands over a single wire to distributed output devices.

For example, an integrated system on the Buick Electra controls exterior mirrors, window motors, and door locks, and provides keyless entry, antitheft, and illuminated entry functions. Multiplexing reduced the number of wires passing through the door on the driver's side from 56 to 20. Multiplexing is also being used in the Cadillac Allante to power interior lighting modules and in Chrysler's collision-detection system to allow an engine-control module, body computer, and trip-fuel consumption computer to share data from various sensors.

The deployment of multiplexing technology in automotive applications has been delayed by a lack of international standards. In pursuit of a common approach to system protocol, standards committees in the U.S., Japan, and Europe have devised three classes of multiplexed systems as a starting point: Class A for low-speed body wiring and control functions, Class B for medium-speed data communications, and Class C for high-speed, real-time control. Furthermore, the Society of Automotive Engineering (SAE) is expected to complete its recommended practice (J1850) for Class B applications late this year.

Networked schemes will also show up in automotive applications. Bosch has developed a technique called the automotive serial controller area network (CAN). Its protocol is supported in silicon from both Microcontroller Div. of Motorola Inc. (Austin, TX) and Intel Corp. (Santa Clara, CA). The network topology is a multimaster bus configuration that operates over either two shielded copper wires or fiber cable with a maximum bus length of 40 m and a data rate of 1 Mbit/s. Other standards vying for universal acceptance are the CarLink protocol from Detroit's Big Three, and Automobile Bus and VAN (vehicle area network) in Europe.

ON THE HORIZON

Even more intriguing features are in the planning stage. Digital signal-processing (DSP) techniques for speech synthesis and speech recognition will enable cellular telephones to be controlled by voice and talk to the driver. Cellular users can already use a system from L.A. Cellular in Los Angeles to receive traffic updates, vehicle location, and recommendations for hotels, restaurants, and trip designations.

For truck drivers, an emerging satellite technology called radio determination satellite service (RDSS) beams messages to areas not serviced by traditional communications systems. A terminal mounted in the cab displays the message on a screen, prints out a hardcopy, or delivers the message with a speech-synthesis system developed by Berkeley Speech Technologies of Berkeley, CA.

DSP technology is also behind an active noise-cancellation system being developed by Lotus Engineering in the United Kingdom. Aimed at reducing interior car noise, the system effectively "fingerprint" the sound picked up by several microphones distributed throughout the car, generates out-of-phase noise signals, and broadcasts this sound through the car's stereo speakers to cancel the noise. The system is expected to be offered to auto manufacturers within two years.

Although market growth beyond the mid-1990s is difficult to predict, driver information systems that work with "smart highway" equipment are expected to help fuel continued growth. Japan and Europe are far and away the leaders in this and related technologies such as sophisticated vehicular navigation systems. However, an experimental program in the U.S. may spur interest among domestic carmakers.

In part because of its legendary traffic jams, California is experimenting with a smart highway program which could lead to a commercial system by the mid-nineties. Jointly conducted by the California Department of Transportation (Caltrans), the Federal Highway Administration, and General Motors Corp., the Pathfinder program was initiated in 1988 to relieve traffic tie-ups by integrating traffic information with a vehicle navigation system.

The $1.6 million experiment uses 25 Oldsmobile Delta 88 sedans equipped with electronic navigation systems from Etak of Menlo Park, CA. The navigation system consists of a trunk-mounted communications console and a display screen fitted on the dashboard. The two-way communications system is linked to other test vehicles and to the Caltrans traffic operations Center in Los Angeles. Drivers receive traffic information visually on the display screen or by computer-synthesized voice. The screen shows area street maps, tracks the vehicle's position, and gives alternate routes for avoiding traffic.

The ultimate solution for smart highways will need to include sensors along the highway for gaging traffic density and speed. A traffic control center will retransmit this information to properly equipped vehicles. The scheme might even be used to regulate vehicle speed automatically. Though the prospects for smart highway technology are dramatic, several major hurdles remain, such as high installation cost, software development, and the need for communications protocols.
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Call the technical information hotline 1-800-5-LECROY for product information including the tutorial, "The Hows and Whys of AFG's", a demonstration version of EASYWAVE, or for application assistance.

CIRCLE 133 FOR INFORMATION
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CIRCLE 144
Seat belts have been widely used on American vehicles since the early 1960s. But recently, lawmakers have dictated that cars be equipped with passive restraints.

Beginning with model year 1990, all U.S. cars must provide a passive-restraint system for the driver, and in 1994 it must be available for the front seat passenger as well. Safety legislation places unusual demands on designers to provide airbag systems that are reliable, do not deploy during minor fender-benders, can remain unused without degradation for long periods, and can survive a crash but still deploy. Key to such a system is a trigger unit that senses the magnitude of the crash.

The trigger unit must contain an acceleration sensor that accurately determines when to blow the air bag or tighten a seat belt. When an evaluation circuit detects deceleration indicative of serious accidents, a firing cartridge triggers an air bag and activates the seatbelt tensioner. In a frontal collision at 30 mph (18 km/h) — the velocity needed to trigger the air bag — the calculation is so fast that the cartridge fires within only 10 ms.

At the same time, the system must be sensitive enough to discern minor bumps that must not deploy the air bag. To prevent such problems, the device checks itself against data from test crashes to implement filtering action. For further reliability, a diagnostic program continuously checks the integrity of the entire electrical system, including the controller, cable and plug, and trigger unit.

At specified deceleration, the trigger sends an electrical pulse to a detonator located in a gas generator. The propellant detonates and fills the air bag. After 100 ms, the gas escapes through slots around the edge of the bag and collapses to absorb the kinetic energy of the driver’s body.

Drivers are protected by an airbag in the steering wheel. Passengers are restrained by a special belt tensioner. Upon impact, a capsule is detonated by an electrical signal, and the resulting high pressure expels a fluid against turbine blades. The turbine turns the shaft, reverses the roll-up mechanism, and tightens the seat belt.

The seat-belt tensioner for the front seat passenger operates from the same trigger unit as the air bag. Propellent forces fluid against impeller blades of a turbine. Turbine wheel rotation forces a roll-up shaft to tighten the belt.

If the vehicle battery is disabled during an accident, a large capacitor gives enough backup power to operate the restraint system. A voltage converter assures that the full operating voltage is available for the trigger unit even if the battery drops as low as 4 Vdc.

A check lamp monitors the electrical system. The lamp illuminates when the ignition switch is on and remains lighted for about 10 s during a test cycle. If the system is operable, the lamp goes out. The lamp stays lighted if system service is needed.

Older restraint systems were primarily mechanical, employing several sensors that can monitor only two or three parameters. Acceleration in these devices contained mechanical switches that tended to cause inadvertent bag deployment. In contrast, newer electronic units contain more sophisticated acceleration sensors, with microprocessor and digital signal-processing ICs for control and monitoring functions.

The accelerometer in a Bosch AB6 system, for example, uses a spring-weight system and electronic circuitry. The dual element sensor detects vehicle deceleration during frontal collision. The movable weight bends a spring that is bonded to four sensing resistors in a bridge circuit. The device generates a voltage that is proportional to the deceleration. The voltage is fed to an amplifier through a highpass filter.

A limiter stage follows that filters out high-frequency vibrations and subtracts signals less than 4 g — accelerations encountered during normal driving conditions. The threshold deceleration value for the seat belt is relatively low. Belts tighten at a frontal collision speed of only 25 mph (15 km/h). But the threshold level for the air bag is approximately 42 mph (25 km/h).
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CIRCLE 97
Newly Developed ICs Driving Auto Electronics

Early automotive electronics had to make do with older semiconductors, but specially designed ICs are opening up a wide range of new applications.

RANDY FRANK AUTOMOTIVE SEGMENT, MOTOROLA DISCRETE AND SPECIAL TECHNOLOGIES GROUP, PHOENIX, ARIZONA

Carburetors and points have gone the way of horseshoes and saddles in the area of personal transportation. Just as the automobile replaced the horse, increasingly sophisticated electronic control systems have made formerly essential components of the auto obsolete. The new systems improve performance, safety, convenience, communications, and manufacturability, and reduce emissions. In addition, they offer superior system diagnostics for improved serviceability, and system integration for increased reliability.

Although the microcontroller unit (MCU) is the critical control element in many current systems (12 applications depend on MCU technology), other semiconductor technologies will also play a key role in achieving high-volume production. Applications will include transient suppression, load controls that need more rugged and smarter power devices, and sensing of numerous vehicle inputs. In addition to supplying more precise control, the automotive semiconductors used in these applications must cope with one of the harsher environments for electronic components.

A good example of an automotive electronic control system is an antilock braking system (ABS). Virtually every auto manufacturer offers some sort of ABS on selected models. The typical ABS uses an MCU, several sensors, semiconductor power devices, and hydraulic components to automatically pump the brakes rapidly and repeatedly. As a result, the driver can maintain steering ability and vehicle stability under difficult road surfaces, such as ice or wet asphalt and under hard braking conditions.

Functions performed by a typical ABS controller include actuation of solenoids, motors, and indicator lamps. A simplified model of a generic ABS system starts with inputs from either vehicle sensors (or switches) or driver-actuated switches (Fig. 1). These inputs are converted to a form that can be employed by the MCU. For simple switched inputs, the interface requirements are minimal or nonexistent, but many sensing inputs require amplification, buffering, temperature compensation, or analog-to-digital conversion.

If designers develop custom ICs...
to link the sensors to the MCU, the ABS controller's complexity and component count can be considerably reduced. For instance, combining signal conditioning with the sensing elements to allow bidirectional communication with the MCU creates a "smart sensor." Smart sensors are typically monolithic semiconductor devices that offer fewer components, improved reliability, and reduced system cost.

The MCU's low-current, digital output must be amplified before it can control the power semiconductor or relay that will ultimately actuate the desired solenoid, motor, lamp, or display. As in the smart sensor, output signal conditioning and power semiconductor devices can be combined into smart-power ICs.

Besides easing the interface task, smart I/O devices also protect the system and supply fault-detection or diagnostic capabilities. With increased vehicle-system complexity, circuit protection and diagnostics are viewed as mandatory for improving manufacturability, safety, and first-time success for repairs.

The sensors measure the speed of the wheels and send the MCU an ac signal whose frequency is proportional to the wheel's speed. When the MCU detects a wheel lock-up, the controller drives relays that activate solenoid valves. The valves control the hydraulic pressure applied to each wheel to keep it in an optimum slip range. Present systems use electromechanical relays and bipolar power transistors or power FETs to activate the solenoids.

One of the many problems that confronts automotive-electronics designers is that the nominal 12-V system in passenger cars is just about anything but 12 V. In typical operations, charging systems regulate the alternator's output to supply sufficient voltage to keep the battery charged under various temperature and load conditions. This voltage can range from over 15 V at 0 °F to about 12 V at maximum underhood temperatures.

Moreover, electronic assemblies on cars must withstand reverse battery conditions to −13 V, jump starts from tow trucks (24 V), short-duration voltage transients that can easily exceed ±100 V, and long-duration (400 ms) "load dump" transients that can exceed +80 V. To prevent damage due to excessive voltage, the systems must either use electronic components with a breakdown voltage that can withstand the various automotive voltages, or they must include protective circuits.

The load-dump effect is a good example of the varying-voltage problem and how it can be remedied. To the voltage-regulated alternator, a properly connected battery appears as a large capacitor, maintaining a low and constant bus voltage. However, when it's disconnected, the alternator suddenly generates a high (by automotive standards) voltage transient lasting several hundred milliseconds (Fig. 2). This transient can cause catastrophic damage to voltage-sensitive electronics.

A common and relatively inexpensive way to suppress these transients is to place a short voltage clipper—such as a Zener diode or surge suppressor—across the input of the electronics. The suppressors, which for automotive applications are in the 24-V to 32-V range, must withstand the energy of the transient. This energy level is defined by many automotive specifications, the most common being 60-V or 100-V peak transients decaying exponentially to a 14-V battery level in a time constant of 0.115 seconds.
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Therefore, for five time constants (0.575 seconds), the suppressor must sustain this source or compliance voltage through a specified limiting resistance. The general range of resistor values produces surge currents in the 0.5-A to 10-A range. In addition, the specifications usually require that the device withstand 10 transient pulses, one every 30 seconds.

The duration of the load-dump transient will cause excessive junction temperatures even in many ruggedized power MOSFETs. However, using avalanche rectifiers (such as Motorola's MR2535L) in the alternator can limit the maximum voltage to 40 V, even with 90 A of reverse current for 80 µs at a junction temperature of 175 °C (Fig. 2, again).

This solution is very cost-effective because the on-resistance of power FETs increases as their breakdown voltage is increased to the 2.2 power. If a lower breakdown voltage can be used, the resulting reduction in on-resistance will reduce the cost of the power FETs, assuming that die size remains constant. Even if only a few power FETs are used, the savings can easily offset the cost of the avalanche rectifiers.

The spectrum of new automotive systems is pushing the development of power electronic components (including smart power ICs), which will ease system design and lower costs. The devices must control lighting, solenoid (inductive), and motor loads; illuminate displays; and perform dc-dc power conversion for 12-to-15-V, 12-to-24-V, and 12-to-48-V systems (see the table). Many of these loads require relatively high in-rush and/or high steady-state currents, so to minimize power dissipation or heatsinking requirements large output devices are used. Power FETs are the most frequently used semiconductor device in these cost-sensitive applications.

A critical factor in under-hood automotive applications is a high ambient temperature. As a result, the auto industry has pushed for higher maximum junction temperatures for power devices. By using plastic packaging materials with a glass transition temperature approaching 200 °C makes it possible for 175 °C ratings for the newest, energy-rated power FETs, such as Motorola's E-FET power MOSFETs.

Another class of devices, ruggedized FETs like the Motorola TMOS series, are designer-friendly components that offer opportunities to reduce the number of circuit components because they're easier to interface and they perform special functions. For example, using tighter processing controls and techniques developed for fabricating MCU and memory chips has substantially improved the typical gate-rupture capability of the MTP50N06E (a 60-V, 50-A, 0.028 Ω power FET) from approximately 40 V to over 90 V. In many applications, this improvement can eliminate the need for an external Zener diode on the gate.

The procedures used to qualify new power devices are also being beefed up. Standard practice is to use 80% of the breakdown rating during reliability tests. For all power FETs, this has been increased to 100% of the maximum data sheet rating to ensure that devices are stressed to the combined maximum temperature and voltage. For example, high-temperature gate bias tests are conducted at 100% VGS and 150 °C, and high-temperature reverse bias testing is done at 100% VDS and 150 °C. Devices that can operate at 175 °C are being qualified at the higher temperature as well.

Another important feature of power ICs is the ability to withstand a shorted load. A current-limited FET, such as the MLP1N08L, offers an integrated solution to protect semiconductor power devices from high in-rush current as well as from short circuits. With a current rating of 1.1 A, minimum breakdown voltage of 80 V, and an on-resistance of 0.75 Ω at 25 °C, the MLP1N08L limits the current that can flow in a logic-level power FET.

The current-limited FET incorporates a small-signal npn transistor and a diode from the gate to the source of an n-channel, logic-level FET (Fig. 3). Because it's designed for medium-speed switching applications that require rfi and emi to be minimized, the device has an integral resistor, R1, that limits the gate charge and discharge rate. R2 is the sensing resistor that determines the maximum current level for forward biasing of the npn tran-
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sistor. As the npn transistor turns on, gate drive is taken away from the power FET, limiting the current. The current limit is temperature dependent and decreases with increasing temperature, from 2.3 A at 25°C to 1.1 A at 150°C. The MLP1N08L withstands over 8 kV in electrostatic discharge tests conducted with the human-body model test circuit.

Because the MLP1N08L conducts current and dissipates power even during a short circuit, a heat sink is needed to keep the junction temperature below the maximum of 150°C. To simplify the user's assembly process, therefore, the current-limited FET will also be offered in a fully isolated package whose thermal performance is similar to schemes that use additional hardware, such as mica washers or commercially available isolation pads. Both versions of the FET are suitable for low-cost applications.

Two ideal automotive uses are in incandescent-lamp operation and in inductive circuitry. A standard, logic-level power FET process produces the current-limited FET. The process, which can create small-signal devices as well as power ICs, enables designers to boost integration levels with only a small increase in area needed by the basic power FET and with the addition of only one masking layer. Consequently, the cost of the added circuitry is minimal compared with the total cost of the power switching device. An intermediate level between smart-power ICs and standard power MOSFETs, dubbed Smart-discretes, differs from an IC process by the lack of isolation between circuit elements (except for the oxide-isolated diodes). Eliminating the isolation keeps the cost down but also limits the circuits that can be obtained. Moreover, parasitic elements that can occur must be accounted for in each design.

Devices made possible by the Smartdiscrete process also help fill another need in automotive electronics: diagnostic signals. The process permits a simple open-drain diagnostic scheme that can indicate the presence of an open or short fault by sending a flag to an MCU. The diagnostic uses information supplied by either the current-limit or thermal-sensing circuits.

Electronic engine control systems have used semiconductors for sensing manifold absolute pressure (MAP) for over seven years. Most frequently, a MAP sensor uses two silicon wafers to produce a piezoresistive silicon pressure sensor. The top wafer is etched until a thin, square diaphragm (approximately 1 mil thick) is created. The square area is extremely reproducible, as is the 54.7° angle of the cavity wall. In addition to absolute pressure measurements, atmospheric pressure or a reference pressure can be applied to one side of the sensor through a hole that's micromachined in the second, constraint wafer.

The latest development in semiconductor pressure sensors is the integration of all conditioning circuitry on the same chip as the micromachined diaphragm. This circuitry adjusts the offset and span, compensates for temperature effects on both offset and span, and supplies an amplified signal (Fig. 4). The device is based upon one piezoresistive sensing element positioned at a 45° angle in the center of the edge of the square diaphragm. The variation of the offset voltage and the full-scale span of this sensing element with temperature is highly predictable.
Designed to withstand continuous maintenance overcharge and high rate discharge in a sealed environment, the superior performance of Sanyo Nickel Cadmium batteries has made them ideal for use in leading products using rechargeable batteries. Review their superior technical performance for yourself and see why Sanyo Nickel Cadmium batteries are the world's choice.

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Cycle Characteristics

<table>
<thead>
<tr>
<th>No. of cycles</th>
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Discharge: (10C x 30 sec. x 1C x 30 sec.) x 20 min.

<Capacity measuring conditions>
Charge: 0.1C x 16 hrs.
Discharge: 0.2C, E = 1.0V

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CIRCLE 115
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improvements in process control implemented by Motorola have greatly increased long-term reliability. The tests used the current transfer ratio (CTR)—the ratio of transistor collector current to forward current—as a measure the LED's light output. After 7500 hours, the average CTR of the improved LEDs was still almost 98% of their initial value (Fig. 5). This testing was performed at room temperature but tests are in progress to evaluate their operation at 85°C, 105°C, and 125°C.

Several custom optical sensors have already been developed for automotive use. Two pairs of optical emitters and detectors were mounted at the end of the steering column to measure steering wheel turn angle direction and speed as part of a ride-control system. Multiple slots in a shutter interrupt the light path of the two pairs of emitters and detectors to provide the quadrature signal.

The MCU in the ride-control system uses an algorithm that determines the straight-ahead wheel position and then calculates the lateral acceleration that will result from the turn angle. If this lateral acceleration is above a programmed level, the shock absorber damping is switched to firm. The optical steering sensor also sends the MCU information that enables it to determine the rate at which the steering wheel is turning. If this rate is too high, the damping is switched to firm to supply more maneuverability.

Perhaps the most significant aspect of semiconductors is the fabrication process, which offers the ability to integrate functions while aggressively reducing cost, especially in the volumes represented by automotive applications. In the 10 years since the first use of microprocessors in vehicles, prices have dropped by more than an order of magnitude, while features and computing capability increased significantly. Continuing development ensures that new devices will be available for cost-effective performance in future automotive systems.
Automotive connectors for new performance standards in the new decade.
Every new idea in automotive electronics must meet high quality standards in a tight economy.

To provide advanced connectors that live up to those requirements, we work under a formal, corporate-wide quality program, starting from an established technological ‘platform’ and developing products that enhance the manufacturing process.

Our latest — the AMPSEAL underhood connector and the POSI-MATE instrument panel connector — typify the philosophy. Both employ proven contact technology, a design platform that offers easy reliability projections and cuts development and testing time significantly.

Yet both still allow application-specific versions, particularly the high-density POSI-MATE connector, which can be implemented in many configurations.

Crimp contacts allow automated termination, and the clean (lanceless) design uncomplicates handling. Terminal position assurance is provided by the housings. Our IP connector goes a step further with connector position assurance: for protection against under-dash tugs, the latch can also be locked.

Both assemble quickly, but our AMPSEAL high-temp submersible connector is unique — it literally goes together in seconds.

The housing comes preassembled, seals in place, with the front partially extended. In a simple, two-stage loading sequence, terminals are first inserted through the rear seal area and held firmly in the positioning stage. When the front is pushed into place, the contacts are locked.

Both connectors provide an inherent quality control check as well — the housings won’t assemble if a contact is in wrong. Ideas like this have helped us meet tough quality/manufacturability requirements in the global automotive arena for decades, and in every related industry as well. We’d like to help you.

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We'd like to name names, but the story is still unfolding.

One of the Big Three automobile manufacturers had been buying custom controllers for instrumentation lighting from an off-shore vendor—we're talking about a million pieces annually—when the dollar suddenly took a downturn.

Faced with continuing price increases, they went looking for a reliable domestic supplier: "All we need is a simple form, fit and function replacement," they said.

Not so simple. As they discovered, other suppliers either wanted to sell them standard parts or an expensive ASIC. Furthermore, no one was willing to make the effort to supply an IC and hybrid and make it cost competitive. It was driving them nuts.

Then in marched the General.

Because we're set up to provide custom hybrid power IC solutions, we routinely dedicate a program manager to the project. In this case, he not only successfully engineered exactly the part they wanted, he also pioneered a few improvements of his own.

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LOW-SKEW CLOCK DRIVERS MAXIMIZE MPU SYSTEMS

Today's CISC and RISC microprocessor systems have frequencies that approach 40 to 50 MHz. As a result, maintaining a synchronous system demands precise, well-controlled clock signals. Many microprocessors also require input clock duty cycles very close to 50%. These stringent timing requirements mandate the use of special, low-skew clock distribution circuits, or clock drivers. Just plugging one of these parts into a board doesn't ensure a trouble-free system, however. Meeting system timing requirements and providing clean clock signals call for careful design techniques for systems and pc boards.

Designers of microprocessor systems want to use as much of a clock cycle as possible without adding unnecessary timing guardbands. Unfortunately, propagation delays of peripheral logic don't scale with frequency. Therefore, as the clock period decreases, system designers have less time but the same logic delays to accomplish the function. How do designers gain more time? One option is to use a special clock source that minimizes clock "uncertainty."

A simple example illustrates this concept. At 33 MHz, $T_{cycle} = 30$ ns. An FCT240A octal inverter buffer, for example, has a high-low uncertainty of the min/max spread of $t_{PLH}$ to $t_{PHL}$ of about 3.3 ns. If 1.7 ns of pin-to-pin skew due to the actual part and pc-board trace delays is also considered, then only 25 ns of the clock period is still available. The worst-case $t_p$ of clock-to-data valid on the 88200 M-bus is 12 ns, which leaves only 13 ns to accomplish other functions. In this case, 17% of a cycle is required for clock distribution or clock "uncertainty." From a system designer's point of view, this percentage is an unacceptable penalty. At 50 MHz,
The penalty balloons to 25%.

A maximum of 10% of the period allotted for clock distribution is an acceptable standard. If multiple levels of clock distribution (one clock driver’s output feeding the inputs of several other clock drivers) are necessary owing to large clock fan-outs, the additional part-to-part skew variations add even more to the clock uncertainty. Standard logic has always been specified with a large (and conservative) delta between the minimum and maximum propagation delays. This delta creates excessive clock uncertainty, which designers have been forced to design into their systems, even though it’s unrealistic.

When system frequencies were below 16 MHz, this large clock penalty could be tolerated. As the preceding example points out, that’s not the case today. A clock driver’s specifications guarantee this min/max delay delta to be a specific, small value. To reduce the clock overhead to manageable levels, a clock driver with minimal variation (less than 5%) from a 50% duty cycle and guaranteed low output-to-output and part-to-part skew must be used.

**CLOCK-SKEW DEFINITIONS**

A typical clock driver has one input, which is usually driven by a crystal oscillator. The clock driver can have any number of outputs, which have a certain frequency relationship to the clock input. And clock-driver skew is typically defined by three different specifications (Fig. 1).

The first specification, \(t_{os} \) measures the difference between the fastest and slowest propagation delays (any transition) between the outputs of one part. Note that this number must be 1 ns or less for high-end systems.

The second specification, \(t_{ps} \), measures the difference between the high-to-low and low-to-high transition for one output (pin). It defines how close to a 50% duty cycle the clock driver’s outputs will be. For example, if this specification is 1 ns (\(\pm 0.5 \) ns), the output duty cycle at 33 MHz is 50% (\(\pm 3.5\%\)). A clock driver, which buffers only the crystal input, creates a 1:1 input to output frequency relationship. This can be a problem if a very tight tolerance to a 50% duty cycle is required.

**OUTPUT DUTY CYCLE**

In this case, the output duty cycle depends on the input duty cycle, which isn’t well-controlled in most crystal oscillators. The clock driver’s outputs switching at half the input frequency (\(\pm 2\%\)) is a common relationship. This means that the outputs switch on only one edge of the oscillator. As a result, the output doesn’t depend on the duty cycle of the input (crystal oscillator frequency is very stable).

The third specification, \(t_{pv} \), measures the maximum propagation-delay delta between any given pin on any part. This specification defines the part-to-part variation between any clock driver (of the same device type) ever shipped. This number reflects the process variation inherent in any technology.

For CMOS, \(t_{pv} \) is usually 3 ns or less (see “What’s available now?”). High-performance ECL technologies can bring this number down into the 1-to-2-ns range. Another way to minimize the part-to-part variation is to use a phase-locked-loop clock driver, which is just now becoming available.

When designing a clock driver into a system, it’s important to give consideration to the skew specs that are usually specified at a fixed, lumped capacitive load. In a real system environment, the clock lines usually have various loads distributed over several inches of pc-board trace, which can contribute additional delay. Because the clock lines sometimes act as transmission lines, the system designer must use careful board-layout techniques to minimize the total...
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LOW-SKEW CLOCK DRIVERS

system skew. In other words, just plugging a low-skew clock driver into a board won't solve all timing problems.

Consider a scale replication of a section of an RISC 88000 system board layout (Fig. 2). The board section includes the MC88100 CPU, the MC888200 cache MMU devices, and the MC88914 CMOS clock driver. The only pc-board traces shown are the clock-output traces from the MC88914 to the various loads. For this clock driver, the output-to-output skew (t_{pdc}) is guaranteed to be less than 1 ns at any given temperature, supply voltage, and fixed load up to 50 pF.

MINIMIZE CLOCK SKEW

To calculate the total system skew, the difference in clock pc-board trace length and loading must be taken into account. For an unloaded pc-board trace, the signal delay per unit length, t_{pd}, depends only on the dielectric constant, e_r, of the board material. The characteristic impedance, Z_0, of the line depends upon e_r and the trace’s geometry. These relationships are depicted for a microstrip line (Fig. 3). The formulas for t_{pd} and Z_0 are slightly different for other types of strip lines. For simplicity, all calculations in this article assume a microstrip line.

The equations are valid only for an unloaded trace. Loading down a line increases its delay and lowers its impedance. The signal-propagation delay (t_{pd}) and characteristic impedance (Z_0) due to a loaded trace are calculated by the formulas:

\[ t_{pd}' = t_{pd} \sqrt{1 + C_d/C_0} \]
\[ Z_0' = Z_0/\sqrt{1 + C_d/C_0} \]

C_d is the distributed load capacitance-per-unit-length, which is the total input capacitance of the receiving devices, divided by the length of the trace. C_0 is the intrinsic capacitance of the trace, which is defined as:

\[ C_0 = t_{pd}/Z_0 \]

Assuming typical microstrip dimensions and characteristics as w = 0.01 in., t = 0.002 in., h = 0.012 in., and e_r = 4.7, the equations yield Z_0 = 69.4 \Omega and t_{pd} = 0.144 ns/in. (Fig. 3 again). C_0 is then calculated as 2.075 pF/in. If it’s assumed that an MC88100 or 88200 clock input load is 15 pF and that two of these loads, along with a 7-pF FAST TTL load, are distributed along a 9.6-in. clock trace, C_d = 37 pF/9.6 in. = 3.85 pF/in. The loaded trace propagation delay and characteristic impedance are then calculated as t_{pd}' = 0.243 ns/in. and Z_0' = 41 \Omega.

In terms of trace c, the two MC88200s are about 3 in. apart (Fig. 2, again). Using the calculated value of t_{pd}', the clock-signal skew due to the trace is about 0.7 ns. Because these two devices are on the same trace, this is the total clock skew between these devices. Careful inspection of all the clock traces shows that clock-signal skew was accounted for and minimized on the board layout. The longest distance between any 88000 devices on one clock trace is

WHAT’S AVAILABLE NOW?

Low-skew clock drivers come in several technologies (see “How is a low-skew clock-driver chip achieved?”, p. 96). There are big differences among clock drivers in operating frequencies, voltage levels, power consumption, and packaging (see the table). Some drivers have features like power-off reset and external reset, which enables multiple clock-driver devices to be synchronized.

One clock driver design that can be helpful in large applications is the MC88915 phase-locked loop. Using an internal V_{cc} and phase-frequency detector, the PLL forces the driver output always to be in phase with the input signal. Thus, a system clock, which feeds several boards and may be of lower frequency, can be regenerated after crossing a backplane to ensure that each board is synchronous with the others.

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<td>4Q'</td>
<td>9Q+9Q'</td>
<td>80Q–1:1</td>
</tr>
<tr>
<td>Levels (V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{oh} )</td>
<td>2.5</td>
<td>-1.1</td>
<td>2.5</td>
<td>-0.5</td>
</tr>
<tr>
<td>( V_{ol} )</td>
<td>0.15</td>
<td>1.5</td>
<td>0.5</td>
<td>1.7/1.6</td>
</tr>
<tr>
<td>Timing (50-pF load; maximum values):</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{pd} )–propagation delay skew (ns)</td>
<td>1</td>
<td>1</td>
<td>0.15</td>
<td>1</td>
</tr>
<tr>
<td>( t_{pd} )–output-to-output skew (ns)</td>
<td>1.5</td>
<td>0.05</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>( t_{pd} )–part-to-part skew (ns)</td>
<td>3.3</td>
<td>0.5/0.5</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Drive sink/source current (mA)</td>
<td>24/24</td>
<td>20/24</td>
<td>50/15</td>
<td>24/15</td>
</tr>
<tr>
<td>Input requirements</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{in} ) (V)</td>
<td>2.0</td>
<td>2.0</td>
<td>-0.7</td>
<td>PECL/TTL</td>
</tr>
<tr>
<td>( V_{il} ) (V)</td>
<td>0.8</td>
<td>0.8</td>
<td>-1.4</td>
<td>PECL/TTL</td>
</tr>
<tr>
<td>Pulse width (minimum) (ns)</td>
<td>3</td>
<td>6</td>
<td>0.1</td>
<td>3.5</td>
</tr>
<tr>
<td>Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>+4.5 to +5.5</td>
<td>+4.5 to +5.5</td>
<td>-5.0 to -5.4</td>
<td>+4.75 to 5.25</td>
</tr>
<tr>
<td>( I_{CC \text{ (quiescent)}} ) (mA)</td>
<td>1.5</td>
<td>70</td>
<td>60</td>
<td>70</td>
</tr>
<tr>
<td>Packaging</td>
<td>14-pin DIP, 14-pin SOIC</td>
<td>14-pin DIP, 14-pin SOIC</td>
<td>28-pin PLCC, 28-pin PLCC</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1 If \( \phi_1 \text{actual} \neq \phi_2 \text{actual} \)
2 Any two outputs from a given input clock
3 For a given set of conditions (that is, capacitive load, temperature, and \( V_{CC} \)) at each device
4 Reference data sheet MC74F803
5 Reference data sheets MC88913, 88914, 88915
6 Reference data sheets MC10E111, 100E111
7 Reference data sheets MC10H, 100H640, 641, 642, 643
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about 4.5 in., which translates to about 1.1 ns of skew.

The two 88000 devices farthest from the clock driver (traces a and c) are at about the same distance along their respective traces. This makes the clock skew between them the 1 ns guaranteed from output to output of the clock driver. As a result, the worst-case clock skew between any two devices on this board is about 2.1 ns.

Consider then a clock-signal waveform seen at the receiver end of an unterminated 0.5-in. trace and an unterminated 9-in. trace (Fig. 4). These results, which were obtained using Spice simulations, may not be exact but are adequate to predict trends and for comparison purposes. The 9-in. trace, well beyond the 1.5-in. limit where transmission-line effects come into play, exhibits unacceptable switching characteristics caused by reflections shuttling along the trace. Even the 0.5-in. line exhibits substantial overshoot and undershoot. At these edge rates, any unterminated line shows some overshoot and undershoot.

Transmission-line effects occur when a large mismatch is present between the characteristic impedance of the line and the input or output impedances of the receiving or driving device. The basic guideline to determine if a p-c board trace needs to be examined for transmission-line effects is as follows: If the smaller of the driving device's rise or fall time is less than three times the propagation delay of a switching wave through a trace, transmission-line effects will be present. This relationship can be stated as an equation:

\[ 3 \times t_{pd} \times \text{trace length} \leq t_{\text{rise or fall}} \]

For the MC88914 CMOS clock driver described previously, rise and fall times are typically 1.5 ns or less (from 20% to 80% of \(V_{cc}\)). Analyzing the clock-trace characteristics presented earlier for transmission line effects means that \(3 \times 0.243 \text{ ns/in.} \times \text{trace length} \leq 1.0 \text{ ns} \) (1 ns is used as “fastest” rise or fall time). Therefore, the trace length must be less than 1.5 in. for the transmission-line effects to be masked by the rise and fall times.

4. SPICE SIMULATIONS, run with parameters of 25° and \(V_{cc}\) of 5 V, were done for an unterminated, 0.5-in., 41-μ transmission line (a) and an unterminated, 9-in., 41-μ transmission line (b). The 9-in. trace shows unacceptable switching characteristics caused by reflections moving back and forth along the trace. Even the 0.5-in. line shows a great deal of overshoot and undershoot.
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Because clock lines are driven only from one location, they lend themselves to termination more easily than bus lines, which are commonly driven from multiple locations. Digital systems use various types of termination techniques (Fig. 5). Because no single termination scheme is optimal in all cases, the trade-offs in the use of each needs to be discussed and recommendations made specific to clock drivers.

The driving device in the Spice simulations of various termination schemes was the MC88914 output buffer. In all simulations, it drove a 9-in., 41-Ω transmission line. The simulations were run using model parameters at 25°C and $V_{CC}$ of 5.0 V.

**Series Termination**

Series termination is recommended if the load is lumped at the end of the trace and the output impedance of the driving device is less than the loaded characteristic impedance of the trace. It is also recommended when a minimum number of components is required. The problem with series termination arises when the driving device has different output impedance values in the high and low states, which occurs in TTL and some CMOS devices. A well-designed CMOS clock driver should have nearly equal output impedances in the high and low states, avoiding this problem. An additional advantage is that series termination doesn’t create a dc current path.

As a result, the $V_{OH}$ and $V_{OL}$ levels aren’t degraded. The Spice-generated waveforms of series termination show that this termination effectively masks transmission-line effects.

If each clock output is driving only one device, series termination is recommended. Because this isn’t realistic in most systems, series termination isn’t generally advised for clock-line termination.

Parallel termination uses one resistor tied to ground or $V_{CC}$, whose value is equal to the line’s characteristic impedance. Its major disadvantage is the dc current path it creates when the driver is in the high state (if the resistor is tied to ground). This performance ECL devices.

Designing and manufacturing a low-skew clock-driver chip calls for many of the same factors in system design, but obviously on a much smaller scale. Careful circuit design, symmetrical layout techniques, and good control of the fabrication process are needed for low output-to-output and part-to-part skew characteristics.

First, using circuit design methods, the high-to-low and low-to-high transitions from the clock input to the distributed outputs must be as close as possible to each other. Then the rise and fall times of a signal out of the output buffers (drivers) must be evenly matched. This is done by matching the output impedances of the pull-up and pull-down transistors. Satisfying these two requirements results in a 50% duty cycle.

The design-related methods depend on computer simulations and the accuracy of the simulator models. But when the circuit is implemented in silicon, layout parasitics can adversely affect circuit performance. Chip-level parasitics are similar to the pc-board trace parasitics that must be accounted for when calculating signal delays on the board level. However, one advantage at the chip level, due to the short length of signal lines, is that transmission-line effects are negligible. A clock-distribution part has several outputs, usually at least four, whose propagation delay skews must be matched within a given tight specification (for example, less than 1 ns). If the path to one output has more layout-induced parasitic resistance and/or capacitance than the other outputs, then its propagation delay might be slower than the others by more than the specified limit.

Layout parasitics are always present, therefore the trick is to match the parasitics of each output as closely as possible. This means that the layout must be symmetrical, with the path from clock input to each output looking almost identical. As such, the length and parasitic resistance and capacitance of each signal path must be equal. ECL’s extremely high switching speeds also demand that the characteristic impedance of the paths be tailored to avoid reflections at the branching points.

Packaging effects must also be considered to minimize skew. The leads of a standard DIP package have large parasitic inductive parasitics. As a result, the outputs must be connected to package leads that have matched inductances—that is, symmetrical pins on opposite sides of the package. Again, for ECL, the high speeds demand a package such as a plastic leaded chip carrier, which minimizes the inductive and capacitive effects of the pins. External impedance matching of clock lines is also important.

Within a part, the circuit design, layout, and packaging techniques that are described guarantee that one part will have low output skew. However, in a synchronous system using more than one clock driver device, the part-to-part output skew must be within a reasonable tolerance (two to three times the output-to-output skew).

Achieving this goal requires tight control over the fabrication process. CMOS particularly doesn’t have ECL’s high temperature and voltage compensation features. How well critical process parameters, such as channel length and threshold voltage, are held within a small tolerance determines how small the part-to-part variation will be.

References
1. “A Clock Distribution Circuit with a 100-ps Skew Window” by Rajnish Maini, James McDonald, and Lou Spangler, IEEE 1987 BTCM.
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causes excessive power dissipation and $V_{OH}$ level degradation. Because a clock driver output is always switching, the dc-current-draw argument loses some credibility at higher frequencies. For one thing, the ac switching current becomes a major component of the overall current. Therefore, the key consideration in parallel termination is how much $V_{OH}$ degradation can be tolerated by the receiving devices. This termination technique is effective in minimizing switching noise. Nonetheless, Thevenin termination has some advantages compared with parallel termination.

Thevenin termination uses one resistor tied to ground and a second tied to $V_{CC}$. When designers use this type of termination, it’s important that they consider the choice of resistor values to avoid settling of the voltage between the high and low logic levels of the receiving device. TTL designers commonly use a 220/330 resistor value ratio, but CMOS is somewhat tricky because the switch point is at $V_{CC}/2$. With a 1:1 resistor ratio, a failure at the driver output would cause the line to settle at 2.5 V. Besides causing system-debugging problems, this could lead to potential damage to the receiving devices.

In Thevenin termination, the parallel equivalent value of the two resistors should equal the line’s characteristic impedance. A dc path does exist in both the high and low states. However, it’s better than parallel termination because the resistance in the Thevenin dc path is at least two times greater.

The Thevenin termination waveforms exhibit characteristics similar to those for parallel termination but with less $V_{OH}$ degradation (Fig. 6). The only real advantage of parallel over Thevenin is fewer resistors (half as many), resulting in more available board space. If space isn’t a factor, Thevenin termination is recommended over parallel.

Ac termination typically uses a resistor and capacitor in series to ground. The capacitor blocks dc current flow but allows the ac signal to flow to ground during switching. The time constant of the resistor and capacitor must be greater than twice the loaded line delay. Ac termination is recommended because of its low power dissipation and the availability of the resistor and capacitor in single-in-line packages (SIP). A pull-up resistor to $V_{CC}$ is sometimes added to set the dc level at a certain point because of the failure condition described in regard to Thevenin termination. As noted earlier, the argument of lower dc current is less convincing at high frequencies. The ac-terminated waveform walks out slightly toward the end of a high-to-low or low-to-high transition, making it somewhat less desirable than Thevenin termination at higher frequencies.

Thevenin and ac termination are the two recommended termination schemes for clock lines, but it depends on the clock’s frequency. It’s safe to assume that ac is the best choice at frequencies of 25 MHz and below. If the system frequency could reach 40 MHz and beyond, Thevenin becomes the better choice.

The results presented might imply that terminating the clock lines completely solves noise problems, but termination can cause secondary problems with some logic devices. Termination acts to reduce the noise seen at the receiver, but that noise actually appears as additional current and noise at the driving device’s output. If the internal and input logic on the source device isn’t sufficiently decoupled on chip from the high-current outputs, internal threshold problems can occur. This phenomenon is commonly known as “dynamic threshold.” It’s usually evidenced by glitches appearing on the outputs of a fast, high-current drive logic device as it switches high or low. This is most severe on “ACT” devices,
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6. SPICE SIMULATIONS, run with parameters of 25° and $V_{cc}$ of 5 V, were done for various terminations of a 9-in., 41-Ω transmission line. Simulation results are for series termination (a); parallel termination (b); Thevenin termination (c); and ac termination (d). The waveforms for Thevenin termination show similar characteristics to those of the waveforms for parallel termination, but there is less $V_{OH}$ degradation.

which have high current and high slew-rate CMOS outputs, along with TTL inputs, which have low noise immunity. This problem can be minimized by decoupling the internal ground and $V_{cc}$ supplies on-chip and in the package.

This decoupling is accomplished by having separate “quiet” ground and $V_{cc}$ pads on-chip, which supply the input circuitry’s ground and $V_{cc}$ references. These pads are then tied to extra “quiet” ground and “quiet” $V_{cc}$ pins on the package or to special “split leads.” These resemble a tuning fork and use the leadframe inductance to accomplish the decoupling. When choosing a clock source, designers should note that the part must have one of these decoupling schemes.

A reliable, high-frequency microprocessor system requires a low-slew clock driver, along with special attention to the board layout of clock traces. The line lengths and loading must be matched to avoid excessive signal skew between CPUs, cache MMUs, and other critical peripheral devices.

To ensure a clean clock signal throughout the system, clock traces must also be terminated in some fashion. Carefully addressing these issues early in the design cycle helps designers to guarantee optimal system performance.

References

Chris Hanke, a CMOS design engineer in Motorola’s Logic IC Division, received BSChemEng and MSEE degrees from Rensselaer Polytechnic Institute, Troy, N.Y.
Gary C. Thoralson, a new product planner in Motorola’s Logic IC Division, Mesa, Ariz., received a BSEE from the University of Minnesota and an MBA from Arizona State University.

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CIRCLE 105
Ganged potentiometers are widely used in audio stereo systems and in many instrumentation circuits. Often, the performance deficiencies in this type of equipment can be traced back to the ganged potentiometers, which have two resistance tracks that are out of step. Here, a circuit is developed to rapidly test the ganged-potentiometer tracking. The tracking error can be measured with an accuracy of better than 1% at all shaft-slider positions in the entire electrical travel of the potentiometer.

The circuit uses ultra low-offset-voltage op amps, eliminating the need for offset nulling (see the figure). The inverting amp built around op amps U₁ and U₃ uses the potentiometers under test as feedback resistors.

At any given shaft-slider position, let $R_1 / R_2 = n$ volts at point A. As a result, $V_A = 1 \times (R_1 \, \text{k}Ω / 1 \, \text{k}Ω) = R_1 = nR_2$.

The voltage at point D, $V_D = V_C / \text{gain of } U_3 = nR_2 / (R_2 / 1) = n$, and at point E, $V_E = 10 \times (n - 1)$.

These relationships show that $V_E$ is positive when $R_1 > R_2$, zero when $R_1 = R_2$, and negative when $R_1 < R_2$. One volt at the circuit's output corresponds to a tracking error of 10%.

This circuit measures the tracking error of ganged potentiometers. Less than 1% accuracy can be achieved at all shaft-slider positions of the potentiometer.
ular concern, especially that produced by resistor R5. The circuit is limited to low-frequency and dc applications due to its 400-nV/√Hz noise. For applications that don’t require the circuit’s 10-pA output, lower values of R5 can be substituted. This will cause an increase in bandwidth.

Because a high impedance exists at the input, a 10:1 resistive attenuator can be added to enhance the resolution of the input source. The output of the circuit is trimmed to 0 pA, while the input is grounded. As the circuit is assembled, care should be taken to prevent leakage-current errors. When the prototype was built, R5 was mounted on teflon standoffs and pin 3 of U2 was soldered directly to R5.

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The RTD’s resistance can also be found by determining the current and voltage separately (see the figure). When the 7407 open-collector output transistor is on, current I flows through R1, R2, and the RTD. R1 limits this current to a maximum of 33 mA.

A data-acquisition system measures the voltage across R2 and across the RTD. The circuit’s microprocessor (not shown in the figure) divides V_R2 by R2 to find I, then divides V_RTD by I to find the RTD resistance. When these steps are followed, I drops out of the equation leaving:

\[ \text{RTD resistance} = \frac{R_2 \times V_{\text{RTD}}}{V_{R2}}. \]

This approach offers four advantages over conventional methods that employ a constant-current source to supply the known current. First, the signal-to-noise ratio (SNR) is excellent because a large RTD voltage is induced by a large current. Second, only one precision component (R2) is required to supply a high-accuracy result. A constant-current source with the same accuracy and SNR would need additional high-precision components.

The third advantage of this method is that the current can be switched on and off by a TTL signal. Errors caused by selfheating of the RTD can be reduced by turning the current off between measurements. Finally, the RTD resistance can vary over a large range. The constant-current-source method has a much smaller range because it can’t supply the required current when the RTD resistance exceeds the quotient of V_supply/I_constant.
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September 11-13, 1990
Dallas Convention Center

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CIRCLE 82
NEW PRODUCTS

WORKSTATIONS AND HDTV GET TRIPLE 10-BIT 80-MHZ DAC ICs FRANK GOODENOUGH

For the first time, designers of high-resolution computer graphics systems can get 10-bit video digital-to-analog converter (DAC) ICs. Moreover, they can get three of these 80-MHz DACs on a single chip for under $20. The ADV7121/22 triple DACs from Analog Devices can resolve over one billion colors at any given time, a capability that's well beyond that of the human eye. Such capability is needed by sophisticated color graphics systems such as HDTV and workstations, to linearize the transfer-function curve of drive current to light output (also known as a Gamma curve) of the display system (see the figure).

The DACs are aimed at any high-resolution color graphics application employing a true-color system or a special lookup table. These include workstations, medical imaging, and even high-end PCs.

With the higher 10-bit resolution (instead of the more common 6 or 8 bits), calculations for the required color shadings become simpler. For the graphic designer in need of a color with half the intensity, it's much easier to call out a digital half-code than to calculate which code associated with the given display system will produce the desired color.

This feature is in such high demand that NHK (the Japanese equivalent of the FCC) designed the 7121 into the prototype system they use for receiving their MUSE HDTV standard. Other HDTV development teams in both the U.S. and Europe are already using these DACs for their prototype systems. The DACs also comply with the Society for Motion Pictures and Television Engineering (SMPTE) 240, a proposed U.S. production HDTV standard.

At the heart of each ADV7121 and ADV7122 lie three RGB, 10-bit 30-, 50- or 80-MHz DACs, each with its own TTL-compatible latched pixel input port. An additional input is provided for the pixel clock which strobes the latches to refresh the DAC outputs. A reference amplifier converts an external 1.235-V reference to a 17.7-to-18.5-mA fullscale current source for each DAC. A variable resistor connected to the amplifier sets the exact fullscale current—the white level for all three DACs. The current sources are compliant from -1.4 to +1 V. Thus, each DAC can develop 0.5 V at the end of a doubly terminated 75-Ω line.

IDENTICAL DEVICES

The two devices are identical (the same chip) except that the 7121 lacks the SYNC and BLANK inputs due to its 40-pin double-width DIP package (the 7122 is in a 44-pin PLCC). In addition to the three speed-versions and two packages types, there are two performance grades. Integral and differential nonlinearity (INL and DNL) of the J-grade device run ±3 and -1 LSB maximum, respectively, over the temperature range of 0 to 70°C. Under similar conditions, INL and DNL of the K-grade units run ±2 and ±1 LSB, respectively. All are guaranteed to be monotonic over temperature.

The availability of three speed versions permit system designers to choose the most economical device as a function of CRT resolution. For example, at a refresh rate of 60 Hz, the 80-MHz converters are required for the latest 1024-by-1024-pixel CRT displays. Maximum current consumption from a 5-V power-supply rail for these CMOS chips is just 125 mA for the 80-MHz units and 100 mA for the others. In quantities of 1000, pricing ranges from $18.35 each for the 30-MHz, J-grade ADV7121 to $35.30 each for the 80-MHz, K-grade ADV7122. Small quantities are in stock.

Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; Chris Hyde, (617) 937-1422 CIRCLE 301
NEW PRODUCTS

MULTIPLEXED SAMPLING AMPLIFIER DELETES COSTLY DACS

While the cost of 12-bit IC d-a converters (DACs) has dropped, if you need a lot of them, total system cost can climb—and they not only take space, but the input digital lines to them do as well. Another approach, somewhat analogous to dynamic vs static RAMs, uses a single DAC and multiple sample-and-hold amplifiers which are continuously refreshed. To fill that need, Precision Monolithics has announced the SMP-08. It has eight, voltage-output, sample-and-hold amplifiers any one of which can have its held voltage uniquely updated, at any time, from a single DAC. A 3-bit input word selects the channel. An update to 8-bit accuracy for 0 and 10 V typically takes 1 µs. Droop rate is 0.25 mV/ms. And that's with on-chip capacitors. Absolute accuracy is 8-bits, linearity 12-bits. Unit price in lots of 100 runs $6.25.

Precision Monolithics Inc. P.O. Box 58202, Santa Clara, CA 95053-8020; Walt Heinzner (408) 562-7254. FRANK GOODENOUGH

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Phone: (214) 272-3571 Fax: (214) 494-2281
Micropac is Certified to MIL-STD-1772
CIRCLE 139

SAMPLE TO 16-BIT ACCURACY IN 250 NS

With the SP9760 sample-and-hold amplifier, you can grab a 10-V signal to 16-bit accuracy in just 250 ns, typical, and a 20-V signal to the same accuracy in typically 350 ns, or 500-ns maximum. This hybrid, whose speed comes from a pair of custom dielectrically-isolated ICs, is the fastest 16-bit accurate sampling amp available. Other critical specifications for the 0-70 °C model include an aperture uncertainty of 75 ps rms and a full-power bandwidth of 2 and 4 MHz respectively for 20- and 10-V output swings. Slew rate is a minimum of 75 V/µs. Total harmonic distortion at 100 kHz for 5 Vp-p output is typically -90 dB; at 10 kHz for a 20 Vp-p signal, it is -88 dB. Applications include CAT scanners, magnetic resonance imaging, and high-performance automatic test equipment. In its 24-pin double width DIP the commercial grade SP9760 runs $199 each in hundreds. The mil-grade unit $90 more.

Sipex Corp. 6 Fortune Dr., Billerica, MA 01821; Jack Worthen (508) 663-9981. CIRCLE 308

SHUNT REFERENCE IN TO-92 SINKS 100 MA

An adjustable shunt-type linear reference/regulator, the LT1431, comes in a 3-pin TO-92 as well as 8-pin DIPs and SOICs. It contains a 2.5-V band-gap reference, its output transistor sinks 100 mA, and, with just a single external resistor, can be connected to deliver 2.5 or 5 V out with 1% accuracy. Two resistors set the output voltage between 2.5 and 36 V. It can also provide the reference and isolated negative feedback in a 5-V switching regulator by connecting a resistor to the regulator's output and driving the LED in an opto-isolator with the IC's open-collector npn. The LT1431 (TO-92) goes for just $0.92 each in hundreds.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott, (408) 432-1900. CIRCLE 304
Want to see a precision narrowband sweep that usually takes about a minute?

Oops, you blinked.

By blending digital-filter and FFT techniques with swept technology, the new HP 3588A spectrum analyzer makes this measurement in less than a second... with high resolution and ±0.25 dB typical accuracy.

This analyzer offers unprecedented speed in two measurement modes. In the swept mode, you get a 10 Hz to 150 MHz range, RBW as narrow as 1.1 Hz and measurements up to 16 times faster than previously available. The narrowband-zoom mode gives you a span of 40 kHz or less anywhere in the 150 MHz range, RBW to 0.0045 Hz and measurements up to 400 times faster than traditional swept analyzers.

So, call 1-800-752-0900 today. Ask for Ext. 1212, and we'll send a videotape demo so you can see these fast measurements for yourself. But don't blink.

There is a better way.
The latest member of the HP 82000 family of IC evaluation systems, the Model D400, boasts a 400-MHz maximum vector rate that lets engineers verify their designs and characterize prototype ICs and ASICs at the devices’ full performance limits. In the past, designers had to use formulas to make assumptions about device behavior at full speed. The system accuracy is an excellent ±200 ps. Maximum pin capacity is 512 pins. Memory capacity of up to 1 Mvector is available behind each I/O pin. A tester-per-pin architecture permits independent per-pin timing and voltage levels.

The HP 82000 series features a modular design, so users can start with a basic configuration and increase pin count and vector rate as the need arises. HP can supply a variety of links to all commonly used electronic design automation systems. New high-throughput software is available to make the tester suitable for small-batch production testing.

The HP 82000 Model D400 costs about $3400 per I/O channel, depending on the number of channels and the system configuration. Delivery is estimated at 12 weeks.

Hewlett-Packard Co. Inquiries, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.

Contact-free soldering and de-soldering of SMD, DIP and pin grid components and connectors in a matter of seconds with the Leister-Labor “S” hot-air tool. Electronic control of temperature and air supply. Over 400 special nozzles available.

Ask for free brochure UW 169

Brian R. White Co. Inc., 313 Henry Station Road
Ukiah, CA 95482 phone: (707) 462-9795
Farmingdale, NJ 07727 phone: (201) 938-2700

A newly designed lanthanum hexaboride high-performance electron source produces an 80-nm probe size for the IDS 5000Plus integrated diagnostic system. The new source offers a long, reliable cathode life approaching 2000 hours on the electron-beam probing system to ensure full brightness during design debug and verification, failure analysis, and device characterization. The unit features an electron column positioning system that delivers 0.2-µm resolution over a die area four times that of other systems, so engineers can probe chips up to 32 mm square. The IDS 5000Plus costs $625,000. Current IDS users can retrofit the IDS 5000Plus submicron capabilities and other features to their older systems.

Schlumberger Technologies, ATE Div., 1601 Technology Dr., San Jose, CA 95110-1397; (408) 453-0123.

A 16-bit multifunction data acquisition board for the PC/AT and compatibles features 16 single-ended and eight differential analog inputs. The LSDAS-16 includes an autocalibrating analog-to-digital converter, a 50-kHz sample rate, two deglitched digital-to-analog converters with optional buffer memory, a digital I/O port, and timers. An optional 32-ksample buffer memory generates waveforms independently of the host. The board comes with a full-function setup program and data acquisition utilities. Other software support available includes libraries to help in program development and a high-level language interface for C, Pascal, QuickBasic, and Fortran. Available from stock, the LSDAS-16 lists for $1285. Volume discounts are available. The optional memory costs $200.

Analogic Corp., Data Conversion Products Group, 360 Audubon Rd., Wakefield, MA 01880; (800) 446-8936.
Small Company's New Golf Ball Flies Too Far; Could Obsolete Many Golf Courses

Pro Hits 400-Yard Tee Shots During Test Round

Want To Shoot An Eagle or Two?

By Mike Henson

MERIDEN, CT — A small golf company in Connecticut has created a new, super ball that flies like a U-2, puts with the steady roll of a cue ball and bites the green on approach shots like a dropped cat. But don't look for it on weekend TV. Long-hitting pros could make a joke out of some of golf's finest courses and real men don't play par-three's. This new fly-power forces us to imagine a pro using it on TV and eagle-ing par-fours? It would turn the course into a par-three, and real men don't play par-three's. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There's more to golf than tournaments, you know.

The company guarantees a golfer a prompt refund if the new ball doesn't cut five to ten strokes off his or her average score. Simply return the balls — new or used — to the address below. "No one else would dare do that," boasted the company's director.

If you would like an eagle or two, here's your best chance yet. Write your name and address and "Code Name S" (the ball's R&D name) on a piece of paper and send it along with a check (or your credit card number and expiration date) to National Golf Center (Dept. H-1448), 500 S. Broad St., Meriden, CT 06450. Or phone 203-238-2712, 8-8 Eastern time. No P.O. boxes, all shipments are UPS. One dozen "S" balls cost $24.95 (plus $2.50 shipping & handling), two to five dozen are only $22.00 each, six dozen are only $109.00. You save $55.70 ordering six. Shipping is free on two or more dozen. Specify white or Hi-Vision yellow.

TV advertising is too expensive to buy on your own, at least for us. "Now, you've seen how far this ball can fly. Can you imagine a pro using it on TV and eagle-ing par-fours? It would turn the course into a par-three, and real men don't play par-three's. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There's more to golf than tournaments, you know."

The company guarantees a golfer a prompt refund if the new ball doesn't cut five to ten strokes off his or her average score. Simply return the balls — new or used — to the address below. "No one else would dare do that," boasted the company's director.

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**NEW PRODUCTS**

**ARRAY-PROCESSOR BOARD COMBINES i860, i960 RISC CHIPS**

A board-level array processor, the Warrior III, from Sky Computers Inc., combines the Intel i860 and i960 RISC processors to achieve a processing speed of 80 MFLOPS. A prevectorized software library optimizes the 64-bit i860, which performs all arithmetic operations. The i960 chip, acting as a DMA engine, handles system I/O, memory transfers, diagnostics, and other housekeeping functions. It can fetch data from anywhere in the VME host and is responsible for prefetching and caching the data. Thus feature minimizes the need for dedicated memory for the array processor.

Because of the extensive software library that exists for the Warrior III, users can easily develop custom applications in C or Fortran. There's no need to resort to complex assembly code or microcode. Users can access and manipulate data in rows, columns, or any pattern in a multidimensional array stored in memory.

Multiple Warrior III boards, operating in parallel, can be tied together without any I/O degradation. And the board uses just 37 W of power with a full complement of memory—nearly 50% less than typical array-processing boards.

Operating systems supported include Unix, SunOS, VxWorks, OS-9, and Concurrent RTU. It's available in either 6 or 9U sizes and conforms to all Sun and VME mechanical requirements. External interface options include SCSI, 32-bit parallel, and custom daughtercard. The Warrior III is priced at $8225 in OEM quantities and is available in 60 days.

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**CIRCLE 92**

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**DESIGN**

8051 68HC11

THE LEADING IN-CIRCUIT EMULATOR TECHNOLOGY.

Nohau EMUL-PC, the PC based in-circuit emulators which find bugs other emulators can't.

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**CIRCLE 92**

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**E L E C T R O N I C**

**A U G U S T 9 , 1990**

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4096 PROCESSORS FILL ONE BOARD

Using just one 32-bit adapter slot, the Coherent Processor board gives an IBM Micro Channel workstation the power of 4096 parallel processors. The board possesses 16 processing elements, each of which contains 256 parallel processors. Content-addressable memory is used to search and operate on an entire table of data in parallel. The board is aided by a Development System that offers hardware and software support for writing, debugging, and running parallel application programs in C language. A compiler lets users create custom design routines. Typical applications are for speeding up databases, neural networks, or expert systems, or to work in a real-time environment such as local-area networks, radar, or process control. The Coherent Processor is available now for $19,500. In addition, a Sun-compatible board will be released later this year.

Coherent Research Inc., 1 Adler Dr., East Syracuse, NY 13057; (315) 433-1010.

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**CIRCLE 310**

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  - 18 to 36 VDC
- Outputs: 2-95 VDC

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For immediate delivery of converters or for additional information call VICOR EXPRESS today at 1-800-735-6200

Component Solutions For Your Power System

CIRCLE 93
In conjunction with the recent Microsoft Windows 3.0 release, Hewlett-Packard Co. announced version 3.0 of their NewWave software applications environment. NewWave, which runs on any 80286- or 80386-based PC running MS-DOS, integrates applications from many different software vendors. The list of independent software vendors porting their software to NewWave is an ever-growing one and now stands at more than 100.

New Wave offers a single, consistent user environment with icons to simplify use. Users aren’t forced to learn the workings of DOS or how to manage different files and programs. Version 3.0 of NewWave also includes an object-storage feature, which lets users share information on a network server by simply moving icons on the screen.

The user environment takes full advantage of all the new features added to Windows 3.0. These features include improvements to the memory management which lets NewWave run with 2 Mbytes of memory rather than 3 Mbytes. Windows also maximizes of the protected mode of 80286 and 80386 microprocessors to supply added memory for both the environment and the applications running on it. The MS-DOS Executive in the existing Windows programs are replaced with a Program Manager, a File Manager, and a Task List to supply a visual shell for completing directory, application, and file-management tasks. Color and design enhancements add to the polished user interface.

HP’s New Wave will be available in August for $195. Present users of NewWave can upgrade for $50. Windows 3.0 is available now for $150.

Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.

Microsoft Corp., One Microsoft Way, Redmond, WA 98052; (800) 323-3577.

Richard Nass
National’s family of CMOS op amps rises to a new all-time low: 40 femtoamps.

TAKING IT TO THE LIMITS WITH ULTRA-LOW INPUT BIAS CURRENT.

National’s new quad/dual CMOS op amps, the LMC660/662 and the LPC660/662, feature an extremely low input bias current of 40 fA typical. You can’t go much lower.

FEATURING RAIL-TO-RAIL OUTPUT SWING.

With a newly patented double feed-forward circuit architecture, National’s op amps provide an output swing that extends from one supply rail to the other. You can’t swing any more than that.

Use the LMC660/662 and LPC660/662 to drive rail-to-rail input A/Ds, or take advantage of the LMC’s fully specified 600 Ω load capability to process audio in telecom and cellular radio applications. Other typical applications include:

- Handheld meters
- Medical instrumentation
- Remote sensors
- Electrometers
- Spaceborne/Avionic subsystems

INPUT BIAS CURRENT VS. TEMPERATURE:

NATIONAL REDEFINES SINGLE-SUPPLY OPERATION.

In the past, a single supply op amp was an amplifier whose input common-mode range included ground. But in today’s +5V systems, you need op amps that take advantage of every last volt that the supply provides, and whose outputs swing fully from rail-to-rail. National was the first to deliver rail-to-rail performance with the LMC660 and now has a complete family—all in CMOS.

POWER UP WITH LOW POWER AND MICROPWR.

If you’re looking for low power, there’s the LMC660/662, which operate at 375 µA/amplifier. Or if your application calls for 40 µA/amplifier, we offer the LPC660/662, micropower versions of the popular LMC series. In either case, you get lower power dissipation and a longer lasting battery.

LMC660/LPC660 VS. THE COMPETITION

<table>
<thead>
<tr>
<th>Output Swing (V+ = 5V)</th>
<th>LMC660/1</th>
<th>LPC660/1</th>
<th>TLC274/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>V0.5 (max)</td>
<td>3mV</td>
<td>3mV</td>
<td>5mV</td>
</tr>
<tr>
<td>Ii (typ)</td>
<td>400A</td>
<td>400A</td>
<td>6000A</td>
</tr>
<tr>
<td>Supply Current (typ)</td>
<td>375µA/amp</td>
<td>40µA/amp</td>
<td>675µA/amp</td>
</tr>
</tbody>
</table>

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For more information on our new CMOS op amps and growing family of high-performance amplifiers, including VIP™ Bi-FET™ Super-Blocks™ and precision, call or write us today: 1-800-624-9613, Ext. 66. In Canada: 1-800-548-4529, Ext. 66. National Semiconductor Corporation, P.O. Box 7643, Mt. Prospect, IL 60056-7643. And find out how we can help take your designs to new heights.
Pass Data At 25 MHz With Bidirectional FIFO

Rather than use two memory blocks on the same chip to form a 2-kword-by-9-bit bidirectional first-in/first-out memory, the CY7C439 employs a lone 2-k-by-9 memory block and some on-chip control logic to move data. Furthermore, Cypress Semiconductor’s designers add two other data paths into the chip—a registered bypass mode and a transparent bypass mode. The registered mode acts like a 1-word-deep FIFO register in the reverse direction to the main FIFO buffer. It permits the sending system to transfer a 9-bit status word to the FIFO buffer’s write port. The transparent bypass feature allows a single 9-bit word to be immediately transferred in either direction, temporarily turning the chip into a 9-bit bidirectional buffer. With these modes, the chip can serve in applications such as a disk-drive buffer in which the transparent bypass mode allows the host to configure a ‘dumb’ peripheral while the registered bypass mode holds the status response from a data transfer.

Able to access in just 30 ns and operate with a 25-MHz cycle frequency, the bidirectional FIFO register’s transfer direction can be selected on a cycle-by-cycle basis. Indicator flag signals are available for conditions such as Empty/Full, and Half-Full.

Since only one memory block is required, the chip is small enough to squeeze into a 300-mil-wide DIP or small-outline J-leaded package. In 100-unit quantities the chip sells for $33.15. Samples are available from stock.

Cypress Semiconductor Corp., 3901 N. First Street, San Jose, CA 95134; Bill Eichen (408) 943-2600

Dave Burksy

Wide-Input PLDs Decode Addresses Fast

Designed specifically for address decoding, a very-wide-input decoder packs 36 input lines, 10 dedicated output lines and 12 additional programmable I/O lines. Fabricated in an advanced bipolar process the PHD48N22-7 can decode up to a 48-bit bus pattern (by using the 12 I/O lines as additional inputs) in just 7.5 ns from input to output (through the AND logic), making the chip the fastest wide decoder available from any company. Four of the 12 bidirectional I/O lines also serve as OR logic outputs, and three of those four provide 7 product terms; the fourth line has a slightly longer propagation delay—8 ns. The wide decoder is available in production quantities, and the plastic-housed leaded-chip carrier version sells for $22 in 1000-unit lots.

Philips-Signetics Corp., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088; Paul Sasaki, (408) 991-2000.
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You know that a front-panel display is the first thing your customers will notice about your product. You need something to set your product apart from the competition, but you've got tight budget and packaging constraints. Now, IEE has a new family of brilliant answers!

You can have the outstanding appearance of a vacuum fluorescent display at an affordable price, with IEE's latest generation of enhanced "Ninety Series No-Frills" FLIP™ VFD modules.

Price isn't the only thing that's unusually trim. Surface mount technology makes these modules exceptionally compact. Other features include:

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Call or write today and tell us your problems. We offer a wide variety of display technologies; what you see here are just a few of the answers we can give you.

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(818) 787-0311, ext. 418
9600-BIT/S MODULE EASES MODEM DESIGN

Offering full-duplex operation at 9600 bits/s, the CH1790 modem module provides full V.32 compatibility. It has fallback and compatibility with 4800-, 2400-, 1200-, 300- and 110-bit/s rates and meets CCITT V.32, V.22 bis, V.22, V.21, and Bell 212A and 103 standards. Able to respond to the full Hayes "AT" command set, the modem can be controlled by a wide variety of available data-communication packages. Features include automatic answer, automatic speed and parity adjustment, and call-progress tone detection. Trellis forward error correction is used at 9600 bits/s along with MNP Level 4 error control. A built-in RS-232 (5-V) serial interface allows the host to communicate with the module. An evaluation test system that contains the modem, DAA and other hardware to run the module through its paces is also available—the CSP9696A. In small quantities, a full-featured V.32 modem, sells for less than $500.

Cermetek Microelectronics Inc., 1308 Borregas Ave., Sunnyvale, CA 94088-3565; Thomas Newton, (408) 752-5000. 

CIRCLE 316

FAX MODEM CHIP TARGETS PORTABLE APPLICATIONS

Features added to the YM7109 fax modem IC qualifies the device for portable and remote applications. The new chip, the YM7109E, combines the capabilities of the earlier version with error correction for Group 3 fax, HDLC framing including bit stuffing, bit stripping, and CRC calculations, a UART for Bell 103 transmission, and an external clock synchronous mode for cellular phone and remote fax applications using radio transmission or satellite communications. Also on the chip are serial and parallel ports, a scrambler and descrambler, a programmable touch-tone generator and detector, and a programmable tone-detector for non-DTMF tones.

On-chip data converters have a 9.6-K samples/s sampling rate with a 12-bit resolution for voice recording and playback. The chip complies with standard half-duplex synchronous CCITT V.29 at 9600/7200 bps and V.27ter at 4800/2400 bps; synchronous CCITT V.21 half- and full-duplex at 300 bps; and full-duplex asynchronous Bell 103. The CMOS chip comes in a 40-pin DIP, a 64-pin quad flatpack, or a 68-pin PLCC. Pricing is $35 each in quantities of 10,000. Samples are available now, and production quantities are coming in November.

Yamaha Corp. of America, 981 Ridder Park Dr., San Jose, CA 95131; Robert Starr, (408) 437-3133. 

CIRCLE 317

CUT FREQUENCY HIGHS DOWN TO SIZE

Micro/Q 3000 Controls High Frequency Noise From ASICS

Design PGA packaged ASICS or MPUs into your board design and the noise level starts climbing. Surround these PGAs with standard 2 pin decoupling capacitors, and you’ll use valuable board space and provide inferior decoupling. Micro/Q 3000 decoupling capacitors from Rogers provide excellent noise suppression over a wide frequency range. For space savings, they’re specifically designed to fit under PGA devices such as fully custom ASICs, MPUs and gate arrays - where low noise and high density are essential.

Featuring the high performance reliability you’ve come to expect from Rogers, this family of very low inductance decoupling capacitors is through-hole mounted under pin grid arrays, PGA sockets, and PLCCs/LCCs mounted in sockets. They are available for all PGAs in a variety of sizes and dielectrics, including X7R and P3J dielectrics for greater temperature stability.

Micro/Q 3000 capacitors. Excellent noise suppression for high performance.

Write or call for free literature and product samples.

Micro/Q 3000 capacitors fit under PGA packaged ASICS and MPUs.

Also available through Mektron Europe, Ghent, Belgium and Rogers Inoue Corp., Nagoya, Japan. Micro/Q is a registered trademark of Rogers Corporation.

CIRCLE 102
THE ROAD TO INNOVATIVE SOLUTIONS

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CONTROLLERS BOOST SERIAL COMMUNICATIONS PERFORMANCE

Two CMOS serial communications controllers from Zilog Corp. simplify system design by integrating functions previously performed by discrete devices.

The ZS5130 enhanced serial communications controller (ESCC) is a dual-channel, full-duplex multiprotocol controller with each channel containing a crystal oscillator, baud-rate generator, and digital phase-locked loop. The ESCC also includes an 8-byte-deep receive FIFO buffer and a 4-byte-deep transmit FIFO buffer for reducing data overruns, interrupts, and host CPU overhead by accumulating byte strings. The programmable FIFO and DMA request levels allow the user to select packet-handling response. SDLC protocol enhancements offload the CPU with automatic handling of frame conditions.

The ZS5C80 serial communications and small computer interface (SCSCI) combines Zilog’s ZS5C80 10-MHz serial communications controller (SCC) and the 3-Mbyte/s ZS3C80 small computer system interface (SCSI). Both functions share an 8-bit address and data bus for use in any system having a SCSI interface defined by the X3.131-1986 standard. The SCSCI has all features required to build a network using a typical disk-based file server, including an interface to multiplexed or non-multiplexed CPUs, programmable channels for asynchronous or synchronous datacom protocol, and a 10-by-19-bit FIFO buffer and 14-bit byte counter that support high-speed SDLC transfers using DMA controllers.

Packaged in a 40-pin DIP and 44-pin PLCC, the ZS5130 16-MHz version costs $13.65 in 1000-piece quantities. The 10-MHz part costs $8.85. Packaged in a 68-pin PLCC, the ZS5C80 costs $12.45 each in 1000-piece quantities.

Zilog Corp., 210 Hacienda Ave., Campbell, CA 95008; Mike Huime, (408) 370-8000. CIRCLE 339

DAA MODULE TACKLES HIGH-SPEED MODEMS

Designed specifically to improve the performance of high-speed modems, the CH1832 data access arrangement mates directly to V.32, V.33 and V.29 type modems. The DAA passes voice and data at speeds starting at 300 bps and up to 38.4 kbps. High-voltage isolation and surge protection up to 1000 V are built into the DAA. System features include ringing detection, hook-switch control, billing delay, and provisions for 2-wire or 4-wire leased-line operation. A 2-wire-to-4-wire converter is included in the 2.2-by-3.25-by-0.65-in. module. The DAA module is also pre-registered for FCC part 68, thus reducing the waiting time needed by a system that must obtain part 68 approval.

Cermetek Microelectronics Inc., 1308 Borregas Ave., Sunnyvale, CA 94088-3565; Thomas Newton, (408) 752-5000. CIRCLE 342

9600-BPS V.22 BIS-COMPATIBLE MODEM TRIMS PRICE, NOT FEATURES

Able to operate at 9600 bits/s in a full-duplex mode, the 9624 modem series employs a custom chip set developed by Sharp to achieve CCITT V.22 bis compatibility. The custom chips allow the company to incorporate MNP5 error correction as well as the company’s own extended-baud-rate technology, which, together, permit a 2400-bit/s chip set to provide 9600-bit/s full-duplex asynchronous operation, as well as standard 2400-, 1200-, and 300-bit/s data modes. (To achieve the 9600-bits/s rate, a pair of

BOARDS PUT MACINTOSH ON ARCNET LANS

A line of board-level products enables Macintosh SE and Macintosh II computers to join an ARCNET local area network, the environment typically used for networking IBM PCs and compatibles. The Macintosh-on-ARCNET family allows the use of PC-type file servers and printers, eliminates the need for a dedicated Macintosh server, and enables Macs to share data among themselves without additional networking accommodations or cable. Furthermore, networks can employ coaxial cabling, twisted-pair wiring, or a mix of the two in in star, bus, or daisy-chain topologies. Hardware consists of a controller board and a transceiver board for the MAC SE, while the MAC II requires only one board. To accommodate the various topologies and cabling systems, four versions are available. For the MAC SE, the SE100 supports coax star topology and the SE250 handles twisted-pair star and daisy-chain topologies. For the Macintosh II, the NB210 supports coax star and bus topologies, while the NB250 is for twisted-pair star and daisy-chain topologies. The SE100 and SE250 sell for $495 each; the NB210 and NB250 cost $545 each.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11788; (516) 273-3100. CIRCLE 241

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SPAN DESIGN CYCLE

The Cadence Microwave Musician design tools carry engineers from schematic capture through physical layout in one integrated package. The system offers front-to-back design capability for both monolithic microwave ICs and hybrid devices. Users can produce hierarchical schematics using a library of ideal components and a library of foundry components. In addition, the package supports multiple simulation runs at the same time. The Musician front end, which consists of schematic transferred through a system manager to the manufacturer's design and compilation software. Each system is tailored to the needs of the manufacturer by controlling libraries, hierarchies, drawing sizes, and output forms. The Schema-Quik package includes software, reference manual, and tutorial, and is upgradable to the Schema III package. The product is shipping now for $899.

Omnation Inc., 801 Presidential Dr., Richardson, TX 75081; (800) 553-9119. CIRCLE 330

RENEW SUSIE SIMULATOR RUNS
30 TIMES FASTER

The newest version of the popular Susie logic simulator from Aldec Co. is not only up to 30 times faster than the previous version, but also supports VHDL IC models and easy-to-use windowing. Susie 6.0 achieves the speed gain with a new event-driven algorithm and by taking advantage of 32-bit direct addressing on 80386- and 80486-based computers. In addition, the simulator runs from mouse-driven pop-up menus.

Version 6.0 gives users the same real-time operation they are used to, but adds high-speed simulation of VHDL IC models. Users can toggle switches, move jumpers, change propagation delays of any IC, modify Jedeec and hex files, and then instantly simulate the new design without visible compilation. Users can also perform instant simulation of selected design areas, which can speed the simulation process by 10 to 100 times.

Also, Aldec's VHDL IC timing model builder, Mobic/T, is a high-level modeling language designed specifically for Susie. It generates IC timing models with 11 input states and 15 output states, and includes predefined functions for modeling memories and PLDs. Susie 6.0 comes with TTL VHDL libraries. There are over 6000 parts available in Aldec's optional libraries.

Susie 6.0 is available now for $5995. The Mobie/T IC-model builder is $1995, and the optional libraries start at $795.

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Engineers can have a schematic-capture system for less than $100 with Omnation Inc.'s Schema-Quik software, a low-cost version of the company's Schema III software. The package is aimed at PLD manufacturers as an alternative to data entry with logic equations, truth tables, or state machines.

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CIRCLE 90
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*C86 is a trademark of Intel Corp.
RUGGED ON-LINE UPS SYSTEM CAN HANDLE BROAD INPUT

Aimed at military and hostile industrial applications is an online ruggedized UPS from Transistor Devices Inc. The MIL-UPS combines the company’s BCE battery charger/power supply with its ACE sine-wave inverter.

The BCE module’s wide input range of 90 to 250 V from 40 to 440 Hz, as well as its high power factor, provide immunity to ac-input-voltage fluctuations. The system can handle a broad range of line disturbances such as extended-brownout conditions as low as 83 V, and frequency disturbances from 40 to 440 Hz, without battery power. It’s suited for remote site locations where generator fluctuations and low-power-factor loads can be too much of a burden for other UPS systems. Thanks to its universal-input feature, the system can function as a frequency changer and voltage conditioner between American, European, and special military power applications.

The charger/power module also features a battery-equalizer function, which optimizes battery-cell potentials and extends battery life. To prevent too many repetitive equalizing cycles, the function is automatically locked out at the end of each equalizing cycle. In addition, the BCE module has a reduced-voltage mode that prevents the batteries from heating excessively during a rapid recharge cycle.

From the sine-wave-inverter module, a true sine wave is generated with less than 1% total harmonic distortion. The module’s fixed-frequency output is crystal-controlled to better than 0.1% stability. The zero-lea-to-zero-lag load power factor of the system’s inverter easily drives unfriendly, non-linear load types such as motors and rectifier loads.

A 2-kVA system occupies only 12 in. of height in a 19-in. rack. Without batteries, the system weighs under 65 lbs. Such a system goes for about $10,000 without batteries.

Transistor Devices Inc., 85 Horsehill Rd., Cedar Knolls, NJ 07927; (201) 267-1900. Circle 327

DAVID MALINIUK

CONVERTER AND FILTER TANDEM NEAR MIL-STD-883C APPROVAL

With final process certification near, a combination of a dc-dc converter and EMI filter will soon pass the last hurdles to full compliance with MIL-STD-883C, method 5008. Interpoint’s MHF converter and matching FMC-461 EMI filters give military designers the reliability of components that have passed test conditions applied to mission-critical components.

The 883C versions of the converters and filters have dramatically increased tolerance to temperature extremes and acceleration. That’s achieved by using higher switching frequencies to reduce the magnetic’s mass and by redesigning the platforms the magnetics are attached to.

Input range for the 883C-qualified converter is 16 to 40 V dc. It produces closely regulated outputs of 5, ±12, or ±15 V dc in single or dual configurations up to a maximum output of 12 W. The operating temperature is from −55 to +125°C. The package is a low-profile (0.525 in.) hermetically sealed, gold-plated steel case that takes up just 1.6 square inches of board area. Power density for the device, which switches constantly at 600 kHz, is 30 W per cubic inch. The matching FMC-461 EMI filter reduces the converter’s reflected input-ripple current to meet MIL-STD-461B CE03 standards.

Pricing for the MHF converter is $780 in quantities of 100. In similar quantities, the FMC-461 EMI filter goes for $365. Pending qualification testing for the company’s process, the MIL-STD-883C-compliant devices will be available this fall.

Interpoint Corp., Box 97005, Redmond, WA 98073-9705; (206) 892-3700. Circle 328

DAVID MALINIUK

CONTROL 400 V AT 1 A WITH 5-V LOGIC

The PWR-NCH201 IC can control solenoids, lamps, relays, and small motors with 5-V logic while powered directly from the rectified 115-V ac line. Packaged in a 16-pin “batwing” DIP, it contains a monolithic pair of MOSFETs rated at 400 V and 675 mA each. On-resistance of each is just 5 Ω. Another version, the PWR-NCH401, holds four smaller FETs with a similar voltage rating; but with a current rating and on-resistance of 335 mA and 10 Ω, respectively. It is in a 24-pin skinny DIP.

With both FETs in parallel, the 201 handles up to 1 A; with all four FETs in parallel, the 401 handles up to 675 mA. Unlike other high-voltage MOSFETs, these turn on hard with just 5 V between gate and source, permitting logic-level control. The devices are current-sensing, or mirror FETs. Each has a separate source output-pin that provides a scaled current equal to approximately 1/1500 of the FET’s current. Versions rated at 200 and 400 V are also available. Pricing in hundreds ranges from $2.60 to $5.84.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Doyle Slack, (415) 960-3572. Circle 324

REGULATOR IC SENSES VOLTAGE AT LOAD

A low-dropout linear regulator, the LT1087, offers both adjustable output voltage and 4-wire Kelvin sensing of the voltage across the load. The chip is rated at 5 A and regulates down to an input-to-output voltage of just 1.5 V maximum at 5 A. The 4-wire remote sensing feature eliminates load-regulation errors caused by voltage drops in the hot side of the line to the load and in the ground return. The feature is particularly important where sensitive circuitry, such as wide-band op amps operating at high gain, must be isolated from heat or noise generated by power supplies; in most regulators today the output voltage is sensed inside the package. The chip’s reference voltage is trimmed to 1% and the current limit is trimmed as well. This precision current limit minimizes stress on both the regulator and the power-source circuitry when the circuit is overloaded. The LT1087 comes in 4-pin TO-3 metal cans and 5-pin TO-220 packages. In quantities of 100 pricing for the latter runs $4.45.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott (408) 432-1900. Circle 329
**HIGH-RESOLUTION LCD MODULE MAKES GRADE FOR LAPTOP PCS**

A thin plastic film is used in the EG9007 LCD graphics-display panel to achieve a high-contrast black-and-white display that's well suited for notebook-and-laptop-PC applications. With its depth of just 0.33 in., the display offers the LCD market's thinnest profile, according to Epson OEM.

Epson's use of its newest formulated twisted-nematic technology in the EG9007 display results in a lighter, thinner module as well as lower manufacturing costs. The single-layer LCD also enabled the company to use edge lighting for the display, which further contributes to its thin profile.

Also featured in the 10- by-6.25-in., 1.5-in. display is a chip-enable transmission system that significantly reduces power consumption. Thanks to Epson's chip-on-flex technology, the display's drivers are mounted on a flexible printed-circuit board that is lighter and more compact than traditional rigid printed-circuit boards. The display, which weighs a scant 1.5 lbs, produces white characters on a black background with a resolution of 640 by 480 dots and a 1/242 multiplex ratio.

The EG9007 display also offers a faster fluid response time (120-ms turn-on at 25°C) than competitive displays. This translates into faster animation of text and graphic images. A cold-cathode fluorescent backlight provides illumination of the display.

In quantities of 100, the EG9007 display costs $285. It is available now in OEM quantities.

Epson OEM Division, Epson America Inc., 3145 Kashiwa St., Torrance, CA 90505; (213) 534-4500.

--- CIRCLE 326

**SLIDE-BASED LED REPLACES BULBS**

Slide-based incandescent lamps can be directly replaced with a high-intensity packaged-LED device. The 5SBF multi-LED device uses six discrete chips and boasts a lifetime of 100,000 hours. The incandescent pilot light it replaces, the 120PSB, lasts only 7500 hours. That suits the LED to tasks with high vibration. The LED device draws 7 mA at 120 V and comes in seven colors with peak wavelengths ranging from 555 to 660 nm. Pricing starts at $3.56 for lots of 1000 with availability in six weeks after receipt of order.

Data Display Products, 445 S. Douglas St., El Segundo, CA 90245-4630; (213) 640-0442.

--- CIRCLE 328

**TINY SURGE KILLERS SUIT AUTO TASKS**

A cost-effective and reliable alternative to Zener diodes for transient-voltage suppression in automotive applications has arrived. The V24ML series of semiconducting ceramics come in leadless chip form and are fabricated to absorb internally or externally generated surges that might otherwise damage or destroy a car's electronic components. The surface-mounted devices have no lead inductance and therefore act faster. The series is rated for peak currents up to 2000 A and comes in 1206, 1210, 2220, and 2820 sizes. Samples of the V24ML1220 are available now and production lots will be available in August. In lots of 1000, the device costs $0.46.

Harris Semiconductor, Box 883, Melbourne, FL 32901; (800) 442-7747.

--- CIRCLE 327

**10-IN. COLOR LCD HITS PRODUCTION**

Higher resolution, contrast, and brightness than the company's earlier color-TFT LCDs is offered in Hitachi's TM26D01VC 10-in. display, which is now in production. The direct-view display offers 640-by-480-pixel resolution and eight colors. When used with third-party gray-scale controllers, the number of colors can increase to 256. Contrast ratio is 100:1 and the display's brightness level is 80 NT, which meets or exceeds the brightness of CRTs. Response is quick enough for real-time monitoring applications. The display's wide viewing angles suit it to use in medical instruments. Production units are available now with samples priced at $3500 each. Initial production pricing is less than $200 per unit.


--- CIRCLE 328

**TO-254 HEATER REGULATES TEMPERATURE**

Hermetically sealed in a TO-254 package, the DN-501 is the first in a series of proportionally controlled heaters whose temperature can be programmed between 50°C and 100°C by one external resistor. What's more, it can deliver up to 28 W of power from an unregulated supply. The subminiature device, which operates from -55°C to +100°C, can be used for regulating the temperature of sensitive electronic components, such as crystal oscillators and microwave filters. It features 28-V operation and is electrically isolated from the case. The part can also be customized to meet specific application requirements.

Daum Electronics Inc., 2049 California St., Suite 2, Carson City, NV 89701; (702) 882-7721.

--- CIRCLE 317

**5-IN. COOLING FAN BOOSTS AIR FLOW**

Air flow that's improved by up to 50% while reducing noise by 50% compared with 4.7-in. fans is featured in the Galaxy 5-in. fan. The 1.5-in.-deep unit delivers air-flow levels of 150, 125, and 110 cfm at 12, 24, and 48 V. Comair Rotron's ThermaPro-V circuitry provides programmability, voltage regulation, and thermal speed control. Other features include electronic locked-rotor protection with automatic restart. The fan costs from $18 to $20 in OEM quantities. Samples are available now and production lots will ship in late August.

Comair Rotron, North St., Saugerties, NY 12477; (914) 246-3615.

--- CIRCLE 337
PHYSICAL-VAPOR-DEPOSITION SYSTEM BOASTS HIGH VACUUM FOR PURER FILMS

An ultra-high vacuum level (10^-9 torr base pressure) in the process chamber of Applied Materials' Endura 5500 physical-vapor-deposition (PVD) system is the key to purer aluminum-alloy and barrier-metal films for advanced IC metallizations. Besides higher purity, films produced with the system also exhibit a nine-fold improvement in resistance to aluminum electromigration.

By building on the company's experience in chemical-vapor deposition, the PVD system is designed to give exceptional step coverage and step-coverage symmetry—even in high-aspect-ratio, sub-micron features over wafers up to 200 mm. A down-sputtering source design uses rotating permanent magnets to give complete surface target erosion, with no adjustment needed in process parameters over the life of the target. The result is better uniformity and step-coverage symmetry.

A low-voltage precleaning chamber, which is part of the mainframe unit, conditions each wafer before metal deposition. This yields maximum wafer-surface cleanliness with no damage.

Base pricing for the Endura 5500 PVD system starts at under $2 million. The first system was shipped in April.

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POWER CONNECTOR HAS SECONDARY LOCKS

The Mini-Fit TPA power connector incorporates secondary locks in the form of red-colored keys that are inserted into the housings, ensuring that the terminals within are correctly and permanently sealed. The connector is particularly useful in wire-harness applications, where wires and connectors are often abused during manufacture.

The red secondary locking keys cannot be inserted unless the terminals are properly inserted, fully seated, and locked in the housings. An optional lock—a redundant, independent secondary housing lock—is applied after the connectors are mated. The Mini-Fit TPA can handle up to 9 A per circuit, at 250 V depending on circuit size. The centerline between contacts is 0.165 in. and from row to row is 0.217 in. The envelope size of a mated pair of wire-to-wire connectors is 1.36 in. Typical pricing for a 10-circuit housing is $0.06 per mated line (production quantities). Lead time is four to six weeks.

FIBERGLASS WEBS PROVIDE INSULATION

Craneglas fiberglass webs offer thermal and electrical insulation for a wide range of industrial, commercial, and consumer applications. When laminated with dielectric films and papers, as well as woven fabrics, they offer unique advantages as electrical tapes, wire and cable coatings, gaskets, flame retardants, and thermal-insulation materials. Combining Craneglas with foil results in an excellent heat-shield material. Non-wicking and abrasion-resistant treatments are also available. As a carrier for thermosetting electrical insulating resin systems, Craneglas webs are a low-cost means of insulating motors, generators, transformers, and reactors. They are also a cost-effective alternative as a core material for composite laminates in printed circuit boards. Craneglas is offered in a range of thicknesses from 5 to 120 mils (0.005 to 0.120 in.). Call for pricing and availability.

Electrolock Inc., P.O. Box 368, 16838 Park Circle Dr., Chagrin Falls, OH 44022; (216) 543-6626.

Fiberglass webs are a low-cost means of insulating wires and cables. They provide thermal and electrical insulation for a wide range of applications.

Craneglas fiberglass webs offer thermal and electrical insulation for a wide range of industrial, commercial, and consumer applications. When laminated with dielectric films and papers, as well as woven fabrics, they offer unique advantages as electrical tapes, wire and cable coatings, gaskets, flame retardants, and thermal-insulation materials. Combining Craneglas with foil results in an excellent heat-shield material. Non-wicking and abrasion-resistant treatments are also available. As a carrier for thermosetting electrical insulating resin systems, Craneglas webs are a low-cost means of insulating motors, generators, transformers, and reactors. They are also a cost-effective alternative as a core material for composite laminates in printed circuit boards. Craneglas is offered in a range of thicknesses from 5 to 120 mils (0.005 to 0.120 in.). Call for pricing and availability.

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Rene Oliver says he's got the best of both worlds. He's a tax accountant who works out of his home so he can be there for his two-year-old daughter Windy. "As a father, I'm concerned about being able to afford Windy's college," he says. "But as an accountant, I know the best way to save." Rene recommends U.S. Savings Bonds, the Great American Investment. "If you buy Bonds when your children are young, you'll be ready," he says. Today's Bonds pay competitive rates, and now can be completely tax free when used for education. To find out more, call 1-800-US-BONDS.
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SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TOSW-230 ZFSW-230DR</th>
<th>TOSW-425 ZFSW-425DR</th>
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<tbody>
<tr>
<td>Freq. Range (MHz)</td>
<td>10-3000</td>
<td>10-2500</td>
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<tr>
<td>Insert Loss (dB)</td>
<td>typ: 1.3, max: 1.9</td>
<td>typ: 1.1, max: 1.7</td>
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<tr>
<td>Isolation (dB)</td>
<td>typ: 60, min: 40</td>
<td>typ: 60, min: 40</td>
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<tr>
<td>1dB Compression (dBm)</td>
<td>typ: 17, min: 6</td>
<td>typ: 17, min: 6</td>
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<tr>
<td>VSWR (ON)</td>
<td>typ: 1.3, max: 1.6</td>
<td>typ: 1.3, max: 1.6</td>
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<tr>
<td>Switching Time (µsec)</td>
<td>typ: 2.0, max: 4.0</td>
<td>typ: 2.0, max: 4.0</td>
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<td>Oper. Temp (°C)</td>
<td>-55 to +100</td>
<td>-55 to +100</td>
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<td>Stor. Temp (°C)</td>
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<td>-55 to +100</td>
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<tr>
<td>Price (1-24)</td>
<td>$39.95</td>
<td>$89.95</td>
</tr>
<tr>
<td>Price (1-9)</td>
<td>$59.95</td>
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