Semi memories are exploding with "moire" bits per chip than ever before. Access time, power and prices are dropping and new technologies are emerging. But beware—don't see something that isn't there. All those parameters can play tricks on the senses and your "second source" may turn into a phantom. Page 56.
Your alternative to lower performance controls and higher cost precisions.

LASER-TRIMMED SAVINGS
Now, for about $2*, the Bourns® Model 87/88 semi-precision, single-turn potentiometer delivers ±2% zero-based linearity. Compare the accuracy to the $5 precision pot with ±1% independent linearity that you’re buying now... especially the performance at the low end setting, where dial setting accuracy is most critical. Laser trimming and advanced element design* deliver performance and savings in a ¾” square modular package.

MOVE UP FROM INDUSTRIAL GRADE CONTROLS
Again, for about $2, the Model 87/88 offers 200-300% greater panel setting accuracy over industrial grade controls. They’re perfect for applications requiring close, consistent calibration of output-to-panel setting and versatility of design.

MODEL 87/88 — THE ALTERNATIVE
Don’t compromise your application with lower performance controls or pay a premium for precision pots. Specify the alternative — Bourns Model 87/88. Write or call today for complete technical information.

$2 SEMI-PRECISION MODULAR POTS . . . BEAUTIFUL!

* Production quantities, Domestic U.S.A. price, Single cup unit only. 
©Pending Patent

For Future Application — Circle 230

For Immediate Application — Circle 130

TRIMPOT PRODUCTS DIVISION, BOURNS, INC., 1200 Columbia Avenue, Riverside, California 92507, Telephone (714) 781-5122 — TWX 910 332-1252.
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And, since they’re end or side stackable, they’re ideal for flush mounted panel indicators, backlighting legends, and linear arrays. Plus you get long life and solid state reliability. And they’re in stock right now. Choose our 5082-4570 for yellow, the 5082-4670 for high efficiency red, or the 5082-4970 for green. Priced at $1.00* in quantities of 1000. *U.S. Domestic prices only

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In Canada, contact Schweber Electronics or Zentronics, Ltd.
MIL-SSR UPDATE

Ready for military service:
Our new AC power SSR.

Commercial relays are no match for severe military or aerospace environments. But there's no doubt about our new 652 Series. Designed expressly for military and aerospace applications, this new AC SSR is packaged in a rugged, hermetically sealed aluminum case with the internal circuit assembly encapsulated to resist shock and vibration. What's more, all circuit components are military grade including the inverse parallel SCRs that provide reliable output switching — up to 25 Amps — over the frequency range of 45-440Hz.

Other features include logic compatible input drive circuitry, optical isolation, and zero voltage turn-on to reduce EMI.

To top it all off, our 652 Series is designed to meet MIL-R-28750 and all categories of MIL-STD-704A, with an operating ambient temperature range of -55 °C to +110 °C.

For complete specification data, contact your nearest Teledyne Relays sales office listed in EEM, Gold Book and Electronics Buyers' Guide. You'll find we have the experience, products, and technical support to meet all your SSR needs — including a quick reaction capability to design SSRs specifically for your application.

TELEDYNE'S MILITARY SSRS

A. P/N 683-1 DC SSR  
   DIP package, with output rated at 600mA/50VDC

B. P/N JM640-1 Bi-polar SSR  
   Mil P/N M28750/5, TO-5 package, with bi-polar (AC/DC) output rated at 60mA/40V

C. P/N JM643-1 DC SSR  
   Mil P/N M28750/6, TO-5 package, with output rated at 300mA/40VDC

D. P/N JM643-2 DC SSR  
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E. 652 Series AC Power SSR  
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TECHNOLOGY
56 FOCUS on semiconductor memories: Second-sourced devices may provide a false sense of security. Supposedly identical memories may not be. Caution is necessary with specs marked "typical."

66 Memory Technology: Part 1. Standards for dynamic MOS RAMs are emerging. But among equivalent parts, some are more equal than others.

72 Model RAMs automatically for gate-level logic simulators with RAMGEN. Such a model lets you develop test programs for complex PC boards with ease.

78 Predict a 4-k RAM's average lDD with a few simple calculations. The method accounts for both the transient and steady-state components.

82 Microprocessor Basics: Part 18. Cut your processor's computation time by storing information in tables. Accessing a table can take less time than doing an algorithm.

92 Simplify analog/computer interfacing. Choose the data-acquisition configuration that's best for your system, then use the right analog-to-digital converter.

102 Ideas for Design: Control the speed and phase of a dc motor by comparison. Get 32 times the bit rate instead of 16 from a programmable baud generator. Logic interfacing circuit translates many levels to TTL regardless of polarity. Float charger independently recharges two lead-acid cells connected in series.

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Cover: Photo of a 4-inch, 4-kbit, static-RAM wafer by Frank Saude, courtesy of Advanced Micro Devices.
How to do three things at the same part:
If you want a great 8-bit D-type register with common clear, get our Am25LS273. If you want one with three-state outputs, get our terrific Am25LS374. If you're looking for a sensational common enable, you want our Am25LS377. However, if you'd be willing to settle for all three, read on.


And all that really means is that next time you're thinking about registers, low-power Schottky and TI, you should also be thinking about AMD. Or calling. Or writing. (After all, where else can you do three things at the same part?)

Advanced Micro Devices
Bipolar LSI. N-channel, silicon gate MOS. Low-power Schottky. Multiple technologies. One product: excellence.

CIRCLE NUMBER 19
TAKE THE GAMBLE OUT OF SPECIFYING POWER SUPPLIES

When you specify power supplies manufactured by Abbott Transistor Laboratories, you minimize your risks and maximize your return.

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No "BOX CARS" either — Abbott units are compact

Don't go the "HARD WAY," specify Abbott, the easy way to solve your power supply requirements

Abbott makes a wide variety of industrial/commercial, OEM, military and aerospace power supplies. Each and every unit is subjected to rigorous quality control and electrical testing before shipment to insure that when you put it on the line, it will pass every time.

So when you want a reliable power supply, come to Abbott, the winner for price and performance.

Please see pages 1836-1848 of your 1976-77 EEM (ELECTRONIC ENGINEERS MASTER Catalog) or pages 672-682 Volume 2 of your 1976-77 GOLD BOOK for information on Abbott Modules.

Send for our new 60 page FREE catalog.
Across the desk

Slow-down circuit can cause problems

In the Idea for Design, "Digital-Integrator for Intrusion Systems" (ED No. 5, March 1, 1977, p. 74) author Gross' slow-down circuit at pins 1 and 9 of the 4015A dual 4-bit register can be troublesome for two reasons:
1. If the comparator output "bounces," the clock signal could hover close to its transition level, and thus defeat the 15-µs transition spec for the 4015A.
2. The circuit increases the power-supply noise susceptibility.

My solution: Use an MC14015B with a dc clock circuit and insert a hysteresis slow-down circuit having a fast transition time (see figure).

A. Frisch
VP, Engineering
Zygo Industries Inc.
P.O. Box 1008
Portland, OR 97207

The author agrees, but...

The circuit shown in my article works. However, should it not function properly because the clock signal "hover" or because of power-supply noise, the failure is safe. We agree with reader Frisch that his proposed circuit is an improvement, which we and other readers should use when cost considerations allow.

Thomas B. Gross
T. A. O. Gross & Associates
Lincoln, MA 01773

Audio-amplifier delivers regulated dc power

Some of your readers may have a need for a continuously adjustable, regulated, bipolar dc power supply that can deliver 20 A at 100 V. We recently had a requirement for just such a device to drive the highly inductive field coil in a homopolar generator. After a lengthy search, we decided to use a Model M-600 audio amplifier manufactured by Crown International, Inc., of Elkhart, IN.

This amplifier can deliver the required dc power continuously. By simply adding an SPDT switch, a pair of 1960-Ω resistors and a 2-kΩ, 10-turn pot to the front panel plug-in circuit board, one obtains a completely self-contained, well regulated power supply at a fraction of the cost of the nearest commercial equivalent.

Gilbert A. Miranda
University of California
Los Alamos Scientific Laboratory
P.O. Box 1663
Los Alamos, NM 87545

Misplaced Caption Dept.

Actually, the floppy disc concept isn't all that new.


(continued on page 10)
Our 2114 has already become the most widely second-sourced 4K static RAM for the same reason Intel’s 2102A is the industry standard 1K static RAM. The 2114 simplifies system design, like the 2102A, and provides the highest possible density and modularity in static memories.

The 2114 is the first of several new generation Intel static 4K RAMs. We are now delivering both the standard 2114 series and the low-power 2114L series in production volumes. The 2114L is just as fast as the 2114 but consumes 30 percent less power. We will soon be shipping the 2142 to designers who want an extra chip select and output disable control inputs. Next, we’ll add the super high-speed 2147.

This new generation assures a continuing reduction in static RAM costs. We fabricate the 4K chips with an evolution of our 2102A technology. At 181 mils square area, the 2114/2114L packs four times the bits in only twice the silicon area. The chips fit into standard 18-pin plastic or ceramic packages, keeping volume production costs low.

Our 4K RAMs also inherit the 2102A’s ease of use and low overhead. You don’t need a clock, address setup timing, or refreshing. You don’t even need pullup resistors or output gating. These RAMs operate at TTL levels on a single

+5v supply and have buffered, three-state outputs. We guarantee identical access and cycle times, so you can surpass the performance of clocked RAMs. For instance, you can achieve a data rate of 20 million bits a second with our 200-nanosecond parts. That’s up to twice the rate of clocked RAMs with 200-ns access time. Intel specs also guarantee that even at such high throughput you’ll need only 25 to 50 percent of the power of first-generation static RAMs.
4K static RAM family.

As for board density, look at the pinouts. The 18-pin 2114/2114L configuration provides the highest density possible in 4K static RAMs.

Our 20-pin 2142 adds a second chip select—so you can go to 4K without external decoders—and an output disable for direct control of the output buffers. And since it is a simple modification of the 2114, it promises similar production economies.

You can minimize package count at any number of kilobytes since these new RAMs store 1Kx4 bits. With our compatible 256x4-bit static RAMs, you now have the widest range of modular design options. They are all listed in our new Static RAM Family Album.

<table>
<thead>
<tr>
<th>Intel’s 4K Static RAMs</th>
<th>Access Time (max)</th>
<th>Cycle Time (min)</th>
<th>$I_{CC}$ (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1K x 4</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>2114-2</td>
<td>200 ns</td>
<td></td>
<td>100 mA</td>
</tr>
<tr>
<td>2114L2</td>
<td></td>
<td></td>
<td>70 mA</td>
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<tr>
<td>2142-2</td>
<td></td>
<td></td>
<td>100 mA</td>
</tr>
<tr>
<td>2114-3</td>
<td>300 ns</td>
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<td>100 mA</td>
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<tr>
<td>2114L3</td>
<td></td>
<td></td>
<td>70 mA</td>
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<td>2142-3</td>
<td></td>
<td></td>
<td>100 mA</td>
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<tr>
<td>2114</td>
<td>450 ns</td>
<td></td>
<td>100 mA</td>
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<tr>
<td>2114L</td>
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<td></td>
<td>70 mA</td>
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<td>2142</td>
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<td>100 mA</td>
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<td>2147</td>
<td>70 ns</td>
<td></td>
<td>160 mA</td>
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<td></td>
<td></td>
<td></td>
<td>Active 20 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Deselected</td>
</tr>
</tbody>
</table>

The 2114/2114L series is already as easy to get from stock as the 2102A. The 2142 soon will be. Contact any Intel franchised distributor: Almac Stroum, Component Specialties, Cramer, Elmar, Hamilton/Avnet, Harvey Electronics, Industrial Components, Liberty, Pioneer, Sheridan, L.A. Varah or Zentronics.

For your copy of our Static RAM Family Album, write: Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.


intel delivers.
Across the desk
(continued from page 7)

Markets, not people make the differences

In response to your editorial challenge about the differences in consumption patterns between countries (ED No. 2, Jan. 18, 1977, p. 51), let me suggest some marketing reasons for dissimilarities by relating them to automatic transmissions:

- The American market may include a greater population of women who make the purchasing decisions and prefer automatics.
- The American market may have a higher level of expendable income, thus more interest in accessories.
- The American cultural background may make automation more acceptable.

I submit, then, that the markets are different—much more so than the innate differences in any two comparable individuals, one from each market.

Charles F. Turner
Engineer
Cricket Hill
Amherst, NH 03031

Try depending on personal values

I don’t know if all men are brothers (see “Are All Men Brothers?” ED No. 2, Jan. 18, 1977, p. 51), but there sure are a few I would hate to see marry my sister. Some differences really do go pretty deep—or else we wouldn’t need police. Still, most people are very much the same the world over—as your editorial pointed out. Including the habit of absorbing their concepts of value from those around them, by a process akin to osmosis. An extreme example: it is not really necessary to tell one’s children that it is not nice to barbecue the neighbors for lunch. The idea is obvious, because the matters involved are both so important and so obviously objective.

However, the value of remote controls in television receivers isn’t obvious. Most consumers’ grasp of what remote controls are good for and what they mean to them is derived entirely from the implicit “idea pool” in their market area. And their resultant purchases are the expression of these ideas in action. It would be interesting to see what would happen if the idea took hold that each individual consumer has to grasp the values involved for himself—and live with the results of his evaluation. Marketing patterns might change in rather surprising ways.

Richard W. Bowser
President
R.W.B. Research Co.
5648 Pierce
Omaha, NE 68106

What’s in a name...

In your editorial of Jan. 18, 1977 (ED No. 2, p. 51), you asked for help in explaining the buying habits of Europeans. Why this is bought instead of that—not even market-research experts can explain. I have no answer either. However, there is one thing I know: Johann Schiller did not write the “Ode to Joy.” It was Friedrich von Schiller (1759 to 1805).

Also, the German, “Alle Menschen werden Brüder,” translates into “All men become brothers,” not “are brothers.”

Manfred Moerre
Consumer Products Group
The Singer Co.
321 First St.
Elizabethtown, NJ 07207

Ed. Note: We bow to Mr. Moerre’s superior fluency in German but, in apology, wish to point out that our “All men are brothers” is from a free translation by the poet and anthologist, Louis Untermeyer. We disagree with the statement that Johann did not write the Ode, but agree that Friedrich did. The man’s name was Johann Christoph Friedrich von Schiller.

Headlight circuit works as advertised

In reply to William Sloan’s letter appearing in the March 1 issue (ED No. 5, p. 7) concerning my headlight delay circuit (ED No. 18, Sept. 1, 1976, p. 114): I maintain that the circuit will work “as advertised” if the switch, S1, in the original circuit—with no other modifications—has a center-off position. This subtlety, which was not fully explained, provides the versatility of three functions: delay, automatic shut-off and bypass.

In the delay mode, the delay begins after the ignition is turned off regardless of the light-switch position. In the automatic shut-off position (S1 in center-off mode), the delay starts after the ignition is switched off, provided the light switch is in the on position. The delay is terminated, if the light switch is turned off first. The center-off-position switch is more efficient than Mr. Sloan’s circuit, which adds extra components. Furthermore, Mr. Sloan reduces the three-function capability of the original circuit to two functions.

To improve the original circuit further, substitute a DPDT switch (with center off) for the SPDT S1 to provide two different time-outs: a long delay for the delay mode and a short (or no) delay for the automatic shut-off mode (see circuit).

John Okolowicz
Honeywell Inc.
1100 Virginia Dr.
Fort Washington, PA 19034

---

**Diagram:**

![Headlight Delay Circuit Diagram](image-url)
FAIRCHILD ANNOUNCES THE GREATEST BREAKTHROUGH IN BULK MEMORY SINCE THE DISC.
FINALLY. BULK MEMORY WITHOUT THE BULK.

Introducing the Fairchild 64K F464.
The first semiconductor CCD memory designed for the bulk memory market.
It plugs the gap between MOS and magnetic memories.
It's as important to bulk memory systems as the semiconductor RAM was to core.
It's a higher-density, lower-cost alternative to discs and drums.
The fact is, the new F464 is the densest memory ever made. A compact die size of less than 40,000 mil² — not much larger than today's 16K RAMs. All packaged neatly in a standard 0.3-inch 16-pin DIP.
This isn't a preview of coming attractions. The Fairchild F464 is available right now. With a second source already signed up.
THE STUFF INDUSTRY STANDARDS ARE MADE OF.

There has never been a device like the new F464.
It's a 65,536 x 1-bit dynamic serial memory organized as 16 randomly accessible shift registers of 4096 bits each. The four address bits are decoded on-chip to select which one of these 16 shift registers is to be accessed. Control inputs include Write Enable and Chip Select. It requires standard power supplies of ±12V and ±5V.

All inputs (except the clocks) are directly TTL compatible.

The two high-frequency and two low-frequency clock inputs are low capacitance 12V signals which can be easily generated with simple logic.

The data rate ranges from 1 MHz to 5 MHz. Since all 16 registers shift simultaneously, the average random access time (called latency) is only 410 µs at 5 MHz—a truly significant performance improvement over other bulk memory technologies! And, at the same time, the power dissipation remains low: typically 3.5 µW/bit at 5 MHz, and 0.6 µW/bit during standby at 1 MHz.

These performance benefits make the F464 a natural for hybrid head-per-tracks and fixed-head discs, extended cache, and many other high-density memory applications.

LOW COST FROM DAY ONE.

The new F464 is three to four times less expensive than RAMs. It is also cost-competitive with all fixed-head and many movable-head discs. So there are no trade-offs between price and performance. The Fairchild F464 gives you the best of both.

We also give you excellent delivery. Fairchild has a plant in San Jose, California totally dedicated to VLSI technology and production.

FOLLOW THE LEADER.

Fairchild pioneered CCD technology. We introduced the world's first commercially available charge-coupled device in 1973. Today, we offer the world's broadest line of CCD products. It stands to reason we'd be the ones to make CCD memories a reality.

For more information on the F464 (or our other CCD products), contact your Fairchild sales office or representative today. Or use the direct line at the bottom of this ad to reach our MOS/CCD Division. Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, Calif. 94042. Tel: (415) 962-3941. TWX: 910-373-1227.
Field lab!

Now you can take advanced multi-channel recording technology out of the laboratory and into the field. EMI's proven SE7000 rivals the versatility, fidelity and performance of the most expensive lab recording systems. Yet it's rugged enough, compact enough to travel to the factory floor, the launch pad or any other operation site.

The SE7000 handles the full range of requirements from routine 14-track midband all the way to 42-track recording capability. It offers a choice of eight speeds between 15/16 and 120 ips providing 600 kHz DR or dc to 80 kHz FM at 120 ips. Equalizers and filters for all tape speeds are built in as standard. And it has a built-in calibration module, eliminating the need for time-consuming cross-patching.

All these features are packed into a transportable unit so rugged that the system is warranted unconditionally for a full year. Complete with its internal AC or DC power supply, the weight is less than 100 pounds.

The SE7000 has gone into the field in automotive, aerospace, petrochemical and transportation applications all over the world. Applications, like yours, that need laboratory precision but can't be brought to the lab.

EMI Technology Inc., Instrumentation Division, 55 Kenosia Avenue, Danbury, CT 06810 (203) 744-3500, TWX: 710-456-3068
The TRW TDC-1004J is a 64-bit digital correlator capable of operating at 15 MHz with analog correlation output. Digital parallel correlation is a signal processing technique used for bit synchronization, bit detection, error correction coding, pulse compression and other applications. Correlation takes place when two binary words are serially shifted into two independently clocked shift registers. The two words are continually compared bit-for-bit by exclusive-OR circuits.

Each exclusive-OR circuit controls a current source D/A. The current outputs of the D/A circuits are summed to produce the correlation function.

The mask register allows the user to selectively choose "no-compare" bit positions.

For detailed data, applications information and prices, contact your local TRW components sales office or call (213) 535-1831 or write TRW LSI Products, An Electronics Components Division of TRW, Inc., One Space Park, Redondo Beach, Calif. 90278.
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of your microprocessor system, HP's compact, low cost lab power supplies offer more. For example, Models 6236B and 6237B offer three adjustable output voltages. Model 6236B covers 0 to 6V at up to 2.5A. Model 6237B is 0 to 18V at up to 1A. Both have plus and minus outputs of 0 to 20V that track within 1%, or you can switch to a variable tracking mode which allows the negative output to be separately set lower than the positive providing three different output voltages. There are no turn-on/off voltage transients so your circuit is protected against damage. Both models are designed to make development work with microprocessors easier.

for the end product...

where you can feature a triple output OEM Modular Supply specifically designed for powering microprocessor systems. Model 62312D provides three isolated, independently adjustable outputs. The main output is rated at 4.75V to 5.25V at 3A. Two others each range from 4.75V at 0.38A to 12.6V at 0.6A. Other standard features to help optimize your microprocessor design include an internal AC line fuse, fixed foldback current limit, over voltage protection on the main 5V output, remote programming terminals for margin testing and much more. Write for complete details or contact your nearby HP field sales office.
Low-cost logic analyzers aim to fill more needs

As prices for logic-state and logic-timing analyzers fall, digital test techniques using these analyzers are filtering down from research and design labs to production floors, out into the field, and even to the hobbyist. In fact, the latest logic analyzers are so inexpensive that engineers may no longer have to share a lab’s single analyzer.

“Each digital-circuit designer can have a logic analyzer,” says Dave Blecki, marketing vice-president at Biomation Corp., “just like he has his own oscilloscope.” The Cupertino, CA, firm’s latest logic-timing analyzer, the Model 920-D, is priced at $1295—about the same as a high-quality scope like the Tektronix 465. Biomation’s older models are 10 times more expensive.

Hewlett-Packard Co., too, has introduced a low-cost logic analyzer, the Model 1602A. Priced at $1800, the HP logic-state analyzer is aimed at production-line and field-service testing, says Bruce Farly, product planning manager for digital products at HP’s Colorado Springs division.

An even less expensive analyzer, from Paratronics Inc., San Jose, CA, is the $429 Model 150. Available for $349 in kit form, the 150 has a single card that plugs into the S-100 small-computer bus and monitors 64 of the bus’s lines. The S-100 bus lines monitored include data in, data out, address, status, control, and interrupts, with an additional eight user-selected lines.

“It’s an easy way to look at the bus,” says Ira Spector, Paratronics president. What’s more, “Sophisticated logic-analyzer functions can now be an integral, resident part of a mainframe computer system.” A small control pod connected to the analyzer through a ribbon cable allows the operator to set the 150’s triggering, display formatting, and operational modes. A coaxial cable brings signals from the analyzer to an oscilloscope.

Data on the scope screen can be in octal or hexadecimal format, with 16 eight-bit data words grouped in threes or fours.

The Model 150 can be triggered to store data by the 16 bus-address lines or by eight input-data lines, or both for a 24-bit trigger word. The clock can be external or taken directly from the S-100 bus. Data collection rate is up to 8 megabytes/s.

HP’s Model 1602A, controlled by an F8 microprocessor, has a memory 16 bits wide and 64 words deep. It automatically tests itself every time power is turned on, and has an optional IEEE-488 interface.

Setting the 1602A is simplified by the F8—a feature necessary for field-service applications. Pushbuttons select logic polarity and clock-pulse polarity, and set the display to hex, decimal, octal or binary. A trigger word is selected, and a delay of anywhere from 0 to 65,535 clock intervals before data trace can be specified.

A clip-on probe set plugs into an edge connector on the 1602A probe. The connector mates with similar connectors at test points on new equipment—which simplifies point-to-point probing.

Biomation’s 920-D is a 20-MHz logic-timing analyzer that has eight channels plus a ninth input that can serve as either an extra signal input or as a trigger marker and qualifier. Besides the eight combinational trigger and qualifier switches, an extra switch works with the auxiliary input. Delay can be by events or by as many as 9990 periods.

The 17-lb 920-D has a latch input mode that can capture narrow pulses or glitches as short as 10 ns.

For Biomation Circle No. 316
For Hewlett-Packard Circle No. 317
For Paratronics Circle No. 318

Plastic-cased PROM matches EPROM for less

A PROM housed in an expensive plastic package not only costs less than half as much as a 2708 EPROM, but can fit into every socket that uses a 2708.

There is one catch. Unlike the 2708 EPROM, the MCM2708P from Motorola, Austin, TX, can’t be reprogrammed. The opaque plastic housing prevents UV light from erasing the memory contents.

However, in many cases, a 2708 EPROM isn’t reprogrammed anyway. Normally used to hold a program during its development, the EPROM is often left in a final product until the designer can replace it with a less expensive, mask-programmed ROM. And the designer may have to wait anywhere from four to 12 weeks for it.

But with the MCM2708P, there is no wait. The chip slips right into a 2708 EPROM socket, programs just like a 2708 EPROM, and matches its performance. The Motorola chip accesses in 450 ns and dissipates 600 mW.

When purchased in 100-qty lots, the MCM2708P is expected to go for less than $10.

Yak it up long-distance—but watch the charges

Dial a number—any number—in the U.S. or Canada, and a µP-based telephone system, the Extension I, knows the current long-distance rates. Even as you talk, a LED display shows you how much the call is costing. (An audible “beep” warns you six seconds before you incur the next cost increment.) When you hang up, you get a hard-copy record of the call, including the number you called, how long you waited—and exactly how much you owe.

For Paratronics Circle No. 319

August 16, 1977
The Extension I designed by Tele-neutronics of San Jose, CA, is a 7-lb., 11 × 17-in. desk telephone that looks like a standard Call Director. But the similarity ends right there. The Extension I uses a Motorola 6800 µP, a 6-kbit memory, four keyboards and a thermal printer for both accounting and nonaccounting jobs. Tap in a three-letter code and the computer telephone will dial one of 100 commonly dialed numbers of your choosing. Used as an event timer for meetings and incoming calls, the Extension I will add the charges onto clients’ monthly totals.

This 10-line business-phone system also has a five-function calculator and an appointment-calendar system, both with printouts. An alphanumeric “typing” keyboard lets you add notations into the printed reports.

But even with these many convenience features, plus the ability to call you half an hour early to remind you of key appointments, the main reason for developing the Extension I was to attack cost-control problems.

Dwight R. Nunes, now president of Tele-neutronics, was running a chemical brokerage firm, and helplessly watching his phone bill hit $3000 a month. “I had no control over the charges, and that’s when I went to work on this idea,” he recalls.

Scheduled for September deliveries, the $1995 Extension I only handles calls to specific area codes, but permits exceptions for certain allowed numbers. However, the telephone won’t work at all unless you first “unlock” it by identifying yourself with a special code. If Extension I is accidentally or illicitly unplugged from the computer-telephone network, it sounds an alarm and “locks” itself so that no calls can be made.

### Home computer spells out errors in plain English

The latest entry in the personal computer market—Pecos 1016—uses an extension of JOSS language to make it easier for the user to spot his own errors.

JOSS, developed by the Rand Corp., is similar to BASIC but has a superior plain-language error commentary, according to Ken Boilen, chief engineer for APF Electronics, New York, which developed the personal computer. For example, if the user inadvertently tries to divide a number by zero, Pecos will say, “I have a zero divisor.”

The Pecos, which will be initially supplied with a 9-in. CRT monitor, is based on MOS Technology’s 6502, 8-bit microprocessor. A later model will be able to use a home TV screen the way a typewriter, plus additional keys to simplify communication with the Pecos. To request action or input information, a user types in simple English sentences with up to 80 characters per sentence. The output is up to 40 characters per line, with up to 16 lines at a time. Moreover, when the screen is filled, Pecos can scroll. That is, it shifts the top line off of the screen and adds a new one on the bottom.

There are two main computer memories, one holding 16-k 8-bit bytes of dynamic RAM, the other a 14-k operating-system ROM. Two 30-min. tape cassettes handle programs that exceed the internal-memory storage. These decks can store 1000 lines of commands at 80 characters per line—a maximum of 80,000 bytes.

Once the tapes are engaged, the operator can tell Pecos to read or write. The computer then takes control. An address track on each tape tells the computer where to find specific data. In addition, information on one tape can be transferred to the other.

The Pecos can process arithmetical, logical and textual strings. It has a floating-point-arithmetic capability of nine digits with a calculations range of 10^-9 to 10^9.

The keyboard is full ASCII, with both upper and lower case letters. An RS-232 output is provided for the Pecos printer, which can be operated at 110, 150, 300 or 1200 bauds.

Deliveries start in December. Price is projected to be between $1000 and $1500.

### MOSFET-type IC detects smoke, measures humidity

An IC device can detect smoke or measure humidity by combining thin films of special polymers—similar to plastic—with the structure of a so-called “charge-flow transistor.” The transistor resembles a MOSFET, but with a portion of a MOSFET’s metallic gate structure replaced by the polymer film.

The detector and the circuitry necessary to operate it can be put on a chip 0.05 in. square, according to its inventor, Dr. Stephen D. Senturia, associate professor of electrical engineering at MIT.

The humidity and smoke-sensitive polymers are just two of many polymer materials developed by Senturia to respond to the pressure of microscopic particles in the air. As a matter of fact, Senturia adds, “We hope to find other polymers that will respond to a number of hazardous gases and pollutants.”

The sensor is fabricated with the standard four-mask process for p-channel MOSFETs. Depositing the polymer film is the final step. A change in sheet resistance of the film is the key to device operation.

The charge transistor was developed with the support of the National Aeronautics and Space Administration. “We are now finding that the charge-flow transistor is an excellent tool for studying the properties of thin films,” says Senturia. “Our current experiments are aimed at developing a theory to explain the behavior of thin films.”
What's in a Number?

For over a decade Military Specifications have been written around Semtech E.l.A. registered medium power rectifiers. Many suppliers can provide parts with the same JAN, JANTX or JANTXV label. Although these devices may comply with the appropriate military specification, there can be significant differences in the design and manufacture that may affect the reliability; such as, different lead materials, pin materials, body materials, junction types and junction areas. Devices of one manufacturer are not necessarily the same as those of another, even though they are labeled with the same part number.

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| MIL-S-19500/286C | JAN, JANTX, JANTXV 1N4245 |
| MIL-S-19500/358B | JAN, JANTX, JANTXV 1N4942 |
| MIL-S-19500/411C | JAN, JANTX, JANTXV 1N5415 |
| MIL-S-19500/420A | JAN, JANTX, JANTXV 1N5550 |
| MIL-S-19500/427B | JAN, JANTX, JANTXV 1N5614 |
| MIL-S-19500/484(EL) | JAN, JANTX 1N5835 |
| MIL-S-19500/503(EL) | JAN, JANTX, JANTXV 1N6073 |
| MIL-S-19500/516(EL) | JAN, JANTX, JANTXV 1N6102 thru 1N6137 |
| MIL-S-19500/533(EL) | JAN, JANTX, JANTXV 1N6138 thru 1N6173 |
| MIL-S-19500/563(EL) | JAN, JANTX, JANTXV 1N6550 |
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| MIL-S-19500/420A | JAN, JANTX, JANTXV 1N5550 |
| MIL-S-19500/427B | JAN, JANTX, JANTXV 1N5614 |

**NASA (MSFC) Approvals**

85M01645 (NASA) S1N645S & S1N649S
85M03895 (NASA) S1N4245-1, S1N4247-1, S1N4249-1, S1N4942-1, S1N4946-1 & S1N4948-1
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CIRCLE NUMBER 15

ELECTRONIC DESIGN 17, August 16, 1977
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CIRCLE NUMBER 20
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New York's blackout: Too many questions, not enough answers

Was it an "act of God"? Or was it “gross negligence” on the part of Consolidated Edison Co., New York's electric-utility company, that left sections of the city without power for as long as 25 hours? Could better protective circuitry on the company's power lines have prevented the disaster? Or did the protective circuits installed in response to the last Great Blackout, in 1965, actually contribute to this year's outage?

In 1965, a failure at a distribution center near Buffalo knocked out utilities one by one across the northeast. Some large generators were damaged as they tried to keep power flowing.

To prevent a recurrence, automatic disconnect relays were installed between utilities, so that a severe drain in one would not drag others along. In addition, Con Ed added power lines north of New York City so that no one line would have to carry the whole burden. Additional relays were put in to disconnect overloaded generators from the system.

Even with these safeguards, Con Ed went down. Though the problem was limited to Con Ed, and no damage was done to any of Con Ed's generators, the precautions designed to prevent a blackout failed. New York City went dark again.

The city, whose mayor, Abraham Beame, considers Con Ed negligent, will investigate. Con Ed, whose chairman Charles Luce, blames God, will investigate. So will New York State's Public Utilities Commission and the Federal Power Commission. But all that's really known right now is that 9-million people in the six counties served by Con Ed were unplugged at about 9:35 p.m. on July 13, and that service to some of Con Ed's customers wasn't restored until 10:30 the following night.

Lightning strikes

Trouble actually started at about 8:30 p.m., when a severe thunderstorm passed through Westchester county, north of New York. Lightning apparently struck two 345-kV transmission lines near a substation at Buchanan, NY (see map). Without the substations, 900 MW then being supplied by the Power Authority of New York's nuclear power plant at Indian Point—Indian Point 3—were disconnected from the rest of the power grid. Indian Point 2, which is owned by Con Ed, was out of service for repairs, and the obsolete Indian Point 1 has been shut down for years.

According to Arthur Hausburg, president of Con Ed, the loss of the Indian Point generators was easily made up by drawing more power from upstate New York and Canadian sources. Of the 5800-MW demand on Con Ed at the time, half—2900 MW—was already being drawn from outside sources.

Con Ed is required by New York State law to deliver power to its customers at the lowest possible cost, explains Luce. And it is less expensive to buy power from outside sources than to generate it within New York City.

When power-line problems occur, an operator at Con Ed's energy control center on the west side of Manhattan begins switching in alternate sources of power and planning for the possibility of further losses. The control center, built in 1962, employs 100 technicians to monitor and supervise power generation and transmission through Con Ed's network of 325 substations.

At the control center, six system operators, one on duty at all times, forecast the expected load for each day based on weather reports and historical demands. The operator interfaces with Con Ed's control computer through a CRT terminal on which information from every substation can be displayed. Visible and audible alarms warn of problems, and a row of seven switches cuts off power to sections of the Con Ed service area when the demand for electricity exceeds the supply.

With part of Con Ed's capacity out

Andy Santoni
Associate Editor
The only Double-Balanced Mixers with a 2-YEAR GUARANTEE featuring Hi-Rel tested diodes.

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of service, the operator began increasing power generated within the system. About 1000 MW are available from other Con Ed plants by computer command or telephone instructions to plant crews.

Suddenly, at 8:56, two more transmission lines went out—also apparently struck by lightning. These lines, just east of Buchanan, carry power from the northeast power-sharing grid. So now only one line was still connected to the north. Smaller ties were still connecting Con Ed to the Long Island Lighting Co., east of the city, and to Public Service Electric and Gas Co., in New Jersey.

**Outside power drawn**

Before lightning struck, 250 MW of power was actually flowing from Con Ed to Long Island via the LILCO tie line. But with Indian Point and the lines to the north out of service, Con Ed began drawing power from LILCO, as well as PSE&G.

To protect its system, Con Ed dropped voltage first by 5%, then by 8%, and disconnected power from Mount Vernon and Elmsford in Westchester county. That cut the load on Con Ed to between 5000 and 5500 MW.

But at 9:19, for a still-unknown reason, the third and last line to the northeast power grid was lost. This left Con Ed with its own capacity and the two smaller tie lines: LILCO could supply about 300 MW and PSE&G between 400 and 500 MW. But the combined demand from these two lines was at least 1100 MW, and surged to as much as 2500 MW.

One minute later, the LILCO tie line tripped out—a protective measure developed after the 1965 blackout. Circuit breakers prevented the “domino” effect from reaching outside Con Ed’s service area.

Phase-angle regulators sense changes in line frequency quickly, and as power demand exceeds supply and generators slow, power-line frequency begins to change. Thus, the tie to PSE&G disconnected at 9:30 to prevent that utility from joining Con Ed in darkness.

Now Con Ed was left with about 3000 MW of its own generating capacity, and a demand still around 5000 MW. Line frequency dropped to less than 59 Hz, from its normal 60 Hz, and lights began to dim throughout the service area.

Another feature of the protective system developed after the 1965 blackout is the ability of Con Ed to drop sections of its service area. The seven load-shedding switches in the Con Ed energy-control center can cut off up to 50% of the load, according to chairman Hauspurg, “controls regulating the voltage began to have difficulty following the swing. The machines became unstable.”

To protect itself from overload damage, Ravenswood 3 automatically disconnected from its manufacturer, Allis Chalmers. Without sufficient load shedding, Ravenswood 3 couldn’t supply enough power. As line frequency changed, says Hauspurg, “controls regulating the voltage began to have difficulty following the swing. The machines became unstable.”

To prevent itself from overload damage, Ravenswood 3 automatically disconnected itself from the Con Ed system. Protection had been installed after the 1965 blackout to prevent a recurrence of the damage sustained by the generator when its oil pumps lost power, and a loss of lubrication destroyed the machine’s bearings and windings.

The Ravenswood 3 relays had operated before another protective series of relays, installed after the 1965 blackout, could shed load automatically. The phase-sensing relays did not trip because the line frequency did not change enough before Ravenswood 3 cut out.

Without “Big Allis,” Con Ed’s other generators shut down. Total failure struck at 9:34.

In the hour between the first sign of trouble and the loss of Big Allis, not enough of Con Ed’s standby generating capacity could be brought up to handle the load. The next day, after power had been restored, Con Ed began staffing its standby plants around the clock, to speed turn-on when necessary. One suggestion made—an expensive one—was to keep standby generators spinning, even if they are delivering little power. Otherwise, checking it out the generator, getting oil into its bearings, and bringing it up to speed and in synchronism with the rest of the power grid could take an hour or more, as this year’s blackout proved.

**Trying to cope without power**

In the city’s commercial centers, computers without backup power went off the air immediately. Those with battery-based uninterruptible power supplies shut down in a more orderly fashion, first storing data in non-volatile memories. A few sites, like the Citicorp banking computer center, had emergency generators and kept working with only an hour or two lost.

Computer-service crews raced around the city—carefully, since traffic lights were out—checking for damage and preparing equipment for a sudden surge of power and the voltage spikes that are inevitable when air conditioners, elevators, lights, and water pumps all come on at once. New York Telephone Co., which once suffered from equipment shortages that led to waiting minutes for a dial tone, came through. Since almost all its customers are served by battery-backup power systems, even the unusual volume of emergency calls during the blackout didn’t clog the system.

**Power begins to return**

To bring power back on without surges that would simply knock the system out again, Con Ed first had to open breakers on feeder lines throughout the city. Unlike virtually all other utilities, Con Ed maintains most of its lines underground. The lines are insulated and cooled by oil, so each segment has to wait for oil pressure to build up before coming on stream. As capacity was brought up, sections of the service area were cut in one at a time, matching supply to demand.
Save time and money with SAE Strip-Pak™ rotary PCB switches. These snappy little numbers come in a wide range of output codes, and are the most reliable PC board rotary switches you can buy.

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Computer-graphic photo montage simplifies land-use projects

A new computer-graphics technique may make environmental reports easier to produce and may cut the costs of landscape architecture.

A computer is used to draw oblique pictures that represent landscape changes. The resulting photo montage will reduce the cost, time and subjectivity of artists' concepts.

Such a system has been developed for the U.S. Department of Agriculture by the Aerospace Corp., El Segundo, CA. It is installed at the U.S. Forest Service headquarters at Fort Collins, CO, to evaluate the visual impact of new fuel breaks—clear-cut strips designed to contain forest fires in inaccessible areas.

The Environmental Protection Agency (EPA) frequently demands environmental impact reports to illustrate the visual aspects of land-use projects such as refineries, man-made lakes, mountain roads and ski roads.

It starts with a camera

The process begins with a photo of the proposed site. A camera is positioned at a vantage point of concern, say a picturesque bend in a distant road.

Next, a U.S. geological-survey map of the area with a resolution of 7-1/2 minutes is digitized along its contour lines and fed to the computer.

"Up to 40,000 individual points on the map can be digitized in one day," says Aerospace program manager Al Stevenson. "And the process can cost as little as $50."

At least four ground-reference points are selected to key the photo to the map. Using these references, the computer rotates the "bird's eye" view of the map down to coincide with the camera's more normal perspective.

Taking a picture of a lake that isn't there yet is less costly than surveying, more accurate than an artist's concept and quicker than building a model. Photograph of actual site (top) is matched to a survey map of the area. The map is digitized along its contour lines, software-rotated to the camera's vantage point and outputted to a pen plotter (middle). A photographic process superimposes the two into a montage; an artist adds color and texture (bottom).
AN OPEN CHALLENGE:

"We defy you to find a more reliable DIP socket or a less expensive one."

Joe Bradley, Mktg. V.P. Burndy Corporation
Forget everything you've ever known—or thought you knew—about DIP sockets. And especially about DIP socket costs.

Burndy's new low-cost, high-reliability GTH DIP sockets have changed everything for the better. Now, for just pennies you can use DIP sockets where you never dreamed of using them before—to enhance your product without pricing it out of the market.

And in most cases, using our DIP sockets adds nothing to overall costs. It can even result in a net cost reduction in many applications by simplifying design. Speeding installation.

Laboratory Proof

<table>
<thead>
<tr>
<th>Test Performed</th>
<th>Min.</th>
<th>Max.</th>
<th>Avg.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUP 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mating Force (lbs./contact)</td>
<td>0.600</td>
<td>0.730</td>
<td>0.643</td>
</tr>
<tr>
<td>Contact Withdrawal Force (oz. w/0.008&quot; blade)</td>
<td>2.500</td>
<td>8.100</td>
<td>4.940</td>
</tr>
<tr>
<td>Insulation Resistance (600 VAC for 1 min.)</td>
<td>2x10⁶</td>
<td>2x10⁶</td>
<td>2x10⁶</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>2.950</td>
<td>5.860</td>
<td>4.650</td>
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<tr>
<td>GROUP 2</td>
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<tr>
<td>Vibr. &amp; Mech. Shock</td>
<td>5.050</td>
<td>5.930</td>
<td>5.420</td>
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<tr>
<td>Durability (50 cycles)</td>
<td>5.050</td>
<td>6.750</td>
<td>5.520</td>
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<tr>
<td>GROUP 3</td>
<td></td>
<td></td>
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<tr>
<td>Insulation Resistance (5,000 megohms min.)</td>
<td>&gt;2x10⁶</td>
<td>&gt;2x10⁶</td>
<td>&gt;2x10⁶</td>
</tr>
<tr>
<td>Ins. Res. after Moist. Res. (5,000 megohms min.)</td>
<td>&gt;2x10⁶</td>
<td>&gt;2x10⁶</td>
<td>&gt;2x10⁶</td>
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<tr>
<td>GROUP 4</td>
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<tr>
<td>Contact Resistance</td>
<td>5.200</td>
<td>6.350</td>
<td>5.545</td>
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<tr>
<td>after Corrosive Atmos.</td>
<td>4.850</td>
<td>6.350</td>
<td>5.519</td>
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Comparative Test Data (Durability and Moisture)

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</tbody>
</table>

Low-cost DIP sockets for all types of applications

Burndy DIP sockets are currently being used in a wide variety of applications where high reliability and economy are required.

Burndy DIP sockets are used in the Dictaphone Thought Center 293, a multiple-cassette, central dictation system for word processing applications.

Burndy DIP sockets have been specified for the Model 1430 print-plus-display calculator by Monroe, The Calculator Company.

Burndy DIP sockets have helped simplify design for Fairchild's popular Video Entertainment System.
Dear Joe: I like what you’re saying but you’ve got to prove it to me in my own application. Here are my requirements:

- Product Application
- Operating Temperature
- Mating Cycles

Please use the Quick Response Card and I’ll send you data worth its weight in gold.

Name: ______________________  Title: ______________________
Firm: ______________________
Address: ______________________
City: ______________________  State: ______________________  Zip: ______________________
Leaded or leadless Burndy leads the way in DIP Socket Design

Leaded or leadless. Solder tail or surface mount. Standard or hybrid. Top, bottom or side pad. Any required shape or size. Burndy makes DIP sockets to fit virtually every application need, any performance level. And they all have two things in common. Low cost and high reliability. That's because they all feature our patented GTH contact design that delivers good-as-gold connections without the cost of gold. And that's why you find our DIP sockets in such a wide variety of applications from highly sophisticated computers to TV receivers, from automotive applications to complex process control systems. Burndy Corporation, Norwalk, Connecticut 06856.

For more information on how Burndy low-cost, high-reliability DIP sockets can help you improve your product without pricing it out of the market, send us your particular requirements.
HP's new Display Trace says a lot:

Large 500 cm² (77.4 in²) viewing area says the 1304A is excellent for applications in electronic analyzer systems; analytical instruments; weather, harbor or fire-control radar; plus medical patient monitoring systems.

Complex graphic display plus a large number of characters says high-writing speed and fast settling time. HP's new 1304A Large Screen Display has a linear writing speed greater than 25 cm/psec, and settles to within one spot diameter in 300 nsec.

Small spot size (0.020") and high brightness says sharp pictures and good readability...even in normally lighted industrial environments.

It all adds up to value. Low cost, high performance, high reliability, flexibility and after-sales service. A good combination for any display system. Ask your HP field engineer for all the details including OEM and quantity discount prices. He can also give you details on other models in HP's growing family of large and small screen displays.

* Domestic U.S.A. price only.

Hewlett Packard
1507 Page Mill Road, Palo Alto, California 94304

For assistance call Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

CIRCLE NUMBER 24

Electrostatic deflection means low power consumption (just 60W average), thus higher reliability due to lower operating temperature. Light weight compared to magnetic displays is another plus.

The price of just $2400* means benefits and performance of electrostatic displays at a cost approaching that of magnetic displays.

Modular construction and an uncluttered interior means easy servicing and calibration.

Controls and user-settable adjustments concealed behind a front-panel door means fast access while discouraging knob twiddlers.
Then it outputs the entire rotated image to a pen plotter to see if it registers with the photo.

For registration, three or more points on the map and the photo must align. "You can select roads, storage tanks, or mountain peaks," according to Gerry Harju, Aerospace department head who did the programming. "But if you pick a point on the map that turns out to be hidden in the photo, you will have to reiterate the process."

Once the two images are in registration, a drawing of the proposed landscape alteration gets digitized and inputted to the computer. The system can handle three types of alterations:
- Political boundaries and ski runs that lie on the surface of the terrain.
- Lakes and strip mines that actually change the topology of the area.
- Man-made structures, like towers, buildings and smokestacks.

Alphanumerics can be generated and used for identifying particular features.

After being digitized, registered, and integrated with the scene, the proposed alterations can be manipulated to determine how best to implement them.

If, say, a proposed ski run looks too far to the left or to the right, software can move it over.

Alterations can be mathematically manipulated, too. A series of images showing the progression of a strip mine's boundaries over a period of time (as a function of the volume of earth removed) can be generated.

"A movie showing the evolution of a strip mine over its entire lifetime can be enlightening," remarks Stevenson. "The technique will show where the overburden is piled, stored and ultimately returned as fill."

Real-time digital audio processor picks out distorted conversations

The FBI is using industry's first real-time digital audio processor to solve a case involving America's national security. This Automatic Digital Audio Processor (ADAP) from Rockwell International, Anaheim, CA, uses digital spectral analysis to strip away masking noise from a recorded clandestine conversation.

If the FBI gets it's man, it should have little trouble convincing a court of what was actually said. The noise will be filtered out well enough for the remaining audio to be admitted as evidence.

The "real" key

The spectral-analysis technique enables the self-contained ADAP to operate in real time by bypassing the conventional reiterative recording step used by other audio processors.

"Two different audio-enhancement schemes are at work in this instrument," explains Program Manager Dr. James Paul, "and they are both adaptive in nature."

One process, called "adaptive predictive deconvolution," wrings out such signal-related noise as echoes, reverberations and other signal convolutions.

In this single-input mode, ADAP uses a 150th-order digital filter to estimate the amount of noise associated with a signal. The filter's response time is adjustable from the front panel.

If elimination of the conventional recording step required in other digital audio processors, it can be used in real-time communications systems.

This digital audio processor is the first to operate in real time. Since it eliminates the conventional recording step required in other digital audio processors, it can be used in real-time communications systems.
Hello, 25% Higher Current, 45 V @ 150°C, Switchmode Schottkys.

Meet the world's first power Schottky rectifiers to give top performance at high temperatures with no derating, backing off or baloney. Motorola Switch-mode* Schottkys.

Switchmodes are full-rated at 150 A, 45 V, 150°C conditions simultaneously. You-know-who’s aren’t.

And the MBR7520-45 series can save you 20% in power at 100 A because of lower VF— or 12 W less power loss vs competition. The 1,000 A surge current rating is something to welcome, too.

The whole family has unique guarding construction providing avalanche characteristics for transient protection plus low leakage for added reliability.

<table>
<thead>
<tr>
<th>Schottky Type</th>
<th>Peak Forward Current* (Rated VR) (Amps)</th>
<th>Average Forward Current* (Rated VR) (Amps)</th>
<th>Max VR @ TJ = 150°C (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBR7545‡</td>
<td>150 (Tc = 90°C)</td>
<td>70 (Tc = 90°C)</td>
<td>45</td>
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<tr>
<td>SDS1†</td>
<td>120 (Tc = 70°C)</td>
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<tr>
<td>MBR6045‡</td>
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<td>45</td>
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<tr>
<td>1N6098</td>
<td>-</td>
<td>90 (Tc = 90°C)</td>
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<td>MBR3545‡</td>
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<td>1N6096</td>
<td>-</td>
<td>25 (Tc = 90°C)</td>
<td>40</td>
</tr>
</tbody>
</table>

Even dv/dt is better . . . 1,000 V/µs for the MBR7545. And C. It’s just 0.8°C/W instead of the usual 1.0 for more efficiency.

And that’s what Schottkys are all about—superior performance and efficiency in high-frequency switching applications. The new series will be state-of-the-art industry standards in those designs.

Prices are more attractive, too!
Say hello to our good buys. Send for Switchmode Schottky data sheets and get spec-by-spec, side-by-side comparison of these new DO-4s and DO-5s with outgoing standards. It’s an eye-opener.

Write Motorola Semiconductors Inc., P.O. Box 20912, Phoenix, Arizona 85036.

*Trademark of Motorola Inc.
When adjusted to a slow adaption rate, ADAP cancels out echoes and other long-term stationary effects. Dialing in a faster adaption rate lets the instrument track and kill shorter-term interfering signals like background music or another, unwanted voice. ADAP can even clear up a telephone voice disguised with the old 'handkerchief-over-the-mouthpiece' trick or one with background music.

Two mikes help

The other enhancement scheme, called real-time adaptive filtering, uses two simultaneous inputs from two different microphones. One input contains the desired audio signal combined with all on-site ambient noise. The other comes from a microphone that samples the background noise alone.

This second input's noise may differ quite a bit from the first, but the signal is modified by a transversal filter that adjusts noise amplitude and phase. This produces an estimate of the noise component in the first audio signal.

This estimate is subtracted from the (first) composite signal and then fed back to the transversal filter to null out the audio signal's noise component.

The instrument's adaption speed ranges from less than 200 ms to over 5 s, according to Dr. Paul. It attenuates convolution and additive noise by over 40 dB, and has 12-bit d/a and a/d resolution. The digital filter can be adjusted as high as the 256th order.

Many crimes have already been solved with the ADAP, including murder, rape and burglary.

It can also be used in live communications systems like air-traffic control or on-location radio and television news coverage. Pretaped audio from police "bugs" or cockpit recordings from wrecked airplanes are also candidates for audio cleanup.

ADAP measures 3-1/2 x 19 x 21 in., weighs 40 lb and costs $25,000.

Manpack satellite communications
links soldiers with air, sea support

Both voice and digital-data satellite communications can now be conducted between soldiers in battle and ships, aircraft and ground stations with a manpack communications system. The AN/PSC-1, a 25-lb transceiver, can output 35 W of power directly to an orbiting satellite to achieve long-range, interference-free communications—as far as 9000 miles.

The power required for the transmitter has been kept to a minimum by using a special modulation scheme. As a result, the transceiver can achieve extremely low signal-to-noise ratios.

The transceiver uses time-interleaved quadrature binary phase-shift-keyed modulation to transmit digital data at 300 bps. And with a combination of offset quadrature-phase, shift-keyed modulation and continuously variable slope-delta modulation, the transceiver can transmit voices to within 2 dB of the theoretical signal-to-noise ratio, according to Ed Rueve, project manager for Cincinnati Electronics in Ohio, which developed the AN/PSC-1 for the Army Satellite Communications Agency.

The transmitter can operate in either a satellite or line-of-sight mode. In the satellite mode it sends out 35 W. But the line-of-sight mode of operation requires only 2 W.

For satellite operation, a medium-gain helical antenna is provided, with a minimum gain of 6 dB. The antenna folds up into 300 cubic inches and can be assembled and ready for operation within two minutes. For line-of-sight operation, a whip antenna is used.

Transceiver is brainy

While the transmitter and receiver portions of the set are based on conven-
Making data move is the name of the game in today's switched or dedicated-line networks. If you're moving it at any speed up to 2400 BPS, Universal Data Systems has the proper modem for reliability, economy and efficiency in your system.

UDS has more than 30,000 modems in active field service, and the total is growing by more than 1,000 units per month. Our product line includes CMOS 201s, plus 103s, 202s, ACUs and the new 12·12, which permits full-duplex 1200 BPS communication over only two wires. UDS also offers the multiple modem RM-16, which contains up to 16 units in any configuration mix you desire.

In addition to our products, we're extremely proud of our customer service. Check us out: Call us on the telephone. You'll like what you hear.

universal data systems
4900 Bradford Drive • Huntsville, Alabama 35805 • Telephone (205) 837-8100 • TWX 810-726-2100
tional uhf designs, the control section of the transceiver is unusual, notes Rueve. A CMOS microprocessor uses an internal frequency synthesizer to control the frequency of operation, mode and the receiver's offset frequency. The micro does it with an internal frequency synthesizer.

Besides voice transmission, the transceiver features secure voice, data, selective calling and conference calling. It can receive any one of 15 selectable channels plus a conference channel. It also carries separate audible and visual alarms for selective and conference signals.

Unlike most military field-communications systems designed for voice transmissions, the AN/PSC-1 can accommodate digital-data transmissions as well. This is done with a digital message-entry device (DMED), which is basically a hand-held battery-powered terminal.

An Intersil 6100 microprocessor enables the DMED not only to send and receive digital alphanumeric data, but to edit the data as well. The DMED can change, delete or insert any character in the output message. In addition, input or output messages can be reread as often as desired.

**Mini keyboard enters data**

Data are entered into the DMED via its 32-switch ASCII keyboard, and are presented on 16 alphanumeric LED-display devices. An incoming or outgoing message may be scrolled across the display in ticker-tape fashion.

Several scrolling speeds can be selected for the keyboard.Scrolling may be stopped and started at will, and even reversed if desired.

In addition to the alphanumeric LED displays, the DMED has six LED status indicators, five of which are software-controlled. The displays indicate low battery, memory overflow, edit mode or acknowledge, shift mode, illegal operation and receive. To conserve power, the display is automatically shut off approximately 8 seconds after the microprocessor has completed its cycle. A change of either the frequency, receive offset or function controls will cause the microprocessor to start a new cycle and illuminate the display.

The DMED also features a serial, asynchronous I/O with selectable transmit and receive rates. If a modem is used, rates of 150, 300, 500 and 1200 bps can be selected. If not, 2400, 4800, 9600 and 19,200 bps rates can be used as well as the four modem rates.

The output of the device is a 6-bit ASCII code with odd parity, one start bit and two stop bits. The hand-held terminal transmits and receives in a burst mode.

In a recent test of two AN/PSC-1 systems, communication was established over a distance of 9000 miles via the Marisat satellite—which is in stationary orbit 22,300 miles above the earth near West Africa. Two terminals located in Cincinnati talked to each other via the satellite.

---

**Laser scanner finds textile flaws**

One of America's largest textile manufacturers is now using a laser-scanning system to detect and identify flaws in woven goods.

The high-speed fabric inspection system, developed by Ford Aerospace & Communications Corp.'s Western Development Laboratories, Charlotte, NC, is being used at Springs Mills, Inc., Leroy Plant in Fort Lawn, SC.

The system includes three parallel laser-scanning heads, each with a rotating mirror that moves the laser beam across the material. Fiber optics catch light passing through and bouncing off the surface of the cloth.

For scanning, fabric rolls feed through an optical inspection frame. When a flaw or abnormality is detected, a mark is automatically placed on the selvage edge of the fabric.

The output of the laser scanners is correlated by analog and digital-signal processors. A computer readout is provided.

Fabrics can be inspected at speeds up to 250 yards per minute.

---

**Digital data can be transmitted** from soldiers in the field by using a uhf transceiver and a hand-held computer terminal developed by Cincinnati Electronics.
About that 'new' kid on the block...

Actually, he's not that new. He's been around for quite a while now. Other vendors keep announcing miniature cylindrical ceramic capacitor 'innovations', but Sprague Electric, the pioneer in layer-built ceramics, can state with pride that this type of capacitor was introduced by Sprague more than ten years ago.

Sprague Type 292C MONOLYTHIC® Capacitors are the industry's best-constructed axial-lead capacitors, thanks to MFT*, a closely-monitored material modification of electrode metal and ceramic reacted with glass. The result—less capacitance change with temperature change, improved stability with life, and improved impedance with frequency characteristic.

These low-cost miniature capacitors feature a dimensionally-precise molded construction and can be ordered taped and reeled for automatic insertion. They are available in body formulations to meet characteristics ZSU (general-application), X7R (semi-stable), and COG (NPO).


* Modified Formulation Technology

THE BROAD-LINE PRODUCER OF ELECTRONIC PARTS

CIRCLE NUMBER 27
1 You simply set two intensified markers at the desired points using the START and STOP controls.

2 For maximum accuracy, switch to delayed sweep and use the STOP control to overlap the expanded traces.
For improved Δ-time measurements, plus autoranging AC/DC volts, amps and ohms...

HP's the Answer.

Now you can choose from two new scopes with improved Δ-time capability: The 200 MHz 1715A priced at $3000* or the 275 MHz 1725A for $3300*. Both offer an optional built-in DMM for direct Δ-time readout, plus autoranging AC/DC volts, amps, and ohms. Δ-time measurements are now faster with the 1715A and 1725A. They're more accurate because scope and operator errors are significantly reduced. Plus you have switch selection of channel A or B as the starting point for Δ-time measurements, often eliminating the need to move probes and simplifying trace overlap for zeroing. But you can still select conventional delayed sweep with the flip of a switch, for brighter low-rep-rate traces and convenient trace expansion.

The optional autoranging 3½ digit DMM is priced at $325* factory installed. Or, for easy field installation, there's a kit priced at $375*. Another option, HP's "Gold Button" for $150*, gives you pushbutton selection of either time domain or data domain when the 1715A or 1725A is used with HP's 1607A Logic State Analyzer.

Like all new high-frequency HP scopes, the 1715A and 1725A have switch selectable 50 ohm or 1 Megohm inputs. And the 1725A, with 275 MHz bandwidth, is the fastest 1 Megohm-input scope available. That reduces the need for active probes when working with fast logic near maximum fan-out.

The story with both of these scopes is user convenience—from front-panel controls to the minimum of adjustments for servicing. Your local HP field engineer can give you all the details.

And here's something NEW for scopes, HP's Easy-IC Probes. A new idea for probing high-density IC circuits that eliminates shorting hazards, simplifies probe connection to DIPs and generally speeds IC troubleshooting. The probes are standard equipment with these two scopes. *Domestic U.S.A. price only.
Here's our latest addition

For $130

New Compact Portable Model 461
Complete with nickel-cadmium batteries, AC charger/adapter, test leads and instruction manual

- 8 FULL HOURS continuous battery operation... a full day's work without interruption
- 0.25% DC V accuracy
- Large bright 0.3" LED display
- Automatic zero and polarity
- 100V, 0.11µ, 100 nA sensitivity
- 26 pushbutton selected ranges
- High energy fuse safely contained in case
- Folding bench stand
- Only 2 x 5.6 x 4.6"; 1½ lb.

ALL SIMPSON DMM'S HAVE

- Reliable overload-protected LSI circuitry
- Easy-to-read 3½ digit red LED displays with automatic polarity
- Performance proven with a 200-hour burn-in, backed up by a one-year guarantee
- Complete line of accessories is available

For $210

Popular Priced Model 464A
- 0.1% DC V accuracy
- 20 pushbutton ranges including 10A AC/DC
- Bright 0.43" LEDs, automatic zero
- High-impact case with tilt-view adjustable handle
- For AC line operation. Optional AC/rechargeable version available for $247

For $285

Deluxe 460-3A
- 0.1% DC V accuracy, custom MOS/LSI circuitry
- 32 ranges including low power resistance ranges and 10A AC/DC current
- Bright 0.43" LEDs, automatic ZERO
- Calibrated auxiliary analog meter
- For AC line operation. Optional AC/rechargeable version available for $322

For $295

Autoranging Model 465A
- Automatically selects and displays the proper measuring range
- High 0.1% DC V accuracy, custom MOS/LSI circuitry, 0.43" LEDs
- Measures DC voltage to 1000 V, AC voltage to 600 V, resistance to 20 megohms, low power ohms ranges AC/DC current to 10A
- AC line operation. Optional AC/rechargeable version available for $332

For $257

Digital VOM — the 360-2
- AC line and rechargeable operation standard
- 0.25% DC V accuracy exclusive MOS/LSI circuitry, automatic zero
- 29 ranges including low power resistance
- Calibrated zero center analog meter
- Recorder output

CHOOSE THE ONE THAT'S BEST FOR YOU

AT YOUR LOCAL ELECTRONICS DISTRIBUTOR

SIMPSON ELECTRIC COMPANY
853 Dundee Avenue, Elgin, Illinois 60120
(312) 697-2260 • Cable SIMELCO • Telex 72-2416

CIRCLE NUMBER 29

INDUSTRIAL EQUIPMENT GROUP
If you’re designing with the TL081 series, you made the right choice!

TL081 PRICE CURVE

<table>
<thead>
<tr>
<th>Price (100 pieces)</th>
<th>July, 1977</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0.52</td>
<td></td>
</tr>
<tr>
<td>$0.33</td>
<td></td>
</tr>
</tbody>
</table>

ALL FIVE POPULAR OP AMP PINOUTS

- **TL080-Single**
- **TL081-Single**
- **TL082-Dual**
- **TL083-Dual**
- **TL084-Quad**

BIFET op amps from Texas Instruments. Now priced to replace bipolar.

By designing with the TL081 Series, you’re using the first BIFET op amps priced to replace such widely used bipolar as the µA741, MC1458, LM308, LM324, µA747, RC4558 and the RC4136. They’re now priced as low as 33 cents each for 100 pieces. And look what you’re getting for your money! You’re getting tomorrow’s technology for today’s products. High-impedance JFET inputs and a low-distortion bipolar output backed by ion implant reliability that ensures uniform device characteristics. The TL081 Series simplicity, small chip size and ease of manufacturing result in low cost for you.

The TL081 Series gives you two singles, two duals and a quad with the broadest selection offered in operational amplifiers. Five devices with identical specifications that allow you to standardize virtually all of your op amp requirements in just one family, the TL081 Series from Texas Instruments.

- Input bias current — 0.4 nA max.
- Input offset voltage — 15 mV max.
- Unity gain bandwidth — 3 MHz
- Slew rate — 12 V/µs
- Ic / per op amp — 2.8 mA max.

And there’s more! You’re also getting the benefit of TI’s long experience in plastic packaging. The same experience, the same plastic, the same outstanding performance TI has instilled in hundreds of millions of Linear, TTL and MOS products.

BIFET op amps in a proven plastic package at a price on par with bipolar op amps. They’re on the shelf now, waiting for you at TI or your local authorized TI distributor.

Mail the coupon below for your free copy of the BIFET op amp brochure that provides a complete description of the TL081 Series including data sheets, applications circuits, comparative specifications and price information. It’s yours for the asking.

**FREE BROCHURE**

**BIFET OP AMP Family from Texas Instruments**

- Schematics
- Specification comparisons
- Ordering information
- Data sheets
- Application circuits
- Price information

Texas Instruments Incorporated
Inquiry Answering Service
P.O. Box 5012, M/S 308
Dallas, Texas 75222

Please send my free copy of the TI BIFET op amp brochure.

Name ____________________________ Title ____________________________

Company ____________________________

Address ____________________________

City ____________________________ State ________________________ Zip ____________________________
You've designed, debugged, and loaded your system software. Now you need several powerful capabilities to ensure trouble-free execution on the prototype: the ability to look at data in different ways... to compare known good data with new data quickly and easily... to analyze both system and peripheral-interface timing.

The TEKTRONIX 7D01F Logic Analyzer offers you all those capabilities in a single instrument.

**Troubleshooting a microprocessor-based system is easier...**

Look at data in different ways.

The 7D01F lets you choose from five display modes: maps; state tables in hexadecimal, binary, or octal code; or timing diagrams. How often have you encountered a problem you knew you could spot just by scanning overall program flow? How often have you wished you could compare state tables in the hexadecimal code you work with as well as the binary code your microprocessor knows? How often have you wanted to switch from a state table display to its corresponding timing diagram? The 7D01F can help at each step of this troubleshooting procedure.
Compare known good data with new data.
The 7D01F features two comparison modes which facilitate in-depth software/hardware debugging. The EXCLUSIVE-OR and RESET-IF modes speed up what would otherwise be a very tedious process: checking the program flow chart against what falls out when the program is run.

For an EXCLUSIVE-OR comparison, simply verify known good data, store it in reference memory; acquire new data, and select a table comparison mode. The reference table and the compared table (which may be in hex, octal, or binary) will be displayed side by side, and the differences between the two will be highlighted for ready identification.

Use RESET-IF to track down an intermittent fault. In this mode the 7D01F can automatically acquire and compare up to 4096 bits of new data to 4096 bits of reference data. Data is continually reacquired until a mismatch occurs. If there is a mismatch, the instrument holds the display, highlights the differences, and displays the number of resets that occurred. This frees the operator from continually monitoring for wandering programs, intermittent loops, or ragged-edge timing problems.

Analyze system and interface timing.
The 7D01F offers synchronous data acquisition at speeds up to 50 MHz. But it is sometimes necessary to view microprocessor operation with increased timing resolution, as well as to locate timing discrepancies in the system's interface with the outside world. You may, for example, need to asynchronously examine data coming into the I/O port before you can determine whether incorrect information is coming from the I/O port itself or the hardware on the other side. The 7D01F offers asynchronous data acquisition at sample intervals of up to 100 MHz.

...with the Tektronix 7D01F Logic Analyzer.

All these unique features are available only in the TEKTRONIX Logic Analyzer. To find out more about how the 7D01F can simplify your work with microprocessor-based systems, just call your local Tektronix Field Engineer. He'll demonstrate the 7D01F in your application, and acquaint you with its many other features, including 16-channel word recognition, 1M1/5 pf logic probes, 16-channel data acquisition, 4k formattable memory, and 7000-Series mainframe compatibility.

You should also send for our newest application note, describing in detail how a 7D01F can be used with microprocessor-based systems. Write Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077. In Europe, write Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.
Kepco’s new SN-488 digital interface provides you with a convenient way to put our programmable power supplies on your General Purpose Interface bus. The model SN-488 responds to the “listen” instruction, provides the “handshake” interaction and gives you two addressable channels on each card. Up to eight cards can be addressed through a single bus connector.

Each channel provides 12 bits resolution with programmable range (10:1) and programmable polarity (for use with bipolar power supplies). Kepco makes hundreds of power supplies that can listen on your bus through the SN-488 interface: fast models, slow models, high voltage and low; unipolar, bipolar, voltage stabilizers and current stabilizers... power supplies designed for today’s automatic test equipment.
Washington report

ASPJ may be biggest-ever ECM procurement

The Navy plans to issue requests for proposals in October for what may be the biggest procurement of electronic countermeasures in military history.

The program is the Airborne Self-Protection Jammer (ASPJ), and potential contractors are forming teams to submit bids. Slated for 800 planned F-18 and A-18 Navy fighters at an estimated cost production of $300,000 each, ASPJ represents at least $250-million worth of business.

The system also may be retrofitted into as many as 500 F-14 fighters as well as some A-6 attack aircraft—both used by the Navy and Marine Corps—and is a candidate for the Air Force's new F-16 fighter. The Air Force plans to buy more than 1300 F-16s for its own use, while 650 F-16s have been ordered by four European countries.

Teams will submit common designs, but will split the procurement based on annual competitive price proposals. Teams already formed include ITT Avionics and Westinghouse Defense Electronic Systems Center, Sanders Associates Electronic Warfare Div., Northrop Defense Systems Div., and Raytheon with its recently acquired Kuras-Alteman subsidiary and Loral Electronics.

Tomahawk, ASALM to get B-1 funds

The Navy's Tomahawk cruise missile was the major recipient of the money made available from the cancellation of the B-1 bomber, but the Pentagon is also seeking funds to begin developing a supersonic Air Force cruise missile. An amended budget request sent to Congress by Defense Secretary Harold Brown asked permission to redirect part of the $1.4-billion already sought for five B-1 bombers for fiscal 1978. About $380-million would be shifted to cruise missiles and other weapons while $1-billion would be subtracted from the fiscal 1978 budget.

Tomahawk would get an extra $103-million for development of a version that can be launched from a B-52 bomber, and $64-million for initial production. But hidden in the Pentagon's amended budget request under an item labeled "strategic bomber penetration" is $14-million to accelerate testing of a supersonic cruise missile, the Advanced Strategic Air Launched Missile. Another $90-million is earmarked for a new cruise missile-carrying aircraft, probably a version of the Boeing 747 or some other wide-bodied jet.

Meanwhile, the Air Force canceled a new Short Range Attack Missile, the SRAM-B, which was being developed by Boeing for the B-1.

Seasat-A users won't get digital data

The National Aeronautics and Space Administration (NASA) plans to supply users of the Seasat-A environmental satellite with optical processed film rather than digital data from the satellite's synthetic-aperture radar. As a result, information is likely to be more costly and harder to use. The film will not be fully corrected geometrically or radiometrically.

These films will be provided in strips covering 30 to 50 km of the radar's 100-km swath, and the users will have to match them up to create photo mosaics.
Digital outputs would have covered the whole swath.

The step was taken to save $2-million after NASA discovered it had overspent the $66.5-million budgeted for Seasat-A by $2.2-million.

The cost overrun was caused, according to NASA, by changes required by the Air Force to make the satellite compatible with the Atlas-Agena launch vehicle, which the Air Force will use to launch Seasat-A for NASA in May, 1978.

**Navy uses MLS to land jet fighter**

The Navy has successfully landed one of its high-performance fighter aircraft fully automatically with the Bendix narrowband microwave landing system (MLS). The device from Texas Instruments incorporates L-band distance-measuring equipment.

The MLS picked up the aircraft seven miles from touchdown and guided it straight down the glide path for an automated landing. The test was conducted at the Federal Aviation Administration's National Aviation Facilities Experimental Center (NAFEC), Atlantic City, NJ, and involved an F-4J from the Naval Air Test Center, Patuxent River, MD, piloted by Lt. James O. Ellis.

Further tests are planned for the MLS in November at the Navy's own instrumented range at Crow's Landing, CA. These tests, to be conducted jointly with the Ames Research Center of the National Aeronautics and Space Administration, will involve curved and segmented approaches that will require digital computers instead of the present hybrid analog-digital systems.

**U.S. overseas arms-sale backlog skyrocket**

The U.S. backlog of foreign military sales (FMS) orders is now more than $30-billion, according to a State Department report required by Congress, and includes weapons to be delivered as late as 1982. As a result, the U.S. will have to honor these commitments, and any changes in U.S. arms-sales policies should focus on new requests, contends Secretary of State Cyrus Vance.

Among the proposals currently before Congress are limiting annual FMS to $8.5-million (in 1975 dollars), holding next year's sales to 40% below this year's level, and cutting sales by 10% each year for the next four years.

U.S. arms sales abroad are declining anyway. From a peak of nearly $11-billion in 1974, they have fallen below $9-billion. An additional $1-billion a year, handled by individual American companies working directly with foreign governments, doesn't go through the Pentagon's FMS machinery.

The report stressed that U.S. cutbacks might not affect the global-weapons trade. Other suppliers might leap in to fill the void—even though they cannot offer the variety and advanced technology of U.S. weapons. France, Britain, Israel, West Germany, Italy, Belgium, the Soviet Union and Sweden were cited.

**Capital Capsules:** The Royal Australian Air Force will be in the market for **$22-million worth of Barnes and Fairchild serial cameras** to outfit four of its F-111C fighters for reconnaissance missions. The cameras are currently used on U.S. RF-4Cs. ...The Air Force for the first time has had two of its **Big Bird reconnaissance satellites operating in orbit at the same time.** The first, launched last Dec. 19, has established a new longevity record. It was joined by a second on June 27. The Air Force is operating the satellites in higher orbits (up to 530 km), which suggests that more powerful cameras may be operational. ...Final information requests to the two competitors in the Air Force's Advanced Nodium STOL Transport (AMST) program, the Boeing YC-14 and the McDonnell Douglas YC-15, are now scheduled to be sent out in late August. One will be selected to be a cargo aircraft employing advanced avionics. The solicitations were originally planned for June.

48 ELECTRONIC DESIGN 17, August 16, 1977
WIN A TENNIS VACATION IN HAWAII

or other valuable prizes
25 SECOND PRIZES
Wilson T-2000 metal racquet plus cover, or choose the Wilson Kramer or Evert autograph racquet. (Winners will be able to select their grip size and weight when notified).

40 THIRD PRIZES
Wilson tennis bags made of tough vinyl. These bags feature two outside racquet pockets and inside zippered "wet" pocket for damp clothing. (Winners can select from four colors when notified).

400 FOURTH PRIZES
Wilson optic yellow tennis balls. 3 balls per can.

THE MONSANTO TENNIS SWEETSTAKES

GRAND PRIZE
6 nights at the Royal Lahaina Hotel at the beautiful Kaahana Beach Resort, Maui, Hawaii, for 2. Prize includes round-trip coach air transportation from the U.S. mainland to Hawaii; transportation between the Honolulu Airport and Royal Lahaina Hotel also included. Modified American plan (includes double room and 2 meals per day), local sight seeing trip, and tennis lessons at your option.

TOTAL VALUE OF PRIZES IS $4,800.
IT'S EASY TO WIN.
Check over our quality products and fill out the R.F.Q. on the back.

DISPLAYS

<table>
<thead>
<tr>
<th>DIGIT SIZE</th>
<th>DESCRIPTION*</th>
<th>COLOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3&quot;</td>
<td>CA; RHDP</td>
<td>MAN71A MAN3610A MAN81A MAN51A</td>
</tr>
<tr>
<td></td>
<td>CA; LHDP</td>
<td>MAN72A MAN3620A MAN82A MAN52A</td>
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<td>CA; RHDP; (+1)</td>
<td>MAN73A MAN3630A MAN83A MAN53A</td>
</tr>
<tr>
<td></td>
<td>CA; RHDP</td>
<td>MAN74A MAN3640A MAN84A MAN54A</td>
</tr>
<tr>
<td>2 Digit; CA; RHDP</td>
<td>MAN6710</td>
<td>MAN6610</td>
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<tr>
<td>.350&quot;</td>
<td>5 x 7 (35 dot) Alpha-numeric</td>
<td>MAN2A</td>
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</table>

*CA = Common Anode; CC = Common Cathode; RHDP = Rt. Hand Decimal; LHDP = Left Hand Decimal

FEATURED

- 0.5" Double Digits (MAN6710 or orange MAN6640)
- Matching single digits also available

DISCRETE LAMPS

<table>
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<tr>
<th>SIZE</th>
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<th>COLOR</th>
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<tbody>
<tr>
<td>Rectangular</td>
<td>Rectangular legend lamp</td>
<td>MV57124 TO BE ANNOUNCED</td>
</tr>
<tr>
<td>T-1¾&quot; (.2&quot; diam.)</td>
<td>Narrow beam; point source</td>
<td>MV5052 MV5752 MV5152 MV5352 MV5252</td>
</tr>
<tr>
<td></td>
<td>Wide beam; diffused lens</td>
<td>MV5053 MV5753 MV5153 MV5353 MV5253</td>
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<tr>
<td></td>
<td>Narrow beam; diffused lens</td>
<td>MV5054 MV5754 MV5154 MV5354 MV5254</td>
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<td>.2&quot; lens ht.; .6&quot; lead</td>
<td>MV5074B MV5774B MV5174B MV5374B MV5274B</td>
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<tr>
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<td>.2&quot; lens ht.; 1&quot; lead</td>
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<tr>
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<td>MV5077C MV5777C MV5177C MV5377C MV5277C</td>
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</tbody>
</table>

NEW

• Rectangular legend light (MV57124)
• High Brightness
• Stackable

OPTOISOLATORS

<table>
<thead>
<tr>
<th>MODEL NO.</th>
<th>CURRENT TRANSFER RATIO</th>
<th>SPEED (MAX. t_on, t_off)</th>
<th>U.L. APPROVED ISOLATION VOLTAGE (rms)</th>
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<tr>
<td>CONTROLLED GAIN</td>
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<tr>
<td>MCT271</td>
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<td>7 usec</td>
<td>2500</td>
</tr>
<tr>
<td>MCT272</td>
<td>75-150%</td>
<td>10 usec</td>
<td>2500</td>
</tr>
<tr>
<td>MCT273</td>
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<td>2500</td>
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<tr>
<td>MCT274</td>
<td>225-400%</td>
<td>25 usec</td>
<td>2500</td>
</tr>
<tr>
<td>HIGH VOLTAGE OUTPUT (80 volts)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCT275</td>
<td>70-210%</td>
<td>15 usec</td>
<td>2500</td>
</tr>
<tr>
<td>HIGH SPEED</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCT276</td>
<td>15-60%</td>
<td>2.5 usec</td>
<td>2500</td>
</tr>
<tr>
<td>TTL/TEMP COMPENSATED</td>
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<td></td>
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<tr>
<td>MCT277</td>
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<td>15 usec</td>
<td>1500</td>
</tr>
<tr>
<td>GENERAL PURPOSE</td>
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<tr>
<td>MCT2E</td>
<td>20% MIN.</td>
<td></td>
<td>2500</td>
</tr>
</tbody>
</table>
ENTRY BLANK
Monsanto Request for Quotation

Gentlemen: Please give me your quote on the following Monsanto products and enter my name in the Monsanto Tennis sweepstakes drawing.

<table>
<thead>
<tr>
<th>PART #</th>
<th>DESCRIPTION</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

I don't see the Monsanto part listed that meets my exact specifications. Please give me the nearest Monsanto equivalent part to:

Mfg. Name: __________________ Part #: ____________

Or describe: _______________________________________

2. Gentlemen: Please give me your quote on the following Monsanto products and enter my name in the Monsanto Tennis sweepstakes drawing.

To enter, submit the official entry blank / request for quotation to your Monsanto certified public accountant. Winners will be notified by mail. Entrants can enter restricted by law.

OFFICIAL RULES:

1. To enter, submit the official entry blank / request for quotation to your Monsanto distributor by October 17, 1977. Entry may also be made by sending a letter, postcard or the above entry blank, without a request for quotation, to your Monsanto distributor by October 17, 1977. No purchase is necessary to enter.

2. Winners will be determined by random drawing conducted by an independent certified public accountant. Winners will be notified by mail. Entrants can obtain a list of all prize winners by sending a stamped, self-addressed envelope to Monsanto, Palo Alto, California.

3. Taxes, if any, are the responsibility of the winners. All prizes will be awarded. Prizes are non-refundable and Monsanto is not obligated to offer other prizes of cash in lieu of the prizes specified. Trip must be taken within one year of its award.

4. Sweepstakes is open to residents of the United States, except employees and their families of Monsanto Company, its subsidiaries, affiliates and advertising agencies. Void in Missouri and wherever else prohibited or restricted by law.

NO PURCHASE NECESSARY.

SEND THIS ENTRY BLANK / RFQ TO YOUR MOST CONVENIENT MONSANTO DISTRIBUTOR.

Monsanto DISTRIBUTORS

Alta Electronics, Inc.
2280 South Main Street
Salt Lake City, UT 84115

Avnet Electronics
350 McCormick Avenue
Costa Mesa, CA 92626

Emar Electronics
6777 East 50th Avenue
Comerica City, CO 80022

Hampton/Avnet
1092 W. Washington Blvd.
Culver City, CA 90230

Elmar Electronics
805 Oster Drive N.W.
Huntsville, AL 35805

2615 South 21st Street
Phoenix, AZ 85034

575 E. Middlefield Road
Mountain View, CA 94040

2615 South 21st Street
Phoenix, AZ 85034

Monsanto Request for Quotation

My entry sent to
(dist. name)

Monsanto
3400 Hillview Avenue, Palo Alto, California 94304
Our new series of male and female "D" connectors offer you a cost effective external mass termination cable and connector system second to none. Its uniqueness begins with a one-piece "D" connector package that meets industry standards for size, pin spacing, and contact reliability. With no loose parts to match up, positive cable-to-contact alignment is assured. Conductors are mass terminated in seconds with our standard BLUE MACSTM hand or bench tools. The results? Faster installation, higher reliability.

Contact pins are spaced on .0545" centers — a perfect fit for any standard inter-cabinet "D" type connector application. Our new "D" connectors are designed to mate with standard .050" pitch flat cable as well as our new, improved jacketed cable — the only flexible flat cable engineered specifically for out-of-cabinet use.

The Ansley BLUE MACSTM jacketed cable is U.L. listed for external interconnection of electronic equipment. Electrically, it outperforms standard jacketed twisted pairs in typical I/O applications. And there's no special zipper lock tubing required — reducing the need for an extra cable accessory. Installation is faster, easier. And like all Ansley connectors, you can daisy chain our "D" types anywhere in the cable — along with our DIP socket, card edge, or pc board connectors.

Cable alignment and high contact reliability is assured — because both cable and connector are grooved for absolute alignment. Our patented TULIP™ 4-point insulation-displacing contacts are permanently fixed and sealed-in to provide a reliable, gas-tight, corrosion-free mass termination.

For the full reliability/cost effectiveness story and technical data, call or write:

T&B/Ashley Corporation • Subsidiary of Thomas & Betts Corporation
3208 Humboldt St. • Los Angeles, CA 90031 • Tel. (213) 223-2331 • TWX 910-321-3938

Available through authorized Ansley distributors
In Canada: T&B/Ashley, Ltd.
700 Thomas Ave., Industrial Park
Iberville, P.Q.
When the output of a 555 timer switches high, a large current spike is generated which can drag down your power supply and upset your flip-flops. One way to cure it is with several hundred μF of capacitance. But that’s awkward and space-consuming. Teledyne’s new 355 timer is a better way.

The 355 Timer is a pin-for-pin substitute for the 555. It is part of Teledyne’s High Noise Immunity Logic (HiNIL) family. It, too, generates a current spike — but only on the order of 1 mA, as compared to 300 mA for the 555.

Two other problems encountered with the 555 are a potential failure to reset on command, and a tendency to exceed the power dissipation ratings when running at 15V. The Teledyne 355 is designed specifically to answer these two potential problems as well.

If you’d like full technical information on our new 355 Timer — or any other members of the Teledyne HiNIL family of logic — call us at (415) 968-9241, or contact your local Teledyne Semiconductor distributor.
The man who was wrong

Charlie and Joe were both strong executives. Both knew how to make decisions—even tough ones. They would assemble available background data, knowing that they would frequently lack some of the information they'd want. And they'd decide.

Then, each in his own way, they would move ahead to implement the decision. And each would march ahead as if there were 100% certainty that the correct decision had been made. Well, maybe 95% in Charlie's case.

Charlie knew he wasn't perfect. So he always left some room to maneuver out of his position if he found he had erred. In those cases—there weren't many—when he felt he had made the wrong decision, he would admit it. And here's where Charlie and Joe differed. For Joe was never wrong.

If any of Joe's decisions ran into a snag, he'd know why. "My decision was right," he'd point out. "The problem is that our engineers can't get the hang of designing out some of the bugs. And the sales guys aren't selling it right." So Joe would spend his efforts trying to get his engineering and sales people straightened out. That was always the problem—never the decision.

Charlie, in contrast, would freely confess: "I was wrong. That's why things ain't working right. Let's see how we can get back on the right course." And he'd devote his efforts to fixing the results of his off-target decision.

Some people feel that Joe was the stronger leader. Once he chose a course, he never wavered. But I'll put my money on the guy who's wrong sometimes—if he knows how to admit it. It's true that Charlie changed course once in a while. And it's true he occasionally hesitated. So he'd sometimes get to a goal somewhat slower than Joe did. But almost invariably Charlie got to the goal.
1. MICROPROCESSORS: New Directions for Designers by Edward A. Torrero, #5777-6, paper, 1975, 144 pp., 8½ x 11, illus., $10.95.

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3. FUNDAMENTALS AND APPLICATIONS OF DIGITAL LOGIC CIRCUITS by Sol Libes, #5505-6, paper, ($6.95), #5506-4, cloth, ($9.95), 1975, 192 pp., 6 x 9, illus.

4. COMPUTERS IN ACTION: How Computers Work by Donald D. Spencer, #5861-6, paper, 1974, 160 pp., 6 x 9, illus., $5.50.

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6. PROGRAMMING PROVERBS by Henry F. Ledgard, #5522-6, paper, 1975, 144 pp., 6 x 9, illus., $6.50.

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A ravenous appetite for bit storage has propelled semiconductor memories so far along that each new product generation doubles and redoubles its bit density. And this creates problems.

Manufacturers, eager to be the first on their block to announce yet another round of increased density, have developed a reputation for jumping the gun. To further complicate matters, it's not at all apparent which manufacturer's parts can be substituted for another's: A device that is second-sourced means only that there is another manufacturer who can supply a part with a similar function and pinout—but not necessarily the same performance.

The onus of true alternate sourcing is on you. You've got to nit-pick the specs to determine if you can safely swap one part for another. Not easy.

Try selecting a 4096 x 1-bit dynamic MOS RAM:

Memory-systems design gets easier and easier, as you go from core to dynamic then static semiconductor RAMs. Dynamic MOS-memory design is no cinch, however—it takes TTL-to-MOS level shifters, output sense amplifiers and a handful of parts to refresh the RAM. Static RAMs at right are the easy way out (Intel).
The advantage of CCD memories over dynamic RAMs is that about 70% of the chip area is used for storage, while dynamic RAMs use less than half. TI’s CCD, the TMS-3064 (a), is organized as an array of 16 shift-register loops, each loop 4096-bits long. Four address pins describe which loop accepts or delivers data (b). Each loop is actually an arrangement of serial-parallel-serial shift registers, in a format of 32 x 128 x 32 bits (c).

One source specifies 39 ac parameters, repeated for each of four different grade parts, plus 13 common dc parameters, six timing diagrams and 22 footnotes. Selecting a MOS RAM means matching all those data to all the alternatives—and not just the “typical” numbers, either.

You’ve got to reckon with both the max and the min values because if you read the fine print, you’ll find that “typical” is specified at room temperature—certainly not a valid condition in the real world, where memory devices sometimes operate hot as a pistol.

The parameter-priority paradox

With so many parameters to weigh, it is far too easy to take a pin-the-tail-on-the-donkey approach to device selection. But by listing the memories’ parameters in order of importance, then comparing numbers, you can avoid feeling like a donkey’s rear end.

Start with the power supply. Unless you’re working on a full-blown mainframe EDP system, or something of that magnitude, you’ll probably want to avoid designing-in a special power supply just for bit storage. Smaller μP-based control systems may not be able to justify the extra 12-V and 5-V supplies. So look for a memory that uses TTL power—just 5 V.

Basically it’s a TTL world, and the memory manufacturers know it; the trend is to provide parts that are compatible with your host system’s power supply. For example, the available 2102-type static RAMs are second-generation 1101s. Unlike the older 1101s, which needed three supplies, the 2102s require only a single 5-V source.

Once you’ve narrowed the field down to single-supply parts, scrutinize the I/O levels and noise-margin specs. Those numbers, too, should conform to the host system. Adding level translators and the like can only complicate matters and leave more room for things to go wrong.

Don’t use typical values—they represent the overall average of a great many pieces and are not

The size of the die directly affects the cost of a semi memory. The original design of this 1024-bit memory from Signetics is shown in the background; it requires 25,000 sq mil of silicon. The present design, shown in the foreground, is only 14,500 sq mil. Data sheets often indicate the die size.
guaranteed by the manufacturer. Also, parts may be screened before shipment, so the average may actually be far away from the typical values stated.

"Min/max limits at worst-case voltages and worst-case temperature are the only responsible way to specify any semiconductor memory," a spokesman for Harris Semiconductor asserts. Some firms, like EM&M Semiconductor, are finally dropping the "typical" column from their data sheets.

**After levels, check performance**

With system power supplies and I/O levels out of the way, dive right into the performance specs. It takes power to move bits quickly, and the manufacturer who supplies rapid access time with low power consumption is offering high performance.

Here, too, you should specify in terms of the host system—a CMOS part may not be as fast as ECL, but it runs cool and might save you a lot of money on power supplies. On the other hand, bipolar devices are high performers that run hot. NMOS parts generally fall in between. Performance costs, so if you don't need the speed, save the money for a year-end bonus.

The Gaussian distribution ensures a spread of access times for any given production lot. After the manufacturing process is complete, semi houses almost always sort out the faster chips from the slower ones; the faster ones, of course, command a premium price.

Lowest performers are often identified with the basic part number, while faster ones get “dash numbers” (part-1, part-2). But there is no standard for such labeling, or binning. Remember that access doesn't start until all the address bits are presented to the chip—so be careful, and deskew the host system to get all the bits nicely lined up in time. Otherwise, you may think the part doesn't conform to the data sheet.

If you're buying many memories, give the vendor your production schedule. He may be able to integrate your requirements with those of another customers', and thereby save you money.

When analyzing input-threshold specs, which are sometimes given in terms of one of the supply voltages, be sure to use the worst-case situation. Output drive should be specified at the more rigorous $V_{CC\min}$. Check the test conditions for load capacitance; for a given access time ($t_{acc}$), less capacitance means less performance.

For timing specs, look at the timing diagrams, and check the reference points. Worst-case evaluation should include 90% of the rising and falling edges on the waveform under consideration.

Some firms will offer you a precalculated power-dissipation parameter. Beware. There are several ways to calculate $P_d$, and you may not be getting the whole picture, especially if the memory is dynamic. It's best to calculate it yourself.

The graphs that often accompany semi-memory specs are to be used for trend projection only. These data, too, are only typical, and any individual part may not agree with the curve.

Some high-volume users write their own data sheets rather than trust published specs. “Rolling your own” avoids that ominous footnote: “Subject to change without notice.” But don’t try to incorporate all the best features of all the manufacturers into one phantasmagorial part. It can’t be done. Like everything else in life, you get a semi memory only by compromising.

**Which package?**

Like most semiconductor products, a memory’s package is important to both design and price. Ceramic
packages are the top of the line. They perform well under the most adverse conditions and often cost as much as the chip inside, sometimes more. The chip fits into a cavity, which is sealed after bonding to protect the die and the bonding wires.

Plastic packages cost much less than the top-of-the-liners. But they're molded, and the plastic strains the die and bonding wires by flowing right over them. It doesn't take much to break a golden wire that is half the size of a blonde hair; consequently, the yields are lower. The ones that don't break are the ones that ship.

Manufacturers go to great lengths to match the plastic's coefficient of expansion to that of the silicon chip and bonding wires, but nothing is ever perfect. If the memory will experience many drastic temperature changes or will require a high degree of reliability, the chances are you can justify the extra cost of a ceramic package. A good compromise is "Cerdip," a modified-ceramic "sandwich" that offers the stability of conventional ceramic at lower cost.

Don't reinvent the wheel

After you've painstakingly picked through the specs for power-supply compatibility, I/O levels, noise margins, power-supply drain, access and cycle times, you will appreciate the opportunity to ignore something—the input leakage current. With MOS memories, leakage is usually not very significant. In practice, the device is either an open or a short.

Once you've narrowed the field to just a few candidates, contact the manufacturers for applications and reliability data—only then will you have covered all the bases. Semi firms put a lot of effort into their app notes, and one note might just have your complete design. Motorola, for example, offers an app note entitled A Non-Volatile Microprocessor Memory Using 4-k NMOS RAM (AN-732A).

Don't be afraid to specify a device that's been around for a long time. Older types, which presumably have their bugs ironed out and their designs optimized, get better yields. And since most manufacturers' specs have had a chance to converge, a pseudo-standardized part can emerge. Also, since they've been designed into a great many OEM products that still enjoy healthy sales volumes, they're not likely to be discontinued.

On the other end of the stick—new memories—watch out for the data sheet that's stamped "PRELIMINARY." That usually means the manufacturer hopes to ship a lot of devices, but right now the part is "being sampled"—a euphemistic way of saying that the producing semi house is sticking its big toe in to see if the market is hot or cold.

Having pored over the specifications, you are ready to select a RAM. Different RAMs have different attributes—and some have special needs.

Move slowly with dynamic RAMs

For example, dynamic RAMs require refreshing, and that can lead to trouble. When you specify a dynamic RAM, be especially careful to consider all the timing details. Watch out for specs that don't, without good reason, include 90% of the transition edges.

Vendors balance density, power and speed, so you can specify a part that optimizes the characteristics most important to you and trade off those you don't need. Another compromise to consider is density vs dollars. The new 16-pin, 16-k parts will soon be cheap enough to compete with the assortment of 4-k devices now available.

If it's a 4-k you're considering, maybe you can
replace it with a 16-k part, pin for pin, level for level and nanosecond for nanosecond. For instance, the chip-select pin—pin 13 in the standard Mostek pinout—becomes A₆ in many of the 16-k devices. With a DIP switch or a jumper, you can design a field-upgradable memory board—just pop out the 4-k, do a little hardware change and pop in the 16-k. Presto! You've increased the board's capacity by four—that is, with 4-k RAMs that allow you to do so.

Desirable features to look for in 16-k RAMs include: page-mode addressing, row-address-strobe refreshing and (long overdue) ±10% power-supply variations. Choose between latched or unlatched outputs and 64 or 128-cycle refresh.

You should understand the difference between Read-Modify-Write cycles and plain old Read cycles and Write cycles. R-M-W is a timing mode that slices nanoseconds off the cycle time. If you expect the software to be doing a lot of file updating (as opposed to number crunching), use R-M-W to access a word, modify all or part of the word, then restore it immediately. You'll design a more efficient machine.

If anything on your data sheet is unclear, don't hesitate to contact the manufacturer. Almost everything on a timing diagram is interrelated, and if you don't completely understand what's going on inside the part, you can't make a valid selection. Besides, once you know one device thoroughly, you'll be able to comprehend all the others.

The standard pinout for the 16-k generation will probably be Mostek's 16-pin arrangement: a power supply in each corner, input and output across from each other, and address bits increasing in significance in a counterclockwise manner. Most likely, the next generation of 16-k memories will see no change in the refresh rate—it will remain one or two ms.

The 16-k generation

Dynamic RAMs—almost always implemented in NMOS—are available in 16, 18, and 22-pin DIPs. Be sure to check out all the manufacturer's types—some may be more readily available than others.

The MK4116 family of 16-k memories from Mostek offers access times down to 150 ns. The company's 4-k × 1 families include the MK4022, 4027, 4096, and 4200, with 200-ns devices over the full commercial temp range of 0 to 70 C.

A 250-ns, 16-k × 1 device from Intel, the 2116, comes in three different tₘₙₖ bins. This industry leader's 2108 is an 8-k × 1 chip with 200-ns access. Intel's 4-k parts include a number of bin selections in the 2104 and 2107 families.

A 16-k × 1 memory from Texas Instruments, the TMS4070, comes in three bins, according to access and cycle times. TI's 4-k line includes the TMS 4030, 4050 and 4060. Another 4 k, the 4051, takes TTL-compatible clocks.

Dynamic RAMs store data in small capacitors. The presence or absence of a charge represents a ONE or a ZERO. Since the capacitor will leak away most of its charge in a few milliseconds, it must be continually refreshed (a). A static RAM is basically an array of flip-flops. One side or the other of each memory cell is "ON" at any time, and this defines whether the cell is storing a ONE or a ZERO. At least four transistors are needed to make a single memory cell. Consequently, static RAMs consume more power and need more chip area (b).

A 16,384-bit dynamic RAM, the MCM-6616, is produced by Motorola in four bins. And for something in a 4096, look into the company's 6604 and 6605. Access times are as low as 150 ns for the 6605.

A 16-k chip offered by Fairchild has the most meaningful designation: F16k. You can get it in three timing bins. Fairchild also makes the only bipolar 4-k dynamic RAM—the 93481C, and it's fast—100 ns from 0 to 70 C.

The quickest 8-k chip anywhere is the 7008-10 with a 150-ns tₘₙₖ. It's from newly merged Intersil/AMS, which also produces a 16 k, the 7116, as well as a good
The column-address strobe (CAS) and the row-address strobe (RAS) appeared around 1974, when linear addressing began to limit the number of addresses in cost-effective 16 and 18-pin packages.

The old 1103, with 1024 × 1 addressable words in an 18-pin package, used 10 precious pins just for address definition. Going to 2-k and then to 4-k addresses would have required 11, and then 12 pins—clearly unacceptable for a part meant to be inexpensive.

CAS and RAS solve the dilemma by splitting the address bits into most and least-significant halves and delivering the bits to the memory in two “waves.” Thus, the number of pins required to define any given address can be cut in half.

With CAS and RAS, up to 65,536 discrete addresses can be described with a mere eight pins. These eight pins describe one of 256 rows—as well as one of 256 columns. (Both row address and column address are internally latched and decoded.) Consequently, only 10 pins—CAS, RAS plus eight more—are necessary, and that is why Intel's 4096 × 1 dynamic MOS RAM (type 2104) needs only a 16-pin DIP, whereas the older, smaller 1103 needed 18 pins.

Multiplexed addressing is one reason that chip density will continue to quadruple, rather than merely double: One more pin devoted to addressing doubles the number of columns, but also doubles the number of rows. So the size of the internal cell matrix can grow by a factor of four.

The 65-k limit of eight address pins will probably be breached by one of two schemes. Adding a ninth address pin will allow for up to 262,144 addressable locations. But adding a third multiplex pin will provide “three-dimensional” addressing, with a whopping 16,777,216 locations in a single package.

TTL RAMs can't go quite as fast as ECLs—they bottom out at about 50 ns. But then, TTLs consume fewer milliwatts than ECLs while covering the same density range.

With one notable exception (Fairchild), the densest bipolar TTL RAMs are made by Signetics (82S110), Fairchild (93415), TI (54 S 314), National (93425), Raytheon (5500), AMD (93415), Intersil (55 S 08), NEC (2205) and Hitachi (2501). These are all 1024 × 1 bits. Fairchild's 4 k, the 93471, is a TTL-compatible static RAM with an eye-popping 55 ns access time. It uses an integrated-injection-logic technique.

At 15 µW/bit, complementary MOS (CMOS) RAMs take the low end of the power scale. CMOS memories are available in 16 to 1024-bit arrays, and in access times from 80 all the way to 1500 ns.

The highest-density CMOS RAMs are made by Harris (6508), RCA (5501), Intersil (6508), Solid State Scientific (5502), AMI (6508), National (74 C 929) and Toshiba (5007). Hughes has recently entered this arena with a 32 × 8 CMOS RAM and two shift registers.

The line between p-channel and n-channel MOS is quite distinct. While the highest-density PMOS RAM is a mere 256 bits, static NMOS RAMs are available from 1024 to 4096 bits. Almost all new designs are being implemented in NMOS.

An NMOS process that promises to provide even denser memories than standard NMOS is the vertical MOS technique developed by American Microsystems. Fabricating the transistors vertically in a V-shaped groove—instead of in a horizontal plane—reduces RAM cell size by almost 50%, yielding a smaller, faster part. The first VMOS product is the AMI S4015-3.
45-ns static RAM, with a chip size of only 4400 square mils—about half that of the Fairchild 93415, a bipolar equivalent of the 1-k × 1 VMOS RAM.

The one on the cover

Today's largest capacity static NMOS RAMs are all organized as either 4 k × 1 or 1 k × 4. (For clarity, those devices with i-k × 4 organization will be indicated in italics: 4 k × 1 will be in normal type.) EM&M Semi's 4402 ties NEC's µPD 410 for the quickest tacc. The former yields its data in 100 ns maximum over 0 to 70 °C—very good performance for a MOS device. The latter is available in three bins. Other 4-k parts from EM&M are the 4104, 4200, 4801 and 4804, each with a number of bin selections.

Intel's recently introduced family of 4-k static RAMs boils down to two basic type numbers with a total of six bin selections. The 2114 comes in an 18-pin DIP; the 2142 features two additional control pins.

Mostek's MK4404 needs only a single 5-V supply. Mostek's other static RAM, the 4104, carries a 200-ns tacc, as does the MK4404. Signetics offers one of each—the 2114 and the 2316.

National's two static RAMs, the 5255 and the 5256 are "nibble" (half-byte) organized. Also, its 5257 4 k is a "X 1." Intersil's 7114 is available in four bins and the 7144 also has 4 grades of tacc.

Nitron has two "X 1" parts—the 4402 and 4200. The 4200 uses only two power supplies, −5 and 12 V. The 4402 is Nitron's 1-k × 4. Another Fairchild memory, the 3245, is nibble-organized.

The fastest (55 ns) 4096-bit static RAMs in the business are in Fairchild's 93470/71 series. Implemented in TTL, the /70 is usable over the full military temperature range of −55 to 125 °C.

General Instrument makes two kinds of NMOS static RAMs—the RA3-4402 and RA3-4200. Advanced Micro Devices offers the 9130 and the 9140 series. The 9145, an unconventional 4-k × 1 NMOS RAM, uses a relatively new technique—clocking—that cuts down on the power consumed. You can consider it a hybrid, falling somewhere between dynamic and static, whose popularity will increase as static devices grow in density. The 9145, in wafer form, is shown on the cover.

A special thanks to the following individuals for their help in organizing the material in this article: Bill Blood, Motorola; Brian Cayton, GI; Richard Florence, CompuCorp; Joe Heesbeen, Macrodata; John Hewkin, TI; Ralph Kaplan, Signetics; Fran Krch, EM&M; John Latham, Rockwell; Harry Masuda, Signetics; Jerry Prioste, Motorola; Bill Regitz, Intel.

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CIRCLE NUMBER 41
Standards for dynamic MOS RAMs are emerging. But among equivalent parts, some are more equal than others. Static-RAM standards lag.

Increasing demands for lower cost, higher bit density, and better performance have caused a proliferation of new semiconductor memories—particularly dynamic MOS RAM chips. But, instead of developing a line of standard parts, manufacturers have devoted most of their efforts to maximizing performance and density—which usually means devices with unique "new" problems that result from not eliminating problems in available families.

Today, available 4-k, n-channel dynamic RAMs include at least five pin-out versions of three different packages, with numerous electrical-specification variations. Yet perhaps 90% of the market needs might have been satisfied with but one standard chip design.

This variety stems largely from the lack of a single part with good enough performance and low-enough cost to command undisputed leadership. Some of the types produced are fast, but draw excessive power and are noise sensitive. Other types offer good PC-board density, but have doubtful manufacturing economies and few alternate sources.

However, as the 16-k RAMs are beginning to appear, standards for dynamic RAMs are also beginning to emerge. In dynamic RAMs, Mostek parts have established a clear technical lead. Their specs have been sufficiently tight to delay alternate sourcing of their parts and even to discourage some companies enough to drop out of the game altogether. In static RAMs, standards are coalescing more painfully. The Mostek MK 4104 will likely set one standard. But the competition of the scaled-up 2102A and the fast Intel parts will prevent a single device standard from emerging.

Who sets the standards?

In the early days, the Intel 1103 was pretty much the standard. Tricky to build and even trickier to use, it was still second-sourced by enough companies to lead the field. With the coming of the 4-k RAM, the Motorola 6605 and the Intel 2107 introduced the 22-pin package (with different pinouts). But Texas Instruments' 22-pin version became the standard, and the Intel 2107A and 2107B followed.

Meanwhile, Mostek pioneered the 16-pin, multiplexed-address part, the MK 4096. With the emergence of the Mostek 4-k MK 4027 in 1976 and the general acceptance of the 16-pin, multiplexed-address concept, 22-pin parts and their 18-pin derivatives became obsolete. One important factor influencing this move was that the 4027, unlike its predecessors—the 4096—used standard silicon-gate processing.

A powerful argument for the 16-pin format is that it can be readily converted to a high-board-density 16-k RAM, by replacing the CS input with an input carrying the two extra address bits. So far, only Mostek (MK 4116) and Intel (2116) have shipped significant quantities. But despite the common pinning there are substantial differences between these seemingly similar memories.

Mostek sets the pace

The Mostek 4116 is setting the standards because of its circuit design (Fig. 1). A combination of high speed and low power requires new approaches to the on-chip peripheral circuits and to the sense amplifiers. Nearly all earlier designs, including the 2216, use sense amplifiers in which load current drawn from \( V_{DD} \) is
traded off for cycle time set by the period needed to pull up a bit-line.

To escape this compromise requires balanced, all-dynamic sense amplifiers. Such circuits are more complex and difficult to lay out. More serious still, are the design problems created by the need for the Y-access circuits to connect both sides of the divided bit line to the read/write circuits when a bit line is selected. If this is not done, an all-dynamic sense amplifier will not allow read-modify-write cycles (see box).

Prior to MK 4027 and MK 4116, only the National

18 and 22-pin parts used balanced all-dynamic sensing. Failure to do so accounts for other companies' first attempts at 16-pin designs winding up with specifications incompatible with either the older 4096 (which uses all-dynamic, but unbalanced, sensing) or the 4027. It now seems certain that all future dynamic-RAM designs must feature all-dynamic sensing to be performance-competitive.

A second key area in dynamic-RAM design in which Mostek sets the pace is the address buffer. Although detecting TTL levels should be a slight problem compared with the correct sensing of less than 10^6 electrons of stored charge in a memory cell, poor address-buffer design has caused many designs to founder. Unfortunately, a poor buffer shows up by its effects on the decoders, and the obscure errors created are very pattern-dependent.

Finally, Mostek is leading the way in shrinking the chip dimensions. A reduction in line widths by x tends to give a speed advantage of x^2 since transistor gains increase by x and gate-capacitance loads diminish by x. A reduction in all linear dimensions achieves similar results, since transistor gains now stay constant and capacitance loads decrease as the square. When the MK 4027 first appeared, it used layout dimensions close to accepted industry standards. But later versions shrank 15%. The MK 4116 has come out in this smaller version from the start, and further size reductions are forecast.

Second sourcing—but how?

A key element in the success of any part is the degree to which it is “second-sourced.” But in memories especially, care must be taken when defining a second source. On the one hand, users can sometimes accept quite different parts, maintaining system compatibility only at the board level. On the other hand, identical parts might be used interchangeably to simplify procurement, testing, spares logistics and maintenance.

Until very recently, this latter option was hardly available. Parts to the same nominal specification usually differed so much in second-order “unwritten spec” parameters that they were not fully interchangeable. The MK 4027 was the first n-channel dynamic RAM to be copied exactly by second-sourcers.

There is a hidden paradox in second-sourcing: While having identical multisourced parts seems ideal, if a design problem emerges in production, all identical second sources will be affected. Some 1103 pioneers were hurt in this way when the now-famous “column disturb” problem was discovered.

So despite the inconvenience, using different designs aimed at the same specifications has its advantages. For example, the new Intel 2104A approach to balanced all-dynamic sensing is totally different from that in the 4027, which it second-sources (Fig. 2). However the differences are minor and can be accommodated by users. But, as always with differing designs, it would be risky to consider the parts entirely interchangeable or intermixable.

Meanwhile, the pin-out for 64-k RAMs has been defined by JEDEC as identical to 16-k parts but with the V_{CC} pin converted over to the eighth-pair of address bits. What is not yet generally agreed is whether V_{DD} stays at 12 V, or is established at 5 V or some other intermediate nonstandard voltage. If V_{DD} is not 5 V, then V_{CC} must be derived internally for the output buffer which can be done readily.

The problem in fixing the V_{DD} level comes from having to reduce line widths and clearances to keep chip size compatible with standard 16-pin package-well dimensions. A 12-V supply bootstrapped internally to 16 V or even 20 V is likely to be incompatible with smaller dimensions. On the other hand, a nominal 5-V V_{DD} will give intolerably small internal voltage margins.

One possible way to increase operating margins is to use two cells per bit, as in the 2104A. This ensures that a stored ONE is always compared with a stored ZERO and vice versa, rather than being compared with an intermediate-reference level. Near-perfect balance can be achieved, too, but only by increasing the silicon area of the chip. However, the increase isn't so great, since the array itself does not double in size,
and is in any case only 30% to 45% of the total chip area. Indeed, the total chip area might actually be reduced if the fabricating technique allows fine line widths and a 5-V $V_{DD}$.

Eliminating the $-V_{BB}$ supply is another way to reduce chip area. An on-chip generator might replace the external supply, as in several present static RAM designs. But the problem with using an on-chip generator for dynamic parts is that large peaks of substrate current occur because of capacitance coupling from the bit lines and other parts of the circuit. To minimize such current spikes calls for either an external decoupling capacitor or still more constraints on the circuit design.

As an intermediate step on the road to the 64 k, 16-k parts may emerge with 5-V-only power requirements. The problems will not be easy to solve, but unless some way is found to exploit advanced fine-line-width processes in dynamic designs then static RAMs, which use them now, will become more attractive than dynamic RAMs in performance and cost.

The future of dynamic RAMs

While 64-k dynamic RAM chips are now being promised, 4-k parts are still being actively developed by the charging current available from the sense-amplifier load. If a dynamic circuit is used to cut off the wasted load current fed to the low side, then a ONE level cannot be written back in.

Thus, the key problem is arranging the Y decoder to give balanced access to both sides of the divided bit line. One method, used in the MK 4116, is to run the decoder up the center of the array along with the sense amplifiers. Another is to fold the bit-line halves parallel to each other, giving access to both halves at either end. This method is used in the NEC $\mu$PD 414D and Intel 2104A, and lends itself to a two-cells-per-bit format.

Why all-dynamic sensing?

The balanced flip-flop sense amplifier, used in all first-generation, balanced, one-transistor-cell RAM designs, gives the classic speed-power trade-off. Current taken by the sense-amplifier loads can be reduced only by increasing the time taken to pull up the 1 pF or so of bit-line capacitance. However, sense time or access time needn't be affected, because bit lines can be precharged high. It is the read-modify-write cycle, in particular, which is extended.

The extension occurs because the Y decoder gives access to only one half of the divided bit-line; and a ZERO read-out from the side remote from this access can be written back in only as a ONE at a rate set by the charging current available from the sense-amplifier load. If a dynamic circuit is used to cut off the wasted load current fed to the low side, then a ONE level cannot be written back in.

Thus, the key problem is arranging the Y decoder to give balanced access to both sides of the divided bit line. One method, used in the MK 4116, is to run the decoder up the center of the array along with the sense amplifiers. Another is to fold the bit-line halves parallel to each other, giving access to both halves at either end. This method is used in the NEC $\mu$PD 414D and Intel 2104A, and lends itself to a two-cells-per-bit format.
to serve the real market. In early 1976, 16-k RAMs before year's end were promised by every supplier. Most have yet to emerge and it still seems reasonable to expect volume availability of multisourced equivalent parts in 1978.

Beyond the 16-k, the crystal ball gets cloudy. The 16-k dynamic RAM is a happy combination of reasonably well-proven processing and well-developed circuit techniques that fit a chip nicely into a standard package, while offering a good balance of performance features. This act will be hard to follow.

Advanced MOS processes at or beyond the limits of optical photolithography will be needed to improve real densities. (A 64-k chip in a larger package will be only a marginal benefit.) Smaller geometries will likely require that the 12-V supply and the still higher bootstrap levels currently used be eliminated. This would match the trend to 5-V-only parts but would create a new set of design problems.

While such difficulties probably will be overcome during this decade, it is also likely that different companies will solve the problems in different ways, and what happened in the early days of 4-k parts will happen again. As a result, acceptance of any one approach would be delayed, and the 16-k would have an unusually long-life—several years at least.

**Outlook for static RAMs**

Right now, a MOS static RAM has more than twice the area of a dynamic RAM, but this ratio may not stay constant if short-channel advanced MOS technologies now emerging in static RAMs can't be applied to dynamic RAMs. Unfortunately, the 4-k static is being standardized in an ad hoc way resembling the early history of the 4-k dynamic RAM. The situation is also complicated by three distinct though overlapping areas of static-RAM use—and a design that is best for one won't necessarily serve another as well.

One area is the replacement of bipolar RAMs in applications requiring access times faster than 50 ns. Such parts use all-static design to match bipolar functions. But they are more difficult to fabricate, and then they require more power than the slower static RAMs. But even with these two drawbacks, these fast static RAMs are likely to be an improvement over bipolar standards.

A second area—microprocessors—has been traditionally served by simple all-static parts like the 2102 and its 4-k successor, the 2114. But this area is now diverging. Since µP systems are nearly always synchronous, it is better to design a static RAM cell with clocked peripheral circuits as in the MK 4104. This largely avoids the speed-power trade-off inherent in the static inclusions of the address buffers and decoders in all-static parts.

Clocked-periphery circuits result in much lower power consumption, which particularly benefits systems with battery back-up and may even allow n-channel MOS to replace CMOS in some applications.

Compounding the variation in circuit techniques is a divergence in package styles and pinnings. An early 4-k static part, the AMD 9130/9140, used a 22-pin package. But later 4-k memory designs are all aimed at 18-pin packages for reduced cost and better board-packing density.

**Process standards**

In the 4-k RAM, several variations of n-channel technology were used. Most were silicon gate processes, but the industry was about evenly divided between “coplanar” processing and “standard” processing, whereby a uniformly grown field oxide is etched to define active device locations. In the former, field oxide is selectively grown and device areas are screened by silicon nitride to inhibit the field-oxide's growth. Coplanar reduces step heights and can save an ion-implant masking step used in controlling field-threshold voltage. On the other hand, coplanar processes have been associated with gate-oxide-quality problems giving “stuck ONEs” and/or refresh failures.

Other variations existed: Some parts used a “buried-contact” masking step to provide direct connection between polysilicon and n-diffused regions. Even “philosophical” differences existed. Some companies used relatively large chips, claiming that relatively generous layout rules increased yields. Others used tight rules to achieve small chip sizes.

At the 16-k level, however, there is more standardization—for now. Silicon-gate coplanar processing is standard. The two layers of polysilicon reduce cell area that doesn't contribute to cell capacitance. A diffused bit line and a metal word line are used in the process. The extra pitch between bit lines allows sense amplifiers to be laid out without a buried-contact masking step.

In addition, relatively tight layout rules are forced on 16-k chip design by the need to ensure that the chip will fit in the well area of a 16-pin package. As a result, the maximum allowable chip width of the 16-k memory is about 145 mil.

**Prices keep tumbling**

This year, 4-k RAMs have become readily available at less than 0.1¢ per bit, which has reduced the cost of memory systems dramatically. By year's end, according to predictions, 16-k RAMs will be at this level. And the 16-k devices are already saving in overhead circuitry and board area, among other things.

However, the same techniques that can lower the 16-k prices might produce still cheaper 4-k parts. A chip area of less than 15,000 mil² on a basic four-mask process with scratch protection should give yields of 150 good chips per wafer or more—provided that the
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Progress in dynamic RAMs, 1973 to the present

<table>
<thead>
<tr>
<th>Mfg.</th>
<th>Part no.</th>
<th>Bits</th>
<th>Pins</th>
<th>Remarks</th>
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<tbody>
<tr>
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<td>TMS 4030</td>
<td>4k</td>
<td>22</td>
<td>1st commercial 1-T cell</td>
</tr>
<tr>
<td>M.I.L.</td>
<td>MF 2107C</td>
<td>4k</td>
<td>22</td>
<td>1st, clocked-source sensing</td>
</tr>
<tr>
<td>Intel</td>
<td>i 2107B</td>
<td>4k</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>T.I.</td>
<td>TMS 4050</td>
<td>4k</td>
<td>18</td>
<td>1st 18-pin part</td>
</tr>
<tr>
<td>T.I.</td>
<td>TMS 4051</td>
<td>4k</td>
<td>18</td>
<td>TTL-level CE clock</td>
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<tr>
<td>T.I.</td>
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<td>4k</td>
<td>22</td>
<td>Re-specified TMS 4030</td>
</tr>
<tr>
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<td>MM 5280</td>
<td>4k</td>
<td>22</td>
<td>1st All-dynamic sensing</td>
</tr>
<tr>
<td>National</td>
<td>MM 5270</td>
<td>4k</td>
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<td>Nonstandard 18-pin</td>
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<td>i 2104</td>
<td>4k</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Motorola</td>
<td>MCM 6604</td>
<td>4k</td>
<td>16</td>
<td></td>
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<tr>
<td>AMD</td>
<td>Am 9060</td>
<td>4k</td>
<td>22</td>
<td>Similar to TMS 4060</td>
</tr>
<tr>
<td>AMD</td>
<td>Am 9050</td>
<td>4k</td>
<td>18</td>
<td>Similar to TMS 4050</td>
</tr>
<tr>
<td>Mostek</td>
<td>MK 4027</td>
<td>4k</td>
<td>16</td>
<td>Leading 4-k part</td>
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<tr>
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<td>i 2104A</td>
<td>4k</td>
<td>16</td>
<td>Mosaid Inc. patents cover these two</td>
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<tr>
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<td>4k</td>
<td>16</td>
<td></td>
</tr>
<tr>
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<td>i 2116</td>
<td>16k</td>
<td>16</td>
<td>1st 16-k RAM</td>
</tr>
<tr>
<td>Mostek</td>
<td>MK 4116</td>
<td>16k</td>
<td>16</td>
<td>Leading 16-k part</td>
</tr>
</tbody>
</table>

Part design and/or spec do not cause significant parametric yield loss. With low-cost assembly, a price in the region of $2 seems attainable.

With most interest centered on 16-k parts, such prices may not materialize. But if they do, then 16-k parts will find it difficult to beat the 4-k price per bit until 1979. As always, price may not follow costs too closely in such a competitive market. At any rate, the pace of RAM development shows no sign of slackening in the near future.

References

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Model RAMs automatically for gate-level logic simulators with RAMGEN. Such a model lets you develop test programs for complex PC boards with ease.

Printed-circuit boards are getting more and more complex as microcomputers employ more ROMs and RAMs for program storage and scratchpad memories. To ensure that such boards will work under all foreseeable logic combinations, tests of ever increasing complexity are needed, forcing you to use logic simulators for their development.

Instead of trying your test plan on the actual PC board, you use a simulator program that applies the tests to a model of the board, and pinpoints areas that need improvement. Naturally, you must supply the computer with a model of every component on the PC board, including RAMs and ROMs.

Modeling of ROMs has already been discussed in ED No. 20, Sept. 27, 1976, p. 88. To automatically model RAMs for use in gate-level logic simulators, you can use a program called RAMGEN.

The program can model any RAM from a minimum of four input address lines, up to a maximum of ten input address lines. It accommodates up to eight output-data lines. But RAMs with 10 input address lines are limited to one output.

Developed for a General Automation SPC 16/45 minicomputer, the program is written in Fortran IV. The output is punched into computer cards so that it can be incorporated into the circuit model.

Models for the Lasar

Gate-level logic simulators have been defined as "describing the system by a collection of gates and their interconnections." The simulator output not only summarizes the thoroughness of the test pattern, but also pinpoints timing problems that may exist on the PC board. One gate-level logic simulator, the D-Lasar by Digitest is widely used for both commercial and military systems. It uses NAND, AND, OR, and Wired-OR gates, and flip-flops as building blocks for more complex functions.

RAMGEN generates NAND-gate models of RAMs in D-Lasar format, which has the general form XXXCC/I1, I2, ..., I n/O1, O2, ..., O n, where XXX is the

James J. Hanratty, Electronic Engineer, Automatic Test Equipment Engineering Div., Naval Air Rework Facility, Alameda, CA 94501.
In the D-Lasar, the memory cells are interconnected by data (in and out), address, read and write lines. CC is the component name, \( I_n \) are the component inputs, and \( O_n \) are the component outputs.²

To model a RAM you must know its basic operation and configuration (Fig. 1). Every RAM has input address lines, data input lines, control inputs, and data output lines. A memory plane contains memory cells which store the data bits. An input-address decoder directs a read or write request to the desired memory location.

To write into the RAM, the data are placed on the data-input lines. Then the address of the desired memory location is placed on the input-address lines. Finally, the write-control line is brought to the appropriate voltage level.

To read data from the RAM, the address of the desired memory location is placed on the input-address lines, the read-control line is brought to the appropriate voltage level, and the data are read on the RAM output data lines.

Putting it all together

As the flow chart of RAMGEN (Fig. 2) shows, the program sequentially generates models for the RAM's basic parts: the input address decoder, the memory plane, and the memory cell. Then all of these models are combined to model the RAM.

The memory cell model must provide the basic control functions—read, write, address, and data input—and exhibit memory. The NAND-gate model and D-Lasar description in Fig. 3 fulfill the memory-cell functions required.

The model provides memory with cross-coupled NANDs, and has inputs for all control functions. This memory cell is designated component BC. Component AD is the input-address decoder (Fig. 4). It is modeled as an m-to-n decoder where m is the number of inputs and n equals \( 2^m \).

The next model in the flow chart simulates the memory plane, which is a collection of memory cells. The memory plane, MP, consists of 16 memory cells (Fig. 5) whose data, read, write, and column address lines are tied together, as are the data output lines. The RAM-model component, RM, incorporates all of these models.

RAMGEN uses two basic RAM configurations (Fig. 6)—one for RAMs with four to nine inputs, and one to eight outputs, the other for RAMs with 10 inputs and one output. The general model generated by RAMGEN requires some additional gating to represent any specific RAM exactly. The basic model becomes a component in the final RAM model, which
5. A memory-plane model reserves 16 lines for the row address, one for the column address, one for data output, and three for control.

6. In an m x n RAM (top), the model has m input lines and n output lines. A different model is used for a 10 x 1 RAM (bottom).

7. The RAMGEN input consists of one card—all that's required is the number of inputs and outputs.

8. The RAM-model printout identifies inputs and outputs for all the submodels as well as for the whole RAM.

References

Electronic Design 17, August 16, 1977
RAMGEN program listing

IMPLICIT INTEGER(*,*)
DIMENSION BUFFER(1:10), TEMP(1:10)
DATA A=9.4E-10,
   B=1.1E-10,
   C=1.3E-10,
   D=1.5E-10,
   E=1.7E-10,
   F=1.9E-10,
   G=9.4E-10,
   H=1.1E-10,
   I=1.3E-10,
   J=1.5E-10,
   K=1.7E-10,
   L=1.9E-10,
   M=1.1E-10,
   N=1.3E-10,
   O=1.5E-10,
   P=1.7E-10,
   Q=1.9E-10,
   R=9.4E-10,
   S=1.1E-10,
   T=1.3E-10,
   U=1.5E-10,
   V=1.7E-10,
   W=1.9E-10,
   X=1.1E-10,
   Y=1.3E-10,
   Z=1.5E-10,
   DATA R=9.4E-10,
   S=1.1E-10,
   T=1.3E-10,
   U=1.5E-10,
   V=1.7E-10,
   W=1.9E-10,
   X=1.1E-10,
   Y=1.3E-10,
   Z=1.5E-10,
   READ(13). I=NO
1 FORMAT(2X)
2 FORMAT(*, 'ADD BIT CELL / *', 'NAME='1*'), 'MODEL'/
3 WRITE(5,2)
4 WRITE(5,2) BUFFER(1:12)
5 WRITE(5,2) BUFFER(1:12)
6 WRITE(5,2) BUFFER(1:12)
7 WRITE(5,2) BUFFER(1:12)
8 WRITE(5,2) BUFFER(1:12)
9 WRITE(5,2) BUFFER(1:12)
10 WRITE(5,2) BUFFER(1:12)
11 WRITE(5,2) BUFFER(1:12)
12 WRITE(5,2) BUFFER(1:12)
13 WRITE(5,2) BUFFER(1:12)
14 WRITE(5,2) BUFFER(1:12)
15 WRITE(5,2) BUFFER(1:12)
16 WRITE(5,2) BUFFER(1:12)
17 WRITE(5,2) BUFFER(1:12)
18 CONTINUE
19 END
20 CONTINUE
21 END
22 CONTINUE
23 CONTINUE
24 CONTINUE
25 CONTINUE
26 CONTINUE
27 CONTINUE
28 CONTINUE
29 CONTINUE
30 CONTINUE
31 CONTINUE
32 CONTINUE
33 CONTINUE
34 CONTINUE
35 CONTINUE
36 CONTINUE
37 START
38 START
39 START
40 START
41 START
42 START
43 START
44 START
45 START
46 START
(continued on page 76)
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Besides scintillation counting, the teacup PMT can also be useful in gamma ray spectroscopy for medical applications. Several leading manufacturers of medical diagnostic equipment recently conducted their own tests on these gamma-camera type tubes, and pronounced them a giant step forward in improving camera performance.

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Predict a 4-k RAM's average $I_{DD}$ with a few simple calculations. The method accounts for both the transient and steady-state components.

When working with 4-k NMOS RAMs, you can accurately predict the average $I_{DD}$ under any timing conditions and at any operating frequency. All you have to do is specify an average $I_{DD}$ at one defined frequency and clock-duty cycle, then specify the dc components of $I_{DD}$ for the various clock-signal logic states. The results for any $I_{DD}$ follow. You can also calculate the worst-case $I_{DD}$ for any frequency and clock-timing arrangement.

During the dynamic operation of 4-k RAMs, you must consider both the ac and dc components of $I_{DD}$. The former component stems from transient currents associated with signal edges, and the latter from signal-logic levels. The two components differ in that the ac is unrelated to clock durations and results from the charge or discharge of capacitive nodes or current-spiking caused by signal-transition timing conditions.

The current-time integral of the transient currents is constant over one memory cycle. Therefore, the average magnitude of this component over many cycles is directly related to frequency.

**Looking at the dc component**

The steady component flows in dc paths that are switched on by clock-logic levels during normal operation. Since the 4-k RAM is dynamic, you can't observe the dc currents by applying steady voltage levels, nor can you generate or sustain the charge necessary to turn on or access a dc path under static dc conditions.

However, you can observe the dc currents by extending the clock signals' duration several microseconds to allow the transient currents to disappear, and thus display only the steady-state values of current resulting from the various clock-logic states.

If the RAS and CAS clocks are so extended, and also offset in time, you can observe the $I_{DD}$ dc components for each of the four logic-state combinations of the signals. When you look at the currents for 16-pin, 4-k RAMs from five different vendors, you'll find that each has a unique profile of $I_{DD}$ magnitudes; the worst-case $I_{DD}$ current for the different types occurs at different logic-state combinations of RAS and CAS. Thus, you must specify a maximum current for all combinations.

The specification writer may choose to make the maximum current the same for all logic combinations, but you should place a limit on the spec to guard against excessive dc components. And you should measure the $I_{DD}$ currents for all four logic states (at least initially) to determine the worst case in a particular design.

**Calculating the ac component**

The ac component is not easy to measure directly, but you can calculate it, knowing the dc value and the average $I_{DD}$. This calculation is possible since the average $I_{DD}$ is the sum of the dc and ac components.

First, define the four steady-state values of $I_{DD}$ occurring during extended clock durations, but with a clock repetition rate that provides a cycle interval no longer than the refresh period. Measure the following:

- $I_{DD1}$ with RAS false and CAS false.
- $I_{DD2}$ with RAS true and CAS true.
- $I_{DD3}$ with RAS true and CAS false.
- $I_{DD4}$ with RAS false and CAS true.

The last factor needed to calculate the ac component is the average $I_{DD}$. It can be theoretically measured at any frequency and clock duty factor, although the accuracy of the resulting ac calculation increases at higher frequencies, since the ac component gets larger.

Now you can calculate the ac component:

$$I_{DD(ac)} = I_{DD(avg)} - I_{DD(dc)};$$

$$I_{DD(ac)} = I_{DD(avg)} - \frac{I_{DD1}T_1 + I_{DD2}T_2 + I_{DD3}T_3 + I_{DD4}T_4}{T_1 + T_2 + T_3 + T_4},$$

where $T_1$, $T_3$, $T_1$, and $T_4$ must agree with the respective times for the $I_{DD(avg)}$ measurements (Fig. 4).

The $T_{CYC}$ interval for the measurement of $I_{DD}$ average should approximate a normal memory cycle (500 ns or less), and the values for $T_1$, $T_2$, $T_3$, and $T_4$ should be proportionally short. Remember that...
measurements of $I_{DD1}$, $I_{DD2}$, $I_{DD3}$, and $I_{DD4}$ should be made at an extended cycle.

By specifying the average $I_{DD}$ at stated conditions of cycle interval and clock timing and, in addition, by specifying $I_{DD1}$, $I_{DD2}$, $I_{DD3}$, and $I_{DD4}$, you can calculate the ac component for the defined cycle time. Moreover, you can calculate the average $I_{DD}$ for any cycle time and clock duty factor. Simply multiply the ac component at the known frequency by the proportionality factor between that frequency and the frequency of interest. This method is valid since the ac component is directly proportional to the frequency and is independent of the clock duty cycle.

You can calculate the dc component from the known values for $I_{DD1}$, $I_{DD2}$, $I_{DD3}$, $I_{DD4}$ and the respective clock duty factors. The calculated average $I_{DD}$, then, is the sum of the calculated components, $I_{DD(ac)}$ and $I_{DD(dc)}$.■
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See our catalog in EEM, page 1056.
How to operate your MPUs at 2x their rated power... or 1/2 their case temperature.

Unique new Micro-Clip heat sinks permit MPU operation in much hotter environments

Time was when microprocessors posed no thermal problems for designers. That's because earlier MPUs required very little power — up to 250 mw or maybe ½ watt at most. Then, too, designers usually spec'd only one to a circuit board. Surrounded by plenty of air, the lonely MPU did its job without generating much heat. So nobody worried much about heat dissipation.

Today's reality: serious MPU thermal problems

Today, designers are specing many MPUs on the same board. And these boards often must operate in military-type environments where ambient temperatures reach 71°C. Also, today's MPUs do more and, therefore, generate much more heat than earlier models. For example, they often function as both the arithmetic logic unit and the control section of a computer. These factors combine to cause serious thermal problems. Coping with these problems has become an increasingly important part of a circuit designer's job.

IERC finds efficient solution

To solve growing MPU thermal problems, IERC recently introduced its two-piece "Micro-Clip" series of heat dissipators. These units adjust to fit all double DIP, CMOS, MOS-FET, and microprocessor packages within the 20- to 40-pin range.

As the adjacent drawing shows, the Micro-Clip's unique spring-finger design lets the dissipator make good, solid contact with both the top and bottom of the MPU, assuring efficient heat transfer from case to dissipator. Tests show these units dissipate up to 100 percent more heat than conventional glued-down devices.

Staggered-finger design also assures more efficient heat dissipation

Micro-Clip series dissipators capitalize on IERC's patented staggered finger design. Heat radiates to the ambient, never transfers from one finger to another. In forced air modes, the staggered fingers maximize turbulence, further increasing heat transfer efficiency. Three finger heights are available — ¼ in., ½ in., and ¾ in. — to meet varying space and dissipation requirements. Micro-Clip dissipators weigh only 4 grams and require only .6 in.² more board space than the IC device itself. So board densities and spacing between rows of, for example, double DIPs and CMOSs are unaffected.

Stocking problems greatly reduced

Designed to (1) meet an infinite number of application needs and (2) fit an entire range of package sizes, Micro-Clip dissipators greatly simplify a user's stocking problems. This benefit appeals especially to companies with high-volume manufacturing operations.

Easy to attach

Only two screws or rivets or dots of thermally conductive epoxy are needed to fasten Micro-Clip dissipators securely into position. Mounting Micro-Clip units to MPUs already mounted to boards requires no disassembly.


IERC Heat Sinks/Dissipators

ELECTRONIC DESIGN 17, August 16, 1977
Cut your processor's computation time by storing information in tables. Accessing a table can take less time than doing an algorithm but you'll use memory space.

Tables can speed microprocessor operations such as converting codes, doing look-up calculations and providing messages or test patterns. The main advantage of using a table is that you don't have to calculate answers or deal with each case separately. Microprocessors can easily handle tables since they have special instructions and addressing modes to access them.

Note, however, that tables don't save time if there is a simple relationship between input and desired output, e.g., the output is twice the input. Nor is the table useful if there is an easy way to directly perform the calculation. When using a table, you must be willing to trade off memory space for speed.

Tables themselves are just simple lists of data that are stored sequentially in a memory array. A telephone directory is a good example of an alphabetical read-only table. Variable tables stored in RAM allow the system user to assign meanings to inputs and to determine sequences of tests or output patterns. Some function generators even use ROMs that hold the

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Dr. Lance A. Leventhal, Instructor, Engineering and Technology Dept., Grossmont College, 8800 Grossmont College Dr., El Cajon, CA 92020.

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The table contains the codes in hexadecimal with the most significant bit always 0, followed by the bits for segments g, f, e, d, c, b, and a in that order.

1. Converting decimal inputs into seven-segment drive signals requires a simple table with a separate entry for each decimal number (a). An easy three-step procedure is all that's needed to access the table (b). Assembly-language programs for the 8080 (c) and the 6800 (d and e) require less than 10 lines of code. Note that # indicates "immediate" and X means "indexed" on the 6800 assembler. Also, 0, X can be abbreviated to just X.
envelope values of a sine wave and generate waveform outputs by reading out the tabular information in cycles. A processor can also form a variable table much as it forms any other data array. (For more about data-array handling, see reference 1).

Besides mathematical data and standard codes, tables can contain starting addresses for programs. Such tables are very useful for performing special program operations by interpreting a coded input from a keyboard as a starting address for a subroutine. An obvious task for a table, though, is to perform a code conversion when no simple relationship exists between input and output.

A simple code conversion problem

A common output task for a µP is to convert a decimal digit to a seven-segment display code. The code table for the display can be set up for common-anode or common cathode LED displays very easily (Fig. 1a). However, before the table is used, some questions must be answered:

- Where does the table start?
- How is the table organized?
- Which entry do you want?

In this simple conversion, the table is short and entries are in consecutive order, from 0 to 9. To use the table, you must obtain its starting address, add the entry number (the decimal number to be converted), and use the resulting address as a pointer.

Most minicomputers and some µPs can get an answer from a table with a single instruction by using indexed addressing. In indexed addressing, the starting address of the table is part of the instruction and the entry number or index is in an index register. The processor adds the two together and uses that address to get the data (Fig. 1b). But since neither the 8080 nor the 6800 has true indexing capability, the procedure takes several instructions instead of just one.

The 8080 program to convert the code uses register-indirect addressing where the address of the data is in registers H and L of the 8080. A Double Add instruction (DAD) can do the indexing by adding the contents of another register pair to the H and L registers.

The assembly-language program to do the table accessing is shown in Fig. 1c. The program must extend the 8-bit data into a 16-bit number before adding it to the base address (SSEG) of the table.

Accessing a table with a 6800 µP requires that its so-called indexing mode be used, but this takes some effort. You actually have two alternatives:

- Increment the index register the appropriate number of times (see program Fig. 1d).
- Place the data and the eight most significant bits (MSBs) of the starting address in the index register and use the eight least significant bits (LSBs) of the starting address as the offset in the instruction (see Fig. 1e).

The transfer through memory is awkward, but necessary for the 6800 since there is no other way to move data from the 8-bit accumulator to the 16-bit index register. The 16-bit index register must hold eight bits of the starting address and eight bits of the index since the 6800 only uses an 8-bit offset with the instruction. (Remember, the instruction is typically in ROM so the data can't be part of it.) However, since the 6800 adds the offset to the contents of the index register as part of the normal addressing procedure, no explicit addition instruction is necessary.

The 8080's program can be simplified by placing the table so that it's all on one page (a page is a 256 word section of memory in which the eight MSBs of all addresses are the same.) Thus there are never any carries into the MSBs from the starting address to the indexed address. For example, the decimal-to-seven-segment table could occupy memory addresses E034 to E03D. In general, if the table starts at an address given by SSEGM (eight MSBs) and SSEGL (eight LSBs) and it is contained on a single page, the conversion program simplifies to the extent shown in Fig. 2a.

The program can be made even simpler (Fig. 2b) if the table starts at an address that is an even multiple of $0100_{16}$. Then SSEGL = 0, and addition is unneces-

```
| LDA   | DIGIT   | ;GET DECIMAL DIGIT |
| MOV   | L, A    | ;USE AS LSBs OF ADDRESS |
| MVI   | H, SSEGM;GET MSBs OF 7-SEGMENT TABLE |
| MOV   | A, M    | ;GET 7-SEGMENT CODE |
| STA   | SCODE   | |
| HLT   |         | |

LDA   #SSEGL;GET MSBs OF STARTING ADDRESS
STAA  TEMP
LDA   DIGIT;GET DECIMAL DIGIT
STAA  TEMP+1
LDX   TEMP;MOVE OFFSET ADDRESS TO INDEX REGISTER
LDAA  SSEGL,X;GET 7-SEGMENT CODE
STAA  SCODE
WAI
```

2. Handling a table can be simplified by keeping the entire table on one 256 word page (a) or by starting the table at the beginning of a page (b).
sary. However, the total program savings is small compared to the size of the table; the more general approach shown in Fig. 1c permits the table to be placed anywhere in memory.

Indeed, if you want, assembler pseudo-operations can place a table at the beginning of a page—but look out for problems if the table has to be moved or expanded beyond the page. Also, you may have to waste memory to keep the table in the proper place and avoid overlapping with other programs.

The 6800, on the other hand, does indexing as part of its normal instruction execution. Nothing is saved by aligning tables. Even if the offset value is zero, the 6800 has to store the offset in program memory and add it to the index register. Page boundaries are automatically handled because even though the offset is only eight bits long, the indexing is a 16-bit operation with carry. However, all 6800 indexing operations take extra cycles because the ALU is just eight bits long.

**Other µPs also handle tables**

Other processors have their own ways of accessing tables. For instance, the F8 µPs uses a Load DC Immediate (DCI) instruction to place a 16-bit starting address in the data counter (DC), an Add to Data Counter (ADC) instruction to add the contents of the.

---

3. When each table entry requires more than one byte, as with this 14-segment display example (a), an extra operation must be added to the program flow chart (b).
A typical error code table would be:

<table>
<thead>
<tr>
<th>CODE</th>
<th>STARTING ADDRESS (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1000</td>
</tr>
<tr>
<td>1</td>
<td>1015</td>
</tr>
<tr>
<td>2</td>
<td>1027</td>
</tr>
<tr>
<td>3</td>
<td>1037</td>
</tr>
<tr>
<td>4</td>
<td>1050</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The error messages could be:

<table>
<thead>
<tr>
<th>STARTING ADDRESS</th>
<th>ERROR MESSAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>TOO MANY TEST POINTS</td>
</tr>
<tr>
<td>1015</td>
<td>ILLEGAL CHARACTER</td>
</tr>
<tr>
<td>1027</td>
<td>NO SUCH COMMAND</td>
</tr>
</tbody>
</table>

The error messages are stored as character codes and each ends with a carriage return.

4. Tables can also hold message addresses, where each message is stored as a string of character codes and ends with a carriage return (a). The program flow chart now has to detect the end of message code (b).

5. The error-handling routines for both the 8080 (a) and the 6800 (b) are single subroutines that print all the error messages. When the main program (c) detects an error it loads the accumulator with the appropriate code and forces the processor to execute the subroutine.

accumulator to the data counter (a 16-bit operation with carry) and a Load Memory (LM) command to load the accumulator with the contents of the memory location specified by the data counter.

On the 2650 μP, indexing is done by the instruction LODA R0 BASE, R0 loads register R0 with the contents of the address BASE plus the old contents of R0. Therefore, the 2650 can perform indexing with a single instruction. For the 6502 μP, indexing is done by the instruction LDA.

LDA DIGIT :GET HEXADECIMAL DIGIT
ADD A     :INDEX = 2 · HEXADECIMAL DIGIT
MOV L,A   
MVI H, 0  
LXI D, SEG14 :BASE = STARTING ADDRESS OF TABLE
DAD D     :POINTER = INDEX + BASE
MOV E, M  :LSBs OF CODE = (POINTER)
INX H     
MOV D, M  :MSBs OF CODE = (POINTER + 1)
XCHG      
SHPD SCODE :STORE 14 SEGMENT CODE
HLT

LDA DIGIT :GET HEXADECIMAL DIGIT
ASLA INDEX = 2 · HEXADECIMAL DIGIT
STAA TEMP+1
LDAA #ETABU GET 8 MSBs OF ADDRESS TABLE
STAA TEMP
LDA TEMP MOV OFFSET POINTER TO INDEX REGISTER
LDA ETABL, X GET MESSAGE ADDRESS FROM TABLE
ERRP LDAA X GET A CHARACTER FROM MESSAGE
JSR SEND AND PRINT IT
INX CMA #CR IS CHARACTER “CARRIAGE RETURN”? BNE ERRP NO, KEEP PRINTING
RTS

8080 EPRNT: ADD A :INDEX = 2 · CODE
MOV L, A
MVI H, 0
LXI D, ETAB :BASE = STARTING ADDRESS OF ADDRESS TABLE
DAD D :POINTER = INDEX + BASE
MOV E, M :LSBs OF MESSAGE ADDRESS = (POINTER)
INX H
MOV D, M :MSBs OF MESSAGE ADDRESS = (POINTER + 1)
XCHG ERRP: MOV A, M :GET A CHARACTER FROM MESSAGE
CALL SEND :AND PRINT IT
INX H CPI CR IS CHARACTER “CARRIAGE RETURN”? JNZ ERRP NO, KEEP PRINTING
JNZ CR, ERRP NO, KEEP PRINTING
RTS

6800 EPRNT: ASLA INDEX = 2 · CODE
STAA TEMP+1
LDAA #ETABU GET 8 MSBs OF ADDRESS TABLE
STAA TEMP
LDA TEMP MOV OFFSET POINTER TO INDEX REGISTER
LDA ETABL, X GET MESSAGE ADDRESS FROM TABLE
ERRP LDAA X GET A CHARACTER FROM MESSAGE
JSR SEND AND PRINT IT
INX CMA #CR IS CHARACTER “CARRIAGE RETURN”? BNE ERRP NO, KEEP PRINTING
RTS
BASE, X, which loads the accumulator with the contents of address BASE plus the contents of index register X. BASE is a complete 16-bit address stored in two words of program memory, while X is an 8-bit index register.

The table example in Fig. 1 assumes that each entry only occupies one byte. However, when entries require more than one byte, programming gets a little more complex: The program must multiply the data by the number of bytes per entry to get the correct index. Then the program must fetch all the bytes of the entry.

For example, assume the table output drives a 14-segment display (Fig. 3a). A flow chart for the program as well as an example are shown in Fig. 3b. The 8080's program has only a few changes from the seven-segment program: two bytes of data are used for each entry and the hexadecimal digit must be multiplied by two to get the index. To do the multiplication, add the data to the data (Fig. 3c). The 6800 program is similar, except that all 16 bits of the answer can be fetched with a single Load Index Register (LDX) instruction. An arithmetic left shift does the multiplication by two (Fig. 3d).

**Tables can contain addresses, too**

Tables can contain more than just data. An error routine, for example, can use a table to find the starting point of an operator message from a code in the accumulator. This single error routine can thus print the code and the error message for all possible errors (Fig. 4a). Furthermore, you can easily add more error messages by expanding the table. The programs are similar to the previous examples except that the entry from the table is the starting address for the output routine (see the flow chart in Fig. 4b). Remember that addresses are 16 bits long.

Both the 8080 and 6800 programs (Fig. 5a and b) print the error message ending with a carriage return (SEND is an output routine for one character). The main programs for both the 8080 and 6800 place the code in the accumulator and call the error routine (Fig. 5c).

The same technique can be used to interpret switch closures. Assume that a keyboard contains a numeric keypad and function keys similar to a calculator keyboard (Fig. 6a). An encoder or PROM can translate each key closure into a unique code, 0 to 9 for the digit keys and 10 on for the function keys. Here, a table organized as in Fig. 6b will do the job. The program, shown in flow-chart form in Fig. 7a, performs the following steps:

*Step 1:* Fetch keyboard data.

*Step 2:* If key number is less than 10, the key is a digit, so go to Digit routine.

*Step 3:* Otherwise, use key number to access the table of subroutines. The index is 2 X (key number minus 10), since each entry is 2 bytes long.

*Step 4:* Transfer control to the proper subroutine by jumping to the address obtained from the table. The 8080 program uses PCHL, an indirect jump that transfers the contents of registers H and L to the program counter (Fig. 7b). The 6800 program uses an indirect jump to the address in the index register (Fig. 7c). Remember that the 6800 has no separate I/O instructions, so LDAA PIADRA is equivalent to IN KBD on the 8080. Even though the 6800 indexes awkwardly, it can fetch the 16-bit address with a single instruction. An actual example is shown in Fig. 7d. Note how easy it is to add more function keys—all you have to do is write the new function subroutine and place it in program memory. Then place the starting address of the function subroutine in the jump table, and wire the new key so that it produces the correct input.

A similar procedure can interpret single-letter commands from a full alphanumeric keyboard (Fig. 8). The only difference is that to index the table, you must subtract the internal representation of A from the character-coded input. Undefined letters can simply cause a jump to a reset or error routine. Adding extra commands won't change the keyboard program. All you have to do is place the address of the new subroutine—in place of the error-routine address—in the table.

**Implement equations in tables, too**

Tables can do still more. Say you have an analog input to interpret or an output to produce or a trigonometric function, logarithm, or exponential to
To handle keyboard inputs, the processor must make a decision and determine whether the key pressed is a number or a function (a). Both the 8080 (b) and the 6800 (c) can handle the task, as shown by these simple programs. An example, using one of the table entries, is also shown.

Assume the table is:

<table>
<thead>
<tr>
<th>MEMORY LOCATION (HEX)</th>
<th>KEY NUMBER</th>
<th>MEMORY CONTENTS (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>10</td>
<td>00</td>
</tr>
<tr>
<td>1001</td>
<td>11</td>
<td>43</td>
</tr>
<tr>
<td>1002</td>
<td>12</td>
<td>67</td>
</tr>
<tr>
<td>1003</td>
<td>13</td>
<td>20</td>
</tr>
<tr>
<td>1004</td>
<td>14</td>
<td>A1</td>
</tr>
<tr>
<td>1005</td>
<td>15</td>
<td>B7</td>
</tr>
<tr>
<td>1006</td>
<td>16</td>
<td>D5</td>
</tr>
<tr>
<td>1007</td>
<td></td>
<td>20</td>
</tr>
</tbody>
</table>

If the key number is 14, the process is:

STEP 1) \( \text{INDEX} = 2 \cdot (\text{KEY NUMBER} - 10) \)

STEP 2) \( \text{POINTER} = \text{BASE} + \text{INDEX} \)

STEP 3) LSBs of PC = (POINTER)

MSBs of PC = (POINTER + 1)

So the next instruction to be executed will be the one in memory location 20A1. Remember that the 6800 stores its addresses with the most significant bits first.

8. A more complex keyboard can also be handled by the processor. Just expand the table of look-up functions and allow enough space in memory.
For example, if the data is 6D, the program would search through the memory starting in location 1009 (see Figure 2) and ending when it finds the code in location 1005. The backward search is convenient since the counter is always one more than the index.

The 8080 program is:

```
LXI H
SSEGE :POINTER = END OF TABLE
MVI B, 10 :COUNTER = LENGTH OF TABLE
LDA DATA :GET DATA
SRTAB: CMP M :IS DATA = TABLE ENTRY?
JZ DONE :YES, DONE
DCX H :NO, GO TO NEXT ENTRY IF ONE EXISTS
DCR B
JNZ SRTAB
DONE: DCR B :RESULT = COUNTER -1
HLT
```

The 6800 program is:

```
LDX #SSEG: POINTER = END OF TABLE
LDAB #10 :COUNTER = LENGTH OF TABLE
LDAA DATA :GET DATA
SRTAB: CMPA X :IS DATA = TABLE ENTRY?
BEQ DONE :YES, DONE
DEX :NO, GO TO NEXT ENTRY IF ONE EXISTS
DECB
BNE SRTAB
DONE: DECB RESULT = COUNTER -1
WAI
```

9. A table can also be searched to find the index corresponding to an entry (a) by scanning all the table entries until the desired one is found and reading out the location. Both the 8080 and 6800 programs for this job (b) require less than a dozen lines of code.

evaluate. To solve these problems, you can find a functional relationship in an engineering manual or a book of algorithms. Or you can simply use a table.

For an analog input or output, the table is often a calibration table. To handle an input, the calibration table contains the actual reading that corresponds to the input data. To handle an output, the calibration table contains the data required to produce that result.

For the 14 segment table the pseudo-ops are:

INTEL 8080

```
SSEG: DB 3FH, 06H, 5BH, 4FH, 66H
DB 6DH, 7DH, 07H, 7FH, 6FH
```

MOTOROLA 6800

```
SSEG FCB $3F, $06, $5B, $4F, $66
FCB $60, $70, $07, $7F, $6F
```

10. To actually store the tables in memory, you can use pseudo-ops if you're working with an assembler. For the examples used in Fig. 1 and Fig. 3, the required pseudo-ops are shown in (a) and (b), respectively. Note that the 8080 assembler uses a final H to indicate hexadecimal notation while the 6800 assembler uses an initial $.

The table must store all the possible results, so if the input and output are both 8 bits long, 256 8-bit words are required. In more concrete terms, that amount of memory translates to one 1702 PROM or one-quarter of a 2708 PROM.

Of course, not all tables are organized in a simple consecutive order. Perhaps only a few inputs will ever occur. But you can get the right entry from the table without first having to store a lot of entries.

In simple cases, searching through a table for the data will do the job. Often, you can check data against each entry in the table until you find a match. The answer will be the index of the matching entry. For example, you can use the table from Fig. 1 in reverse to convert a seven-segment code to a decimal digit (the seven-segment code might be an output from a calculator chip). If the code is in the table, the answer will be the digit. If not, the answer will be -1. The procedure, flow-charted in Fig. 9a, boils down to:

Step 1: Initialization

- Pointer = End of table
- Counter = Length of table

Step 2: Search table

- If (Pointer) = Data, go to step 4.

Step 3: Decision and loop

- Pointer = Pointer -1
- Counter = Counter -1

Step 4:

- Result = Counter -1

Of course, if the table is long, this procedure is slow; it's like looking up a telephone number by starting
at the front of the book and checking every name. For long tables, some better search procedures include:
• A binary search, which checks the halfway point of an ordered table, determines which half of the table the entry is in, then halves the correct half, and so on. The procedure is much like that used by a successive-approximation analog-to-digital converter.
• Two-level indexing, whose first level gives you a starting point much as the letter tabs in a dictionary do, while the second level provides the exact location.
• Hashing, whereby you derive a starting point from the data by using some kind of function.\(^7\)\(^8\)

One problem remains—how to store the tables in memory. Most assemblers have a pseudo-operation (often called DATA) to do this. Microprocessor assemblers, in fact, usually have two pseudo-operations, one for 8-bit data and one for 16-bit addresses. The Intel 8080 pseudo-ops are DEFINE BYTE (DB) and DEFINE WORD (DW). The Motorola 6800 pseudo-operations are FORM CONSTANT BYTE (FCB) and FORM DOUBLE CONSTANT BYTE (FDB). The required pseudo-ops to place the seven-segment and the 14-segment tables in memory are shown in Fig. 10a and 10b, respectively.

As mentioned earlier, you can often simplify table-accessing programs by aligning the tables so that they start at the beginning of a page, e.g.:

```
SSEG EQU 1300H (for the 8080), or
SSEG EQU $1300 (for the 6800)
```

Then the program needn't consider carries into the more significant digits when performing the indexing. If you want to be able to vary the page number, try either of the following routines:

For the 8080

```
TPAGE EQU 25H
TBASE EQU TPAGE * 256
```

For the 6800

```
TPAGE EQU $25
TBASE EQU TPAGE * 256
```

The 256, of course, is \(2^8\), and multiplying by it moves the page number to the eight MSBs. Now you can assign the table to a particular page by giving TPAGE a value before assembling the program.\(^\star\)

References

3. For more about the 8080, see Nichols, A.J. and McKenzie, J., “Microprocessor Basics: Part 2, Build a Compact Microcomputer with the 8080,” Electronic Design, No. 10, May 10, 1976, p. 84.
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<table>
<thead>
<tr>
<th>EC Core</th>
<th>2 Gapped Cores</th>
<th>1 Gapped + 1 Ungapped Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>35 mm</td>
<td>325 AT</td>
<td>200 AT</td>
</tr>
<tr>
<td>41 mm</td>
<td>370 AT</td>
<td>220 AT</td>
</tr>
<tr>
<td>52 mm</td>
<td>540 AT</td>
<td>330 AT</td>
</tr>
<tr>
<td>70 mm</td>
<td>860 AT</td>
<td>570 AT</td>
</tr>
</tbody>
</table>

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CIRCLE NUMBER 50

ELECTRONIC DESIGN 17, August 16, 1977
Simplify analog/computer interfacing. Choose the data-acquisition configuration that's best for your system, then use the right analog-to-digital converter.

The choice of configuration for your data-acquisition system can influence your choice of a/d converters, and it can influence system speed, accuracy, data latency, power and dollars. There are three important data-acquisition configurations.

In the multiplexed random-channel-addressed configuration (Fig. 1a), multiplexed analog switches deliver one sensor's signal at a time to a sample-and-hold (s/h) circuit. This looks at and stores the momentary value of the signal for digitizing.

In the parallel-conversion system (Fig. 1b), each analog channel has a dedicated a/d converter. And in the multiplexed-with-memory system (Fig. 1c), the inputs are multiplexed, as in a multiplexed random-addressed system; while the outputs, after they are digitized, are all stored for immediate access.

Converters are more than just a/d

The multiplexed random-channel-addressed system boasts advantages of simplicity, straightforward design and low cost. Such a system then operates in the Command mode and so the computer waits for data once a conversion starts.

The operating sequence for the Command mode is:
- The computer addresses a specific channel.
- The analog multiplexer (MUX) selects the desired channel.
- An s/h circuit acquires and holds the analog signal.
- An a/d converter digitizes the signal and returns a Ready signal to the computer after the data are presented to the data bus via three-state bus drivers.

Unfortunately, when the acquisition system operates in the Command mode, the computer must enter a Wait mode while the data are readied; or proceed with its assigned task, watch for a Data Ready flag, and return for the data. All this takes up processor time.

A microprocessor wastes less time when it accesses input data as it would memory.1 In addition, when input-data and main-memory access times are equal, waiting for data is eliminated. So some systems make conversions in parallel. On each input-data channel, these parallel systems use one a/d converter containing three-state output-data latches.

Fig. 1b shows such a parallel-conversion system containing only an address decoder and multiple a/d converters, with all outputs wired in parallel onto the data bus. This system doesn't use s/h circuitry. The ideal converter package for this system would include buffered three-state output-data latches in addition to the a/d converter.

The system should convert continuously. Data from the last conversion should remain in the output latches until the next completed conversion transfers its data into the latches. Latest valid data are thus always available for readout on the data bus, except for the brief period when the data are updated. In contrast, a converter without buffered output latches does not hold data after a Start Conversion signal.

Converter prices are coming down

Though parallel conversion provides simple and immediate data access, the cost of one a/d converter per channel has, in the past, been a heavy burden. However, the low cost of many monolithic and even some hybrid a/d converters now make parallel conversion practical. Furthermore, the downward trend for converter prices should continue as more monolithic units are released.

At present a/d converter prices, however, one can get immediate access, particularly for 12-bit data at a lower cost than that of parallel conversion. The multiplexed system with memory, Fig. 1c, interfaces to a computer in the Memory Access mode—without any waiting period.

One particular system with memory features a dedicated, on-card, 16 × 12-bit RAM that supplants buffered output latches. One can, of course, replace the RAM with main-memory locations, but writing into memory then uses valuable machine time. With the dedicated RAM, the latest data are available in the acquisition system and the processor software is simplified.

But cost and simple software aren't the only considerations. There is, of course, the matter of data bandwidth. The bandwidth of a sampled-data system is limited by Shannon's sampling criterion and prac-

Jim Sherwin, Data-Acquisition Applications Manager, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051
Random-addressed multiplexed systems make computers wait while the lone a/d converter processes the selected input channel (a). Parallel-conversion systems (b) process each input channel with a dedicated converter and so eliminate an error source—the analog multiplexer. In the multiplexed system with memory (c) a RAM stores the converted data from the single a/d unit and so the computer has immediate access to any channel. Data-bandwidth curves for 8 to 14-bit systems, with and without s/h, indicate that parallel-conversion systems without s/h can process only low-bandwidth data.

**Without s/h, conversion must be fast**

In a system where there is no s/h, as in parallel-conversion, digitizing must take place within the time it takes the input signal to change by ±1/2 LSB or by one part in \(2^{n+1}\), where \(n\) is the resolution in bits. The data bandwidth for a sine wave is \(2^{-(n+1)}\) divided by the conversion time. For the same 50-\(\mu\)s conversion cycle as in the sampled-data system and an 8 bit accuracy requirement of ±1/2 LSB, the unsampled-data bandwidth is 12 Hz. Data bandwidths for 8 to 14-bit systems with and without s/h are compared in Fig. 4.

Adding an s/h module in front of each converter in a parallel-conversion system can easily double the cost per channel of an 8-bit system. The cost also climbs when conversion speed increases significantly, except with tracking converters.

With a system that can afford to go into a Wait mode after it requests data, a random-accessed system costs less than any other. The waiting period can be as short as 10 to 20 \(\mu\)s with fast s/h and a/d circuits, but these are expensive.

Lower-cost systems can prolong the waiting period to 100 to 200 \(\mu\)s. With complex software, the computer can remain busy during the conversion cycle, and return when the data are ready.

The curves in Fig. 4 show that system sampling each channel every 20 ms can process 16 channels of 10-Hz data. This is a data-throughput rate of 16 divided by 20 ms—which is 800 Hz. The higher cost systems of this type are capable of 50 to 100-kHz throughput rates.

Parallel-conversion systems without s/h circuits can process only low bandwidths (Fig. 4). Parallel conversion uses many converters, so it’s advisable to avoid expensive ones. That leaves only 8 or 10-bit successive-approximation-register (SAR) converters or 12-bit integrating monolithic converters. Cost alone, then, limits parallel-conversion systems to 10 to 30 Hz for 8 bits, 2 to 5 Hz for 10 bits, and lower than 1 Hz for 12 bits. Replacing SARs with tracking converters can raise bandwidths of 8 and 10-bit systems by 8 to 10 times.

Unlike the situation in parallel-conversion systems, in multiplexed systems with memory, the bandwidths and data-throughput rates are mainly limited by s/h and converter operating times. At only a slightly higher cost per channel than even a random-addressed system, the system with memory lets the computer operate efficiently.

**Consider all the costs**

To be valid, cost and performance comparisons for the three types of acquisition systems must include all the required hardware and even the software. With
3. There is no waiting period in the Memory Read cycle for an 8080 microprocessor interfaced to this 16-channel, 8-bit, parallel-conversion system. The converters can drive only a lightly loaded bus (one TTL load).

16 channels, a random-addressed multiplexed system uses an a/d converter, an s/h module, a 16-channel multiplexer, complex control circuits, complex software, and 16 anti-aliasing filters. (Anti-aliasing filters are low-pass devices that prevent frequency-folding or aliasing errors caused by sampling rates too low for the data bandwidth.) Access to the data is slow.

Parallel conversion for 16 channels requires 16 a/d converters, 16 anti-aliasing filters, simple control circuits, power for the converters and simple software. The data bandwidth is low, however. A 16-channel multiplexed system with memory takes an a/d converter, an s/h module, a 16-channel multiplexer, 16 anti-aliasing filters, a 16-word by 12-bit-per-word RAM, complex control circuits and simple software. Access to data, via the memory, is fast.

Fig. 2 shows an 8080-compatible, random-addressed, 16-channel, 12-bit system. The analog section contains a 16-channel analog multiplexer, an s/h block and a 12-bit a/d converter. Before the s/h block, the multiplexer might be a differential type and differential or even instrumentation amplifiers could be useful to simplify system integration.

The data-output circuits can interface directly to an 8-bit data bus, like those of the 8080 and 6800 microprocessors. An 8-bit µP must accept the 12-bit data word in two 8-bit bytes. Since a processor usually accesses a 12-bit word with two consecutive addresses (0 and 1 as LSB), multiplexers like the DM8123 work well here. They have three-state outputs and the address LSB can directly drive the Channel Select input. To interface a 16-bit address bus, such as in the PACE µC, replace the output multiplexers with three-state output buffers such as the DM8097. For a lightly loaded data bus, low-power versions of these parts provide adequate drive and save power.

Address comparators raise capacity

For address decoding, a 6-bit magnitude comparator (DM8131 is one type) looks at the six MSBs of the address. With only these six bits, a single system has 64 possible sets of 16 input channels each and uses up to 64 pages of memory. When more input capacity is needed, two address comparators, ORed together, can handle 12-bit addresses and thereby increase the 64 sets of inputs to 4096.

The magnitude comparator(s) plus the four address lines to the 16-channel multiplexer make up the complete address decoding. The magnitude comparator indicates which converter is addressed; the four address lines select one of 16 channels for processing by the selected converter.

When operating with an 8080 µP, the acquisition system in Fig. 2 receives a Memory Read command, MRDC. When data are ready the system issues an acknowledgment, XACK. This is the simplest possible interface between an a/d converter and any computer. And though the 8080 is one of the least complex processors to interface with, it takes only minor changes to mate this system with most other microcomputers—with the 6800 or the PACE, for example.

The only timing anomaly in the logic of Fig. 2 is a ZERO-level pulse of from 10 to 40 ns that occurs when the XACK buffer is enabled. However, the computer isn't affected by the XACK signal at this time and so enters the Wait mode until XACK is returned later.

Speed and accuracy—that's all

The converter in this random-addressed system can be a conventional type; only speed and accuracy matter. Three-state output buffers or data latches aren't needed because the data are latched in the register until a new Start Conversion command occurs.

As shown in Fig. 2, a complete a/d converter, adequate for the 8080-compatible, random-addressed system can be made up of a 12-bit a/d converter block that is specifically tailored for use with a successive-approximation register. Devices such as DM74C905 and DM2504 SARs mate with converters like the DA1200. Many other converters that will work well
in this system can either be put together from components or purchased complete. The component cost for the converter shown in Fig. 2 is about $9.50 per channel and it uses 2.8 W total.

Parallel a/d's give fresh data fast

Though the random-addressed system of Fig. 2 may be the simplest to interface with most microcomputers, a parallel-conversion system is most likely the simplest microcomputer-compatible system in which the latest input data can be accessed as if they were in main memory. But because so many a/d converters are used, each must use only very little power. The individual a/d converters in Fig. 1b include three-state outputs for Wire-ORing on the data bus. However, making each converter capable of driving a heavily loaded bus would raise the power significantly. Accordingly, when the bus loading so requires, add a set of three-state TTL buffers.

The control circuits are simple; primarily, they accept the Memory Read command and then return the Memory Ready signal. Any control-circuit complexity stems from processors that accept data in two 8-bit bytes rather than in one of 16 bits. And even this doesn't make the controls very messy. Small differences in the address decoder and control circuits will exist, depending on the computer.

The 16-channel parallel-conversion system in Fig. 3 interfaces with an 8080, without a waiting period in the Memory Read cycle. Components for this unit cost about $10 per channel. It is, however, a minimal system, capable only of driving a lightly loaded bus. For heavier loads, use two quad three-state buffers.

Handshaking follows addressing

A 4-to-16-line decoder selects the addressed channel using the address' four LSBs. The six MSBs select one of the 64 memory pages. These six MSBs also operate the comparator that gates the 4-to-16 decoder. In addition the comparator, gated by the Memory Read command MRDC, inhibits the clock to prevent data change in the output during the data-access period.

A Data Ready acknowledgment returns to the processor when the address is correct and MRDC is true. No other logic is required; however, inverters are necessary in the converters' Enable lines due to a sense mismatch between these Enables and the 4-to-16-decoder outputs.

Fig. 4a shows a 16-channel, 12-bit, parallel-conversion system for the 8080. The converters are hypothetical units containing d/a switches, ladder network, comparator, up/down counter (for tracking conversion), control logic and three-state buffered outputs. The converters operate continuously, with the output-data buffer updated at the end of each conversion.

Such converters can settle in 1 to 4 $\mu$s (after an initial but longer acquisition period) without being costly. Also, this sort of converter can provide 12-bit accuracy to ±1/2 LSB at a data bandwidth of 10 to 20 Hz. A single external buffered reference can handle all channels. An external gated clock can drive all the converters.

The address decoding is the same as that for the 8-bit system. The LSB of the address selects either byte 1 or 2 of the 12-bit output-data word via the two quad, three-state, two-input, multiplexers. A ZERO selects the eight LSBs of data (byte 1) and a ONE selects the four MSBs (byte 2). ZEROs are placed on the four remaining data lines of byte 2.

Address bits 1 to 4 are decoded into 1 of 16 Select bits that enable the three-state output of the selected converter. Since ZERO is the true state for the decoder DM75L15A, it is desirable that ZERO also be the true state for the converter's Enable input. Otherwise, 16 inverters would be required. For two's complement
5. ANDing the VMA and R/W signals decodes a valid address in the 16-channel parallel-conversion system for the 6800 microprocessor (a). Address information, the valid-memory-address signal, VMA, and the read/write signal, W/R, all come up together. Data are due at the data bus 100 ns before Ready changes state (b).

...coding of positive or negative analog signals, the 12th bit is inverted and extended to the four remaining data lines, so that signals appear as valid data to the microprocessor.

The control timing is referenced to the 8080 timing as shown in Fig. 4b. The total circuitry for address decode, control, clock and output-drive logic is contained in six DIPs. To complete this 8080-compatible, parallel-conversion system, a code-select header, a reference and 16 converters are needed. The system consumes 4.2 W and provides 16 channels of 12-bit data from ±5-V, 10-Hz bandwidth, analog, input signals. Limiting the output-drive capability to only low-power TTL reduces the power drain by 370 mW. Total cost of the parts runs to about $16 plus about $25 for each a/d converter.

Similar logic ties in most micros

For systems feeding most other microcomputers the logic changes only slightly. Fig. 5a details the logic section of the acquisition system of Fig. 4a, modified to interface with the 6800 microprocessor. The 6800 timing and control signals are shown in Fig. 5b. In the 6800, the address, the Valid Memory Address (VMA) signal and the Read/Write (R/W) signal all appear almost simultaneously and remain active for at least 1 µs. The data need not be on the data bus until the final 100 ns.

The valid address is decoded by ANDing the VMA and R/W signals in a three-state two-input gate. When enabled by the comparator output, this gate returns a Ready signal to the processor and also enables the output multiplexers. As with the 8080 system, the address LSB selects the appropriate data byte. Delays in disabling the output multiplexers and the a/d converter provide the required 10-ns data-hold time. The rest of the system is the same as in Fig. 4a. The cost and power required in this 6800-based system are
close to those for the 8080-based system.

Fig. 6a shows the logic section of the system of Fig. 4a modified to interface with a PACE microcomputer. The PACE timing is shown in Fig. 6b. Since the PACE µC has but a single bus for both address and data, address decoding requires latches. These latches are included on PACE CPU cards, but when using just the PACE chip, latches must be added to the system as needed. The address comparator used in this system (DM8131) contains output latches, but the 4-to-16-decoder (DM74L154A) does not, so a quad latch is inserted ahead of the decoder.

The latches set on the rising edge of the NADS signal which comes from PACE when the bus has address information. The latches reset on the next NADS signal. The comparator output then gates the decoder and so provides an Enable ADC signal that lasts until the falling edge of the next NADS pulse. The IDS signal, ANDed with the comparator output, enables the three-state output buffers and inhibits the clock.

An additional MSB inverter is needed for positive and negative analog signals to provide the two's complement code. All the circuitry for address decode, control, clock, and output drive is contained in seven DIPs—one more than required for the 8080 system interface. Total power and cost are comparable to those for the 8080-based system.

Three-state latches are a must

The a/d converter for a parallel-conversion system must contain three-state output-data latches. Otherwise, it can be a conventional type. Several 8-bit a/d converters, intended to connect directly to a data bus, contain the necessary output latches.

To be ideal for an 8-bit parallel-conversion system, a converter should be of the tracking variety, with ZERO the true state for its Enable and ONE true for the binary outputs. But, data polarity isn't very important because most systems need bus drivers and these can be either inverting or noninverting. On the other hand, matching the polarity of the Enable with the decoder output can save 16 inverters.

For this parallel-conversion data system the data bandwidth is limited to about 10 Hz for 8-bit SAR converters. It can be increased to 150 or 300 Hz with 8-bit tracking converters. For 12-bit systems the data bandwidth is 1/16 that of 8-bit systems. On the other hand, no s/h module is required. Data rates can be considerably increased with s/h modules added to each channel; but costs per channel would more than double. For use with s/h modules, SAR converters are faster than tracking types, allowing data bandwidths of over 600 Hz per channel for 12-bit data.

MUXed system with memory outputs fast

A multiplexed data-acquisition system containing memory is probably the most cost-effective way of providing an immediate data-access interface to processors. To obtain data, the processor addresses the peripheral data-acquisition system, without entering a Wait mode, just as if it were accessing main memory. Latest valid data are always present within the acquisition system's memory, which is updated at a rate determined by the channel-multiplexer rate and the conversion speed.

The multiplexed system with memory shown in Fig. 1c takes care of routinely updating its memory by sequentially sampling each data channel, digitizing the channel signals, and writing data into its self-contained memory. When the system is interrogated, the sequential process is momentarily interrupted, the RAMs are addressed by the processor, and data are read out to the data bus. The memory can be implemented with three 16 × 4-bit RAMs.

The microcomputer interfaces shown in Figs. 7a and 7b are similar to that of Fig. 2. The PACE interface is slightly less complex than that of Fig. 7a for 8-bit data-bus machines. A single card with plug-in or strap options could interface any of the three micros con-

7. The address comparator and control for the multiplexed system with memory for the 8080 and 6800 microprocessors (a) only differ by a NOR gate. Logic for the PACE-based system (b) is the simplest.
considered. Such a universal circuit is shown in Fig. 8. This circuit also includes an option that provides binary output for unipolar analog signals or complementary-binary output for bipolar signals. In the case of binary output, data bits 13 through 16 are set to ZERO. In the case of two's complement binary, the sign bit is extended to data bits 13 through 16 for validation of the sign by the computer. The multiplexed immediate-access system of Fig. 8 dissipates a total of 3.5 W and costs $11 per channel.

The a/d converter for this application is similar to that for the conventional system except that the data output should be complemented to compensate for the data inversion within the RAMs.

**Match the converter to the system**

Each approach to the data-acquisition problem requires different characteristics of the a/d converter. Both sequential or random-addressed types require similar converters. If the random-addressed system includes bus drivers, the converter is identical to that for the system with memory. Only the parallel-conversion type must contain buffered three-state output latches to hold each converter’s data.

It is desirable that the a/d converter for parallel conversion also have the other characteristics listed in the table.

The first two items (three-state output latches and TTL control and data signals) are by far the most important.

TTL-compatible control and data signals are desirable so that TTL-to-MOS and MOS-to-TTL interface buffers are not required between the a/d converter and the rest of the system. Dual-output strobing allows wire-ORing the interface directly to an 8-bit data bus, or using only an 8-line buffer without output multiplexers as shown in Fig. 2. However, a separate buffer is required in most systems. Tracking operation provides higher speed for a conversion circuit without an s/h. Inhibiting data transfer into the output-data latches, when the output is enabled, prevents reading changing data. An external gate can perform this inhibit function but it’s easier if the converter does the job. Straight-binary output is preferred for all microprocessor interfaces (except the 8080 when it operates with Intel’s system-bus drivers and receivers). It may be necessary to add
Desired a/d converter characteristics for data-acquisition systems

<table>
<thead>
<tr>
<th></th>
<th>Parallel conversion</th>
<th>Sequential with memory</th>
<th>Addressed without memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buffered three-state output data latches</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TTL-compatible control &amp; data signals</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Dual output-enable (Bits 0-7 &amp; Bits 8-11)</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Counter logic</td>
<td>UP/DN</td>
<td>SAR</td>
<td>SAR</td>
</tr>
<tr>
<td>Internal comparator</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Both Q &amp; Q̅ outputs on MSB</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Binary output polarity</td>
<td>Data*</td>
<td>Data</td>
<td>Data*</td>
</tr>
<tr>
<td>Busy output (three-state w/enable)</td>
<td>?</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal clock</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Continuous recycle when CC = SC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inhibit data XFR to latches when enabled</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Unimportant if Bus drivers used.

three-state line drivers to drive the data bus; so data can be complemented with inverting buffers, when required. Having both the MSB and its inverse MSB simplifies data readout in binary or two’s complement without adding an external inverter. The table shows a/d converter characteristics in approximate order of importance for parallel-conversion systems; the order is different for multiplexed-data systems.

More converters are coming

Several monolithic a/d converters of 8 to 12-bits have been announced. Some have three-state output latches. These monolithic converters and future versions of them promise to bring converter prices down to a level which will make parallel conversion economically feasible. Several hybrid converters also have been announced with attractive prices; however, it is the monolithics that promise the lowest ultimate cost.

In the future, an a/d converter most suited for parallel-conversion might appear as in Fig. 9a. This design meets all the goals set forth in the table. It could run at a clock rate of 0.25 to 1 MHz (1 to 4-µs conversion time) because it is a tracking converter. It should contain three-state, buffered, output-data latches and separate High and Low Bit-Enable lines allow two-byte operation of an 8-bit data bus; the output latches should not change state when the output is enabled; and the CC and SC terminals should be strappable for continuous conversion.

An 8 or 10-bit converter and possibly a 12-bit converter of this type might be built on a single chip. A hybrid or two-chip design is certainly practical. Where speed is not of importance, monolithic 10 or 12-bit converters can be built with integrating or voltage-to-frequency conversion techniques. The integrating technique seems to provide highest accuracy with the least circuitry, and therefore is a prime contender. Because the integrating a/d converter consists of both linear and digital circuits, it is normally multichip. However, as technology advances, it will become increasingly practical to produce, on a single chip, the low-drift low-offset amplifiers, integrators, and current sources required in a 12-bit a/d converter, along with the necessary logic. A two-chip approach is the likely choice now.

Reference

COMING IN

POWER SUPPLIES

The 8th in Electronic Design's 1977 series of award-winning FOCUS reports is scheduled for the September 27 issue. The Topic: Multiple-output DC Power Supplies.

There is growing interest in power supplies that deliver more than one voltage. These units have all the problems of ordinary power supplies, plus special ones of their own. The report will help engineer-readers avoid pitfalls in specification, application and use. It will look at questions like:

- Why should you select one supplier over another?
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- How do they obtain these features?
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Potter & Brumfield
Control the speed and phase of a dc motor by comparison against a control frequency

The speed and phase position of a small dc motor can be controlled with a Norton op amp operating as a frequency comparator. The op amp amplifies the difference between two frequencies:

\[ V_0 = K (f_2 - f_1), \]

where \( V_0 \) is the average voltage output of the op amp, \( K \) is a constant, \( f_2 \) is an input control frequency from an external source, and \( f_1 \) is a frequency derived from a chopped-light source driven by the motor (see figure).

A feedback loop from the phototransistor, \( Q_1 \), via monostable IC\(_2\) feeds \( f_1 \) to the inverting input of an LM3900 Norton op amp. When the speed of the motor is slow, the comparator output is a high (greater than 50%) duty-cycle signal. As a result, transistors \( Q_1 \) and \( Q_2 \) stay on proportionately longer and produce a high average voltage, which increases the motor's speed. With the control frequency, \( f_2 \), slower than \( f_1 \) produced by the motor speed, the comparator produces a lower average voltage.

The phase between the motor speed and the control input is based on monostable IC\(_3\)'s duty cycle and can be varied between the leading and trailing edges of the control-input signal by adjusting \( R_1 \). A phase lock within ±250 \( \mu \)s can be achieved. And varying potentiometer \( R_1 \) allows a wide range of speeds—240 to 3600 rpm—for the motor as \( f_1 \) and \( f_2 \) vary between 4 and 60 Hz.

Diode \( D_2 \) minimizes voltage transients from the motor, and \( Q_2 \) should have a heat sink to correspond to the size of the motor. The motor's voltage supply should exceed the maximum motor needs by 2 V to allow for \( Q_2 \)'s saturation drop.

An opaque 3-in. disc with eight small holes evenly spaced along its edge is mounted on the motor's shaft. The disc chops a light beam into pulses to represent the motor's speed. A phototransistor, \( Q_3 \), and a type-47 light bulb, aligned on opposite sides of the holes, generates the pulses.

Mike Yakymyshyn, Edmonton Telephones, 10405-104 Ave., Edmonton, Alberta, Canada T5J-OK7.

CIRCLE NO. 311

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Ideas for design

Get 32 times the bit rate instead of 16 from a programmable baud generator

Some LSI devices that incorporate the functions of a UART (Universal asynchronous receiver and transmitter) require a clock input 32 times their final bit-rate output, instead of the usual 16 times supplied by standard baud generators. The clocking circuit in the figure derives this doubled frequency from a 4702 fully programmable 8-channel baud generator without increasing its crystal frequency.

The 32-times clocking circuit uses two 9LS170, 4 × 4 register files to store the channel-frequency selection information, which is supplied on a per-channel basis. (For clarity, the write circuitry for these devices is not shown.) The 4702's two least-significant scan-counter outputs, Q₀ and Q₁, are the read-address inputs of the 9LS170s, A₀ and A₁, and Q₂ provides the read enables. In addition, the Q₀ through Q₇ 4702 outputs address the 9LS138 decoder.

Consider the LOW-to-HIGH transition of the 4702's clock output (CO), when its internal 3-bit scan counter changes from state 7 (HHH) to state zero (LLL): The Q₀ through Q₇ outputs of the 4702 are LOW until the next LOW-to-HIGH transition of the CO output; information for channel zero, now available at the 9LS170's outputs, feeds the S₀-through-S₇ bit-rate selection inputs of the 4702; and data from the output flip-flop in the 4702, clocked by the same LOW-to-HIGH transition; appears at the Z output and also is clocked into a 9LS164 shift register.

As clocking continues and the Q₀, Q₁, and Q₂ outputs of the 4702 change, the 9LS170 locations are read out sequentially and information is shifted into the 9LS164. After each of the eight clock transitions, a channel-7 output from Z appears at the Q₂ output of the 9LS164.

Although the 4702's Z output is 16 times the selected bit rate, the Exclusive-NOR output is 32 times the selected bit rate. As the clocking continues, each channel signal appears serially at the Q₀-output of the 9LS164 and is compared with the corresponding current-channel output by the Exclusive-NOR gate. But because of the eight-clock-pulse delay between them, each channel-output transition at Z results in two at the Exclusive-NOR output. Clearly, the Exclusive-NOR and the 9LS138 decoder operate as a transition detector and a synchronous demultiplexer.

Krishna Rallapalli, Manager of Applications Engineering, Fairchild Camera and Instrument Corp., 464 Ellis St., Mountain View, CA 94042.

CIRCLE NO. 312

The addition of an Exclusive-NOR gate and a shift register generates 32 times the final bit rate instead of the usual 16 produced by a programmable baud generator. And the circuit does it without doubling the crystal frequency that is fed into the 4702 generator.

104 ELECTRONIC DESIGN 17, August 16, 1977
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See Electronic Design's 1977-78 "GOLD BOOK"-Vol. 3, page 266
The circuit in Fig. 1 is an instrument interface that will allow almost any logic system—TTL, DTL, RTL, HNIL, ECL or any voltage CMOS—to drive TTL-input instrumentation. And this is done without worry about polarity. The circuit responds to input signals of 1 to 15 V without the need of level adjustment or polarity selection. Moreover, the input impedance of the basic circuit (Fig. 1a) to signals below 5 V is 1 MΩ shunted by only a few picofarads.

Dual FET Q1 is a dc source follower that presents a high input impedance to the interfaced logic circuit. An input-standardizing trimmer capacitor, C2, can be added to allow connection of a 10X scope probe for no-load observation of 10-to-15 V CMOS logic. Resistor R2 and diodes D1 and D2 clip input voltages over ±5.5 V, but resistor R1 is high enough in value so the clipping action won’t upset CMOS logic.

Pot R4 is adjusted for zero dc volts at the junction of resistor R1 and R2. Positive-going signals appearing at this point bias normally cutoff transistor Q3 into conduction, driving the normally high input of the TTL gate low. Similarly, negative-going signals bias normally cutoff transistor Q1 into conduction. This drops the gate bias of FET Q4 to near zero. The resulting low drain-source resistance also allows the TTL input to go low.

Biasing via the scheme shown in Fig. 1b greatly increases the sensitivity of the circuit at the cost of three additional parts—diodes D3, D4 and D5. Diode D4 reduces the required trigger voltage to only 0.4 V, allowing the use of a 10X scope probe on 5-V CMOS. Shunt diodes D1 and D2 protect the base-emitter junctions of Q1 and Q2 from reverse breakdown.

The basic circuit can even be used as a frequency doubler under certain circumstances. Because of the auto-polarity feature, the circuit will respond in both directions to signals symmetrically disposed about ground, and produce a pulse output at twice the incoming rep rate. However, unlike many digital frequency doublers, the width of the output pulses is roughly proportional to period.

Doubling will not occur with unidirectional logic. However, for maximum versatility, a switch can be installed at the input to the TTL gate to select positive logic only, negative logic only or both (Fig. 1c).

M. J. Salvatti, Engineer, Sony Corp., 47-47 Van Dam St., Long Island City, NY 11101. CIRCLE NO. 313

1. The basic level-converting circuit (a) can couple a wide range of logic families of either voltage polarity to TTL. The 1-to-15-V range of the basic circuit is extended down to 0.4 V with the addition of three diodes (b) and an optional switch can be added to make the circuit polarity-sensitive (c).
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**Ideas for design**

**Float charger independently recharges two lead-acid cells connected in series**

The deceptively simple circuit in the figure can simultaneously float-charge two series-connected sealed lead-acid batteries, with only one adjustable float voltage. As an added bonus, the circuit inherently compensates for the required variation of float voltage with ambient temperature.

When two rechargeable batteries—especially sealed lead-acid—are wired in series and have different capacities, or have been discharged to an unequal degree, you ordinarily use a separate charger for each battery. However, this float-charger circuit can do as good a job as two chargers.

The values shown are for a series combination of two 6-V, 1.2 A-h batteries, but they can be scaled to other batteries. With R₄ fully counterclockwise, Q₁ doesn't conduct and the triac can trigger each time the input voltage exceeds the voltage at MT₁ by about 1.5 V. When the input is positive, current flows in battery B₁, and in B₂ when the input is negative. With R₄ adjusted clockwise, a clamp level produced at the triac gate prevents triggering, unless the MT₁ voltage is lower than the clamp voltage by about 1 V.

Thus, each battery charges independently, and the point of triggering for each retards separately to supply less current until the batteries no longer charge, except for an occasional burst to boost a sagging terminal voltage.

The clamp voltage at MT₁ is set by R₄ with both batteries disconnected. For the 6-V batteries, set MT₁ to 8.8 V (17.6-V pk-pk clipped sine wave), which yields a float voltage of 7 V. For best results make the adjustments at 25°C. The float voltage will then vary with temperature by about −15 mV/°C and effectively match the charge voltage needed by the battery.

Arnold Frisch, VP/Engineering, Zygo Industries, Inc., P.O. Box 1008, Portland, OR 97207.

**IFD Winner of April 12, 1977**

**Terry Dollhoff,** Dir. of Computer Science, Acuity Systems, Reston, VA 22090 and **Jim Ferry,** President, Ross Corp., 9218 Brian Dr., Vienna, VA 22180. Their idea “A Programming Controller for the 2708 EPROM Copies Data In-circuit” has been voted the Most Valuable of Issue Award.

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With a new kind of subnanosecond logic called "base-coupled logic" (BCL), logic devices developed for future digital telecommunications systems promise more than 1-Gbit/s bit rates.

Composed of base-coupled current-mode switches and emitter followers, the BCL elements use a 2.2-V supply, which is lower than that for ECL. In fact, BCL elements dissipate less power and have propagation delays, rise times and fall times of about 300 ps.

Fabricated by Siemens of West Germany, the BCL devices beat ECL elements further by having negligible Miller capacitance and using only one temperature-sensitive base-emitter junction in series with the supply line.

In the basic BCL gate structure, Q1 and Q2 form a current mode switch (see Fig. 1). The gate input is applied to the base of one of the emitter followers (Q3). Two complementary outputs are available from the collectors of Q1 and Q2. The current source, I8, is provided to prevent saturation, which would reduce switching speeds.

The switching curves for the BCL logic-gate inverter (Fig. 1) are shown in Fig. 2. These curves apply for a reference voltage (Vg) of -0.3 V and a supply (VEE) of -2.2 V.

The AND and OR functions are obtained by replacing Q1 with a multi-emitter transistor (Q1A in Fig. 3), in which each emitter has its own input emitter follower. A NAND output is also available from the Q2 output. Parallel-input emitter followers driving a single emitter-version of Q1A give the OR/NOR functions.

A fast R-S flip-flop can be made with only six transistors, and a D-type flip-flop with seven.

The prototype devices are hybrids using thin-film technology. This avoids the parasitic inductances and capacitances associated with transistor packages.

Noise down, speed up in low-voltage photodiode

Low noise, high speed, high quantum efficiency and relatively low operating voltage characterize an avalanche photodiode (APD) to be used in fiber-optic communication systems.

The device responds to wavelengths between 0.6 and 0.94 μm with better than 80% external quantum efficiency. At room temperature, the dark current is only a few picoamperes.

In the new device, developed at the Central Research Laboratories of Nippon Electric Company Ltd., Japan, both avalanche and drift regions are formed by epitaxial growth. Moreover, double epitaxy simplifies the subsequent processing and leads to good reproducibility.

The variation of the multiplication factor and dark current with the bias voltage are shown in the figure. The APD consists of high-low p-π layers and a planar junction with an n-type guard ring. The π-layers have more than 60 Ω-μm resistivity, typically, and are about 20 μm wide. For the p layers, 3 × 10²⁸/cm³ impurity concentrations and 6.8 μm widths have been used. But these values can be altered for tradeoffs between noise and operating voltage.

A shallow phosphorus diffusion forms the n+ layer; the junction is about 0.3 μm deep with a diameter of 270 μm. The APD's optical window has an antireflection coating.

Because the relationship between multiplication factor and bias voltage is fairly smooth, automatic gain control and temperature-stabilization circuitry can be relatively simple.

The device was tested in a 0.83-μm optical pulse communication system. The average signal level required to achieve a bit-error rate of 1 × 10⁻⁹ was found to be -51 dBm at 100 Mbits/s and -42 dBm at 400 Mbits/s.
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Lillian Herold is Purchasing Manager, Kantz Electronics Industries, Clifton, New Jersey. Kantz designs and prepares prototype circuitry for printed circuit boards and provides manufacturing facilities for PC board production. Her directory? Electronic Design's GOLD BOOK.

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Ms. Herold uses the GOLD BOOK about 15 times a week. Among other purchases, she has recently ordered 300,000 resistors, 20,000 sockets, solder bars, a wave soldering machine and an axial forming machine through its use.

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Alphanumeric printer handles 240 char/s

Centronics, Hudson, NH 03051. Thomas Eftler (603) 883-0111. P&A: See text; 4 to 8 wks.

A high-speed, low cost printer, the Micro-1, prints at 240 characters per second. Aimed at the home, hobby and microprocessor markets, the printer costs just $595 including case, power supply, 96 character ASCII generator and interface, paper roll holder, low paper detector, bell, and multiline asynchronous input buffer. Producing copy on aluminum coated paper by discharging an electric arc to penetrate the coating, the printed characters are impervious to light, temperature and humidity. The microprinter can produce copy at a rate of 180 lines per minute on 4.75-in. wide roll paper and provides the user software selection of 20, 40, or 80 columns.

Combination µP includes RAM, CPU and clock

Motorola Semiconductor, 3501 Ed Bluestein Blvd., Austin, TX 78721. (512) 928-2600. From $25 (unit qty); stock.

The MC6802, a combination µP, contains the CPU, a 128 x 8 RAM and a clock oscillator with driver circuit. And, the MC6802 is completely software compatible with the MC6800. It can be used with the entire M6800 family of parts and is expandable to 65 kwords. When combined with the MC6846 (to be introduced later this year) a two-chip microcomputer is possible for those systems where a minimum configuration with full expandability is desired. The on-chip RAM has an additional feature: the first 32-byte section has a low-power mode that, when coupled with a VCC standby source, will retain memory during power-down conditions. The MC6802 is available in either a plastic or ceramic 40-pin DIP.

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The RMRV-8K, an 8 k x 16 E/PROM memory board, is designed for use with the LSI-11 microcomputer from Digital Equipment Corp. It occupies one dual height module slot in an LSI-11 backplane. Packaging density is achieved by using the UV erasable 2708, an 8192 bit PROM. Addressing is impervious to light, temperature and humidity. The microprinter can produce copy at a rate of 180 lines per minute on 4.75-in. wide roll paper and provides the user software selection of 20, 40, or 80 columns.

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Development Aids Simplify Design
The SDB/AIM provides the user with the ability to create and edit Source Listings using the Resident Text Editor and assemble into Object Code using the Resident Assembler. Object Code may then be copied to AIM-70 for execution. This is a true in-circuit-emulation configuration. Real time execution of the target system code, breakpoint insertion, and single-step operation are a few of the features available with this system.

With completion of software development and debugging, prototypes may be emulated for field testing and evaluation using the compact PROM-based EMU-70. This capability allows exact verification of code before committing to mask programmed MK 3870's.

*The MK 3870-based VAB-2: a typical example of logic replacement.
For customers desiring to evaluate the MK 3870 in an actual application, a pre-programmed version is available for $50. This particular device has been designed to replace much of the logic normally required for sophisticated video terminal applications. The complete Video Adaptor Board (VAB-2), is available through our distributors for $195. Call or write today for a data sheet.
How to defend against attack by air,

Series 1 panel sealed lighted pushbuttons are qualified under MIL-S-22885.

FW solid state self-contained proximity controls provide high reliability and long life.

Panel sealed solid state keyboards in a variety of arrays.

TL toggles offer environment-proof sealing and many circuit options. TW provides switching versatility in a smaller size.

SE and XE miniature basic switches are environment-proof. HM version provides hermetic sealing and larger-sized HT withstands extreme temperatures.

EN is environment-proof limit switch with variety of actuators, circuitries, and electrical ratings. HS is hermetically-sealed version.
Programmer boards do EPROMs or bipolar PROMs

Zilog, 10160 Bubb Rd., Cupertino, CA 95014. Dave West (408) 446-4666. From $475: 30 days.

Three programmer boards have been added to the company's MCB family of microcomputer boards. The Z80-PPB/EPROM programmer board is designed for programming 24-pin EPROMs of the 2708 or 2704 variety. Software provides the user with the capability to program, verify, list and duplicate. The Z80-PPB/PROM programmer board is intended to program 16 and 24-pin Harris PROMs of the 7620, 7621, 7640, or 7641 type. Like the PPB/EPROM version, the PPB/PROM board gives the user the software to program, verify, list and duplicate. A composite of the two boards is the Z80-CPB/PROM that allows users to program 2708/2704 EPROMs and Harris 7620, 7621, 7640 and 7641-type PROMs.

CIRCLE NO. 306

Pre-etched boards hold Z80 CPU or 8 k of RAM

Ithaca Audio, Box 91, Ithaca, NY 14850. Steven Edelman (607) 272-3271. $25 (2102 board); $35 (Z80 board); stock.

Pre-etched printed-circuit boards, compatible with the S-100 bus, are available for either an S-100 memory bank or for a Z80 CPU. The memory board holds 64 of the 2102 or equivalent static RAMs and includes full buffering on all address and data lines, memory protect/unprotected and optional selectable wait states. The Z80 CPU board provides all 8080 compatible control signals, including phase 1 and phase 2 clocks and sync. Provisions are also made for one 2708 EPROM on the board for reset and jump so that the board can operate without a front panel.

CIRCLE NO. 307

Microcomputer diagnostic system goes to the field

Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. $1520 (console); $480 (Probe 8080A); 90 days.

The µScope 820 microprocessor system console is a portable microcomputer system developed to support OEM test and maintenance of µP systems. Unlike conventional instruments, the µScope console provides active control over microprocessor-based systems. The unit is a general purpose support system based on the 8085 µP and uses “personality probes” and overlays for its keyboard-display panel to reconfigure the system. For 8080 systems, the µScope's 8080A probe can be used with the console. The probe is supplied with a keyboard-display overlay and personality ROM that uniquely configure the basic instrument. The panel can be used to monitor, display and alter register, memory and I/O values of the system under test. It also gives complete control over microprocessor operations including halt, single-step, run with display and run in real-time. For more rigorous diagnostic tasks, the console has a 32-bit maskable hardware breakpoint with optional courses of action after a breakpoint match, a 256 x 32-bit trace memory, and a 128-byte overlay RAM for real-time entry of test routines via the keyboard. The console is packaged in a 19 x 15.5 x 7-in. carrying case and has a self-contained power supply.

CIRCLE NO. 308

Filler

It's really fortunate that we have such terrible reliability. That gives us a chance to show how great our Service Department is.
Hurrayyy!

PMI's DAC-08 does have a second source!

Whaddayaknow! When we challenged the DAC-08's "second sources" to come forward with 100 1/4 LSB-grade equivalents, we really didn't think anyone would come forward. But someone did. And we're glad. National, Signetics and AMD didn't show at all. Not a word. Then, at the eleventh hour, Fairchild sent over an entry.

And they worked O.K. They didn't meet all of our data sheet specs, but they were pretty fast. In settling time, they were faster than we are at the trailing edge. But then, we were faster at the rising edge, so it came out a wash. In other areas such as zero scale offset, power consumption, and non-linearity, PMI's were better, but theirs did meet the spec.

The tests, by the way, were made with our standard DAC-08 production test fixtures and equipment, and supervised by DCA Reliability Laboratory. Copies of the test report are available—just ask for one on your letterhead.

It's good to know that our DAC-08 now has a second source. Good for business. Good for customers.

So now we all know who really makes and delivers DAC-08's and their "equivalents." You can get the original, high-quality DAC-08 from PMI and its distributors.

Tests supervised by DCA Reliability Laboratory.
North Star Computer, 2465 Fourth St., Berkeley, CA 94710. (415) 549-0858. From $1599 (one drive); stock.

Using the 4 MHz Z80, the Horizon microcomputer comes with 16 kbytes of memory and a disc controller with one or two Shugart minifloppy disk drives, and full extended disc Basic. A serial I/O port is included for connection to any standard baud-rate terminal. Options for the Horizon computer include additional disc drives, hardware floating point arithmetic board, 24-line by 80-character upper and lower-case video display controller (VDC) board, and a 16 k memory board with parity check. When used in conjunction with the 16 k memory board, the VDC board will provide high resolution (480 by 250) graphics on a TV monitor. The Horizon computer uses the widely supported S-100 bus, allowing possible use of a large selection of available peripheral products.

CIRCLE NO. 309

**Assembled microcomputer comes ready to operate**

Audio Engineering, 121 Wisconsin NE, Albuquerque, NM 87108. (505) 255-6451. See text; stock.

Fully assembled and ready to operate, the Motorola MEK6800D2 kit just needs a regulated 5-V, 1-A supply. The assembled version, Model SY1-068, includes sockets for all ICs, a stand for the CPU board, and an attractive case for the keyboard/display board. The SY1-068 has a 1-k monitor, 256 bytes of RAM, serial I/O (used for cassette interface), parallel I/O, and crystal clock. The assembled system costs $269, and the case for the keyboard costs an additional $12.50. An extra 128 × 8 RAM can be obtained for $7.50 and a power supply kit with 60-Hz clock adds another $29.95.

CIRCLE NO. 310
**Single board computer uses 8080 processor**


The SBC 80/05 single board computer, at a cost of less than $200 in OEM quantities, is only one-third as much as previous systems with multiprocessor bus structures. The board also cuts the power requirement since it operates from just a +5-V supply. In addition to a complete central processor with crystal clock, four-level vectored interrupt control and arbitration/logic for operation on the company’s Multibus, the SBC 80/05 computer contains memory, parallel and serial I/O (input-output), and an interval timer. Also available is the SBC 80P05 prototyping package. It includes a complete SBC 80/05 with a resident monitor program that facilitates program loading, execution and debugging, a modular card cage/backplane, a full complement of I/O and power supply cables, EPROMs, I/O drivers and terminators, and complete documentation.

**Core memory provides 8 k for micro storage**

Micro Memory, 9438 Irondale Ave., Chatsworth, CA 91311. (213) 988-0070. $850; stock.

Designed specifically for nonvolatile operation with the S-100 bus IMSAI and Altair microcomputers, the MM-S100 memory provides 8 k x 8 of core storage. The memory system eliminates data loss upon power removal and can plug directly into existing S-100 bus microcomputers. Cycle time is 1 µs, with no wait states required. On board module selection is available in 4-k increments up to 64 k. The memory module measures 6 x 10 x 1 in.

**Expansion memory for 6800 system holds 16 k**

Motorola Semiconductor, 3501 Ed Bluestein Blvd., Austin, TX 78721. (512) 928-3000. $295 (1 to 10); 4 wks.

A new memory system for expanding the memory capacity of the MEK800D2 kit, the MMS 69104, provides up to 16 k x 8 of RAM storage. The board is pinout compatible with the "D2" kit and measures 6 x 9.75 x 0.44 in. Access time is 650 ns, max, and read or write cycle times are 1.6 µs. The board requires +5 V at 920 mA, +12 at 450 mA and −12 V at 10 mA when active.

**Microcomputer hardware includes all components**

Wintek, 902 N. 9th St., Lafayette, IN 47904. Paul Wintz (317) 742-6802.

A complete line of backplanes, card racks, power supplies, and associated items has been added to the company's microprocessor support. These accessories allow the user to quickly assemble a customized microcomputer system using the company's 4.5 x 6.5-in. microprocessor printed-circuit boards with standard, 44-pin connectors. Available cards include the control, RAM, ROM, EROM programmer, analog interface, data acquisition, relay driver/sensor, cassette interface, floppy-disc interface, console, CMOS RAM with battery back-up, and telephone tone transmit/receive modem.

**Magnetic card & reader provide data storage**

Vertel, 167 Worcester St., Wellesley Hills, MA 02181. August Toda (617) 235-2330. $99 (less electronics), $258 (complete); 60 days.

Using a credit-card sized, 1024 byte, programming media called the Kilobyte Card, the Series KB-31 Microloader is designed for low cost program loading. The Kilobyte Card uses four magnetic stripes (tracks), with two "F2F" channels encoded on each track. The KB-31 "Microloader" records and reads both channels per stripe in one cycle, at 5 kbytes per minute. Measuring only 3.2 x 8.19 x 2.48 in. (8.2 x 20.8 x 6.3 cm), the Microloader has a diecast frame and chassis, and a constant-speed governed motor.

**Microcomputer trainer gives hands-on practice**

Integrated Computer Systems, 4445 Overland Ave., Culver City, CA 90230. (213) 559-9265. $545; stock.

A beginner-oriented, software/hardware training course, based on the 8080A, is designed for self-study. With built-in keyboard and display, no expensive teletypewriter or CRT terminal is required. Designed for use in the home or office, the course (No. 125) includes all system hardware, software and information best suited for learning to program and use an 8080-type microcomputer system. A 650-page workbook/text teaches 8080 instructions, programming, debugging and hardware interfacing through 33 hands-on exercises. Memory includes 512 bytes of CMOS RAM (maximum 1 k on board) and 1 k of electrically erasable PROM. I/O ports for hardware experiments, cassette interface, etc. are also included.

**Microprocessor system built around the 6800**

Digimetric, Div. of Sybron Corp., 730 Kalumath St., Denver, CO 80204, Mike McGinnis (303) 534-1190. $5000 (typical); stock.

Designed for OEM users, the Series 6000 microcomputer system comes with a 16-slot mainframe and uses the 6800 µP. The 6015 processor board comes complete with powerfail auto restart, real-time clock and hardware priority interrupt, a loader and Demon monitor in ROM and 32 k of static RAM. A full floppy-disc operating system is available, which supports an assembler, editor and the real-time Basic 6 interpreter. The system also supports a macroassembler and linking loader. Memory is available in 2-k or 8-k increments of static RAM and in 4-k increments of PROM. A full line of I/O cards is available including an integrating a/d and a control interface card with eight independent triacs.
Here are two ways to measure ceramic capacitor reliability

**40**

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You'll find our ceramic capacitors functioning in some of the toughest environments known to man. Here are just a few of the programs. Space: Surveyor, Mercury, Gemini, Apollo (Command Module, LEM, PLSS). Defense: Minuteman II and III, F-14, F-15 and F-16, Polaris and Poseidon, Sparrow, Hawk and Maverick, F-111 and the B-1 bomber.

**15**

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DATA PROCESSING

Digitizing tables boast high accuracy

Altek Corp., 2150 Industrial Pkwy., Silver Spring, MD 20904. (301) 622-3906. From $5000.

A new method of grid manufacture improves the accuracy of Datatab digitizing tables for computer-aided drafting and mapping. The glass-based grids are easily backlit to permit digitization of film negatives and other translucent materials, and provide an absolute accuracy of up to ±.002 in. Table sizes range from 12 x 12 to 42 x 60 in. The variable-intensity lightbox uses standard fluorescent bulbs and a sheet of translucent plastic to mask out the shadows produced by the grid wires.

CIRCLE NO. 329

Dual-floppy smashes
$1000 barrier

Southwest Technical Products, 219 W. Rhapsody, San Antonio, TX 78216. $995 (Kit).

The MF-68 Minifloppy dual-disc kit is designed for use with the SWTPC 6800 system and provides all hardware and software for a dual-disc operating system including two assembled Shugart drives. It can be expanded to four drives with the MF-6X expansion kit ($850). Software includes disc Basic and a floppy-disc operating system (FDOS). The expansion kit includes power supply, chassis, cover, and two assembled Shugart drives.

CIRCLE NO. 330
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Data Processing

Portable terminal never forgets

Computers, 25 N. Ave., P. O. Box 421, Burlington, MA 01803. (617) 273-1550. $3985.

The Miniterm Model 1205 portable data terminal combines 8-k RAM, Mini-cassette tape transport, and modem/audionic coupler in a compact package. Editing memory and Mini-cassette storage make it possible to edit data off-line, then send them directly to the computer at high speed. Each cassette stores 68,000 characters and the RAM is expandable to 82 k. Other features include 35 char/s printing speed, 1000 char-line buffer, upper/lower case typewriter, built-in acoustic coupler with automatic error compensation and RS232 interface. The terminal can also be rented at $195/mo.

Wand reads more characters

Recognition Equipment Inc., P.O. Box 22307, Dallas, TX 75222. (214) 438-8611. $1810 (100 qty).

An improved hand-held OCR WAND-reader, the Class 600 system, reads a substantially longer line of alphanumeric characters than previous WANDs. Connected directly to terminal, computer and other data processing equipment, the optical character-recognition system accepts human-readable source data and transmits the information directly to a terminal or computer. The Class 600 reads data at speeds of 30 to 130 char/s with less than one error per 10,000 characters scanned. In addition to the OCR-A and B fonts, the Class 600 also reads the numerics in type fonts 1403, 12-F and 407-1.

Output driver sinks 300 mA

Adac Corp., 15 Cummings Park, Woburn, MA 01801. (617) 835-6668. $300 (1-4 qty); 4-6 wks.

The Model 1632-HCO module contains 32 discrete latched outputs with 300-mA current capability on a half-quad card (81/2 x 5 in.). It plugs directly into the backplane of a DEC LSI-11 microcomputer and contains bus transceivers, 16-bit status register, and flexible addressing. Two 20-pin headers and cables allow direct connection to the loads. A 16-bit unit (1616-HCO) is also available at $225.

One head for every track

Alpha Data, 20750 Marilla St., Chatsworth, CA 91311. (213) 882-6500. From $3000; 12 wks.

The Model Eighty disc has a maximum capacity of 8 Mbytes with an average access time of 8.5 ms. It uses one retractable head per track, and a metal-plated disc, sealed in a head chamber, eliminating the contamination of oxide-coated discs. The Model Eighty features new head/disc magnetics, efficient data coding, modern read-back signal equalization, good noise immunity, and easy access to all replaceable parts. The unit is compatible with all Alpha Data controllers for Data General and DEC computers. A simple change of one interface card permits emulation of other manufacturers' products.

Speed up data communications

Syntech Corp., 11810 Parklawn Dr., Rockville, MD 20852. G. Fritkin (301) 770-0550.

A character-oriented converter/buffer, the MPB-200C, allows most asynchronous communications systems to be upgraded to the higher speeds of synchronous modems. It can be used on the dial network or on private lines, both point-to-point and multipoint, in full duplex, half duplex or simplex. The MPB-200C accepts synchronous data from the modem receiver and delivers it to the terminal or computer in the original character format, but at the higher data rate.
DATA PROCESSING

Feed mini/micros with 'Serial Box'


The 23-lb "Serial Box" is a portable, interactive terminal that interfaces with any mini/microcomputer through an RS-232 or current loop port, at data speeds from 110 to 9600 baud. Dubbed the Model CO-4420, it consists of a 1-Mbyte direct-access tape drive, a full ASCII keyboard, a 40-character plasma display, an RS-232 port and a µP controller, all built into an attach case. The CO-4420's high reliability results from the LINC tape drive. Without display or keyboard as Model CO-4410, the unit adds mass-storage capability to terminals for $2850.

CIRCLE NO. 336

24 GHz

-30 dBm sensitivity, FM tolerance standard

Just those three features alone put Systron-Donner's new Model 6054B Microwave Counter in a class by itself! But there's lots more . . .

- Coverage: 0.02 to 24 GHz in one band with one connector input.
- Sensitivity: -30 dBm to 10 GHz; -25 dBm to 18 GHz; -20 dBm to 24 GHz.
- Dynamic range: No dead zone! Operative over the complete range up to +30 dBm (1 watt).
- Protection: Flashing LED's provide early warning of pending overload.
- FM tolerance: Full channel loading and heavily modulated signals with rates up to 10 MHz are measured easily.
- Models: If you don't need 24 GHz coverage, S-D also offers 1.25, 4.5, 6.5 and 18 GHz automatic counters.
- Information: Call Scientific Devices or contact S-D at 10 Systron Drive, Concord, CA 94518. Phone (415) 676-5000. Overseas, contact Systron-Donner in Munich; Leamington Spa, U.K.; Paris (Le Port Marly); Melbourne.

SYSTRON DONNER

CIRCLE NUMBER 65

Line printer switches character sets

Data 100 Corp., 6110 Blue Circle Dr., Minneapolis, MN 55435. (612) 941-6500. See text; Sept., 1977.

Optical character-recognition printers with speeds of 125 and 250 lines/min meet National Retail Merchants Association (NRMA) standards. Both OCR A and OCR B character codes are available. The printers can also be used for normal data processing applications by simply changing the print ribbon. Up to 132 columns are printed on fan-fold paper widths up to 17-1/2 in., at six lines/in. and 10 char./in. The 125 lines/min printer costs $5000, the 250 lines/min $7000.

CIRCLE NO. 337

Laser scanner zips through bar code


Two models of bar-code-reading laser scanners were developed for materials handling (Model OBR-70-1) and data entry systems (OBR-70-2). Both models consist of a scanner unit and a decoder unit. The scanner of the 70-1 has a wide scanning range (up to 55 in.), great depth of field (40 in.), and high reading speed for objects moving up to 150 in./s. Model OBR-70-2 is compact in size and thus most suitable as an input device in data-entry systems.

CIRCLE NO. 338

Replacement terminal has diagnostics


The Model 0752 stand-alone data entry terminal is a plug-compatible replacement for the IBM 3755, and supports IBM 3784, 3786, and 3788 printers. The unit offers light pen, OCR wand, and diagnostics which test the 0752 completely in the local mode. The Model 0752 can also be leased for $98/mo.

CIRCLE NO. 339

ELECTRONIC DESIGN 17, August 16, 1977
Featherweight printer is fast, versatile

Datel Systems, 1020 Turnpike St., Canton, MA 02021. (617) 828-8000. From $425.

The AIP-40 prints up to 40 columns on adding-machine roll paper using a 5 × 7 dot matrix impact printer. Up to 64 ASCII-coded characters are printed at a rate of 50 char/s, directly from the interface circuits offered with 8080, 6800 and other μPs. Printing mechanism life is 400 million characters and one 170-ft paper roll is good for 12,000 lines. The AIP-40 measures 13.5 × 13.25 × 7.12 in. (343 × 337 × 181 mm) and weighs 6 lb (2.7 kg). Serial input models are available ($625).

CIRCLE NO. 340

Let the ADAS do the walking


The ADAS Universal Data Reporting System permits users to obtain readings from remote instruments by dialing a telephone number. The unattended remote stations automatically digitize the desired variables, insert the values into a pre-programmed 256-word memory, and transmit the formatted report into the user's teleprinter, computer or tape recorder. The system transmits in ASCII, R3-232 and Bell 103, and interfaces directly with 8-bit (or larger) μPs, minis, or timeshare terminals. ADAS also permits continuous switch-selectable supervision of multiple remote stations through an ASCII video monitor.

CIRCLE NO. 341
ICs & SEMICONDUCTORS

Rectifiers handle up to 16 kV

Solid State Devices, Inc., 14830 Valley View Ave., La Mirada, CA 90638. Dee Peden (213) 921-9660. $0.49 to $1.98 (unit qty); stock.

The S093-4044 series of power rectifiers offer peak inverse voltages from 4 kV to 16 kV in 2-kV increments. Specifications include a recovery time of 250 ns and a maximum average half-wave current of 10 mA. Maximum forward voltage drop is 12 V up to 8-kV PIV and 24 V from 10-kV to 16-kV PIV. Maximum reverse current at 25 °C is 1 µA at maximum rated voltage, 40 µA at 100 °C.

CIRCLE NO. 342

Four package types in high power SCRs

Teccor Electronics, 1101 Pamela Dr., Euless, TX 76039. R. L. Saunders (817) 267-2601. $0.18 to $0.27 (10,000-qty).

Current ratings of up to 4 A at 400 V rms are available in four versions of the industry standard TO-202AB package. Designated T-106 and T-107, the packages can also be configured in five different lead bending versions. The T-106 has a 200-mA gate sensitivity, 3-mA holding current and 20-A surge capability. The T-107 has a gate sensitivity of 500 mA, holding current of 5 mA and a 15-A surge capability. Applications for the devices include motor controls, lighting controls, timers, and small ignition systems.

CIRCLE NO. 343

Opto-isolators operate at megabit data rates


Replacements for the VMP1 and VMP2 power MOSFET devices are available with upgraded specs. The 2N6657 (VMP1) and 2N6660 (VMP2) offer lower input current and lower ON resistance than their earlier counterparts, resulting in greater circuit efficiency and decreased power dissipation. Housed in a TO-39 package, the 2N6660 can dissipate 6.25 W — 1.25 W greater than the 5 W VMP2. The 2N6657, in a TO-3 package, dissipates 25 W. Both units switch typically in 10 ns, have 60-V breakdowns, and can handle up to 3 A. Low drive requirements (100 nA) allow the units to directly interface with CMOS, TTL and other logic families.

CIRCLE NO. 344

Four package types in high power SCRs

CIRCLE NO. 342

Demodulate FM signals with a phase locked loop

Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-7700. $1.25 (100-qty); stock.

The demodulation of FM and FSK signals can be performed without additional circuitry using the NE564. Operating from a single +5-V-dc supply, the TTL-compatible unit contains a VCO, limiter, phase detector and a post-detection processor. Frequency drift is rated at 400 ppm/°C and signal-to-noise ratio is typically 40 dB. The 16-pin DIP uses Schottky clamped transistors at both inputs and outputs and contains a provision for external loop-gain control.

CIRCLE NO. 347

Low power DAC conforms to European PCM systems

Precision Monolithics, 1500 Space Park Dr., Santa Clara, CA 95050. Al Chame (408) 246-9222. DAC-87EX: $9.90, DAC-87CX: $9.00 (100-qty); stock.

A digital-to-analog converter, the DAC-87 is specifically designed to conform with the CCITT exponential "A" characteristic in European PCM systems. Features include 500-ns settling time and power consumption of 141 mW. The device is available in two models covering the 0 to 70 °C temperature range: the DAC-87EX with ±1/2 step accuracy and DAC-87CX with ±1 step accuracy. Housed in an 18-pin hermetically sealed DIP, the device interfaces with DTL, TTL, HTL, MECL or CMOS inputs.

CIRCLE NO. 348

CIRCLE NO. 349
Berg Quickie Connectors are the logical cable interface for Digital minicomputers

Berg Quickie™ Connectors rapidly, reliably terminate multi-lead, flat, round conductor cable—without pre-stripping. Quickie designs allow for visual inspection before and after assembly.

Digital Equipment Corporation likes the Quickie connector’s ease of termination and how its askewed tines strip away insulation to assure positive electrical contact. They like the way Quickie Headers latch to maintain connection integrity through vibration and impact. Digital has found it can rely on Berg ... to supply the products and the application machines that precisely meet its demanding interconnection needs.

Berg is experienced. We read interconnection needs like Digital computers read data. We have the products, the background, and the back-up to do the job. Your job. Let’s work on it, together. Berg Electronics, Division E. I. du Pont de Nemours & Co., New Cumberland, Pa. 17070—Phone (717) 938-6711.

We serve special interests—yours!
Microwave transistor offers low noise figure


The AT-4691 bipolar microwave transistor has a typical noise figure of 0.8 dB at 4 GHz for collector currents between 2.5 and 20 mA. Packaged in a hermetically sealed 0.07-in. square alumina stripline, the 0.5-micron emitter structure gives the device a shallow curve for noise figure vs collector current. Typical figures are $G_{\text{NF}}$ of 9.5 dB, minimum gain of 12 dB, both at 4 GHz. Testing includes 100% dc, rf and fine leak with additional screening and burn-in available.

**CIRCLE NO. 356**

10-year life predicted for pulsed operation LED

Optron, 1201 Tappan Cir., Carrollton, TX 75006. (214) 225-6571. OP 135: $1.44 (1000-qty), OP 136: $0.74 (1000-qty); stock.

Average power degradation of less than 10% after 1 million hours of operation is claimed for the OP 135 and OP 136 devices. The gallium-arsenide chips have typical power outputs of 20 mW for the OP 135 and 35 mW for the OP 136 with an input pulse of 1 A, 10 ms at a 10pps rate. Both units are available in a standard TO-18 package with a choice of either lens or flat window. Although specifically designed for pulse applications, the device can be operated in a continuous mode.

**CIRCLE NO. 357**

Temp compensation improves BIFET op amp

Precision Monolithics, 1500 Space Park Dr., Santa Clara, CA 95050. Shelby Givens (408) 246-9222. Stock.

Input bias currents of 9-nA maximum at 125-C ambient are maintained by a temperature compensation circuit in the OP-15. This can result in significantly lower droop rates in high speed sample-and-hold circuits. The op-amp features a maximum input offset voltage of 500 µV, a slew rate of 17 V/µs and a settling time of 900 ns. Two models, one covering the 0 to 70 C and the other covering the -55 to +125 C temperature range, are available in 8-lead TO-99 packages. The unit was designed to hold error correcting manual adjustments in systems to a minimum.

**CIRCLE NO. 358**

Solid-state controller aims at consumer market


A clock/timer circuit with full time-keeping and alarm capability has onboard circuitry to directly drive a four-digit display. The FCMT7040 also contains two independent keyboard settable registers—a 99-min, 59-s countdown timer and a 24-h start/stop timer. Common anode LED displays of up to 25 mA in the duplex mode can be driven under single-pin control. Other on-board features are a back-up oscillator, internally generated alarm tone, power-up-clear and an additional 10-min timer. Clocks and clock radios, microwave ovens and thermostat timers are typical applications for the device.

**CIRCLE NO. 359**

Create musical sounds with digital noise unit

American Microsystems, 3800 Homestead Rd., Santa Clara, CA 95051. (408) 246-0330, $2.25 (999-qty).

The S2688 noise generator provides the sounds of drums, maracas, brushes and other musical instruments electronically. A 17-stage shift register and exclusive-OR logic produce a pseudo-random broadband white-noise signal. The unit, an exact replacement for the MM5837, contains a reseatability feature to ease parts testing. Output amplitude and noise quality are uniform over the frequency range.

**CIRCLE NO. 360**

Call your nearest ISC sales representative.

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**CALIFORNIA**: San Diego
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CIRCLE NUMBER 69

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CIRCLE NUMBER 70

ICs & SEMICONDUCTORS

Reference diodes have 2-ppm temperature specs

American Power Services, 7 Andover St., Andover, MA 01810. Robert Dimodana (617) 475-4074.

Low level temperature-compensated zeners in JEDEC registered 250-mW and 500-mW series are made with oxide-passivated junctions. The DO-7 packaged units have tolerances of ±2 ppm/°C for the 500 mW series and ±5 ppm/°C for the 250 mW series. The 6.2 V dc devices included in the 500 mW series are the JEDEC types 1N985, 1N940, 1N941, 1N3154, 1N3779 and 1N4565. In the 250 mW series, also at 6.2 V dc, are the 1N821, 1N4765, 1N3496 and 1N4775. The units are also available in either dice or wafer form.

CIRCLE NO. 361

Generate musical scale with 7-stage counter

Fairchild, 464 Ellis St., Mountain View, CA 94042. Bill Callahan (415) 962-3816. $1.17 (1000-qty); stock.

All of the tones of the chromatic musical scale, across eight octaves, are generated by the F4727 counter. Based on a primary chromatic scale, the device generates each of the 12 flats, sharps and natural notes of the seven additional octaves of the primary scale. To generate the entire musical spectrum requires 12 F4727s. Design features of the seven-stage counter minimize interface and cross-talk problems.

CIRCLE NO. 362

4-input gate boasts 500-ps switching speed

Plessey Semiconductors, 1611 Kaiser Ave., Irvine, CA 92714. (714) 540-9979. $12 (100-qty); stock.

Designed to be fully compatible with ECL III and ECL 10K, the SP16F60 dual OR/NOR gate typically switches in 500 ps. The 16-pin ceramic DIP drives 50-Ω loads and is internally temperature compensated to keep its threshold point in the center of the transistor region. System operation and wiring is simplified since unused gate inputs can be left open circuited. Typical power dissipation is 120 mW under no load conditions, and the unit operates over a temperature range of −30 to +85 C.

CIRCLE NO. 363

ELECTRONIC DESIGN 17, August 16, 1977
COMPONENTS

Noncontact level control senses with infrared

Aikenwood Corp., 2151 Park Blvd., Box 26, Palo Alto, CA 94302. (415) 326-2151. From $162 (unit qty); 15 days.

A modulated infrared beam in the Series 3000 level control provides noncontracting level detection. The sensors work with virtually any liquid or solid. Four different sensor heads have ranges of 1, 3, 6, and 12 ft. The sensor heads can operate through glass windows. Electronic control circuits provide multiple output signals for alarm and pump control purposes.

CIRCLE NO. 364

Float-control switch needs no bearings

Signal Systems International, P. O. Box 8, Farmingdale, NJ 07727. (201) 938-3535. $2.95 (unit qty); stock to 4 wks.

The FS101 float-control switch is a welded-steel, omnidirectional, mercury-switch position sensor. The position sensor is encapsulated within a sealed ball float. The float is weighted at the top. Two flexible, insulated control wires extend upward from the float. In normal operation, the ball is suspended by the leads. When the liquid level reaches the suspended float, the weighted ball rises slightly, then tips 180 degrees, which activates the mercury contacts. Two flexible, insulated control wires extend upward from the float. In normal operation, the ball is suspended by the leads. When the liquid level reaches the suspended float, the weighted ball rises slightly, then tips 180 degrees, which activates the mercury contacts. Two flexible, insulated control wires extend upward from the float. In normal operation, the ball is suspended by the leads. When the liquid level reaches the suspended float, the weighted ball rises slightly, then tips 180 degrees, which activates the mercury contacts.

As with zero crossing, the TA1201Q SSRs generate no RFI regardless of the power factor. The relays are 100% immune to dv/dt false triggering induced by line transients, because a custom power transistor, not thyristors, is the output switching element. The relays are rated up to 140 V ac at 0.75 A. Even without a thyristor output, the devices still carry a one-cycle surge rating of 8 A. Nominal control current is 15 mA at optional control voltages of 5 or 12 V dc.

CIRCLE NO. 367

Socket/Carrier Systems Highlight Expanded TEXTOOL Flat-Pack Test Series

Two new socket/carrier systems highlight an expanded TEXTOOL flat-pack test series capable of handling the larger LSI and MSI packages (1¾ x 1¾" maximum) with up to 96 leads. A unique feature of the -2620 plastic lid socket (above with carrier) is the availability of up to 192 contacts (96 lead Kelvin) for single or Kelvin measurements. The 96 pin -4160 socket (below) is basically a metal lid version of the -2620 socket, yet pin for pin, is less expensive for such applications as burn-in where Kelvin contact is not necessarily required. Standard or custom "snap-together" carriers fit both sockets to completely encase and protect device leads, yet are open for circuit repair. The new series also includes a versatile new staggered axial lead ZIP STRIP (below) offering zero insertion pressure testing without lead damage to flat-packs for which no carriers are available.

TEXTOOL's complete flat-pack test socket line now includes units to accept devices with 50, 52, 64, 70, 76, 82 and 96 leads (two and four sided). All sockets feature maximum device protection while insuring consistently good electrical contact. Wiping contacts eliminate "dimpling" or gold removal, and lids are reinforced in the contact area.

Detailed technical information on these and other TEXTOOL flat-pack test sockets is available from your nearest TEXTOOL sales representative or the factory direct.

CIRCLE NUMBER 71

NEW

Magnetostriuctive switch needs small displacement

Magnetoelastic Devices, Crane Ave., Pittsfield, MA 01201. (413) 445-5608. $70 to $120 (unit qty).

Model BS-6, a precision electromechanical limit switch, combines a displacement transducer with a remotely connected solid-state control unit. A signal from a high-compliance magnetostriuctive element in the transducer is compared with a signal from a similar adjustable element in the control unit to determine the state of the outputs. The nominal displacement range of the transducer is 0.025 in. and repeatability is within 0.0002 in. Standard options include one or two set points, LED status indicators, fixed or adjustable on-off differentials and logic-level or solid-state relay outputs.

CIRCLE NO. 365

Solid-state relays don't trigger falsely

Theta-J Relays Inc., 1 DeAngelo Dr., Bedford, MA 01730. (617) 275-2575. $9 (1000 qty); 6 to 8 wks.

As with zero crossing, the TA1201Q SSRs generate no RFI regardless of the power factor. The relays are 100% immune to dv/dt false triggering induced by line transients, because a custom power transistor, not thyristors, is the output switching element. The relays are rated up to 140 V ac at 0.75 A. Even without a thyristor output, the devices still carry a one-cycle surge rating of 8 A. Nominal control current is 15 mA at optional control voltages of 5 or 12 V dc.

CIRCLE NO. 366

PRODUCTS, INC.
1410 W. Pioneer Drive • Irving, Texas 75061
214/259-2676
Thick-film resistors provide ±50 ppm/°C
Du Pont Co., Wilmington, DE 19898. (302) 774-2358.

Birox 1700-Series thick-film resistors for microelectronic circuitry provide temperature coefficients of less than ±50 ppm/°C throughout the 100 Ω/square to 100 kΩ/square resistivity range. Load life, 150-C storage, humidity and thermal shock tests indicate that well under 0.5% end-of-life stability can be expected. Stability after laser trimming and subsequent processing steps permit high yields of close-tolerance resistors. Average change in resistance is 0.05% in 1000 h after laser trimming, with maximum change of less than 0.15%. Resistors change less than 0.05% during solder dipping.

Circular No. 368

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Electronics Design 17, August 16, 1977
Low profile trimmers come in three options


The 1/4-in. dia, single-turn, cermet Type A trimmer offered by A-B have three new options: A4C, A4D and A2C. A4C and A4D are low-profile horizontal versions; A4C, reverse rotation of the A4D and A4B; and A2C, reverse rotation of the A2B. In addition, Type A now uses a new ink with a TCR of typically less than ±35 ppm/°C above 250°C. The trimmers are furnished with TO-5 or 0.1-in.-grid terminal spacings for top or side adjustments. Multi-fingered wipers ensure good wiping action. Power rating is 0.5 W at 85°C. Standard values range from 10 Ω to 2 MΩ with ±10% tolerance. End resistance is less than 2 Ω at both ends of rotation. Contact resistance is typically less than 1% or 1 Ω.

CIRCLE NO. 371

Rotary switches provide binary-coded outputs

Professional Electronics, Stackpole Components Co., P. O. Box 14466, Raleigh, NC 27610. (919) 828-6201.

Rotary switches in special configurations for binary-coded applications are available in Series 100 and Series 80 switches. The Series 100 is offered with 22-1/2, 30 and 26-degree index angles for up to 10, 12 or 16-position applications. The switches have a single-input terminal and one terminal for each binary output. They are fully enclosed in environment-proof packages and come with either PC pins or solder-lug terminations.

CIRCLE NO. 372

CHECK DIGITAL IC'S FASTER THAN A SCOPE, SAFER THAN A VOLTMETER

You're looking at the most convenient and efficient way developed to check digital IC's: CSC's Logic Monitor. It speeds digital design and testing by accurately and automatically displaying static and dynamic logic states of DTL, TTL, HTL and CMOS DIP IC's. All in a compact, self-contained 16-pin circuit-powered unit.

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Very clever. Very portable. Very effective. And very reasonable, at $84.95.* See the Logic Monitor at your CSC dealer, or write for our catalog and distributor list.

CIRCLE NUMBER 72
where weight and space are critical... like this magnetron...

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For minimum space and weight, maximum power efficiency and consistent performance, design your unit around T & S high performance magnetic alloys... Alnicos 8C, 8HC, 8HE, and 9Nb. You can get up to twice the energy product, permitting the use of smaller pieces and assemblies, with less weight and at a lower unit cost. The high coercive force of these magnetic alloys... up to four times that of Alnico 5... reduces stray fields and allows lower leakage factors, permitting more efficient structures for replacing Alnico 5 designs. And these alloys have low temperature coefficients and extreme magnetic stability... are easy to magnetize and stabilize.

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PACKAGING & MATERIALS

Magnetic catches mount with adhesive


Southco's No. 02 magnetic catches now can be ordered with adhesive back for quick mounting. Available in 2, 1-1/4 and 1-1/8 in. over-all lengths, they offer a selection of break-away forces. Installation is simple: Peel away the protective paper backing and press the catch against the door frame. They are easy to use where thick frame members make conventional attachment difficult. The housing and pin of the magnetic catch are aluminum; the pole pieces are zinc-plated steel; the magnet is barrium ferrite.

---

Terminal-strip cover protects against shorts

Kulka Electronic Corp., 520 S. Fulton Ave., Mount Vernon, NY 10551. (914) 664-1024.

Terminal strip safety covers, called Safe-Ti-Caps, protect the wiring connections and terminations. These covers are intended for high-risk areas where spills, dirt and accidently dropped tools could cause a short circuit. Made of nonflammable pliable rubber, the covers are easy to position and remove. When in place, they grip the terminal board barriers securely and will not easily come loose or slide. The covers can be marked with terminal identification.

---

50-contact connectors mass terminated in field

Viking Industries Inc., 9324 Topanga Canyon Blvd., Chatsworth, CA 91311. (213) 882-6275. $2.52 (50-249); stock.

A low-cost connector, called Vitel-F, can be mass-terminated in the field. The connectors can have up to 50 conductors. The connector can also be reterminated in the field to change the conductor pattern. A terminating tool displaces the wire insulation as it presses the conductors into place with a carrier strip. Four stable contact-to-conductor junctions are produced having an apparent junction area of up to 1000 circular mils per coupling. To reterminate, you merely remove the carrier strip back, then reposition the conductors and press the carrier strip into place.

---

Ferrite antenna cores come in almost any size


Uniform ferrite rods for low and very low-frequency antennas come in lengths exceeding 40 in. and diameters greater than 3-1/2 in. The high permeability and low-loss characteristics of these rods result in low coil mass and compact antennas of high efficiency. Engineering and technical assistance in the design of antenna rods is available from Ceramic Magnetics.
The many advantages and unique capabilities of Arrow-M's R Relays are far too extensive to be covered here. Therefore, we'd like to whet your creative appetite with a few outstanding facts:

1. Arrow-M R Relays are available in 1 Form C contacts which can carry a high current capacity of 1 Ampere 20 watts, and are capable of resisting welding at higher inrush currents. The dry circuit type which can switch current as low-level as 100uA is available in addition to the power type.

2. **High Speed**: Arrow-M R Relays can be operated at 500 cycles/sec.

3. Greater reliability and lower cost, due to simultaneous automatic fabrication of coil bobbin, contact and terminal.

4. In addition to the standard there are 1 coil and 2 coil latching types, which are useful for logic circuit design as a memory component.

5. Not only can they be automatically wave soldered on PC boards with a high density of electronic parts, but they are simple to clean with most degreasers and detergents without affecting maximum contact reliability.

6. **High Sensitivity**: Minimum operating power: Single Side Stable 80 mw/Bistable 40 mw

7. **Longer Life**: Mechanical: More than $10^8$ operations. Electrical: More than $10^9$ operations. (1A 20vdc, 0.3A 110vac)

---

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**Western Office**: 22010 So. Wilmington Ave.
Suites 300 & 301
Carson, Calif. 90745
(213) 775-3512
PACKAGING & MATERIALS

'Lazy susan' trays aid in circuit assembly

Wescorp, 1601 Stierlin Rd., Mountain View, CA 94040. (415) 969-7717. See text.

Models 8000 and 8000-A plastic-tray sets eliminate static-electricity problems associated with the production of hybrid ICS and other circuits. Each set consists of three round polyolefin trays that are chip-proof and resist alkalis, acids, paints and stains. The 24 compartments have rounded corners and edges for easy pick-up of small parts. Model 8000 costs $59.95 and has trays in diameters of 24, 20, and 16 in. Model 8000-A costs $44.95 and has trays in diameters of 20, 16, and 12 in.

CIRCLE NO. 377

Grounding kit outfits total work station

The Simco Co., 920 Walnut St., Lansdale, PA 19446. (215) 368-2220. $75 (unit qty).

A grounding kit for component assembly, manufacturing and test areas consists of 13 items. In the Neutro-Stat work-station grounding kit, four of the items are for personnel grounding—wrist strap, sleeve protectors, heel grounder and an anti-static fabric lab coat. The other kit pieces include a floor and work-surface mat, seat cover, high density foam, storage tray, tote box, shorting strip and electrically conductive bags. To ensure a static-free work station, the manufacturer recommends ionizing air devices, and offers as optional equipment a portable unit, for ionizing the work area; a system for laminar flow areas, clean benches and rooms; and a filtered, ionizing air gun, for simultaneously neutralizing and cleaning components.

CIRCLE NO. 378

Burn-in test sockets can be packed densely

Robinson Nugent Inc., 800 E. Eighth St., New Albany, IN 47150. J. Gribbins (812) 945-0211. $9.41 (1000 qty).

Burn-in and test sockets, series TSN, for DIP ICS are low insertion-force units—just 0.495-in. wide—and allow burn-in board densities to be increased more than 50% over old designs. Other features include socket terminals spaced exactly as the IC; a 0.125-in. slot in center of socket that permits easy use of sword-type extraction tools; and a 0.107-in. clearance slot on bottom of socket that allows mounting space for resistors or decoupling capacitors. The sockets are offered in both standard and hi-temp versions with 14 through 40 contacts; body material is polyphenylene sulfide (Ryton).

CIRCLE NO. 379

Lab PC etcher does professional job

Hutchinson Industrial Corp., 40 W. Highland Park, Hutchinson, MN 55350. T. Probst (612) 879-2371. $2700 list price.

A self-contained etcher produces in-convenient 117-V-ac outlet. The etcher is form and plug compatible with Altair 8800, Imsai 8080, and other similar microcomputer systems. Designated the 3690-12, the extender facilitates out-of-chassis troubleshooting and hardware debugging. The 7.5 x 9.99-in. extenders are 0.0625-in. thick epoxy-glass composite material. The 2-oz copper conductors are solder tinned while the card edge connectors are gold-flashed nickel plate for low contact resistance and reduced wear. The mating receptacle has 100 contacts (50 each side) on 0.125-in. centers.

CIRCLE NO. 380

Desoldering braid has tell-tale color

Wik-it Electronics, 140 Commercial St., Sunnyvale, CA 94086. (408) 732-8560. see text.

Desoldering braid, Chroma Wik-it, is now available in a distinctive color. The braid is pretinned for working speed and long shelf life and guaranteed for one year. The built-in color indicates exactly where to snip off used braid with no waste. A typical desoldering of a connection uses one-half cent's worth of the product. A Chroma Wik-it's flux coating is smooth, continuous and nonpowdering. The product works with any regular 30-to-75-W iron and removes solder from the connection in a 1-s operation. It is available in 5-ft rolls of 1/16-in. braid at $1.49 (Cat. #1007A), or 1/8-in. braid at $1.69 (Cat. #1006A). Bulk packs and other lengths and widths may be ordered.

CIRCLE NO. 381

Extender card mates with S-100 bus systems

Vector Electronics, 12460 Gladstone Ave., Sylmar, CA 91342. Floyd Hill (213) 365-9661. $25 (unit qty.); stock.

A circuit card extender, the 3690-12, is form and plug compatible with Altair 8800, Imsai 8080, and other similar microcomputer systems. Designated the 3690-12, the extender facilitates out-of-chassis troubleshooting and hardware debugging. The 7.5 x 9.99-in. extenders are 0.0625-in. thick epoxy-glass composite material. The 2-oz copper conductors are solder tinned while the card edge connectors are gold-flashed nickel plate for low contact resistance and reduced wear. The mating receptacle has 100 contacts (50 each side) on 0.125-in. centers.

CIRCLE NO. 382
Choice!

New Dale MSP Networks let you match profile, power and package to meet your resistance needs.

Dale's new MSP single-in-line networks are the shape of things to come in resistance. Rugged, machine insertable, and available in your choice of profiles: .350" with up to .3 watts per resistor or .195" (.19 watts) to meet critical board spacing requirements. Both are molded for extra protection. Both give you the kind of quality assurance we developed for Dale's SDM—the first network to meet MIL-R-83401. Sample the MSP now. It's available fast in quantity from stock...and it's only part of Dale's complete line of SIP and DIP networks.

Contact your Dale Representative or phone 402-371-0080

DALE ELECTRONICS, INC.
Box 74, Norfolk, Nebraska 68701
In Canada: Dale Electronics Canada Ltd.
In Europe: Dale Electronics GmbH,
8 Munchen 60, Falkweg 51, West Germany
A subsidiary of The Lionel Corporation.

AVAILABLE FAST: .350" model (MSPXXXC) available in 1 week from factory or from distributor stock. 6, 8 or 10 pin models(-01 circuit) in 49 standard values. Consult factory for fast delivery times on other configurations and schematics.

APPLICATIONS: Standard circuit (-01) has 5, 7 or 9 resistors with 1 pin common. Typical applications include 'wired OR' pull-up, power gate pull-up, MOS/ROM pull-up/pull-down, open collector pull-up, TTL input pull-down, TTL unused gate pull-up.

SPECIFICATIONS: Power: .350" model=3 watts max. per resistor; .195" model=19 watts max. per resistor.
Resistance: 33Ω to 1 Meg. standard.
Tolerance: ±2% standard. T.C. ±100 PPM/°C. T.C. Tracking: 50 PPM/°C. Operating
Temperature: -55 °C to +125 °C.
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P.O. Box 3428, Erie, PA, 16508
Tel. (814) 838-3571 TWX 510-696-6886

PACKAGING & MATERIALS

Marker pens apply bright fluorescent ink

Metron Optics, Box 690, Solana Beach, CA 92075. (714) 755-4477. $2.95 (unit qty); stock.

Marker pens with a choice of removable or permanent inks for board inspection are also available with special-purpose inks, electrical-contact lubricant, solder fluxes and liquid two-way tape. The pens contain an ink supply of more than 12,000 dots per pen. An optional microtip-needle applicator (orifice 0.013 in.) provides over 25,000 dots per pen. The brilliant fluorescent color of the ink makes the smallest dot highly visible and allows marking with very fine lines. Removable inks can be flicked off with the fingernail or wiped off with any solvent.

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CIRCLE NUMBER 76

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CIRCLE NO. 383

PC board carriers prevent contamination

Multi Tool & Manufacturing Inc., P.O. Box 553, Cape Canaveral, FL 32920.
John Wright (305) 733-2310. From $40 (unit qty); 3 wks.

When PC boards are stored in cardboard boxes during the assembly process, they can become contaminated. Chemicals and moisture in the cardboard can tarnish gold fingers and affect the solderability of the board. Special carriers that eliminate these problems, and improve PC-board handling, feature uprights that adjust to handle boards from 1-1/2 to 25 in. in width. And they have nylon guides that can be moved in 3/4-in. increments to match board height. The carrier handles PC boards in a horizontal position throughout assembly. If boards are handled vertically prior to soldering, loose components and wires can fall off.

CIRCLE NO. 384

MARKER PEN APPLIES BRIGHT FLUORESCENT INK
Select four outputs with one active filter

Datel Systems, 1020 Turnpike St., Canton, MA 02021. Eugene Murphy (617) 828-8000. $16 (1-9 qty); stock.

Low-pass, bandpass and high-pass transfer functions are simultaneously produced at the output of the FLT-U2 hybrid filter. A fourth uncommitted op amp is available as a summing or buffer amplifier. The 16-pin ceramic DIP operates with ±5 to ±18 V dc power supplies over a 0 to 70°C temperature range. An output voltage range of ±10 V dc for ±12-V dc input makes the unit compatible with other op amps. Gain-bandwidth product is 3 MHz and center frequency accuracy is ±5% from 0.001 Hz to 200 kHz.

CIRCLE NO. 385

Data-acquisition unit plugs directly to 6800

Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734. C. Teeple (602) 294-1131. $140 (100 qty); stock.

The MP21, a complete 16-channel data-acquisition system, interfaces directly to 6800, 650X and 8-bit µPs. Timing and logic-level compatibility eliminate any need for external logic. The hybrid, quad-in-line package houses a 16-channel analog multiplexer, a high-gain instrumentation amp, an 8-bit a/d converter plus all necessary address, data and control interfaces. Without external gain or offset adjustments absolute accuracy is better than ±0.4% (1 LSB) on high-level ranges. Low-level signals such as thermocouple outputs can also be handled directly, but with reduced accuracy. The instrumentation amplifier can be programmed with a single external resistor to provide input-signal ranges as low as ±10-mV FS. The µP accesses the data-acquisition unit as memory. Each analog-input channel occupies one memory location. Any memory-reference instruction can be used to access data. The unit can be used with or without halting the CPU or on an interrupt basis. 1.7 x 2.1 x 0.22 in. 0 to 70°C operation. ±15 and +5-V-dc power.

CIRCLE NO. 386

Video d/a converter outputs current


Designed for summing-point applications (current rather than voltage output), the DAC-V d/a converter comes in an 8 or 10-bit version. The 10-bit-resolution unit boasts output accuracy, including linearity, of ±0.05% FSR and typ settling time to ±1LSB of 20 ns for a full-scale input change. The 8-bit version offers ±0.2% FSR accuracy and 15-nS typ settling time. Accuracy tempco is ±15 ppm/°C for the 10-bit unit and ±30 ppm/°C for the 8-bit unit from −20 to +75°C. The TTL/DTL compatible inputs accept either binary coding for unipolar operation with a 0 to +15-mA output, or offset-binary coding for bipolar ±7.5-mA output. A temperature-compensated reference is included in the module. 2.3 x 2.3 x 0.4 in.

CIRCLE NO. 387

8-bit video converters come on a board

Tektronix, P.O. Box 500, Beaverton, OR 97077. C. Payne (503) 644-0161. See text.

Two video converters, the ADC 820, an 8-bit 20-MHz a/d and the DAC 850, an 8-bit 50-MHz d/a, each come on a board measuring 6 x 8 x 1 in. The a/d unit dissipates 7 W. It has an on-board anti-aliasing filter at the quantizer input. Differential phase and gain are ½ and 1% rms, respectively. The unit does not use a s/h. The d/a converter dissipates 5 W. It comes with 3- or 4-x-subcarrier output filters or with no filter. Differential phase and gain are ¼ and ½% rms respectively. Both units are available for evaluation with TTL logic compatibility. Prices start at $1650 for the a/d and $525 for the d/a. Power required is ±12, +5 and −5.2 V. Production quantities are scheduled for fall; ECL versions are expected several months later.

CIRCLE NO. 388
**MODULES & SUBASSEMBLIES**

**Instrumentation amp isolates also**

Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734. N. Shah (602) 294-1431. From $109 (100 qty); 4 to 6 wks.

The 3456 Isolated Instrumentation Amp gives you a true three-wire-input instrumentation amplifier together with input-to-output isolation plus self-contained isolated power supply, in one module. This amp has a differential input plus a separate input common and provides continuous pk-isolation rating of 2000 V. Isolation impedance is 1012 n in parallel with 14 pF, and isolation-mode rejection is 120 dB at 60 Hz. Among other key specifications are: max gain nonlinearity of ±0.02% at 100 gain and max input-offset-voltage drift of 1 µV/°C at 1000 gain for the B version and 2.2 µV/°C for the A. CMR is 110-dB min, at 100 gain and one resistor programs the gain from 1 to 1000. Operates from -25 to +85 C; 2.3 x 3.5 x 7 in.

**CIRCLE NO. 389**

**Multipleplexer plugs four peripherals into mini**

**12-bit DAC ignores wide temp swings**

Datel Systems, 1020 Turnpike St., Canton, MA 02021. E. Murphy (617) 828-8000. $139 (1-9 qty); stock to 4 wks.

Thin-film-hybrid 12-bit d/a converters feature a 10 ppm/°C gain tempco. This means the full scale output stays within ±1 LSB in the face of a ±24°C ambient change. The 24-pin metal-packaged DAC-HZ12BM-1 (binary-coded) and DAC-HZ12DMR-1 (3-digit, BCD-coded) also feature a settling time of 3 µs for a 10-V output change. The output voltage has five pin-programmable ranges. Output-drive capability is ±5 mA min, and the power-supply requirement is ±15 V dc at 35 mA. The differential-nonlinearity tempco of 2 ppm/°C for both devices assures monotonic output over the -25 to +85-C operating range.

**CIRCLE NO. 391**

**Rf amps offer very wide bandwidth**

Motorola Semiconductor Products, P.O. Box 20912, Phoenix, AZ 85036. Alan Wagstaff (602) 244-6394. $51.75 (1-24 qty); stock.

Four wideband rf amplifier modules covering the frequency ranges of 1 to 250 MHz and 10 to 400 MHz can be used in communication systems. The MHW 590-93 units operate from either 13.6 or 24-V-dc supplies over a temperature range from -20 to +90 C. A hybrid construction technique using thin film gold metalization on an alumina substrate results in a linear response of ±1 dB over the designated bandwidth. Power gain is typically 34 dB and all modules have a noise figure of 5 dB at 250 MHz.

**CIRCLE NO. 393**

**Board converts DPM into ohmmeter**

International Microtronics Corp., 4016 E. Tennessee St., Tucson, AZ 85714. (602) 748-7900. $80 (1-24 qty); 2 wks.

With the 303 A 0-converter option, Series 300 DPMs digitally display the value of an unknown resistor. Ranges are 0.199, 1.999, 19.99, and 199.9 kΩ and accuracy is ±0.1%, when the PC-board option works into the company's series 300 DPMs.

**CIRCLE NO. 390**

**12-bit d/a converters span MIL temperature**

Hybrid Systems, Crosby Dr., Bedford, MA 01730. L. Lauenger (617) 275-1570. From $120; 4 wks.

DAC335 d/a converters are pin-for-pin compatible with the DAC 85-12V converter series from Burr-Brown. With the 12-bit DAC335s you get a typ power drain of 300 mW, operation from -55 to +125 C and a choice of either commercial or 883A Class-B processing. Logic input codes are complementary binary (unipolar) and complementary offset binary (bipolar) at TTL, DTL and CMOS-compatible levels. Three-decade complementary-BCD models are also available. Key specifications are: ±1/2-LSB linearity error, 3-µs settling time, 2-ppm/°C linearity tempco. 24-pin DIP, 4-5 and ±15-V power.

**CIRCLE NO. 394**
Need ROM retention and RAM alterability?

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Our Metal Nitride Oxide Silicon NVM are fully reprogrammable in-circuit. They offer long-duration storage security without battery backup or "power-on" auxiliaries.

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Nitron NVMs are available off-the-shelf for parallel data applications in 64x4 and 256x4 configurations; and for serial data applications in 21x16, 16x18 and 1024x1 configurations. If you don’t see what you need, tell us about it. We custom design NVMs, too.

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ELECTRONIC DESIGN 17, August 16, 1977
Ultra compact "V-PAC" DC-DC power sources use 5v or 12v input, provide ±15v regulated low noise output, which can be balanced.

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- Price: $20.20 (100 pcs)

**INSTRUMENTATION**

120-MHz sig gen offers versatile modulation

Marconi Instruments, 100 Stonehurst Ct., Northvale, NJ 07647. (201) 767-7250. $2650; 90 days.

Model 2016 AM/FM signal generator covers the spectrum from 10 kHz to 120 MHz. The unit uses fundamental frequency generation to cover the range in 12 switched bands. Modulation facilities include two internal oscillators at 400 Hz and 1 kHz, which may be used independently for FM to 75-kHz deviation or AM depth to 100%, or combined with external signals for simultaneous AM and FM.

**Mini DMM stresses long battery life**

**Control & Information Systems**, 10 Spring Valley Village, Richardson, TX 75080. (800) 527-4831. Texas residents (214) 234-4173. $99.95; stock.

The Autoranger digital multimeter gives readings on a 3-½-digit liquid-crystal display. That, plus CMOS logic design, assures low power drain from the unit's single 9-V battery. Featured are autoranging, autozeroing, and automatic lead reversal. Capabilities include ac/dc voltage to 1000 V and resistance to 1000 kΩ.

**Watch those sags with disturbance recorder**


Model 5229 portable, power-line transient-amplitude and duration-disturbance recorder (digital sag/surge recorder) prints out all power-line disturbances, sags and surges, over the entire range of dc to 1 MHz, 0 to 1000 V. Sags (increases in line waveform) and surges (decreases in line waveform) over this range are identified and recorded, along with the time of day. The transient-duration measurement is of true time duration, correlated to the sag or surge producing it, and resolves down to 1 μs.
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**CIRCLE NUMBER 80**
**Instrumentation**

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Two dual Hi/Lo variable filters, Models 452-01 and 852-01, offer a cutoff frequency range from 0.01 Hz to 111 kHz, and resolution down to 0.01 Hz, with Butterworth and linear phase responses, and a cutoff frequency accuracy of ±2% throughout the entire frequency range. Each model consists of two identical filter channels contained in a common cabinet, with separate input/output terminals. Rolloff of the 452-01 is 24 dB/octave/channel, and of the 852, 48 dB/octave/channel.

CIRCLE NO. 403

**Scope or DVM 'probe' reads magnetic fields**

Perfection Mica Co., 740 N. Thomas Dr., Bensenville, IL 60106. (312) 766-7800. $79.50.

The ac magnetic-field evaluator probe operates with a VTVM or oscilloscope. The shielded banana plugs on %-in. centers fit most input jacks. Sensitivity is 60 millivolts per gauss. Either axial (shown) or transverse pick-up coil positions are available. The probes are useful for accurate measurement of the disturbing field intensity in gauss.

CIRCLE NO. 404

**DPM sports low price tag**

Datel, 1020 Turnpike St., Canton, MA 02021. (617) 828-8000. $29 (100s).

Model DM-3100L display-only DPM sells for $29 in hundreds. The unit features differential inputs and auto-zeroing and is housed in a miniature Lexan case measuring 3.0 × 1.8 × 2.2 in. All models feature common-mode voltage ranges of ±2 V at 80 dB CMR. Temperature drift is 50 ppm rdg/°C typical, with displayed accuracy of 0.2% of reading, ±1 count at 25 C.

CIRCLE NO. 405

**Logic analyzer debugs hardware or software**

BP Instruments, 10601 South De Anza Blvd., Cupertino, CA 95014. (408) 446-4322. $4558.

Model 50DI6 16-channel, 50-MHz logic analyzer is designed for the microprocessor system designer who needs to debug not only hardware, but software as well. The 50DI6 features a Data-Trigger mode that allows the user to insert up to three sample bits of delay in the trigger. According to the company, this mode eliminates unwanted triggering on static, noise—or even anomalies appearing on a three-state bus at the time of device transfer.

CIRCLE NO. 406

**Unit traps data flow for later analysis**

International Data Sciences, 100 Nashua St., Providence, RI 02904. (401) 274-5100. $9975; 60 days.

The Hawk 4000 traps 2000 data characters for later recall and study. The Hawk unit is interactive. It can monitor, transmit, and receive data between a modem and a terminal on a 9-in., 512-character screen. The operator issues commands via a simple keyboard. All switches are "stored" in memory which means the Hawk will never become extinct.

CIRCLE NO. 407
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To The Point

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POWER SOURCES

Rechargeable battery comes in popular case

General Electric, P.O. Box 992 C, Gainesville, FL 32602, T. Trueper (904) 462-7100. $3.53 (OEM qty).

Models SD-1 C/10 and /3 are, respectively, standard and quick-charge nickel-cd batteries in the first 9-V-sized package that meets ANSI dimensional specs with maxs of 1.938 X 1.031 X 0.656 in. These power sources are 9-V type only mechanically—their nominal potential is 7.5 V. Among the principal specs at 25 C, min rated capacity is 65 mAh at 65 mA and 70 mAh at 15 mA, max continuous discharge is 150 mA and max momentary discharge is 600 mA. The batteries stand up to 1000 recharges and sustain long continuous overcharging. For standard units recharging takes 16 h while it drops to 5 h for the specially selected /3 quick chargers. Quick-charge units carry a 5% price premium. Safe temps: charging, 5 to 50 C; discharging, -20 to +50 C; storage, -40 to +50 C.

Open-frame family offers 55 supplies

Acme Electric, Cuba, NY 14727. (716) 968-2400.
You can choose from among seven package sizes and 55 models in the Power House ALM series of open-frame supplies. All units feature 0.1% regulation (line and load), 1.5-mV rms or 5-mV pk-pk ripple and noise, from 47 to 63 Hz. An adjustable current-limit range of 50 to 125%, adjustable output-voltage resolution of 1.1%, inherent short-circuit and overload protection, remote-sense terminals (with 0.25 V provided to compensate for line-load loss) and an operating range of 0 to 60 C are all standard. Both single and ± 2% -tracking dual-output models are available. Single outputs range from 2 V at 1.5 to 20 A through 24 V at 0.5 to 10.5 A. Dual outputs range from 11.8 to 15.2 V at 0.55 to 8.0 A. Overvoltage protection modules are optional. Inputs: 100 to 125 or 200 to 250 V at 47 to 440 Hz.

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ELECTRONIC DESIGN 17, August 16, 1977
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Power supplies
A 40-page application and selection guide provides a glossary of power-supply terminology, presents test procedures and recommended practices for the user of both line-operated and dc/dc-converter power supplies and defines the special requirements for safely powering µPs. Semiconductor Circuits, Haverhill, MA

Noise suppression
Technical data and typical applications are included in this basic text on the protection of electronic equipment from line noise and transients. Topaz, San Diego, CA

Test instruments
A 48-page catalog describes applications and specifications of scopes, multimeters, counters, and other equipment. Leader Instruments, Plainview, NY

Temperature instruments
"Energy Conservation by the Use of Portable Temperature Instruments," a 32-page handbook, shows how to choose the correct thermometer, 50 examples of energy-related temperature measurements and a table that summarizes the features of the instruments along with their advantages and limitations. William Wahl Corp., Los Angeles, CA

Executive software
Real-time executive software used with HP 21MX computers and 1000 computer systems is described in a 60-page catalog. Separate sections discuss the system diagnostics library, product support and product training. Hewlett-Packard, Palo Alto, CA

BITE indicators
A four-page brochure covers BITE (Built-In-Test-Equipment) indicators used for fault isolation. Schematics included. North American Philips Controls Corp., Cheshire, CT

Alarm products
Over 900 professional-grade alarm products are described in a 72-page catalog. Mountain West Alarm System, Phoenix, AZ

Data communications
Descriptions and illustrations of modems, network-diagnostic and control systems, and terminals are given in a 16-page catalog. International Communications Corp., Miami, FL

Encoder
The "Logic Engine," an encoder for solid-state-switch arrays, is featured in a six-page catalog. Keytron, Spokane, WA

L-C filters
Custom-built precision L-C filters in frequencies from 20 Hz to 400 MHz are presented in a 20-page catalog. Allen Avionics, Mineola, NY

Capacitors and resistors
Glass, glass-ceramic, ceramic and subminiature solid-tantalum capacitors and metal-film resistors are described in this 72-page catalog. Convenient features include product index tabs and specs in both English and metric units. Corning Glass Works, Corning, NY
Cabinets
Technical details for cabinet housings, front and rear panels, covers, keyboard housings, chassis, internal-slide units, bases, spacers and CRT housings are shown in a 12-page brochure. Backer-Loring, Peabody, MA  CIRCLE NO. 421

Analogue input controller
Technical information, typical applications and ordering information for the RTP7471 low-level analog-input controller are provided in an eight-page bulletin. Computer Products, Fort Lauderdale, FL  CIRCLE NO. 422

Power supplies
A 66-page design-data catalog features power supplies by application requirements: extreme environment MIL-qualified; military; industrial; commercial and OEM. Technipower, Ridgefield, CT  CIRCLE NO. 423

Real-time systems
"Real-Time Systems" describes the hardware and software components of DEC's real-time computing systems based around the PDP-11 family of computers. Digital Equipment, Northboro, MA  CIRCLE NO. 424

X-Y recorders
General specifications, ordering information, OEM and control modules, supplies and accessories for the 2000 X-Y recorder are covered in an eight-page catalog. Houston Instrument, Austin, TX  CIRCLE NO. 425

Phototransistors
Phototransistors and photo-Darlingtons are featured in a four-page brochure. The brochure includes electro-optical parameters, graphs of characteristics and environmental information. Vactec, Maryland Heights, MO  CIRCLE NO. 426

Counters, timers
A 23-page "kit" of application/design bulletins covers mechanical counters and timers. The bulletins illustrate the easy, inexpensive modifications and changes that are possible by building upon the basic unit. Guardian Electric Manufacturing, Chicago, IL  CIRCLE NO. 427

Fiber optics
"An Introduction of Communication Fiber-optics Design," 20 pages, provides a brief historical perspective; reasons for designing with fiber optics; initial costs, hardware savings, installation, reliability/survivability; and applications. Valtec, West Boylston, MA  CIRCLE NO. 428

Power semiconductors
The selection of power transistors, triacs, and SCRs for a wide variety of power circuits is covered in a 48-page brochure. Detailed applications and data sections are provided. RCA, Somerville, NJ  CIRCLE NO. 429
Application notes

Interface bus

A concise, easy-to-read explanation of instrument/computer interfacing, and the development and use of the HP Interface Bus are shown in a 12-page brochure. Hewlett-Packard, Palo Alto, CA

CIRCLE NO. 430

Digital plug-ins

Applications of the digital plug-ins available for 7000-series oscilloscopes are described in "Digital Accuracy—Analog Interpretation." Tektronix, Beaverton, OR

CIRCLE NO. 431

Multiplexer parameters

"Specifying and Testing Multiplexers" details multiplexer parameters and their measurement. Teledyne Philbrick, Dedham, MA

CIRCLE NO. 432

Resistor networks

"Designers Guide to Thin-Film Resistor Networks" contains information on typical applications, key parameters and the construction and processing of both custom and standard thin-film resistor networks. Micro Networks, Worcester, MA

CIRCLE NO. 433

CRT graphics controllers

How to use the company's line of high-resolution-TV CRT-graphics controllers is explained in a 24-page brochure. Detailed pinout descriptions as well as interface diagrams for μPs are provided. Matrox Electronic Systems, Montreal, Quebec.

CIRCLE NO. 434

Count/time data system

A 28-page bulletin explains a data-acquisition system that gathers data from machines, networks, or experimental setups on up to 248 channels, all easily programmed through an on-board keyboard. Esterline Angus Instrument Corp., Indianapolis, IN

CIRCLE NO. 435

Bulletin board

Faster NMOS CPUs are available as retrofits on SC/MP kits from National for only $18.50.

CIRCLE NO. 436

Texas Instruments is second-sourcing National Semiconductor's 3-terminal adjustable regulators, the LM117, LM217 and LM317.

CIRCLE NO. 437

Wintek has added a two-day "Hands on Interfacing Workshop" to its standard three-day "Hands on Microprocessor Short Course with Free Take-home Microcomputer." Tuition is $299. The Fall '77 workshops will be in Dallas; Houston; Washington, DC; Melbourne, FL; Denver; Palo Alto; San Diego; Indianapolis; Boston; Detroit; Chicago and a yet unspecified city in Puerto Rico.

CIRCLE NO. 438

Motorola is expanding its line of wideband video amplifiers by second-sourcing NE592/SE592 device types.

CIRCLE NO. 439

Analog Devices has cut prices of 4 and 3/4-digit DPMs 10 to 20% across the board.

CIRCLE NO. 440

Raytheon Co. Semiconductor Div.'s 2901A 4-bit μP slice is 20 to 30% faster than the standard unit over both the commercial and military temperature ranges. It is designed to be pin-for-pin and functionally compatible with the standard 2901.

CIRCLE NO. 441

Fairchild's 9408 microprogram sequencer now comes in a military temperature-range version.

CIRCLE NO. 442

Zilog has started production of a Z80A μP with a standard clock rate of 4.0 MHz.

CIRCLE NO. 443

Interdata has lowered prices up to 35% for its computer memory systems and 32-bit processor, the Model 7/32CII.

CIRCLE NO. 444
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Want to contact us? If you have any comments or wish to submit a manuscript or article outline, address your correspondence to:
Editor
Electronic Design
50 Essex St.
Rochelle Park, NJ 07662

Electronic Design

Advertising Sales Staff
Tom W. Carr, Sales Director
Sue Apolant, Sales Coordinator
Rochelle Park, NJ 07662
Robert W. Gascoigne
Thomas P. Barth
Stan Tessler
50 Essex St.
(201) 843-0550
TWX: 710-990-5071
(HAYDENPUB ROPK)
Philadelphia
Thomas P. Barth
(201) 843-0550
Boston 02176
Gene Pritchard
P.O. Box 379
Belmont, MA 02178
(617) 489-2340

Chicago 60611
Thomas P. Kavooras
Berry Conner, Jr.
200 East Ontario
(312) 337-0588

Cleveland
Thomas P. Kavooras
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Los Angeles 90045
Stanley I. Ehrenclou
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Texas
Burt Underwood
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San Francisco
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465 S. Mathilda, Suite 302
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116 ELECTRONIC DESIGN 17, August 16, 1977
Using solid-state technology to replace bulky tube-type equipment, ENI's broadband amplifiers are tomorrow ideas available today. ENI's Class A power amplifiers already cover the frequency spectrum of 10 kHz to 1 GHz, with power outputs ranging from 300 milliwatts to over 4000 watts. And we're still climbing. Driven by any signal generator, frequency synthesizer or sweep, ENI's compact portable amplifiers are completely broadband and untuned. Amplifying inputs of AM, FM, SSB, TV and pulse modulations with minimum distortion, these rugged units are versatile power sources for general laboratory work, RFI/EMI testing, signal distribution, RF transmission, laser modulation, data transmission, NMR, ultrasonics and more.

Designed to be unconditionally stable and failsafe (impervious to severe load conditions including open or short circuit loads), ENI power amplifiers will deliver their rated power to any load, regardless of match.


ENI
World's Leader in Solid State Power Amplifiers

CIRCLE NUMBER 231
Cash in on the CMOS advantage ...

New I/O devices make RCA 1800 µP even more flexible.

Here is further proof of how flexible and cost-effective the CMOS RCA 1800 is compared to other microprocessor systems. Easily, and with minimum parts count, you get maximum flexibility—through these versatile, low-cost I/O devices. And CMOS itself helps reduce costs. Thanks to a single, non-critical voltage supply. Low power. High speed and noise immunity. And full military temperature range.

1. Two-mode UART
Unique among industry standard UARTs, the CDP1854 operates in two modes and is pin-out selectable by a single mode control. In Mode 0 it works as an industry standard 1602 UART. Mode 1 makes it compatible with the RCA 1802 and other 8-bit CPUs. And either mode gives high speed—up to 400K baud.

2. Address latch/decoders
These two devices, the CDP1858 and CDP1859, make it easy to expand the RCA 1800 memory. They interface directly with the CDP1802 memory address bus and serve as memory system decoders for large RAM systems. The CDP1858 is designed for use with CDP1821 type memories and the CDP1859 for use with CDP1822 type memories.

3. N-bit decoder
If you need a high-speed, low-power 3-to-8-line decoder circuit with the added feature of optional strobed outputs for spike free decoding, we’ve got that too. The CDP1853 has buffered inputs and outputs. It is fully compatible with the CDP1802 and is used in I/O decoding applications.

4. Bus buffer separators
For easy connection of standard memory and I/O devices to the CDP1802 microprocessor data bus, use the CDP1856 and CDP1857 non-inverting bus buffer separators. The CDP1856 is designed for data bus to memory interfacing and the CDP1857 for data bus to I/O interfacing.

For more information, contact your RCA Solid State distributor, or RCA.

Write: RCA Solid State.
Box 3200, Somerville, NJ 08876;
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Easy I/O.
Part of the CMOS advantage.