Low-cost, 50,000-gate ASIC modeler  pg 13

System simulation embraces real-time control prototyping  pg 49
12-bit ADCs: Now may be the time to upgrade your 8- and 10-bit systems  pg 67

Designing 2.1V Futurebus+ termination system requires system-engineering approach  pg 117
Energy gauges add intelligence to rechargeable batteries  pg 125

Special Report: ESDA tools ease the flow of top-down designs  pg 80
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<th>Absorptive SPDT</th>
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<td>dc- 500- 2000- 5000</td>
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<td>YSW-2-50DR (pin) $14.95</td>
<td>ZYSW-2-50DR (SMA) $49.95</td>
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As system complexity grows, ESDA tool vendors try to convince you they can solve your design problems with a new class of tools. Maybe they can.—Doug Conner, Technical Editor

Designing 2.1V Futurebus+ termination system requires system-engineering approach

Designing a termination system for a Futurebus+ power system can be a formidable task. Tight voltage tolerance and ripple-noise specifications require an approach that considers the power supply, backplane, termination, and backplane-transistor-logic drivers as interconnected units.—Samuel H Duncan and Robert V White, Digital Equipment Corp

Energy gauges add intelligence to rechargeable batteries

An energy gauge built into a rechargeable battery pack can tell you exactly how much charge remains available for use. It can also direct an inexpensive “dumb” charging device to charge the pack in an optimal manner. It can even store a history of battery health.—Malcolm McClure, Span Inc

Low-distortion oscillator starts fast

Paralleling rms converters speeds settling

Circuit protects computer’s input

RS-485 repeater extends standard’s reach

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Simple module gives voice to PC

Security circuit eschews sophistication

Continued on page 7
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<table>
<thead>
<tr>
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Microchip PIC16/17 Microcontrollers

<table>
<thead>
<tr>
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<th>Pins</th>
<th>I/O</th>
<th>Memory</th>
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<td>2048 x 16 (OTP)</td>
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*These products will be the focus of this seminar series.
System simulation embraces real-time control prototyping

Today's control-system simulators employ graphical modeling tools, automatic coding, and DSP “hardware-in-the-loop” simulation to narrow the gap between conceptual design and product reality.

—Brian Kerridge, Senior Technical Editor

12-bit ADCs: Now may be the time to upgrade your 8- and 10-bit systems

A substantial list of low-cost 12-bit devices with competitive power and speed makes upgrading 8- or 10-bit systems seem almost foolproof. However, ensuring 12-bit accuracy means reevaluating many other aspects of a design.—Anne Watson Swager, Technical Editor

Technological proof of innocence: Part 1

When will we start using technology to protect us from the worst technological abuses?—Steven H Leibson, Editor-in-Chief

Embedded Systems .......................................................... 132
Electronic Design Automation ....................................... 134
Integrated Circuits .......................................................... 139
Boards and Buses .............................................................. 145

News Breaks ........................................................................ 13
Signals & Noise ................................................................ 37
Hands On! ......................................................................... 130
Literature .......................................................................... 146
Career Opportunities .......................................................... 152
EDN's International Advertisers Index ............................. 155
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Your Hyundai DRAM Source Guide

<table>
<thead>
<tr>
<th>Size</th>
<th>Part Number</th>
<th>Speed</th>
<th>Refresh</th>
<th>Production</th>
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<tbody>
<tr>
<td>16M x 1</td>
<td>HY5116100</td>
<td>60/70/80</td>
<td>4096/64</td>
<td>ROW</td>
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<tr>
<td>HY5117100</td>
<td>2048/32</td>
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</tr>
</tbody>
</table>

All available in standard and low power versions. Packages include SOJ, TSOP II, reverse TSOP II.
New 16 Mbit DRAMs, designed with team dynamics in mind.

Evaluation samples of Hyundai DRAMs organized 16M x 1, 4M x 4 are available now. Coming soon are DRAMs organized 1M x 16 and 2M x 8. And many will operate off of a 3 volt source too.

Hyundai's new DRAMs feature speeds of 60, 70, or 80 ns. Immediately available, the HY5116100 and HY5117100 are organized 16M x 1 and provide 4096 refresh cycles per 64 ms and 2048 refresh cycles per 32 ms, respectively. New 4M x 4 parts include the HY5116400, with 4096 refresh cycles per 64 ms, the HY5116410 with write-per-bit capability, and the HY5117400 and write-per-bit capable HY5117410 offering 2048 refresh cycles per 32 ms.

All parts are available in standard and low power versions, dissipating 495 mW operating at 60 ns, 440 mW at 70 ns, and 385 mW at 80 ns. Other features include operation from a single 5V ±10% power supply, TTL compatible inputs and outputs, fast page mode operating, multi-bit test capability, read-modify-write capability, and CAS-before-RAS, RAS-only, as well as hidden refresh. Packages include standard 24/28 pin plastic, TSOP II, and reverse TSOP II. TSOP will be available soon.

These new parts are products of Hyundai's 0.55 micron CMOS process, at one of the most advanced electronics manufacturing plants in the world. So if purchase of 16 Mbit DRAMs is on your agenda, and you don't want to get caught short the way some did on 4 Mbit, start the team dynamics now.

Free 1994 16 Mbit DRAM Data Book. Yours for the asking. Please phone, fax, or write for your copy today. Phone (408) 473-9274. Fax (408) 473-9370. Address Hyundai Electronics America, 166 Baypointe Parkway, San Jose, CA 95154.
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Logic animator prototypes 50,000-gate ASICs

By throwing out assumptions built into its Enterprise family of ASIC emulation systems, Quickturn Design Systems has produced a less-expensive ASIC prototyping tool, the Logic Animation System Model S50, which models 50,000-gate ASICs at 8- to 16-MHz typ clock speeds. The company lowered the cost of this product by simplifying the hardware design, eliminating some features, and unbundling the software. Consequently, you can use the S50 to create several hardware prototypes that permit software development well before the actual ASICs emerge from fabrication.

In Quickturn's vision of rapid ASIC prototyping, you start with a netlist in one of several standard formats (currently EDIF, TDL, NDL, and Verilog) that your ASIC design tools create. You feed this netlist, properly massaged, into the S50, and it "becomes" your ASIC. If your ASIC design incorporates memory, standard-logic ICs, or logic cores for which "bond-out" parts exist, the S50 can directly make use of these ICs through an external interface module. This feature can extend the S50's modeling abilities beyond 50,000 gates. Like the company's larger emulation systems, the Logic Animation System connects to the target hardware through an emulation cable and plug. The S50 has 448 bidirectional I/O pins for logic animation.

Unlike the emulation systems, the S50 doesn't provide extensive internal debugging facilities. Instead, it makes use of an instrument found in every hardware lab: a logic analyzer. A separate cable links the S50 to a logic analyzer and connects as many as 448 signals inside the modeled ASIC to the logic analyzer. Currently, the S50 software supports Hewlett-Packard's 1650 and 16500 logic-analyzer families. Support for the Tektronix DAS logic analyzers will appear this year.

The S50's software runs on a workstation and shares many of the same features as the company's Enterprise emulation systems, such as single-pass compilations, correct-by-construction timing, interactive speed optimization, and incremental probe changes for debugging. The software produces 2- to 4-Mbyte files representing the ASIC model. You download these files to a PC, which then runs the S50. Thus, you may need only one $60,000 copy of the software to create several ASIC prototypes using $30,000 S50s and PCs.

Once you have verified your design, you can continue to use the S50 ASIC prototypes while waiting for the actual ASICs to arrive from the foundry. This ability may save you weeks of system-development time by allowing software development and ASIC fabrication to occur concurrently. Because the ASIC model files are relatively small, you can even consider downloading the files over the phone. Consequently, you can provide regular and speedy design updates to software developers miles or continents away from your ASIC-development site.

One more characteristic differentiates the S50 from its larger brethren: It's not expandable. To drive down system cost, the S50's designers created a single-board system with no expansion capabilities. However, more than half of the ASIC designs currently under way are below the S50's 50,000-gate limit.

—by Steven H Leibson
Circle No. 434

Second-generation LONWorks µP runs on half-power

Migrating to a 0.8-µm fab process has reduced the cost and dropped (by one-half) the active power dissipation of Toshiba's second-generation Neuron µP for Echelon's local-operating networks (LONs). The new µP draws 16 mA typ at 10 MHz while operating and only 15 µA (formerly, 500 µA) in sleep mode. A Neuron µP comprises three processors on one chip: two to run the networking protocol and one to run the application program for the application.

The second-generation Neuron is available in two forms: the TMP3150 and TMP3120. Both µPs contain 512 bytes of EEPROM and a unique 48-bit serial identification number. The TMP3150 also includes 2 kbytes of RAM and comes in a 64-lead QFP package. The TMP3120 includes 1 kbyte of RAM and 10 kbytes of ROM and is available in a 32-lead SOIC package. Both devices will sell for around $5 (10,000).—by Steven H Leibson
Circle No. 435

Intel adds clout to PC/104

Intel Corp has raised the visibility of the PC/104 Consortium's modular-computer standard by joining the group as an executive member. Although PC/104 has more than 100 member companies, the addition of Intel, which is virtually synonymous with the µPs that control PCs, gives the group a big boost in credibility and presence. Intel's motivation, no doubt, is to gain a forum for promot-
More linear-IC price cuts. Joining Comlinear Corp in reducing prices (EDN, December 9, 1993, pg 16) is Harris Semiconductor. Enhancements and yield improvements to the company's complementary-bipolar technology are allowing price cuts of up to 50% for wideband amplifiers and buffers. Prices for the latest generation of 350-MHz op amps are approaching the level of older, 100-MHz devices. The price cuts affect op amps and buffers with 3-dB bandwidths in the range of 350 to 850 MHz. One example is the HFA1105/06/35/45 family of 350-MHz, 6-mA quiescent current op amps whose new prices range from $3.25 to $4.12 (100). The new price for the HFA1100 850-MHz op amp is $4.95 (100), down from the previous price of $7.95. Harris Semiconductor, Melbourne, FL, (800) 442-7747.

Circle No. 436

High-power semiconductor laser suits high-density optical-disk drives. Mitsubishi has announced the ML1412R, a high-power semiconductor laser that emits 690-nm wavelength red light, approximately 100 nm shorter than conventional wavelength. A single power supply drives the laser, which will find applications as a light source for writing and reading in next-generation, high-density optical-disk drives. Sample quantities cost ¥30,000. Mitsubishi Electric Corp, Tokyo, Japan, (3218) 2456.

Circle No. 437

Booklet outlines EMI-shielding benefits of perforated metals. If you're a designer, specifier, or buyer concerned about EMI/RFI prevention, you might want to read this free handbook to familiarize yourself with the advantages of perforated metals. The 108-pg publication from the Industrial Perforators Association contains application photos, charts, and data detailing perforated metals' EMI-shielding effectiveness and other properties. Industrial Perforators Association, Milwaukee, WI, (414) 271-2265.

Circle No. 438

ing its embedded-PC architectures. The chip company predicts a huge market for embedded 386-type processors, and it expects the PC/104 format to play a key role in that market. Stackable PC/104 modules, measuring 3.6x3.8x0.6 in., allow construction of embedded PCs without card cages or backplanes.

—by Gary Legg

PC/104 Consortium, Mountain View, CA, (415) 903-8304.

Circle No. 439

25-Mbps ATM chip set available for LANs

Transswitch recently announced a technology-access agreement with IBM, which allows Transswitch to market a 25-Mbps asynchronous-transfer-mode (ATM) chip set to LAN-equipment vendors. The ALI-25 chip set permits communications over unshielded LAN cabling.

Transswitch offers an integrated family of standard chip sets that provide ATM access over high-speed channels, including synchronous optical network (SONET), DS-3, and E-3 channels. ALI-25 costs $35 (10,000).

—by John Gallant

Transswitch Corp, Shelton, CT, (203) 929-8810.

Circle No. 440

HyperSPARC modules top 100 MHz

Using multichip-module techniques, Ross Technology has packed a high-performance CPU with a 256-kbyte second-level cache into a 131-pin PGA (pin-grid-array) package, the RT629. The module fits sockets in workstations that accept HyperSPARC CPUs and runs a fully qualified port of Solaris 2.3. It draws 3.5W and runs 3.3V internally with a 5V external interface.

The modules are available in a variety of speeds. Modules offering 80-, 90-, and 100-MHz CPUs will be in full production by the third quarter. Samples are available now. Samples of a 110-MHz version will be available in July. Sample prices range from $2511 to $4019 in single quantities.

The module joins a family of the company's devices and modules that use the HyperSPARC architecture. The family includes Mbus modules with single or dual CPUs as well as a single-chip version (RT628) with 128 kbytes of cache.—by Richard A Quinell

Ross Technology Inc, Austin, TX, (500) 774-7677.

Circle No. 441

Information Superhighway forum for building national infrastructure

The first conference on forming an infrastructure for the National Information Superhighway takes place September 26 to 28 in San Jose, CA. The summit features a keynote address by Dr John McQuillan, an expert in networking technologies; Ethernet inventor Dr Robert Metcalfe's program for building the infrastructure; tutorials; and seminars. In addition, the summit features

- Reviews of applicable technology and architectures
- Commentary from interexchange carriers, cable companies, and governmental agencies
- Assessment of possible foundations, such as telephone networks, cable systems, and Internet
- Debate on alternatives to delivering voice, data, and video via cable TV, copper-based telephone lines, fiber-optic cabling, and wireless
- Appraisal of new and expected industries and business ventures resulting from the superhighway.

—by Jim Leonard

IDG World Expo, Framingham, MA, (500) 545-3976; (508) 879-6700.

Circle No. 442

Group promotes bare-die documentation

The DIE Industry Group, formed by ARPA (Advanced Research Projects Agency) to promote multichip-module technology, has developed a specification for providing models and design information on bare-die devices. That specification, DIE (Die Information Exchange) Format 1.0, provides a standard format and information content for bare-die documentation. The infor-
You found it! Flash370 is a family of seven erasable complex PLDs—with up to a whopping 256 macrocells and 256 I/O pins. Even more remarkable is their 100% routability. This combines with the shortest pin-to-pin delays of any architecture through all speed paths—a blazing 8.5 ns for the 32-macrocell, 44-pin CY7C371. What’s more, you get this high speed with 100% timing predictability. So you never have to struggle with variable timing again.

SURE, RECORD-BREAKING SPEED IN A COMPLEX PLD IS A BIG PLUS BUT IT SHOULDN'T ROUTINELY BE A TEST OF YOUR ABILITY TO HANDLE PLIERS.

(FOLD AS SHOWN FOR THE ALTERNATIVE.)

The Flash370 family's exceptionally clean and simple architecture helps get your products to market faster. And as part of Cypress’s comprehensive UltraLogic™ family, the Flash370 is supported by Warp™ VHDL open design tools. So start designing with a data sheet instead of a soldering iron. And watch the competition fold.

Call for your free Flash370 design kit: Warp™ design tool for the CY7C371, sample certificate and product data. 1-800-858-1810®, Dept. C4H.

*In Europe, fax requests to the above Dept. at (32) 2-652-1504 or call (32) 2-652-0270. In Asia, fax requests to the above Dept. at 1 (415) 940-4337. Warp and UltraLogic are trademarks of Cypress Semiconductor © 1994 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134 Phone 1-408-943-2600.
**SHORTS**

**"Trojan horse" compromises Internet.** The Federal Computer Emergency Response Team has announced a major breach of the Internet communications system. According to team members, perpetrators planted a "Trojan horse" program in various Internet users' systems. The program gathered log-on information from users accessing a specific system through the Internet. The break-in could affect thousands of Internet users, according to the team, which serves as a clearing house for Internet security concerns. Federal Computer Emergency Response Team, Carnegie-Mellon University, Pittsburgh, PA, (412) 268-7080. Circle No. 443

**Aspec to offer $40,000 ASIC design.** Attendees at the Design Automation Conference, scheduled for June 6 to 8 at the San Diego Convention Center, will have a chance to win a $40,000 design award. Aspec Technology Inc will offer a free design of as many as 100,000 gates based on the company's proprietary high-density array, sea-of-gates technology. The design award comprises a complete package, from netlist to database tape. Alternatively, the winner can apply the $40,000 to the purchase of an Aspec Portfolio family of ASIC design tools. Aspec Technology Inc, Santa Clara, CA, (408) 988-4411. Circle No. 444

**Yamaha asserts audio patents.** With the expiration of the original patents covering FM sound synthesis, several manufacturers sought to break Yamaha's virtual monopoly in supplying synthesis ICs to the sound-board market by making or incorporating OPL-equivalent devices. Yamaha has brought suit against them, asserting that still-active US Patents 4,249,447 and 4,813,236 cover the specific techniques used in its OPL chips and are being infringed. Hearings began on May 6. Circle No. 445

**Recognize an outstanding peer**

*Test & Measurement World* magazine is soliciting nominations for its fifth annual "Test Engineer of the Year" award. To qualify, individuals must spend most of their time working on test problems, but a specific test-engineer title is not mandatory. The nominee must work in the electronics industry and be involved with testing, measuring, inspecting, quality assurance, or another related function.

If you're a peer, supervisor, or subordinate who knows a deserving engineer, send a fax to T&MW at (617) 558-4470 for a simple form to complete. All nominations are due by August 15. The magazine will present the award at the International Test Conference in Washington, DC in October. The winner receives a certificate and $1000; the nominator gets $250.—by Joan Lynch

**Human Designed Systems, King of Prussia, PA, (610) 277-8300. Circle No. 447**

**X terminals offer full-motion video**

Human Designed Systems has added full-motion video to its line of RISC-based X Window terminals. Called HDS Video, the capabilities allow users to display full-motion video in as many as four windows on their HDS X terminal screens. HDS Video supports analog and digital video with onboard compression and decompression.

Full-motion video suits applications such as presentations, training, monitoring, and teleconferencing. For teleconferencing applications, the company has also introduced HDS Conference video-teleconferencing application software, which allows multiple X terminal users to communicate over Ethernet and view each other in an X Window.

Users can connect a camera, a video CD-ROM, or a videocassette recorder to a terminal and display the video from this source on the screen in movable, resizable windows. The terminal supports full-screen display of video at 30 frames/sec with broadcast quality.

Digital video allows HDS X terminals to support video in networks for applications such as video teleconferencing. HDS supports the Intel/Microsoft Indeo compression standard and offers optional MPEG hardware decompression.

An optional capability, HDS Audio, allows recording and playback of stereo sound. With HDS Audio, each terminal has an internal speaker and connections for external speakers. Users can also connect an audio source, such as a stereo CD, a microphone, or a tape recorder, to the terminal.

Adding HDS Video or Audio to the company's ViewStation multimedia terminals costs $199 for stereo sound, $199 for digital video, $499 for analog and digital video, and $199/user for the HDS Conference application.—by Fran Granville

**Human Designed Systems, King of Prussia, PA, (610) 277-8300. Circle No. 448**

**“Smart batteries” lower portable-products’ costs**

Duracell and Intel have announced the Smart Battery Data (SBD) and the System Management Bus (SMBus), two "smart-battery" specifications. End users can expect portable products, such as notebook computers, video camcorders, and cellular telephones, incorporating the specifications to have lower costs, more reliable battery-level information, and the ability to adapt to new battery technologies.

A smart battery is a rechargeable
If your interconnect application is an odd-ball, throw it our way. Whether it’s the plating, body or pins that are a little strange, our Solution Casebooks give you a head start on solving the mysteries. They’re free and loaded with ideas on turning otherwise normal interconnects into the bizarre.

Call 1-800-SAMTEC-9 for our complete series of Solution Casebooks. Circle reader service number for our new Full Line Catalog F-193.

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CIRCLE NO. 114
### SHORTS

**IC maker starts East Coast design facility.** Linear Technology Corp is recruiting staff for its recently established Boston Design Center in Burlington, MA. The company seeks approximately 12 linear designers of MOS and bipolar data converters, power-supply and management products, references, comparators, and op amps. The Boston unit joins Linear’s headquarters in California and a similar center in Singapore. Linear Technology Corp, Milpitas, CA, (408) 432-1900. Circle No. 449

**ITT Cannon forms joint venture with ZCF.** ITT Cannon, a supplier of electronic components, interconnection systems, and information-card technology, has formed a joint venture with Zhenjiang Connector Factory (ZCF), the largest connector company in China. ITT Cannon, Santa Ana, CA, (714) 261-5300. Circle No. 450

**Digi-Key earns ISO 9002 certification.** Digi-Key Corp recently earned ISO 9002 certification covering the purchasing, warehousing, and distribution of the company’s electronic components, computer products, and accessories, including value-added assembly processes. Digi-Key Corp, Thief River Falls, MN, (800) 344-4539. Circle No. 451

**Guide explains PCMCIA standard.** The PCMCIA Developer’s Guide provides a comprehensive overview of the Personal Computer Memory Card International Association (PCMCIA) standard. The 450-pg book also offers design examples for PC cards, hosts, and software drivers; it gives information on reference materials. $89.95. Sycard Technology, Sunnyvale, CA, (408) 247-0730. Circle No. 452

**DEC introduces Internet service.** Digital Equipment Corp has announced the Internet Electronic Connection, a set of free services allowing consumers in educational institutions and research laboratories to obtain information about—and place orders for—DEC’s products and services directly over Internet. Digital Equipment Corp, Maynard, MA, (508) 493-5111. Circle No. 453

**Consortium aims to advance technology.** The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has established the Interconnect Technology Research Institute (ITRI). ITRI’s goal is to provide a vehicle for collaboration among the electronic-interconnection industry, government, and academia to develop and deploy advanced technology for printed wiring boards and printed-wiring-board assemblies. IPC, Lincolnwood, IL, (708) 677-2850. Circle No. 454

**Catalog lists more than 1200 software products.** This 95-pg, indexed catalog, “Software for Science,” lists more than 250 new products and 100 CD-ROM titles for astronomy, CAD, curve fitting, data acquisition, electrical engineering, and a variety of other disciplines. In addition, the catalog includes articles on software selection, such as “Equation Editor or Word Processor,” “A Practical Guide to Survey Design,” and “Choosing an Image-Analysis System for Remotely Sensed Data.” Seitech International Inc, Chicago, IL, (800) 622-3345. Circle No. 455

**Booklet helps Internet users get on-line.** This 64-pg, $2.95 booklet, “Internet Public Access Guide,” defines Internet terms; describes Unix commands; and details electronic mail, Usenet news, remote-system access, and information searching. Specialized System Consultants Inc, Seattle, WA, (206) 527-2806. Circle No. 456

**Zap confusing buttons from your remote control**

How many buttons on your TV or VCR remote control go unused because you can’t find the original documentation? What if you have the manual but don’t understand what a button is for—or don’t want to use it—anyway? In an effort to make electronic products easier to use and to battle “technophobia,” Arthur D Little Enterprises has developed a technology that lets you eliminate unwanted or unused buttons from electronic products’ keypads.

Called Custom Control, the technology lets you add, remove, and reposition unwanted or confusing controls from remote controls, telephones, calculators, and other products with buttons or keys. Custom Control supplies the target product with a set of buttons, each having its own electrical/mechanical identity, which corresponds to a feature or function of the product. You select only the buttons or keys you want from this set of controls and then place the controls on a “blank” control panel in whatever arrangement is most convenient. If you change your mind, you can recustomize the controls at any time.

The company is currently negotiating with major consumer electronics companies about licensing. The first implementation of the technology will hit the stores in September—in the form of a universal remote controller.

—by Fran Granville

The world’s lowest power 1MHz 12-bit ADC: Designers of high-end instrumentation and communications systems no longer have to rely on expensive, power-hungry hybrids to fulfill their high speed/high resolution requirements. Because nothing combines low power, high speed, and precision like National’s new 1MHz ADC12062.

Maximum power dissipation of just 75mW at 5V provides the low power consumption needed to improve overall system efficiency. Fast sampling rate of 1MHz is ideal for high-speed data acquisition. Patented EEPROM trimming architecture guarantees AC and DC specs unmatched in the industry: Gain error = ±1LSB (max.), offset error = ±1.25LSB (max.), INL = ±1LSB (max.), DNL = ±0.95LSB (max.), and SNR@100kHz is 69.5dB (min.), ensuring the accuracy of the signal received by a microprocessor or DSP.

On-board 2-channel MUX and sample/hold amplifier, and parallel interface save board space and test costs. Power-down feature increases battery life in portable instrumentation designs.

In oscilloscopes, signal analyzers, and data acquisition boards for test and measurement applications, National Semiconductor’s ADC12062 simply does more. On less. 1000-piece price (U.S.) starts at $29.30.
The world’s fastest 12-bit data acquisition system: There are certain applications — diagnostic systems, portable instrumentation, industrial control — where nothing short of a high-speed, low-power, fully integrated data acquisition system will suffice. Fortunately for those applications, there’s nothing faster, more power-efficient, or more fully integrated than the LM12H454/8.

Maximum conversion rate of 5.5µs (minimum throughput rate of 140ksp/s) - The industry’s lowest power consumption: 34mW (50µW in powerdown mode) - Mixed analog and digital technology creates a complete system on a chip, fully capable of providing stand-alone operation - High integration simplifies complex designs by reducing testing and debugging - Analog front-end consists of a self-calibrating 12-bit plus-sign ADC with sample and hold, a reference, and a four- or eight-channel MUX - Digital features include an eight-word instruction RAM, a sequencer, a 16-bit timer, and a 32-word FIFO - "Watchdog" comparison mode provides quick (1.4µs) threshold detection and alarm monitoring.

Guidance and control. Medical instrumentation. Energy management. For applications that demand it all, the LM12H454/8 delivers. 1000-piece price (U.S.): $17.00.

The ADC12062 offers the industry’s best combination of power consumption, speed, and precision. The LM12H454/8 provides an unmatched mix of high speed and high integration. For more information, call 1-800-NAT-SEMI, Ext. 287.
offset drift of 10µV/°C (max.) - Increased dynamic range through rail-to-rail output swing - Low voltage noise (e_n=22nV/√Hz @ 1kHz) provides higher signal-to-noise ratio than JFET input type meter amplifiers
- Low supply current of 750µA (max.) is ideal for power-sensitive applications and minimizes heating effects on input current and offset voltage
- Available in plastic DIP - Designed and guaranteed for operation over the industrial temperature range (-40°C to +85°C) - Available in A Grade (25fA), B Grade (100fA), and C Grade (1000fA).

The LMC6001 is exactly what you need for transimpedance amplifier applications. In 1000-piece quantities, pricing (U.S.) starts at: A Grade - $8.50; B Grade - $5.15; C Grade - $1.40 (8-pin PDIP).
Versatile: High speed, high drive, low power.

The LM6181/2 and LMC6572/4: You no longer have to pay a premium for op amps that deliver solid, all-around performance.

LM6181/2: Single- and dual-current feedback amps for video, communications, and imaging systems - 100MHz unity gain bandwidth and 100mA of output current - No-hassle, one-chip solution eliminates output buffer - Differential gain of 0.05% and differential phase of 0.04° - 2000V/µs slew rate and 50ns settling time (0.1%) - Tight offset voltage (3mV max.) and input bias current (Ib+ = 2.0µA, Ib− = 5.0µA max.) for precision needs - Fully specified for ±5V and ±15V operation - DIP and SOIC.

LMC6572/4: Provides guaranteed 2.7V and 3V single-supply performance for portables and mobile communications systems - Ideal for interfacing with 3.3V digital logic regulated or unregulated supplies - Rail-to-rail output swing maximizes S/N and dynamic signal range, providing an efficient interface to ADCs - Wide input range from below ground to 800mV below the positive supply - Low input current of 20fA increases accuracy - Low supply current of 40μA - 120dB voltage gain/amp - Specified for 100kΩ and 5kΩ loads. In quantities of 1000, pricing (U.S.) starts at: LM6181 - $2.00; LM6182 - $3.60; LMC6572 - $.90; LMC6574 - $1.20.

For more information on the LMC6001, LM6181/2, and LMC6572/4, call 1-800-NAT-SEMI, Ext. 287 for free product sample kits.
3-volt analog: Fueling the portable wave.

Maximum performance on a minimum of power:
The popularity of portability is rising fast. Portable computing, mobile communications, and handheld instrumentation designs need low-voltage solutions that will reduce system size and extend battery life.

That's why National is leading the way by offering high-performance 3V analog products in data acquisition, power management, and amplifier ICs. Products that save power without sacrificing performance.

LM12L454 8 12-bit plus sign data acquisition system: Complete system on a chip with 106ksps throughput, 15mW (max.) power dissipation (5µW in power-down mode), and all the functionality needed for stand-alone operation - ADC12L030/2/4/8 12-bit plus sign A/D: Fastest 3V 12-bit serial A/D (maximum conversion time of 5.5µs) at 15mW (max.) power dissipation (40µW in power-down);

configurable registers - LMC6572/4 op amp: Low supply current of 40µA/op amp minimizes power consumption; guaranteed 2.7V and 3V single-supply performance;

low input current increases accuracy - LMC6482/4 op amp: Rail-to-rail input and output increases dynamic signal range at 3V; lower offset voltages and higher CMRR increases precision - LM2574/5/6 SIMPLE SWITCHER® power converter: First easy-to-use power converter family with 3.3V output and guaranteed system performance; requires just four external,
off-the-shelf components; design software available -

**LP2950/51 low dropout regulator:** Very low dropout voltage of 380mV extends battery life; low quiescent current of 75µA reduces power consumption and power dissipation -

**ADC12L038**

- **3V analog solutions**
- For 3V analog that will fuel your imagination as well as your designs, call 1-800-NAT-SEMI, Ext. 287.
- We'll send you free product sample kits or information kits.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PRICE*</th>
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<tbody>
<tr>
<td>LM121454/8</td>
<td>$15.00</td>
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<td>ADC12L030</td>
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<td>LM4041</td>
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</tbody>
</table>

*Quantities of 1000, U.S. only

system size; adjustable voltage option (1.24V to 10V) provides design flexibility.

All of National's 3V analog solutions are designed to increase the performance of your portable designs — while reducing power consumption. And all of them come with the quality and reliability you expect from the original leader in analog IC technology. For pricing information, consult the box to your left or call the number below.
Magnetics: Opto-less chipset brings reliable power supplies offline.

The world's only 1MHz magnetically coupled offline power supply chipset: For the first time, high-speed pulse magnetics replace opto feedback devices. The result is smaller, more efficient, more reliable switchmode power supplies. The reason is National's LM3001/3101 offline power supply chipset.

Two-chip solution: LM3001 primary side driver and LM3101 secondary side controller:

Fast AC feedback provides quicker response than optos - Up to 1MHz switching frequency enables the use of smaller inductors and capacitors.

LM3001: Accepts AC pulse feedback - 10ns rise and fall times provides greater efficiency and fast response to faults - On-board oscillator manages chip start-up - 2.5A peak current drives MOSFETs at high speed - Dual-level current limit provides virtually fail-safe operation: Cycle-by-cycle current limit offers fast current protection, while second-level current limit initiates complete shutdown in the case of a major fault.

LM3101: Generates AC pulse feedback - Pulse-width-modulator (PWM) provides master pulse width control - ±2% voltage reference for high-precision control of output voltage - Trimmed on-board oscillator offers programmable frequency control - 8MHz bandwidth error amp ensures fast, stable, easy loop compensation - Frequency shift for short circuit assures the best possible overload protection. 100-piece pricing (U.S.) starts at: LM3001 - $1.85; LM3101 - $1.70.
The world's first dual micropower low dropout regulator: When it comes to extending battery life in portable applications, two regulators are better than one. Case in point: National's LP2956. Two low dropout regulators in one package make it possible to shutdown one system and save power, while keeping a second system active.

Low dropout voltage of 470mV extends battery life - Low quiescent current of 170µA reduces power consumption and power dissipation -

In portable applications, the dual LP2956 shuts down inactive systems while maintaining continuous power for essential functions.

Independent, auxiliary low dropout regulator enables second load (up to 75mA) to be driven while driving a primary load of up to 250mA - Electronic shutdown allows device to be turned on and off as desired - Auxiliary comparator can be used for low-battery detection, fault detection, or as a reset signal to a microprocessor - Error flag for the main regulator indicates when it has fallen out of regulation by more than 5%.

The LP2956 is the highest performance dual low dropout regulator available. It's the best thing to happen to your battery-powered designs since the batteries themselves. 100-piece price (U.S.): $2.95.

If your design plugs into a wall socket, we've got your power supply chipset. If it runs on batteries, we've got your low dropout regulator. To get your free product sample kits, call 1-800-NAT-SEMI, Ext. 287.
03% THD:
60 watts never sounded as good as this.

The world's best sounding monolithic audio amplifier: See if you like the sound of this.

National's LM3886T provides a higher standard of high fidelity, as well as maximum power with maximum protection.

Lowest typical total harmonic distortion (THD) from 20Hz to 20kHz at 25, 40, and 60 watts of continuous power provides the industry's best distortion/power rating.

- Signal-to-noise ratio is greater than 95dB min.

The 60-watt LM3886T enables better, louder, longer sound in high-end audio applications like A/V surround sound receivers.

(Note floor of 2.0µV), meeting the demands of CD-quality digital sound.

Mute function eliminates transients at power up and power down — Devices can be easily bridged together — spike™ self-protection circuitry adjusts output drive capability according to operating conditions, protecting output transistor array from overvoltages, undervoltages, or current limiting conditions, and providing thermal shutdown.

Dynamic SOA protection ensures that power transistors won't be destroyed — even if faults continue for extended periods.

In component and compact stereos, surround-sound amplifiers, and high-end stereo TVs, you get better sound with National's audio amplifiers.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>THD (typ.)</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2876T</td>
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<td>LM3876T</td>
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<td>40W</td>
</tr>
<tr>
<td>LM3886T</td>
<td>0.03%</td>
<td>60W</td>
</tr>
</tbody>
</table>

* from 20Hz to 20kHz
130 MHz:
High-speed
LM1205 saves
board space.

Complete broadband preamplifier system: When used with National's LM2419 CRT driver (see back cover), the LM1205 130MHz RGB video preamplifier replaces up to 36 components, compared to using standard preamps and discretes.

Provides the entire amplifier path required between the rear chassis input and the cathode for 1024 x 768 monitors - Each channel contains matched video amplifiers - Gated, single-ended input and black-level clamp provide brightness control - Matched DC-controlled attenuators provide contrast control - DC-controlled sub-contrast attenuators provide white balance - All DC control inputs are high impedance and operate over a 0 to 4V range for easy interface in microcontroller-based systems - Blanking circuit clamps the video output voltage to within 0.2V of ground - For high-speed, space-conscious designs.

In high-end, 17-inch RGB CRT monitors, 1280 x 1024 pixel systems, video AGC amplifiers, and wideband amplifiers with gain and DC offset controls, the LM1205 gives you more performance. While using less board space. In quantities of 1000, pricing (U.S.) starts at $2.50.

To fully appreciate the sights and sounds of National's audio and video ICs, call us at 1-800-NAT-SEMI, Ext. 287 and we'll send you free sample kits containing product samples, a blank applications board, data sheets, and application notes.
High-performance triple CRT driver for high-resolution monitors: Picture a device that provides resolution up to 1024 x 768 in color monitors while simplifying overall design. You're picturing the LM2419, National Semiconductor's triple 65MHz CRT driver. Typical rise/fall time of 5ns provides clean, sharp signal transition edges for high-resolution images - 65MHz video bandwidth at 50Vpp output swing with 8pf load for a bright screen and a clear image - Three drivers match red, green, and blue channels in one device - Available in industry-standard TO-220 molded power packages - Electrically isolated heat sink may be grounded for ease of manufacturing and improved RFI/EMI shielding - Pin-for-pin compatible with LM2416, simplifying upgrades - No low-frequency tilt compensation required. For direct cathode drive capability in VGA, SVGA, XGA, IBM and Macintosh monitors, nothing looks better.

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<table>
<thead>
<tr>
<th>Organization</th>
<th>Refresh Rate</th>
<th>Access Time (ns)</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Mx16, 3.3V</td>
<td>1K, 4K</td>
<td>70/80</td>
<td>SOJ, SOP</td>
</tr>
<tr>
<td>1Mx16, 3.3V</td>
<td>Self-Refresh</td>
<td>70/80</td>
<td>SOJ, TSOP</td>
</tr>
<tr>
<td>1Mx16, 5V</td>
<td>1K, 4K</td>
<td>60/70/80</td>
<td>SOJ, TSOP</td>
</tr>
<tr>
<td>1Mx18</td>
<td>1K</td>
<td>60/70/80</td>
<td>SOJ</td>
</tr>
<tr>
<td>2Mx8</td>
<td>2K</td>
<td>60/70/80</td>
<td>SOJ, TSOP</td>
</tr>
<tr>
<td>4Mx4</td>
<td>2K, 4K</td>
<td>50/60/70</td>
<td>SOJ, TSOP</td>
</tr>
<tr>
<td>16Mx1</td>
<td>4K</td>
<td>50/60/70</td>
<td>SOJ</td>
</tr>
</tbody>
</table>

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Make a note

We inadvertently neglected to include Lambda in our Special Report on distributed power (EDN, April 28, pg 54). You can contact the Melville, NY, company at (516) 694-4200. Or Circle No. 357.

It was also Lambda, not Calex, that should have gotten the credit for the thermogram that ran on pg 56; we’ve reprinted the photograph here.

Debugging debate

I read your article titled “Teaming a logic analyzer with a debugger provides advantages to both tools” (EDN, January 20, pg 21). Excellent discussion.

I’ve spent about eight of my 12 years interested in embedded-system development tools. I’ve written and hacked around with ROM monitors for x86, 680x0, AMD29K, and MIPS. And I’ve written a full source-level debugger (COFF-based) for the same processor families. I’ve also built some trivial x86-based hardware that integrates some basic logic-analyzer stuff with the monitor for firmware debugging (address/data comparators, etc), and I’ve found that to be very useful.

I most definitely agree with you that the logic-analyzer/debugger combination is an extremely effective development environment. As a matter of fact, referring to the “Looking ahead” box in your article, my debugger has the “dashed line from the logic analyzer to the workstation.” This feature isn’t needed every day, but when there’s a tough bug lurking, it is definitely a priceless capability. This can actually be a simple interface if it can be assumed that the logic analyzer can dump its trace data in some columnar format.

One of the nice things about the logic-analyzer/debugger combination is that the logic analyzer is not a piece of equipment that needs to be purchased solely for the person writing the drivers or really low-level firmware. It was probably already purchased for the hardware-design group and has been used for a lot more than just setting complex breakpoints. My point is that if the debugger “knows” a little about the logic analyzer, then there is no need for an emulator; hence, no need to put out the extra money (which is not trivial). Emulators don’t come cheap, especially for the high-speed stuff.

I see only two real deficiencies in the logic-analyzer/debugger approach. As you mentioned in your “Cons” list, the logic analyzer is helpless when it comes to the CPU’s cache, and, along those lines, it can also be a bit confusing to deal with any kind of bus-unit prefetch (even without cache). In the case of cache, instruction/data access can occur without the logic analyzer’s knowing it, and, in the case of prefetch, instructions can be fetched (seen by the logic analyzer) but not executed.

If you have a decent ROM monitor, then some of the cons mentioned can also disappear. If the trigger of the logic analyzer is tied into the same interrupt as the ROM monitor’s UART, then it can look just like a breakpoint. Also, with a decent analyzer/debugger interface, you can debug at the high-level-language level.

This leaves me with two questions, and I’ll follow them with the only answers I can think of.

1. Why aren’t more CPU manufacturers providing a debuggable processor? All that is really needed is the equivalent of the “watch trap” on the MIPS R4000—the ability to set a data breakpoint. What is so difficult about that? I know the 386 has one, but why hasn’t it become a generic feature like the breakpoint trap? I’ve always assumed that it must be cost, but I would also think that a feature like that could swing a potential customer from one CPU to another. I don’t get it.

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advantage an emulator gives a firmware developer that a logic analyzer has trouble with is the fact that the logic analyzer is “external” to the processor; hence, it can’t handle internally cached memory accesses. But based on the added cost, that doesn’t justify the need for an emulator anyway. Usually, you can disable cache in some way to allow the logic analyzer to do its thing. My only conclusion here is that the hardware is not designed with debugging in mind. Some very simple up-front work can usually save a lot of debugging time down the road. As a result, when the time comes to put on some firmware, somebody has to dish out some big bucks.

My conclusion is that there really isn’t much consideration for debugging at the hardware-design stage. Even if the addition of a debug UART and some RAM is out of the question for the actual production version of the hardware, facilities for a debug daughterboard can easily be justified in most cases. Then, depending on the energy level of the designer, the debug daughterboard can even eliminate the need for the logic analyzer in many cases. For a minimal cost (especially when compared to the price of an emulator or a logic analyzer), you can add real-time trace, multiple-state breakpointing, convenient logic analyzer connections (if still necessary), high-speed download, etc—the works!

Ed Sutter
AT&T Bell Labs

More to know about ATM...

The article in EDN’s March 3 issue (pg 66) on the ATM convergence-sublayer and physical-interface devices was excellent. We are very excited about these products because they provide a complete, intelligent ATM termination when coupled to our ATMizer Architecture. The author of the article, however, was unaware of our ATM offerings.

The ATMizer is the first reprogrammable ATM cell-processing architecture. The heart of the architecture is an on-chip RISC-based ATM-processing unit, which allows customers to quickly and easily update their products as the
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ATM standard evolves. Users simply download new code to accommodate changes in the ATM standard or congestion-control algorithms. The ATMizer performs segmentation and reassembly and all layer operations up to 155 Mbps. It supports all ATM adaptation layers and can process up to 64,000 virtual channels of voice, data, and video simultaneously.

The ATMizer Architecture is available as a single chip or as an ASIC architecture to complement products mentioned in EDN's article. In addition, this flexibility and performance is being used to address the open issues raised in the Special Report, including congestion control, LAN emulation, and traffic management.

Tony Stelliga
Vice President
Telecom Products Div
LSI Logic
Milpitas, CA

...and more

EDN has received some updated information for the ATM Special Report (March 3, pg 66). The correct phone number for AMCC is (800) 925-2622. Also, if you want to contact the ATM Forum, the company reports that it has moved to new quarters in Foster City, CA; phone (415) 578-6860.

Cooling hot µPs

We believe your coverage of the hot microprocessor problem (“Cooling hot microprocessors,” EDN, January 20, pg 40 and “Shrinking devices put the squeeze on system packaging,” EDN, February 17, pg 41) has shortchanged your readers in two areas. Among the fastest-growing techniques for cooling board-mounted processors and other hot devices is the use of low-profile, tape-mounted heat sinks and extremely compressible thermal-gap-filling materials.

The world's leading supplier of double-sided thermal tapes and thermal gap fillers is Chomerics Inc (Woburn, MA). In both thermal and adhesion properties, our Thermattach tapes have set the performance standards in PC markets worldwide. A unique, stable, thermally conductive, pressure-sensitive adhesive (PSA) makes them suitable for even high-temperature applications—where traditional acrylic PSAs have a tendency to lose their grip.

In thermal gap fillers, we believe our Cho-Therm T274 and A274 materials are the only commercially available, easy-handling alternatives to bags of fluorocarbon liquid.

In general, we found both articles well-written and informative, but their exclusion of references to Chomerics' thermal interface products left us somewhat overheated.

Robert A Rothenberg
Director of Market Development
Chomerics Inc
Woburn, MA

New number

ATI Technologies Inc, which was discussed in the article entitled “New chips give PCs TV-quality video” (EDN, March 31, pg 42), has a new telephone number. Contact the company at (905) 882-2600.

Call a different number

We appreciate the reference to our Video Integration Processor and our OEM customers, S3 and Xtec. We are great IBM chip designers, but alas, we are not part of IBM Microelectronics. We are part of IBM's Networking Hardware Div in Research Triangle Park, NC. Your readers will want to call a different number from the one listed in your manufacturers' listing to get information on the processor, which is offered as an OEM product. Readers can call (919) 543-7976.

George M Henke
Program Manager
IBM Networking Systems

Listen up

In response to Mr Green's (Unilever Research) "Listen to your computer" letter: We incorporated an audio monitor in our Texas Instruments seismic data processor (computer) in 1959. We drove a speaker from a signal counted down from the AOC (Acquire anOther Command), the signal that initiated the next instruction fetch from memory.

We originally incorporated it to tell us when the computer had halted. How many times have you sat in front of that infernal machine, wondering if it were caught up in some endless loop, with no visible means of telling? In our case, we also had almost every operation blinking one or more lights, but the lights only told us something was happening.

By having a predefined low-frequency tone generated, we could know if the machine had stalled. Also, if it did get into a loop, the constant, repeating sound would indicate a failure.

Our (and the customer's) operators soon got to know the sequence of tones generated in different portions of the programs and could tell what was going on and how long a particular program could be expected to continue.

Needless to say, but I will anyway, our smart-as-a-whip engineers found a way to make whimsy of this capability. During the 1964 Christmas season, I went back to the system-checkout area and heard Christmas music playing away. Upon investigating, I found it emanating from my computer. Those clever people had found a way to write programs that would exercise that sound monitor.

"Listening to your computer" is not as strange as it sounds. For what it's worth, and thanks for your column.

John Harrett
Agoura Hills, CA

Sound off

"Signals & Noise" lets you express your opinions on issues raised in the magazine's articles or on any engineering-related topic. Send letters to EDN, 275 Washington St, Newton, MA 02158; fax (617) 558-4470. Or use EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter ss/soapbox, then W to write us a letter. You'll need a 2400-bps (or less) modem and a communications program set for 8,N,1. EDN reserves the right to edit letters for clarity and length.
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<table>
<thead>
<tr>
<th>SCSI</th>
<th>FAST SCSI*</th>
</tr>
</thead>
<tbody>
<tr>
<td>53C90A</td>
<td>53CF90A</td>
</tr>
<tr>
<td>53C90B</td>
<td>53CF90B</td>
</tr>
<tr>
<td>53C94</td>
<td>53CF94</td>
</tr>
<tr>
<td>53C96</td>
<td>53CF96</td>
</tr>
</tbody>
</table>

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Technological proof of innocence: Part 1

Life has certainly gotten more complicated since I moved to Massachusetts two and a half years ago. The fables about terrible Boston driving and parking don't tell half of the story. I've even received a parking ticket for parking in a place I've never been at 2 AM on February 27. Now I'm sure that my car and I were both safe, warm, asleep, and at home on that night, at that time.

On the designated day, I went to the town that issued the parking ticket and pleaded my case. Now, we're very efficient in Massachusetts. You don't appeal parking tickets in court; you go straight to the collector of fees, taxes, and fines. The person behind the desk listened to me, got up, looked on the computer, and assured me that it was indeed my car that was illegally parked.

I asked to see the ticket. Once again, the clerk got up, rummaged in a closet for 10 minutes and returned with the actual ticket. It was my license number on the ticket all right, if you ignored the unreadable third character. However, the ticket identified the car as a brown Ford, and I drive a gold Toyota. "Aha," I said, "that's not my car!" The clerk replied, "Hey, you can't expect the officer to get everything right at 2 in the morning. That's your license-plate number. Pay up."

This experience prompted me to start thinking about the use of technology to prove innocence. Governments have plenty of technology for pressing guilt upon us. We could use some defense.

In the movie "Back to the Future," Doc Brown returns from the future in his time-traveling DeLorean with a bar-coded license plate. It seems to me that we ought to seriously consider adopting license plates that carry bar codes or other machine-readable identification in addition to human-readable numbers. Police could use scanners to read these plates at a distance with better accuracy than what I experienced from my brush with the parking patrol.

Note: This is the latest in a series of articles on C-Quad engineering. C-Quad (or C') stands for the convergence of computer, consumer, and communications technologies.

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13/5/94

CIRCLE NO. 66
System simulation embraces real-time control prototyping

BRIAN KERRIDGE, Senior Technical Editor

System simulation is an important design activity in control-engineering applications. But, while most simulation products focus on conceptual issues, relatively few readily assist you in implementing a design. The few products that do support implementation incorporate direct links to development hardware and, overall, form integrated rapid-prototyping systems.

The key feature of rapid-prototyping systems is fast transfer of a slow-motion “off-line” simulation running on a PC or workstation, to a “real-time” simulation running on dedicated DSP hardware. These simulators rely heavily on block diagrams for model building and automatic coding for generating source code, usually in C. These two features alone are instrumental in achieving rapid prototyping and, in consequence, enable a low-cost route to design iteration—an unavoidable feature of control-engineering developments. In practice, automatic coding takes only a few seconds, and, for a system that’s already initialized, you can complete one design iteration in a matter of minutes. Fig 1 outlines the design-flow path of a typical rapid-prototyping system.

Simulating real-time control systems requires that you model not only a controller’s functions, but also the dynamics of the plant you want to control. Such a system offers you the rapid-prototyping options of a simulated controller driving a real plant, an embedded real-time controller driving a simulated plant, or a mixture of the two. Fig 2 illustrates these options.

No matter which option you choose, rapid-prototyping systems offer substantial timesaving benefits—from concept to reality—and other important benefits. Simulator vendors cite examples of 50% cuts and more in project time (see box, “Rapid prototyping shortens DC-X space-vehicle development”).

As a prelude to adopting one of the prototyping options, it’s useful first to transfer an off-line simulation of the controller and the plant to a DSP test bed. This step moves the application closer to reality and allows you a first opportunity to examine critical timing in your overall control strategy. For example, at this stage, sampling-time parameters you build into your models may force elements of the simulation to require service in synchronism with the system.
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CIRCLE NO. 87
REAL-TIME SYSTEM SIMULATION

clock. Failure to meet model sampling times means your DSP test bed ceases to represent a real-time model and implies your system needs more DSP power.

In practice, monitoring software forewarns you of a system crash and, even before attempting a real-time simulation run, indicates when a system cannot execute in the sampling times you specify. Increasing system power is simply a matter of installing more DSP hardware, and all systems include multiprocessing expansion for this purpose.

Specifying model sampling times in relation to real-system response times requires modeling experience and lets you trade off modeling integrity and complexity with DSP power. For example, it would be overkill to specify a 10-msec sampling time for a model of a valve that takes several minutes to change state. On the other hand, a 10-msec sampling time is grossly inadequate for a crankshaft-sensor output on a high-performance auto engine.

DSP emulates control or plant

Of the main prototyping options, using a DSP test bed to emulate only a controller and its I/O functions is a fast route to proving a control concept and refining control parameters. However, using DSP to emulate a plant, or “hardware-in-the-loop” simulation, offers major development-time reductions.

Overall, the arrangement allows you to test the validity of controller electronics well in advance of the availability of the live plant. This feature is significant because most control-engineering applications accommodate the vagaries of a real-world environ-

Fig 1—Rapid prototyping systems form an integrated environment for modeling, simulation, design, and real-time testing. (Courtesy dSpace Inc)

ment, thus increasing the likelihood of design flaws appearing late in a development cycle.

In addition, performing live-plant prototyping at the outset is often inconvenient and unsafe, as in automotive,

LOOKING AHEAD

MS-Windows is increasingly the preferred design-tool environment for engineering applications, yet Integrated Systems’ Matrix, remains for the time being a workstation-only product. The company is planning to add a multiprocessing TMS320C40 card to its RealSim low-cost PC test-bed product line. Additionally, Integrated Systems and Mentor Graphics will soon support links between Matrix, and Mentor’s System Design Station/QuickSim2 simulator. This combination will allow you to cosimulate a system using the RealSim DSP test bed to simulate a plant and QuickSim2 to emulate control. QuickSim’s VHDL model outputs will provide a fast route to custom-built controller chip sets.

The MathWorks plans further graphical-user-interface enhancements to some of its toolbox options, including its system-identification tool, as part of a general effort to attract engineers, as well as academics, to use these products.
REAL-TIME SYSTEM SIMULATION

in-flight, and nuclear-control applications. This type of prototyping is inconvenient because live prototypes involve complex and substantial parts that take many months to fabricate and assemble. It’s unsafe because loss of control threatens human life.

Hardware-in-the-loop simulations offer you other interim rapid-prototyping steps. For example, you can progressively replace sections of a simulation as a real plant becomes available or as system confidence increases. In addition, you can even emulate a controller and a plant separately in two DSP test beds and watch them play. In fact, the combinations are virtually endless.

In an off-line simulation, your host computer conveniently handles models of both controller and plant functions, but simulation models need separate treatment for real-time simulation.

For example, a hardware-in-the-loop simulation requires that you selectively code only those sections of a block diagram that represent the plant. In practice, rapid-prototyping tools ease this task by enabling you to select in a window only those sections of a block diagram you need to code before downloading to the DSP test bed. Additionally, connections-editing software assigns ADCs, DACs, and other I/O hardware in the DSP test bed to appropriate I/O signals on your block diagram.

Simulators link to DSP systems

The principal vendors offering integrated rapid-prototyping tool sets are Integrated Systems Inc, The MathWorks Inc, and dSpace Inc. Prices vary widely, depending on whether the host is a PC or a workstation and on how much DSP power you build into your test bed. Typically, though, expect to pay $15,000 for a very basic setup to more than $50,000 for a “power-user” setup. Automatic coding software adds $10,000 or more to these prices (see box, “Automatic coding cuts design-iteration time”).

Integrated Systems’ Matrix, modeling, simulation, analysis, and code-generation tools run on Sparc and VAX workstations and combine with the company’s RealSim series of real-time hardware test beds. In addition, Matrix, requires runtime software that includes a graphical user interface, cross compilers, device drivers, and an Ethernet interface. RealSim comes in a range of configurations from a 486-based portable PC with a single TMS320C30 processor card to a high-end Multibus chassis that accommodates one to 11 I860s. A wide range of I/O options includes ADCs, DACs,

**Fig A** (b) shows an example section of code.

Automatic source-code generation is a key feature of rapid-prototyping systems. Using such systems, you first create a system at the block-diagram level and perform “off-line” simulation. Then, the rapid-prototyping systems’ pull-down menus offer you automatic-coding options.

For example, The MathWorks’ Simulink C-code generator ($9999) gives you a choice of C-code styles, and Integrated Systems’ SystemBuild Autocode ($15,000) lets you produce code in Ada, C, or Fortran. Fig A (b) shows an example section of code.

Automatic coding handles continuous, discrete-time, or hybrid-control systems. Coders also embody a task scheduler to prioritize separate operations in multirate systems, for example, acting on sensor inputs before less-frequent user inputs.

Vendors maintain that automatic coding produces code optimized for speed in real-time operation. For example, the coder unrolls loops, minimizes functions calls, and removes unnecessary ones and zeros from numeric computations. There is no doubt that experienced real-time programmers can further optimize code for target processors, but vendors suggest that for most applications you modify your system at the block-diagram level and recode automatically. This approach routinely maintains the status of your block diagram and implementation at a current level and eliminates additional documentation-control work.

```
/* Function to compute block outputs */
static void simBlockOutputs (x, u, S)
    double * x; double * u;
    double * B, * P; / *Block inputs and outputs */
    double * ssGetBlockIO (S); / *Block inputs and outputs */
    double * ssGetBlockParam (S); / *Block parameters */

    / * Step input: Step Fcn / *
    if (ssGetSampleHitEvent (S, 0))
        B[0] = P[1];
    else
        B[0] = P[2];

    / * Transfer function: Read/Write Head Dynamics / *
    B[1] = x[1];

    / * Summing junction: Sum / *

    / * Gain block: Gain (Kc) / *

    #ifdef SINGLE RATE
    if (ssGetSampleHitEvent (S, 0)) /* Is it a sample hit? */
    #endif
    /
    / * Transfer function: Digital Compensator / *
}
```

Fig A—The block diagram (a) represents a disk-drive head and controller, modeled using The MathWorks’ Simulink library functions. The C-code-generation tool transforms the block diagram to the source-code listing (b), which is comprehensible and well-commented.
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and digital and resolver-synchronous I/O. The product range also includes the DocumentIt software package, which automatically produces a textual description of a system, including tables, hierarchies, and subsystem lists.

The MathWorks does not produce a real-time test bed for its Matlab analysis and Simulink simulation software, but the company supports hardware from dSpace Inc. dSpace offers a wide range of PC plug-in DSP, memory, and I/O cards. Using these cards, you can site your DSP hardware within your PC host computer if it has enough expansion slots. For workstation and already-full PC hosts, the company offers Ethernet-linked, 6- and 20-slot expansion boxes and a depowered 7-slot ruggedized version for field use.

dSpace's DSP cards include single-processor TMS320C30 and TMS320C40 models and a 4-processor TMS320C40 version. The company also provides essential software to process source code and simulate a real plant situation.

**Fig 2—Real-time simulation offers you two main options:**

(a) using DSP hardware to mimic an embedded controller that interfaces with actuators and sensors in a real plant situation and (b) using DSP hardware to simulate the dynamics and I/O signals of a plant connected to a real embedded controller, known as “hardware-in-the-loop” simulation.

**RAPID PROTOTYPING SHORTENS DC-X SPACE-VEHICLE DEVELOPMENT**

Using Integrated Systems' Matrix, rapid-prototyping tools, McDonnell Douglas Aerospace engineers developed flight-control software for the Delta Clipper Experimental (DC-X) space vehicle in 10 months. McDonnell Douglas engineers estimate that the cost of developing software using rapid prototyping is less than 50% lower than using conventional hand-coding. These productivity gains reflect similar reductions in overall project-development time down to less than two years, enabling first-flight trials last August.

The DC-X, a reusable, relatively low-cost, fast-turnaround vehicle, is the forerunner of next-generation satellite launchers. Vertical landing and take-off of the DC-X launcher pioneers new concepts in space-vehicle flight dynamics, requiring equally innovative control algorithms. Particularly demanding is the independent control of four rocket engines on gimbals that maneuver the launcher.

McDonnell Douglas designers used Matrix tools to develop around 30,000 lines of Ada code for the flight- and navigation-control algorithms. In addition to Matrix's core SystemBuild modeling and simulation tool, the company's designers used Interactive Animation, Autocode, and the RealSim test bed for real-time simulation.

Using SystemBuild, designers modeled the DC-X's flight behavior and control functions. After refining performance in off-line simulation runs, designers used Autocode to generate code for real-time testing. The Autocode feature generated separate code representing flight behavior and controller functions. Flight-behavior code was targeted to a RealSim test bed, and controller code was targeted to the real-world DC-X in-flight computer. Running RealSim and the in-flight computer as a closed-loop environment in real time demonstrated the performance of the overall control strategy far in advance of firing up real rocket engines.

Using automatic coding to produce 30,000 lines of Ada code, McDonnell Douglas achieved a 2-year concept-to-launch time with the DC-X space vehicle.
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  - Circle No. 358

- **Hyperception Inc**
  - Dallas, TX
  - (214) 343-8525
  - Circle No. 359

- **Integrated Systems Inc**
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- **McDonnell Douglas Aerospace**
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allows you to adjust control settings, which, in turn, modify control parameters on the fly during a real-time simulation.

One of the limitations of hardware-in-the-loop simulations is that the plant simulator may not be able to mimic sensor output signals accurately in high-speed systems. For example, in advanced automotive-engine management, it takes around 2-µsec timing resolution to sense 0.1° angular rotation at 8000 rpm. Also, even seemingly mundane signals representing slow-changing temperature and pressure may require much higher bandwidth noise elements to preserve the integrity of the overall simulation. In general, there's no chance that the main DSP plant simulator can also generate such time-critical outputs, and, therefore, the system needs additional hardware.

dSpace has recently introduced such a product, DS2301, which uses six TMS320C31 processors and 16-bit DACs. The DS2301 autonomously produces six high-speed output waveforms with edge resolutions below 1 µsec. C code programs the signal-generation algorithms, which are calculated online. dSpace calls the technique “direct digital synthesis” (Ref 2).

References


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- Symmetrical Switch Points
- Superior Temperature Stability
- Operation From Unregulated Supply
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- Reverse Battery Protection
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability ...
- No Moving Parts
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- Open-Collector 25 mA Output ...
- Compatible with Digital Logic
- Reverse Battery Protection
- Activate with Small, Commercially Available Permanent Magnets
- Solid-State Reliability ...
- no moving parts
- Small Size
- Resistant to Physical Stress

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- 4.5 V to 6 V Operation
- Magnetically Optimized Package

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12-BIT ADCs

ple, stand-alone types to highly integrated ICs, such as National Semiconductor's LM12434 and 12438. These converters offer much more than core-ADC and data-acquisition-IC features such as multiple input channels. Each also incorporates an instruction RAM, an event sequencer, and a 32-word conversion FIFO buffer. These recently introduced 3 to 5.5 V power-supply versions also have a power-down output.

The table's converters also feature a variety of input ranges, power-supply voltages (although single 5 V is the most common), package sizes, and variations on or departures from the familiar successive-approximation-register (SAR) architecture.

Inputs range from 0 to 2 V and ±2.5 to ±10 V, sometimes irrespective of supply voltage. For example, Analog Devices builds its 789x SAR-type converters on a BiCMOS process so that these 5 V ADCs can handle inputs of ±10 V. The process allows for the input to go 10 V above the supplies. ADCs built on standard CMOS processes usually have much more restricted input ranges that can go only 0.3 V above the supply, for example.

These converters are also much smaller than their 12-bit predecessors. With just a few exceptions, virtually all of the converters come in both DIP and SOIC packages, and two fit into 8-pin SOICs: Analog Devices' 125-k-sample/see AD7893, and Linear Technology's 12.5-k-sample/see 1286/98. Maxim also

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part no.</th>
<th>Speed</th>
<th>Key features</th>
<th>Power (mW max)</th>
<th>No. of pins</th>
<th>Price (1000)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Devices Circle No. 301</td>
<td>AD7893/6</td>
<td>125 k samples</td>
<td>Serial, 5 V supply, T/H 0 to 2.5 to ±10 V input range</td>
<td>50</td>
<td>8</td>
<td>$9</td>
</tr>
<tr>
<td></td>
<td>AD7890</td>
<td>125 k samples</td>
<td>Eight single-ended channels, serial, power-down, T/H, reference</td>
<td>50</td>
<td>24</td>
<td>$10.20</td>
</tr>
<tr>
<td></td>
<td>AD7853</td>
<td>200 k samples</td>
<td>3 to 5 V operation, serial, pseudo-differential inputs (7853), four pseudo-differential inputs (7858), power-down</td>
<td>18 (V_{ref}=3V)</td>
<td>24</td>
<td>$8</td>
</tr>
<tr>
<td></td>
<td>AD7891</td>
<td>500 k samples</td>
<td>5 V supply, T/H, 25 ppm reference, eight channels (7891), parallel and serial</td>
<td>75</td>
<td>44</td>
<td>$16.15</td>
</tr>
<tr>
<td></td>
<td>AD7892</td>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>$13.60</td>
</tr>
<tr>
<td>Burr-Brown Circle No. 302</td>
<td>ADS7806</td>
<td>40 k samples</td>
<td>Parallel and serial, power-down, 0 to 4 to ±10 V input ranges, 5 V supply</td>
<td>35</td>
<td>24</td>
<td>$9.25</td>
</tr>
<tr>
<td></td>
<td>ADS7808</td>
<td>100 k samples</td>
<td>Serial, 0 to 4 to ±10 V input ranges, 5 V supply</td>
<td>100</td>
<td>20</td>
<td>$9.25</td>
</tr>
<tr>
<td></td>
<td>ADS7810</td>
<td>800 k samples</td>
<td>Parallel data with latches, ±10 V input range, S/H, clock, reference, ±5 V supply</td>
<td>250</td>
<td>28</td>
<td>$26.50</td>
</tr>
<tr>
<td>Crystal Semiconductor Circle No. 304</td>
<td>CS5030</td>
<td>500 k samples</td>
<td>Reference (1 ppm 5030 and 5031; 60 ppm 5032), ±5 V supply, input ranges of ±2.5 (5030 and 5032) or 0 to 5 (5031); flexible serial, parallel, and byte interface</td>
<td>70</td>
<td>24</td>
<td>$18.50</td>
</tr>
<tr>
<td></td>
<td>CS5031</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$18.50</td>
</tr>
<tr>
<td></td>
<td>CS5032</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$15.90</td>
</tr>
<tr>
<td>Harris Semiconductor Circle No. 306</td>
<td>Hi5810</td>
<td>100 k samples</td>
<td>5 or 3.3 V (5813) supplies, S/H, parallel</td>
<td>42</td>
<td>24</td>
<td>$7.30</td>
</tr>
<tr>
<td></td>
<td>Hi5812</td>
<td>50 k samples</td>
<td></td>
<td>10 (typ)</td>
<td>16</td>
<td>$6.95</td>
</tr>
<tr>
<td></td>
<td>Hi5813</td>
<td>40 k samples</td>
<td></td>
<td>9</td>
<td></td>
<td>$8.41</td>
</tr>
<tr>
<td>Linear Technology Circle No. 307</td>
<td>LTC1286/98</td>
<td>12.5 k samples</td>
<td>2.7 to 9 V supplies, S/H, 2-channel multiplexer or differential inputs, serial</td>
<td>0.5/1.2</td>
<td>8</td>
<td>$4.65</td>
</tr>
<tr>
<td></td>
<td>LTC1273</td>
<td>300 k samples</td>
<td>5 or ±5 V supplies, S/H, 25 ppm reference, clock, parallel, inputs of ±2.5 (1275), 0 to 5 (1273), and ±5 V (1276)</td>
<td>75 (typ)</td>
<td>24</td>
<td>$14.09</td>
</tr>
<tr>
<td></td>
<td>LTC1275</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$12.65</td>
</tr>
<tr>
<td></td>
<td>LTC1276</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$13.20</td>
</tr>
<tr>
<td></td>
<td>LTC1278</td>
<td>500 k samples</td>
<td>5 or ±5 V supply, 5-mW power-down with instant wake-up, S/H, reference, clock, parallel</td>
<td>75</td>
<td>24</td>
<td>$14.35</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$17</td>
</tr>
<tr>
<td>Maxim Integrated Products Circle No. 308</td>
<td>MAX186</td>
<td>133 k samples</td>
<td>Eight input channels, reference, (186), 5 or ±5 V supplies, power-down, serial</td>
<td>12.75</td>
<td>20</td>
<td>$8.95</td>
</tr>
<tr>
<td></td>
<td>MAX188</td>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>$8.45</td>
</tr>
<tr>
<td></td>
<td>MAX120</td>
<td>500 k samples</td>
<td>5 and 15 V supplies, T/H, 25 to 40-ppm references, ±5 V input range, parallel (120 and 122), serial (176)</td>
<td>315</td>
<td>24</td>
<td>$16</td>
</tr>
<tr>
<td></td>
<td>MAX122</td>
<td>333 k samples</td>
<td></td>
<td>315</td>
<td>24</td>
<td>$12</td>
</tr>
<tr>
<td></td>
<td>MAX176</td>
<td>250 k samples</td>
<td></td>
<td>172</td>
<td>8 or 16</td>
<td>$13.20</td>
</tr>
</tbody>
</table>
packages a number of its converters in shrink SOICs.

SAR architecture rules

The SAR architecture still dominates in this 10-KHz to 2-MHz frequency range. However, these SAR converters come in two implementations: those that implement the conversion using an R-2R ladder network and those that use switched-capacitor structures. Texas Instruments uses a patent-pending switched-capacitor SAR architecture to enable the TLC2543 to achieve 12 bits with a small die size (and thus the $5.25 price). The converter also uses a fuse-blown technique, which prevents the need for expensive laser trimming.

Whether a converter is based on an R-2R or switched-capacitor structure doesn't change the way you communicate with and use the ADC. However, these structures, along with whether the converter uses BiCMOS or CMOS technology, do change power consumption, input range, and performance of internal references.

For example, those ADCs striving to achieve the lowest possible power consumption generally have a CMOS, switched-capacitor architecture. In general, these ADCs' internal references aren't as accurate as R-2R or switched-capacitor types built on bipolar or BiCMOS processes. Some companies use BiCMOS processes because they allow IC designers to build better references. ADCs built on BiCMOS processes, such as the AD7892/1, LTC1273/5/6, and MAX120/122, feature internal references with precision characteristics of 25 ppm/°C compared with 50 to 60 ppm/°C for other internal references.

But it doesn't always take a BiCMOS process to produce accurate reference performance. Crystal Semiconductor set out to produce a 12-bit SAR converter with absolute accuracy, including the drift characteristics of the reference. The company uses EEPROM-based calibration circuitry in the CMOS CS5030 and 31 to produce a 2.5V on-chip reference with an extremely low temperature coefficient of 1 ppm/°C reference. The designers also brought the reference to an output pin, so you can use the reference for the rest of the system.

As these converters' sampling rates approach 1 MHz, other architectures start appearing, such as the 2-step conversion methods common to high-speed hybrid ADCs. Both National Semiconductor's and Micro Linear's 1-MHz devices use this method. Soon, some 200-kHz oversampling converters will also debut. (See box, "Oversampling converters quietly creep up in sampling rate."")

Differentiating features

The group of low-cost 12-bit ADCs often have competitive dc and ac specifications, including differential nonlinearity specs around ±1 LSB with no missing codes. (However, some converters' differential nonlinearity can be as high as ±4 LSBs.) Integral nonlinearity can vary from 1 to 2.5 LSB, and minimum S/N-ratio-plus-distortion (SINAD) specs can be as high as 72 dB with −80-dB THD.

### Table 1—Representative Low-Cost 12-Bit ADCs (continued)

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part no.</th>
<th>Speed</th>
<th>Key features</th>
<th>Power (mW max)</th>
<th>No. of pins</th>
<th>Price (1000)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro Linear</td>
<td>ML2230</td>
<td>31.5 µsec</td>
<td>µP compatible, 12-bit plus-sign ADC, S/H, ±5V supplies</td>
<td>400</td>
<td>24</td>
<td>$7.65</td>
</tr>
<tr>
<td>Micro Power Systems</td>
<td>MP3275</td>
<td>15 µsec</td>
<td>16 channels, 50V overvoltage protection, serial (3276) and parallel</td>
<td>200</td>
<td>68</td>
<td>$24.09</td>
</tr>
<tr>
<td>Circle No. 309</td>
<td>MP3276</td>
<td>15 µsec</td>
<td>S/H, 5V supply, parallel (7091) or serial (7092), T/H</td>
<td>200</td>
<td>28</td>
<td>$24.68</td>
</tr>
<tr>
<td>Circle No. 310</td>
<td>MP8790</td>
<td>2000 k samples</td>
<td>T/H, 5V supply</td>
<td>225</td>
<td>52</td>
<td>$25.58</td>
</tr>
<tr>
<td>National</td>
<td>ADC120L030/73</td>
<td>12000 k samples</td>
<td>8-channel multiplexer, S/H, low-power T/H, 5V supply, parallel</td>
<td>15</td>
<td>16 to 28</td>
<td>$11.90</td>
</tr>
<tr>
<td>Semiconductor</td>
<td>ADC12062</td>
<td>1500 k samples</td>
<td>12-bit plus-sign, self-calibrating, 3.3V operation, T/H, 2-, 4-, and 8-channel multiplexers</td>
<td>75</td>
<td>44</td>
<td>$25.50</td>
</tr>
<tr>
<td>Circle No. 311</td>
<td>ADC12662</td>
<td>140 k samples</td>
<td>2-channel multiplexer, S/H, low-power T/H, 5V supply, parallel</td>
<td>200</td>
<td>34</td>
<td>$29.30</td>
</tr>
<tr>
<td>LM12434/38</td>
<td>ADC12062</td>
<td>1500 k samples</td>
<td>12-bit plus-sign system with serial I/O and self-calibration, S/H, RAM, 8-channel multiplexer, FIFO buffer, 3 to 5V supply</td>
<td>34</td>
<td>28</td>
<td>$18.90</td>
</tr>
<tr>
<td>Sipex</td>
<td>SP8480</td>
<td>100 k samples</td>
<td>Eight input channels, parallel, S/H, reference 5V supply, bipolar (85xx) and unipolar (86xx), reference, S/H, parallel, clock</td>
<td>200</td>
<td>28</td>
<td>$13</td>
</tr>
<tr>
<td>Circle No. 313</td>
<td>SP8481</td>
<td>333/200/100 k samples</td>
<td>Serial, 5V supply, S/H, clock, 11 input channels, power-down, built-in self-test</td>
<td>125</td>
<td>24</td>
<td>$14</td>
</tr>
<tr>
<td>Texas Instruments</td>
<td>TLC2543</td>
<td>10 µsec</td>
<td>Serial, 5V supply, S/H, clock, 11 input channels, power-down, built-in self-test</td>
<td>12.5</td>
<td>20</td>
<td>$5.25</td>
</tr>
</tbody>
</table>
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12-BIT ADCs

The issue of absolute accuracy can be bothersome to system designers who are used to using 8- or 10-bit converters in the 100-kHz to 1-MHz range. These lower-resolution converters, including the reference, generally have no trouble meeting a ±1- or ±2-LSB overall accuracy spec.

However, the same isn't true for 12-bit converters and systems. These ADCs' total unadjusted error (TUE)—the sum of integral- and differential-linearity, offset, and full-scale errors—covers a wide range. TUE can be as low as 1 LSB (as it is for Crystal Semiconductor's CS5030/31 with the 1-ppm reference) and as high as around 20 LSBs, roughly equivalent to an accuracy somewhat less than 8 bits (2N=20 LSBs, where N is the number of bits equivalent to the TUE in LSBs. In this case, N=4.3, so overall accuracy is 12-4.3=7.7 bits). So, many of these ADCs approach 12-bit accuracy only with a system calibration.

Although system calibration is common, reasonable accuracy without calibration is sometimes desirable. For example, to detect voltage drop-off, a battery-voltage monitor may require a resolution of 8 bits, but not quite 12. This means that you can buy an 8-bit converter and calibrate or buy a 12-bit converter with a fairly good TUE. The industrial and commercial grades of Harris Semiconductor's 3.3V H15813 for example, have respective TUEs of 9 and 13 LSBs, which both equate to around 9 bits of accuracy.

The wide variety of available low-cost 12-bit converters removes many barriers to upgrading to 12 bits. However, finding the right converter with a

A list of 12-bit converters with speeds exceeding 100 kHz doesn't normally include any oversampling ADCs (also known as delta-sigma and sigma-delta converters). Since their appearance as the latest ADC architecture, oversampling converters have assumed roles in very low-frequency and audio niches. However, companies are working on higher-than-audio-speed oversampling converters and two—one 12- and one 16-bit device—will shortly be available. Crystal Semiconductor also has some high-speed oversampling ADCs in the design phase. These converters will provide communications systems and others with the advantages of the oversampling architecture: a simple antialiasing filter and a low cost.

Analog Devices' 12-bit AD7721 (around $15) has a 210-kHz input bandwidth. The output word rate is 468.75 kHz, and the sampling rate is 30 MHz (set by a nominal 15-MHz external clock). The ADC features an internal reference, operates from 5V supplies, and accepts a differential input of 0 to 2.5V or ±1.25V. As with other oversampling converters, the on-chip filtering reduces the external antialiasing requirements to first order in most cases.

National Semiconductor's ADC-16071/471 ($19.90 (100)) is a 16-bit ADC with a 192k-sample/sec throughput with 64 times oversampling of 24.576 MHz. (The company presented this part at this year's International Solid State Circuits Conference.) This IC also features a 2V reference and, operating on a single 5V supply, consumes 375 mW max (1 mW max in standby mode). S/N ratio is 94 dB, and THD is 0.0015% at 1 kHz.

For free information on the ADCs discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.
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12-BIT ADCs

low price is just a start; many additional factors determine the success of an upgrade. The ADC itself may not be the limiting factor. Remember that users of 10-bit systems expect them to be four times more accurate than 8-bit systems and 12-bit systems to be four times more accurate than 10-bit systems. These expectations have ramifications, some of which go far beyond the converter itself.

An increase in system resolution

LOOKING AHEAD: ABOVE AND BEYOND 12-BIT, 10-MSEC ADCs

The future goal of most 12-bit ADC manufacturers is to increase the speed of their low-cost devices. By year-end, Linear Technology hopes to introduce a 12-bit, greater-than-1M-sample/sec converter; the company is currently evaluating the first silicon for this product. Micro Power Systems is designing devices in the 4- and 5-MHz range.

Numerous 12-bit higher-speed monolithic and hybrid ADCs exist, but they cost significantly more than the devices this article details. Although hybrid ADCs once dominated this high-speed arena, more ICs are beginning to appear. For example, Analog Devices recently introduced the monolithic 5-MHz, 12-bit AD871 ($95), and Harris Semiconductor is working on a lower-power version of its 1W, 12-bit, 3-MHz H138500 ($85). Also, by the end of this summer, Comlinear Corp will introduce a monolithic 12-bit converter, the CLC950, capable of taking 25M samples/sec ($185 (100)). Signal Processing Technologies also plans to announce a 12-bit, 20-MHz CMOS ADC by the end of the summer. This ADC will join the company’s line of bipolar 12-bit ADCs, the 10-MHz SPT7920, 20-MHz 7921, and 30-MHz 7922 ($99 to $161 (1000)).

Hybrid manufacturers include Datel and Comlinear. Datel will soon announce the 10-MHz ADS-119 ($336) and is releasing a new design for the 5-MHz ADS-118 ($238 to $262), a spin-off of the ADS-119 design. After the release of the ADS-119, Datel’s 12-bit ADS family will comprise five converters covering a 500-kHz to 10-MHz frequency range. Comlinear’s CLC925 and 93X family covers a higher range of 10 to 30 MHz, with prices around $450 to $500.

In other future developments in low-cost 12-bit ADCs, BurrBrown will continue to expand its ADS family by introducing versions covering 0 to 5, ±2.5, and ±3.3V input ranges; more serial-output devices in 20-pin packages; and the company’s first multichannel devices. TI will soon introduce a 3.3V version of the TLC2543 and other 12-bit ADCs for cellular phones.

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12-BIT ADCs

requires a reevaluation of signal-conditioning circuits, particularly the drive amplifier. Every 1-bit jump in resolution constitutes a 6-dB increase in S/N ratio. A 12-dB jump from 10 to 12 bits means 12 dB more visibility to potential limitations of driving circuits, such as noise and distortion.

If a drive amplifier's distortion is extremely low before a resolution upgrade, the amplifier probably won't limit the performance of the new ADC. However, a design using the cheapest signal conditioning possible to accommodate an 8- or 10-bit system may show its limitations at 12 bits. Unfortunately, an ultra-low-distortion op amp costs much more than a medium-distortion op amp.

Amplifier distortion and noise aren't the only accuracy limitations. Another source of noise and interference is poor pc-board layout, including improper grounding, bypassing, and coupling of digital and analog signals. The bad effects of poor circuit layout rise dramatically when you upgrade a system from 10 to 12 bits. But, if the initial board design is based on a good layout, you may not need to change it. Good layout practices generally include keeping analog and digital signals separate to minimize coupling between the digital and analog sides.

An even more drastic measure may be to reevaluate the effects of a switching power supply on the analog circuits. Switching-power-supply designs are using higher and higher switching frequencies, and these higher frequencies can affect the accuracy of an analog system. You may have to consider how the quality of the power-supply voltage affects the ADC.

When switching from using a µP's internal ADC to using an external one, be aware of what may happen when you join the ADC and the µP. Despite the fact that the ADC may have 3-state output drivers, you can't expect a 12-bit accurate ADC to produce a 12-bit answer if its outputs are directly tied to some noisy system bus that also carries 10-, 20-, or 30-MHz signals. Consider using digital buffers between the ADC and the µP.

Moving up to 16 bits

These system-design problems become even worse if you upgrade beyond 12 bits. At 16 bits, the drive amplifiers' settling time and full-power bandwidth become extremely important, along with the dynamic loading effects of the ADC's input. Even with low-frequency signals of 1 to 3 kHz, distortion that doesn't show up at 12 bits does show up at 16 bits. Certain trade-offs are mandatory at the 16-bit level; it's important to consider whether the application requires the absolute minimum of noise or distortion and how much minimizing of those two parameters the design can afford.

You can reach Technical Editor Anne Watson Swager at (215) 645-0544.

Article Interest Quotient (Circle One)

High 598 Medium 599 Low 600

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A Generation Ahead.
As system complexity grows, ESDA tool vendors try to convince you they can solve your design problems with a new class of tools. Maybe they can.

Not content with “EDA” for “electronic-design automation,” trade-publication editors have conspired with EDA-tool marketers to create “ESDA” for “electronic-system-design-automation,” the newest in a never-ending stream of acronyms. Your job as a designer isn’t to understand what ESDA means. That’s backward. Instead, the ESDA vendors should understand what designers need. However, you do need to understand which ESDA tools and design methods might help improve your effectiveness as a designer.

You can best understand what you need from ESDA tools by focusing on a methodology that best fits the type of work you do. In the quick-paced world of electronics, rethinking your design methodology every few years is inadequate; the process must be ongoing. You must constantly hone your methodologies. After each design, evaluate the tools and methods you’ve been using to see what works, what doesn’t, and what you need to fix.

Furthermore, the perfect methodology for one company may very well drive another company out of business. For example, a test-equipment vendor with relatively uncomplicated systems but with extremely tight timing requirements may
BEGIN
next_state <= state;
CASE STATE IN
WHEN waiting =>
    IF ( start_write="1"
      next_state <= writing_to
    ELSIF ( start_read="1" ) THEN
        next_state <= reading_from
    ELSE
        ...
END CASE
}
Electronic-system-design automation

still find that the best design method uses gate-level schematics and simulation. A company designing DSP systems may find system-level functionality a greater problem than is timing. That company may adopt a top-down design methodology using system-design tools, a hardware-description language (HDL), logic synthesis, and simulation, and the company may never descend to the gate level except to generate a netlist for device fabrication.

Every new-ESDA-product presentation starts by showing how time to market is your No. 1 enemy. Although reducing time to market is often vital, you must also understand the factors affecting time to market for your company's products—and whether the ESDA tool and any new methodology in question will help.

The first thing you need to do is evaluate where your company spends time in design work. (See box, "Where does the time go in your design group?") Your organization may suffer from some of the problems the box mentions or have problems unique to the type of systems your company designs. In either case, the first step toward improving your design tools or methodology is to identify the problem. Once you do that, you can look for tools to solve the problem.

Large, complex system designs generally cause—or at least magnify—the problems that so-called ESDA tools aim to solve. However, the term “ESDA” is much too general to tell you anything useful about a tool. For example, one ESDA tool may be strictly for graphical-design entry and have no simulation capability at all. Another may be for digital simulation of large systems; another, for analog simulation. But one of these tools may answer some of the needs of your design organization. Table 1 (see pg 88) provides a representative listing of “ESDA tools,” although not every manufacturer calls them ESDA tools.

Top-down design

A concept common to most ESDA tools is the use of top-down design. Although some tools can support both top-down and bottom-up design methods, most designers favor top-down design for using ESDA tools. You don’t need ESDA tools to adopt a top-down design approach; however, most ESDA tools (and EDA tools in general) help you follow such an approach.

“Top down” means you start with a set of system-level requirements and develop high-level system block diagrams or a high-level architecture. After verifying that the architecture satisfies the system requirements, you treat each block as a subsystem and develop the architecture of each subsystem. You continue in this manner until you complete the specification of a design in whatever detail is necessary and verify compliance to the specification.

The top-down approach to system design doesn’t just sound clean and logical. It is clean and logical, and it’s the approach that most designers adopt when possible. The top-down approach implies the separation of system design and implementation. First, you need to design the right system; then, you must correctly implement it. The point between the design and implementation phases is where some tool vendors draw the line distinguishing EDA and ESDA tools. They claim that ESDA tools help you design the right system and that EDA tools help you design the system right. However, the distinction doesn’t hold up under close scrutiny because many tools are useful for both system design and implementation.

The distinction between the system-level design phase and the implementation phase is, however, a useful one. During system-level design, you determine the behavior of the system and high-level system architecture. Once you create and verify a satisfactory high-level architecture, you can proceed to implementation, during which you flesh out the details.

Sometimes, you need to mix bottom-up and top-down design approaches. The bottom-up approach is often necessary for designs built on a specific device or technology. For example, if you build a data-acquisition system around a high-speed A/D converter, a bottom-up design surrounds the converter, but you can design the remainder of the system using a top-down approach.

Many designers believe that a design starts with a set of requirements, but that simply isn’t true. A design usually starts with a need, a vision, or a little of both. For example, a designer might see a problem that an electronic system can solve or see a way to improve an existing system. Another designer might envision a completely new system. From
Top Ten Reasons for Using MaxRoute II

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10. Quality – MaxRoute II will complete your design with a substantially lower via count and a lower total trace length than any other router. Quality routing = time well spent.

9. Platform Flexibility – MaxRoute II is a 32-bit Windows and Windows NT application offering you access to today's hottest RISC platforms. The speed is incredible!

8. Control – MaxRoute II's Interactive and manual routing give you the most productive routing tools in the industry bar none! Toggle between fully manual and interactive tools, without ever releasing your trace, to create the most productive union of expert designer and software possible.

7. More Control – “Fast Route” - flies through your design for quick feedback about your placement quality. “Manual Place” - lets you change your component placement in MaxRoute II and accurately back annotate your host PCB package. You do not need to leave MaxRoute II until your design is complete. “Strategy Files” - easily preset all of your critical routing criteria. MaxRoute II is designed work with your design expertise.

6. Speed – MaxRoute II is the new breed of Massteck router. In a recent benchmark MaxRoute II for Windows NT completed a 6,000 connection, 488 component, 4 routing layer SMT board in under 7 hours with 31% fewer vias than than the Unix “shape based” competitor that chugged along for over 25 hours.

5. Completion – Every good designer will edit an autorouted design to give it their “touch”. MaxRoute II works so intelligently there is always room on the board for those final edits or changes.

4. Support – Massteck offers technical support second to none. Whatever your level of question Massteck's dedicated support staff has the answer you need, when you need it!

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*In 1987 MaxRoute was the first PCB application developed for Windows™
Electronic-system-design automation

these needs and visions, designers create system requirements or a specification.

The translation of a need or a vision into system requirements is the first risk of introducing an error—either an outright error or simply the omission of a detail—into a system design. This translation is also often the reason for system specifications to keep changing during a design. It’s difficult to reach the finish line fast if you start by designing a system based on an incorrect specification, and more diligence does not necessarily solve the problem. Designers cannot typically eliminate all errors in a design before simulation, so they shouldn’t expect a person or an organization to create an error-free specification for a complex system without first testing it against a working prototype or a simulation.

A corollary assumption of the top-down design approach is that the earlier you find and correct errors, the more time and money you save. For example, finding an error in postlayout simulation of an ASIC is better than finding it after fabrication. Finding the error in prelayout simulation is even better. Finding an error at the architectural or system-requirements stage is better still.

As system complexity increases, the possibility of creating an error-free design without simulation or prototypes becomes more remote. ESDA tools for simulation offer some help by allowing you to create a system simulation early and giving you a means to test the system architecture, functional operation, and system specification against the original concept.

In theory, any simulator can help with system simulation, provided that it covers the domains in which you work, such

WHERE DOES THE TIME GO IN YOUR DESIGN GROUP?

Before you can fix a problem, you have to know what the problem is. The first step toward improving your design process is to identify the problems that eat design time in your organization. The following scenarios illustrate situations you might consider when evaluating your company’s design methodology and possible ways to improve it:

Problem: My company has to design systems several times because the requirements keep changing.

Solution: Nail down the requirements earlier. Design engineers often feel helpless and frustrated about this problem because another department, such as product marketing, or even another company is causing those changing requirements. If the end result is that projects move slowly through your design organization because you have to design a complete system multiple times, you can and should do something about it.

Electronic-system-design-automation (ESDA) tools can help by showing you the implications of a design’s requirements earlier. You create a system simulation and show it to a customer, get feedback, and make changes to the requirements earlier in the design cycle. System simulation doesn’t keep requirements from changing but may let you zero in on the final set of requirements before you invest a lot of detailed design work implementing a design.

Problem: My organization knows what it wants to build (the system requirements don’t change), and the design works when we build it, but we redesign it several times to reduce the cost or optimize the performance.

Solution: System-level design tools can help with the optimization stage, too, by providing a simulation of the system and evaluating its performance. Exploring alternative designs isn’t a mistake; it’s part of the design process. Sometimes, simple calculations or intuition can help you weed out unworthy design alternatives. Simulation provides even better insight into a design and how it performs, helping you decide which alternatives are worth pursuing. The earlier you weed out unworthy architectural alternatives and pursue winners, the more time you save.

Problem: My company knows what it is trying to build (the system requirements don’t change), but the design doesn’t work the first time—or the second.

Solution: Sometimes, you miss the bull’s eye, but if you miss by a lot or if you miss every time, there may be a problem you can correct. If you aren’t simulating at all, then that’s the problem. If you are simulating, then you probably aren’t performing the exhaustive verification that the design requires. Implementation-level problems aren’t typically a strength for ESDA tools; however, you can often uncover functional design problems with system-level simulation. If your problems are in timing, ESDA tools will not help.

Problem: The design works when we finally get it done, and we don’t go through a lot of design iterations. It just takes a long time.

Solution: Determine in greater detail where all the time is going. You may need tools that streamline some time-consuming parts of your design process, or you may need a new design methodology. If you are still creating digital designs at the gate level, you might consider moving to a hardware-description language (HDL). If the thought of text-based design leaves you cold, consider one of the many ESDA tools that provides graphical-design entry.

Graphical-design tools let you connect high-level blocks in a diagram, much like a schematic. Each block performs a general class of functions, such as adding or counting. You fill in a parameter table to specify the exact function, how many bits wide, and other specifications. From this graphical block-level design, many of the ESDA tools generate VHDL or Verilog code for input to logic-synthesis tools. Using these tools lets you avoid learning an HDL or at least lets you learn them at your own pace while completing designs in a timely manner.

If your design cycle takes too long because you spend too much time simulating to eliminate all the bugs, you may have a simulation-speed problem. Some ESDA tools provide cycle-based simulators that are 100 to 1000 times faster than ordinary logic simulators; these cycle-based simulators find functional design problems.

If your simulation problems are in timing, ESDA tools probably won’t help. Instead, look for fast simulators or hardware accelerators.
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Electronic-system-design automation

as analog, digital, mixed signal, or mechanical. In practice, an effective system simulator must be fast enough to run the simulation at an acceptable speed and have sufficient capacity for your system design. The simulator should also provide the information you need in a format that makes it easy to understand and evaluate a system's operation.

For most systems, behavioral-level models and cycle-based simulators can provide the required speed. Gate-level digital simulators and transistor-level analog simulators often cannot. Many companies use behavioral-level models in VHDL, Verilog, C, Spice, and proprietary languages.

Cycle-based simulators find functional design problems in synchronous systems. These simulators involve a tradeoff, however, because they sacrifice timing information for simulation speed in hunting down functional design problems. Cycle-based simulators are best suited to a divide-and-conquer approach of system design. First, you create and debug the functional design; then, you solve timing problems. For some systems, timing is the heart of the system, and trying to separate it from functional design is pointless.

How a simulator presents information is also an important selection criterion. Most logic simulators offer a waveform display for examining logic problems, but such a display is relatively inefficient for identifying system-level problems. You may need to show a system simulation to a customer who is not an electronic design engineer. With an easily understood format, such a customer can more likely find system problems in simulation instead of in the finished product.

Most ESDA simulators provide simulation results in a graphical format. Some tools, such as Redwood Design Automation’s Race Simulator and Reveal Interactor, Mentor Graphics’ System Design Architect, and I-Logix’s Statemate family let you tailor a system’s simulation output to almost any type of graphic display. These tools let you create a virtual-prototype system and test it against the specification and the original concept before investing the time in a full design implementation. These tools not only help you explore architectural approaches, but also let all members of the design work from a common vision of the finished system.

Implementing the design

Once you develop what appears an acceptable system architecture, you can move to the implementation phase. Most—but not all—graphical-ESDA tools are part of an implementation path. Conversion of graphical design information into a synthesizable description is the reason many of these tools exist. With these tools, you provide a graphical block or state diagram, and the tool translates it into synthesizable code, usually VHDL or Verilog.

Because logic-synthesis tools differ, graphical-design tools often develop code differently for each logic-synthesis tool. You should verify that any combination of design and synthesis tools you are considering using generates high-quality code.

Some high-level ESDA-simulation tools don’t provide an implementation path through logic synthesis. These tools may be effective architectural tools to help verify that you are designing the right system, but they force you to create the physical design description separately.

Even before ESDA tools were in fashion, some designers created behavioral-level HDL models of systems for simulation and architectural verification and then created a register-transfer-level (RTL) description to implement the design. Because you cannot synthesize behavioral-level HDL designs, except for very low-level designs, this approach also leaves you without a direct implementation path. It does, however, let you insert your RTL-logic blocks into the full system design for simulation as you transform the architectural design into an implementation.

If your goal is to work at a higher level and design more gates in a short time, consider using macros or building blocks having high gate counts to perform the functions you need. For example, Synopsys’ DesignWare and Intergraph’s MacroSyn include libraries of parameterized logic blocks that implement efficiently in synthesis.

Every component in Synopsys’ ALU family has multiple architectures for each function. You can optimize these architectures for either performance or area to meet your design goals. If you find the building blocks you need, this design approach should raise your design efficiency.

A variation on the design-efficiency theme is design reuse. Salvaging parts of a design from a previous system and reusing them with relatively minor variations saves considerable time over generating them from scratch. In designs requiring greater variations, you can use Synopsys’ DesignWare Developer, which lets you develop your own parameterized modules. The attraction of this approach is that you can implement the modules you need in the way you want. The disadvantage is that you invest time in creating the modules. If you will use the modules frequently, however, this time investment is probably justified.
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### Electronic-System-Design Automation Tools

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>Description</th>
<th>Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anacad EES</td>
<td>HDL-A</td>
<td>VHDL-based analog behavioral modeling system for use with the company's Eldo simulator; models analog and mixed-signal systems, including electrical, mechanical, fluid, rotational, magnetic, thermal</td>
<td>VHDL and proprietary HDL-A language</td>
</tr>
<tr>
<td>Analogy Inc</td>
<td>Saber</td>
<td>Analog and mixed-signal simulation; works with logic simulators; model libraries and templates available for many applications</td>
<td>Spice models and proprietary modeling language (MAST)</td>
</tr>
<tr>
<td>CADIS Software</td>
<td>Cossap</td>
<td>Integrated tool for the design, simulation, and implementation of digital-processing and communication systems</td>
<td>Graphical block diagrams</td>
</tr>
<tr>
<td>Comdisco Systems Inc</td>
<td>System Design Architect</td>
<td>System-level design for ASICs, field-programmable gate arrays, and microcoded processors using a parameterized library of synthesizable blocks</td>
<td>Graphical function blocks, VHDL, C</td>
</tr>
<tr>
<td>Compass Design Automation</td>
<td>ASIC Navigator</td>
<td>Top-down ASIC design system with application to general-purpose design, DSP, image processing, and communication</td>
<td>Block diagrams for data path, state machines, memory templates, VHDL, Verilog, gate-level schematics, Boolean equations, and truth tables</td>
</tr>
<tr>
<td>Elanix Inc</td>
<td>SystemView</td>
<td>Dynamic system simulator for conceptual design and evaluation of analog and digital designs; emphasis on signal processing, communications, control systems, and general mathematical modeling</td>
<td>Graphical block diagrams and graphical templates</td>
</tr>
<tr>
<td>HP-EESof</td>
<td>OmniSys</td>
<td>System simulator for evaluating topologies of communication systems; analyzes complex waveforms in systems based on arbitrary topologies and modulation schemes</td>
<td>Graphical block diagrams</td>
</tr>
<tr>
<td>Hyperception</td>
<td>Hypersignal for Windows</td>
<td>Graphically develops and simulates DSP and communication systems; generates source code for porting designs to other platforms or cross-compiled for specific DSP chips</td>
<td>Graphical block diagrams</td>
</tr>
<tr>
<td>i-Logix Inc</td>
<td>Statemate 5.0</td>
<td>Requirements traceability, graphical design, simulation, analysis, and code generation; hardware/software co-design</td>
<td>Architectural block diagrams, behavioral state charts, C</td>
</tr>
<tr>
<td>Intergraph</td>
<td>MacroSyn Design Expressions</td>
<td>Provides template-driven creation of synthesizable macros; Design description allows entering of designs using truth tables, state tables, Boolean equations, VHDL, and Diablo for design descriptions</td>
<td>Graphical symbols and templates, Truth tables, state tables, Boolean equations, VHDL, Diablo for analog behavioral descriptions</td>
</tr>
<tr>
<td>Knowledge Based Silicon Inc</td>
<td>FlowHDL</td>
<td>Creates system descriptions as a collection of hierarchically partitioned concurrent flow-diagram threads for general-purpose design</td>
<td>Graphical and textual design entry for state-machine, data-path clocking, memory, synchronous, and asynchronous, and resolution functions VHDL, Verilog, block diagrams</td>
</tr>
<tr>
<td>Mentor Graphics</td>
<td>System Design Station</td>
<td>Top-down system design from requirements through graphical or textual design to verification and implementation of general-purpose and DSP designs; VHDL-code generation</td>
<td>Graphical state and data-flow diagrams, state-transition matrix and table editor, VHDL</td>
</tr>
</tbody>
</table>

*May 26, 1994*
<table>
<thead>
<tr>
<th>Outputs</th>
<th>Simulation</th>
<th>Provides an implementation path</th>
<th>Computer required</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Models compatible with the Eldo simulator</td>
<td>Mixed signal; also works with most logic</td>
<td>Simulation only</td>
<td>Workstation</td>
<td>HDL-A development system: $30,000,</td>
</tr>
<tr>
<td></td>
<td>simulators for large VDHL descriptions</td>
<td></td>
<td></td>
<td>runtime version: $8000, Eldo: $22,000</td>
</tr>
<tr>
<td>Simulation</td>
<td>Analog and mixed signal</td>
<td>Simulation only</td>
<td>Workstation</td>
<td>Starts at $20,000</td>
</tr>
<tr>
<td>VHDL, DSP-executable code</td>
<td>Yes</td>
<td>Yes</td>
<td>Workstation</td>
<td>$30,000</td>
</tr>
<tr>
<td>VHDL, Graphical Waveform</td>
<td>Cycle-based simulator</td>
<td>Yes</td>
<td>Workstation</td>
<td>$5000 plus $25,000 for SPW</td>
</tr>
<tr>
<td>C or assembly code for DSP chips (VHDL optional)</td>
<td>Floating point (fixed point optional)</td>
<td>Yes</td>
<td>Workstation</td>
<td>$25,000</td>
</tr>
<tr>
<td>Complete ASIC and and field-programmable gate-array designs</td>
<td>VHDL and Verilog</td>
<td>Yes</td>
<td>Workstation</td>
<td>$40,000</td>
</tr>
<tr>
<td>Mathematical models</td>
<td>Yes</td>
<td>No</td>
<td>PC/Windows</td>
<td>$985</td>
</tr>
<tr>
<td></td>
<td>Simulation</td>
<td>No</td>
<td>Workstation</td>
<td>$26,000</td>
</tr>
<tr>
<td>C optional</td>
<td>Yes</td>
<td>On path (software)</td>
<td>PC/Windows</td>
<td>$1995, C-code generator: $5000, Advanced</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Transmission library: $1495</td>
</tr>
<tr>
<td>VHDL, Verilog; optional C and Ada code</td>
<td>Yes</td>
<td>Yes</td>
<td>Workstation</td>
<td>$20,000 to $40,000</td>
</tr>
<tr>
<td>VHDL, Verilog</td>
<td>No</td>
<td>Yes</td>
<td>Workstation</td>
<td>$10,000</td>
</tr>
<tr>
<td>VHDL, Verilog, ABEL</td>
<td>No</td>
<td>Yes</td>
<td>Workstation</td>
<td>$8000</td>
</tr>
<tr>
<td>VHDL, Verilog, ABEL</td>
<td>No</td>
<td>Yes</td>
<td>Windows NT, Unix workstations</td>
<td>$3500</td>
</tr>
<tr>
<td>VHDL, Verilog</td>
<td>Cycle-based simulator</td>
<td>Yes</td>
<td>Workstation</td>
<td>$10,000</td>
</tr>
<tr>
<td>VHDL, Verilog</td>
<td>Optional</td>
<td>Yes</td>
<td>Workstation</td>
<td>$2800</td>
</tr>
<tr>
<td>ASIC and field-programmable gate-array libraries; interface to</td>
<td>VHDL, gate-level simulator</td>
<td>Yes</td>
<td>Workstation</td>
<td>$94,900</td>
</tr>
<tr>
<td>computer-aided software engineering, DSP, analog, VHDL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(table continued on pg 90)
## ELECTRONIC-SYSTEM-DESIGN AUTOMATION TOOLS (CONTINUED)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product</th>
<th>Description</th>
<th>Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mentor Graphics</td>
<td>System Architect</td>
<td>Graphical and textual design of systems for DSP and general-purpose applications; state-machine verification and VHDL-code generation</td>
<td>Graphical state and data-flow diagrams, VHDL</td>
</tr>
<tr>
<td>NuThena Systems</td>
<td>Foresight 3.00</td>
<td>Development tool for constructing and analyzing executable system models for embedded and distributed systems</td>
<td>Proprietary modeling language, graphical entry</td>
</tr>
<tr>
<td>R·Active</td>
<td>Better State Pro</td>
<td>Generates C, C++, VHDL, or Verilog from state diagrams</td>
<td>Graphical state diagrams</td>
</tr>
<tr>
<td>Redwood Design Automation</td>
<td>Race Simulator/Reveal Interactor</td>
<td>Cycle-based simulation engine and graphical prototyping tool</td>
<td>VHDL, Verilog, C, C++</td>
</tr>
<tr>
<td>Scientific and Engineering Software Inc</td>
<td>SES/Workbench</td>
<td>Evaluates functionality and performance of architecture before prototyping of computers, complex software systems, large data-communication networks, bus-interfaces, communication protocols, μPs, and ASICs</td>
<td>Graphically models systems with a variety of node types; creates custom nodes in C; Verilog cosimulation optional</td>
</tr>
<tr>
<td>Speed Electronics Inc</td>
<td>SpeedChart</td>
<td>Graphical design tool for generating VHDL and Verilog code</td>
<td>State diagrams, schematics, behavioral code, spreadsheet tables</td>
</tr>
<tr>
<td>Summit Design Inc</td>
<td>Visual HDL</td>
<td>Captures designs using four graphical languages, simulates and outputs designs in VHDL or Verilog</td>
<td>Block diagrams, state diagrams, flow charts, truth tables, VHDL text</td>
</tr>
<tr>
<td>Synopsys</td>
<td>DesignWare</td>
<td>Parameterized, fully synthesizable modules for general-purpose design; allows the addition of custom components to the library</td>
<td>Selects modules, then inputs parameters to customize them for a design</td>
</tr>
<tr>
<td>TD Technologies Inc</td>
<td>Transcend</td>
<td>Design, analysis, and verification tool for complex electronic hardware- and software-systems design</td>
<td>Proprietary- graphical/ textual-language, C++ VHDL, and Verilog submodules</td>
</tr>
<tr>
<td>Tesoft Inc</td>
<td>Tesla</td>
<td>Block-diagram simulator for communication, signal-processing, and control systems</td>
<td>Proprietary-language and graphical-function blocks</td>
</tr>
<tr>
<td>Vantage Analysis Systems</td>
<td>TD Connection/ TD Simulator</td>
<td>Transaction-based simulator allowing analysis of architectural tradeoffs, cosimulation with VHDL designs optional</td>
<td>Proprietary- graphical/textual-language, VHDL submodules</td>
</tr>
<tr>
<td>Viewlogic Systems Inc</td>
<td>ViewState</td>
<td>Graphical VHDL entry tool allowing graphical creation of complex behavioral models; supports hierarchical and concurrent state machines Synthesizes hardware architecture from behavioral VHDL descriptions, producing architectural block diagrams and detailed register-transfer-level design structure ready for logic synthesis</td>
<td>State diagrams Behavioral and register-transfer-level VHDL</td>
</tr>
<tr>
<td>Vista Technologies</td>
<td>Design Vision</td>
<td>Graphically develops HDL models</td>
<td>Graphical entry of control-flow and data-flow diagrams</td>
</tr>
<tr>
<td>Visual Software Solutions Inc</td>
<td>StateCAD</td>
<td>Graphically creates state diagrams and translates them in ABEL or C code</td>
<td>Graphical</td>
</tr>
</tbody>
</table>

**Manufacturer Information:**
- Mentor Graphics: Wilsonville, OR (503) 685-8000 (Circle No. 408)
- NuThena Systems: McLean, VA (703) 356-5056 (Circle No. 409)
- R·Active: Cupertino, CA (408) 252-2808 (Circle No. 410)
- Redwood Design Automation: San Jose, CA (408) 291-3850 (Circle No. 411)
- Scientific and Engineering Software Inc: Austin, TX (512) 328-5544 (Circle No. 412)
- Speed Electronics Inc: Oak Brook, IL (708) 990-1910 (Circle No. 413)
- Summit Design Inc: Beaverton, OR (503) 643-9281 (Circle No. 414)
- Synopsys: Mountain View, CA (415) 962-5000 (Circle No. 415)
- TD Technologies Inc: Cleveland Heights, OH (216) 371-9777 (Circle No. 416)
- Tesoft Inc: Roswell, GA (404) 751-9785 (Circle No. 417)
- Vantage Analysis Systems: Fremont, CA (510) 659-0901 (Circle No. 418)
- Viewlogic Systems Inc: Marlboro, MA (508) 480-0881 (Circle No. 419)
- Vista Technologies: Schaumburg, IL (708) 706-8300 (Circle No. 420)
- Visual Software Solutions Inc: Coral Springs, FL (305) 346-8990 (Circle No. 421)
<table>
<thead>
<tr>
<th>Outputs</th>
<th>Simulation</th>
<th>Provides an implementation path</th>
<th>Computer required</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>VHDL</td>
<td>State-machine animator</td>
<td>Optional synthesis</td>
<td>Workstation</td>
<td>$34,900</td>
</tr>
<tr>
<td>Reports, animated data visualization</td>
<td>Yes</td>
<td>No</td>
<td>Workstation</td>
<td>$25,000</td>
</tr>
<tr>
<td>VHDL, Verilog, C, C++</td>
<td>No</td>
<td>Yes</td>
<td>PC/Windows</td>
<td>$1195</td>
</tr>
<tr>
<td>Simulation</td>
<td>Cycle-based simulation</td>
<td>Simulation only</td>
<td>Workstation</td>
<td>Race/Reveal combined: $65,000</td>
</tr>
<tr>
<td>Simulation</td>
<td>Graphical animation</td>
<td>No</td>
<td>Workstation</td>
<td>SES/Workbench: $37,000, Verilog cosimulation: $6000</td>
</tr>
<tr>
<td>VHDL, Verilog; C optional</td>
<td>Yes</td>
<td>Yes</td>
<td>Workstation</td>
<td>$26,000</td>
</tr>
<tr>
<td>VHDL, Verilog</td>
<td>Yes (presynthesis)</td>
<td>Yes</td>
<td>Workstation, PC/Windows</td>
<td>Unix: $25,000, PC/Windows: $12,500</td>
</tr>
<tr>
<td>VHDL</td>
<td>Optional</td>
<td>Yes</td>
<td>Workstation</td>
<td>Libraries: $5000, developers tools: $45,000</td>
</tr>
<tr>
<td>Simulation</td>
<td>Yes</td>
<td>Yes</td>
<td>Workstation</td>
<td>$35,000</td>
</tr>
<tr>
<td>Graphical and text</td>
<td>Digital and analog</td>
<td>No</td>
<td>PC</td>
<td>$695</td>
</tr>
<tr>
<td>Simulation</td>
<td>Yes</td>
<td>No</td>
<td>Workstation</td>
<td>TD Connection: $12,000, TD Simulator: $35,000</td>
</tr>
<tr>
<td>VHDL</td>
<td>Simulates state transitions</td>
<td>Yes</td>
<td>Workstation</td>
<td>$11,000</td>
</tr>
<tr>
<td>VHDL, hierarchical block diagrams</td>
<td>No</td>
<td>Yes</td>
<td>Workstation</td>
<td>$25,000</td>
</tr>
<tr>
<td>VHDL, Verilog</td>
<td>Compatible with standard VHDL and Verilog simulators</td>
<td>Yes</td>
<td>Workstation</td>
<td>$15,000</td>
</tr>
<tr>
<td>ABEL, C, state diagrams</td>
<td>Functional state simulation</td>
<td>Yes</td>
<td>PC/Windows</td>
<td>$995</td>
</tr>
</tbody>
</table>
At fast edge rates, the wrong interface takes on unexpected qualities.

AMP high-speed connectors - in hard metric, shielded hard metric, Futurebus, stripline, and microstrip versions - offer a broad range of signal management solutions.
As the demand for performance pushes clock rates up, signal integrity can become a real challenge—especially when traffic moves from board to board, or board to cable. Interconnects that worked last time around suddenly act a lot like bumpers and flippers when your signal hits them. Fortunately, expert interconnect help is available.

We’ll show you a broad range of technology solutions—the newest and best of subnanosecond interfaces. We’ll work with you to choose the right combination of performance and features to meet tough circuit requirements. And our experience in design and in manufacturing can help make sure your choice works on the production line, as well.

Our high-speed and controlled-impedance interconnect solutions are engineered for hassle-free implementation, even with edge rates pushing 250ps. Our board-to-board selection includes high-density open pin field types (shielded versions available), plus stripline and microstrip styles that allow you to match characteristic board impedances to minimize crosstalk, reflection, and groundbounce. Our board-to-cable selection includes precision miniature coax and transmission line offerings to maintain signal integrity with minimum propagation delay.

And we offer the simulation tools you need to confirm performance in software, before you build your first prototype. Talk with your AMP Sales Engineer today, or call; we’re ready to help.

AMP is a trademark.
Finally, op amps designed to operate with real world capacitive loads. LTC’s C-Load family of op amps solves the problem of capacitive load induced oscillations. Our C-Load op amps slow down when capacitively loaded, while other op amps oscillate.

Driving coax, twisted pair and other difficult loads take no extra care when C-Load op amps are used. C-Load op amps are stable when driving loads of over 10,000pF, more than most applications require.

Capacitive load driving capability isn’t limited to any one type of amplifier. LTC’s family of C-Load op amps include devices from the 7pA, FET-input LT1457 to the 250mA, 70MHz LT1363.

The LT1206 with its 250mA minimum output current has enough drive to slew 10,000pF at 50V/µs. Precision instrumentation applications? The LTC1152 rail-to-rail input and rail-to-rail output zero drift op amp provides 10µV max offset as well as C-Load driving.

<table>
<thead>
<tr>
<th>Part #</th>
<th>Max $V_{BB}$</th>
<th>Max $I_B$</th>
<th>Min $I_{OUT}$</th>
<th>Bandwidth</th>
<th>Slew Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1097*</td>
<td>60µV</td>
<td>350pA</td>
<td>5.7mA</td>
<td>700kHz</td>
<td>0.2V/µs</td>
</tr>
<tr>
<td>LTC1152</td>
<td>10µV</td>
<td>100pA</td>
<td>4mA</td>
<td>1MHz</td>
<td>1V/µs</td>
</tr>
<tr>
<td>LTC1206</td>
<td>10mV</td>
<td>5pA</td>
<td>250mA</td>
<td>60MHz</td>
<td>900V/µs</td>
</tr>
<tr>
<td>LT1220</td>
<td>1.0mV</td>
<td>300nA</td>
<td>24mA</td>
<td>45MHz</td>
<td>250V/µs</td>
</tr>
<tr>
<td>LT1224*</td>
<td>2.0mV</td>
<td>8µA</td>
<td>24mA</td>
<td>45MHz</td>
<td>400V/µs</td>
</tr>
<tr>
<td>LT1354*</td>
<td>800µV</td>
<td>300nA</td>
<td>30mA</td>
<td>12MHz</td>
<td>400V/µs</td>
</tr>
<tr>
<td>LT1357*</td>
<td>600µV</td>
<td>500nA</td>
<td>30mA</td>
<td>25MHz</td>
<td>600V/µs</td>
</tr>
<tr>
<td>LT1360*</td>
<td>1.0mV</td>
<td>1µA</td>
<td>40mA</td>
<td>50MHz</td>
<td>800V/µs</td>
</tr>
<tr>
<td>LT1363*</td>
<td>1.5mV</td>
<td>2µA</td>
<td>70mA</td>
<td>75MHz</td>
<td>1000V/µs</td>
</tr>
<tr>
<td>LT1457</td>
<td>800µV</td>
<td>75pA</td>
<td>10mA</td>
<td>1.7MHz</td>
<td>4V/µs</td>
</tr>
</tbody>
</table>

*Duals and Quads are available.

Specifications for the table shown are low cost grades in plastic DIP. Prices for our C-Load op amps start as low as $1.05 for the LT1097CN8. For details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035/408-432-1900. For literature only, call 1-800-4-LINEAR.
Low-distortion oscillator starts fast

Mika Maaspuro, Helsinki University of Technology, Espoo, Finland

Unlike a Wien-bridge oscillator, the phase-shift oscillator in Fig 1 starts up quickly. Also, the circuit does not require that you adjust several trimming resistors just to tune the oscillator to a given frequency. Experiments show that the circuit's total harmonic distortion (THD) measures approximately 0.5% or less.

Connecting the output of a bandpass stage to its input via a phase inverter realizes a phase-shift oscillator. In practice, a phase-shift oscillator also needs a limiter stage. Unfortunately, the limiter can distort the output sine wave.

Diodes D1 and D2 in the feedback loop of IC1A form a limiter that does not distort the output. The equation for the circuit is

\[ f_{osc} = \frac{1}{2\pi \sqrt{\frac{1}{2nC R_2 R_1} + \frac{1}{R_3 R_1}}} \]

\[ R_1 \] tunes the frequency of the oscillator.

To have a stable output voltage and minimum distortion, you must set the gain of the loop carefully. The gain needed for oscillation varies slightly with frequency; the circuit needs more gain for lower frequencies. You can leave \[ R_1 \] fixed to a value that yields the lowest frequency.

The circuit can generate a good-quality sine wave at low frequencies. In those cases, the values of capacitors \( C_1 \) and \( C_2 \) may be several microfarads. With such large capacitors, the startup time increases to several hundred milliseconds. You can avoid this delay by connecting diode D3. With D3 in place, startup always takes no more than a few milliseconds. D3 does not distort the characteristics of the circuit because D1 and D2 already limit the output to a few hundred millivolts, peak-to-peak. With D3 connected, the circuit needs a little more gain to develop a stable output.

EDN BBS/ D1 SIG #1423 contains a writeup of this circuit and a comprehensive Spice model. (D1 #1423)

Paralleling rms converters speeds settling

Bernard Courtiol, Cegeloc Soprano, Vaulx Milieu, France

An rms-to-dc converter requires an output lowpass filter, which sometimes leads to overly long settling times. Paralleling two converters reduces the circuit's settling time signal without increasing conversion errors (Fig 1).

The circuit in Fig 1 monitors 50-Hz mains. IC1, IC2, and their associated circuitry compose a phase shifter. The phase shifter has a 90° delay for 50-Hz inputs and constant gain. The second-order, lowpass, state-variable filter, IC3, sums...
and filters the outputs of rms-to-dc converters IC<sub>3</sub> and IC<sub>4</sub>. The circuit’s settling time to 1% of final value is 20 msec. F(p)=0.5/(a<sup>2</sup>p<sup>2</sup>+2kap+l), where k=0.7 and a=0.5 msec. If the circuit were to have only one rms-to-dc converter, its settling time would be 100 msec.

To reduce the circuit’s settling time further, you could parallel more converters, each having a different phase shift. The trick is to set up the phase shifts so as to cancel ripple in the summed signal. (DI #1424)

**To Vote For This Design, Circle No. 425**

Fig 1—Paralleling these two rms-to-dc converters reduces the circuit’s settling time without increasing conversion errors. The op amps shift the phase of one signal so as to cancel ripple in the summed signal.

---

**Circuit protects computer’s input**

Ang Tzu Seng, Halliburton Drilling Systems, Singapore

The circuit in Fig 1 performs input protection, level translation, isolation, and debouncing. The circuit allowed the output of a relay driver to connect to a computer even though the relay driver delivered a voltage as high as 24V and the relay driver had no ground connection.

With the values in Fig 1, the low and high thresholds at the circuit’s input were approximately 8 and 16V, respectively. The cutoff frequency was high enough to allow counting 1200 counts/min. The input withstood 110V ac continuously—the optoisolater’s withstand voltage is 3 kV.

I tested the debouncing function with a microswitch in series with a 24V-dc power supply and the relay driver. I detected no switch bounce.

You can change capacitor C<sub>1</sub> to suit other applications’ cutoff frequencies. Altering the resistors may be tricky because you will affect the circuit’s low- and high-threshold levels. To use inputs other than 24V, change R<sub>1</sub>. (DI #1425)

**To Vote For This Design, Circle No. 426**

---

Fig 1—This circuit performs input protection, level translation, isolation, and debouncing for a computer’s input.
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<table>
<thead>
<tr>
<th>Model</th>
<th>Freq. Range</th>
<th>Gain Min.</th>
<th>Gain Flatness*</th>
<th>Max. Output</th>
<th>NF typ.</th>
<th>Isol. typ.</th>
<th>DC PWR</th>
<th>Price $ ea</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAN-1</td>
<td>0.5-500</td>
<td>28</td>
<td>1.4</td>
<td>8.0</td>
<td>4.5</td>
<td>41</td>
<td>12/60</td>
<td>13.95</td>
</tr>
<tr>
<td>MAN-2</td>
<td>0.5-1000</td>
<td>18</td>
<td>1.5</td>
<td>7.0</td>
<td>6.0</td>
<td>37</td>
<td>12/65</td>
<td>15.95</td>
</tr>
<tr>
<td>MAN-1LN</td>
<td>0.5-500</td>
<td>28</td>
<td>1.4</td>
<td>8.0</td>
<td>2.6</td>
<td>42</td>
<td>12/60</td>
<td>15.95</td>
</tr>
<tr>
<td>^MAN-1HLN</td>
<td>10-500</td>
<td>10</td>
<td>0.8</td>
<td>15.0</td>
<td>3.7</td>
<td>16</td>
<td>12/70</td>
<td>15.95</td>
</tr>
<tr>
<td>MAN-1AD</td>
<td>5-500</td>
<td>16</td>
<td>1.0</td>
<td>6.0</td>
<td>7.2</td>
<td>50</td>
<td>12/65</td>
<td>24.95</td>
</tr>
<tr>
<td>MAN-2AD</td>
<td>2-1000</td>
<td>9</td>
<td>0.7</td>
<td>-2.0</td>
<td>6.5</td>
<td>33</td>
<td>15/22</td>
<td>22.50</td>
</tr>
<tr>
<td>MAN-11AD</td>
<td>2-2000</td>
<td>8</td>
<td>1.5</td>
<td>-3.5</td>
<td>6.5</td>
<td>27</td>
<td>15/22</td>
<td>29.95</td>
</tr>
</tbody>
</table>

* Midband 10f<sub>0</sub> to f<sub>0</sub>/2, +/- 0.5 dB  ** At 1dB compression point  ^ Case height 0.3 inch

CIRCLE NO. 103

Actual Size

P.O Box 350166, Brooklyn, New York 11235-0003  (718) 934-4500  Fax (718)332-4661

For detailed specs on all Mini-Circuits products refer to • THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCTS DIRECTORY • EEM • MINI-CIRCUITS 740- pg. HANDBOOK.

CUSTOM PRODUCT NEEDS...Let Our Experience Work For You.
RS-485 repeater extends standard’s reach
Mitchell Lee, Linear Technology Corp, Milpitas, CA

RS-485 specifies communications for distances up to 4000 ft. This limit is the consequence of losses in the twisted pair used to carry the data. Beyond 4000 ft, skin effect and dielectric losses take their toll, attenuating the signal beyond use.

Fig 1 shows a simple RS-485 repeater. Two RS-485 transceivers connected back-to-back relay incoming data from either side. A pair of cross-coupled one shots control the data flow so that only one transmitter turns on at a time.

A 1-to-0 transition at the output of either idling receiver signifies incoming data. The first receiver to spot such a transition triggers its associated one shot, which, in turn, activates the opposite transmitter to ensure smooth data flow from one side of the repeater to the other. At the same time, the one shot locks out the other receiver/transmitter/one-shot combination, so that only one data path is open.

Successive 1-to-0 transitions and start bits retrigger the one shot, holding the data path in its present configuration. Set the one shots’ time constants slightly greater than the interval between any two start bits.

When received data stops arriving, the previously active line idles high, producing a 1 at the receiver’s output. The one shot resets, returning the opposite transceiver to the receive mode—ready for any subsequent data flow in either direction.

The software protocol must wait one word length after the end of any data transmission before responding to a call or initiating a new conversation to allow adequate time for the one shots to reset. The repeater in Fig 1 handles 100-kbps data rates and an 8-bit word length, plus start and stop bits.

To Vote For This Design, Circle No. 427

---

Fig 1—This simple RS-485 repeater can compete with µP-based repeaters if you set up your software protocol properly.

98 • EDN May 26, 1994
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CIRCLE NO. 96
Pulse generator verifies test setups

Jim Williams, Linear Technology Corp, Milpitas, CA

Verifying the rise-time limit of wideband test-equipment setups is a difficult task. In particular, you must often know the "end-to-end" rise time of an oscilloscope/probe combination to ensure measurement integrity. Fig 1's circuit provides an 800-psec pulse having rise and fall times shorter than 250 psec. The pulse's amplitude is 10V, and the circuit's source impedance is 50Ω. The circuit is similar to the one Ref 1 details, except that this circuit is triggerable instead of free-running. This triggering feature permits synchronizing with a clock or another event. You can vary the delay of the output with respect to the trigger by 200 psec to 5 nsec.

The circuit requires a high-voltage bias for operation. A cascaded high-voltage transistor, Q₂, combines with a switching regulator IC to form a high-voltage, switched-mode supply. IC pulse-width-modulates Q₂ at a 100-kHz clock rate. L₁'s inductive events get rectified and stored in the 2-µF output capacitor. The adjustable resistor divider provides feedback to IC. The diode and RC combination at Q₂'s base damps inductor-related parasitic behavior. The 10-kΩ/1-µF pair filters noise from the supply line.

The R₁/C₁ combination applies high voltage to Q₁, a 40V-breakdown device. Set the high-voltage "bias-adjust" control at the point where free-running pulses across R₄ just disappear. This setting puts Q₁ slightly below its avalanche point.

Subsequently, applying an input trigger pulse causes Q₁ to avalanche. The result is a quickly rising, very fast pulse across R₄. C₁ discharges, Q₂ collector voltage falls, and breakdown ceases. C₁ then recharges to just below the avalanche point. At the next trigger pulse, this sequence repeats.

The circuit requires some special considerations for optimal performance. L₁'s very small inductance combines with C₂ to slightly retard the trigger pulse's rise time. This retardation prevents significant trigger-pulse artifacts from appearing at the circuit's output. You should select C₂ for the best compromise between output-pulse rise time and waveform purity. You may also have to select Q₁ to get the desired avalanche behavior. Such behavior, while characteristic of the device, is not guaranteed.

A sample of 50 Motorola 2N2369s, spread over a 12-year date-code span, yielded 82% usable devices. All "good" devices switched in less than 600 psec. Select C₄ for a 10V output amplitude. C₇ is typically between 2 and 4 pF. Ground-plane construction with high-speed layout, connection, and termination techniques are essential for good results from this circuit. (DI #1427)

**Reference**


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CIRCLE NO. 26
Simple module gives voice to PC

Jerzy R Chruszcz, Institute of Computer Science, Warsaw University of Technology, Warsaw, Poland

The circuit in Fig 1 uses the ISD1020A voice-record/playback chip (Information Storage Devices, San Jose, CA, (800) 825-4473) to allow an IBM PC to speak and hear. The analog part of the circuitry comes from the company’s application notes. The host PC controls address inputs (A0 through A7), Chip Enable (CE), Playback/Record (P/R), and Power Down (PD). The host also—supposedly—monitors End Of Message flag (EOM).

The ISD1020A latches an address when CE goes low, requiring a 300-nsec setup time. Fortunately, the PC’s bus controller automatically inserts several wait states (typically four wait states at 8 MHz) into I/O cycles. Consequently, the circuit needs no intermediate latching, allowing you to tie inputs A0 through A7 directly to the data bus.

A GAL20V8 PLD integrates other interface functions (Listing 1). The ZIPfile attached to EDN BBS /DI_SIG #1433 contains the listing for the PLD as well as a writeup and circuit diagram. Because of limited pin count, the PLD uses only one of the PC’s data lines. You generate various control patterns by accessing locations within address area 300H to 31FH. The PC’s I/O map reserves these locations for prototype boards. (DI #1433)

**Fig 1**—This simple interface circuit allows an IBM PC to control an advanced record/playback audio IC.
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<table>
<thead>
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<th>DEVICE</th>
<th>TOTAL SUPPLY CURRENT (μA Max, 25°C)</th>
<th>INTERNAL REF ACCURACY OVER TEMP</th>
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</table>

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CIRCLE NO. 27
Security circuit eschews sophistication

I-Cheng Chen, AEG, Ajax, ON, Canada

Because of the many states involved in implementing sequential combination locks, most designers use a microcontroller or a PLD. But for those die-hard discrete designers who don’t want to bother with debugging programs, here’s a dead-simple circuit that verifies a security code’s entry from a 10-digit keypad.

The circuit in Fig 1 verifies an 8-digit code. You preset each digit in the code sequence by installing a shunt in the respective shunt-header position. That is, to set the first digit in the code to 3, install a shunt in position 3 of SH1; to set the second digit to 7, install a shunt in position 7 of SH2, and so on.

When the circuit resets, flip-flop IC3a’s output goes high, energizing the shunted output on header SH1. If a user presses the correct key on the keypad (matching the shunted position on SH1), the input voltage to IC1B and IC1C is high enough to cause a pulse on both their outputs. If the user presses the wrong key, the R1/R2 voltage divider on the selected line supplies just enough voltage to produce a pulse only on IC1C’s output.

The output of each op amp, IC1B and IC1C, clocks its own corresponding shift register, IC4 and IC5. IC4 always advances when the user presses a correct or an incorrect key. However, IC5 advances only if the user presses the correct key.

When IC5 advances, its outputs energize the next shunt header (SH2, SH3, and so on) sequentially. Only when the user (or an intruder) presses the correct key on every stroke does IC4 advance at the same rate as IC5. When the user correctly enters all the digits in the code, the last output of IC4 toggles the output-control flip-flop. If any one of the digits is wrong, IC5’s output does not advance far enough before IC4’s output resets IC4.

Di through D8 provide isolation between the shunt headers, so that only the energized shunt header has high output on its shunted line.

C1 debounces the keypad and introduces a small time delay between the output pulses of IC1B and IC1C. This delay is critical because the output of IC1B must clock IC4 to produce an output upon the last correct digit before IC4’s output resets IC4.

Resistor array R5 is optional; it provides added security, so that if an intruder tries to press more than one key at a time on the keypad to bamboozle the circuit, the voltage drop across R5 is sufficient not to trigger IC1B because of the added load.

You can expand this circuit to as many keys and to as long a code sequence as you want by cascading multiple IC8s and IC9s. IC8’s output can drive an LED indicator to signal if the keypad is waiting for input or is in the middle of a code sequence. The ZIPfile attached to EDN BBS/DI_SIG #1429 contains a writeup of this design and its schematic in OrCAD format. (DI #1429)

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Software Shorts

Program simplifies microstrip calculations
B Breusser, Satellite Microwave & Communications Ltd Weert, The Netherlands

Written in Fortran, the simple, menu-driven programs in EDN BBS/DI_SIG #1407 determine physical line-width and quarter-wavelength dimensions from input characteristic-impedance, frequency, and substrate parameters or returns characteristic impedance from given physical line width and substrate parameters.

To Vote For This Design, Circle No. 431

Breakpoints change Spice parameters during simulation
John R Stice, Physio-Control Corp Redmond, WA

The Spice switch subcircuits in EDN BBS/DI_SIG #1408 allow simulation parameters to change on the fly when breakpoint voltages or other preset conditions occur.

To Vote For This Design, Circle No. 432

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on EDN’s bulletin-board system: (617) 558-4241, 300/1200/2400 8, N, 1. From Main Menu, enter ss/DI_SIG, then rknmm, where nnnn is the file referenced above.

Feedback & Amplification

 Corrections

Make the following corrections to DI #1351, “Line driver economically synthesizes impedance,” by Victor Koren, EDN, January 6, 1994. Add V_ox to the schematic as the output of IC. Change R_s in the schematic to R_s’ . R_s’ + R_ADD = R_p. Change R_s to R_s in equations. The circuit uses feedback, not “…a second op amp,” to synthesize the output impedance. V_ox is the output of IC, not “…the output voltage with the input shorted.” Insert a parenthesis in equation 1 after the first R_s. The last equation should be

R_s = (R_s’ x R_s + R_ox x R_s’)/ (R_ox - R_s)

The output resistance of the circuit is proportional to 1/(R_s’ - R_ox). R_ox and R_s must be very accurate and are also close in value. An inexpensive and easy way to achieve these values is to split R_s into R_s’ and R_ADD. Then, making R_s’ and R_s the same value, you can use a resistor network and achieve good matching. The output resistance then becomes

R_ox = R_s’(2R/R_A DD) + 1)
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Mark Andrews
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108 • EDN May 26, 1994
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<table>
<thead>
<tr>
<th>Interface</th>
<th>State at Reset (RST strobe)</th>
<th>Price:</th>
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<tr>
<td>7 DAC8420</td>
<td>Serial Programmable (mode pin)</td>
<td>$25.16 in 1000s</td>
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<tr>
<td>8 DAC8412</td>
<td>Parallel Reset to zero</td>
<td>$24.26 in 1000s</td>
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<tr>
<td>9 DAC8413</td>
<td>Parallel Reset to midrange</td>
<td>$24.26 in 1000s</td>
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</tbody>
</table>

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- Getting the most from high resolution digital-to-analog converters
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- DAC ICs: How many bits is enough?
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The AD7893 provides a throughput rate of 117ksps, with a power dissipation of less than 50mW. It handles data transfer via a two-wire serial interface.

OCTAL ADC—7X SAVINGS IN SIGNAL CONDITIONING
The AD7890 is an eight-channel version which offers a seven-fold savings in channel support circuitry over other integrated solutions. This economy is possible because access to MUXOUT means that the same signal-conditioning circuitry can be used for all eight channels. The AD7890 has a throughput rate of 100ksps. It also features a power dissipation of less than 50mW, and on-chip reference.

Robust Inputs
Both parts are available with three distinct input range options. Like the AD7892, they operate from a single 5V power supply, and their analog inputs are tolerant to voltages which extend well outside of the supplies, protecting them from overvoltage fault conditions (up to 17V outside for the -10 version).

The AD7890 is available in both a 28-pin cerdip and 28-pin PLCC package, in commercial, industrial and DESC versions.

FASTER SIGNALS AND CLEARER RESULTS — THE HIGHEST SINAD SPECS FROM A COMPLETE 12-BIT 1.25MSPS ADC
The AD1671 delivers leading-edge performance from a complete converter — with on-chip reference and wide bandwidth, high impedance sample-and-hold amplifier.

The AD1671's exceptional dynamic performance includes 69dB SINAD, a full power bandwidth of 2MHz and a small signal bandwidth of 12MHz. This allows better, faster data acquisition — delivering sharper images from scanners or clearer signals from communication links.

The AD1671 performance and price breakthrough are enabling markets that were previously prohibited by cost, power or price constraints. They include communications systems (high speed modems, base stations, HDSL), imaging (color scanners, medical imaging, IR) and high-speed data acquisition.

The AD1671 is available in both a 28-pin cerdip and 28-pin PLCC package, in commercial, industrial and DESC versions.

13 AD1671 Less than $40 in volume
THE WIDEST RANGE OF 12-BIT DEVICES IN THE INDUSTRY

TINY, COMPLETE SINGLE SUPPLY DACS — SMALLEST PACKAGES, EASIEST TO USE

Total DAC System — In the Industry’s Smallest Packages

The DAC8512, DAC8562, AD8522 and AD8582 are a set of single-supply 12-bit DACs, offering a complete “plug and play” output system. Everything there, everything included, everything tested and specified. And everything squeezed into a tiny SO-8 package (DAC8512).

Each part includes all the related circuits — bandgap reference, voltage-switched R-2R ladder DAC, and an output rail-to-rail op amp. Full-scale voltage of 4.095V with 1mV/bit output coding creates a programming-friendly environment while maximizing the analog output swing for all loads.

These parts also feature low power dissipation of 3mW/DAC and compact designs which make them ideal for portable or battery-operated equipment.

<table>
<thead>
<tr>
<th>Channels</th>
<th>Interface</th>
<th>Package</th>
<th>Price (in 1000s)</th>
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<td>14 DAC8512</td>
<td>Single</td>
<td>SO-8 / DIP-8</td>
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<td>15 DAC8562</td>
<td>Single</td>
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<td>16 AD8522</td>
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<tr>
<td>17 AD8582</td>
<td>Dual</td>
<td>SO-24 / DIP-24</td>
<td>$9.44</td>
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</tbody>
</table>

PROBABLY THE BEST VOLTAGE REFERENCE IN THE WORLD

5V voltage reference — low dropout, low power, high accuracy

Many of our converters are available with built-in voltage references, but sometimes you want to use an external reference. And when that’s true, there is no better choice than the REF-195.

To say that this has been popular would be an understatement — it has been a scorching success, with thousands of applications and millions shipped. And when you look at the specifications, it is obvious why — a 5V micropower reference with only 0.1V drop-out, low power (just 45mW) and high accuracy (±3mV).

What’s more, because it can source up to 30mA, the REF-195 can act as both a precision voltage reference and a highly efficient voltage regulator. And all that for an astonishingly low cost — what more could you look for in a reference?

18 REF195 $1.94 in 1000s

HIGH PERFORMANCE 12-BIT ADC SAMPLES ACROSS WIDE DYNAMIC RANGE

The AD7886 is a high-speed, power-efficient 12-bit ADC with a throughput rate of 1Msps. Its high performance makes it ideal for sampling applications requiring a broad dynamic range over a large bandwidth, as well as high-speed and multiplexed data acquisition systems. The full-power bandwidth of the on-chip sample-and-hold extends well above the 500kHz Nyquist limit, allowing the AD7886 to be used in undersampling systems in addition to the standard signal-processing applications.

The AD7886 has a low power dissipation of 250mW, and is comprehensively specified for AC and DC parameters. It features a high speed interface with 57ns bus access times, making it directly compatible with DSPs and microcontrollers.

It is available in 28-pin DIP and 28-pin surface mount packages. Temperature ranges are -40°C to +85°C for the industrial grades and -55°C to +125°C for the extended range.

19 AD7886 under $40 in 1000s

FOR INFORMATION
FAST 12-BIT SIGMA-DELTA ADC ELIMINATES NEED FOR ACTIVE ANTI-ALIASING FILTER

The AD7721 is a 12-bit sigma-delta ADC with a 200kHz bandwidth and an output word rate of 470ksps. It offers all the advantages of digital filter design, including freedom from the component matching or drift issues commonly associated with analog filters. It also drastically simplifies the design of the input anti-aliasing filter — in many cases no filter other than a simple RC roll-off is required. Other advantages include device-device repeatability, linear phase characteristics and dramatic improvement in SNR.

Operating from a single 5V supply, the AD7721 dissipates only 175mW of power while supporting a full-power signal bandwidth of 200kHz. Other features include an on-chip reference and a choice of either parallel or serial interfacing, a power-down mode and pseudo-differential inputs. It also offers a calibration mode to minimize offset and gain errors.

The AD7721 is available in 28-pin plastic DIP, SOIC and cerdip packages. Temperature ranges are -40°C to +85°C or -55°C to +125°C for the extended grade.

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The TrimDAC family reduces space requirements by providing eight independent gain channels in 20- and 24-pin packages, guaranteed to operate over the extended temperature range (-40°C to +85°C). Other features include low-power dissipation and 3-wire serial controller interface to simplify periodic service or remote adjustment.

For DC adjustment, the DAC8800 provides high and low reference inputs to establish the output swing. For AC signals, the DAC8840 features 4-quadrant multiplying adjustment for inputs up to 1MHz, while the AD8842 is suited for lower bandwidths (50kHz) at a lower price and half the power requirement.

TrimDAC is a registered trademark of ADI.

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Upgrading your design with the latest generation of 12-bit multiplying DACs couldn't be easier. The AD7943/45/48 set new standards in performance, power efficiency and cost. And feature pin-outs compatible with the industry standard AD754x DACs.

The AD794x series feature significantly improved accuracy, fast 600ns settling time, and low 60nV-sec glitch energy. They also feature the fastest digital interface available anywhere -40ns pulse width. Operating from a single +3V or +5V supply, power consumption is a miserly 1mW.

For new designs, the AD794x series lets you save valuable space; all devices are available in ultrasmall 20-pin SSOP packages, which use less than 0.1 square inch of precious board space.

The AD7943, AD7945 and AD7948 provide serial, parallel and byte digital interface, respectively. In addition to the SSOP, industry standard packages are available. These devices are specified over the -40°C to +85°C temperature range.
12-BIT 500KSPS ADCS THAT SURVIVE OVERVOLTAGE!

Real-world data acquisition and control systems often have to cope with tough environments. It's not always possible to guarantee which system will power up first. Sometimes signals on input lines can go out of range — even beyond the supply rails. Until now, this was a guarantee for destroying your ADC — and that was an expensive fuse!

The ADC7892 is a versatile, high-speed ADC expressly designed to cope with these circumstances. It is a 12-bit sampling A/D converter with a throughput rate of 500ksps, low power dissipation of only 60mW and the flexibility of both serial and parallel interface capability. Crucially its analog inputs are tolerant to voltages which extend well outside of the supplies;

A HIGH-RESOLUTION A/D CONVERTER, MOTOR CONTROLLER AND ISOLATION DEVICE FOR ONLY $2.95

The AD654 provides designers with a converter that can be applied to solve a wide range of design problems at much lower cost than ever before possible.

It is a monolithic V/F converter which reduces space requirements by integrating an input amplifier, precision oscillator system and a high-current output stage. Its high performance, low cost, low power consumption and small size make it the perfect choice for an unlimited variety of applications.

The AD654 provides a square wave output and can drive up to 12 TTL loads, opto-couplers, long cables or similar loads. The input amplifier provides low drift, permitting operation directly from low level transducers like thermocouples, strain gauges and current shunts. It also offers a high (250MΩ) input resistance to positive voltage signals. Only 2.0mA of quiescent current is required using the single positive supply from 4.5V to 26V, and the output stage can sink up to 10mA with saturation voltage less than 0.4V.

The AD654 combines low cost with very high accuracy. Linearity error is only 0.03% for a 250kHz full scale frequency, and operation is guaranteed over an 80dB dynamic range. A single RC network is all that's needed to set up any full scale frequency up to 500kHz.

Applications for this product range from high-resolution A/D converters, process control systems, and isolation to energy management, motor speed controls and power monitoring.

The AD654 is available in 8-pin PDIP and 8-pin SOIC packages in commercial temperature ranges. Temperature ranges are -40°C to +85°C for the industrial grades and -55°C to +125°C for the extended range.

Continued from front

Finally, the AD8600 features a new DAC design (patent-pending) which reduces reference glitch during reprogramming.

Space savings is a major benefit of this part, since it provides all these capabilities in a PLCC-44 package. But other features include: simplified full-scale setting; fast 2µs settling time for fast updates for analog instrument systems; minimal zero level system errors; and fast (30ns) data loading write times. A data readback feature allows system self-check at power-on.

The AD8600 operates from dual ±5V or single +5V supplies, in extended temperature range —(-40°C to +85°C).

Printed in U.S.A.
Designing 2.1V Futurebus+ termination system requires system-engineering approach

Samuel H Duncan and Robert V White, Digital Equipment Corp

Designing a termination system for a Futurebus+ power system can be a formidable task. Tight voltage tolerance and ripple-noise specifications require an approach that considers the power supply, backplane, termination, and backplane-transistor-logic drivers as interconnected units.

The demands placed on a 2.1V Futurebus+ termination power system require a system-engineering approach. With the Futurebus+, worst-case switching conditions can inject a transient on the power-supply backplane that has a current change vs time (di/dt) greater than 3A/nsec. Most power supplies can withstand only a 1A/msec load transient. To meet the Futurebus+'s demanding requirements, Digital Equipment Corp has designed a system that attaches a tightly integrated power supply directly to the Futurebus+'s backplane. The design procedure, although not exactly a "cookbook" approach, should help experienced engineers design a Futurebus+ system.

DEC's approach mounts only passive components onto the backplane because replacing defective active components requires expensive service. The design uses only one power supply, which, although not part of the backplane assembly, plugs directly into the backplane. Bypass capacitors on the backplane lower the impedance of the 2.1V power supply so that voltages at the terminators remain stable. A system approach considers the terminators, backplane, and power supply.

Before considering the power system, review the requirements for the 2.1V backplane. The two most important requirements are the voltage tolerance and the output-load current. The Futurebus+ standard specifies that the output voltage must be within ±2% of 2.1V and have a voltage ripple lower than ±50 mV. The ±2% tolerance includes variations in initial tolerance, line regulation, average dc regulation, temperature drift, long-term drift, and ripple and power-supply noise. Because of the switching actions of the bus, the design must meet the ±50-mV specification at the terminators, not at the power-supply output.

Meeting the ±2% power-supply tolerance can be challenging. DEC systems use reference voltages having a tolerance of only 0.25%. Although tight tolerance references are expensive, they eliminate voltage trimming in the factory. Bypass

![Diagram](image-url)
FUTUREBUS+ TERMINATORS

capacitors that maintain the ±50-mV ripple specification attenuate power-supply and ripple noise. However, load current can introduce dc-distribution losses. You can calculate the minimum and maximum load current, even though the current is stochastic.

To determine the load-current bounds, consider a Futurebus+ active single driver and two backplane 33.2Ω resistor (Fig 1). When any signal line is in the low state, the driver draws current from the 2.1V supply. Typical current draw/signal line is:

$$I_{\text{typ}} = 2 \times \frac{(V_{\text{term}} - V_{\text{low}})}{R_{\text{term}}}$$

$$I_{\text{wc}} = 2 \times \frac{(2.10\text{V} - 1\text{V})}{33.2\Omega} = 66.3 \text{mA}.$$  

The 66.3 mA is a typical current draw. In worst-case conditions, the terminator voltage can be as high as 2.142V, and the logic low voltage can be as low as 0.75V. In addition, the terminator resistors have a ±1% tolerance. Adjusting for worst-case parameters, the worst-case current is:

$$I_{\text{wc}} = 2 \times \frac{(2.142\text{V} - 0.75\text{V})}{32.868\Omega} = 84.7 \text{mA}.$$  

A 6-slot backplane having a 64-bit data bus has 130 signal lines that can draw current from the power supply when you include the arbitration signals. Generally, no more than 100 lines switch simultaneously, however. Therefore, 100 signal lines, each drawing 66.3 mA, typically draw 6.63A total current from the power supply. The absolute worst-case condition occurs when 130 lines draw 84.7 mA, resulting in an 11A current draw from the power supply. This is an unrealistic case, however. A worst case of 10A is more likely.

The minimum load current occurs when all of the drivers are off and no current is drawn from the power supply. Although this is an unrealistic case, a conservative design requires the 2.1V supply to remain within specification when there is no load. To be more precise, a conservative design assumes no external load. A preload current is usually drawn from a switching power supply to keep the power supply operating in its linear, continuous mode. This design uses a preload current of 0.5A, which dissipates only 1W. If you use a linear regulator, the preload current biases the pass transistor into its active region.

To meet the 50-mV specification, assume that 100 signal lines can change at once and that the bus switches in a minimum of 2 nsec. The load transient under these conditions is 6.6A/2 nsec=3.3A/nsec. In practice, the load transient is not this large. Because of bus skew, all of the signals do not arrive simultaneously at the terminators. The terminator resistors' inductance also slows the rise of the current transient on the 2.1V backplane. However, to find the worst-case load transient, this design ignores these factors.

Consider the complete power-supply system when determining the voltage at the terminators. Designing a backplane by throwing in some random bypass capacitors and hooking up a power supply using 1m of cable does not work. Designing a complete power system means considering the terminator resistors, 2.1V layers in the backplane, bypass capacitors, backplane to the power-supply connectors, and power-supply output. The DEC design uses Spice to simulate the system, although it can use a lumped-element model because the 2-nsec backplane doesn't require a transmission-line model. The Spice model describes the load as a series of resistance and time-varying voltages.

Locate the 2.1V power line and its return on adjacent layers and on inner layers of the backplane to minimize impedance. This arrangement reduces inductance and increases capacitance. The design requires a 2-oz-thick min
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**A/D Family Features**

<table>
<thead>
<tr>
<th>Model</th>
<th>Resolution</th>
<th>Sample Rate (MSPS)</th>
<th>Input Bandwidth (MHz)</th>
<th>Power Consumption (W)</th>
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<td>8-bit</td>
<td>500</td>
<td>300</td>
<td>2.8</td>
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<tr>
<td>HI1166</td>
<td>8-bit</td>
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<td>HI1396</td>
<td>8-bit</td>
<td>125</td>
<td>200</td>
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<tr>
<td>HI1386</td>
<td>8-bit</td>
<td>75</td>
<td>150</td>
<td>0.58</td>
</tr>
<tr>
<td>HI1175</td>
<td>8-bit</td>
<td>20</td>
<td>18</td>
<td>0.06</td>
</tr>
</tbody>
</table>

Also available:
- HI20201, 10-bit, 160 MSPS update rate
- HI20203, 8-bit, 160 MSPS update rate
- HI1171, 8-bit, 40 MSPS update rate

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copper line. Connect the 2.1 V power supply to the backplane near the center of the board, which is equidistant from the terminators. Using this arrangement, the distribution resistance of the power-supply plane is about 500 µΩ.

In selecting bypass capacitors, calculate the minimum capacitance to hold up the 2.1 V terminator voltage until the power supply can respond, and calculate the maximum amount of inductance allowed on the 2.1 V distribution line. The DEC design calculates the capacitance and inductance for a linear power supply to maintain a 50-mV ripple voltage. Supply response time is 50 µsec. Estimating the capacitance based on allowing no more than 50 mV of droop in 50 µsec yields:

\[ C = \frac{I \times dt}{dV} = \frac{6.6A \times 50 \mu \text{sec}}{50 \text{ mV}} = 6600 \mu \text{F}. \]

Estimating the inductance yields:

\[ L = \frac{V \times dt}{di} = \frac{50 \text{ mV} \times 2 \text{ nsec}}{6.6A} = 15.2 \text{ pH}. \]

The capacitance is large but physically realizable. Although the inductance is too small to be realizable, many terminators contribute to this lumped-element calculation. The maximum inductance for a terminator is:

\[ L = \frac{V \times dt}{di} = \frac{50 \text{ mV} \times 38 \text{ nsec}}{33.1 \text{ mA}} = 57 \text{ nH}. \]

Although the 3-nH inductance is small, surface-mount-technology (SMT) capacitors are available with subnanohenry inductances. Such capacitors include a 0.082-µF capacitor with 0.7-nH effective series inductance (ESL) and 40-mΩ effective series resistance (ESR). The company also offers a 0.15-µF model with 1.5-nH ESL and 70-mΩ ESR. Designs incorporating the 0.15-µF capacitor need only one capacitor/two terminator resistors; designs with the 0.082-µF capacitors require one capacitor/four terminator resistors. This design uses the 0.082-µF part, which requires 62 capacitors. The equivalent lump-capacitance sum is 5.08 µF (4.07 µF worst case, allowing for a ±20% tolerance).

**Place capacitor close to terminator**

Place these capacitors close to the terminator resistors. The design requires at least three vias to connect the mounting pads to the 2.1 V and return layers. Any discrete etch noticeably degrades performance. **Fig 2** shows a suggested backplane-layer and capacitor-connection scheme. Although the capacitors have a small enough inductance to support the load transient, they do not have enough capacitance to hold up the terminator voltage until the power supply can respond. Using the following approximation, the bypass capacitors at the terminators should hold up the voltage for only a few nanoseconds:

\[ dt = C \times dV / I = 5.08 \mu \text{F} \times 50 \text{ mV} / 6.6A = 38 \text{ nsec}. \]

The above equation shows that the design requires at least another stage of capacitors to hold up the voltage. Each terminator requires no more inductance than the that of the following equation:

\[ L = \frac{V \times dt}{di} = \frac{50 \text{ mV} \times 38 \text{ nsec}}{33.1 \text{ mA}} = 57 \text{ nH}. \]

This is a reasonable amount of inductance to provide the additional hold time. The design includes 16 100-µF SMT electrolytic capacitors on the backplane between the termination resistors and the point at which the termination power enters the backplane. Even though the total capacitance does not quite equal 6600 µF, the electrolytic capacitors are sufficient for the task.

DEC's first systems use power modules that plug directly into the backplane. One system uses card-edge connectors, and the other uses DIN-style power pins and sockets. Direct plug-in connection to the backplane results in a minimum amount of resistance and inductance parasitics. However, the Spice model must include these parasitics. The design uses three 2200-µF, low-ESR aluminum capacitors for the power-supply output. It also uses 0.220-µF ceramic capacitors at the power-supply connection to filter high-frequency noise.

To meet the Futurebus+ specifications, the design stages an array of capacitors throughout the backplane in three stages. The first stage comprises 0.082-µF, high-frequency bypass capacitors near the terminator resistors. The second stage, an array of 100-µF electrolytic capacitors, provides the bulk storage. The third stage includes the power-supply output capacitors. **Fig 3** shows a simplified schematic of the Spice model for the final design.

The Spice model predicts that the configuration can meet the Futurebus+ specification under worst-case switching conditions of the bus. You can test this condition by building an exerciser for the Futurebus+ that allows the simultaneous transition of any number of signal lines. When all lines are additional hold time. The design includes 16 100-µF SMT electrolytic capacitors on the backplane between the termination resistors and the point at which the termination power enters the backplane. Even though the total capacitance does not quite equal 6600 µF, the electrolytic capacitors are sufficient for the task.

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**Text continued on pg 122**
Identify signal distortions before they occur.

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References

Acknowledgment
Thanks to Bill Samaras, who created the staggered-capacitor idea, and Bruce Loughlin, who performed much of the Spice simulation and other research.

Authors’ biographies
Samuel H Duncan is a consulting engineer for Digital Equipment Corp, Maynard, MA. For 15 years, he has done development and consulting work on I/O architectures and interfaces, firmware, and diagnostics. He also helped develop the DEC 4000, 7000, and VAX 8800 computers. Duncan has a BSEE in applied math and computer science from Tufts University, Medford, MA, and is a member of the IEEE Computer Society, IEEE Bus Architecture Standards Committee, and IEEE µP and µC Standards Committee. He is also chairman of the working groups that developed IEEE 1212.1-1993, 896.1a-1993, and 896.2a standards. He is married; has three children; and likes to restore his home, sail, wind-surf, bicycle, and ski.

Bob White works for AT&T Bell Laboratories in Mesquite, TX. Before joining AT&T, White was a principal engineer in the Power Systems Engineering Group at Digital Equipment Corp in Maynard, MA. He served as DEC’s internal consultant on power-related issues in the Futurebus+ specification development. He was also the power-system architect and technical-team leader for the DEC 4000 computer system. White is the technical vice president of the IEEE Power Electronics Society.

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An energy gauge built into a rechargeable battery pack can tell you exactly how much charge remains available for use. It can also direct an inexpensive "dumb" charging device to charge the pack in an optimal manner. It can even store a history of battery health.

It's too bad laptop computers, camcorders, and cellular phones can't run for 20 hours on a battery the size, shape, and value of a quarter. But they can't, so manufacturers offer ICs and other components to simplify the job of efficient power management. Such products include dc/dc converters, battery-charging devices, and power-switch arrays that control energy-consuming components like disk drives and backlit screens.

But perhaps the most dramatic advance in power management is in battery-energy gauges. These units, which often reside inside a battery pack, actually monitor the amount of energy that flows into and out of a battery to make accurate estimates of the amount of charge remaining. These estimates are available not only to the user, via an on-pack display, but also to the battery-run device, via some sort of serial data link. To a designer, this data is valuable information because the battery pack is often a device's largest, heaviest, and most expensive component.

Voltage readings aren't enough

Most rechargeable batteries for portable electronic devices are nickel-cadmium (NiCd) or, more recently, nickel-metal hydride (NiMH). These batteries' chemistries allow fast recharging and offer a good combination of energy density, uncharged shelf life, and low cost. Unfortunately, a simple reading of terminal voltage, either open circuit or under load, yields little information about their present state of charge. To understand why, look at the discharge curve for a NiCd battery (Fig 1). (NiMH batteries, by the way, behave in almost the same way during discharge.)

As Fig 1 shows, terminal voltage drops rapidly for a brief time and then is followed by a long period of slow decline. As the battery nears depletion, the voltage again falls off quickly. At first glance, it would appear a simple matter to translate the terminal voltage, especially in the central region of the graph, into a measure of remaining charge. Indeed, some manufacturers have marketed crude energy gauges that use this approach. The results are woefully unreliable, however, because the absolute cell voltages are a function of temperature, internal pressure, and battery age. The amount of deviation caused by these factors negates any meaningful information derived from voltage alone.

The situation during charging is similar, as indicated in Fig 2's typical charge curves for NiCd and NiMH cells. As in discharging, these two chemistries behave in an almost identical manner, an exception being that the NiMH batteries do not experience as much decline in voltage as they go into overcharge. Here, too, terminal voltage does not give a reliable measure of the state of charge, because the absolute values of the voltages vary with factors such as temperature and pressure.

The only accurate way to know how much charge is actually in a battery pack is to count the coulombs as they come and go. While this appears a conceptually easy task, a number of subtleties arise that quickly make it a formidable one.

![Fig 1 - The absolute level of a battery's discharge curve depends on several variables, including temperature and pressure. The curve shown here is typical of NiCd batteries.](image-url)
ENERGY GAUGES

Nonetheless, highly accurate gauges are now available that take these subtleties into account.

A simplistic way of viewing a rechargeable battery is as a tank of electrons. As the charge depletes, the tank drains. As it recharges, the tank fills. To know how full the tank is, you need to count the electrons as they go into the empty tank. If the size of the tank is also known, you can make an estimate of "percent full."

Electrical current is a measure of electron flow, where 1 A = 1.6 × 10^19 electrons/sec. To count electrons, the energy gauge must monitor battery current and then numerically integrate it over time. This process requires three elements of hardware to implement: a current-sensing device, an A/D converter, and a processor to perform the integration and send the results to the host.

For monitoring really large currents, a Hall sensor can measure the magnetic field surrounding the current path and translate it into a current reading. But Hall devices require cumbersome magnetic cores and support electronics, and they're not cost-effective for most applications.

By far, the least expensive and most common approach for current sensing is to insert a low-value resistor in series with the current path and measure the voltage drop across it. Since any resistance inserted in the main current path potentially wastes power and may even limit the amount of current that can flow under surge conditions, the minimum possible resistance is preferable. Typical values range from 0.01 to 0.50.

An A/D converter measures the voltage across the current-sensing resistor. To resolve currents of 1 mA over a range of ±4 A, converter resolution of 13 bits is necessary. The signals involved may be minuscule, typically on the order of 100 µV. After conversion to digital form, it is relatively easy to numerically integrate the readings with a µP.

Battery capacities exceed ratings

Returning to the analogy of a battery as a tank of electrons, it is important for an energy gauge to be able to measure the actual size of the tank. Manufacturers of rechargeable batteries specify the capacity ratings for their cells in milliamp-hours (mAh). These ratings are minimum values, and the actual pack capacity often exceeds its rated value by 20%. Also, the capacity usually decreases as the pack ages.

For the gauge to measure actual pack capacity, it must be able to sense when the "tank" is completely empty and when it is completely full. It does this by monitoring pack voltage and temperature as a function of time. For NiCd and NiMH batteries, it considers the fully discharged state to be when the pack voltage drops below about 1 V per cell. The fully charged state can be characterized in several ways.

An approach that battery manufacturers recommend for determining the fully charged state of NiCd cells is called negative-delta-V detection. This approach requires sensing when the terminal voltage just starts to drop from its peak (Fig 2). While this technique also works with NiMH cells if the voltage resolution is sufficiently high, many cell manufacturers recommend dT/dt detection for NiMH. The dT/dt approach considers full charge to be when the pack temperature starts rising faster than some specified threshold.

Adding these capabilities for determining the fully charged state requires additional channels of A/D conversion or, perhaps, extending the resolution of the existing channels. For instance, to resolve voltage changes of 1 mV out of a battery voltage of, say, 20 V (as is necessary for using negative delta V with NiMH batteries) requires an A/D resolution of 15 bits. By contrast, temperature sensing requires only about 9 bits of resolution. As it turns out, both temperature and voltage readings are necessary for proper gauging.

Energy gauges' advantages

Once an energy gauge has the ability to sense when a battery is fully charged and fully depleted, it can perform several other important functions. First, the gauge can automatically calibrate itself to the pack by measuring the actual amount of energy that can be extracted from the pack. In some gauging devices, the host must initiate this calibration; in others, calibration happens automatically whenever the pack runs from a fully charged state to a fully discharged one. With internal registers, a gauge can store capacity information for use in calculating present charge state as a percentage of capacity. A gauge can also monitor pack capacity over time as a barometer of battery health.

Once a battery gauge has the features just described, it has all the intelligence necessary for charging the battery pack. This intelligence need not be duplicated in external charging devices as long as some means exists for the pack to control an external "dumb" charger. The gauge can bring this control information out on a single hardware line or transmit it as part of a data stream.

Because determining actual pack capacity can take several hours, it would be unfortunate if this information got lost. This is a very real possibility, however, because the user can inadvertently let the pack discharge below the level necessary to keep the energy gauge working. Or, a static discharge could corrupt an internal register. For these reasons, some vendors have incorporated electrically erasable PROM (EEPROM) into their gauges for storing critical parameters.

The addition of nonvolatile memory also lets the vendor offer a single standard product with a menu of features that the user can select through appropriate programming of EEPROM registers. For example, the menu might offer a range of charge-termination techniques, including negative delta V and dT/dt, with all the parameters selectable by the user.

Addition of EEPROM also allows the gauge to track battery history. This history might include basic information, such as how many charge cycles the pack has experienced, or...
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EDN May 26, 1994 • 127
more exotic things, like the maximum and minimum temperatures experienced by the cells. Such information is useful in projecting a pack’s life expectancy and even for deciding whether to honor a warranty on a supposedly defective unit.

Using the measured information

Now that the energy gauge has amassed all this information about the battery, what happens to that information? The most fundamental piece of information, the percentage of full charge, is often directly available on an LED or LCD. LEDs draw significantly more current than LCDs, so they’re usually accompanied by a pushbutton switch for momentary activation. LCDs, on the other hand, can run continuously, but they’re more delicate (removable battery packs are highly susceptible to being dropped), and they don’t behave well at temperature extremes. For these reasons, LEDs are currently the display of choice.

Battery information is also usually available to the host equipment via some form of serial link. Various protocols are available, ranging from custom versions to standard RS-232C. The amount of information provided also varies among manufacturers. Along with percentage of full charge, it may include instantaneous readings of voltage, current, temperature, pack capacity, charger-control information, multiple levels of low-battery warning, and indications of any potential battery-error conditions.

Because most energy gauges reside inside a battery pack and draw their operating power from the battery, they must use as little power as possible, especially when the pack is not in use. Good gauges, therefore, enter a low-power mode when they sense their host is turned off. Quiescent currents of 50 µA are typical.

Operating voltage is also worth considering. Some energy gauges require a 5V source for their supply, which can require tapping into the battery string for 1.2V/cell NiCd and NiMH batteries. With packs of four or fewer cells, these gauges become unusable. Other gauges, however, can handle supply variations ranging from 3V or less to more than 25V.

You also have to consider the ways in which rechargeable batteries differ from the simple model of an electron storage tank. For example, all batteries, rechargeable or otherwise, exhibit the phenomenon of self-discharge. That is, a fully charged cell loses charge over time. The phenomenon is particularly noticeable with NiCd and NiMH cells, which typically lose about 1 to 2% of their charge each day. After three months of sitting idle, a previously fully charged pack will be dead. Worse yet, the self-discharge rate is a strong function of temperature. Storing the pack at 40°C instead of 25°C will cause it to fully discharge in just a few days.

Because equipment used outdoors or left in the trunk of a car can experience high temperatures, energy gauges must monitor battery temperature and use it to account for self-discharge. However, the rate of self-discharge as a function of temperature varies with cell chemistry and manufacturing techniques. If an energy gauge has onboard EEPROM, an OEM can program the appropriate self-discharge parameters; other gauges must either approximate self-discharge with a ‘one-size-fits-all’ algorithm or ignore it altogether.

Other factors that affect gauge accuracy include various charge and discharge efficiencies. For instance, charging efficiency is always less than 100% and drops off considerably as a pack nears full charge, because much of the energy pumped into the pack goes toward producing gasses rather than into a retrievable form. Likewise, temperature affects charge efficiency. All these parameters vary with chemistry and manufacturing techniques, but they can be accounted for if a gauge has the means to do so.

For an idea of the accuracy you can expect from an energy gauge, see the data in Fig 3. The plot shows pack voltage and percentage of remaining charge while a battery discharges at a constant rate of 1000 mA. This data, representing the fifth discharge cycle after calibrating a gauge to a battery pack, yields an overall accuracy of 0.22%. Under less ideal conditions, accuracies of 1 to 2% are typical.

The benefits of incorporating an energy gauge into a product line are several. First and foremost, both the user and the host equipment can know exactly how much charge is available from a battery pack. This is true whether the pack is currently in use or has been pulled from storage. A second benefit is that the extra battery capacity above rated value is available for use. In addition, an energy gauge eliminates the need for sophisticated charging equipment; it can control an external “dumb” charger at the cost of one extra terminal on the battery pack. Further, one charger can recharge various types of batteries.

The cost of adding an energy gauge to a product depends on several factors: sophistication and resolution of the hardware, desired current range, size and shape of the gauge, number of interface contacts with the host, communication protocol (if any), and type of display used. With all these variables, it is difficult to give specific price information. However, a typical energy gauge now adds about 25% to the cost of a pack, although prices are likely to drop rapidly over the next few years. Be aware, though, that some units come as fully assembled modules, while others are single ICs that require additional circuitry.

Author’s biography

Malcolm McClure is Director of Battery Servicing Products at Span Inc in Indianapolis, IN. He has BSEE and MSEE degrees, both from Northwestern University.

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If you're planning to buy, use, or design products compatible with the standards of the Personal Computer Memory Card International Association (PCMCIA), you need a copy of *The PCMCIA Developer's Guide* by Michael T. Mori. This self-published book (Tori is an independent design consultant) is by far the best collection of useful information I've seen on PCMCIA—a valuable blend of tutorial information, product information, and design guidelines. Moreover, Mori has obviously taken great care in choosing what not to include in the book, so you can plunge right in and learn quickly, without getting bogged down in details for which you're not yet ready.

The book begins by briefly summarizing the evolution of the association and the PCMCIA standard. Then, in 10 pages or so, it gives a remarkably clear overview of today's expanded standard. The standard itself isn't hard to read, but this summary quickly gives you a good perspective.

The real meat of the book begins in Chapter 3, "Designing a PCMCIA host adapter." A host adapter, in this sense, is simply something that connects to a host computer and accepts PCMCIA cards. It can be part of the equipment you're designing, or it can be an external unit. This chapter doesn't have every design detail you need, but it explains the major design issues, and it provides enough information at the block-diagram level to give you a sense of what you're up against.

Chapter 3's tutorial information is all the better for having just the right amount of basic information about some of the more popular PCMCIA ICs available for designers. (Later, in Chapter 8, there's more detail about a wider range of chips.) Most of the ICs this chapter discusses are socket-controller ICs, which provide the needed connections and signals between a PC bus and one or more PCMCIA card sockets. PCMCIA applications aren't limited to the PC architecture, but commercially available socket controllers are. You can design PCMCIA interfaces for other buses, but you have to do a lot more of the work yourself.

The next chapter, "Designing a PC card peripheral," looks at the myriad issues of designing a plug-in PCMCIA card. In about 35 pages, it covers electronic design, mechanical design, software and compatibility issues, and agency approvals. Most of this information deals with electronic-design issues that are specific to memory cards and to what PCMCIA calls "I/O cards," which can contain practically any kind of peripheral device. You need to read the entire PCMCIA spec before you actually undertake a design, but this chapter boosts you up the learning curve.

Chapter 5, "PCMCIA software requirements," takes on what is undoubtedly the most confusing and troublesome aspect of using or designing PCMCIA products. PCMCIA has not reached all of its ambitious software goals—including plug-and-play operation and "hot swapping" of vastly dissimilar types of cards—despite the existence of some very sophisticated and complex system software. This chapter explains, as well as 20 pages of text can explain, the software issues and which products are available to deal with them.

The chapter does an adequate job of describing succinctly what PCMCIA system software does and, in some cases, what it doesn't do. For example, a PCMCIA system-software module called Card Services (available from several software vendors) is not yet sufficiently general to control every type of card that you can possibly insert in a PCMCIA slot. To get around the problem, card vendors provide specific card "enablers," essentially device drivers that defeat PCMCIA's hot swapping and plug-and-play goals. The issue of specific-vs-generic enablers is one that anyone involved with PCMCIA is going to have to address—a lot.

The future of PCMCIA gets a short chapter of its own in the book. The chapter's main topics are the recent and planned additions and modifications to the PCMCIA standard: additional operating voltages (more than just 5 and 3.3V), the 32-bit CardBus (which is patterned after the PCI-local bus and allows bus mastering), power management, multifunction cards, and more.

Next, the book provides an 80-pg product-information guide. A short chapter summarizes the types of PCMCIA products that are available, and a much longer chapter details several products. The product categories include all types of PCMCIA cards, chips, system software, development tools, and interconnection hardware. This information will soon be out of date, but it appears remarkably complete for now. The book's publisher expects to create revised and updated editions periodically, with the first one coming fairly soon.

Finally, appendixes to the book contain almost 200 pgs of reference information, mostly from the PCMCIA specification. Having all this information in one book is handy, and the resulting single volume isn't all that bulky. It contains 400 or so 8.5×11-in. pages in all—about the size of a 1-in.-thick notebook.

The *PCMCIA Developer's Guide* isn't the only source of information you need to design PCMCIA products, but it's a good starting point. It assembles a lot of useful information, and that information is clear, concise, and probably the most relevant of all the information you need to get a quick start with PCMCIA design.

The book isn't cheap; it costs $89.95 plus shipping. But if you need to learn about PCMCIA and you value your time, you'll get your money's worth and more.—Gary Legg

Sycard Technology, Sunnyvale, CA. (408) 247-0730.

Circle No. 422
Verify DSP-filter designs with SystemView

When performing DSP designs, you must weigh the tradeoffs of FIR vs IIR filters before committing to hardware. FIR filters lack a feedback path, thus ensuring inherent stability. FIR filters also provide an exactly linear phase response, so phase distortion does not occur. However, FIR filters typically require more computational time, especially in hardware that has only a single multiplier. A fast FIR requires a prohibitive number of multipliers to perform multiplications in parallel.

These drawbacks could also be a problem in DSP applications in which software performs the operations sequentially. The more instruction cycles needed to implement a filter, the fewer clock cycles you have for other processing tasks.

Using Ealanix’s SystemView ($98.50), a dynamic system-level simulator, you can quickly address these problems and verify the merits of both types of filters. This graphical system simulator runs on PCs under Windows and lets you specify all relevant information and display the results simultaneously side-by-side.

The application I decided to simulate uses a lowpass filter having a 1-kHz cutoff frequency to operate with a sampling rate of 8 kHz. The first step in setting up the simulation was to select a sweep generator from the sources that the software offers. I configured the sweep generator to run from 10 Hz to 4 kHz. You select the sweep generator from a menu of source signals and specify its parameters by filling in a form. The sweep generator mirrors the actual method of evaluating the performance of the filter. An alternative source could have been the impulse, or “delta,” function.

The next step was to quantize the input to 16 bits. I selected the quantizer from the appropriate function-token library and filled in its parameters. I then connected a signal-display token to the output of the quantizer. You can attach a display token anywhere in the simulation to aid diagnosis or to view intermediate results.

The next step in the simulation was designing the filters. I selected “linear system” from the operator-token library and then chose the types of filters from among FIR, IIR, and Laplace-transform filters. I then filled in another form for each filter with its critical specifications, the amount of gain in the passband and the stopband, and the number of coefficients to use. The software can estimate the number of taps needed to meet the specifications in the FIR menu. You can select fewer taps than the software suggests, but doing so may mean the filter will not meet your specifications.

I examined four filter types: an 18-tap, lowpass FIR filter, a Butterworth IIR filter, a Bessel IIR filter, and a Chebychev IIR filter. All my IIR filters had eight poles, giving the same number of multiply-accumulate operations.

An important consideration when selecting a filter is the effect of quantizing the filter’s coefficients to a specified number of bits. With this software, I simply entered the appropriate values in the text boxes. In this case, I set the coefficient quantization to 16 bits. The simulation showed that quantization has its biggest effect on the Chebychev filter’s performance and a smaller effect on the FIR filter’s.

After I specified all four filters, I started the simulation. The simulation injected the output from the quantized-frequency sweep signal into each of the filters and placed a display token at the output of each filter.

Once the simulation finishes, you can use the program’s analysis window to examine—simultaneously or separately—the output response of each filter. You can view the signals in the time domain or the frequency domain, and you can view the frequency-domain data along a log or a linear axis.

The Butterworth and Bessel filters turned out to have a smooth inband response, but their frequency rolloff was slow. The FIR and Chebychev filters had a much steeper cutoff but had a significant passband-amplitude ripple. For the FIR filter, this ripple arises from the small number of taps. The application specified a 0.1-dB ripple, but the optimization routine could satisfy this constraint only by averaging and by using 18 taps. The 16-bit word size also raised the out-of-band ripple of the FIR filter. The Chebychev filter’s ripple comes from the 16-bit finite-word size of the filter-tap coefficients.

Another design feature you can apply to the FIR filter is “windowing.” Windowing multiplies the given impulse response, h(t), with a window function, w(t), to produce a new filter response g(t)=w(t)h(t). We usually think of windows as a means of reducing the spectral side lobes of Fourier transforms. In this context, multiplying by the window in the time domain convolves the frequency response of the window with the frequency response of the original filter.

The lowpass nature of the window’s response smooths the original response.

Fig 1 compares a Hanning-windowed filter and the original FIR filter. The windowed filter offers a vast improvement in ripple over the FIR filter, but the windowed filter does not roll off as sharply as the FIR filter does.

I chose the windowed FIR filter for this application because of its good cutoff, low out-of-band response, and low in-band ripple. The FIR filter is also inherently stable and has no phase distortion. The actual frequency response of the filter, when implemented in an Analog Devices AD-2101 EZ-Lab DSP evaluation board, exactly matches the SystemView simulation.

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EDN May 26, 1994 • 131
Software probe provides background emulator for HP tools

The HP3490A software probe provides a Motorola background-debug mode (BDM) interface to Hewlett-Packard's software-development tools. It provides run-control, memory-inspection/modification, and code-downloading functions over a network.

The front panel of the instrument connects to a target's BDM port. The front panel also has two BNCs that connect to a logic analyzer. The logic analyzer can use a trigger-out signal as a qualifier to start an event, such as tracing. A trigger-in BNC allows the logic analyzer to force a breakpoint.

Automatically move from a Matlab simulation to an embedded system

Those using The MathWorks' Matlab and Simulink to simulate and analyze systems can now let their computers create the C code to implement models on targets running the VxWorks real-time operating system (RTOS). You can model the operation of the system you are developing by interconnecting block-level diagrams or by using the Matlab language.

You can rapidly prototype a design by letting the C-code generator produce C code, compile it, and run it on your target. Simulink's graphical user interface allows you to select and connect function blocks. It can generate continuous, discrete-time, or hybrid runtime code. Once the system simulation meets your satisfaction, you can move appropriate portions of the system to your target.

For example, you might also simulate real-world inputs when simulating a system. When you move the design to the target, the real world provides the real-world inputs, and you do not need code for these functions. Once you generate the code, you can insert it back into your simulation to test it before letting it loose on the target.

You can use the C-code generator with VxWorks, and you can interface other RTOSs to the tool by modifying a file that defines the RTOS service calls the code generator uses. The C-code generator also includes documentation, source code, make files, and examples for creating RTOS support.

The Control Framework API automatically builds programs based on customizable make files. These make files define compiler options, source files, libraries, and automatic download options.

The C-code generator requires Matlab (starting at $1695) and Simulink (starting at $1995). The C-code generator costs $9995 for either the PC or the workstation version.

PowerPC simulator lets you test your system without the system

The PowerPC Virtual System from IBM allows you to simulate not only the code running on a µP, but also the ASICs and other system components. The Virtual System is built around the PowerPC Visual Simulator (PVS). This simulator provides a simulated debug environment that allows you to test code, optimize system-design considerations, such as cache size and memory-access times, and interact with simulated I/O from a graphical user interface.

With Virtual System, you can model the complete I/O subsystems or just selected functions. A C-based application-programming interface (API) is a set of C-language functions that an I/O model can use to interact with the simulated PowerPC.

The PVS bus-model API can also connect the PVS to a simulation of your I/O. In this case, the bus-model interacts with the ASIC-simulation environment. This interaction lets you use actual ASIC models to provide the I/O simulation to the PowerPC.

The VHDL model for the bus of the PowerPC603 is now available free. Other models will become available in the future. As you debug your software, you can see how it reacts to a simulation based on the actual data used to create the ASIC. You don't have to worry about creating a new model to work with the simulator.

By simulating not only the µP and the other subsystems, but also the actual VHDL-design data, you can check out more of the system before committing to hardware. Catching errors early in the game is a key factor in reducing development time. The PVS runs on IBM RISC System/6000 workstations and costs $6000.
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Synthesize logic from behavioral description

The Behavioral Compiler from Synopsys provides the next step in design automation, offering potentially large improvements in designer productivity. Specifying an IC at the behavioral level requires only one-fifth to one-tenth as much time as specifying at the register-transfer level (RTL), the company estimates. In addition, the compiler lets you routinely simulate your design at the behavioral level, saving significant simulation time over structural-level simulation.

The tool suits designs that are best described by algorithms. Typical applications include telecommunications, high-end graphics, and multimedia. The tool frees you from designing the cycle-by-cycle behavior of a design. Instead, you can focus on algorithms while the tool performs multicycle optimization using techniques such as pipelining, multicycle operation, chaining, and resource sharing.

Many algorithm-based designs start as a C or a C++ language specification. Instead of translating the code into an RTL specification, you can write a behavioral specification in VHDL or Verilog that is very similar to the original language specification. According to the company, the behavioral specification may be only one-tenth as long as the RTL specification for the same design. Furthermore, the close relationship between behavioral-level hardware-description languages (HDLs) and software facilitates software/hardware system design.

Painlessly improve IC-test fault coverage

The tool goes beyond the typical behavioral-level data-path designs available with other tools to include controller and memory inferencing. The tool automatically infers a design's controller from the behavioral specification and integrates it with the data-path portion of the design. The Behavioral Compiler also infers memory reads and writes from HDL-array accesses, allowing it to schedule memory access automatically. You no longer need to perform memory timing and scheduling manually.

Because the behavioral description does not imply an architecture, the synthesized architecture varies, depending on a few easily varied high-level constraints. This technique makes design reuse much more efficient than it is with RTL design.

Behavioral Compiler relies on and offers tight integration with the company's other architectural and logic-synthesis tools. It costs $69,500 and is in Beta test. The company plans to begin shipments in the fourth quarter.

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Behavioral Compiler relies on and offers tight integration with the company's other architectural and logic-synthesis tools. It costs $69,500 and is in Beta test. The company plans to begin shipments in the fourth quarter.

Many of the same current-drain concerns important to designers of battery-powered circuits are also concerns in I_{DDQ} testing. So, the tool improves a design's testability while reducing power consumption. The tool offers such changes as eliminating bus contentions and floating buses by synthesizing structures, such as control gates and bus keepers.

CrossCheck plans to ship Current Synthesis in the third quarter; prices start at $15,000. The product is an option to CurrentTest ($45,000), a currently available tool that develops the I_{DDQ} test vector.
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CIRCLE NO. 115  EDN May 26, 1994  • 135
Logic emulator combines fast compiling with low cost

The Pegasus logic-emulation system from Arkos Designs takes a different approach from logic-emulation systems based on Xilinx field-programmable gate arrays (FPGAs). The emulator uses a massive array of custom logic processors designed specifically for emulation. Each logic-processor chip contains 32 logic-processing units. A fully configured system for emulating 200,000-gate designs uses 512 of the processing chips on eight PC boards for a total of 16,000 processing units. Depending on the size of the design, the processors perform four to 16 sequential operations, reducing the 50-MHz speed of the processing units to a 3- to 12-MHz system-emulation speed.

According to the manufacturer, the emulator has ample routing resources, and compiling a 200,000-gate design takes less than 30 minutes. Instead of solving complex FPGA-routing problems, the system loads the functions into the processing units and assigns routing connections. Because the compiling speed is much higher than those of competitive systems, the emulator lets you find design problems interactively—something you can't do with long recompile times.

Each logic processor includes a 32,000-vector embedded logic analyzer, providing access to every node in an emulated design, as well as on-chip RAM. In addition, each Pegasus board provides 4 Mbits of high-speed RAM for emulating RAM, ROM, FIFO buffers, or multiport RAM.

Pegasus requires a 486 PC or a Sun workstation for operation. Prices for a 25,000-gate version start at $36,000, and a 200,000-gate version costs $115,000. The price includes all hardware, software, and logic-emulation boards. The company will begin shipping the systems in October.

-Doug Conner
Arkos Designs Inc, Scotts Valley, CA.
(408) 461-8100.
Circle No. 342

Verify design equivalence without simulation. The Design Verifier tool verifies the functional equivalence of gate- or register-transfer-level (RTL) descriptions. The tool compares RTL to RTL, RTL to gates, or gates to gates. Typical applications include verifying RTL descriptions that have changed to improve synthesis results, testing gate-level implementations against RTL descriptions, and testing gate-level descriptions modified to alter timing or for scan insertion. Because the tool accepts VHDL and Verilog RTL descriptions, it lets you check the equivalence of VHDL and Verilog models.

$85,000. Chrysalis, Andover, MA. (508) 475-7700.
Circle No. 343

VHDL simulator for Unix systems costs <$1000. The $95 entry-level VHDL simulator runs on Sun and HP workstations. The compiled simulator includes an interactive source-level debugger. The software targets self-paced VHDL training and behavioral-model development. Compass Design Automation, San Jose, CA. (408) 433-4880.
Circle No. 344

Complex-function library speeds ASIC design. The MacroWare 2.1 library of 40 royalty-free complex functions comes in gate-level structural VHDL, gate-level Verilog, and EDIF 200 formats. Functions include the M8051 embedded microcontroller, M765A floppy-disk controller, M91C360 data separator, M16C450 UART, M85C30 serial communications controller, M8042 slave peripheral controller, and 82xx peripheral-interface products. The macros include test vectors providing 98% min fault coverage. A single-node library license costs $48,000. 3Soft Corp, Santa Clara, CA. (408) 982-9017.
Circle No. 345

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Software simulates EMC emissions before you build the product. The Compliance electromagnetic-compatibility (EMC) simulator calculates radiated fields due to systems of printed-circuit boards and common-mode currents on cables and enclosures. The tool is fully integrated into the company's other signal-integrity tools. Quantic Laboratories Inc, Winnipeg, MB, Canada. (204) 942-4000.
Circle No. 348

Design tool improves communication between schematic and PCB-board designers. The Placement and Critical Route (PCR) 386+ tool lets you optimize placement and packaging of PC-board components before layout. The tool lets you move easily between schematic and physical-board form, letting you communicate critical information to the person who lays out the PCB. You can also review PCB-board-layout data from the board designer. The software lets you reuse sections of board designs as modules, so that you can pass them directly to the layout person. The introductory price for PCR 386+ is $995. OrCAD, Beaverton, OR. (503) 671-9500.
Circle No. 347

DSP block-diagram simulator offers real-time simulation. The Hypersignal for Windows Block Diagram simulation software lets you run DSP algorithms designed with the tool on DSP boards. The software combines graphical programming with real-time algorithm-performance evaluation, speeding design development. The price for the software with real-time support ranges from $1495 to $7995. Hyperception, Dallas, TX. (214) 343-8525.
Circle No. 346

ASIC-test tool integrates front-end hardware synthesis and back-end test generation. The ASICtest family of test-automation products includes three tools. Icrambist generates register-transfer-level (RTL) code for built-in self-test (BIST) of memories, including the BIST controller and any required memory interface logic. JTAGsyn generates the RTL code for
an IEEE 1149.1-compliant module incorporating the test-access port (TAP), the boundary-scan chain, all the I/O cells, and the call to the core module. ICscanTest performs scan chain insertion, scan rule-checking, combinational test-pattern generation, and fault simulation. The tools begin at $25,000. Logic Vision Software Inc, San Jose, CA. (408) 453-0146. Circle No. 349

Tool provides standard communication links for design data under Windows and Windows NT. Version 4.0 of EDA-Bridge provides BridgeSpeak integration technology that allows design tools from multiple vendors to interoperate under Windows and Windows NT. Prices start at $1495. EDA CAD TEAM Ltd, San Jose, CA. (408) 437-1313. Circle No. 350

Design kit simplifies timing analysis and verification of Pentium-based designs. The Pentium design-analysis kit works with Intel's Design Guide. The kit helps you perform timing analysis and verification on a wide range of Pentium-based designs. The tool provides timing verification across PCI, EISA, and Pentium host buses. $6000. Quad Design, Camarillo, CA. (805) 988-8250. Circle No. 351

Tool optimizes analog-circuit performance. The Paragon analog circuit optimizer lets you improve circuit performance at both the system (behavioral) and the component levels. For example, the software finds parameter values for an active filter design, satisfying center frequency, bandwidth, and gain. The tool iteratively and automatically changes design parameters to home in on an optimum solution. You can also use the tool while altering circuit parameters by interactively exploring circuits as the tool provides graphical feedback. Paragon will be available in July and costs $1900 on PCs and $3900 on Sun workstations. Also available is a suite of analog- and digital-simulation and programmable logic-synthesis tools that run under Windows 3.1 and NT. MicroSim Corp, Irvine, CA. (714) 770-3022. Circle No. 352

Electronic conferencing software speeds communication. The Electronic design-for-manufacture (DFM) conferencing software helps users of the company's DFM tools communicate effectively with work locations. The software lets you share real-time workstation-based DFM applications over Transfer Control Protocol/Internet Protocol (TCP/IP) networks using 9.6- to 19.2-kbps bandwidth lines. The program requires no additional hardware or software, and it supports 10 remote stations and one host in a single conference. The software will be available in the third quarter and costs $3500 for the host conferencing port and $4500 for each remote conferencing station. AT&T Design Automation, Holmdel, NJ. (800) 336-5256. Circle No. 353

Tool analyzes signal integrity and ground bounce. The Presto signal-integrity simulation software works with the Sprint simulator to analyze circuit boards. The simulator evaluates thousands of transmission lines and inductors in minutes, even when using complex models of pin-grid-array-package ground planes. The software runs on workstations; prices start at $45,000. Anacad EES, (408) 954-0600. Circle No. 354

SHORTS

TangoPRO Version 2.2 for pc boards ($5950), Schematic ($995), and Route ($5,500) are available and run under Windows. Accel Technol­ogies Inc, (619) 554-1000. Circle No. 355

VHDL Editor ($2000) is a context-sensitive description-language editor that includes syntax error checking and a multivendor synthesis-subset-checking tool for VHDL. Vantage Analysis Systems Inc, (510) 659-0901. Circle No. 356
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Regulators supply high current with low dropout. Two families of pnp-based medium- and high-current low-dropout regulators feature maximum dropout voltages of 450 mV at room temperature, 300 mV typ. The company guarantees that all of the regulators operate with <600 mV dropout over worst-case temperature extremes. All are available in 3.3, 5, and 12V fixed-and-adjustable-output versions. The MIC2920A/37A/40A ($1.14 to $1.65 for the 3.3V versions (100)) supply 450, 750, and 1200 mA, respectively; the MIC29150/300/500/750 ($1.93 to $8.33) supply 1.5, 3, 5, and 7.5A, respectively. Package options include the 3-pin TO-220 and the 5-pin TO-220 and TO-263.

MPEG decoder handles system tasks. The ZR36100 provides video decoding and system operations for an MPEG I data stream for <$30. The device separates the video and audio signals in the MPEG bit stream, provides the audio data to an external decoder and synchronizes that audio with decoded video. The decoder handles data rates as great as 5 Mbps, suitable for SIF-resolution format images. A $1995 evaluation board is also available. Zoran Corp, Santa Clara, CA. (408) 944-0800. Circle No. 372

Video decoder includes Digicipher II. The CL9100 RISC-based programmable video decoder handles four decompression algorithms: MPEG I, MPEG II main and simple profiles, and General Instruments’ Digicipher II. The chip handles CCIR 601 resolution, provides video and audio synchronization, extracts user data from the bit stream, and supplies decoded video in YCrCb format. A companion device, the CL9110, demultiplexes the audio and video data streams. Each chip costs $35 in quantity. The CL9100 is available now, and the CL9110 will be available for sampling in the third quarter. Cube Microsystems, Milpitas, CA. (408) 994-8300. Circle No. 374

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100-nsec comparators have rail-to-rail inputs. The MAX941/942/944 comparators each consume <35 µA. The outputs pull within 0.4V of either supply rail without external pullup circuitry, and all I/O pins can withstand continuous short circuits to either rail. The comparators incorporate internal hysteresis, and the single 941 also includes a latch and a 12-µA shutdown feature. The devices come in 8- and 14-pin DIPs and SOICs; prices start at $1.40 (1000). Maxim Integrated Products, Sunnyvale, CA. (408) 737-7600. Circle No. 375

High-voltage driver has 64 channels. The HV57708 driver IC operates from 5V, provides output voltages up to 80V, and sources and sinks up to ±15 mA/channel. The cascadable, serial-to-parallel converter IC has four simultaneously clocked shift registers that allow for a 32-MHz equivalent data-throughput rate. Features include output blanking, latch enable, and polarity reversal. $5.18 (1000). Supertex Inc, Sunnyvale, CA. (408) 744-0100. Circle No. 376

Crosspoint switch targets video designs. The MT88V32 IC comprises 32 T switches in a digitally programmable, 8×4 nonblocking array. The IC features a 200-MHz bandwidth and a digital control interface within maximum setup and hold times of 150 nsec. Differential phase and gain errors are typically 0.05% and 0.1%, respectively. The IC interleaves analog signal lines with ground lines, which improves isolation and limits crosstalk. $11.54 (1000). Mitel Semiconductor, Kanata, ON, Canada. (613) 592-2122. Circle No. 377

SCSI terminator reduces power to 90% of passive components. The UC5613 9-line active terminator features a 3-pF channel capacitance. The IC meets all SCSI requirements and features a disconnect mode that reduces quiescent current to 10 nA. The IC features a 400-mA sink/source regulator, a low-dropout regulator of 0.7V, thermal shutdown, and current limiting. $2.16 (1000). Unitrode Integrated Circuits, Merrimack, NH. (603) 424-2410. Circle No. 379

PCI chip sets target all levels. The 82420 PCIset family provides a range of options for creating 486-based PCI local-bus PCs. The EX chip set for 486 CPUs packs dynamic RAM control, cache control, Integrated Device Electronics control, and power management into a 2-chip set for low cost ($25.20, 10,000). The 3-chip ZX chip set adds all standard ISA-bus signals and a data path unit with write buffers. It also optimizes its interface for the DX4 processor ($38.50). Intel Corp, Folsom, CA. (800) 628-2283. Circle No. 380

HDD read-channel IC fits small forms. The IMP62C540 read-channel IC runs at 5V and handles data rates to 40 Mbps. The IC includes a servo controller with serial addressing to reduce I/O pin count. The device comes in a 64-
pin TQFP and costs <$9 in large quantities. International Microelectronic Products Inc, San Jose, CA. (408) 432-9100. Circle No. 382

LED emits white light. The WhiteLED surface-mount LED with white-light emission offers blue, green, and red light sources on board. Simultaneously illuminating all three sources creates a white light. Illuminating the light sources separately or in pairs creates any color in the spectrum—from yellow to purple. $2 (10,000). Siemens Components Optoelectronics Division, Cupertino, CA. (408) 725-3508. Circle No. 383

Synchronous pipelined burst SRAMs for Pentium and Power PC µPs. The KM732V588 and KM732V592 static RAMs (SRAMs) are for the Pentium and PowerPC cache memories, respectively. The 1M-bit synchronous SRAMs have two stages of data and address pipelining. The units sample all data, address, and control inputs, and all outputs are valid at the positive-going system-edge clock. The SRAMs have a 32,768x32-bit organization and have internal data, address, and control latches. Price is $22 each for 66-, 60-, or 50-MHz versions. Samsung Semiconductor Inc, San Jose, CA. (408) 954-7000. Circle No. 384

CPLD runs at 143 MHz. The CYC371 version of the vendor’s Flash370 complex programmable-logic devices (CPLDs) has 32 macrocells and an 8.5-nsec worst-case propagation delay. The flash CPLDs implement an advanced programmable interconnect matrix for routing signals between logic blocks. The devices also offer a product term matrix, which lets you individually route product terms to macrocells. The 143-MHz CY7C371 is available in 44-pin PLCC packages and costs $31.50 (100). Cypress Semiconductor Corp, San Jose, CA. (408) 943-2600. Circle No. 385

Decoder provides JPEG in single chip. The M65700 IC provides 30-frame/sec compression and decompression using the JPEG standard of images as large as 9640x480 pixels. It includes color-space conversion for the YUV, RGB, and CMYK spaces and handles raster-to-block data conversion. The device holds both default and programmable Huffman and quantization tables and provides an on-chip DMA controller for fast bus access. The sample price is $300. Mitsubishi Electronics America Inc, Sunnyvale, CA. (408) 730-5900, ext 2106. Circle No. 386

LCD controller handles video overlay. The Mustang family of LCD/flat-panel controllers provides a 256x16-color palette, a 24-bit DAC, and a video input port. The devices can simultaneously display on CRTs and monochrome...
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or color LCDs, plasma panels, and electroluminescent panels. The 65540 and 65545 are pin- and software-compatible; the 65545 has a hardware accelerator for Windows. Prices are $24 and $31, respectively (10,000). Chips and Technologies Inc, San Jose, CA. (408) 434-0600. Cirde No. 387

DSP family grows. The MDSP2020 and MDSP2021 DSPs for notebook computers provide audio-speed DSP with a 3.3V supply. They also offer sleep and suspend operating modes. The devices offer 20 kbytes of program and data memory; the 2021 allows for external memory. Their prices are $31, respectively ($10,000). Chips and Technologies Inc, San Jose, CA. (408) 434-0600. Cirde No. 388

Chip set speeds MIPS design. The Rabbit chip set provides an interface between the R4000 MIPS processor and the 486 processor bus. Designers can use the chip set to create systems having peripherals for the ISA architecture. The 2-chip set includes the interface device and a dynamic-RAM controller. The set operates at 67 MHz at 3.3V but includes a 5V interface buffer. Samples will be available in the fourth quarter for $120. NEC Electronics Inc, Mountain View, CA, (800) 366-9728. Circle No. 389

Flash version of the 22V10 is available. The ATF22V10B family, electrically erasable flash versions of the 22V10 PLD, offers 7.5- to 25-nsec speeds. The family is plug-compatible with other 22V10 CMOS and bipolar devices. The devices are available in 24-pin PDIP and CERDIP, plastic SOIC, and PLCC packages. 7.5-nsec version, $11.45 (100).Atmel Corp, San Jose, CA, (408) 441-0311. Circle No. 390

Staggered I/O pads available for gate arrays. Staggered I/O-pad placements for the vendor's AMIGxS family of gate arrays are available. The gate arrays are based on the company's 0.8-µm and triple-metal CMOS process that provides a sea of gates. For a design requiring 208 pad locations, the staggered I/O technique realizes a 39 percent savings in silicon area. Gate array prices for various options range from <$5 to $25. American Microsytems Inc, Pocatello, ID. (208) 233-4690. Circle No. 391

FPGAs have 500-µA standby current. The AT6002 and AT6005 field-programmable gate arrays (FPGAs) have 2000 and 5000 usable gates, respectively. The devices also offer thousands of registers for pipelining, 250-MHz toggle rates, and <1-nsec guaranteed clock skew. The devices also offer a 500-µA max standby current. The devices' T6000 cache logic is the rough equivalent of the cache memory used in µP designs. The AT6002 costs $16; the AT6005, $272 (5000). Atmel Corp, San Jose, CA. (408) 441-0311. Circle No. 392

Triple-video op amp has 125-MHz unity-gain bandwidth. The HA5013 IC contains three current-feedback op amps with 0.07-dB to 20-MHz gain flatness for RGB video and 0.03° differential phase and 0.03% gain at ±5V for composite video. Slew rate is 475 V/µsec at a gain of +2. Typical quiescent current is 7.5 mA/amplifier, and output current into a 150Ω load is typically 20 mA. In 14-pin DIPs and SOICs, the IC costs $3.50 (1000). Harris Semiconductor, Melbourne, FL. (800) 442-7747, ext 7219. Circle No. 393

Modem chip set suits audio applications. The CL-MDI414BA chip set comprises three chips that combine a data, fax, and voice modem with a sound card. Adding a 32-kbyte static RAM provides complete modem functionality. The audio suits multimedia presentations. On-chip DMA increases the audio sampling rate and offloads the host µP. The chip set supports all the popular standards for data, fax, and voice modes, including V.32bis. $60 (1000). Cirrus Logic Inc, Fremont, CA. (510) 623-8300. Circle No. 394
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ATM comes to VME systems. By connecting to a DS3 telephone service, the CVME901 board brings asynchronous-transfer-mode (ATM) communications to VME systems. The board offers a hardware-based ATM adaptation layer (AAL) that handles packet segmentation and reassembly for service categories AAL 3/4 and AAL5. An on-board 1960 processor handles congestion control, error checking, and the host interface. The board's DMA controller handles data transfer at up to 8 Gbytes/sec, ensuring that the card can handle communications traffic at the DS3 link's full speed. Price is $4597 (100). Cyclone Microsystems, New Haven, CT. (203) 786-5536. Circle No. 317

VME module hosts Alpha RISC processor. The VMEAlpha64/SP, a 2-board module, is based on the 150-MHz Alpha AXP processor. The design separates the CPU, its local memory, and secondary cache from the VME I/O channel to avoid interference. The module offers a 512-kbyte secondary cache, 128-Mbyte main memory, and a variety of peripheral interfaces, including Ethernet and SCSI. An 960 CPU is available as an optional I/O coprocessor. With the DEC OSF/1 operating system and a 1-Gbyte SCSI disk, the board costs $16,875. Aeon Systems Inc, Albuquerque, NM. (505) 828-9120. Circle No. 318

Adapter boards provide fast I/O. Working with standard peripheral and network interfaces, the 6U MVME-325XT and MVME686-120 boards provide high-speed I/O capability to the VMEbus. The 325XT ($3600) is a Fast SCSI-2 host adapter that handles as many as 14 devices, providing a 10-Mbyte/sec synchronous data-transfer rate on each of two independent channels. The 385-120 ($6895) uses dual 32-bit-wide static RAM (SRAM) buffers and dual-ported video RAM (VRAM) to match its memory I/O to the speed of its FDDI (fiber distributed data interface) port. The board can transfer data at up to 120 Mbytes/sec from SRAM, 60 Mbytes/sec from VRAM, and 50 Mbytes/sec from the VME interface to the FDDI. Prices start at $3245. Motorola Computer Group, Tempe, AZ. (800) 739-1107. Circle No. 319

Flash-memory board provides fault tolerance. Fitting in a single 6U VME slot, the RM250 board provides as much as 128 Mbytes of static RAM (SRAM) or flash memory. Two RM250 boards work in parallel to provide fault tolerance by automatically duplicating memory writes to one board on the other board and providing a software disable command. The board's non-volatile memory works with either 5 or 12V flash memory or SRAM backed by two on-board lithium batteries. A control-status register reports battery failure. Prices start at $1393. RAMix Inc, Chatsworth, CA. (818) 349-6772. Circle No. 320

Board boosts performance with 68060 CPU. The PT-VME161 carries a 68060 CPU, which provides a 250% performance boost while retaining software compatibility with previous 68040 versions. It also offers a Fast SCSI-2 interface with DMA, dual serial I/O ports, and a 60-Mbyte/sec VME64-bus interface. The board's memory capacity ranges from 4 to 64 Mbytes. Prices start at $3245. Performance Computer, Rochester, NY. (716) 256-0200. Circle No. 321

Frame-grabber board handles rough environments. Designed for military and rugged commercial environments, the SVM/DMV-674 frame-grabber board provides the front end to a digital imaging system. It handles 525-, 675-, or 875-line interlaced frame formats with images as large as 1280×1024 pixels. The image-acquisition section provides three monochrome analog input lines sampled at 35M samples/sec to 8-bit resolution. It also offers a 16-bit digital input port. The board comes in six software-compatible versions for diverse environmental conditions and ranging from air-cooled commercial to conduction-cooled full MIL-SPEC ratings. Prices start at $6522. DY 4 Systems Ltd, Campbell, CA. (408) 377-9822. Circle No. 322

Synchro/resolver accurate to 2 arc-minutes. Handling as many as four channels of synchro or resolver rotational-position-transducer signals, the MPX5000 and 501 VME boards offer an accuracy of ±2 arc-minutes. Each channel is programmable for 10-, 12-, 14-, or 16-bit resolution and offers an 8-bit turns counter. The boards track input signals to 15 rps with 16-bit resolution and to 960 rps with 10-bit resolution. Prices start at $2500. Pentland Systems Ltd, Danville, CA. (510) 736-5113. Circle No. 323

Single-board computer runs Basic. Based on the 8032 processor, the ANC-3052B module allows designers to create applications programs in Basic. The module offers a 32-kbyte RAM bank and sockets for as much as 64 kbytes of PROM in addition to the Basic interpreter in ROM. The board includes two external interrupts, two counter/timers, and eight digital I/O lines, along with a 20-pin adapter that can be wire-wrap configured to meet the I/O signal's pinout needs. The board costs $198 and is available with Basic for $146. Antona Corp, West Los Angeles, CA. (310) 473-8955. Circle No. 324

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500-pg temperature-measurement guide includes technical data. This free guide includes more than 1000 g of technical data and specifications and application data on thermocouples, RTDs, connectors, panels, and instrumentation. Thermo Electric, Saddle Brook, N.J. Circle No. 325

PCMCIA developer's guide. Guide gives comprehensive overview of the Personal Computer Memory Card International Association (PCMCIA) standard, along with design examples and reference materials. The 450-pg book also includes directories of PC Card, host computers, and desktop host adapters, as well as listings of ICs, development tools, and software. $89.95. Syecard Technology, Sunnyvale, CA. Circle No. 326

Application selector guide. This application guide details an extensive line of high-performance adhesive compounds for tacking wires and attaching components to printed wiring boards. The publication details 1- and 2-component epoxies, UV-curable epoxies, reactive acrylics, and hot-melt and cyanoacrylate adhesives. Master Bond Inc, Hackensack, NJ. Circle No. 327

Hot-pluggable connector catalog. The publication contains complete technical, performance, and design information for a SMPS-compatible connector and its contacts, including ac, dc, logic, signal, and hot plug. The catalog also includes photos and dimensional drawings. Elcon Products International Co, Fremont, CA. Circle No. 328


Fiber-optics catalog. A new 132-pg catalog features performance information and technical specifications on a line of fiber-optic connectors and adapters, as well as cable assemblies, termination tools, fiber-optic switches, and premise-wiring products. The catalog also includes a glossary and a section describing connector-termination procedures, including tooling required. Molex Inc, Lisle, IL. Circle No. 330

High-power dc/dc converter catalog. This catalog introduces mountable and plug-in 100W dual-output dc/dc converters, transformers, and inductors. The dc/dc converter section details more than 1100 standard models with output voltages up to 1000V dc. This 136-pg catalog also offers an ac/dc power-supply section with linear and switchers in single, dual, and triple outputs. Pico Electronics Inc, Mount Vernon, NY. Circle No. 331

ISRs catalog. This catalog includes a new family of small, easy-to-use integrated switching regulators (ISRs) and a line of dc/dc converters. The 32-pg publication has complete product information, specifications, photos, and schematics on each power module; it also includes a section on product operation, applications, and special considerations. Power Trends, Batavia, IL. Circle No. 332

Catalog of passive components. This 96-pg catalog presents specifications and outline drawings on a variety of passive components in the frequency range of dc to 18 GHz. Commercial, industrial, and military components in the publication include fixed and tunable filters; fixed, high-power, programmable, and variable attenuators; high-power loads; SPDT, SP4T, and SP8T programmable switches; and built-to-order switching and control, rack-mountable subsystems. Trilithic, Indianapolis, IN. Circle No. 333

User-input device-data book. A data book for custom and standard user-input devices is available for system designers. The literature contains protocol descriptions, scan-code listings, schematics, and detailed application notes on an extensive set of encoder ICs. Also included are a recommended matrix layout for types of keyboards or keypads. For those designing low-power systems, the data book provides techniques to produce low-power keyboards. US AR Systems, New York, NY. Circle No. 334

Brochure describes ESD test system for ICs. This free brochure details systems for testing to MIL-STD 883c, according to a number of models, as well as latch-up testing according to JEDEC standards. KeyTek Instrument Corp, Wilmington, MA. Circle No. 335

Electronic-hardware catalog. A 204-pg, electronic-hardware catalog offers specifications for circuit-board spacers, captive panel screws and retainers, standoff, chassis and cabinet handles, shoulder screws, and more. RAE Electronic Hardware, Seymour, CT. Circle No. 336

Catalog covers DSP hardware, software, and development tools. This free 134-pg catalog describes boards, boxes, systems, operating systems, design software, and development tools. Sonitech International Inc, Wellesley, MA. Circle No. 337

Product handbook. A 320-pg catalog describes the company's line of data-acquisition and imaging products. The handbook highlights software solutions, from programming tools to applications, and includes technical tutorials and products that help you choose the optimum solution for data-acquisition and imaging applications. Free. Data Translation, Marlborough, MA. Circle No. 338

Preview of microterminals. The catalog details small, rugged microterminals designed as operator-interface/control panels and data-collection terminals; it also contains specifications, photos, and information on key features and applications. Burr-Brown Corp, Tucson, AZ. Circle No. 339
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<thead>
<tr>
<th>Company</th>
<th>Page</th>
<th>Circle</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADPI</td>
<td>150</td>
<td>236</td>
</tr>
<tr>
<td>AMP Inc</td>
<td>92-93</td>
<td>104</td>
</tr>
<tr>
<td>AT&amp;T Microelectronics</td>
<td>12</td>
<td>49</td>
</tr>
<tr>
<td>Accel Technologies Inc</td>
<td>129</td>
<td>47</td>
</tr>
<tr>
<td>Advanced Micro Devices</td>
<td>46-47</td>
<td>46</td>
</tr>
<tr>
<td>Advim Systems</td>
<td>149</td>
<td>230</td>
</tr>
<tr>
<td>Allegro Microsystems</td>
<td>66</td>
<td>200-203</td>
</tr>
<tr>
<td>Allied Electronics</td>
<td>39</td>
<td>107</td>
</tr>
<tr>
<td>Altia Inc</td>
<td>38</td>
<td>97</td>
</tr>
<tr>
<td>Analog Devices Inc</td>
<td>77-84</td>
<td>231</td>
</tr>
<tr>
<td>Annabooks</td>
<td>151</td>
<td>231</td>
</tr>
<tr>
<td>Atmel Corp</td>
<td>C3</td>
<td>48</td>
</tr>
<tr>
<td>Burr-Brown Corp</td>
<td>62-63185-196</td>
<td>71</td>
</tr>
<tr>
<td>CEIBO</td>
<td>148</td>
<td>255</td>
</tr>
<tr>
<td>Capilano</td>
<td>150</td>
<td>232</td>
</tr>
<tr>
<td>Computing Systems</td>
<td>144</td>
<td>108</td>
</tr>
<tr>
<td>Capital Equipment Corp</td>
<td>37</td>
<td>37</td>
</tr>
<tr>
<td>Cherry Semiconductor</td>
<td>148</td>
<td>233</td>
</tr>
<tr>
<td>Cirnex</td>
<td>151</td>
<td>231</td>
</tr>
<tr>
<td>Compass</td>
<td>123</td>
<td>65</td>
</tr>
<tr>
<td>Design Automation</td>
<td>151</td>
<td>234</td>
</tr>
<tr>
<td>Cypress Semiconductor</td>
<td>15</td>
<td>17</td>
</tr>
<tr>
<td>DSP</td>
<td>2</td>
<td>109</td>
</tr>
<tr>
<td>Data I/O Corp</td>
<td>149</td>
<td>235</td>
</tr>
<tr>
<td>Data Translation Inc</td>
<td>48</td>
<td>66</td>
</tr>
<tr>
<td>Dataman Programmers</td>
<td>149</td>
<td>237</td>
</tr>
<tr>
<td>Datel Inc</td>
<td>149</td>
<td>260</td>
</tr>
<tr>
<td>Digi-Key Corp</td>
<td>64-65</td>
<td>69</td>
</tr>
<tr>
<td>Digital Equipment Corp</td>
<td>106</td>
<td>71</td>
</tr>
<tr>
<td>Ecliptek Corp</td>
<td>74</td>
<td>3</td>
</tr>
<tr>
<td>Frequency Devices Inc</td>
<td>68</td>
<td>72</td>
</tr>
<tr>
<td>GE Rental/Lease</td>
<td>147</td>
<td>238</td>
</tr>
<tr>
<td>HJJI Co Inc</td>
<td>119</td>
<td>4</td>
</tr>
<tr>
<td>Harris Semiconductor</td>
<td>105</td>
<td>73</td>
</tr>
<tr>
<td>Hyundai</td>
<td>10-11</td>
<td>74</td>
</tr>
<tr>
<td>Electronics Industries</td>
<td>96</td>
<td>76-77</td>
</tr>
<tr>
<td>IEE</td>
<td>149</td>
<td>261</td>
</tr>
<tr>
<td>ITT Pomona Electronics</td>
<td>147</td>
<td>239</td>
</tr>
<tr>
<td>Incredible Technology</td>
<td>151</td>
<td>240</td>
</tr>
<tr>
<td>Innovative Software Design Inc</td>
<td>53</td>
<td>75</td>
</tr>
<tr>
<td>Integrated Device Technology Inc</td>
<td>107</td>
<td>110</td>
</tr>
<tr>
<td>Integrated Technology Inc</td>
<td>6-9</td>
<td>36</td>
</tr>
<tr>
<td>Intel Corp</td>
<td>148</td>
<td>241</td>
</tr>
<tr>
<td>Interactive CAD Systems</td>
<td>57</td>
<td>17</td>
</tr>
<tr>
<td>Intusoft</td>
<td>151</td>
<td>242</td>
</tr>
<tr>
<td>Ironwood Electronics</td>
<td>38</td>
<td>3</td>
</tr>
<tr>
<td>Jeta Power Systems</td>
<td>94</td>
<td>78</td>
</tr>
<tr>
<td>Linear Technology Corp</td>
<td>148</td>
<td>243</td>
</tr>
<tr>
<td>Link Instruments</td>
<td>127</td>
<td>79</td>
</tr>
<tr>
<td>Logical Devices</td>
<td>149</td>
<td>244</td>
</tr>
<tr>
<td>Lorad Data Systems</td>
<td>138</td>
<td>80</td>
</tr>
<tr>
<td>Massteck</td>
<td>83</td>
<td>105</td>
</tr>
<tr>
<td>Maxim Integrated Products</td>
<td>101</td>
<td>26</td>
</tr>
<tr>
<td>Mentor Graphics</td>
<td>36</td>
<td>34</td>
</tr>
<tr>
<td>Metalink Corp</td>
<td>151</td>
<td>256</td>
</tr>
<tr>
<td>Microchip Technology Inc</td>
<td>4</td>
<td>38</td>
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<td>79-79</td>
<td>91</td>
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<td>Semiconductors Inc</td>
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<td>55</td>
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<td>56</td>
<td>31</td>
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<td>98-99</td>
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<td>149</td>
<td>251</td>
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<td>137</td>
<td>115</td>
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<td>149</td>
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</tr>
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<td>99</td>
<td>96</td>
</tr>
<tr>
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<td>150</td>
<td>253</td>
</tr>
<tr>
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<td>147</td>
<td>254</td>
</tr>
</tbody>
</table>

Recruitment Advertising 152-154

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RELAYS ARE LIKE OYSTERS, YOU'VE GOT TO LOOK BENEATH THE SURFACE TO FIND THEIR REAL VALUE.

Call us at 1-800-62-OMRON.
They took 90 pounds of power to new heights, and redefined the meaning of performance.
Atmel also offers championship performance. We married our 3-volt proprietary process with a four-megabit Flash so you can take your design to new heights.
The AT29LV040 is not some stripped-down version. It has all the stuff you’ve come to expect from Atmel’s 3-volt Flash memory. A single power source for both read and write. The world’s easiest algorithm, just load and go – there’s no erase cycle. Small memory sectors for fast and easy reprogramming.
And, for you folks who are not working on carry-on equipment, we also make a 5-volt-only version of our four-megabit Flash, the AT29C040.
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Signal's International Flathead Circles The Globe.

The whole world's going flat out for Signal's International Flathead transformers, because we went all out to win international approval.

These super rugged, low profile transformers, fully encapsulated and hermetically sealed, meet UL, CSA, VDE, IEC and EN standards for international use.

Thanks to their extremely low profile, these IF series transformers are ideally suited for use on densely packed PC boards. Available in 2VA to 30VA configurations, these Flatheads feature dual primaries (115/230V, 50/60Hz) and non-concentric windings. The result: reduced inter-winding capacitance and the elimination of electrostatic shielding.

- Low profile (as low as 0.69")
- Precise pin alignment for drop-in applications
- Class B insulation (130°C)

For more information on Signal's International Flathead Series, contact Signal Transformer, 500 Bayview Ave., Inwood, NY 11696.

Sampling of products offered. A total of 80 part numbers are available off-the-shelf in 2, 4, 6, 10, 14, 18, 24, 30 VA sizes.

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