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OVERALL PERFORMANCE

Engineering & Distribution Survey
Electronic Engineering Times 1993

<table>
<thead>
<tr>
<th>Company</th>
<th>Performance</th>
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<tr>
<td>DIGI-KEY</td>
<td>90%</td>
</tr>
<tr>
<td>Marshall</td>
<td>53%</td>
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<tr>
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<tr>
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<tr>
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<td>44%</td>
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<tr>
<td>Newark</td>
<td>43%</td>
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</tbody>
</table>

In a recent 'Engineering & Distribution Survey' conducted by Electronic Engineering Times, respondents were asked to evaluate distributors with whom they have done business or were most familiar. The table above reflects the percentage of respondents who rated these distributors as excellent (6.5 responses) on a 6 point scale where 6=excellent and 1=poor in terms of OVERALL PERFORMANCE!

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SPECIAL REPORT

Probing the limits of logic synthesis

Logic synthesis has freed designers from the complexities of gate-level design by converting RTL descriptions to optimized gate-level logic. But ASIC, FPGA, and CPLD designers are still constrained by a dependence on silicon. Designers will need to pay more—not less—attention to layout as silicon densities continue to increase.—Ray Weiss, Technical Editor

DESIGN IDEAS

Digital potentiometer controls LCD bias
Programmable diode biases bridge
Synchronized regulator produces coherent noise
Circuit measures software-execution time
Switching-regulator output goes below $V_{\text{REF}}$
Pulse-width adjuster reverses servo motor

TECHNOLOGY UPDATES

Intelligent power ICs:
Auto applications drive up single chip’s IQ

Power-actuator control becomes more elaborate with higher integration of CMOS logic and MOSFET switching. Concentrating this intelligence and high-current handling in single-chip SMT packages invokes neat power-dissipation techniques.—Brian Kerridge, Technical Editor

Continued on page 7
Belden Bends the Rules...

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March 17, 1994 • 7

PC-based EDA-tool directory

PC-based EDA tools are challenging workstation-based tools for utility and low cost. In our directory, we've identified 83 vendors that offer a broad range of products.—Doug Conner, Technical Editor

Harmonious convergence

EDN sets to the task of naming the exploding market that’s growing out of the convergence of computer, communications, and consumer technologies...How does “C-Quad” strike you?
—Steven H Leibson, Editor-in-Chief

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EDN March 17, 1994 • 11
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TSSI and See Technologies merge to form Summit Design

TSSI, a developer of software for test-program-development and timing-specification tools, is merging with See Technologies, a developer of electronic-system-design-automation (ESDA) tools. The result of the merger is Summit Design, a company that offers both test-development and ESDA tools.

The first ESDA offering from Summit is Visual HDL, a tool for graphically creating and verifying VHDL design. Visual HDL lets you specify a design using text or graphical specifications, such as block diagrams, state diagrams, flow charts, and truth tables. The tool also provides an interactive simulator with a source-level debugger. To simplify debugging, the debugger couples design input and simulation results in a cause-and-effect relationship.

According to the company, beta-site users spend less than one-third the time developing designs compared with text-editor-based VHDL-design methods. Visual HDL is available now for $12,500 running under Microsoft Windows. The company plans to ship a $25,000 Unix version in the first half of this year.

Summit is also introducing Xpert HDL, a VHDL-design-specification and -management tool that focuses on the top-down design of ICs and electronic systems. The tool streamlines the flow between specification, simulation, and synthesis; it includes an IEEE-1076-compliant VHDL parser and text editor that check for syntax errors on-line as you enter code. Xpert HDL also offers predefined templates that speed design of all standard VHDL constructs and let you customize them to enforce uniform coding styles across a design team. The tool makes on-line checks of VHDL to verify its coding for compatibility with Synopsys and Viewlogic synthesis tools. The object-oriented browser lets you traverse the design hierarchy to locate related pieces of code. For example, by specifying a signal, you can see everywhere that signal is driven in the VHDL description. Xpert HDL costs $7500 and will be available in April for Sun workstations.—by Doug Conner

Summit Design, Beaverton, OR, (503) 643-9281.

Workstations go portable

Two new SPARC-based workstations let you take your design work home or on the road. The first, from Sun Microsystems Computer Corp, provides new levels of workstation performance for a portable unit; the other, from Tadpole Technology Inc, is easier to take with you and costs less. Sun’s 13-lb unit has a “lunch-box” configuration; Tadpole’s, at 6 lbs, is a more conventional laptop style. Both are available in color and monochrome versions.

Sun’s Voyager uses a 60-MHz MicroSPARC II processor and delivers performance of 43 SPECint92 and 37 SPECfp92. Tadpole’s SPARCbook 3, with a 50-MHz MicroSPARC processor (the Texas Instruments TMS390S10) provides 26 SPECint92 and 21 SPECfp92. A price difference goes along with the performance difference: Sun’s units cost $10,000 to $15,000; Tadpole’s go for $7500 to $10,000.

Display capabilities reflect the price differences, too. Sun’s portables have 1024×768-pixel (color) or 1152×900-pixel (monochrome) displays; Tadpole’s units have 640×480-pixel displays, but special software lets you emulate workstation displays up to 1280×960 pixels. You can also connect any of the workstations to an external monitor and get a regular workstation display—for example, 1280×1024 or 1152×900 pixels with the Tadpole units, depending on model type.

Sun and Tadpole workstations are similarly configured. The Sun units can have 16 to 80 Mbytes of RAM; Tadpole’s have from 16 to 64 Mbytes. Sun has a 340-Mbyte hard disk; Tadpole offers both 340- and 520-Mbyte removable drives. All the workstations have two PCMCIA slots, allowing use of two Type I or II cards or one Type III device. Tadpole provides a built-in 14.4-kbps data/fax modem; Sun’s modem is an optional PCMCIA card. Sun’s units offer ISDN capability, as does one of Tadpole’s. Tadpole provides Solaris 1.1 or 2.3 software; Sun provides Solaris 2.3.

Tadpole claims the SPARCbook 3 operates for one hour on internal, rechargeable nickel-metal-hydride batteries and five hours from external nickel-cadmium batteries. Sun’s Voyager is more transportable than portable, in that battery operation is the exception rather than the rule. Sun claims system power consumption for the Voyager will be 40 to 50W max and 20 to 25W typ.—by Gary Legg

Sun Microsystems Computer Corp, Mountain View, CA, (800) 821-4643.

Tadpole Technology Inc, Austin, TX, (512) 219-2200.
Service will research electronics end users

The Business Research Group (BRG), a division of Cahners Publishing Company, has launched the Electronics Research Service (ERS), a market-research service for the semiconductor and electronics industries. ERS' first study was on multimedia: It estimated that, for 1994, North American companies will spend $4.8 billion on business and commercial multimedia applications. Other research topics include network integration and wireless communications.

BRG sells research reports that analyze specific markets by surveying OEMs and end users in the electronics and semiconductor industries. Research reports detail end-user buying behavior, captive-supplier applications, market trends, overseas-supplier trends, application development, and technology/industry standards.—by Jim Leonard

Server supports remote Unix access over Internet Protocol

Age Logic Inc has announced XoftWare/32 for Windows, Serial Edition, which is based on the company's Serial ConneXion technology. Serial ConneXion transmits compressed data over Internet Protocol lines, transmits Unix applications over remote and serial phone lines, and permits the access and display of multiple applications from multiple hosts. The software accommodates users who want to use serial-line connections within corporate environments and those who need to access Unix hosts from a PC via modem at a remote site.

XoftWare/32 for Windows is currently in beta testing. The company plans to release the package in April, and versions for Windows NT and for OS/2 will be available in the second quarter. The software comes with Age's Professional Edition utilities, which include a network file manager that manages display and transfer of local and remote files and allows users to print Unix files on local PC printers. XoftWare/32 for Windows costs $245; each supported host system requires Serial Host ConneXion, which costs $125.—by Fran Granville

Chip puts ATM on twisted-pair wire

Handling data rates as high as 155 Mbps, the ML6672 transceiver device connects asynchronous-transfer-mode (ATM) systems to Category 5 twisted-pair wire. The device replaces the fiber-optics drivers and receivers in what would typically be a synchronous-optical-network (SONET) link. The transceiver senses the strength of incoming signals and uses that information to tune an equalization circuit to remove distortions in the signal. It sends signals as far as 100m. Cost is $20 (1000) for the 32-pin plastic leaded chip carrier-packaged transceiver.

—by Richard A Quinnell

Fiber-optic module runs at 1.5 Gbps

The FTR-8510 integrated optical transceiver uses ordinary compact-disk laser diodes and multimode fiber but achieves data rates from 100 Mbps to 1.5 Gbps with a 10^-16 bit error rate. The module uses 0.8W at 5V and includes the optical receiver, a transmitter, and link-control logic. The control logic includes self-test and optical diagnostic circuits, so it can provide status information on power transmitted and received, bias voltages, and transmitter temperature. The module costs $600.

—by Richard A Quinnell

Wireless networks get a boost

In late January, the Electronics Industry Association of Alberta, Canada, selected Wi-LAN's Model 902-20 wireless local-area network (LAN) as best new technology of 1993. Model 902-20 is a 20-Mbps wireless LAN that plugs into conventional network interface cards; the unit handles three times more users than Ethernet can—at a rate exceeding the capability of standard Ethernet cable. For security, the wireless LAN's modulation technique makes radio signals difficult to intercept and decipher. The 902-20's multicode direct-sequence, spread-spectrum-modulation technology results from a partnership between the University of Calgary and AGT Ltd (Calgary, AB, Canada) under a grant from the National Research Council of Canada.—by Jim Leonard

SHORTS

Method and Finisar announce joint-development agreement. Method Electronics has announced a joint-development and license agreement with Finisar Inc to develop a line of high-speed, short-wave, low-cost optical data links. Method Electronics Inc, Chicago, IL, (800) 323-6858.

AMD and Digital announce foundry agreement. Advanced Micro Devices (AMD) and Digital Equipment Corp (DEC) have announced an agreement under which DEC will produce wafers for AMD's Am486 64-bit family at DEC's South Queensferry, Scotland, manufacturing facility. Under the agreement, DEC will use its 0.68-μm process technology. Advanced Micro Devices, Sunnyvale, CA, (408) 732-2400.

VHDL International User's Forum to meet in May. "Enabling the System Design Process" is the theme for the VHDL International User's Forum Spring 1994 Conference. The conference will take place on May 1 to 4 at the Claremont Resort and Spa in Oakland, CA. The conference comprises technical and user sessions on system aspects of conceptualization, design, test, synthesis, and modeling. VHDL International, Menlo Park, CA, (415) 329-0578.
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<th>Description</th>
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<tr>
<td>53C90A</td>
<td>53CF90A</td>
<td>Single-bus architecture; SCSI sequences controlled by hardware state machine to minimize host intervention</td>
</tr>
<tr>
<td>53C90B</td>
<td>53CF90B</td>
<td>Adds pass-through parity for increased system reliability</td>
</tr>
<tr>
<td>53C94</td>
<td>53CF94</td>
<td>Adds split-bus architecture for more flexibility</td>
</tr>
<tr>
<td>53C96</td>
<td>53CF96</td>
<td>Adds support for differential transfers</td>
</tr>
</tbody>
</table>

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Harmonious convergence

The world is rapidly going digital, and a lot of people are spending tremendous amounts of time and energy trying to name the market that's emerging from the convergence of computer, communications, and consumer technologies. I'd like to suggest an appropriate name, so that we can stop wasting time and energy on the name and concentrate on something useful—such as creating more products and services for the market.

Existing products and services that are the early fruits of this great digital convergence include such diverse items as CD players, µP-based televisions, music synthesizers, cellular telephones, digital bathroom scales, and on-line information services, such as CompuServe and Prodigy.

Thus, I submit for your approval the name "C-Quad" to represent the four dimensions of this market: convergence, computer, communications, and consumer. Here are the top 10 reasons for adopting this name:

10. It's a short, 2-syllable word that doesn't mean anything in particular, making it a perfect marketing tool for the '90s.
9. It has a military heritage (predecessors being C&C for "command and control," and C-cubed for "computers, command, and control"), thus satisfying the current requirement to convert military technology for civilian use.
8. It vaguely reminds you of "quadraphonic," a prehistoric C-Quad product.
7. Unlike PCMCIA, it's short enough to remember and much easier to pronounce.
6. It's cryptic enough to make you sound smart when you use it.
5. You can abbreviate it as "C4" to save space (it's ecological) and to look really cool.
4. The 4-D aspect indicates that this technology can take us anywhere in time and space.
3. I lived in Boulder, CO, which was an energy nexus during 1987's Harmonic Convergence, so, having been infused with the energies of that event, I am somewhat of a convergence expert.
2. It's a much better name than anything else currently on the table.
1. And, to help you become accustomed to the phrase, here are a few usage examples: director of C-Quad development, C-Quad engineer, C-Quad market analyst, C-Quad Magazine, VP of C-Quad marketing. I'm sure you get the idea. Use the phrase a bit, and it starts to roll off your tongue. Honest.

OK, with the market's name behind us, let's go forth and work up some really great products to make it take off.

Send me your comments via fax at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241, 300/1200/2400 8, N, 1. From the Main System Menu, enter ss/soapbox and select W to write us a letter.
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- Power down/sleep mode capability
- 3V to 8V operation
- Power SOIC, low thermal resistance packaging
- Programmable on time/start delay
- Excellent for applications that switch or plug into a common bus, hotswap, or SCSI termpower
INTELLIGENT POWER ICs

Auto applications drive up single chip's IQ

BRIAN KERRIDGE, Technical Editor

The idea of microcontrollers and high-current switches sharing silicon in single-chip devices seems both incongruous and unlikely, but, nonetheless, is one direction intelligent power technology is moving. The requirement for this unusual combination follows mainly from automotive applications, which demand increasingly greater logic complexity and power handling coupled with lower cost and component count. Small package size is also a prerequisite, because these applications require the IC to mount inside the power actuator it controls.

Typical auto applications include control of mirrors, seats, windows, and instrument panels, and all require ICs with approximately 60V, 4A rating. Other applications, such as computer peripherals, telecommunications, and consumer products can be equally demanding. For example, disk drive and printer motors also require internal control ICs, and toasters, shavers, and battery chargers need off-line switching ability to 600V.

For many applications, logic circuits consisting of standard gates, shift registers, and latches generally provide adequate intelligence. But as logic density increases to include microcontrollers with EPROM, EEPROM, or masked ROM, these same applications benefit from a new level of sophistication. The ability to program and reprogram intelligent power functions allows the IC to adjust or adapt its control characteristics to match different requirements in the controlled device.

For example, resetting zero offsets or scale limits to counter aging or wear in mechanical parts optimizes performance and extends useful product life. Equally innovative, reprogramming current limits or temperature trips adapts devices to different environments or locations. Alternatively, initial programming in manufacture can adapt the same device to suit a family of models, maybe by programming output stage configuration from eight single-ended drivers, to four half H-bridges, to two full H-bridges. Yet other examples include setting up ICs for left- or right-hand functions in autos, or more simply, as a store for product identity, service, or diagnostic data.

Vendors variously describe their intelligent-power-device families as Smart power, SmartMOS, and Powerlogic. But whatever the family title, BCD is a common label for

SGS-Thomson's H081 technology demonstrator IC combines an ST6 8-bit microcontroller with a 60V, full H-bridge power output stage (R_{D(on)}=0.3\Omega).
INTELLIGENT POWER ICs

the process (bipolar, CMOS, and DMOS technologies combined on the same chip). DMOS (double-diffused MOS) describes a particular form of power-MOSFET switch that exhibits low \( R_{\text{DS(on)}} \) (Ref 1).

Each semiconductor technology in the BCD trio donates its own virtue: Bipolar parts add precision to circuits such as voltage references and current and temperature limits; CMOS parts establish the IC's overall IQ; and DMOS parts furnish output switching and power handling.

To meet user demand for higher logic density and power handling, vendors have moved their BCD processes from 4- to 2.5-µm lithography. Most recently, SGS-Thomson announced a process, labeled BCD3, that uses 1.2-µm line width.

Each line-width shrink yields valuable design gains. For example, at each shrink, not only does logic density multiply by approximately 2.5, but DMOS \( R_{\text{DS(on)}} \) approximately halves. This intriguing \( R_{\text{DS(on)}} \) bonus occurs because a lithography shrink concentrates individual cells that comprise a DMOS conduction channel. More cells in a given area of silicon produce a higher current density and lower resistance.

Currently, vendors' mainstream business runs on a 2.5-µm process, which typically yields a CMOS logic density around 1600 transistors/mm² and 60V DMOS power transistors with an \( R_{\text{DS(on)}} \) of 0.5Ω-mm². In contrast, SGS-Thomson's BCD3 process will yield 4000 transistors/mm² and \( R_{\text{DS(on)}} \) of 0.25Ω-mm².

Power limits feasibility

Although logic density and power handling are key factors, cost and size are of overriding importance in today's intelligent power ICs. At unit volume levels in this type of business, cost is directly proportional to IC die size. In practice, it's the power handling ability you demand from an intelligent power IC, rather than CMOS logic complexity, that mostly governs feasibility and price. In a typical intelligent power IC, bipolar and CMOS sections each occupy 25% of the die, with the DMOS power section taking up the remaining 50%.

Looking ahead

SGS-Thomson Microelectronics is the principal proponent of high-IQ power chips that embody a microcontroller. At present, the company offers samples of an H081 technology-demonstrator IC that includes an ST6 8-bit microcontroller with a 60V, 0.3Ω \( R_{\text{DS(on)}} \), 3A H-bridge power section. The company expects to ship commercial versions—equivalent in complexity to H081 and with on-chip EE-PROM or masked ROM—later this year. The volume price target is approximately $6. SGS-Thomson's further plans reveal that, by 1996, the BCD process will use 0.8- and 0.5-µm lithography. At that stage, you can expect the addition of flash memory and DSP cores to deliver intelligent power ICs a further IQ hike.

The Philips Powerlogic octal low-side driver for automotive applications is a typical example of BCD (bipolar, CMOS, and DMOS) technologies combined in a single chip. Bipolar parts provide precision for supply, references, and current-limiting circuits. CMOS offers logic gates, shift register, and latches. DMOS provides the power-handling elements.
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INTELLIGENT POWER ICs

Although lower $R_{Dc}$ implies greater current handling for a given package size, users’ parallel demand for smaller packages threatens to partly negate this advantage. In addition to lower cost, users now require intelligent power ICs in small-outline (SO) packages, which fit within the actuators they control. To satisfy these demands, vendors have been driven to design new packages and to explore more elaborate mounting techniques (see box, “Knowing what’s watt”).

By concentrating complexity and power-handling ability in this way, product designers, particularly in automotive applications, attain a twofold objective. First, a self-contained sub-assembly simplifies final product assembly, and second, fewer internal and external connections give a significant boost to overall reliability.

Custom designs predominate

The range of vendors’ intelligent-power-ICs divides into various application categories as standard or custom designs. Philips Semiconductor’s BCD Logic range covers mainly standard designs in four voltage ratings: 70, 400, 650, and 700V. Philips’ higher voltage designs address applications in the company’s established lighting, TV, and consumer business. The most recent Powerlogic-70’s 70V, 4A process targets 100% automotive applications.

SGS-Thomson’s Multipower BCD range is a mixture of standard and custom ICs using the company’s 20 to 500V BCD process. Standard ICs include switching regulators up to 10A rating, power-factor-correction controllers, audio power amplifiers, and a range of motor controllers. SGS-Thomson’s custom business majors on computer peripheral applications such as disk-drive and printer motor controls, but it also covers automotive and telecommunications.

Designing a custom BCD IC is very complex. The IC vendor must custom design the devices with the customer’s unique requirements in mind. The designer must consider the voltage, current, and other characteristics of the application, and then choose the appropriate ICs from the vendor’s standard or custom offerings. Once the ICs are selected, the customer must work with the IC vendor to design the mounting scheme and heat sink necessary to dissipate the power generated by the ICs.

Knowing what’s watt

Many intelligent power IC designs use surface-mount variants of otherwise conventional multipin TO-220-style packages. Even though these packages comfortably handle power dissipation up to 20W, they do not suit automatic assembly, nor are they small enough for many new applications. And, even though standard small-outline packages meet the two latter requirements, they cannot dissipate more than 2W at best.

In order to satisfy combined requirements of dissipation, handling, and size, IC vendors have devised new packages and mounting techniques. The main innovation is the inclusion of a copper slug molded into the package and situated beneath the die. Fig A shows a range of mounting schemes that use heat transfer (via the slug) into increasingly larger heat sinks to achieve dissipations of 1 to 18W. Table 1 lists the thermal resistances junction-to-ambient, and power dissipation assuming a 50°C temperature rise above ambient temperature.

Fig Aa and b assume the use of standard fiber-glass resin pc-board material. Fig Ac and d assume insulated metal substrate (IMS). IMS is a 3-layer material consisting of an aluminum or copper plate separated from the etched-copper-foil layer by a thermally conductive dielectric layer.

Fig A-An SMT power small-outline package includes a copper slug. The slug contacts 6 cm² of pc-board copper used as a heat sink (a). A grid of 16 copper-filled holes in the pc-board contact a conventional heat sink (b). An insulated metal substrate (40 cm² replaces conventional pc-board material (c), and an additional heat sink is added (d).
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much a vendor-led activity, although both Philips and SGS-Thomson encourage you to work with them at one of their design centers.

Harris Semiconductor's semicustom cell-based Power ASIC technology allows you more design independence. This 60V, BCD process uses the HPA2000 standard cell library. The process includes scalable lateral DMOS devices rated at 20A, which the company's mixed-signal Fastrack design system supports. Harris also offers a range of standard Power ASIC ICs, including 1-MHz pulse-width-modulation switching regulators and 80V full H-bridge driver for external MOSFETs.

Siliconix also favors using BCD ICs to drive external MOSFETs, particularly for current levels greater than 1.5A. The company believes that partitioning current at this level provides users an optimal cost-to-performance ratio. The principal advantage of external MOSFETs is a wider choice of RDS(on) as the company's range of Little Foot S0-8 power MOSFETs with RDS(on) values down to 60 mΩ demonstrates. Siliconix also contests the view that external MOSFETs preclude the possibilities of mounting control circuits internally. The company's recently released SQFP48 5A 3-phase motor driver with external MOSFETs occupies a 2×1.6-in. pc board and is small enough to fit inside the motor.

Table 1—Dissipation of SGS-Thomson Power SO-20 package (Using different mounting methods in Fig A)

<table>
<thead>
<tr>
<th>Fig</th>
<th>Thermal resistance Junction-to-air (°C/W)</th>
<th>Power dissipation (W)</th>
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<td>a</td>
<td>32</td>
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<td>d</td>
<td>2.8</td>
<td>18</td>
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Note: Dissipation assumes 50°C junction rise above ambient. (Data courtesy SGS-Thomson Microelectronics)
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Interactive EDA
PC-based EDA-tool directory

DOUG CONNER, Technical Editor

PC-based electronic-design-automation (EDA) tools have been nipping at the heels of workstation-based tools for years. Although in many cases, you must still look to the workstation-based EDA tools for leading-edge capabilities, a serious examination of PC-based EDA tools shows that they are not too far behind. Some of the same companies offering workstation-based tools also offer PC-based tools, often with virtually the same capabilities.

If you need the highest speed and the most leading-edge technology, buying a relatively inexpensive PC-based EDA tool may be false economy. Conversely, if you are spending money on Unix-based software and workstations to perform functions that you could perform just as well on a PC at a fraction of the price, you may be wasting money. The only way to make sure you are making the right choice is to occasionally evaluate the EDA tools for both workstations and PCs.

The accompanying table lists as many PC-based EDA-tool manufacturers as we could track down. If you're a user of PC-based tools, the table may bring to light a few companies that you might have overlooked. If you haven't been using PC-based EDA tools, you might want to contact some of the companies offering PC-based EDA tools and try some demonstration programs.

As the table shows, most companies provide free demo software that should give you a good idea of the tools' capabilities but usually doesn't let you enter design data. For a nominal price (deductible from a product purchase), most companies also provide manuals and functional software that has a few limitations, such as the lack of saving and printing capabilities. The functional software gives you a chance to try the software and get a feel for the speed on the computer you'll be using, all with a relatively small investment of time and money.

Many tool vendors suggest that their tools require the use of at least a 386-based computer with 4 Mbytes of RAM. About half recommend that for fast response, you need at least a 486-based computer with 8 Mbytes of RAM. Virtually all analog simulation tools require a math coprocessor, either to operate at all or to simulate circuits of any size. The floating-point computations are too slow otherwise.

When a company offers more than one tool or configuration, the table lists two of that vendor's products. It should also help you determine the companies involved in each category of tools. Keep in mind, though, that most of the categories are relatively general.

For example, the field-programmable gate-array (FPGA)/PLD-design column indicates that the company offers products for some or all of the PLD-design process. The product may map logic into PLDs or perform place-and-route operations for FPGAs. Contact the companies for more detailed information using a reader-service card or by phone.

The table shows prices in individual categories in which the company offers products. The prices are typically starting prices. An “X” indicates that the product category is included in the system-price column or in the price of another product category. The system price does not include optional product categories.

You can reach Technical Editor Doug Conner at (805) 461-9699.

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Looking ahead

Managers are understandably reluctant to bring PCs into a company in which workstations are the standard. Adding an operating system (OS) and electronic-design-automation tools, many of which must communicate with each other, complicate an already-complicated situation. The intertool-communications problem requires careful consideration, but managers shouldn’t assume that the situation will be any more difficult than the problem of passing data between workstation-based tools.

Windows NT or another OS should soon bridge the gap between workstations and PCs. When the bridge becomes real, managers will be able to judge hardware and software on their actual merits and not on whether their companies are PC- or workstation-based.
## PC-based EDA tools

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<th>Category</th>
<th>Package</th>
<th>Schematic capture</th>
<th>PC-board layout</th>
<th>Auto-router</th>
<th>IC layout</th>
<th>FPGA / PLD design</th>
<th>Analog simulation</th>
<th>Transmission line / signal Integrity</th>
<th>Mixed A/D simulation</th>
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46 • EDN March 17, 1994
## Logic simulation Timing analysis HDL synthesis HDL simulation Price Minimum system (µP; Mbytes) Demo software Circle Notes

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EDN March 17, 1994 • 47
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Logic synthesis has freed designers from the complexities of gate-level design by converting RTL descriptions to optimized gate-level logic. But ASIC, FPGA, and CPLD designers are still constrained by a dependence on silicon. Designers will need to pay more—not less—attention to layout as silicon densities continue to increase.

Photo courtesy Synopsys Inc

RAY WEISS, TECHNICAL EDITOR

A few years ago, logic synthesis seemed a first step into a world of higher level design. Back then, designers imagined being able to move higher and higher up the synthesis chain, until they could specify a design behaviorally and just push a button—and the software would do the rest. Nice dream, but not a reality for the '90s.

Why? Because design, even with high-level HDLs (hardware-description languages) and simulation, must eventually meet silicon “reality.” And that reality, especially at submicron or deep-submicron levels (below 0.5 µm L-effective) is not a nice, well-behaved world. Instead, it’s where elegant designs meet the layout monster, where signal interconnects dominate circuit delays, and where signal delays can no longer be described by simple fan-out models or RC trees. And that’s not all: Design rules will migrate down to 0.18 µm by 2002, with chip voltages moving down to less than 1V as well.

But that’s not the only reason for a reevaluation of logic synthesis’s reach. Silicon’s higher densities bring new system-level problems. And these problems need—nay, demand—the designer’s touch. Larger ASICs can be likened to systems, and, similar to systems, must be partitioned for design ease and clocking. And last, hardware design is still hardware design; writing code in VHDL or Verilog, even code that simulates well, does not guarantee working silicon.

Spam in a can

The first generation of American astronauts were tagged “Spam in a can” by test pilots because they were simply passengers and had little control over the actual
flights. Today's astronauts, however, are an integral part of flight planning and control. And, similarly, today's designers must take an active role in the design process.

Software-based design tools will not replace designers. True, you can do more with today's CAE tools, but you cannot actually walk away from design. Now, and in the foreseeable future, there is no substitute for the design engineer. Moreover, the fundamental limit on logic synthesis is the designer: Synthesis tools won't turn a bad design into a good one—or convert a bad designer into a competent one.

In fact, synthesis tools, coupled with HDL design, raise the design stakes. Schematics and gate-level design had built-in safety limits: Schematic drawings imposed discipline on signal connectivity and logic-block grouping, whereas an engineer using an HDL, say Verilog or VHDL, to define a design must internalize that discipline. Even worse, careless code can create logic anomalies that will trash a design. Engineers writing an HDL must be “hardware aware.” For example, in software, the expression B=B+1 carries implicit concepts on timing and computer exe-
Mainstream synthesis-control logic

Today’s engineers use logic synthesis primarily for control logic, optimizing and mapping combinatorial logic (equations) into a netlist—and ready for layout. They also use synthesis to instantiate major RTL components such as registers. Some tools, such as Synopsys’ Design Compiler, Cadence’s Synergy, Exemplar’s Core, and Compass Design’s ASIC Navigator, also enable designers to use module generators and megacell/cell libraries to select the correct element. Megacells can be hefty, including µPs, FPUs, ALUs, and DSPs. In effect, the synthesis tools provide a single interface to specify a design. Some synthesis tools, such as Synopsys’ Design Compiler, Cadence’s Synergy, and the forthcoming Viewlogic ViewSynthesis (was SilcSyn) provide some higher level synthesis capabilities. These capabilities include resource allocation and sharing for key RTL blocks, such as adders or registers.

Mainstream logic-synthesis tools from Synopsys, Mentor, Exemplar, Cadence, and Viewlogic also provide state-machine generators and mappings to optimized state machines. Many engineers find these tools work for general state machines, but, typically, they turn to hand design for highly optimized state machines. Industry consensus seems to say it’s still a bit early for efficient state-machine synthesis. However, engineers can define complex controls by defining multilevel state machines (state machines within state machines, etc); these can be defined with current synthesis tools.

Most synthesis users describe designs with an HDL, such as Verilog or VHDL. However, when using an HDL, it’s easy to lose touch with the design; you can define major RTL blocks with simple statements. Thus, a few lines of code can trigger major effects on a design’s timing or performance. Good logic designers, like master programmers, have to keep foremost in their minds the major flows of their designs, continually monitoring any changes that add, delete, or modify RTL blocks. Yesteryear’s schematics also served as block diagrams, illustrating the major RTL blocks and data flows. With HDL code, however, RTL blocks and their flows may not be obvious. For example, X=A+B+C instantiates two adders fed by three registers, defining a major flow. Yet the statements could be buried in complex control code—there’s no HDL highlighting for RTL definitions or flows.

Finally, writing Verilog or VHDL code does not automatically stop you from violating propagation delays or logic constraints such as setup or hold. Moreover, many constraints are functions of the ASIC process (voltage and temperature) as well as of the signal characteristics (slow or fast edges). Consequently, you cannot realistically estimate these timing delays until floor planning or place and route. You’ll have fewer problems downstream with synthesis if you keep these logic realities in mind when coding. Static timing analyzers can catch timing errors, but it’s far easier to design it right the first time.

Logic synthesis is only a small part of the overall design effort. Most system designs are dominated by their data-paths. Unless you are building a control-logic chip, 60 to 70% of a chip’s logic is made up of RTL blocks. These blocks generally define a chip-level data flow. Creating an optimum chip design generally means building an optimized data-flow path, one made up of these RTL elements and then, to control it, creating the control logic. Most designs move data between two or more bus systems (for example, CPU memory bus to an I/O bus). Even a µP can be seen as consuming two data flows, instruction and data, and outputting another data flow.

These data flows connect RTL blocks. The blocks generally are existing megacells or library elements or are generated via specialized module generators. Even though you can describe them in HDL code, selecting or generating the elements has not typically been a logic-synthesis function per se. However, the range of logic-synthesis tools is expanding to provide a common design interface to other synthesis or compilation tools. Synopsys’ Design Compiler, Cadence’s Synergy, and Intergraph’s ArchSyn, for example, call the appropriate module generators to create RTL blocks, such as memory or registers to meet design constraints; they also select RTL blocks that meet synthesis constraints.
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LOGIC SYNTHESIS

Currently, engineers using Synopsys logic-synthesis tools break designs down into synthesizable partitions. The average partition runs 4000 to 6000 equivalent ASIC gates, with some partitions running out to 10,000 (or more) gates. Other synthesis tools claim larger partitions; these include Viewlogic’s SileSyn (recently acquired from Racal-Redac) and Compass Design’s ASIC Navigator, which does automatic partitioning and is integrated with layout.

Full- and partial-scan test generators are now part of most major logic-synthesis tool sets; they provide ASIC testability. Scan generators are also available from test vendors, such as Sunrise Test Systems (TestGen) and CrossCheck (Aida II). Using scan technology, the active flip-flops in a design partition into sets that form sequential scan chains. These scan chains enable active FF values to be set and shifted in for test or to be shifted out for comparison. Partial-scan techniques link most FFs but leave out critical ones for secondary access.

Scan techniques use a more complex, slower flip-flop element that multiplexes in scan shift data and outputs scan data. Scan test has a number of problems, including a 5 to 15% additional logic overhead, scan-connection inefficiencies (better layout after placement), and ensuring that clock triggers are phased to avoid excess power consumption (all flip-flops firing on a fast edge can ruin a chip).

Silicon reality

Designers should never forget that silicon underlies system- and logic-design processes. Unless designs translate and map into working silicon, the logic is useless. Moreover, the underlying silicon is not a fixed target. Silicon capabilities are continually migrating: Gate realities change; interconnect causes the bulk of a signal delay (up to 80%). Interconnect between logic elements becomes the critical portion for design. Unfortunately, signal-delay estimation is no longer a simple matter, especially on deep-submicron processes where the old standby of lumped RC trees is no

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Looking ahead

Today’s EDA vendors are tailoring tools and environments to user design methods and needs. The vendors are trying to meld their tools into existing design environments and methods. This approach differs from the previous tool generation, which was generally a one-size-fits-all or do-it-your-way or forget-about-it school. However, many tools continue to plug away in splendid isolation, ignoring existing design knowledge and the design process. Good logic and system designers never lose sight of the final silicon—that design is independent of layout. Yet the reciprocal is not true; many tools, especially back-end physical tools, do not try to use existing design knowledge to optimize the silicon.

Today, system design houses are turning to floor planners or prefloor planners to reflect final silicon timing. To minimize hand-off iterations to the foundry, accurate timing estimates and constraints are prerequisites. Similarly, physical layout tools need system design knowledge for effective floor planning, placement, and routing. Critical layout-design data includes which logic elements form RTL entities; the flows between the major RTL blocks; and the overall design data flow from input, to RTL blocks, to outputs. Many back-end tools currently interrogate the design netlists to figure out overall design structure and flow. Common formats and mechanisms are necessary to define and pass this key information to back-end tools.

It’s time for front-end design and back-end layout to cooperate. The design side cannot afford to ignore layout consequences. And it’s silly for physical layout tools to recreate the design rather than rely on top-level design perspectives and flows.
Logic synthesis enables engineers to map their RTL-level designs into ASIC technologies. The problem, however, has been that synthesis takes place on the design side of the house—not the silicon or physical side. It's increasingly difficult for design-side synthesis to build logic to meet design constraints without effective knowledge of the final layout. At 0.5 µm and below, synthesis needs closer ties to silicon layout to predict circuit delays.

There are two approaches to linking synthesis and physical IC design. In the first, the synthesizer provides timing constraints to the physical tools to direct layout, which is called synthesis-directed layout. Additionally, layout estimates are fed back to the synthesis tools to verify timing. Synopsys has taken this tack, defining interfaces to deliver timing constraints (PDEF) as well as interfaces to handle feedback (SDEF). A new version of the Design Compiler, due out soon, has a built-in synthesis “floor manager” that dispatches synthesis constraints to a floor planner and receives back-timing feedback to reoptimize the logic. Physical-tool vendors are working to integrate their products with Synopsys' tools (HLD's Design Planner) and ArcSys' ArcCell.

In the second approach, the synthesizer uses layout algorithms and tools to predict final signal routing. The tools also modify the design netlist to reflect layout needs and signal projections. Cadence takes this approach using its well-established IC tools. The Cadence Synergy synthesis tool set adds Place-and-Route. In PBS, timing is reanalyzed using topology. The synthesizer reoptimizes the design to meet timing constraints. Where needed, it rearranges loads, resizes buffers and gate, relocations, and reduces potential long wire runs. Cadence claims a 10 to 30% overall system improvement using PBS.

Functional- and logic-level simulation have to be supplemented with transistor-level modeling, especially for deep-submicron design. This modeling will have to track signal-edge effects, parasitic effects, and power dissipation. At the higher clock rates, frequency becomes a key factor in CMOS-circuit power dissipation—the faster the clock, the more power burned.

**FPGA/CPLD synthesis**

FPGAs and CPLDs came late to synthesis. Built around proprietary logic blocks (FPGAs) or variations of 22V10 PALs (CPLDs), these chips lend themselves to old-fashioned, 5400/7400 TTL-style, schematic-capture-based design. Early adapters and most FPGA engineers still design that way. However, as logic densities increase, engineers are turning to high-level HDLs and logic synthesis for FPGA and CPLD design.

Logic synthesis for FPGAs and CPLDs has yet to reach ASIC efficiencies. Part of the problem is that mainstream algorithms and techniques were developed for ASIC gate arrays and standard cells with their underlying gate elements. ASIC fine-granularity architectures made it easy to map logic to the base gates using 2-level or multi-level optimizations.

In contrast, FPGAs have a proprietary core-logic block, typically a mix-
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LOGIC SYNTHESIS

The synthesis of combinational logic is a process of converting a set of logic equations into a form that is suitable for implementation on a digital circuit. This process is often performed using logic synthesis tools, which are software programs that automate the process of converting high-level descriptions of digital circuits into low-level descriptions that can be used to generate the actual circuit components.

The process of logic synthesis begins with a high-level description of the digital circuit, such as a set of logic equations or a circuit diagram. The logic synthesis tool then uses a set of algorithms to transform the high-level description into a more detailed description of the circuit, which is then used to generate the actual circuit components.

One common approach to logic synthesis is to use a two-step process that involves creating a network of logic gates, known as a network of logic functions (NOLF), and then transforming the NOLF into a more efficient form, known as a network of multiplexers (NOM), which can be used to generate the actual circuit components.

Logic synthesis tools are typically used in conjunction with other EDA (electronic design automation) tools, such as schematic capture, simulation, and layout tools, to create a complete digital design.

The benefits of using logic synthesis tools include increased design productivity, improved design quality, and reduced design costs. By automating the process of creating digital circuits, logic synthesis tools can help designers to create more complex circuits in less time, with fewer errors, and at lower cost.

However, logic synthesis is not a perfect solution, and there are some limitations to the process. For example, the results of logic synthesis may not always meet the requirements of the original design, and the process can be computationally intensive, which can slow down the development process. Despite these limitations, logic synthesis tools remain an important tool in the design of digital circuits.
logic synthesis

Technology that targets data-path applications (AT&T is a second source for earlier Xilinx parts). AT&T is working on its own advanced module generator that has extensions for RTL blocks and data flow.

Other FPGA competitors include Actel, QuickLogic, and Cypress. Even though these FPGAs are not RAM-based, they are highly routable parts that ease logic-synthesis place and route. Similar to the Xilinx parts, these FPGAs have their own proprietary core-logic blocks (Cypress FPGAs are based on QuickLogic parts). These proprietary FPGA cores, with their special routing resources and priorities, complicate logic synthesis. The Actel

For free information on synthesis-related tools such as those described in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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5. Straussberg, Dan, "Boundary-scan testing," EDN, October 14, 1993, pg 78.

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Digital potentiometer controls LCD bias

Michael Cortopassi, Dauphin Technology, Lombard, IL

Designers of pen-based computers can easily relegate some controls that were previously mechanical, such as switches and potentiometers, to on-screen icons. For example, the circuit in Fig 1 shows one way that digital logic can control the -24V-dc LCD bias using two general-purpose I/O command lines. The DS-1669 from Dallas Semiconductor is a 64-step potentiometer available in 10-, 50-, and 100-kΩ ranges. The up-count (UC) and down-count (DC) pins digitally control the wiper of the potentiometer. A low-going pulse to either of these pins increases or decreases, respectively, the wiper's position on the pot relative to RL. This change in position adjusts the base current in Q1, whose collector connects to the adjust pin on an LM337 negative voltage regulator. By changing the amount of current injected into the LM337's adjust pin, the circuitry simulates having another resistor in parallel with R1, and the voltage output at V_out changes accordingly. Tapping a pen on icons that represent contrast—or other computer functions, including brightness, LCD/CRT and suspend/resume—controls the I/O pins.

![Fig 1](image_url)—To digitally control the -24V-dc LCD bias, this circuit uses a 64-step potentiometer to adjust the base current in Q1.

Programmable diode biases bridge

Patrick J Worcester, KAKM TV, Anchorage, AK

A programmable reference diode, such as the Motorola TL431A, can supply constant-current bias for a silicon pressure-sensor bridge (Fig 1). This circuit is simpler than using an op amp and separate reference diode or than using a current diode, which requires temperature compensation.

The TL431A produces a V_REF of 2.5V over a current range of 1 to 100 mA. The value of V_REF/R2 sets the necessary bias current for the bridge sensor, as specified by the sensor manufacturer. The reference diode current, set by R1 and the supply voltage V_S, usually equals the bridge current. As an example, for a supply of 12V, a reference diode and bridge current of 1 mA, and a bridge impedance of 5 kΩ, R1 should equal 2250Ω, and R2 should equal 2500Ω. The bridge output has a common-mode voltage equal to V_REF plus one-half times the voltage across the bridge.

![Fig 1](image_url)—Using a programmable reference diode is a simple way to supply constant-current bias for a silicon pressure-sensor bridge.
Synchronized regulator produces coherent noise

Jim Williams, Sean Gold, and Steve Pietkiewicz, Linear Technology, Milpitas, CA

By using a gated-oscillator architecture instead of a clocked-PWM one, gated-oscillator-type switching regulators permit high efficiency over extended ranges of output current. This architecture eliminates the housekeeping currents associated with the continuous operation of fixed-frequency designs. Gated-oscillator regulators simply self-clock at whatever frequency is necessary to maintain the output voltage. Typically, loop-oscillation frequency ranges from a few hertz to the kilohertz region, depending on the load.

In most cases, this asynchronous, variable-frequency operation doesn’t create any problems. However, some systems are sensitive to the asynchronous characteristics. The system in Fig 1 slightly modifies a gate-oscillator-type switching regulator by synchronizing its loop-oscillation frequency to the system’s clock. The oscillation frequency and its attendant switching noise, albeit variable, become coherent with system operation.

To analyze the system in Fig 1, temporarily ignore the flip-flop, and assume the circuit directly connects the A_{OUT} and FB pin of the LT1107 regulator. When the output voltage decays, the set pin drops below $V_{\text{REF}}$ causing A_{OUT} to fall. The internal comparator then switches to high, biasing the oscillator and output transistor into conduction. $L_1$ receives drive pulses, and the circuit deposits this inductor’s flyback events into the 100-µF capacitor via the diode, ultimately restoring output voltage. This action overdrives the set pin, causing the IC to switch off until it requires another cycle. This oscillator cycle’s frequency is load-dependent and variable.

Now, interposing a flip-flop into the path between the A_{OUT} and FB pins, as the figure shows, synchronizes the regulator to the circuit-generated clock. When the output decays far enough, the A_{OUT} pin goes low. At the next clock pulse, the flip-flop’s Q_2 output sets low, biasing the comparator-oscillator. This turns on the power switch, which pulses $L_1$, $L_2$ responds in flyback fashion and deposits its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case, except that the flip-flop now synchronizes the sequence of events with the system clock. Although the resulting loop’s oscillation frequency is variable, the frequency and all attendant switching noise is synchronous and coherent with the system clock.

The circuit requires a start-up sequence because the output provides power for the clock. The circuit connects the flip-flop’s remaining section as a buffer to furnish start-up. The flip-flop’s connected CLR, and CLK, lines monitors output voltage via the 221-, 82.5-, and 100-kΩ resistor string. When power is applied, Q_1 sets CLR low, which permits the LT1107 to switch, thereby raising the output voltage. When the output goes high enough, Q_1 sets CLR high, and normal loop operation commences. Although this circuit uses a step-up regulator, the technique also works with other types.

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Fig 1—A synchronizing flip-flop forces the LT1107 gate-oscillator-type switching regulator’s noise to be coherent with the 100-kHz clock.

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### Specifications

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<th>MAX.</th>
<th>MIN.</th>
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<td>−72</td>
<td></td>
<td>−73</td>
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<td>72</td>
<td>75</td>
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<td>dB</td>
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</table>

* f_m = 2.45MHz
Circuit measures software-execution time
Yongping Xia, EBT Inc, Torrance, CA

Especially helpful for developing real-time application programs, the circuit in Fig 1 plugs into a PC printer port and measures the execution time of a piece of software. The CD4536 is a 16/24-bit binary counter with a built-in oscillator. This counter has an 8-bit prescaler, which the chip bypasses if the 8_BY pin is high. When this is the case, the CD4536 is a 16-bit counter, and its A through D inputs select which bit is connected to output DO. If the 8_BY pin is low, the CD4536 is a 24-bit counter and the inputs select which 9 to 24 bits connect to output DO. Setting the R pin high clears the counter, and setting CINH high inhibits the counter. With the components values shown in the figure, the oscillation frequency is around 100 kHz. The printer port can directly power the CD4536 because it needs only several milliamps.

A PC printer port has an 8-bit output port. As Fig 1 shows, D_0 to D_3 select the counter’s output bit, D_4 disables the counter, D_5 sets the bypass function, D_6 resets the counter, and D_7 powers the chip. The printer port uses input pin 11 to read the selected bit off the counter.

Listing 1’s C program controls the test. First, the program finds the PC’s printer port address. This address is its

Listing 1—Execution-time measurements

```
#include <conio.h>
#include <stdio.h>
#include <dos.h>
#include <bios.h>
define RESET_ON Ox40
define RESET_OFF Oxbf
define BYPASS_ON Ox20
define BYPASS_OFF Oxdf
define CLOCK_ON Oxef
define CLOCK_OFF Ox10

int out= OxBO , i, out_port , in_port;  
long in , data;  
float temp, dis;  
type def unsigned int WORD;

teast_procedure ()
{  
    /* your procedure */
}

long get_data(void)  
/* read ctr bit by bit */
{
in=0;
for (i=15; i=1; i--)  
{  
    in=2;
    outportb(out_port, outr);  
    delay();
    if ((inportb(in_port) & Ox80)>>0)
    {  
        in++;  
    }
    return in;
}

void clear_counter()  
/* clear ctr */
{  
    out-out & RESET_ON;  
    outportb(out_port, out);  
    out-port & RESET_OFF;  
    outportb(out_port, out);  
}

void set_bypass(int bp)
/* select 16/24-bit ctr */
{
    if (bp=0)  
    out-out & BYPASS_ON;  
    else  
    out-out & BYPASS_OFF;  
    outportb(out_port, out);
}

void main(void)
{  
    clrscr();  /* clear screen */  
    out-port=(WORD far *)IEX_PTR(&0x0040,A); /* find printer */  
    in-port-out-port; /* port address */  
    outportb(out_port, out);  /* power on */  
    delay(1000);
    clear_counter();  /* clear ctr */  
    set_bypass();  /* set 16-bit ctr */  
    out-out & CLOCK_ON;  
    outportb(out_port, out);  /* start ctr */  
    delay(200);  /* delay 200 msec */  
    out-out & CLOCK_OFF;  
    outportb(out_port, out);  /* stop ctr */  
    temp=(float)get_data()200; /* clear counter */  
    set_bypass();  /* set 24-bit ctr */  
    out-out & CLOCK_ON;  
    outportb(out_port, out);  /* start ctr */  
    test_procedure();  /* run test procedure */  
    out-out & CLOCK_OFF;  /* stop ctr */  
    outportb(out_port, out);  /* get data */  
    if (data<256)
    {  
        clear_counter();  /* get counter number */  
        set_bypass();  /* set 16-bit ctr */  
        test_procedure();  /* and test again */  
        if (data=256)
        {  
            dis=(float)(data/temp);  /* find execution time in msec */  
            printf("execution time is 1.2f msec\n",dis);  /* display result */  
            getch();  /* hit any key to return */  
        }
    }
    else
    data=256;
    dis=(float)(data/temp);  /* find execution time in msec */  
    printf("execution time is 1.2f msec\n",dis);  /* display result */  
    getch();  /* hit any key to return */  
}
```
ESD Testing for RS232 Interface Circuits – Design Note 80
Gary Maulding

In 1992 Linear Technology introduced the first RS232 interface circuits capable of surviving in excess of ±10kV ESD transients. Since that time, LTC has introduced more than 30 products with this level of protection. The inherent ruggedness of these products eliminates the need to use external protection devices in most applications. Not one unit has been returned from the field to Linear Technology for an ESD related failure analysis since the enhanced ESD protected devices were introduced.

The ±10kV ESD voltage rating is based on the Human Body ESD Model. When evaluated with other standard ESD test methods, the superior ESD ruggedness of LTC’s transceivers gives equally impressive results when compared to older conventional designs.

The various ESD test methodologies all share a common configuration as shown in Figure 1. A source capacitor is first charged to a high voltage, then the high voltage power supply is disconnected from the capacitor, and the capacitor is connected to the device under test through a limiting resistor. The value of the test capacitor and the limiting resistor differ among the various test standards.

The Human Body Model is the most commonly used ESD test in the United States and is the test method prescribed by Mil-Std-883. This method simulates the ESD discharge waveform seen from human contact to a piece of electronic equipment. The source capacitor is 100pF, limited by 1.5kΩ for the human body model. Linear Technology’s RS232 transceivers can withstand in excess of ±10V when tested with the Human Body Model.

The machine model, commonly used for ESD testing in Japan, is a more severe ESD test. This model simulates metallic contact between the device under test and a charged body. The source capacitor is 200pF with no limiting resistor. The higher source capacitance and the absence of a limiting resistor causes the device under test to be subjected to more voltage, energy, and current than human body model testing. Therefore failures occur at lower test voltages with machine model than with human body model testing. LTC’s RS232 transceivers can withstand ±3.5kV when tested with the machine model.

The IEC-801 test method fits between the human body and machine methods in severity. The source capacitor is 150pF with a 330Ω limiting resistor. LTC’s RS232 transceivers pass test voltages of ±7.5kV with the IEC-801 method.

The performance of LTC’s 10kV protected RS232 transceivers to each of these test conditions is summarized in Table 1. Also included are protection levels achieved to machine model testing by including a simple RC network on the RS232 line pins. The RC network used is a “T” network formed with two 200Ω resistors and a 220pF capacitor to ground. The added resistance and capacitance are small enough to have negligible effect on RS232 signals, but provide a great increase in ESD protection at a lower cost than using TransZorbs® with a diode network, which is commonly used for ESD protection. Test voltages higher than those shown in

TransZorb® is a registered trademark of General Instruments, GSI

![Figure 1. ESD Test Standards](image-url)
Table 1 sometimes cause device damage. The damage seen most commonly is an increase in driver output leakage with functionality failures occurring at even higher voltages.

Table 1. LTC RS232 Transceiver ESD Test Results

<table>
<thead>
<tr>
<th>ESD Test Model</th>
<th>Driver Pin Protection</th>
<th>Receiver Pin Protection</th>
</tr>
</thead>
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<tr>
<td>Human Body</td>
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<td>±10kV</td>
</tr>
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<td>Machine</td>
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<tr>
<td>Machine Model with RC Network on RS232 Pins</td>
<td>±10kV</td>
<td>±10kV</td>
</tr>
</tbody>
</table>

ESD Transients During Powered Operation

The test methods discussed so far involve testing for permanent damage to the integrated circuit from ESD transients. In today’s portable electronics, interconnection of cables to the communications ports may occur while the equipment is operating. This makes it imperative that the circuit can tolerate the ESD transient with minimal disruption of system operation. LTC’s RS232 interface circuits can withstand 10kV ESD transients while operating, shut down, or powered down. Disruption of data transfer is unavoidable during the ESD transient event, but data transmission may resume upon the completion of the event.

Figure 2 is a scope photograph of the data transmission interruption and recovery seen when a -10kV ESD transient strikes a communications line. The test circuit of Figure 3 was used to record this event. The ESD strike is applied to the driver output of an LT1180A and the receiver input of an LT1331. The ESD transient is of too short a duration to be recorded on the photograph, but the effects of the transient can be seen by the corruption of data after the strike. The circuits require about 20µs to recover from the event, after which data transmission continues normally.

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output-port address, and address+1 is the input-port address. After clearing the counter and enabling the clock, the program lets the counter free-run for 1 msec and then reads the counter bit-by-bit. The resultant number indicates how many clock cycles occur during 1 msec and determines the oscillation frequency. Next, the program sets the CD4536 to be a 24-bit counter, clears the counter, starts the clock, runs the test procedure, and stops the clock. If the reading is too small, the program sets the CD4536 to a 16-bit counter and reruns the test. Based on the known clock frequency and counter number, calculating the execution time of the tested procedure is easy. Since the maximum counter number and clock are 24 bits and 10 µsec, respectively, the maximum execution time this circuit can measure is 160 seconds.

Switching-regulator output goes below $V_{\text{REF}}$

Michael Keagy, Maxim Integrated Products, Sunnyvale, CA

The feedback arrangement of typical switching regulators doesn't allow the regulated outputs to go lower than the reference voltage. If you try to lower the output by modifying the feedback network, the compensation components the manufacturer recommends may no longer stabilize the regulator's error amplifier. An external reference voltage (Fig 1) helps overcome this problem.

IC$_1$ regulates by keeping the voltage at its FB pin equal to the internal $V_{\text{REF}}$, which normally sets a lower limit of 2.21V for $V_{\text{OUT}}$. The FB voltage usually results from a resistive divider that connects between $V_{\text{OUT}}$ and ground. However, this circuit connects the divider between $V_{\text{OUT}}$ and the higher-voltage shunt-regulator output of D$_2$. As you adjust $R_5$, the resulting output voltage ranges from 2.21 to approximately 1.2V, according to the following equation, where $V_{FB}=V_{\text{REF}}=2.21$V, and $V_z$ = zener voltage = 7.5V:

$$V_{\text{OUT}}=V_{FB}(R_1+R_2)/R_2-V_z(R/R_2).$$

Because IC$_1$'s error amplifier is inherently stable, the simple compensation components $R_1$ and $C_1$ ensure that the circuit is stable. You can set $V_{\text{OUT}}$ lower than 1.2V if you also modify the compensation network. And, the feedback modification shown in this circuit can let other regulators produce outputs lower than $V_{\text{REF}}$ if you can stabilize their error amplifiers.

IC$_1$'s highest allowable input voltage is 40V. If $V_{\text{IN}}$ differs significantly from 40V, adjust $R_1$ as necessary to return the zener current to approximately 1.5 mA. $R_3$ is an optional load resistor that prevents the otherwise unloaded output from approaching the zener voltage.

The circuit can supply 5A and offers 0.75%/V line regulation for inputs between 30 and 40V. Load regulation for the output currents between 0.1 and 5A is 0.4%/A. Losses occur in D$_p$, which drops about 0.2V, and in the inductor, whose series resistance is approximately 0.06Ω. Together, these components consume about 2W at 5A. $C_1$ and the internal, power Darlington transistor also consume power.

When supplying 1A, Fig 1's efficiency for $V_{\text{REF}}=1.2$V is approximately 50%—and 60% for $V_{\text{OUT}}=2$V. Efficiency degrades at light loads because of relatively high supply current. The levels at dc—8.5 mA in the IC and 1.5 mA in the zener diode—decrease somewhat with the switching frequency. IC$_1$'s internal Darlington switch drops about 1.8V. Other regulators that have lower voltage drops across the switch will have higher efficiencies at lower load currents.

Fig 1—Connecting the $R_4$ and $R_5$ feedback network to 7.5V instead of to ground enables this switching regulator to produce a regulated output that's lower than its internal reference voltage.

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Pulse-width adjuster reverses servo motor
Joe Utasi, Jomar Products Corp, Cincinnati, OH

Typical remote-control systems and robotics applications use standard R/C servos, which often require a reversal of the direction of rotation. Since varying the input signal’s pulse width between 1 and 2 msec controls the servo’s output position, a circuit that adjusts the pulse width to cause direction reversal can often come in handy. Many such circuits exist that use relatively sophisticated servo-control ICs, but the implementation in Fig 1 uses a standard CMOS IC to produce a reliable design at low cost.

Q₁ functions as an input buffer, which allows correct control even if the input is not logic-level compatible with the CMOS chip. At the beginning of the active-high normal servo pulse, the output of Q₁ goes low, triggering timer IC₁₄, which the circuit sets for 3 msec. This action forces the clear line of timer IC₁₈ high, getting this second timer ready to accept a trigger pulse. At the end of the normal servo pulse, Q₁ goes low, timer IC₁₈—which is configured as a latch—triggers, and its output remains high until IC₁₄ times out. Since IC₁₈’s output doesn’t go high until the original input pulse goes low, the output of IC₁₈ is the difference between the input and IC₁₄’s 3-msec timer. Thus, as the input signal increases in width, the output decreases, and the circuit essentially reverses the direction of the servo-control pulse. D₁ and C₁ filter battery noise caused by the servo system and ensure that the servo-pulse reverser does not introduce any jitter into the system. EDN BBS/DL_SIG #1389

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To shorten the duration of an input pulse and thereby reverse the direction of the servo-control pulse, this circuit essentially subtracts the input pulse width from timer IC₁₄’s fixed-pulse-width output.
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LanICE moves PC-based in-circuit emulators onto Ethernet

The world is going distributed. One evidence of this phenomenon is the increasing number of development teams who are connecting their targets to the LANs to which their workstations or PCs are connected. This allows the team members to develop software in the comfort of their own offices and provides all team members with access to the target. The target itself can be anywhere that is accessible to the LAN.

One company that is facilitating this move is Nohau. It basing its in-circuit emulators (ICEs) on boards that plug into IBM PCs. Until now, users had to control the ICE with a PC that was very close to the target or use an RS-232C box to connect to the ICE via a standard but slow COM port.

The Nohau LanICE box allows you to connect the ICEs to your network. It is based on a 66-MHz 486. In essence, it is a PC without a keyboard or a display but with an Ethernet interface and all the software to control the ICE from a workstation running X Windows. LanICE comes in a tower configuration that houses as many as five emulators.

LanICE's 10-Mbps interface maintains high throughput to the ICE. This allows program downloads, single-stepping, and other operations to run very quickly from a workstation or a networked PC.

LanICE creates Transfer Control Protocol/Internet Protocol (TCP/IP) messages that contain all of the font and other information X Windows needs to display in an MS-DOS-compatible or a Microsoft Windows-compatible window. When you use the Windows-compatible window, the ICE works as if you were using a PC directly connected to the ICE. The LanICE costs $3500. -David Shear

Nohau Corp., Campbell, CA. (408) 378-1820. Circle No. 336
IDT adds the Quarter-Size Outline Package (QSOP) to complete its winning hand of surface-mount packages for its high-speed FCT Logic family. With products available in TSSOP, QSOP, SSOP, and standard SOIC packages, IDT now offers the industry’s widest line of high-density packaging for both Octal and Double-Density logic.

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**Optimized libraries for TI C30 and C40 DSPs**

Two new libraries are available for the Texas Instruments TMS320C30 and TMS320C40 DSPs. STD/Mathlib is a runtime library that contains 33 mathematical functions commonly used in machine control, DSP, and graphics. The library also includes hand-coded trigonometric, transcendental, hyperbolic, and other functions. STD/Mathlib costs $495 on DOS and $695 on Sun/OS.

The DSP/Veclib library of DSP functions for the TMS320C40 includes more than 300 hand-coded functions, such as FFTs, convolutions, and correlations. It is available for DOS and Sun/OS systems and costs $3000. —David Shear

**PC-based, 4×6-in. SBC incorporates video**

The 16-MHz V-40 µP-based single-board computer (SBC) contains 640 kbytes of user DRAM, disk controllers, and a VGA video/LCD controller. To round out the PC-based architecture, the 4×6-in. SBC also includes a 128- to 256-kbyte BIOS flash EPROM, three RS-232C ports, a parallel port, a real-time clock with a battery, and an optional ARCnet interface. The PC/+v consumes 2W and costs $300. —David Shear

**Simulation library offers block diagram**

Engineers designing digital communications can now prototype their designs with block diagrams using Hyperception's Hypersignal for Windows advanced transmission library. It works with the Hypersignal for Windows block-diagram simulation software.

The new blocks in the library include baseband transmission models, modulation, demodulation, carrier and clock recovery, arbitrary filter design, and system-performance measures. Hypersignal for Windows costs $1495. —David Shear

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Toshiba 8-bit µC offers 60 kbytes of ROM elbow room

For most microcontroller (µC) system designers, there's never enough memory; they're continually shoehorning code into small memory spaces. Toshiba's TLCS-870 8-bit µCs give these designers some breathing space—up to 60 kbytes of ROM and 2 kbytes of RAM. Built with a register-banked architecture, the 870 has a 2-MHz internal bus and a full instruction set.

You can buy a lot of code forgiveness with 60 kbytes. With that much ROM, you can pay more attention to code correctness than just to code size. Not only that, but a 2-kbyte RAM, even with 16 banks of eight registers each, leaves a lot of room for stack operations. The 870 supports a software stack and has the room for it. The large code space, moderate-size RAM, and software stack make C a viable programming option. Toshiba offers its own C compiler.

The 870 has a full set of peripherals, including an 8-bit ADC, three 8-bit timer/counters, two 16-bit timer/counters, a watchdog timer, and three serial interfaces. Additionally, the 100-lead chip provides 90 I/O pins for data input and output.

To conserve power, the 870 has a dual clocking system: an 8-MHz fast clock and a 32-kHz slow clock. It has five power-saving modes: Stop (no oscillator), Slow (32.8-kHz clock), Idle1 (CPU stopped, peripherals on fast clock), Idle2 (CPU stopped, peripherals use fast or slow clocks), Sleep (CPU stopped, peripherals use slow clock). Interrupts trigger an exit from these modes. Toshiba supplies development tools for the 870; these include the C compiler, an assembler/linker/loader/library, and an in-circuit emulator.

—Ray Weiss
Circle No. 404
8/32-bit \(\mu\)C combines RISC and traditional design

RISC technology is not confined to 32-bit, high-memory-bandwidth processors. For example, although Hitachi's H8/300H 32-bit microcontroller (\(\mu\)C) is not quite RISC, it combines RISC design techniques (simple instructions, pipelining) with traditional \(\mu\)C design. Using 2- or 4-byte instructions, the CPU delivers a peak instruction rate of 7.6 MIPS with a 16-MHz external rate; Hitachi claims a 1.9-MIPS Dhrystone rate.

The H8/300 integrates up to 64 kbytes of on-chip program ROM with off-chip DRAM. It has up to 2 kbytes of RAM for fast local data access but also enables programs to make use of a large, slower, low-cost DRAM. Designing in the chip is easy; the \(\mu\)C has an on-chip DRAM controller, complete with programmable wait states, row-access/column-access strobes, and refresh cycles. The device lets you execute code from the DRAM, but doing so reduces execution rates. For example, memory fetches would take longer with this method, and with a 16-byte-wide DRAM bus, a 32-bit instruction would take two memory cycles to access.

The H8/300H is a full-fledged \(\mu\)C, not a RISC CPU with a few peripherals. It includes a timer complex with a free-running clock; a 10-bit ADC; a timing-pattern generator for stepper-motor, motor-control, and event-generation applications; an 8-bit DAC; and three serial I/O ports. A DMA controller offloads the CPU; the controller directs an I/O stream to or from memory without causing the CPU to spend the overhead to take, process, and return from an interrupt. The \(\mu\)C comes in a 100-pin chip and has up to 48 I/O pins for monitoring and control.

Development tools from Hitachi and third-party vendors include a C compiler, a GNU development environment, an assembler/linker/loader/library, a simulator/debugger, and an in-circuit emulator.—Ray Weiss


\[\text{Circle No. 405}\]
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Rack-mounted case holds PCs in industrial applications. A series of ruggedized rack-mounted cases for PC mother boards and adapters measures 4U (7 in.) high and 17.7 in. deep. The cases have predefined mounting positions for all sizes and formats of 386 and 486 motherboards. A hinged front cover is lockable. The front panel meets the IP21 sealing spec. A removable mass-storage subassembly accepts hard drives. The manufacturer can also supply 8-, 12-, or 14-slot passive backplanes and power supplies, $600 (wired, power supply, 8-slot backplane). BICC-Vero Electronics Inc, Hamden, CT. (203) 287-0062.

Gang jack features eight positions and four cavities. The TM5RL-3232 gang jack has plastic holdowns and measures 0.46 in. high (shielded version, 0.47 in.). The jack accepts the company's 8-position plug. Typical applications are LAN pc boards. $5.27 (100). Single-position unit: $1.56 (100). Hirose Electric USA Inc, Simi Valley, CA. (805) 522-7958.

Ultraminiature selector switches measure 0.157 and 0.236 in. square. The 7600 Series of single-pole, multiple-throw selector switches come in surface-mount and through-hole versions. The rotary switches have five or 10 positions—four throws plus one off or nine throws plus one off. $1.14 and $1.53, respectively. Bournes Inc, Riverside, CA. (909) 781-5140.

Extender card brings PCMCIA bus out into the open. A 5V, 68-pin PCMCIA extender card accepts Type I, II, and III PCMCIA cards. The extender card has test posts for all pins. $169.95 (10). Swart Interconnect, South San Francisco, CA. (415) 588-4450.
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Cypress Semiconductor, the PLD and memory vendor, is determined to become a major player in high-end programmable logic. Cypress’ latest entry is its own proprietary complex PLD (CPLD). It combines flash-memory reprogrammability with a high-routability, fixed-speed interconnect that links as many as 256 macrocells. The Flash370 introduction follows a January release of the company’s pASIC380 field-programmable gate-array (FPGA) family, based on the Quicklogic FPGA.

Built on a multilayer-multiplexed programmable interconnect, the CPLD delivers 10-nsec pin-to-pin combinational logic delays. These delays are maximums for any logic combination or path on the chip. Maximums for the macrocell D flip-flops reach 6-nsec setup time and 6.5-nsec delay (input pin to D input, D output to output pin) with a maximum external clock rate of 70 MHz (not counting board delays). Internal clock rates are 110 MHz max for register-to-register transfers. Cypress claims 60-MHz external and 80-MHz internal clock rates (average maximum frequency) running the Prep benchmarks.

The Flash370 integrates PAL-like macrocells into logic blocks, with 16 macrocells per logic block. I/O feeds into the programmable interconnect as well as into adjacent logic blocks. Each logic block has 36 inputs, including feedback terms from the macrocells. Each macrocell uses up to 16 product terms as inputs.

The macrocells share these sets of product terms with adjacent macrocells. The Flash370 overlaps these product terms for adjacent macrocells: The first macrocell gets the first 16 product terms (one through 16), the second macrocell gets 16 product terms shifted four terms down (five through 20), the third macrocell gets 16 product terms shifted another four terms down (nine through 24), etc. This product-term overlap enables the macrocells to share product terms without stripping terms from or taking over adjacent macrocells.

The device provides only fixed delays; there are no other delays due to term sharing or expanders. Because the programmable-interconnect delays are fixed, there are no penalties for large fan-outs. Outputs also go through the programmable interconnect and, therefore, cause no additional delays. You can shift or reprogram the logic that feeds output-I/O pins without delay penalties. These CPLDs provide a large number of product terms, ideal for implementing control logic. However, as with most other CPLDs, you must make some compromises to fit large numbers of macrocells—22V10 look­alikes. For one thing, the maximum number of signals available to the logic block is 36. These signals, in turn, feed the 16 macrocells that make up the logic block. The total number of product terms available to each logic block is 96. The macrocells share these signals, and three adjacent macrocells can use most of the signals. The CPLD builds on Cypress’s flash-memory technology and currently requires 12V for programming.

Cypress offers the Warp II development tools for the Flash370 line and is working on fitters, back-end tools that fit the netlist onto the FPGA architecture, for third-party tools. A fitter is available for Data I/O’s Abel system. Warp II supports Cypress PLDs, FPGAs, and the new CPLDs. Warp II enables you to design in the VHDL high-level hardware-description language, which is synthesized and mapped into a chip. The tool includes a functional simulator and a timing analyzer. Warp II sells for $995 and comes in versions for PCs and Sun workstations.—Ray Weiss

Cypress Semiconductor, San Jose, CA. (408) 943-2600. Circle No. 340

FPGA targets dynamically reloadable logic

In the main, logic design has been a relatively conservative activity; core-design techniques have not changed in 20 years. That is about to change, as logic designers come to grips with dynamically reconfigurable logic: programmable logic that is reconfigured on the fly while the logic is running.

Pushing that changeover is Atmel with its first dynamically reconfigurable field-programmable gate-array (FPGA), the AT6000 family. Based on the Crosspoint FPGA technology Atmel acquired last year, the SRAM-based AT6000 builds on a matrix of several small core-logic cells. Underlying SRAMs that must be loaded on initialization define these logic cells and their configurations. These configuration SRAMs can be loaded dynamically during circuit operation. Moreover, you can specify loading any cell or set of sequential cells via a serial, pin-oriented load. Thus, you can dynamically reconfigure portions of your logic during runtime, similar to the way a computer can load a new application or thread into memory for execution. This technique enables computers to time-share memory for multiple applications and lets you do the same with logic: load in specific logic functions for time-dependent execution.
The AT6000's array of moderately fine-grained cells is organized into an X-Y matrix. Each cell has a D flip-flop with multiplexer-oriented logic. You can configure the cells as basic SSI/MSI functions with or without the flip-flop. These cells are ordered in 8X8 local submatrices. The cells can serve as switches that connect cell to cell, cell to local bus, cell to express bus, or local bus to local bus. You can use a cell to turn a signal 90° and to connect it to a local or express bus or to an adjacent cell. The relatively large number of cells easily provides registers for data-path implementations.

You can interconnect these cells via a busing network, which has local buses (connects as many as eight cells) and express buses for long distances. You can move signals from bus to bus via repeaters, which can be tri-stated and have a delay of 1.6 or 2.1 nsec for express or local connections, respectively. The chip includes logic for vertical (column) clock distribution and asynchronous reset for the cell D flip-flops.

The cell registers have a 2-nsec setup time and a 2-nsec output delay. Cell logic delays are on the order of 2.2 nsec for a NAND and 2.4 nsec for an EXOR gate delay. I/O-buffer delays are 1.2 and 3.5 nsec, respectively. Each I/O can sink or source 12 mA, and you can combine I/Os for more power. All delays—express or local bus, local connections, gate, and flip-flop—are highly predictable. Thus, routing is highly deterministic for timing.

Atmel supplies an FPGA Physical Design System for $995. It includes a macro library, an automatic place-and-route tool, a static-timing analyzer, a design-rule checker, a load bit-stream generator, and other utilities. These tools integrate with Viewlogic Viewdraw (schematic) and Viewsim (functional simulator). Prototyping board kits are also available.

---Ray Weiss
Atmel, San Jose, CA. (408) 441-0311.
Circle No. 341

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### Atmel AT6000 FPGA family

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<td>96</td>
<td>120</td>
<td>108</td>
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<td>32 x 32</td>
<td>40 x 40</td>
<td>56 x 56</td>
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<td>Typical operating current (mA)</td>
<td>30</td>
<td>45</td>
<td>80</td>
<td>173</td>
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<tr>
<td>Package</td>
<td>44-pin PLCC</td>
<td>44/84-pin PLCC</td>
<td>68-pin PLCC</td>
<td>84-pin PLCC</td>
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<tr>
<td>Price (5000)</td>
<td>$16</td>
<td>N/A</td>
<td>$72</td>
<td>N/A</td>
</tr>
</tbody>
</table>

---

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**Self-timed SRAMs operate with Pentium µP.** The CXK77910A, a 1-Mbit synchronous self-timed SRAM, comes in 10- and 12-nsec cycle times and suits use with Pentium and SPARC µPs. The device integrates input registers, high-speed memory, and output registers onto a monolithic chip, which eliminates the need for off-chip pulse generation. The device has a 128k×9-bit organization and consumes 945 mW. Sample price is $100 for either speed. Sony Component Products Co., Cypress, CA. (800) 288-7669. Circle No. 345

**Analog transceiver is faster than digital versions.** The ML6580 is a bus transceiver that has a propagation delay of 1.5 nsec. The low propagation delay of the octal device lets data and addresses move between a µP and memory at high speeds. A µP operating at 66 MHz reads data on each clock tick, which is 15 nsec. Conventional digital receivers would take two clock ticks, or 30 nsec. The chip can drive 50-pF loads operating at 50 MHz and has a 300-mV typ ground bounce. 1.5-nsec version, $700 (100). Micro Linear Corp., San Jose, CA. (408) 433-5200. Circle No. 346

**Low-cost wideband buffers consume just 3.5 mA.** The CLC109 and CLC111 closed-loop unity-gain buffer amplifiers feature respective bandwidths of 270 and 800 MHz, slew rates of 350 and 3500 V/µsec, and typical supply currents of 3.5 and 10.5 mA when operating on ±5V supplies. The buffers can also operate on single 3V supplies. The CLC109’s gain flatness is ±0.1 dB to 30 MHz. The CLC111 features low distortion of ~62 dBc for second and third harmonics (at 20 MHz and 1000 Ω loads) and a 1.40 dB output impedance. In 8-pin plastic DIPs and SOICs, 100-piece prices for the 109 and 111 are $1.49 and $2.75, respectively. Comlinear Corp., Fort Collins, CO. (303) 225-7437. Circle No. 347

**Synchronous SRAMs suit cache memories.** The MT55SLC2K36, a 66-or 50-MHz synchronous SRAM, has a 32k×36-bit organization. The devices provide zero-wait states for cache memories, operate at 3.3V, and have 5V tolerant inputs and outputs. Options include support for 4-cycle burst-mode access and pipelined and nonpipelined operations. Cycle times are as fast as 15 nsec, and access times are as fast as 7 nsec (pipelined) and 12 nsec (nonpipelined). The devices come in a 100-pin thin flatpack, 12-nsec version; $40 (100). Micron Semiconductor Inc., Boise, ID. (208) 368-3900. Circle No. 348

**Four-quadrant multiplier inputs four channels.** Each channel of the MLT04 accepts a 12.5V input and delivers a normalized voltage output that implements a factory-calibrated transfer function of X×Y/2.5V. With ±5V supplies, typical power dissipation is 150 mW. In an 18-pin DIP or SOIC ($91.95 in 100), the MLT04 includes a stable 1.23V bandgap reference and individual output amplifiers. It requires no external components. Nonlinearity error is typically 0.2% with 0.005%/°C total error over temperature. Analog Devices Inc, Wilmington, MA. (617) 937-1428. Circle No. 349

**Dual op amp combines precision with speed.** The LM6182 dual current-feedback amplifier features a 100-MHz bandwidth and a 2000V/µsec slew rate. Precision specifications include a maximum offset voltage of 3 mV and maximum inverting and noninverting bias currents of 5 and 2 µA, respectively. The op amp supplies 100 mA of output current. A high-power output stage enables each amplifier to directly drive a 2V signal into 50 or 75Ω back-terminated coaxial cable over the −25 to +85°C temperature range. Differential gain and phase are 0.05% and 0.04°, respectively. A and standard grades cost $4.30 and $3.60 (1000), respectively. National Semiconductor Corp, Santa Clara, CA. (408) 721-6973. Circle No. 350

**Cache RAMs operate with 55-MHz 486 µPs.** The CXK784862Q-33/55 RAMs operate as a cache memory for 33- and 55-MHz 486 µPs, respectively. The device is a 2-way set-associative, zero-wait-state cache that operates with high-speed memory, and output registers onto a monolithic chip, which eliminates the need for off-chip pulse generation. The device has a 128k×9-bit organization and consumes 945 mW. Sample price is $100 for either speed. Sony Component Products Co., Cypress, CA. (800) 288-7669. Circle No. 343

**Single-supply op amps cost cents/channel.** The 4-MHz dual OP292 and quad OP492 cost $1.32 (1000) and $2.16, respectively, making per-channel costs $0.66 and $0.54, respectively. Operating from a single 5V supply, the OP292’s guaranteed maximum dc specifications include 800-µV offset and 10-µV/°C drift with 700-nA input offset current over the IC’s −40 to +125°C operating temperature range. Both amplifiers feature voltage and current noise of 15 nV/√Hz and 0.7 pA/√Hz, respectively. Slew rate is typically 4V/µsec, and channel separation at 1 kHz is 100 dB. The dual and quad amplifiers come in 8- and 14-pin DIPs and SOICs, respectively. Analog Devices, Wilmington, MA. (800) 879-4963. Circle No. 344
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MAX709 versus TL7705 Comparison

- External Components Required: MAXIM 0, TI 3
- Operating Supply Current: MAXIM 65μA, TL7705 35μA
- Power Supply Glitch Immunity: MAXIM Yes, TI No
- +5V Reset Threshold Options: MAXIM 2, TI 1
- +3V Reset Threshold Options: MAXIM 3, TI 1
- Guaranteed Min Reset Delay: MAXIM Yes, TI No

Low-Cost μP Supervisors Replace Several Components

<table>
<thead>
<tr>
<th>Part</th>
<th>Reset Threshold (V)</th>
<th>Manual Reset</th>
<th>Extra Comparator (Power Fail)</th>
<th>Battery Backup Switchover</th>
<th>Watchdog Timer</th>
<th>Active High Reset</th>
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ISA bus waveform-capture board takes 500M samples/sec in real-time

The 350-MHz-bandwidth DA500 waveform-capture board from Signatec represents a significant accomplishment. Its top acquisition speed is 500M samples/sec, putting it in the same class as some of today's faster real-time-sampling benchtop scopes. Moreover, when you install a piggyback RAM card, the 8M-sample memory is as deep as that on the deepest-memory benchtop scope. And when higher-capacity SRAMs become available, the 8M-sample capacity will increase by a factor of four. Nevertheless, The DA500 doesn’t have the wide attenuation range of a general-purpose DSO. And, despite several trigger modes, the product lacks the trigger flexibility of a modern benchtop scope. That’s why the vendor calls the $6950 board a waveform digitizer and not a scope.

Even before the advent of devices that will allow a piggybacked 32-Mbyte acquisition memory, you can couple the DA500 via an auxiliary bus to some of the vendor’s other ISA bus boards. At 200M samples/sec and below, the DA500 can pump as many as 256M samples into a MEM500 board. The DA500 can drive up to four MEM500s, allowing 1 Gbyte of memory—the equivalent of over 5 sec of data at 200M samples/sec.

The board has two channels, but when you use both, the top acquisition speed declines to 25M samples/sec. If you want to acquire more channels at higher speeds, you can have as many as three additional DA500s act as slave boards attached to the first one and run all of them at 500M samples/sec.

The DA500’s spec sheet is more detailed than those of most DSOs. (Suppliers of waveform digitizers generally provide more performance detail than DSO vendors.) With a signal frequency of 250 MHz and a sample rate of 500M samples/sec, the board’s effective linearity is 7 bits. Its typical aperture jitter is 2 psec. The input attenuator spans 30 dB in 2-dB steps.

As you might imagine, the board dissipates a lot of power for a device that resides within a PC. Its maximum dissipation is 24W. Signatec provides two power-saving modes. In Off mode, the board powers down almost fully. Standby mode disables the data-acquisition circuits, reducing the dissipation by almost 90%. If the temperature of the ADC rises above 65 ° C, the board goes into the standby mode.- Dan Strassberg
Signatec Inc, Corona, CA. (909) 734-3001.

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Software accelerates LabView DSP operations up to 100×. QuView works with both Windows and Macintosh versions of National Instrument's LabView and with the vendor's ISA bus and Nubus plug-in boards, which are based on the AT&T 32C and TI TMS320C30 DSPs. The boards interface with external data-acquisition and control units. The acceleration software is free of charge to purchasers of the vendor's DSP or data-acquisition hardware units. From $9500. Sheldon Instruments, Orem, UT. (801) 376-7861. Circle No. 310

ISA bus DMM board resolves 5½ digits. The SM-2020 makes 4-wire resistance measurements as well as dc and 10-Hz to 100-kHz true-rms ac voltage and current measurements. Resolution is ±300,000 counts (equivalent to over 19 bits). For dc, the error is 100 ppm for one year. The accompanying software includes libraries for Windows and DOS that allow writing control programs in Quick C and Visual C++. The board is also compatible with ATEasy, LabView for Windows, and LabWindows for DOS. $995. Sigmetrics Corp, Seattle, WA. (206) 524-4074. Circle No. 311

Handheld, clamp-on instruments measure power quality. The $795 CPM2000 (for ac) and the $995 CPM2100 (for ac and dc) measure ac frequency, power factor, and volt-amperes (to 2 MVA), voltage (to 750V ac and 1 kV dc), current (to 2000A), and resistance (to 400 kΩ). A 100-Hz lowpass filter lets you detect the presence of harmonics. The meters also check diodes and indicate continuity audibly. Wavetek Corp, San Diego, CA. (619) 279-2200. Circle No. 314

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16-channel thermocouple data-acquisition unit plugs into PC's parallel port. You can connect up to 16 grounded thermocouples to the DI-221 TC's built-in terminals. The unit, which incorporates a temperature sensor for cold-junction compensation and auto-zero circuits to correct for amplifier drift, can average as many as 32,000 consecutive readings for noise cancellation. Thermocouple outputs are linearized in real time using DSP-based 10th-order polynomial compensation. You can select a full-scale range of ±200 or ±1200°C. $1395. Dataq Instruments Inc, Akron, OH. (216) 668-1444.

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Low-cost multimedia workstations perform engineering tasks, too

Two new Hewlett-Packard workstations designed primarily for commercial applications, such as financial trading and document and image management, also suit electronic-design work. Both are software-compatible with current HP 9000 Series 700 workstations, and both have computing power that is impressive for their price tags. With emulation software, they can run PC applications.

The new HP 9000 Series 700 models, the 60-MHz 712/60 and the 80-MHz 712/80i, use HP's new low-cost PA-7100LC processor. The 712/60, which sells for as little as $3995, delivers 58 SPECint92; the 712/80i, beginning at $8820, performs at 84 SPECint92. Both deliver 79 SPECfp92. According to comparison data provided by HP, that's better performance per dollar than any competitor provides.

Reasonably priced graphics and multimedia capabilities in the new workstations result from several innovations. For example, the PA-7100LC processor has fast MPEG decompression capability built in, allowing the display of video at a full-motion 30 frames/sec. To reduce the amount of expensive video RAM (VRAM) needed, HP uses a patented process called "color recovery." This approach uses only 8 bits per pixel, reducing VRAM by two-thirds, but, according to HP, most users can't distinguish the results from 24-bit "true" color.

The entry-level ($3995) 712/60 includes a 15-in. color monitor (for 1024×768-pixel display), 16 Mbytes of memory, and a 260-Mbyte hard disk. The lowest-priced ($8820) 712/80i has the same memory and disk configuration, but has a 17-in. color monitor for a 1280×1024-pixel display. A 12-in., 1024×768-pixel color flat-panel display will be available before midyear for $10,595.

Gary Legg
Hewlett-Packard Co, Palo Alto, CA. Phone (800) 637-7740; in Canada, (800) 387-3867.

Fax modem is PCMCIA compliant. The PCMCIA144FAX modem has a 14.4-kbps line speed, V.42 error correction, and V.42bis and MNP 2-5 data compression that handles data throughput up to 57.6 kbps. A fully integrated DAA on the modem complies with PCMCIA Type II standards. The modem supports V.32, V.32bis, V.22bis, V.22, V.21, 212, 103 data standards and V.29, V.27ter, and V.21 fax standards. Fax functions include background send and receive, multiple transmissions, graphics file conversion to fax format, and viewing before sending. $999.

Ven-Tel Inc, San Jose, CA. (800) 538-5121.

Circle No. 320

PCMCIA-card drive replaces floppy-disk drive. The CDD300 memory-card drive physically replaces a conventional 3.5/5.25-in. floppy-disk drive. The unit interfaces directly to a conventional 3.5/5.25-in. floppy-disk drive. The unit interfaces directly to a conventional 3.5/5.25-in. floppy-disk drive.

The entry-level ($3995) 712/60 includes a 15-in. color monitor (for 1024×768-pixel display), 16 Mbytes of memory, and a 260-Mbyte hard disk. The lowest-priced ($8820) 712/80i has the same memory and disk configuration, but has a 17-in. color monitor for a 1280×1024-pixel display. A 12-in., 1024×768-pixel color flat-panel display will be available before midyear for $10,595.

Gary Legg
Hewlett-Packard Co, Palo Alto, CA. Phone (800) 637-7740; in Canada, (800) 387-3867.

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Circle No. 320

PCMCIA-card drive replaces floppy-disk drive. The CDD300 memory-card drive physically replaces a conventional 3.5/5.25-in. floppy-disk drive. The unit interfaces directly to a standard host system and is compatible with 1.44-Mbyte/720-kbyte and 1.2-Mbyte/360-kbyte disk formats. The single- or dual-slot unit accepts Type I and II PCMCIA 2.0 (JEIDA 4.1)-compatible

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SRAM cards. Single- and dual-slot units cost $250 and $360, respectively. Aval Corp, Dublin, Ireland. (1) 2892136.

Circle No. 321

Host adapter delivers instant PCMCIA-to-SCSI connections. The SlimSCSI, a rugged, credit-card-sized I/O device, lets users attach peripherals to their portable systems. The 16-bit SCSI adapter fits PCMCIA Type II or III slots. Users can daisy chain as many as seven devices simultaneously. The adapter achieves data-transfer rates of 2 Mbytes/sec. $349. Adaptec, Milpitas, CA. (408) 945-8600.

Circle No. 323

Card upgrade offers lower power consumption. The IBM PC/AT-compatible Cardio-86 uses the power-management schemes of Chips and Technologies F868A µP to make power consumption less than that of its predecessor, Cardio-386. The credit-card-sized mother board retains full support of the PC/AT bus's 8-MHz clock performance; its interface is Epson's All-in-one System Interface (EASI), and an interface that is not an EASI is available for PCMCIA support. $250 (1000). S-MOS Systems, San Jose, CA. (408) 922-0238.

Circle No. 324
EPSON

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MEMORY CARDS

JEIDA/PCMCIA 68 PIN STD

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<td>256KB-2MB</td>
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Mathematica applications library available for EEs. The Electrical Engineering Pack is the first in a series of Mathematica applications libraries. The EE pack is a collection of notebooks and packages written in Mathematica. The collection helps EEs use Mathematica for circuit-analysis, transmission-line, antenna-design, and other problems. The customizable pack also provides a set of Mathematica functions for common tasks. The software runs on Macintosh, Microsoft Windows, and X-Window systems equipped with Mathematica 2.2. $195. Wolfram Research Inc, Champaign, IL. (800) 441-6284. Circle No. 326

Electronic book provides on-line access to Mathcad features. Mathcad 5.0 Treasure, Volume I: Mathcad Foundations, a "book" that runs on PCs, Macs, and Unix workstations, gives Mathcad 5.0 users interactive, on-line access to all the mathematical features and algorithms of Mathcad. It also provides detailed explanations and examples of how those features operate. Every number, formula, and plot in the book is live and interactive, letting users adapt them for individual problems. The book includes tips, techniques, and examples for making full use of Mathcad 5.0's functions. $99. MathSoft Inc, Cambridge, MA. (617) 577-1017. Circle No. 327

Card automatically controls multiple drives. The PCMCIA Type II Multi Drive I/O card simultaneously controls drives for CD-ROMs, floppy disks, fixed hard disks, removable-cartridge hard disks, QIC-80 tape, QIC-3010 tape, and QIC-3020 tape. The first drive connects directly to the card, and the rest daisy chain to the unit. The card senses drive capacity and type without user intervention. $199. PacRim, Hayward, CA. (510) 782-1017. Circle No. 328

PCL chip and board support SCSI peripherals. The 32-bit 36C70 PCL local bus-to-SCSI II IC forms the basis of the TMC-3260 PCL-to-SCSI board. Together, the chip and card offer fast-synchronous 10-Mbyte/sec support for high-performance SCSI peripherals. The products support Windows NT, OS/2, Unix, NetWare, Interactive Sunsoft/Unix, and UnixWare. Chip, $20 (OEM); card, $259. Future Domain, Irvine, CA. (714) 253-0400. Circle No. 329

1.3-Gbyte magneto-optical drive fits half-height slot. The JY-800 magneto-optical disk drive features a compact half-height package for horizontal or vertical mounting. The 1.3-Gbyte drive has a 40-msec seek time and effective transfer rate up to 2 Mbytes/sec. The drive fits in standard 5.25-in. floppy-drive bays and is compatible with PCs, Macintoshes, and Unix workstations. Average power dissipation is 17W. $2400. Sharp Electronics Corp, Mahwah, NJ. (800) 642-0261. Circle No. 330

Frame grabber acquires images in real time. The DT55-LC, a PC/AT ISA-bus/EISA-compatible optically isolated frame grabber, provides 12-bit A/D conversion for 32 analog input channels (16 differential). The board also includes testing capabilities for off-line and real-time fault detection. A software-controlled front-panel LED turns on at system reset, and the software turns it off when the test is complete. $1199. VME Microsystems International Corp, Huntsville, AL. (205) 880-0444. Circle No. 333

Scanning board includes testing. The VMIATX-$125, a PC/AT ISA bus/EISA-compatible optically isolated scanning board, provides 12-bit A/D conversion for 32 analog input channels (16 differential). The board also includes testing capabilities for off-line and real-time fault detection. A software-controlled front-panel LED turns on at system reset, and the software turns it off when the test is complete. $1199. VME Microsystems International Corp, Huntsville, AL. (205) 880-0444. Circle No. 333

Touch monitor measures 17 in. The TruPoint-DS17 touch monitor, a 17-in., flat, square touch monitor, provides a screen with 1.5 times as much space as a standard 14-in. screen, giving developers more area for displaying graphics and touch buttons. The flat, square CRT reduces image distortion and makes viewing images at the edge of the display easier, according to the vendor. The display provides flicker-free 1280×1024-pixel, 74-Hz noninterlaced resolution and a 30- to 78-kHz horizontal scan rate. $1975. MicroTouch Systems Inc, Methuen, MA. (508) 659-9000. Circle No. 334
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Dual IGBT power modules contain complete half bridge. The model VIE 12S isolated-gate transistor (IGBT) power modules feature a fully isolated gate drive, dual 1200V/150A IGBTs connected as a half-bridge. The modules also contain transformers that achieve a 2500V input-to-output isolation. The modules’s on-board supply powers the modules’s gating and protection circuitry. 150A version, $228.15; 100A version, $152.75; 75A version, $113.75. IXYS Corp, Santa Clara, CA. (408) 962-0700. Circle No. 352

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Supply is hot-swappable. The model LT1700 400W ac/dc universal converter supplies 54V dc (power output jumps to 550W for inputs above 155V ac). The supply measures 4 X 5 X 5.7 in. The unit features power-factor correction and no inrush current. The unit also sports transient suppression, filtering, and shock and vibration immunity. You can parallel as many as three units in one 5.25-in. rack without forced-air cooling or heat sinking. A negative temperature coefficient allows for safe 48V backup-battery charging. $1036 (one), delivery is six weeks ARO. Melcher Inc, Chelmsford, MA. (508) 256-1812. Circle No. 354

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- Available from 100 milliwatts to 3 watts
- Impedance from 20 ohms to 100 K ohms
- Operating temperature -55°C to +130°C
- Low profile .2" ht.

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