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HP scopes make digital designs easier to understand.

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Compare the stats:

<table>
<thead>
<tr>
<th></th>
<th>PM 6680</th>
<th>HP 5334B</th>
<th>HP 5335</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range, A</td>
<td>225 MHz</td>
<td>100 MHz</td>
<td>200 MHz</td>
</tr>
<tr>
<td>Frequency Range, C (optional)</td>
<td>2.7 GHz</td>
<td>1.3 GHz</td>
<td>1.3 GHz</td>
</tr>
<tr>
<td>Single Shot Res.</td>
<td>500 ps</td>
<td>2 ns</td>
<td>2 ns</td>
</tr>
<tr>
<td>Max. Reading Rate</td>
<td>2000/s</td>
<td>150/s</td>
<td>125/s</td>
</tr>
<tr>
<td>Base Price</td>
<td>$2,075*</td>
<td>$2,305</td>
<td>$5,000</td>
</tr>
</tbody>
</table>

Besides setting a faster pace, the PM 6680 adds new time and frequency analysis tools. Built-in mathematics and statistics functions give you stand-alone processing power that makes it easy to obtain measurements such as drift and rate of drift.

Put those features together with 2000 readings per second and you have a powerful tool for analyzing timing jitter without a controller. The PM 6680 can also characterize VCOs or frequency agile sources quickly and easily.

And a host of new measuring capabilities give you the versatility to address your toughest measurement problems.

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Plus the PM 6680 is the first GPIB timer/counter to use the SCPI standard so you’re assured of easy upgradability and modification down the line. Without a doubt the PM 6680’s thoroughbred speed and power will put you in the winner’s circle for a workhorse price. It’s backed by Fluke’s strong track record as a leader in electronic instrumentation and test solutions, plus complete technical support and fast service.

To get significantly more performance from a timer/counter for significantly less cost, discover the PM 6680:

the new breed of timer/counter from Fluke. Call 1-800 44-FLUKE ext. 701 for more information and a free demo.

Thoroughbred performance at a workhorse price.
Design for test (without really trying)

Despite the dangers of ignoring testability, subtle costs can make designing an ASIC for test prohibitively expensive. Testability tools provide construction techniques that lower the cost of designing for test.  
—Michael O Markowitz, Technical Editor

Designer’s guide to measuring op-amp distortion

—Jerald Graeme, Burr-Brown Corp

Part 1—Op-amp distortion measurement bypasses test-equipment limits

Part 1 of this 2-part series introduces the theory involved in measuring the low distortion levels of state-of-the-art op amps. It also provides simple methods for characterizing some low-distortion op amps.

Part 2—Advanced techniques tackle advanced op amps’ extremely low distortion

The second part of this 2-part series describes how to measure the distortion of more complex amplifier circuits and how to handle the highest-performance op amps.

Continued on page 7
Introducing PLDecoders.

Taking systems to 40 MHz and beyond has become a whole lot simpler with these new, function-specific BiCMOS Decoder PLDs. For RISC, including our highest performance SPARC processors, choose the input-registered versions to capture addresses quickly. For CISC, such as 80X86, we offer output-latched versions that optimize system performance. Choose simple addressing versions at 6 ns for fastest performance, or 7 ns bank select or byte-write versions to suit your application precisely.

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When your circuit designs run up against data-book specification limits, turn to a dc parameter analyzer—it will accurately measure the performance limits of your components. PAGE 65

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European manufacturing contractors encourage close relationships

European contract manufacturers want to contribute to the success of your product by becoming part of the business.—Brian Kerridge, Technical Editor

Parameter analyzers give you a closer look at dc-circuit performance

Parameter analyzers based on source-measure units provide flexible and sensitive instruments for characterizing dc circuits.—Doug Conner, Technical Editor

High-speed digital circuits: Timing techniques help signals stay in sync

You'll need a variety of practical skills and tools to tackle high-speed timing problems.—Anne Watson Swager, Technical Editor

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µC and software kit for Appletalk
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February 17, 1992

**DESIGN IDEAS**

- Miniature power supply works off line  
- Split supply operates from a single cell  
- Synchronous switch mutes line noise  
- Large capacitor serves as battery backup  
- Spice model mimics reference  
- Feedback and Amplification  

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**PROFESSIONAL ISSUES**

- Training with technology  
  Sports science and high-tech training equipment have helped our Olympic athletes, but a shortage of funds hinders the program.—Jay Fraser, Associate Editor  

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275 Washington St, Newton, MA 02158  
EDN Bulletin Board: (617) 558-4241  
MCI: EDNBOS  
(617) 558-extension

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Roger Bannister made the running of the mile an exact science, analyzing every moment, every aspect. And became the first man to break the 4-minute barrier in 1954. Scrutiny of every detail in electronics reveals a simple fact: Your equipment is only as fast as its slowest component.

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Seekers of something for nothing can start their quest with Technical Editor Michael M Markowitz’s Special Report “Design for test (without really trying).” Although you won’t find a prescription for free testability in this article, you will find a realistic look at the true costs of design for test (DFT). You’ll also find tools and techniques that make designing for test much easier than you might think. Be sure to check out the top-10 reasons for not using DFT methods in the same article.

Many engineers don’t employ DFT techniques because some of these test methods degrade device performance. However, designers who use only the data-sheet specifications rarely know the true performance limits of the devices they incorporate in their designs. You’ll find several articles on device characterization in this issue of EDN.

For starters, Technical Editor Doug Conner examines parameter analyzers. You might think parameter analyzers are primarily for incoming inspection, but you can also use these instruments to characterize device aspects not detailed in the manufacturer’s spec sheets. If you need to develop or refine realistic simulation models, parameter analyzers let you collect aggregate parametric information over device lots.

Fans of Burr-Brown’s analog guru Jerald Graeme will find his latest article, on characterizing op-amp distortion, in this issue. Graeme points out that distortion performance in op amps has become increasingly important because of the recent upswing in DSP applications.

Time is another tough parameter to characterize. If you can’t master your design’s timing, you’re really in trouble. In her Technical Update on high-speed digital circuits, Technical Editor Anne Watson Swager focuses on timing techniques, such as timing skew and clock generation and distribution, that help you take up the temporal slack.

One reason for characterizing devices is to ensure manufacturability no matter where the product is built. If your company expects to sell products based on your designs in Europe, you might want to study Technical Editor Brian Kerridge’s report on contract manufacturing within the European community.

Steven H Leibson, Executive Editor
There's nothing we hate more than delays. That's why we developed high-speed CMOS PAL devices that no one can beat—our CMOS 7.5ns 16V8H-7 and 10ns 22V10H-10 PAL devices.

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It's never been easier to make your innovative designs a reality. We offer you a complete family of powerful FPGAs, like the A1010 and A1020, available in 44, 68 and 84 pin PLCC versions and implementing up to 273 flip-flops or up to 546 latches. And the first member of our ACT 2 family, the power-
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EDN February 17, 1992 • 15
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EDN·NEWS BREAKS
EDITED BY SUSAN ROSE

New CPU boards shown at Buscon

A number of companies showed their new CPU boards for open buses at Buscon '92 West in Long Beach, CA, a few weeks ago. The emphasis of most of the products, naturally, is on faster CPU performance and highly integrated boards. For example, Omnibyte Corp's VMEbus Taurus board employs a dual-bus architecture that links onboard 25-MHz 68040 and 68030 µPs. The design dedicates the 68030 to I/O tasks, thereby freeing the 68040 to execute application code with little interruption. The board includes a memory architecture that lets the 68040 address as much as 256 Mbytes of memory, and the 68030 has access to as much as 64 Mbytes of memory. You can order configurations of the board with an Ethernet port, a SCSI host adapter, six serial ports, a parallel-printer interface, and 32 programmable digital I/O lines. A configuration featuring 4 Mbytes of dynamic RAM, 128 kbytes of static RAM, six serial ports, and the parallel interface costs $3495.

Motorola, meanwhile, announced its plans for board-level support of the new 88110 RISC µP. The company plans a single-slot VMEbus board that will include SCSI-2, Ethernet, and VSB interfaces as well as the µP and a 64-bit-wide memory array. Final specs and pricing of the board have been delayed because the company's IC division has yet to ship production versions of the 88110 IC. The new µP, however, will have a 3-D graphics-execution unit and a floating-point unit on chip. Omnibyte Corp, West Chicago, IL, (708) 231-6880, FAX (708) 231-7042; Motorola Inc, Tempe, AZ, (602) 438-3000.-Maury Wright

Embed a workstation in your next test system

You can use a 33-MHz 80486-based workstation with as many as four Expansion Module bus (EXMbus) expansion slots for your next embedded VXI controller. The EPC-7 from Radisys is a C-size plug-in board that you can use in place of an external workstation connected to your test rack. To provide flexible I/O expansion, the board's EXMbus architecture accepts modules for IEEE-488, Ethernet, RS-232C, RS-422, RS-485, a modem, solid-state disks, an interval timer, and an assortment of video controllers. An adapter module lets you plug in a full-length ISA expansion board for specialized I/O interfaces that aren't available as EXM modules. Standard hardware includes a serial port, a printer port, a reset button, and a keyboard interface. Three connectors let you externally route VXIbus trigger and clock signals. A SCSI connector lets you add external equipment such as tape-backup units or optical-disk drives.

For $6995, this 2-slot-wide controller includes a 33-MHz 80486 CPU, 2 Mbytes of dynamic RAM, a 52-Mbyte hard-disk drive, a 3½-in. floppy-disk drive, and the EP-Connect runtime package for DOS. A VGA graphics controller sells for $450. All software and application programs that run on the firm's EPC-2 systems will also run on the board without modification. Radisys Corp, Beaverton, OR, (800) 950-0044; (503) 690-1229, FAX (503) 690-1228.—J D Mosley

Gate array has 60-psec gate delay and 350,000 gates

Vitesse Semiconductor Corp continues to push GaAs semiconductors into mainstream semiconductor applications. The new VGFX350K member of the FX family of gate arrays includes 1.2 million active transistors—approximately the same number as the Intel 80486 µP. The 0.6-µm gate arrays feature a channel-less architecture with gate delays less than 60 psec. The first array Vitesse produced for a customer includes two 44-kbit blocks of static RAM and two 5-port register files. The RAM array features a 3-nsec access time. Expect a non-recurring engineering cost of $70,000 to $120,000 to develop a VGFX350K array. The company also introduced 20,000- and 40,000-gate members of the FX family that previously included only 100,000- and 200,000-gate arrays. Vitesse Semiconductor Corp, Camarillo, CA, (805) 388-3700, (805) 987-5896.—Maury Wright

EDN Asia gets Chief Editor

Michael Markowitz is leaving his post as Technical Editor at EDN Magazine to become Chief Editor of EDN Asia. Michael will join Jack Kompan, Publisher of EDN Asia, in Cahners Publishing's Hong Kong office.

Michael has been with EDN since 1988. Before coming to EDN, he was Senior IC Design and Applications Engineer at Marconi Electronic Devices and before that he designed...
custom ICs for General Instruments Microelectronics Division (now Microchip Technology). Michael has a BS in Liberal Arts from Haverford College, a BSEE from SUNY, Stony Brook, and an MBA from Adelphi University.

EDN Asia will begin monthly publication in May and will have a controlled circulation of 28,000. The magazine will carry the same types of technology features, reviews of technology trends, and surveys of state-of-the-art product areas as EDN does in the United States and Europe. It will also carry original, Asia-specific new-product stories, literature available in Asia, and career-related articles. The magazine is based in Hong Kong and will circulate to readers in Korea, Taiwan, Hong Kong, and ASEAN (the Association of South East Asian Nations, which comprises Brunei, Indonesia, Malaysia, the Philippines, Singapore, and Thailand). It will be published in English, Chinese (Mandarin), and Korean.

Send EDN Asia-specific product announcements to Jack Kompan or Michael Markowitz. EDN Asia, 22/F Lo Yong Court, 212-220 Lockhart Rd, Wanchai, Hong Kong, (852) 572-2037, FAX (852) 838-5912.—Susan Rose

European Group aims to advance MCM technology

Eureka project EU462 brings together 13 European companies with the common objective of developing design tools and manufacturing techniques for multichip modules (MCMs). Funding provided by governments supporting the project amounts to 18.3 million ECU (roughly $23.4 million), which will be spent over the next three years. The project members will make a special study of the use of nonsilicon substrate material such as ceramic, laminate, aluminum nitride, and metal-based compounds. Project teams will focus on seven key areas covering substrates, thermal management, die attachment, interconnection, protection, thermal and electrical modeling, and CAD tools. Two specific aims of the project are to achieve high-frequency performance to 40 GHz for telecommunications work, and 40 W/cm² for automobile applications.

Project member companies come from four countries: Nokia in Finland; SAT, SOREP, ES2, and Racal-Redac TAD in France; Saab-Sania Combitech in Sweden; and BNR, Newmarket Microsystems, Racal-Redac Systems, University of Warwick, Johnson Matthey, Gwent Electronic Materials, and TWI in the UK. TWI, an independent R&D contractor, is providing the project coordination and leadership. TWI, Abington, Cambridge, UK, 0223 891162, FAX 0223 892588, contact Norman Stockham.—Brian Kerridge

12-bit A/D converter won’t sweat in 200°C

Guaranteed to perform in temperatures exceeding 200°C, the 12-bit I-6H005 is a pin-compatible replacement for Burr-Brown’s A/D converter. Packaging techniques provide this chip with a 50% reduction in mass over the Burr-Brown part, which the company claims makes the chip less susceptible to shock in high g-force situations. Offering both serial and parallel data outputs, this IC also has a monolithic, internal 10V reference. Suitable for applications involving engine or power control, this device also has an internal clock and hermetic packaging. The chip costs $650 (100); evaluation samples cost $250. ITAC Hybrid Technology, Garland, TX, (214) 494-3073, FAX (214) 494-4159, contact Rick Carr.

—J D Mosley

Get fuzzy in Japan

Followers of fuzzy logic should check out the proceedings of the International Fuzzy Engineering Symposium ’91 held last November in Yokohama, Japan. The symposium dealt with both the theoretical underpinnings of fuzzy systems and practical applications such as digital signal processing, robotics, and flight control. For more information about the symposium, which will be held every three years, contact the Laboratory for International Fuzzy Engineering Research, Yokohama, Japan, 81-45-212-8211, FAX 81-45-212-8255.

—Steven H Leibson

Coprocessor accelerates CAD/CAE applications

Users of PCs based on the 80386DX processor can now boost performance of their CAD/CAE applications packages with a coprocessor chip set designed specifically for engineering applications. The Intel RapidCAD engineering coprocessor chip set replaces the 80386DX CPU and 80387DX coprocessor in your system. The chip set will also work with all 386DX clock frequencies over a variety of bus architectures, including ISA, EISA, and MicroChannel. Performance improvements benchmarked by the company using Autodesk’s AutoCAD Release 11 range from 8% for Redraw, 35% for Regen, and 46% for Hide.

Two chips comprise the set. The first chip fits in the CPU socket and is an 80386 processor with an integral 80387 coprocessor. The second chip fits in the coprocessor socket and provides glue logic for expansion...
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Semicustom array combines analog and digital macrocells

The RLDA80 mixed-signal array from Raytheon Semiconductor combines 32V analog performance with some basic digital functions. A unique feature of the array is that it combines high-voltage operation with precision thin-film resistors. The array's major components include 8 analog gain blocks with matched thin-film resistor blocks, 8 large resistors, 4 medium-power npn transistors, 36 small npn transistors, 12 small pnp transistors, 10 digital input and output cells, 16 D flip-flops, and 18 logic function blocks.

The company provides kit parts and Spice models for prototyping and simulation. The analog macrocells have a frequency-response range of dc to 1 MHz. The digital macrocells have propagation delays typical of LS TTL logic. Thin-film resistors provide 200V isolation from the substrate and 100 ppm/°C typical temperature coefficients. The resistor tolerance is 10% with values as high as 200 kΩ. The array is available in a 44-pin leadless chip carrier in commercial, industrial, and military temperature ranges. Nonrecurring engineering charges start at $30,000 and include layout, ten prototypes, and test development. Minimum order size is $100,000. Delivery is 10 weeks after final design review. Raytheon Semiconductor, Mountain View, CA, (415) 968-9211, FAX (415) 966-7620.

IC ensures clock operation in absence of power

As an inexpensive way to ensure static-RAM (SRAM) data protection and reliable clock operation in the absence of power, the bq4285 real-time clock IC and bq4287 module also let PC designers easily upgrade nonvolatile memory capacity without extensive redesigning. Not only do these clocks eliminate any need for a second battery to protect your static RAM (SRAM) data, they also let you use low-cost commercial SRAMs and improve reliability by protecting the battery from the environmental contaminants associated with board assembly. The lithium cells embedded in these clocks ensure data retention and clock operation for a minimum of 10 years in the absence of power. Including 114 bytes of user RAM for PC BIOS, prices range from $4.38 to $8.40 (1000). Benchmark Microelectronics Inc, Carrollton, TX, (214) 407-0011, FAX (214) 407-9845, contact David Heacock.

Logic-analyzer plug-in handles 102 channels

Hewlett-Packard has tripled the state-analysis speed and quintupled the timing-analysis speed of its 16500A. The 16550A plug-in holds 102 channels. Two plug-ins together make a 204-channel analyzer and you can install five card pairs in one unit. One card pair does 500-MHz timing analysis on 102 channels with 8 kwords of memory or 250-MHz timing analysis on 204 channels with 4 kwords. If you use transitional timing, you cut the maximum timing-analysis speeds in half. Although there are faster timing analyzers, the company claims this unit provides the fastest timing analysis in a unit that also does state analysis. As with earlier units, you can use some channels for timing analysis and others for state analysis and obtain synchronized state and timing displays. The card costs $8800; the mainframe, $7700. Delivery is 4 to 8 weeks, ARO. Hewlett-Packard Co, Colorado Springs, CO, (800) 752-0900.
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Pointing out a few differences

In the article “Vintage filter scheme yields low distortion in new audio designs” (EDN, November 7, 1991, pg 267), I’d like to point out some differences I’ve found.

In simulating Fig 5 (GIC and 2 × Sallen and Key) circuits, the results indicate that the 2 × Sallen and Key filter misses the desired 40-kHz cutoff frequency by 11 kHz and has slight amplitude peaking. Although the GIC (general-immittance-converter) filter meets the desired 40-kHz cutoff without peaking, it achieves only 50-dB stopband attenuation. However, this discrepancy may be due to the OP-42 model limitations. In the simulation, I substituted OP-42 models for the OPA627 and OPA2604 because Spice models for the OPA types were not readily available.

I’ve found that by solving the transfer function of the third-order Sallen and Key lowpass filter with equal resistor values (the 2 × Sallen and Key filter in the article has equal capacitor values), the “greater-than-unity gain to realize the component values” requirement can be eliminated. This solution realizes the unity gain 1 × Sallen and Key filter illustrated in the figure below. PSpice simulations of the design indicate a cutoff frequency of 40 kHz and -80-dB stopband attenuation without any amplitude peaking. The unity gain 1 × Sallen and Key filter also has lower output noise because of the lower gain.

Michael A Wyatt
Senior Engineering Fellow
Honeywell SSO
Clearwater, FL
WHO'S THE LATEST MOVER AND SHAKER IN 4M DRAMs?
The biggest thing to shake the DRAM market is Goldstar's latest entry of a mature second-generation 4 megabit product that is faster, smaller, and lower-powered than the early market entries. The new Goldstar 4M DRAMs are designed and built to meet or exceed the finest Japanese standards while offering all the improvements of a second-generation product. These new products are offered with access times of 60/70/80 nanoseconds in industry-standard 300 mil
26/20-pin SOJ surface-mount packages as well as in 20-pin ZIP, and they are also available with a low standby current rating of 200 µA for battery-supported applications. The devices are provided in two organizations—4M x 1 and 1M x 4—and can also be ordered in 4M x 9 and 1M x 9 (3-chip) modules.

So, if you are looking for high quality, high performance 4M DRAMs for your desktops, portables, laptops and workstations, look to Goldstar.

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The devices in Goldstar’s new generation of dynamic RAMs are provided in two organizations—4,194,304 x 1 and 1,048,576 x 4. These high-performance 4M DRAMs offer Fast Page Mode for high-speed access times as low as 60 nanoseconds. The combination of high performance with the higher density in these new devices has been achieved by the use of submicron design rules and an advanced CMOS process technology.

<table>
<thead>
<tr>
<th>ORG</th>
<th>TYPE NO.</th>
<th>MAX ACCESS TIME (ns)</th>
<th>CURRENT (mA)</th>
<th>FEATURE</th>
<th>PACKAGE (MIL)</th>
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<tr>
<td>4M x 1</td>
<td>GM71C4100A-60</td>
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<td>20 SOJ (500)</td>
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<tr>
<td></td>
<td>GM71C4400A-60</td>
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<td>20 ZIP (400)</td>
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<tr>
<td>1M x 4</td>
<td>GM71C4256A-60</td>
<td>60 110 1</td>
<td>FAST PAGE</td>
<td>20 ZIP (400)</td>
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<tr>
<td></td>
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<td>60 90 1</td>
<td>FAST PAGE</td>
<td>20 ZIP (400)</td>
<td></td>
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<tr>
<td>256K x 4</td>
<td>GM71C4256A-60</td>
<td>60 90 1</td>
<td>FAST PAGE</td>
<td>20 ZIP (400)</td>
<td></td>
</tr>
</tbody>
</table>

With multiplexed address inputs, these new 4 megabit chips fit into the same small packages as the 1 megabit devices, providing the user with four times the DRAM capacity in the same space on a board. The devices are offered in the new industry standard 300 mil SOJ and 400 mil ZIP packages that are compatible with widely available automated testing and insertion equipment.

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overcome the "greater-than-unity gain to realize the component values" problem. He accomplishes this by solving for equal-valued resistors, rather than equal-valued capacitors. Although this approach is valid, it’s much easier to find or fabricate equal-valued capacitors and 1% resistors than the other way around. Given the fact that the Sallen and Key realization suffers from much higher component value sensitivities than the GIC realization, the equal-valued-capacitor approach is the most likely one to be used in a manufacturing environment.

However, there may be realizations of a Sallen and Key filter that don’t require an overall filter gain of greater than unity. Although I couldn’t cover all the possibilities in my article, I picked an example which illustrated my point best: the gain-of-two Sallen and Key filter. Unity-gain active-filter realizations, whether Sallen and Key or some other topology, have always proven to have a higher THD+N than the GIC realization. One hypothesis may be that the noise gain of these circuits is higher than the GIC realization. This result may not be intuitive, because Sallen and Key filters generally have fewer op amps than GIC filters; I leave proving or disproving this hypothesis to someone who has the inclination and time. I used an example with higher gain simply to make this point clear. Wyatt’s unity-gain Sallen and Key has “lower output noise because of the lower gain”; this statement is certainly true compared with the \(2\times\) case, but is it lower than the GIC? I no longer have the lab or test equipment to make bench tests.

Spice models for the OPA2604 and OPA627 are available from Burr-Brown, either on disk or by signing on to their BBS at (602) 741-3978, or from the EDN BBS (617) 558-4241 300/1200/2400/8,N,1. The 50-dB stopband attenuation that Wyatt mentions on the GIC filter is probably an artifact of his model; using the OPA2604, the same 80-dB attenuation is achievable as with the Sallen and Key topology.)

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**Lowpass Components**

<table>
<thead>
<tr>
<th>Model</th>
<th>Passband MHz</th>
<th>Stopband MHz</th>
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<td>8-10</td>
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<td>PLP-10.7</td>
<td>DC-10.7</td>
<td>18-20</td>
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<td>PLP-21.4</td>
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<td>PLP-30</td>
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<td>PLP-200</td>
<td>DC-200</td>
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**Flat Time Delay, dc to 1780MHz**

**Highpass Components**

<table>
<thead>
<tr>
<th>Model</th>
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<td>DC-200</td>
</tr>
<tr>
<td>PHP-500</td>
<td>DC-500</td>
</tr>
</tbody>
</table>

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* Suggested U.S. list price. Optional holster with belt stand available.

The New Series 10. A Small Price For A Fluke.

Fluke and Philips The T&M Alliance

Sparks fly as insulation fails

I have used the ICL7107 3½-digit integrating decimal-output ADC IC for voltage measurement in a circuit that measures insulating materials' dc leakage current, as Fig 1 shows. The circuit works well as long as the insulator under test does not break down. But if a spark is generated across points A and B because the insulation fails when subjected to high voltage, the IC gets damaged, even though the current through the In High and In Low terminals remains well within the maximum permissible limit specified by the manufacturer.

Any capacitor or clamping diode I connect across points C and D does not help. However, if I use the Fig 2 circuit, which has a 10-MΩ resistor (R,) connected between In Low and the sparking points A and B, the IC is not damaged when the insulation fails. This result indicates that the damage in the earlier case may be due to static discharge, but exactly how it is causing damage is not very clear to me.

Could you comment on why the 7107 fails and suggest some solution to avoid this damage? In some other similar application, I may not be able to use a high-value resistor between one of the IC's input terminals and the sparking points.

Sanjay R Chendvankar
Tata Institute of Fundamental Research
Bombay, India

Peter Sharrock of Maxim Integrated Products replies: Much of the circuitry is not shown in your figures, so there could be several failure modes that I haven't identified. However, the solution outlined below should give protection in all the configurations I can think of.

The circuit of Fig 1 has parasitic capacitance between the 7107 circuitry and ground. When the insulation of the device under test breaks down, the voltage applied to In Low falls very rapidly. The parasitic capacitance prevents all of the ADC circuitry from instantly falling in voltage, so the In Low pin sees a momentary multikilovolt insult. This is the most likely cause of failure.

The circuit of Fig 2 has a 10-MΩ resistor between the device under test and the 7107. When the insulation fails, any sudden change in the voltage across the device under test is transmitted to the ADC through the RC network comprising R and the circuit parasitics. The In Low pin of the 7107 does not get exposed to such high voltages, so the part does not fail.

Another equally valid way of protecting the 7107 is to add an extra protection resistor between node D and the In Low pin. This resistor gives good protection in the circuits of both Fig 1 and Fig 2. You could use a value of 10 MΩ to match the 10-MΩ resistor in series with the In High pin. Alternatively, you could try two 4.7-MΩ resistors.

Finding yourself with satellites

Do you know where I can find information regarding the Global Positioning System (GPS)? I've heard a lot about it, and I would like to know what is needed to build a GPS receiver that would tell me exactly where on Earth I am. Up to now, I haven't had any luck finding information or specs on the system.

Javier Perez
Boston, MA

Try the Electronic Proving Ground GPS Range Instrumentation System (EGRIS) BBS at (602) 538-3818, N,8,1 for 300- to 2400-bps modems, or (602) 533-8087 for 9600-bps modems. Two other GPS bulletin-board systems are the US Coast Guard's GPS Information Center at (703) 866-3890, N,8,1 for 300-to 2400-bps modems, (703) 866-3894 for 9600-bps modems; and the US Air Force's Holloman GPS BBS at (505) 349-1525 for all modems. These BBSs provide information about constellation status, almanac data, electronic mail, downloadable files, and user advisories.

Also try GPS World magazine published by Astor Publishing Co, Box 10460, Eugene, OR 97440 USA.

Yet more information about the GPS is available from the Institute of Navigation, 815 15th St, Suite 832, Washington, DC 20005, USA. Phone (202) 783-4121. You can also purchase a 3-volume set of books, Global Positioning System, Volumes 1, 2, and 3, all for $50, from Navtech Books, 2775 S Quincy St, Suite 610, Arlington, VA 22206, USA. Phone (800) 628-0885; (703) 931-0500, FAX (703) 931-0503. The books, which you can also buy separately, provide all of the signal protocols and frequencies that you would need to pick up and decipher GPS information. The books are called "The three little red books" by some GPS users. Navtech Seminars Inc offers courses, seminars, and tutorials about the GPS. Its address and phone are the same as Navtech Books. Have fun.
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CIRCLE NO. 31

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FAST ANSWERS

FLUKE
Where have all the investments gone?

Like most engineers, I took a course in economics when I was an undergraduate. And like most engineers, I’m no expert on economics. But like most people who work in the private sector—and in the US, that’s most people—economics has a profound influence on my life.

Most of the time, I don’t think about economics a whole lot. But at times like this, with the US economy—and probably the world economy—in dire straits, I think about economics more than usual. Sure, a lot of people have their favorite scapegoats for the current economic malaise: Democrats like to blame George Bush and Ronald Reagan. Republicans like to blame the Democrat-controlled Congress. People who don’t identify strongly with either party like to blame the bureaucrats in Washington, the directors of failed S&Ls, the Tax Reform Act of 1986, the budget deficits, the national debt, leveraged buyouts, corporate and private debt, widespread greed, the low savings rate, the reluctance of consumers to spend, bank regulators, bank loan officers, and any number of other vaguely defined entities.

At the moment, I’m not blaming anybody or anything. I do think, though, that it’s time we get answers to some vexing questions—not for the purpose of assessing blame, but in the hope of learning from our mistakes so we can avoid repeating them.

I want to know why, with all the profitable opportunities for investment in this country during the decade just ended, so much investment money went into commercial real estate—for example, to build office buildings that are now sitting empty. In fact, some of these buildings cost so much to leave unoccupied that their owners are razing them.

America’s productive capacity is aging and outdated. Investment in plants and equipment could have greatly improved our competitive position in the world. Investments in R&D could have produced new products and fueled demand. Increased demand would have created jobs and generated profits, which would have provided more investment money and tax revenues. The tax revenues, coupled with even a modest “peace dividend” could have made it possible to rebuild our crumbling infrastructure—things like bridges and roads. Improvements here would have helped to slow or halt the erosion of our competitive position.

So what went wrong? Why are we left with millions and millions of square feet of commercial real estate that, with some luck, we might actually occupy by the turn of the century? And why are our plants and production equipment still outdated, our infrastructure still crumbling, and the money to be spent on developing new products still inadequate? As an engineer, you’re probably just as curious as I am. As an American, you should be curious. And as a engineer with only minimal training in economics, you probably don’t have all the answers or even most of them. But if you have some ideas, we’d like to hear them. Please write to us. Use the mail or the /soapbox Special Interest Group on the EDN BBS. We’ll publish your responses.
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Test and Measurement
Manufacturing products in Europe is one way for companies to avoid import tariffs, and is thus a motivating factor for using a European contract manufacturer. For non-EC (European Community) countries, Europe’s harmonization program offers further inducement, as since 1988, there has been no trade barriers among member states to products manufactured within the community.

More than avoiding tariffs, contract manufacturers say the main demand for their services follows when a company realizes it has to design in surface-mount-technology (SMT) components. The learning curve and capital cost of SMT is enough for many companies to halt in-house manufacture and look for an outside facility.

But using a contract manufacturer does not mean simply unshouldering all responsibility for getting your design produced. You should not expect to avoid being drawn into production issues as your product passes through the contractor’s process.

To obtain the best service from a contractor, you need to re-create with that contractor the relationship you presently have with an in-house production facility. It’s well understood that production inputs to the early phases of a design ensure a smooth passage for the product in the production phase. Equally beneficial is a designer’s involvement with early production runs.

Contractors are keen to work with you in this way and are at pains to express the virtue of this approach. Without this product engineering, you’ll be missing out on a wealth of experience that can make your design cheaper, more producible, and therefore more competitive. Take your contractor’s advice on board, and the likelihood is that your customer will end up with an all-around better product.

Contract manufacturers are scattered throughout Europe, but the major concentration is in France and the United Kingdom. In these two countries, professional associations represent the interests of about 50 member companies. Turnovers of the companies range from 1 to over 100 million dollars. Not every company belongs to an association either—in France alone, estimates suggest approximately 1000 companies exist. The range of services available from contractors doesn’t stop at manufacturing. Procurement of parts and test facilities are also standard offerings. But the key service from a designer’s point of view is product engineering—adjusting the design both electrically and mechanically to make it more producible.

An additional and valuable service that contractors offer is “Europeanizing” a product if its design origin is outside the EC. Often, components specified in a parts list are not available locally, and equivalent types need to be found. As a bonus, if a contractor can build-in enough local cost content to your product, it may qualify as originating in the EC. In this case, your product would be exempt from import tariffs if you export it to countries that have a preference agreement with the EC, such as EFTA (European Free Trade Association) countries and Israel. Rules for determining local content vary, but
generally for electronic products there needs to be a local cost content of greater than 60% of the product's ex-works price. The EC member country's customs offices publish details (Refs 1 and 2).

CEL-CEP (Jouy en Josas, France) is typical of many European contractors in its ability to offer a turnkey manufacturing service. This company can design your pc-boards, subassemblies, and product enclosure. It will product-engineer your circuit design, and purchase all components and parts. Following manufacture, the company can perform in-circuit and functional test of the individual boards. It can assemble to final product level, carry out a burn-in operation, and ship direct to your customer or distributor if need be. Even maintenance and customer-service facilities are available.

Dr Daniel Thauvin, CEL-CEP's sales manager and vice president of a French contractors' professional association, says that although contractors are flexible enough to work on one or all phases of a manufacturing process, they have a preferred way of going about things.

In order for a contractor to do an effective job, the designer needs to provide more than just schematics and parts lists. CEL-CEP likes to have a functional description of the product, with quality and price objectives firmly stated at the outset. Naturally, the designer needs to specify clearly restrictions on choice of components, assembly parameters, and test methods. If a prototype sample is available, that's also useful.

One thing Thauvin emphasizes is the importance of setting up efficient communication between customer and contractor. He suggests both companies nominate one person to transfer information back and forth. Or, on larger projects, for companies to provide a list of specialist staff to answer the range of questions that crop up.

Communication is also an issue to consider when you have no base in the country where you propose to have your product produced. Thauvin explains that when a contractor simply wants large volume production of an existing fully designed product, or there is limited product Europeanizing involved, then a local presence is not essential. But where you intend to use the full range of design and development services, a local customer base is a prerequisite. CEL-CEP does not accept contracts without that arrangement.

Thauvin adds that while open relationships with customers are beneficial, it should be clear what each partner expects of the other. He cautions that at all times, the technical and functional responsibility for the product remains
EUROPEAN CONTRACT MANUFACTURING

Getting the best from contract manufacturers

Establish liaisons with your contract manufacturer as you would with your own production facility:

- ideally involve contractor with your design from the outset
- involve contractor in all mechanical issues
- encourage contractor’s advice on changes to type and value of components
- let your contractor lay out the pc board
- use your contractor to “Europeanize” your design
- use your contractor’s test facilities.

Manufacturers need flexibility

It’s not only large contractors that stress the importance of working in concert with clients. Gerald Willard, technical director of Xpert Systems (Mitcham, UK), and one of many smaller contractors, emphasizes the same point. Xpert prefers you to provide a circuit diagram and a generic components list as a starting point for its service. The company likes to do the pc-board layout and select individual component types for your design. Willard argues this procedure allows flexibility to optimize a product for manufacture. Willard cites the example where for an optimal pc-board layout, a capacitor may need to bridge five pc-board tracks. If you’ve already precisely specified the component as a chip capacitor, that freedom is lost.

In the same way, Willard says adjusting component type or voltage rating to match what Xpert currently uses takes advantage of better quantity pricing on the part. Also, this adjustment may avoid an extra reel on the automatic insertion handler, or avoid changing reels more often.

Willard makes the point that except for eurocards, there are few standards for pc-board size. He says if you know in advance the fixing requirements of insertion, soldering, and test jigs that the contractor uses, you can lay out the pc board accordingly and

Finding a European manufacturing contractor

You can easily locate potential contract manufacturers in France and the UK through trade associations. Both associations publish brochures that list and profile members. The UK association brochure generously lists many nonmembers.

In France, contact Jaques Bayle-Ottenheim
Syndicat National des Entreprises de Sous-Traitance Electronique (SNESE)
11 Rue Hamelin
75783 Paris, Cedex 16, France
(1) 45057053
FAX (1) 45530393
Circle No. 711
In UK, contact Derek Duffert
Association of Contract Electronic Manufacturers (ACEM)
Ramano House
399-401 Strand
London WC2R 0IT, UK
(71) 497-2311
FAX (71) 497-2335
Circle No. 712
ACEM plans a major presence at the Nepcon Electronics show set for March 24 to 26 at the National Exhibition Centre, Birmingham, UK. A contract manufacturing center at the show will provide a dedicated forum for companies to promote their services. For more details, contact Peter Telford in the UK, phone (799) 26699, FAX (799) 26088.

It’s quite likely that special components in your design will not be readily available for your contractor to procure locally. In this case, if you are outside the EC, import tariffs apply when you free issue such parts to your contractor. There are as many different tariff values as there are component types, but generally the figure for electronic parts falls in the range of 5 to 14%. Needless to say, parts such as ASICs are at the high end of that range. On top of this figure, you need to add carriage, insurance, and freight charges, and the cumulative figure for these items is further subject to value added tax (17.5% in the UK). The basis for import-tax figures is a mystery. For example, on finished products such as spectrum analyzers and oscilloscopes the figure is 11%, but for DMMs it’s 10.6%. Whatever figure applies, the information is readily available from customs offices in all European cities and ports. (In the UK, at Her Majesty’s Customs and Excise offices).
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avoid tooling costs for special jigs.

In addition, where you use SMT components, Willard says it's important to consider component placement in relation to the direction of flow during wave soldering. Running IC pins in line with the wave direction, and avoiding component shadowing (placing low-profile parts behind high parts), are typical small details that can have a big effect on how easy your assembly is to produce.

At ACW Technology in Petersfield UK, Operations Director Chris Knowles says with disappointment that only one in ten first-time customers shows an interest in forming a long-term working relationship. He says the situation is improving, but the majority still turn up with a finished pc-board assembly and simply request the best price and delivery. Although ACW, like most contractors, is flexible enough to work this way, Knowles feels that the product suffers by this nonpreferred approach.

Knowles says engineers, in general, do not appreciate the benefits of designing for manufacture. He says any design can benefit from a manufacturer's inputs, and manufacturers are often in the best position to decide such aspects as component types, pc-board construction (single, double, or multilayer), and layout. Knowles advises that when you search for a contract manufacturer to work with, look for a contractor with ideally 10, and no more than 20, main customers. When a contractor tries to support more customers than this level, Knowles believes it's not possible to give adequate attention to the range and extent of design and manufacturing problems that inevitably arise.

References

Article Interest Quotient
(Circle One)
High 482 Medium 483 Low 484

For more information on contract manufacturing in Europe, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their services mentioned in EDN.

For more information . . .

AB Electronic Products
Rogersome
Newport NP1 9AA, UK
(633) 692345
FAX (633) 895755
Circle No. 713

ACW Technology
Hylton Rd
Petersfield GU32 2JY, UK
(730) 66045
Chris Knowles
Circle No. 714

ARS Industries
Z I Arc-lsère
73220 Aiguebelle, France
(9802) 0304
FAX (7936) 4184
J P Vivot
Circle No. 715

Ascom
Ziegelmattstrasse 1
CH-4503 Solothurn, Switzerland
(65) 242424
FAX (65) 224012
Circle No. 716

CEL-CEP
100 Avenue Albert Calmatte
78350 Jouy en Josas, France
(1) 3055-9515
FAX (1) 3055-9060
Anne Le Sayec
Circle No. 717

Datron Electronic
In den Gansackern 10
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FAX 9977-1146
Circle No. 727

System Contact
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67038 Strasbourg, France
8878-2089
FAX 8877-0411
Circle No. 728

Xpert Circuit Assemblies
c/o Philips Components Mitcham
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400 MOPS FOR 6U VMEbus SYSTEMS

This 6U VMEbus board performs 400 million operations per second and is optimized for frequency-domain processing such as FFTs and finite impulse response (FIR) filters using fast convolution. The FDaP features a private 32-bit, 20 MHz high-speed data input/output bus and extensive double buffering for continuous processing of real-time data. An additional 32-bit complex output provides phase/magnitude data. The a66540 is available in 25 MHz and 40 MHz versions. A single 40 MHz version can execute a 1K point FFT in 132.7 µs and a 64K point FFT in 13.1 ms. These times are nearly halved for real input. Multiple FDaPs can be cascaded to achieve almost linear improvement in FFT performance. Plug 400 MOPS into your system by calling array Microsystems' Hotline: 719-540-7999.

CIRCLE NO. 133

CORNERTURN PROVIDES QUANTUM LEAP IN 2D IMAGE PROCESSING PERFORMANCE

The a66554 Cornerturn™ board, used in conjunction with the a66540 FDaP board for real-time two-dimensional image processing, is the first capable of processing an entire 256 x 256 pixel frame of image data in 15.2 milliseconds. This equates to a continuous, real-time rate of 65 frames per second. For 512 x 512 images, the board set transforms images in 71 milliseconds, or 14 frames per second. Designed for medical imaging, radar, sonar, machine vision, and other real-time 2D image processing applications, the board set features performance of 400 MOPS at a clock rate of up to 40 MHz. The Cornerturn accepts 32-bit complex I/O data through 10 MHz double-buffered external I/O connectors or through the VMEbus and stores it in one of four on-board frame store memory buffers. For technical assistance, call array Microsystems' Hotline: 719-540-7999.

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arraysoft™, a complete DSP software development system supporting array Microsystems' a66 Family of Products, provides a menu driven user interface allowing easy access to a suite of powerful development tools at the click of a mouse. This development system features a DaSP/PaC code generator, assembler, disassembler, window generator, full DaSP/PaC program control, on-screen display of data, and board-level diagnostics. For technical information or original program assistance, call array Microsystems' Hotline: 719-540-7999.

CIRCLE NO. 137

THE DaSP/PaC CHIPSET: The heart of the world's fastest DSP product family

The Digital array Signal Processor (DaSP) executes 16 high-level instructions, including FFT butterflies, windowing, complex multiplies, and general-purpose functions. The Programmable array Controller (PaC) manages the entire system, including address generation for the DaSP and memory, and I/O up to 60 MHz. Using a single chip, for example, a 1024 point FFT requires only 12 instructions and can execute in only 131 µs; a complex FIR filter, using 28 instructions, processes at a 2.3 MHz rate. For even higher performance, you can cascade the chipset. Both utilize a 144-pin PGA format and are available in 30 and 40 MHz versions. To receive complete technical information, call array Microsystems' Hotline: 719-540-7999.

CIRCLE NO. 134

PC-FDaP PERFORMS 250 MOPS!

The a66550 Frequency Domain array Processor (FDaP) brings high performance FFT processing to any PC-AT compatible computer. The two board set will fit into two full size PC-AT slots, operate on the 16 bit PC-AT (ISA) bus, and allow real or complex input from either the high speed connectors on the back panel or from the PC-AT bus. The FDaP accommodates an optional complex I-and-Q to magnitude-and-phase converter for post-FFT processing. Available in two memory configurations, the a66550 handles complex FFTs up to 32K points and real FFTs up to 64K points. The a66550 can compute a 1024 point complex FFT in just 210 µs. For complete technical information, call array Microsystems' Hotline: 719-540-7999.

CIRCLE NO. 135

DSP Built For Speed

PC-AT DSP
1K FFT/126µs

DSP engine for the 16-bit PC-AT Industry Standard Architecture (ISA) bus

Performance Benchmarks

<table>
<thead>
<tr>
<th>FFT size</th>
<th>a66550/32K @25MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 Real</td>
<td>7.2 µs</td>
</tr>
<tr>
<td>64 Complex</td>
<td>10.9 µs</td>
</tr>
<tr>
<td>1024 Real</td>
<td>125.9 µs</td>
</tr>
<tr>
<td>1024 Complex</td>
<td>209.9 µs</td>
</tr>
<tr>
<td>32K Real</td>
<td>5.0 µs</td>
</tr>
<tr>
<td>32K Complex</td>
<td>10.49 µs</td>
</tr>
<tr>
<td>64K Real</td>
<td>15.73 µs</td>
</tr>
<tr>
<td>64K Complex</td>
<td>3.64 µs</td>
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</tbody>
</table>

VME DSP
1K FFT/79.6µs

DSP engine for industry-standard VMEbus

Performance Benchmarks

<table>
<thead>
<tr>
<th>FFT size</th>
<th>a66540A @40MHz</th>
<th>a66540A Cascade Sys.</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 Real</td>
<td>2.9 µs</td>
<td></td>
</tr>
<tr>
<td>64 Complex</td>
<td>3.7 µs</td>
<td></td>
</tr>
<tr>
<td>1024 Real</td>
<td>29.6 µs</td>
<td></td>
</tr>
<tr>
<td>1024 Complex</td>
<td>59.1 µs</td>
<td></td>
</tr>
<tr>
<td>32K Real</td>
<td>0.91 ms</td>
<td></td>
</tr>
<tr>
<td>32K Complex</td>
<td>1.82 ms</td>
<td></td>
</tr>
<tr>
<td>64K Real</td>
<td>1.82 ms</td>
<td></td>
</tr>
<tr>
<td>64K Complex</td>
<td>3.64 ms</td>
<td></td>
</tr>
</tbody>
</table>

Call the DSP Hotline: 1-719-540-7999

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CIRCLE NO. 138
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CIRCLE NO. 35
Parameter analyzers based on source-measure units provide flexible and sensitive instruments for characterizing dc circuits.

Parameter analyzers give you a closer look at dc-circuit performance

DOUG CONNER, Technical Editor

When your circuit designs run up against data-book specification limits, it may be time to take a close look at the actual device performance. For digital devices, you often are interested in AC parameters, so you reach for pulse generators, time-interval analyzers, and oscilloscopes to get your answers. For analog components, and even occasionally for digital, you need dc parameter analyzers that can test the performance limits of the components.

Semiconductor device manufacturers perform extensive dc characterization of their devices, and some of that information ends up in the device data sheets. If you need more information, you can try to get it from the device manufacturer or you can make measurements yourself using a parameter analyzer.

Parameter analyzers are also useful for collecting data on real devices for use in creating accurate component simulations (Ref 1). In addition to generating data for simulation, you can test several devices to get a measure of the performance variation among components of the same type. Using the device-variation information, you can predict performance variations in your end product.

Any time you measure device characteristics that are unspecified by the device manufacturer, you must be careful how you use the information. Unspecified characteristics can vary significantly among different lots of parts. If you need a continuing supply of devices with certain characteristics not specified on the device data sheet, you need to work out special arrangements with the device manufacturer.

Parameter analyzers used to measure dc characteristics are typically of two types. The first is the curve tracer, which can test specific characteristics of various semiconductor devices. The sec-

Source-measure units connected to a computer for control and display let you create a parameter analyzer or test system to suit varied requirements. The model 238 from Keithley Instruments offers current to 1A.

EDN February 17, 1992 • 65
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PARAMETER ANALYZERS

Parameter analyzers are a more general-purpose instrument typically built around a source-measure unit (SMU). Four instruments go into an SMU: a voltage source, a voltmeter, a current source, and a current meter. An SMU either sources voltage and measures current or sources current and measures voltage.

For testing a component as simple as a diode, you need only one SMU. A transistor typically requires three SMUs, and an op amp might use four.

Although you could make the same measurements using separate voltage and current meters with voltage and current sources, using SMUs has some advantages. Because an SMU is capable of performing any source or measure function, you can have a general-purpose test setup that tests any type of device without your having to reconfigure the setup. Having all the instruments integrated into one means you only have to deal with one set of accuracy specifications. And a single instrument is often easier to program for automated testing.

Keeping safe compliance limits

Whenever you use a current or voltage source, it will have some compliance range over which it can source current or voltage. The compliance limits should be adjustable (they are on SMUs) to prevent damaging the circuit you are testing.

For example, if you are using an SMU (or any current source) to source current to a circuit, the source will increase the voltage until either the programmed current flows into the device terminal or the current source reaches its compliance limit. While performing a test, you can typically set compliance limits to safe values for the device, then vary the force value.

Similarly, an SMU operating as a voltage source will increase current until it reaches its compliance limit or the programmed voltage level.

Only the instrument operator can set limits to protect a device under test from voltages or currents that will damage it. An SMU, though, at least has some built-in protection from self-damaging situations.

For example, if you are measuring the high-voltage breakdown of a device, you force an increasing voltage until the current flow indicates breakdown. If you've neglected to set a safe compliance level on the current, when breakdown occurs, the current may destroy the device under test. If you are using a separate voltage source and current meter, it's also possible you'll overload the current meter, damaging it or blowing a fuse. SMUs have a higher degree of built-in self protection because the integrated instrument always knows what levels it is sourcing and measuring and what its compliance limits are.

SMUs are able to make extremely sensitive voltage and current measurements (see Table 1). Voltage resolution to microvolts and current resolution to fA (that's femto-amps, $10^{-15}$) requires using Kelvin connections and guard lines (Fig 1).

Kelvin connections, sometimes referred to as 4-wire measure-

Comprising four SMUs integrated into a benchtop instrument, the HP4145B provides programmable data acquisition and display. You can store test setups and data, using the floppy-disk drive, or control the instrument through an IEEE-488 bus interface.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model</th>
<th>Number of SMUs</th>
<th>Voltage range</th>
<th>Current range</th>
<th>Display</th>
<th>Price</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hewlett-Packard</td>
<td>4142B</td>
<td>0 to 8 (modular)</td>
<td>±1000V</td>
<td>±10A</td>
<td>None</td>
<td>$12,000 base</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4145B</td>
<td>4</td>
<td>±100V</td>
<td>100 mA</td>
<td>CRT</td>
<td>$27,500</td>
<td></td>
</tr>
<tr>
<td></td>
<td>236</td>
<td>1</td>
<td>±110V</td>
<td>10 mA</td>
<td>Digital readout</td>
<td>$4990</td>
<td></td>
</tr>
<tr>
<td></td>
<td>237</td>
<td>1</td>
<td>±110V</td>
<td>±110 mA</td>
<td>Digital readout</td>
<td>$6490</td>
<td></td>
</tr>
<tr>
<td></td>
<td>238</td>
<td>1</td>
<td>±110V</td>
<td>10 mA</td>
<td>Digital readout</td>
<td>$8290</td>
<td></td>
</tr>
<tr>
<td>Keithley</td>
<td>370A</td>
<td>NS</td>
<td>2000V</td>
<td>20A</td>
<td>CRT</td>
<td>$20,000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>371A</td>
<td>NS</td>
<td>3000V</td>
<td>100 m/Div</td>
<td>CRT</td>
<td>$25,900</td>
<td></td>
</tr>
<tr>
<td></td>
<td>571</td>
<td>NS</td>
<td>100V</td>
<td>5 mA/Div</td>
<td>CRT</td>
<td>$3190</td>
<td></td>
</tr>
<tr>
<td></td>
<td>577ID-2-177</td>
<td>NS</td>
<td>1600V</td>
<td>5 mA/Div</td>
<td>CRT</td>
<td>$10,395</td>
<td></td>
</tr>
</tbody>
</table>

Note: NS = Not specified.

Finest resolution is not available over full voltage or current range.
PARAMETER ANALYZERS

ments, use separate wires for current flow and sensing voltage. The sense wires connect at precisely the point where you want to force or measure a voltage. Some SMUs can have current levels of several amps, which can easily cause drops of tens of millivolts in the current-carrying wires. The Kelvin connection prevents the voltage drop in the current-carrying wires from affecting the accuracy of the measurement.

Guard lines minimize current leakage from interfering with measurements. The SMU drives the guard line to the same voltage as the sense lines, so little or no current flows between the force, sense, and the guard lines. Because the guard lines surround the force and sense lines, current leakage from the outside is to the guard line and, thus, does not affect the measurements.

Some of the important variations in parameter analyzers are in the voltage and current ranges shown in Table 1. Obviously, you'll need appropriate ranges to cover the circuits you'll be testing. Another significant difference in parameter analyzers is whether you can use the instruments in a stand-alone mode or if you'll need a computer for control and display.

The curve tracers from Tektronix are stand-alone instruments. Although curve tracers do not offer the general-purpose capabilities of parameter analyzers made with SMUs, they do perform important functions in semiconductor parameter analysis.

A key feature favoring curve tracers is their ease of use. You can learn to operate a curve tracer quickly. The ease of operation is partly due to curve tracers' limited flexibility. They almost always offer only a voltage-vs-current display.

Compared with parameter analyzers using SMUs, curve tracers have limited sensitivity. As Table 1 shows, the curve tracers are all several orders of magnitude less sensitive in current measurements than the SMU-based instruments.

Yet curve tracers, especially Tektronix's 371A, have strong high-power testing capabilities. The combination of high current and high voltage allows testing to 3-kW power levels—far higher than any of the SMU-based instruments. The 3000V capability is also higher than for SMU-based parameter analyzers.

The curve tracers let you test devices at high power levels using pulsed-power testing. The periods of high-power pulses are separated by periods of zero power, keeping the average power low and avoiding the need for heat sinking. Some SMU-based parameter analyzers use the pulse-power technique even though power levels are considerably lower. The pulsed-power testing technique helps you avoid thermal effects that can cause device performance to change over the course of a test.

In addition to the curve tracers from Tektronix, the only other instrument in Table 1 that operates stand-alone to produce device performance plots is the HP4145B. The instrument is a fixed configuration.
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Brooktree Corporation, 9950 Barnes Canyon Road, San Diego, CA 92121, (619) 452-7580, FAX (619) 452-7294
of four SMUs in a benchtop unit that handles all control and display functions. The instrument can perform mathematical functions on the acquired data rather than just plot voltage and current values on the screen. For example, you can program the instrument to plot gain vs current for a transistor.

The other parameter analyzer from HP, the 4142B, is a modular unit that requires a separate computer for control and display. Software for the instrument lets you operate it in a benchtop manner similar to the 4145B, although you'll still need a separate computer. With the HP4142B, you can select among four different SMU modules that cover the range of voltages and currents shown in Table 1. The high-voltage module 41422A and the high-current module 41423A are both 2-quadrant units, meaning they can source current only for positive voltages and sink current only for negative voltages.

Another module for the instrument is the analog feedback unit 41425A. The module lets you quickly find the input conditions required for a specific output condition. Typically, using a parameter analyzer, you would sweep through a set of input source levels and record the output measured. The analog feedback unit produces a plot of the input vs output that lets you zero in quickly on the input required for a specific output.

Although technically you’d have to say Keithley’s family of SMUs operates stand alone, in practice you’d want to connect them to a computer, unless all you want to do is make single-point measurements. The 236, 237, and 238 are all single SMUs with different current and voltage limits as shown in Table 1.

The instruments work in an IEEE-488 setup with a minimum of bus traffic. Each SMU can take a 1000-point sweep of data that includes the sourced and measured values, the delay between each measurement, and elapsed time. When using a setup with more than one SMU, you can have each SMU trigger the next in a data sweep. Daisy chaining the triggers lets you limit the required IEEE-488 bus traffic to setting up measurement sweeps and downloading measurements from the SMU at the end of a data sweep. The reduced IEEE-488 bus traffic results in faster data acquisition.

The parameter analyzers using SMUs can record data vs elapsed time to examine characteristics that vary over time. For example, if you are characterizing a capacitor for precision sample-and-hold applications, you need a capacitor with low dielectric adsorption. You can test for dielectric adsorption by forcing a voltage, then forcing zero volts, and finally forcing zero current and measuring the voltage across the capacitor vs time. The capacitor’s memory effect due to dielectric adsorption will cause the voltage to increase over time to some small fraction of the initially forced value.

A simple measurement such as dielectric adsorption shows the general-purpose nature of a parameter analyzer. You don’t need to create any special instrument setup beyond programming the source and measure values. Creating your own test lets you test a capacitor with the voltage levels and time intervals appropriate to your sample-and-hold application. You probably won’t find information that’s so tailored to your needs on a capacitor data sheet.

Curve tracers typically do not provide characteristics vs elapsed time. However, Tektronix’s 370A offers limited characteristics-vs-time measuring capabilities. The 370A uses an envelope mode to show how a semiconductor’s parameters change over time. Using the 370A’s envelope mode is similar to using an envelope mode on a digital storage oscilloscope.

For some test applications, a parameter analyzer may be overkill. If you only need to perform a few parameter-analyzer functions occasionally, you may be able to connect existing instruments to make the measurements. If you find you need to characterize components often, you may want to use a general-purpose parameter analyzer. Don’t overlook the flexibility of SMUs when setting up in-house ATE systems for dc testing.

---

**For more information...**

For more information on the parameter-analyzer products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Address</th>
<th>Phone Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hewlett-Packard Co</td>
<td>19310 Pruneridge Ave, Cupertino, CA 95014</td>
<td>(800) 752-0900 Circle No. 708</td>
</tr>
<tr>
<td>Tektronix</td>
<td>Box 500, Beaverton, OR 97077</td>
<td>(800) 835-9433 Circle No. 709</td>
</tr>
<tr>
<td>Keithley Instruments</td>
<td>28775 Aurora Rd, Cleveland, OH 44139</td>
<td>(216) 248-0400             Circle No. 710</td>
</tr>
</tbody>
</table>

---

**Reference**


**Article Interest Quotient**

(Circle One)

High 479   Medium 480   Low 481
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Keyboard-Controlled Power Supplies at old-fashioned knob prices.

Model DPS 2S-3M
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- Three (volatile) memory locations store configurations
- Programmed active pulldown circuit for fast SLEW from full voltage to zero
- Serial interface RS 232C can drive up to 31 instruments
- Full voltage and current readback through RS 232C

DPS STATIC SPECIFICATIONS

<table>
<thead>
<tr>
<th>Influence Qty</th>
<th>Condition</th>
<th>Output Effects Voltage Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>MIN-MAX</td>
<td>+ (0.02% + 3)mV</td>
</tr>
<tr>
<td>Load</td>
<td>No Load-Full Load</td>
<td>± (0.02% + 3)mV</td>
</tr>
<tr>
<td>Time</td>
<td>0.5-8.5 hours</td>
<td>0.1%</td>
</tr>
<tr>
<td>Temperature</td>
<td>per °C</td>
<td>0.1%</td>
</tr>
<tr>
<td>Ripple &amp; Noise</td>
<td>rms</td>
<td>5mV</td>
</tr>
<tr>
<td>(BW = 20MHz)</td>
<td>p-p</td>
<td>50mV</td>
</tr>
</tbody>
</table>

INTERFACE TABLE

<table>
<thead>
<tr>
<th>Connectors</th>
<th>Control in</th>
<th>PC/AT 9-pin D female</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Control out</td>
<td>PC/AT 9-pin D male</td>
</tr>
<tr>
<td>Levels</td>
<td>—</td>
<td>RS232C standard</td>
</tr>
<tr>
<td>Isolation</td>
<td>—</td>
<td>Optically isolated</td>
</tr>
<tr>
<td>Handshake</td>
<td>Signal</td>
<td>Nil</td>
</tr>
<tr>
<td>Baud rate</td>
<td>DIP switch select</td>
<td>1200, 2400, 4800, 9600</td>
</tr>
<tr>
<td>Word length</td>
<td>—</td>
<td>8 bits</td>
</tr>
<tr>
<td>Parity</td>
<td>—</td>
<td>None</td>
</tr>
<tr>
<td>Stop bit</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>Protocol</td>
<td>KOIB</td>
<td>One std RS232C links up to 31 devices</td>
</tr>
</tbody>
</table>

GENERAL

- Operating temperature: — 0-40°C
- Storage temperature: — -40 to +75°C
- Relative humidity: — 0-95% non condensing
- Shock: — 5g 3 axes
- Vibration: — 2g 10-55Hz 3-axes
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### DPS MODEL TABLE

<table>
<thead>
<tr>
<th>MODEL</th>
<th>d-c OUTPUT HIGH RANGE</th>
<th>d-c OUTPUT LOW RANGE</th>
<th>RESOLUTION</th>
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<tr>
<td></td>
<td>VOLTS</td>
<td>AMPERES</td>
<td>VOLTS</td>
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<tr>
<td>DPS 12.5-6M</td>
<td>0-12.5</td>
<td>0-6</td>
<td>0-6</td>
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<tr>
<td>DPS 25-3M</td>
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<td>0-3</td>
<td>0-9</td>
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<tr>
<td>DPS 40-2M</td>
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<td>0-15</td>
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<td>DPS 125-0.5M</td>
<td>0-125</td>
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### DPS GENERAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>CONDITION</th>
<th>RATING DESCRIPTION</th>
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<tbody>
<tr>
<td>INPUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>a-c Voltage</td>
<td>User selectable</td>
<td>115/230 Va-c ± 10%</td>
</tr>
<tr>
<td>Current</td>
<td>Max load 115Va-c</td>
<td>1.4A</td>
</tr>
<tr>
<td>Fuse</td>
<td>115Va-c</td>
<td>3A</td>
</tr>
<tr>
<td></td>
<td>230Va-c</td>
<td>2A</td>
</tr>
<tr>
<td>Frequency</td>
<td>Range</td>
<td>50-60Hz</td>
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<tr>
<td>OUTPUT</td>
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</tr>
<tr>
<td>d-c output</td>
<td>Microprocessor controlled</td>
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<tr>
<td>Type of stabilizer</td>
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<tr>
<td>Voltage</td>
<td>0 to 40°C</td>
<td>0-100% rating in two ranges</td>
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<tr>
<td>Current</td>
<td>CCP</td>
<td>Current limit mode</td>
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<tr>
<td></td>
<td>OCP</td>
<td>Over current protection disables output</td>
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<tr>
<td></td>
<td>Short circuit protect</td>
<td>Disables output after 10 seconds</td>
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<tr>
<td>Error sense</td>
<td>Drop</td>
<td>0.25V per lead</td>
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<tr>
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<td>Output to ground</td>
<td>400 Vd-c or peak</td>
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<tr>
<td>Leakage current</td>
<td>rms at 110Va-c</td>
<td>50 microamperes</td>
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<td>Output to ground</td>
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</tr>
<tr>
<td>Series connection</td>
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<td>Parallel connection</td>
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<tr>
<td>OVP</td>
<td>Control limit</td>
<td>Voltage stop</td>
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<tr>
<td>Type</td>
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<td>Remote</td>
<td>RS232C</td>
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<tr>
<td>Dynamics (Resistive load)</td>
<td>Rise time</td>
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<td></td>
<td>Fall time</td>
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<td>MECHANICAL</td>
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<tr>
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<td>IEC type</td>
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<tr>
<td>Output connections</td>
<td>Front</td>
<td>Binding posts</td>
</tr>
<tr>
<td>Meters</td>
<td>Two LED</td>
<td>Three digit</td>
</tr>
<tr>
<td></td>
<td>Remote</td>
<td>Talk</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Listen</td>
</tr>
<tr>
<td>Indicators</td>
<td>LED</td>
<td>OPE (output enable)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OCP CCP</td>
</tr>
<tr>
<td>Mounting</td>
<td>19&quot; rack</td>
<td>RA56</td>
</tr>
<tr>
<td>Cooling</td>
<td>—</td>
<td>Convection</td>
</tr>
<tr>
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<td>Outside HxWxD</td>
<td>4.5&quot;x13.1&quot;x8.5&quot;</td>
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<tr>
<td>Panel finish</td>
<td>Fed Std 595</td>
<td>Color 26440, Gray</td>
</tr>
<tr>
<td>Weight</td>
<td>Packed for shipment</td>
<td>14.5lb-6.6Kg</td>
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<tr>
<td></td>
<td>NET</td>
<td>13lb-5.9Kg</td>
</tr>
</tbody>
</table>

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Dimensions in light face type are in inches. dimensions in bold face type are in millimeters.

DIMENSIONS

Dimensions in light face type are in inches. dimensions in bold face type are in millimeters.

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<table>
<thead>
<tr>
<th>Oki Toolset Support for nX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
</tr>
<tr>
<td>Software</td>
</tr>
<tr>
<td>Relocateable Assembler</td>
</tr>
<tr>
<td>Linker</td>
</tr>
<tr>
<td>Librarian</td>
</tr>
<tr>
<td>Symbolic Debugger</td>
</tr>
<tr>
<td>Object Converter</td>
</tr>
<tr>
<td>Object Analyzer</td>
</tr>
<tr>
<td>80C51 Translator</td>
</tr>
<tr>
<td>C-Compiler</td>
</tr>
<tr>
<td>C-Debugger</td>
</tr>
<tr>
<td>Hardware</td>
</tr>
<tr>
<td>OMFICE + EVM65524</td>
</tr>
<tr>
<td>OMFICE + EVM66201</td>
</tr>
<tr>
<td>OMFICE + EVM67620</td>
</tr>
</tbody>
</table>

* Under development
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You'll need a variety of practical skills and tools to tackle high-speed timing problems—even the best timing device presents no magical solution.

Without effective clock management, the benefits of a synchronous digital design break down at high speeds. Driving logic with synchronous clock edges will prevent any number of timing uncertainties, but only if those clocks are truly synchronous. As µP speeds pass 33 MHz and head for 50 MHz and higher, generating and distributing those high-speed clocks becomes a specialty of its own.

This specialty requires diverse skills: knowledge and use of the appropriate parts for clock generation; knowledge of high-speed layout techniques; and the ability to simulate, analyze, and test clock paths (see box, "Simulation spots timing uncertainties"). Acquiring these skills involves paying more attention to details, such as feedback techniques and transmission-line characteristics, once considered to be exclusively analog-circuit design's domain.

These details relate respectively to the two problems of high-speed timing: generation and distribution. In the first

Fig 1—Phase-locked loops are popping up in purely digital designs for two reasons: They can produce multiples of an input clock reference, and they enable you to control the phase difference between that reference and the output. Motorola's MC8891S provides one output at 2X, six at 1X, and one at $\frac{1}{2}$X the input frequency.
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### Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>Whitesmiths</th>
<th>Introl</th>
<th>Archimedes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dhrystone speed</td>
<td>369/sec.</td>
<td>192/sec.</td>
<td>225/sec.</td>
</tr>
<tr>
<td>code size</td>
<td>1691 bytes</td>
<td>1826 bytes</td>
<td>1794 bytes</td>
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<tr>
<td>Sieve speed</td>
<td>715 ms</td>
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<td>169 bytes</td>
<td>153 bytes</td>
<td>164 bytes</td>
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<tr>
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<td>264 μsec.</td>
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<td>450 μsec.</td>
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<td>234 bytes</td>
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<tr>
<td>—Simulation</td>
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<td>IDB</td>
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<tr>
<td>—Evaluation Board</td>
<td>C &amp; ASM</td>
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<tr>
<td>Pentica, Orion,</td>
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<td>No</td>
<td>No</td>
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<td>Nohau</td>
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<tr>
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<tr>
<td>Compiler Price (PC)</td>
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<td>$1295</td>
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**68HC16 Whitesmiths**

<p>| | | | |</p>
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<tr>
<td>—Simulation</td>
<td>CXDB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>—Evaluation Board</td>
<td>C &amp; ASM</td>
<td></td>
<td></td>
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<tr>
<td>—In-Circuit Emulator</td>
<td>EVB16</td>
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<td></td>
</tr>
<tr>
<td>Pentica, Orion,</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nohau</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>In-Line Assembler</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overlaid Local Data Storage</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compiler Price (PC)</td>
<td>$1600</td>
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</tr>
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case, you want to generate multiple copies of a clock signal having fixed relationships to one another. Without interferring with those relationships, you want to distribute these clock copies to various points within a board or an entire system.

On the generator side, specialized clock drivers can produce copies of clock signals with a maximum skew of 0.5 to 1 nsec for TTL- and CMOS-compatible outputs. Also, some state-of-the-art clock drivers contain internal phase-locked loops (PLLs) that, when locked to a clock reference, can provide multiples and fractions of the reference with precise phase-delay characteristics (Fig 1.)

On the distribution side, the judicious use of delay lines can help you adjust a clock signal's characteristics as it travels through the system. However, there's no magic way to get around the fact that high-speed signals require layout techniques that minimize the length of traces and evenly load a clock driver's various outputs. You may also have to incorporate impedance matching and load termination into your layout techniques.

Generating and distributing high-speed signals is tricky whether you're working at the chip, board, or system level. Clocking within an ASIC has its own unique challenge because of the clock tree, or lack thereof, designed in by the vendor. Though not discussed in detail in this article, many ASIC vendors are addressing the issue of timing by either implementing innovative clock trees or by designing on-chip PLLs.

**Acknowledge potential problems**

It's easy to discuss the problems you can have generating and distributing high-speed clock signals. But designing to prevent those problems, and detecting them if they do occur, is not so simple.

Accumulated skew—the difference between the expected and actual arrival time of a signal—eats into set-up-time and hold-time safety margins and can force the system to come dangerously and unreliably close to violating them. Imagine that two leaves on remote branches of your system's clock tree are exchanging data. The clock signal comes from two very different paths with relatively large differences in delay. In this case, skew can amount to an entire clock-to-output delay. This amount of skew results in zero hold time.

Race conditions caused by inadequate set-up and hold times can also force the outputs of latches and registers into a metastable state. Even though semiconductor manufacturers have attempted to deal with the problem of metastability, no device is completely immune to it. The necessity of avoiding metastability compounds the importance of limiting skew.

Unfortunately, timing problems are some of the most elusive. A hold-time violation caused by communication between remote branches may not cause problems all the time or even some of the time. Your design may be working right at the edge of the safety margin without your knowing it. You, and your test equipment, may miss glitches entirely during prototype testing only to have them surface in volume production.

Not only are the problems hard to detect, but they're also sensitive to a number of system conditions: temperature variations, absolute power-supply level and power-
supply noise, and master clock noise and jitter.

All types of skew can accumulate to the point that your system literally operates on borrowed time. The most often quoted rule of thumb says that skew should be at most 10% of the system clock’s period. For a 33-MHz clock, 10% of the period is 3 nsec. For 50 MHz, the number is 2 nsec. Thus, most of the 1-nsec parts in Table 1 would be sufficient to meet the 10% skew specs for these systems.

However, rules of thumb aren’t guarantees. For some systems, the percentage of tolerable skew may be much lower, in which case the available TTL and CMOS clock drivers don’t give you much margin. ECL is about your only choice for skew requirements less than 0.5 nsec. If you have any prejudice against ECL, you may want to take a second look at its benefits for clock distribution (Ref 2).

Many forces, including changing system conditions, work against the timeliness and integrity of high-speed signals. These forces all produce clock skew. Managing the production of that skew is the subject of Clock Management 101.

Various types of skew can affect high-speed timing. Intrinsic skew arises in the generator circuitry; extrinsic skew arises in the distribution circuitry, which includes the receivers and the traces that carry signals to them (Fig 2). Controlling clock skew at the generator is the first step.

### Table 1—Representative clock drivers (buffer and PLL types)

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part</th>
<th>Description</th>
<th>Input/output levels</th>
<th>Maximum skew (nsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated Device Technology Inc</td>
<td>49FCT805/6</td>
<td>Dual, 1-to-5 buffers</td>
<td>TTL/TTL</td>
<td>0.7</td>
</tr>
<tr>
<td>Motorola Inc</td>
<td>MC10/100H640</td>
<td>+2 and +4 buffers for 68030 and 040 µPs</td>
<td>PECL or TTL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>MC10/100H641</td>
<td>1-to-9 clock driver</td>
<td>PECL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>MC74F1803</td>
<td>Quad, D-type invertin flip-flops</td>
<td>TTL/TTL</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>MC10/100E111</td>
<td>1-to-9 differential clock driver</td>
<td>ECL/ECL</td>
<td>0.05</td>
</tr>
<tr>
<td></td>
<td>MC88915FN55</td>
<td>PLL type with 8 outputs</td>
<td>TTL/CMOS or TTL</td>
<td>0.5 (rising edge)</td>
</tr>
<tr>
<td>National Semiconductor Corp</td>
<td>CGS74B2525/ ' 2525</td>
<td>1-to-8 clock buffers</td>
<td>TTL/TTL, CMOS/CMOS, TTL/CMOS</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>CGS74C2526/ ' 2526</td>
<td>2-to-8 clock buffers</td>
<td>CMOS/CMOS, TTL/CMOS</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>F100115</td>
<td>1-to-4 clock buffer</td>
<td>ECL/ECL</td>
<td>0.075</td>
</tr>
<tr>
<td>Silicon Connections Corp</td>
<td>SC3501Q-1</td>
<td>1-to-20, +2, +4, and +8 clock buffers with symmetry adjust</td>
<td>TTL or PECL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>SC3502Q-1</td>
<td>1-to-20 clock dividers</td>
<td>TTL or PECL/TTL</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>SC3505Q-1</td>
<td>1-to-20 clock buffer</td>
<td>TTL or PECL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>SC3507Q-1</td>
<td>1-to-20 clock divider</td>
<td>TTL or PECL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td>Texas Instruments Inc</td>
<td>SN74AS303/4/5</td>
<td>1-to-28 clock dividers</td>
<td>TTL/TTL</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>SN74ABT328</td>
<td>1-to-6 buffer with selectable polarity</td>
<td>TTL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>74AC11204</td>
<td>Hex inverting buffers</td>
<td>CMOS/CMOS</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>5474ACT11208</td>
<td>Dual, 1-to-4 buffers with 3-state outputs</td>
<td>TTL/CMOS</td>
<td>1.0</td>
</tr>
<tr>
<td>Triquint Semiconductor Inc</td>
<td>GA1110E-50</td>
<td>PLL-type 1-to-6 buffer</td>
<td>TTL/TTL</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>GA1210E-50</td>
<td>PLL-type clock doubler</td>
<td>TTL/TTL</td>
<td>0.5</td>
</tr>
</tbody>
</table>

**Notes:** PECL=ECL referenced to 5V. NS=not specified. NA=not applicable.
Standard buffers, such as the '244, don't specify skew on their data sheets. You could arrive at a rough skew figure by taking the difference between the low-to-high and high-to-low propagation delay specifications. However, manufacturers claim this calculation produces vague and overly conservative numbers. Also, these calculations don't provide any information on how skew varies with system conditions.

Skew's importance has increased as speed has increased. So the types of clock buffers in Table 1, which includes both buffer and PLL types, are much more than respecified '244 buffers. The chips listed were designed to minimize internally generated skew. Manufacturers of these clock drivers recognize five different types of intrinsic skew: output-to-output skew; part-to-part or process skew; duty-cycle, pulse, or pin skew; input skew; and limit skew.

Output-to-output skew is the difference between output edges of clock drivers that generate multiple copies from a single input clock. These devices have anywhere from 6 to 20 outputs (Table 1). Currently, the lowest output-to-output skew—the guaranteed maximum—for TTL or CMOS-compatible devices is 0.5 nsec. For ECL devices, the best is around 50 psec.

For those devices with mixtures of inverters and buffers, such as the Texas Instruments SN74A30X family, the skew is the same, 1 nsec,

<table>
<thead>
<tr>
<th>Propagation delay</th>
<th>Output frequency (MHz)</th>
<th>Number of Q outputs</th>
<th>Number of Q outputs</th>
<th>Output drive (I0H, I0L)</th>
<th>Package(s)</th>
<th>Price (100)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.5</td>
<td>NS</td>
<td>5/0</td>
<td>0/5</td>
<td>-24, 64 mA</td>
<td>20-pin DIP, SOIC, LCC</td>
<td>$8</td>
</tr>
<tr>
<td>6.27</td>
<td>66</td>
<td>42, 2, 4</td>
<td>2</td>
<td>-15, 24 mA</td>
<td>28-pin LCC</td>
<td>$15.11</td>
</tr>
<tr>
<td>7.5</td>
<td>35</td>
<td>9</td>
<td>0</td>
<td>-15, 24 mA</td>
<td>28-pin LCC</td>
<td>$15.11</td>
</tr>
<tr>
<td>0.73</td>
<td>600</td>
<td>9 pairs differential</td>
<td>0</td>
<td>NS</td>
<td>28-pin LCC</td>
<td>$30.67</td>
</tr>
<tr>
<td>NS</td>
<td>55/70</td>
<td>5 x 1, 1 x 2, 1 + 2</td>
<td>1 x 1</td>
<td>-36, 36 mA</td>
<td>28-pin LCC</td>
<td>$15.11 / $14.57</td>
</tr>
<tr>
<td>4.8</td>
<td>NS</td>
<td>8</td>
<td>0</td>
<td>-24, 24 mA</td>
<td>14-pin DIP, SOIC, 20-pin LCC</td>
<td>$6.10 / $8.29</td>
</tr>
<tr>
<td>7.8</td>
<td>NS</td>
<td>8</td>
<td>0</td>
<td>-24, 24 mA</td>
<td>16-pin DIP, SOIC, 20-pin LCC</td>
<td>$8.29 / $8.29</td>
</tr>
<tr>
<td>1.2</td>
<td>NS</td>
<td>4 pairs differential</td>
<td>NA</td>
<td>NS</td>
<td>16-pin SOIC</td>
<td>$7.25</td>
</tr>
<tr>
<td>NS</td>
<td>80</td>
<td>10 + 2, 5 x 2 or + 4, 5 + 4 or + 8</td>
<td>0</td>
<td>-24, 24 mA</td>
<td>52-pin QFP</td>
<td>$25</td>
</tr>
<tr>
<td>NS</td>
<td>80</td>
<td>5 x 2, 5 + 2 or + 4</td>
<td>5 + 2, 5 + 2 or + 4</td>
<td>-24, 24 mA</td>
<td>52-pin QFP</td>
<td>$25</td>
</tr>
<tr>
<td>NS</td>
<td>80</td>
<td>20</td>
<td>0</td>
<td>-24, 24 mA</td>
<td>52-pin QFP</td>
<td>$25</td>
</tr>
<tr>
<td>NS</td>
<td>80</td>
<td>10 + 2, 5 x 2 or + 4, 5 + 2 or + 4</td>
<td>0</td>
<td>-24, 24 mA</td>
<td>52-pin QFP</td>
<td>$25</td>
</tr>
<tr>
<td>9</td>
<td>80</td>
<td>8/8/4</td>
<td>2/0/4</td>
<td>-24, 48 mA</td>
<td>15-pin DIP, SOIC</td>
<td>$6.64</td>
</tr>
<tr>
<td>4.8</td>
<td>NS</td>
<td>user selectable</td>
<td>user selectable</td>
<td>-15, 64 mA</td>
<td>16-pin SOIC</td>
<td>$9.13 / $11.62</td>
</tr>
<tr>
<td>5.7</td>
<td>NS</td>
<td>0</td>
<td>6 independent inverters</td>
<td>-24, 24 mA</td>
<td>20-pin DIP, SOIC</td>
<td>$7.05</td>
</tr>
<tr>
<td>10.2</td>
<td>NS</td>
<td>2 groups of 4 of one selected polarity</td>
<td>see left</td>
<td>-24, 24 mA</td>
<td>20-pin DIP, SOIC, chip carrier</td>
<td>$7.47</td>
</tr>
<tr>
<td>1.0</td>
<td>50</td>
<td>6 in user-selected 2-nsec phase-shift increments</td>
<td>see left</td>
<td>-24, 24 mA</td>
<td>16-pin DIP</td>
<td>$33.20</td>
</tr>
<tr>
<td>1.0</td>
<td>100</td>
<td>6 in user-selected buffering, inverting, or doubling configurations</td>
<td>see left</td>
<td>-24, 24 mA</td>
<td>16-pin DIP</td>
<td>$37.40</td>
</tr>
</tbody>
</table>
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within the groups of $Q$ and $\bar{Q}$ outputs. However, the skew across the $Q$ and $\bar{Q}$ outputs can be as high as 2 nsec.

Part-to-part or process skew is the difference in output skew across different packages of the same device. Tight part-to-part specs are difficult to achieve, and you can see from Table 1 that they are always worse than the output-to-output specs. Also, many manufacturers don't test for or guarantee any part-to-part numbers. Thus, depending on how many copies of the clock you need, you should either attempt to choose one driver for them all, such as one of Silicon Connections' 20-output devices, or use individual drivers for various branches of a clock tree.

For those applications that require clock duty cycles very close to 50%, duty-cycle skew is an important parameter. Duty-cycle skew is the difference between low-to-high and high-to-low propagation-delay times when a single input causes one or more outputs to switch.

As Table 1 reflects, most manufacturers don't routinely include duty-cycle skew specifications for all their devices. For its 1-input to 20-output drivers, Silicon Connections specifies that at a threshold voltage of 1.5V the maximum asymmetry between high-to-low and low-to-high transitions is $\pm 0.25$ nsec. Just as with the output-to-output specs, these numbers apply only within certain output groupings. Some of the company's devices also feature a symmetry adjustment. Using three inputs, you can move the output edge of the SC3501 in 0.25-nsec increments from $+0.75$ to $-0.75$ nsec.

Two skews go unspecified

The final two types of skew are rarely specified and aren't as relevant as the previous types. Input skew pertains to multiple input devices and is the difference between any two propagation-delay times that originate at different inputs and terminate at a single output. Limit skew is the calculated difference between the maximum specified values of either low-to-high or high-to-low propagation delay and the minimum values of the same. This calculated number can tell you how much the propagation delay varies due to change in supply voltage, temperature, output load, and other operating conditions.

Of all of these types of skew, the data sheets at best specify the first three. When specified, the skew numbers for different parts don't cover the same performance range, which varies from manufacturer to manufacturer. So even having the specifications available doesn't guarantee that you can compare parts easily.

Some of the specs cover the entire operating temperature range of the part. Others are only true at 25°C. Also, manufacturers derive certain specifications from tested results while deriving others from calculated or simulated results. National Semiconductor is one manufacturer that provides extensive test data, such as that in Fig 3, to show the performance of their devices as parameters such as output frequency and capacitance change.

Just as the data sheets aren't standardized, neither are the parts themselves. These drivers don't come in any standard package or pinout. Some have center power and ground pins. The drivers' numbers of outputs and their configuration, whether buffered, inverted, or both, varies. Some of the devices can accept positive ECL (PECL) signals, (ECL signals referenced to 5V). Others have TTL-compatible inputs with CMOS-compatible outputs.

PLL types lock on

Most so-called clock drivers can produce copies or divided-down versions of an input clock. But they do not give you control over the delay through the device. On the other hand, those drivers with internal PLLs can produce multiples of the input clock and give you some control of the phase difference between input and output. Motorola and Triquint Semiconductor are currently the only manufacturers of PLL-type clock drivers. However, Texas Instruments is currently designing a PLL device that should be available in the first half of this year.

PLL-type clock drivers are useful for two primary reasons: to multiply the input clock and to phase-
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advance or retard the output in relation to the reference input. For example, using select pins and external feedback, you can phase-adjust the outputs of the GA1110E in ±2-nsec increments. The GA1210E produces multiple copies at 2× the input frequency. Because of feedback, PLL-based drivers can compensate for process, temperature, and voltage variations by always locking the output of each part to the common input reference clock.

The standard PLL contains a phase detector, voltage-controlled oscillator (VCO), and a loop filter, and can include a frequency detector (Fig 1). The free-running frequency of the VCO is usually much higher than the output frequency, which allows the parts to generate various multiples of the input frequency. The internal VCOs in Triquint Semiconductor’s GA1110 and 1210 run at 500 MHz, but the device’s outputs are set for output frequencies of 25, 33, 40, and 50 MHz.

The loop filters of these PLL-based drivers may require external components. The loop filters of the GA1110 and 1210 are on chip, whereas Motorola’s MC88915 requires an external RLC network of six passive components. Requiring an external loop filter does have one advantage—it provides the PLL with a wide frequency range. While the free-running outputs of the Triquint parts are set to specific output frequencies, the 70-MHz version of the MC88915 can lock onto an input that ranges anywhere from 10 to 35 MHz.

As versatile and useful as the PLL-based devices are, they have their own unique performance quirks. Any phase-locked system

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requires a finite time to reach the locked condition. The time required for the GA1101 and GA1210 to acquire lock is typically 200 µsec and maximally 500 µsec. The typical wait for resynchronization in a 33-MHz system would then be 6600 cycles. Texas Instruments' SN74ABT338 requires a minimum of 50 µsec. Motorola's MC88915 takes a minimum of 1 ms and a maximum of 10 ms.

These numbers are fractions of the normal start-up times required by the clock oscillator. Thus, from start up, the time required for lock doesn't require any waiting, since you're already waiting for the oscillator. However, if the path from the system clock and the device is interrupted for any reason—without the clock source itself losing power—once the clock signal returns, you can't expect any precise relationship between input and output until the chip itself reestablishes lock.

Distribute without adding skew

Generating multiple clock-signal copies with low skew solves just half of the timing problem. Extrinsic skew can accumulate during distribution due to trace-length differences, loading differences, or because the clock signal's waveform has been corrupted. Layout techniques that evenly load all of the outputs of one clock driver, by matching trace lengths for example, are another step toward minimizing extrinsic skew. Some parts, such as delay lines, do exist that help correct for distribution effects by allowing you to de-skew multiple channels of a shared clock (Ref 3). Analog Devices and Brooktree both make delay lines primarily for the ATE industry that are applicable to many high-speed systems. For exacting timing requirements, Brooktree's Bt622 dual and Bt624 quad delay lines ($32 and $43, respectively, (100)) allow you to adjust both the delay and the width of high-speed ECL pulses. These devices let you compensate for differences in positive-vs-negative-going signal delays.

Adjustable delay lines are more useful than those with fixed delays at their tap points because you can use one device to cover a variety of delay times. The CMOS Bt630's ($11.10 (100)) five tap points at 20, 40, 60, 80, and 100% of the full-scale delay are adjustable over a 25- to 400-nsec full-scale range. Analog Devices' ECL AD9500 ($16 (100)) and TTL- and CMOS-compatible 9501 ($8.60 (100)) are digitally programmable delay generators with resolutions as small as 10 psec and a delay range of 2.5 nsec to 10 µsec full-scale range.

All specialized timing devices can help you generate and distribute high-speed clock signals more effectively. However, every high-speed design and every high-speed layout is unique: No one device works in every situation. High-speed timing problems can only be averted by the combination of part selection, layout, simulation, and thorough test.

References


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The module speeds your processor's access to its DRAM in a variety of ways. For example, the module uses a first-in, first-out (FIFO) buffer to store as many as 16 words coming in from the processor. The buffer allows the module to accept burst writes at the processor's speed, independent of the DRAM's speed or refresh status. The buffer also allows the module to offer a posted write, temporarily holding the data until the processor has completed a read operation, then writing the data to DRAM. The posted write allows the processor to swap cache lines without waiting for the DRAM write cycles to complete.

The module speeds read access by using as many as four banks of memory and multiplexing the data to the processor. When the processor addresses one DRAM word, the module reads from all the banks simultaneously, pipelining the data so that subsequent sequential read operations are independent of the DRAM's timing.

The module handles all DRAM control while maintaining a straight-forward interface to your processor. This interface is programmable to adapt to a variety of 32-bit processors, including SPARC, i486, i5860, 68040, and 88110. For example, the interface can handle either multiplexed or separate data and address buses. You can also set the module's bus acknowledge signal timing, choose big- or little-endian byte ordering, set the length and sequencing of burst accesses, and choose bus parity.

The module's system interface also supports multiprocessor configurations. It allows processors with snooping cache controllers to inhibit read or write operations initiated by another processor. The inhibited operation can then be redirected to account for differences between the DRAM's data and data stored in the various processor caches.

For example, the snooping processor would inhibit a read operation if its cache contained the requested data and the DRAM data was not current. The snooping processor would then supply the requested data in place of the DRAM. A command line on the module also allows the inhibited read to become a reflective read. A reflective read requires the module to capture the processor-to-processor data transfer and update the DRAM when the transfer is complete.

The module's DRAM interface handles all DRAM addressing and refresh operations, supporting DRAM arrays as large as 1 Gbyte with speeds as fast as 80 nsec. The
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DRAM array can have as many as four blocks of memory, each as deep as 16 Mbits. Each block has four banks of memory with 32 data bits and 7 check bits. The module’s address timing is programmable, allowing you to use 256-kbit-, 1-Mbit-, 2-Mbit-, or 4-Mbit-deep devices. The DRAM interface timing is synchronous, deriving from a frequency-multiplied version of the system clock generated by the module’s phase-locked loop.

Large banks of memory increase the opportunity for soft errors to creep into your data. To help maintain data integrity, the module offers two error-handling features.

It has built-in error-detection-and-correction (EDC) circuitry that operates on 32 bits at a time. The module has four EDC circuits, one for each bank. The circuits can detect a 2-bit error and correct a 1-bit error as the data is transferred from the DRAM to the processor. The module keeps an internal FIFO log of any errors detected and can generate a system interrupt when an error occurs.

Automatic data scrubbing allows the module to check for errors on all four banks simultaneously, as it refreshes each block of memory. If it detects a correctable error, the module changes the DRAM refresh cycle to a read-modify-write cycle, then corrects the corrupted data. The module can scrub a 1-Gbyte array every 15 minutes.

The CYM7232 module comes in a 400-pin pin-grid array that measures 2.8 in. square. Samples will be available in March at a cost of $327 (100).—Richard A Quinnell

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μP/peripheral-function building blocks speed system-design tasks

Having a library of microprocessors and peripheral functions allows you to design complex ASICs quickly, much as you'd build a breadboard. The Coreware library contains three groups of building blocks: 16- and 32-bit microprocessors, floating-point processors, and peripheral functions.

Several ASIC-vendor libraries contain 4-, 8-, and 16-bit microprocessor cores. One ASIC vendor, VLSI Technology, offers a core of its Acorn 32-bit RISC (reduced-instruction-set-computer) processor. LSI Logic's Coreware library offers familiar 32-bit RISC cores that allow you to customize designs by tailoring the cache or peripherals to meet your application's special needs. These building blocks are high-speed, standard components with existing software bases and large installations of native hosts.

At introduction, the library contains embedded SPARC and MIPS microprocessor cores and a 1750A 16-bit processor core. Among the range of pipelined and nonpipelined IEEE-754-compliant floating-point units are 32- and 64-bit ALUs and multipliers as well as a pipelined 32-bit divider. Initially, peripheral functions are limited to a SCSI-1 controller, a generic multiprocessor bus interface, an SBus DMA controller, and a MIPS read-write buffer. JPEG (Joint Photographic Experts Group) Image Compression, a Reed-Solomon Codec, and the MIPS integrated FPU/CPU functions are currently in the works.

Each function block, like ASIC primitives, consists of a schematic representation and a gate-level simulation model in LSI Logic's proprietary format. In addition, the function blocks also offer behavioral-level simulation models. These C-code models are kept in an intermediate format that the vendor can translate to VHDL (VHSIC Hardware Description Language), Verilog, and its own behavioral-simulation language.

In addition, the function blocks feature existing test vectors. These vectors allow the vendor to perform comprehensive in-circuit manufacturing tests on each of the blocks. The test method that each pattern uses varies depending on the particular functional blocks; the embedded SPARC module uses an internal scan chain whereas the embedded MIPS module uses parallel-input vectors that require you to provide pin access to the block's borders. These tests reduce your design responsibility to just providing observation and control of nodes within the random logic and non-Coreware library functional blocks.

The roughly 20,000-gate embedded SPARC core is a bare-bones processor. The core is based on the early SPARC instruction set; it doesn't perform direct multiplication or division. In addition, the core offers no floating-point coprocessor interface and requires two memory cycles for load instructions. The core, which runs at 20 MHz, does provide on-chip cache support or offers an interface to off-chip cache.

The MIPS family is represented by two core processors, which can run at 25, 33, and 40 MHz. Both the roughly 35,000-gate embedded core and the 25,000-gate CPU are fully static designs that implement most of the MIPS I instruction set. Using 1-μm fabrication, you can surround the core with approximately 65,000 gates of additional logic. The embedded core provides a 4- or 8-kbyte instruction cache, an optional data cache, a DRAM (dynamic RAM) controller, a bus-interface unit, and three counter/timers.

A direct data-bus interface bypasses the bus-interface unit and provides single-cycle data transfers between the embedded CPU and dedicated on-chip static RAM or ROM. The cores offer provisions for DMA, although they sacrifice co-processor support, a memory-management unit, and translation look-aside buffers (TLBs). Without the TLB registers, the CPUs don't offer instructions to manipulate them; if your code contains them, these instructions will cause exceptions.

Pricing depends on several factors, including the core, volume, and design requirements. The access fee, which includes function-block royalties, starts at $30,000. This fee supplements the nonrecurring engineering cost, which starts at $30,000. If your needs require it, the vendor will actively participate in the design. —Michael C Markowitz

LSI Logic Corp, MIS D102, 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 954-4875.

Circle No. 731

Low-cost package links 68HC16 to PC

Debugging critical code for an embedded μC is a bit easier with Motorola's ICD16 debugging tool for the 16-bit 68HC16 microcontroller (μC). This tool links a PC host computer to a 68HC16 target system. The ICD16 module plugs into a PC parallel port. Using the module, users can directly control μC target code's execution.

The ICD16 takes advantage of the background mode, which Motorola added for on-target debug-
In background mode, normal processor execution is halted and an external host can control the processor via eight control pins. In background mode, a remote user can interrogate or set register or memory values as well as set breakpoints. When execution hits a breakpoint, processor execution halts and control passes to background mode.

Unlike an ICE (in-circuit emulator), the debug tool requires some board space for wiring and a 10-pin header. In addition, the ICD16 operation is intrusive: Debugging affects code execution. The ICD16 uses processor resources, mainly execution time, to execute breakpoints, retrieve and set memory or register values, and communicate with the host PC. However, once you set a breakpoint, you can monitor execution in real time until the code hits it and breaks.

In contrast, ICEs are mainly non-intrusive. They collect trace data in separate buffers, not affecting performance until the trace buffer is full. A breakpoint will, of course, stop execution. The ICD16 approach is less intrusive than that of using a monitor—a small debug kernel, which takes up memory and processor resources. In addition, the ICD16 does not need to use the µC's serial port to link to a host; it uses special pins. You could actually run a monitor—linked via a serial port—and the ICD16 simultaneously, because they don't share link resources.

You can debug 68HC16 target code without an ICE. To monitor and control execution, the ICD16 links to the target µC via background mode.

The ICD16 package consists of the module, a target cable, and debugging software. The software is a more advanced version of the integrated assembler furnished with Motorola's 68HC16 evaluation board. This version provides a windowed development environment, which integrates a macroassembler, an editor, and a source-code debugger with a host-to-target communications link.

The source-code debugger enables you to debug target code at the source level (C or assembly). It adds performance monitoring (address reference counts), macroscripts, a dumb terminal window, file verification, and interrogation of the 68HC16 multiply-and-accumulate unit. P&E Microsystems Inc (Woburn, MA) developed the core software for Motorola.

The ICD16 supplements Motorola's 68HC16 evaluation board; initially, you can work the 68HC16 with the evaluation board, and then use the ICD16 to debug target boards. You could also bypass the evaluation board and use the ICD16 with a simple target configuration.

The ICD16 costs $99. The 68HC16 evaluation board costs $168 during the first quarter of 1992; the standard evaluation-board price will be $320 thereafter.—Ray Weiss
Motorola Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 440-2000. Circle No. 732

32-bit µC integrates SPARC with embedded peripherals

Fujitsu's 32-bit SPARClite MB86931 integrates the SPARC RISC (reduced-instruction-set-computer) architecture with a set of µC peripherals tailored for embedded processing. The SPARClite "event processor" handles real-time events. The chip integrates the SPARC integer processor with 2 kbytes each of on-chip instruction and data cache, an interrupt controller, counter/timers for monitoring external events, and a dynamic-RAM controller.

To increase execution speed,
Eliminate +5V RS-232, Use 1/2 the Power and Meet the New EIA/TIA-562 Requirements

- Guaranteed Operation Down to 3.0V
- 4 Drivers, 5 Receivers
- Meets New EIA/TIA-562 Standards
- 1µF External Capacitors
- Guaranteed RS-232 Compatibility*
- 1µA Shutdown Mode

Maxim's new MAX561 is the first device to implement the new EIA/TIA-562 standard that guarantees operation with output voltages as low as ±3.7V. The MAX561 consumes 1/2 the power of +5V RS-232 and operates from a 3.3V power supply. And, as stated in its forward, EIA/TIA-562 "allows for electrical interoperation with equipment designed to conform to EIA/TIA-232D interfaces."

Choose a +3.3V Transceiver and Save Power

<table>
<thead>
<tr>
<th>Quiescent Current</th>
<th>8mA</th>
<th>15mA</th>
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<tr>
<td>Data Rate</td>
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<td>Receiver Input Voltage, Max</td>
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<td>Ty Load Impedance</td>
<td>3kΩ to 7kΩ</td>
<td>3kΩ to 7kΩ</td>
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<tr>
<td>Rx Input Resistance</td>
<td>3kΩ to 7kΩ</td>
<td>3kΩ to 7kΩ</td>
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<tr>
<td>Instantaneous Slew Rate</td>
<td>&lt;30V/µs</td>
<td>&lt;30V/µs</td>
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Fujitsu added instructions to the original SPARC instruction set: an integer multiply instruction and a divide step instruction, as well as a bit-scan instruction that looks for the first nonsign bit. This bit-scan instruction helps in processing bit maps.

In addition, the chip is a fully static design. SPARClite cleans up a number of problems of earlier SPARC implementations. For example, loads and store are typically one instruction cycle, compared with two and three cycles for earlier SPARC CPUs. Some of these speed-ups are a result of a Harvard architecture with divided dual instruction and data caches, unlike Sun SPARC's single unified cache.

Also, this family has on-chip hooks for embedded system test and built-in, in-circuit-emulator/monitor support. The processor has six breakpoint registers. To monitor code execution, users can set two instruction, two data-value, and two data-address breakpoints.

The chip has small on-chip caches. These 2-kbyte caches are generally effective if inner loops fit into the caches. Cache entries can be locked in, enabling critical code to be kept in the 2-way set associative caches for continuous processing. The CPU doesn't wait for the 2-word cache line to be filled from external memory: The first word is used without waiting for the second.—Ray Weiss

Fujitsu Microelectronics Inc, Advanced Products Div, 77 Rio Robles, San Jose, CA 95134. Phone (408) 922-9000. FAX (408) 943-9293. Circle No. 733

8-bit μC handles power and keyboard management

L

aptop power-management and control functions are becoming a major application area. Signetics 80C550 microcontroller (μC) is an 8051 derivative that combines key laptop functions: power management and keyboard control. The 8-bit μC crams the 8051 architecture (with 30 I/O pins and A/D converter) into a 40-pin DIP or 44-lead PLCC (plastic leaded chip carrier). This chip fills a gap in the 8051 world: It supplies enough peripherals to handle power management and provides the I/Os and program-

80/83/87C550

Clock . . . . . . . . . . . . 3.5 to 16 MHz
Program . . . . . . . . . . . 4 kbytes ROM/EPROM
Data . . . . . . . . . . . . . 128-byte RAM
I/Os . . . . . . . . . . . . . . 30/32 pins
Interrupts . . . . . . . . . 2 external
Special . . . . . . . . 8 channel, 8-bit ADC
Package types . . . . . 40-pin DIP, 44-lead plastic leaded chip carrier or quad flatpack
Price . . . . . . . . . . . . . . $4.60 DIP ROM (10,000)
$17.83 one-time-programmable

Power-management design kit

Today, laptops are hot and laptops require power management. The Signetics design kit lets engineers design in 80C752/550 μCs for laptop power management.

The kit consists of an application note, which defines the design; a schematic of the complete design; and the application source code.

Using this kit, you can modify the design for your own needs or use it to understand a power-management application. This baseline design saves time by providing an easy-to-understand base to start from. The kit defines a Signetics optimizer board that monitors power. It controls the system frequency generator for clocks and the system-memory, dynamic-RAM-refresh cycles. Keyboard and peripheral activity drives the state machine that controls power management.

An on-chip A/D converter monitors the system battery level and VCC. The optimizer drives the clock-frequency generator and controls the system-refresh generator. Six operational modes include full power; doze, when the clock rate is halved; shutdown, when power to specific peripherals is turned off; shutdown-doze; sleep, when power is removed from display backlight and LCD regulator; suspend, when the μC takes over memory refresh task and removes power from the rest of the system; and off, when all power is turned off.

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  - 150mA @ 12V (MAX732, VIN > 4.5V)
  - 100mA @ 15V (MAX733, VIN > 4.5V)
- Regulates From Low Input Voltage:
  - 2.5V & Up (MAX731/MAX752)
  - 4.0V & Up (MAX732/MAX733)
- Logic-Controlled 6µA Shutdown
- 8-Pin DIP & 16-Pin SOIC

### Evaluation Kits

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<tr>
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<td>2.5V to 4.65V</td>
<td>+5V</td>
<td>200mA</td>
<td>85%-90%</td>
<td>$3.20</td>
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<tr>
<td>MAX732</td>
<td>4V to 9.3V</td>
<td>+12V</td>
<td>200mA</td>
<td>85%-95%</td>
<td>$2.60</td>
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<tr>
<td>MAX733</td>
<td>4V to 11V</td>
<td>+15V</td>
<td>125mA</td>
<td>85%-95%</td>
<td>$2.60</td>
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<tr>
<td>MAX752</td>
<td>2.5V to 15V</td>
<td>Adjustable</td>
<td>2.7V to 15.75V</td>
<td>85%-95%</td>
<td>$3.20</td>
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### Specifications

- **Input Output Power**
  - 1 Watt of 5V Logic input from a 3V digital supply

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has standard 8051 idle and power-down modes for power saving. In idle mode the CPU shuts down, but selected peripherals continue to operate. In power-down mode, the entire µC shuts down. An interrupt or reset will resume µC operations.

The chip runs at 16 MHz. Its power-supply current is 35 mA for active mode, which drops to 6 mA in idle mode and falls to 50 µA in power-down mode.—Ray Weiss

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000. FAX (408) 991-2311.

µC combines small pinout, power management, application protection

Designing controllers for low-cost appliances and industrial controllers is a tough compromise among low cost, multiple functions, and safety. National Semiconductor's 8-bit COP820CJ microcontroller (µC) can take a little of the pain out of appliance design. It combines a 1-µsec CPU core with power management, brownout detection, direct display drive, A/D conversion, pulse generation for motor or sound generation, and multiple timers.

The µC is built around the National COP800 CPU core. This core is an accumulator-based implementation (six registers), with 1-kbyte program ROM and 64 bytes of data RAM. This µC is designed for low-end appliance applications such as toasters, coffee makers, vacuum cleaners, and food processors. These applications require fail-proof safety, moderate program capability, multiple hardware interfaces, and power management.

Safety features are built in to the µC. Brownout, power failure, infinite software loops, and other error conditions will automatically force a CPU reset. To save power, a hold mode drops power consumption in the static device from 8 mA at a 10-MHz clock to 10 µA.

A brownout-protection circuit monitors \( V_{cc} \) and automatically resets the µC when the power level falls below 3V. It also detects transients with pulse widths of 70 nsec or greater. On a transient fault, the µC will stop CPU execution, returning to normal-mode operation when the transient ends. Detection circuitry saves designers from building external, discrete protection circuitry.

The µC responds to multiple external events. Eight of the I/O lines can be edge programmed to wake the processor from halt mode. Like other interrupts, the wake-up forces the CPU into a power-up or reset condition to start processing.

This controller has three timers. The 8-bit programmable watchdog timer has a divide-by-256 prescaler and can detect runaway software. The 8-bit PWM timer enables code to generate high-frequency pulses, including variable duty-cycle pulses (PWM) for motors or other electronic control.

The third timer is a 16-bit general timer/counter with a load/compare register. This counter counts down, once per instruction cycle. On underflow, it generates a pulse for output or for interrupting the CPU. At the same time, it loads from the load/capture register. The counter can be programmed as an event counter, counting down for external signal pulse (500 kHz max). It can also serve as an input timer, counting down until an external signal triggers, whereupon the current count is saved to the load/compare register.

Smart appliances can be controlled with a single low-end, 8-bit µC, the COP820CJ. In a 20-pin DIP, the chip supports small displays, motor control, power management, and user appliance control.
SMAU. +5V & ADJUSTABLE DC-DCs HAVE 94% EFFICIENCY!

No Design Required for Guaranteed 300mA (1.5W) or 750mA (3.75W) Outputs

The new MAX730/MAX738 and MAX750/MAX758 step-down switching regulators are compact and simple solutions for battery-powered portable applications. They extend battery life by providing 85% to 95% efficient step-down regulation. Pre-selected components simplify design work and the standard application circuit delivers the guaranteed power over all specified line, load, and temperature conditions. High-frequency 160kHz pulse-width modulation (PWM) current-mode control provides low-noise operation and reduces output ripple to less than 50mVp-p.

- Evaluation Kits – SOIC and DIP*
- Guaranteed Output Current:
  - 750mA for VIN > 10.2V (MAX738/MAX758)
  - 300mA for VIN > 6.0V (MAX730/MAX750)
- Regulates From Low Input Voltage:
  - +5.2V to +11.0V (MAX730/MAX750)
  - +6.0V to +16.0V (MAX738/MAX758)
- Logic-Controlled 6µA Shutdown
- Adj. Output: 1.25V to VIN (MAX750/MAX758)
  - Fixed Output: +5V ± 5% (MAX730/MAX738)
- Space-Saving Footprint:
  - 8-Pin SOIC and 8-Pin DIP (MAX730/MAX750)
  - 16-Pin SOIC and 8-Pin DIP (MAX738/MAX758)

Evaluation Kits* Reduce Design Cycle & Provide Immediate Results

Surface-mount and through-hole kits are available for all four products, and contain a PC board and all external components, including inductor.*

The MAX730/MAX738 evaluation kit has all the components needed to build a complete +5V step-down circuit.

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The COP820CJ doesn’t have a full A/D converter. Instead, it has an analog comparator to test external voltages. With the proper program, you can use the comparator to build a single- or dual-slope A/D converter.

In addition, the µC supports as many as 24 I/Os. These I/Os comprise a 4-bit output port, a 4-bit input port, and two 8-bit programmable ports. The programmable-port pins can be set at a high-impedance input (weak pull-up) or a push-pull output. Four of the programmable pins can directly drive LEDs with as much as 15 mA. The 16-pin DIPs or SOICs have only 12 I/Os.

—Ray Weiss
National Semiconductor Corp,
2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 721-5000. FAX (408) 730-0764.

μC and software kit tames Appletalk

PCs and workstations can now take advantage of the Appletalk network for desktops and offices. Zilog is releasing a design kit for the two lower layers of the 6-layer Appletalk protocol. With this kit, developers can link peripherals and systems using the Appletalk network. The Appletalk protocol transfers data at 230.4-kbits/sec.

The kit implements the toughest part of the Appletalk protocol, the data-link level—the Local Talk Link Access Protocol (LLAP). The Local Talk protocol is implemented as an assembly-language program running on the Zilog Z80181, an 8-bit microcontroller (µC) for communications processing.

The remaining higher levels of the Appletalk protocol are less timing and processor dependent. They can be implemented on a back-end or host CPU: The Z80181 serves as a front-end communications processor, buffering packets for transmission or for passing back to the host. However, the Z80181 has enough headroom for the complete protocol. It can address as much as 1 Mbyte, and the LLAP implementation takes up only 5 kbytes.

The LLAP supports node-to-node transmission and receipt of data and control packets. Because of tight signal-timing and synchronization constraints, this transmission is the most difficult part of Appletalk to implement. LLAP is a CSMA/CA (carrier-sense multiple-access and collision-avoidance) protocol with synchronous pulse generation and frame transmission and reception for each node.

The software kit includes assembly source code for the first two layers of the Appletalk protocol, a hardware evaluation board with a 10-MHz Z80181 µC, the LLAP driver in an 8-kbyte EPROM, 8 kbytes of static RAM (SRAM) for additional user programs, RS-422 drivers, and a DIN-8 LLAP connection module. For PC-host-based debugging, the kit provides a debug monitor and a terminal emulator.

The Local Talk implementation of the physical layer uses an SDLC (synchronous data-link control) frame format with FMO bit encoding (checks for bit transition on line) and RS-422 as a physical medium with a differential driver and 3-state signals.

Appletalk also defines data-link and physical levels for Ethernet (Ether Talk) and Token Ring (Token Talk). The data-link levels, including Local Talk, encapsulate or strip packets for a network level, which defines a Datagram Delivery Protocol (DDP). The data-link level supports node-to-node packet transmission and receipt. (It does not guarantee packet delivery but does deliver error-free packets.)

The Appletalk LLAP driver kit costs $5,000, including source code. There is no run-time licensing fee.—Ray Weiss
Zilog Inc, 210 E Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8066.

Help for the toughest part of the Appletalk communications protocol is available in a kit that includes source code and a Z80181 µC-based board.
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SEMINAR LOCATIONS

<table>
<thead>
<tr>
<th>Date</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 30</td>
<td>Orlando</td>
</tr>
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<td>April  8</td>
<td>Orange County</td>
</tr>
</tbody>
</table>

*Note: Seminar Schedule:
8:30 am-12:00 pm
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For example, the library of mega-function blocks contains cores of our µCOM87, V20H and V30H microprocessors, plus intelligent peripheral functions such as those provided by NEC’s 72-series and 82-series standard peripheral devices. And because most of these megafunction blocks are hard macros, derived directly from the chip layouts of our standard parts, they have fully characterized timing parameters and can be tested with the standard part test vectors.

Our hard macros are complemented by an extensive range of soft macros to provide additional peripheral device and system support functions, and by a library of over 300 standard logic functions available for both silicon realization approaches, the ‘High-density’ (CB-C7HD) and the ‘Fast TAT’-option (CB-C7FT). And of course, all our RAM and ROM blocks can be compiled to exactly match your system requirements.

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The high silicon utilization of the process allows us to achieve integration levels of over 180,000 usable 2-input NAND-gate equivalents per chip – more than sufficient to put high-performance systems into single-chip solutions. And although CB-C7 ASICs consume very little power – only 6.5 µW/gate/MHz – their 48-mA drive capability allows them to deliver power when it's needed.
Fast turnaround and low unit price are often conflicting requirements when it comes to implementing your ASIC designs – the first suggesting the use of a gate array solution, and the second dictating a standard cell approach. NEC's CB-C7 ASIC technology solves these cost/turnaround trade-offs – with combined gate-array-standard-cell solutions for fast turnaround, and full standard-cell implementations for low unit cost.

Whichever option you choose, the hard-macro, megafunction block and RAM/ROM blocks in your design will be floor-planned onto the chip in much the same way. If you need finished silicon in less than a month, we will then implement your customer specific logic in a 'sea of gates' gate array, laid down around these cells. Alternatively, if you are aiming for minimum piece price, we will implement the entire ASIC as a standard cell design – using sophisticated cell optimization algorithms to ensure we achieve minimum chip area.

High Performance ASICs and Packages

Both the fast turnaround and low unit cost versions of CB-C7 ASICs feature the same high performance - so there are no compromises with either solution.

To match this performance, we have an equally impressive range of packages in which to house them. You can choose between conventional plastic DIPs, quad flat-packs, PLCCs and high pin-count plastic or ceramic pin-grid arrays. NEC's state-of-the-art packaging technology provides CB-C7 ASICs with maximum protection from their environment, ensuring their long-term reliability.

Open CAD Design System - flexibility in design

NEC OpenCAD gives you maximum freedom in the CB-C7 design process. Freedom to perform schematic capture using popular EDA software such as DAZIX, Mentor, Valid and VIEWlogic, on industry standard workstations from DEC, HP-Apollo, IBM and SUN.

After schematic capture, your design is completed by compiling RAM/ROM blocks and optimizing user-defined logic. It is then floor-planned using ChipPlan, simulated with System Hilo or Verilog, and placed and routed using Cell-3 Ensemble. After post-layout simulation and design-rule checks, we pass pattern generation data to one of our wafer fabrication facilities in Japan, the USA or Europe.

To simplify your design task, logic optimization, simulation, and chip layout are normally carried out by a NEC ASIC design center on their SUN or DEC workstations. Providing access to NEC's Unified Design Environment - a suite of ASIC design tools which operate under DEC PowerFrame system management software - these workstations ensure a simple user interface and smooth data flow from one design process to the next.

However, OpenCAD also gives you the flexibility to install part or all of the NEC Unified Design Environment on your own system, so that you can perform as much, or as little, of the CB-C7 design process as you choose.
NEC Unified Design Environment - A Framework for Right-First-Time Designs

To handle the complexity of CB-C7 ASICs, and that of our next generation of ASIC technologies, we have taken some of the best ASIC design packages in the industry—such as VIEWlogic schematic capture software, Synopsys HDL compilers and logic synthesizers, Genrad System Hilo, and Cadence simulation, layout and routing software—and integrated them into the NEC Unified Design Environment.

At the heart of this design system lies the NEC Central Unified ASIC Database—a technology independent database which allows us to automatically generate new simulation models as new process technologies are introduced.

So with NEC, you not only get ahead, you stay ahead.

Open CAD Design System

Wherever you are in the world, there is a NEC design center close enough to support you in CB-C7 ASIC design. If you are already using industry standard workstations and EDA software to design ASICs, you probably have all the hardware and software design tools you will need. Simply install the CB-C7 ASIC libraries, and you can start on a CB-C7 design tomorrow. Interested...? Then phone your local NEC office today.

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UK Tel: 020-691333, Ireland Tel: 621-8420, Telex: 56847, Hong Kong Tel: 755-9018, Telex: 54558, Taiwan Tel: 02-716-2377, Telex: 223127
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It isn’t very edible, but it does make for very tasteful reading.
Design for test (without really trying)
You have every reason to ignore test in your projects. Schedules make little or no allowance for the extra time design for test requires; in fact, shrinking product-development cycles give you less time to finish more complex projects. In addition, although design specifications occasionally include test metrics, management judges you by your ability to meet your specifications' demands on function and cost. The bottom line is that schedule, function, and cost are the standards management use to grade your performance. Test? "Oh yeah, make sure the manufacturing guys can test your designs."

Designers often cite performance and area penalties as the most vexing problem of design-for-test strategies. Unfortunately, as with most generalizations, these may be untrue in specific cases. If you underutilize a gate array or design a pin-limited standard-cell circuit, then area shouldn't be an issue. And, although I/O requirements may prevent you from dedicating pins to testing, you may be able to multiplex test pins with functional ones. In fact, although the IEEE-1149.1 test port requires four dedicated pins, Toshiba, through its Vertex subsidiary, multiplexes signals to offer a test interface option where you dedicate only one pin to test. The test pin internally selects between functional I/O and a pseudo-IEEE-1149.1-compatible test port. (IEEE-1149 was formerly known as the JTAG—Joint Test Action Group—specification.) Toshiba can't call its port IEEE-1149.1-compatible because a true IEEE-1149.1 must have four dedicated test pins.

Performance-impact fears can be an even bigger paper tiger. Many designers claim that their design is too close to the edge of the ASIC vendor's process capabilities. However, these designers forget that not every path is critical. Adding testability to less worrisome paths may not make your design fully testable, but the design will be more testable than it might otherwise be. In addition, several ASIC vendors, Toshiba among them, of-
fer zero-delay scan latches, which don't rob time from your functional circuits.

Aside from designing smart, there are several ways your company can build testable circuits without specifically designing them that way. Over time, these testability enhancers will take as much control for design testability as you are willing to give them.

In addition to letting your company test your designs, many design-for-test (DFT) strategies offer a side benefit. If the test strategy lets you control internal voltage levels, then you can also use the test circuits to set internal states and conditions. By defining a particular initial condition, you can analyze behavior and facilitate prototype or device debug. Strategies that provide internal observation points simplify evaluating the capability.

Perhaps the simplest approach to designing for test is to pass the responsibility off to your ASIC vendor. Many vendors, among them Gould AMI and Fujitsu, provide transparent test as an internal service. You'll pay for the privilege, however; the vendors will add the cost of making your designs testable to your NRE. And the service isn't entirely transparent; you must recheck the vendor's simulation results to ensure the inserted testability doesn't impact your design's timing specifications.

In general, commercial testability tools fall into two broad categories. One group physically changes your design by adding logic, scan chains, or testability enhancers such as built-in logic-block observers (BILBOs) or test matrices. In contrast, the other type of tool accepts your design and creates test patterns to evaluate it.

Of those test schemes that modify your design, the Crosscheck approach is the most innovative and seems to least affect performance. The approach, available to ASIC designers only through Crosscheck licensees (Fujitsu, Harris, LSI Logic, NEC, Oki Electric, Raytheon, and Sony), provides observability at most every node in your design by adding minimum-sized p-channel transistors.

Using Crosscheck's approach, you design your circuits using library cells that appear and function as conventional cells; the ASIC vendor has already incorporated the additional p-channel transistors into the cells. According to Nitin Deo, applications engineering manager at Fujitsu, and Cliff Vaughan, strategic marketing manager at Oki, the parasitic capacitance of these transistors might add 2 to 3% to propagation times—though long p-channel transistor stacks, such as those in a 4-input NAND gate, may suffer a delay penalty of 6%. In contrast, both John Defalco, manager of programs, design support, and business development of Raytheon's Microelectronics Center, and Farzad Zarrinfar, product marketing manager at LSI Logic, say that their companies' implementations are nominally faster. Their approaches beef up the p-channel devices to compensate for the additional capacitance, and these larger transistors provide faster switching.

The embedded-matrix approach requires adherence to several minor design rules: the design can't rely on stored charge, and internal freerunning oscillators must allow initialization to a known state.

Where the approach exacts a bigger price is in its 4-pin test bus. The bus, compatible with IEEE-1149.1, provides a means for serially shifting the node data off the chip for comparison with "good" data. The 4-pin test bus and the additional observability transistors combine to claim an area penalty.
Don't test my circuits

Many engineers still misunderstand the purpose of design for test, according to Scott Creekbaum, senior engineer at AT&T's Santa Clara Design Center. Too often, Creekbaum sees designers who get defensive when they are asked to design for test. These designers know that their circuits are good.

No ad-hoc or structured test approach tests or guarantees your design's function. You or your design team are the only ones who can attest to the goodness of your design. You reach this conclusion via extensive simulation, breadboarding, and functional testing of the design.

In contrast, design for test starts with a fundamental assumption: The design is good. Design for test then seeks to qualify the manufacturing of the design. In fact, a more appropriate name might be designing to test manufacturing.

Since testing a device requires control and observation of internal logic states, design for test aims to provide this access. Using this access, the test seeks to answer such questions as: Are any of the nodes stuck high or low? Does the particular device under test have any opens or shorts? Do signals take too much time to make the transition between voltages? Does the design sink and source reasonable amounts of current? Finally, does the device initialize properly and consistently?

What does it cost?

This area penalty may not translate into significantly higher dollar costs. Although several of the licensees will charge a premium for designs that use this test approach, this premium may be deceptive. You can offset the higher charges with savings in test-program development and debug time for circuits without DFT or the additional time to manually design in test.

Currently, the Crosscheck approach offers only massive observation of internal nodes. Toward the middle of this year, the company will introduce a capability to provide control of flip-flops as well.

A more common design-modification approach is scan substitution. This approach changes your design by replacing all or most of your non-scan flip-flops with scannable ones. In effect, the scan philosophy converts a sequential logic design into a multitude of combinational ones. In these scan designs, each combinational circuit contains paths of combinational logic terminated by one storage element. Scan then builds a mechanism to shift data serially to and from each of the storage elements so each storage element acts as a primary input or output to its combinational circuit.

Many of the transparent test-synthesis tools offer this scan-insertion capability. Among the tools are Intergraph's Testsyn, Philips' Locam, Racal-Redac's Silcsyn Test Synthesis, Sunrise's Testgen, Synopsys' Test Compiler, and Teradyne's Frenchip Synthesis. The tools offered from Intergraph, Philips, and Teradyne were developed for internal use (AT&T developed Scan Test and Dassault Electronique developed Frenchip Synthesis) and are being marketed externally to help defray costs.

Two features help distinguish among these scan-test tools. First, designers looking for push-button test insertion will have to push sev-
eral buttons. For example, you insert scan using Test Compiler after synthesizing your logic, but before you optimize the design. Test Compiler does generate test patterns, though, so you needn’t run a separate pattern generator. Testsyn inserts the scan chains and generates patterns after synthesis and optimization. In contrast, Locam and Silcsyn Test Synthesis insert the test logic into the design during synthesis, but neither generate patterns; optional tools from the vendors perform that function.

A third alternative is Testgen, which like Testsyn, is a test-insertion tool rather than a test-synthesis tool. Testgen accepts a “test budget,” consisting of acceptable performance and area penalties. Using these design constraints, the software swaps some flip-flops for scan-flips and generates patterns to test the circuit. The tool performs no logic optimization.

Table 1—Test-logic insertion tools

<table>
<thead>
<tr>
<th>Company</th>
<th>Product</th>
<th>Function- and test-logic optimization</th>
<th>IEEE-1149.1-controller/multiple internal scan chains/multiple clocks</th>
<th>Input/output formats</th>
<th>Inserts BIST/ multiplexed isolation</th>
<th>Cost (availability)</th>
<th>Transparency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compass Design Automation</td>
<td>Test Assistant</td>
<td>Yes</td>
<td>Yes/yes/yes</td>
<td>Schematics, EDIF, VHDL, Verilog</td>
<td>Yes/yes</td>
<td>$60,000 (now)</td>
<td>Separate operation. Tool generates patterns.</td>
</tr>
<tr>
<td>Dazix</td>
<td>Testsyn</td>
<td>No</td>
<td>No/yes/yes</td>
<td>VHDL, Verilog, C, EDIF, Dazix, Netlist/VHDL, EDIF</td>
<td>No/no</td>
<td>$25,000 (2Q '92)</td>
<td>Separate operation.</td>
</tr>
<tr>
<td>Pyramid</td>
<td></td>
<td>No</td>
<td>No/yes/yes</td>
<td>VHDL, Verilog, EDIF, TDL</td>
<td>Yes/yes/no</td>
<td>$25,000 (2Q '92)</td>
<td>Separate operation.</td>
</tr>
<tr>
<td>GEC-Plessey Semiconductor</td>
<td>Gatemap</td>
<td>Yes</td>
<td>Yes/no/no</td>
<td>EDIF or truth table/EDIF</td>
<td>No/no</td>
<td>$25,000 (now)</td>
<td>Inserts scan chain during synthesis of function logic. Separate tool adds BIST.</td>
</tr>
<tr>
<td>LSI Logic</td>
<td>Test Builder</td>
<td>No</td>
<td>Yes/yes/yes</td>
<td>VHDL, EDIF, NDL</td>
<td>Yes/no</td>
<td>$80,000 (now)</td>
<td>Separate operation. Tool tests megafunctions using multiplexed isolation with your guidance.</td>
</tr>
<tr>
<td>Philips Electronic Design and Tools</td>
<td>Locam</td>
<td>Yes</td>
<td>Yes/yes/yes</td>
<td>EDIF, VHDL, Elle/EDIF, VHDL, Mentor schematic</td>
<td>No/no</td>
<td>$30,000 (now)</td>
<td>Inserts scan chain during synthesis of function logic.</td>
</tr>
<tr>
<td>Racal-Redac</td>
<td>Silcsyn’s Test Synthesis</td>
<td>Yes</td>
<td>Yes/yes/yes</td>
<td>VHDL, Silcsyn, EDIF, Cadat, Visual/VHDL, Cadat, EDIF, NDL</td>
<td>Yes/no</td>
<td>$54,000 (March '92)</td>
<td>Test logic is synthesized with function logic.</td>
</tr>
<tr>
<td>Sunrise Test Systems</td>
<td>Testgen</td>
<td>No</td>
<td>No/yes/yes</td>
<td>TDL or NDL, Netlist, Verilog/TDL or NDL</td>
<td>No/no</td>
<td>$95,000 (now)</td>
<td>Separate operation. Tool accepts user-guided “test budget.” Generates test vectors.</td>
</tr>
<tr>
<td>Synopsys</td>
<td>Test Compiler</td>
<td>Yes</td>
<td>Yes/yes/yes</td>
<td>Verilog, VHDL, Netlist, schematic, Boolean equations</td>
<td>No/no</td>
<td>$40,000 (now)</td>
<td>Separate operation. Generates test vectors.</td>
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<tr>
<td>Teradyne EDA</td>
<td>Frenchic Synthesis</td>
<td>Yes</td>
<td>Yes/yes/yes</td>
<td>VHDL, espresso/ VHDL, and netlists in several formats</td>
<td>Yes/no</td>
<td>$75,000 (now)</td>
<td>Test logic is synthesized with function logic.</td>
</tr>
</tbody>
</table>

Notes: 1. EDIF=Electronic Design Interchange Format, VHDL=VHSIC Hardware Description Language, NDL and TDL=proprietary description languages.
2. BIST=built-in self test.
Methods require integration of all storage elements into the scan chain. The other distinguishing feature of some of the test insertion tools is their ability to build partial scan into designs. Testgen, Silcsyn Test Synthesis, and Frenchip Synthesis all allow partial scan. In fact, each of these tools will choose which storage elements to include in the scan chain based on the software's assessment of efficacy. The pattern-generator partner of these tools will recognize and create high-coverage patterns.

Although Testsyn, Test Compiler, and Locam are full-scan-based tools, they don’t force you to trade all storage elements for scannable ones. You can protect portions of your circuit from these tools to ensure timing, area, or logic isn’t changed. The downside of protecting sections of your circuit from full-scan-based tools is that the pattern generators can’t assure testability.

Beyond full- and partial-scan-based tools, several tools can create modules that self-test function blocks. Function blocks that particularly lend themselves to built-in self-test (BIST) contain highly regular structures and include memories and data paths. LSI Logic’s Test Builder includes a module that generates BLBOS for memories. The BLBOS are the logic that perform and grade BISTs. Modules within Compass’s Design Assistant let you generate BLBOS for memories, data paths, multipliers, and circuits of your own design. Frenchip Synthesis also offers BLBO generation for your circuits.

One other design-modification method for test insertion is multiplexed isolation. As the name implies, you can design for test, if you want. Some designers do design for test. If you want to design for test, beyond the tools discussed in the article, you have several ways to do it. Your choices range from manually inserting control and observation points into the design to using test-analysis tools.

Test-analysis tools can be bundled with the test-insertion or pattern-generation tools or they can be offered independently. Among the bundled tools are an analyzer that comes with Teradyne’s Aida pattern generator. This tool examines your design against 24 internal rules to let you know whether pattern generation will be successful. Similarly, the AT&T scan-insertion tools, which Dazix, an Intergraph Co, incorporates into its own tool set, performs a design audit looking for testability design-rule violation.

Going a step beyond the rule-checking capability, several tools actually analyze your design. Since Racal-Redac’s Silcsyn Test Synthesis, Sunrise’s Testgen, and Teradyne’s Frenchip let you constrain the “scannability” of your design, they include analysis capabilities that try to select the most efficient storage elements to include in the scan chains.

Both Dazix and Teradyne also offer independent tools to assist you in choosing test schemes or in selecting control or observation nodes. Dazix’s $5000 Pioneer tool is a rule checker that assures your design is suitable for the company’s pattern-generation tools. Although Teradyne’s $50,000 Lasar is primarily a board-design or system-design tool, you can use it to design your ASICs. The software contains two utilities that rank internal nodes based on their control and observation efficacy. When you select a node to make a primary input or output, the software regenerates the list to account for dependencies.
DESIGN FOR TEST

plies, this technique uses multiplexers to provide access to functional blocks or mega-cells embedded in your design. Via this access, you can independently test these blocks without the effect and influence of peripheral circuits. Only Test Builder and Test Assistant offer this capability.

If you are reluctant to let anyone or anything modify your design, or if you want to generate test patterns for a circuit after running any of the test-logic insertion tools, you have several choices. One general note about using commercial pattern generators though: Talk to your ASIC vendor before you make a big financial commitment. Automatically generated test patterns are much like simulation results—ASIC vendors insist on qualifying the models and tools you use to generate them.

Developing test patterns to test strictly combinatorial circuits is relatively easy. So, by extension, is developing test patterns to test full-scan-based circuits. Developing patterns to test circuits with sequential logic is far more complex because the software must move data through storage elements to...

The top-10 reasons you don't design for test

At a panel session on the acceptance barriers confronting design for test and built-in self test (BIST), Richard Sedmak, president of Self-Test Services ((215) 628-9700), presented a list of reasons designers don't design for testability. With apologies to David Letterman, we have adapted that list here.

10) There is no push-button answer to designing for testability. And everyone knows how much engineers like to push buttons.

9) Test requirements are usually poorly defined. Failure of the marketing people to put a specification for testability into the statement of work makes it easy for you to meet it.

8) Little or no communication occurs between the design, manufacturing, and service organizations. When you don't know the sort of problems that arise after your designs reach the production floor and ultimately, the customer, you can't improve subsequent iterations.

7) Companies don't do a good job of tracking manufacturing defects and field failures. You aren't the only one who doesn't know what happens once designs leave your hands.

6) Your company has no life-cycle cost-of-test model. Because the company has never tracked the impact of failure to test over the life of a product, the company can't make informed tradeoffs about the up-front cost of designing for test versus the back-end cost of ignoring it.

5) The testing crisis within your organization hasn't reached a critical level. Your company hasn't yet had to recall a high-impact product and placate angry customers because of a design or component problem that test failed to catch.

4) Management has no real commitment to test. Oh sure, everybody says that test is important. But how do they spend their money? Has your company developed life-cycle cost-of-test models? Does the testability of your projects influence your raises and promotions?

3) Schedules and budgets make no allowance for increased testability. Because there are no real transparent methods, making a design testable takes time and costs money.

2) Adding testability steals precious nanoseconds from performance and demands high real-estate penalties. This is probably the most common excuse to avoid testability and the most specious. Most designers who do design for test say performance and area impacts aren't design killers. All paths are not critical. You can provide control to and observation of nodes near, but not on, the critical path. Real-estate costs are a function of your chosen testability scheme, the complexity of your design, and the technology you choose for building it. If you're using 50% of a large gate array, for example, adding scan-based testability will lower yield and will appear to cost you pennies. Ultimately, though, you'll save money through reduced failures in test or in the field. In contrast, if you've decided to implement a register-oriented design in a small, highly utilized gate array, adding scan could force you into a larger array and cost substantially more.

1) You are rarely rewarded if you do design for test and seldom penalized if you don't. If adding testability forces you to slip your schedule, are you praised for adding test or punished for slipping the schedule? Do your gate budgets include an allowance for test? If adding test forces your design into a larger gate array, would your company add the test logic, remove some of the design's function, or keep all the function and shoehorn a little bit of test logic into the smaller array?

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reach primary inputs and outputs. (Ref 1 is a very good, detailed explanation of the theoretical underpinnings of test-pattern generation.) The maximum distance, measured in number of storage elements, between any storage element and a primary input or output is the circuit’s sequential depth. Although you may exclude storage elements from a scan chain, full-scan-based pattern generators can

Manufacturers of transparent-test design tools

For more information on transparent-test design tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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only generate high-coverage patterns for circuits whose sequential depth is 0.

Some tools want to be alone

Several pattern-generation tools work with logic-synthesis tools. In fact, test-synthesis tools Testsyn and Test Compiler, both full-scan tools, include pattern generators as integral parts of their capabilities. Several other pattern generators don't assume or require any synthesis.

In addition to Testgen, which can swap storage elements for scanable ones based on a user-defined budget before creating patterns to test the design, Racal-Redac's Intelligen automatic test-pattern generator (ATPG) is coupled with the company's function-and test-logic synthesis tool. As a result, you can feed data between the tools to trade off area, speed, and testability. You can also use the tools independently of logic synthesis to create patterns.

Other pattern-generation tools, such as Expertest's Test Design Expert, Adas's Test Pattern Generator (TPG), and Teradyne EDA's Aida ATPG Toolkit operate independently of synthesis tools. Like pattern generators that work with synthesis tools, these tools may require you to adhere to a particular design style. For example, the Aida ATPG Toolkiet does not generate patterns for sequential designs. In contrast, both Adas's TPG and the Test Design Expert will generate patterns for designs ranging from fully synchronous to asynchronous.

While the ASIC vendors must qualify automatic pattern generators for mask-programmed devices, you have greater flexibility in using pattern generators for user-programmed devices, such as PLDs, PLAs, and FPGAs (field-programmiable gate arrays). Generally, as long as you can accurately model and present the actual implementation of your design to the pattern generators, you can use any automatic pattern generator to create test patterns for these devices. You also have a lower-cost alternative. Acugen's test pattern generator, the least expensive software listed in Table 2, is specially written for user-programmable devices.

You can use many of the available tools to build testable circuits without designing for testability. On the other hand, as good engineers, you should know that truly transparent test is really an illusion. No tool operates in a vacuum. You can't trust any of the tools to do your job for you.

<table>
<thead>
<tr>
<th>Company</th>
<th>Product</th>
<th>Direct or control synthesis</th>
<th>Supported design methods</th>
<th>Generate sequential-scan patterns</th>
<th>Cost (availability)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acugen Software</td>
<td>Acugen</td>
<td>No</td>
<td>PLAs, PLDs, FPGAs</td>
<td>No</td>
<td>$2000 (now)</td>
</tr>
<tr>
<td>Adas Software</td>
<td>Adas TPG</td>
<td>Via optional scan-flop substitution</td>
<td>All</td>
<td>Yes</td>
<td>$100,000 (early '92)</td>
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<tr>
<td>AT&amp;T</td>
<td>Gentest</td>
<td>No</td>
<td>All</td>
<td>Yes</td>
<td>$150,000 (May '92)</td>
</tr>
<tr>
<td>Compass Design Automation</td>
<td>Scan Test ATVG and Star</td>
<td>No</td>
<td>LSSD 2 and multiplexed flip-flop for scan</td>
<td>No</td>
<td>$40,000 (second quarter)</td>
</tr>
<tr>
<td>Dazix</td>
<td>Picasso</td>
<td>No</td>
<td>All</td>
<td>Yes</td>
<td>$120,000 (second quarter)</td>
</tr>
<tr>
<td>Expertest</td>
<td>Test Design Expert</td>
<td>No</td>
<td>All</td>
<td>Yes</td>
<td>$140,000 (now)</td>
</tr>
<tr>
<td>LSI Logic</td>
<td>SATPG</td>
<td>No</td>
<td>Synchronous design</td>
<td>Yes</td>
<td>$100,000 (now)</td>
</tr>
<tr>
<td>Philips Electronic Design and Tools</td>
<td>Panther CubiSprint</td>
<td>No</td>
<td>Scan and LSSD</td>
<td>No</td>
<td>$30,000 (now)</td>
</tr>
<tr>
<td>Racal-Redac</td>
<td>Intelligen</td>
<td>Yes</td>
<td>All</td>
<td>Yes</td>
<td>$127,000 (now)</td>
</tr>
<tr>
<td>Sunrise Test Systems</td>
<td>Testgen</td>
<td>Yes</td>
<td>Works with most scan techniques</td>
<td>Yes</td>
<td>Included with test-logic insertion tool</td>
</tr>
<tr>
<td>Synopsys</td>
<td>Test Compiler</td>
<td>No</td>
<td>Supports several scan methods</td>
<td>No</td>
<td>Included with test-logic insertion tool</td>
</tr>
<tr>
<td>Teradyne EDA</td>
<td>Aida ATPG Toolkit</td>
<td>No</td>
<td>Scan</td>
<td>Yes</td>
<td>$90,000 (now)</td>
</tr>
</tbody>
</table>

Notes: 1. FPGA=field programmable gate array.
2. LSSD=level-sensitive-scan design.
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References

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Op-amp distortion measurement bypasses test-equipment limits

Jerald Graeme, Burr-Brown Corp

Part 1 of this 2-part series introduces the theory involved in measuring the low distortion levels of state-of-the-art op amps. It also provides simple methods for characterizing some low-distortion op amps.

Until recently, distortion performance was not important in most op-amp applications. Now, common use of the fast Fourier transform (FFT) extends the importance of op amps' distortion beyond audio applications into general signal processing. Any distortion introduced by an amplifier produces erroneous Fourier components. To predict these error components, you must first characterize your op amp's distortion. But op amps' distortion performance often surpasses that of available test equipment, defying characterization. Making the amplifier-under-test part of the test system solves this characterization problem. This solution works exclusively with feedback amplifiers, op amps included.

Feedback reduces an amplifier's distortion—at its output—to minuscule levels. Feedback also separates the amplifier's distortion from the test signal. This separated distortion is none other than the error signal fed back to the op amp's inputs. Once separated, the amplifier-distortion signal is insensitive to any distortion in the incoming test signal. Also, the separated signal has a reduced magnitude that reduces the dynamic range your test equipment has to handle.

Three distortion-measurement methods capitalize on the signal-separating action of op-amp feedback. In the first method, you measure the separated signal directly. This method circumvents test-equipment limitations. In the second method, selectively amplifying the amplifier's distortion raises this error signal above the threshold of the test equipment. Finally, the third method removes the test signal yet avoids measuring any effects of the added amplifier. This method bootstraps the op amp's power supplies on the test signal itself to remove the test signal from the measurement. Part 1 of this series covers direct measurement and selective amplification; Part 2 covers selective amplification and bootstrapping.

Each approach greatly improves distortion resolution but also has specific constraints. Signal separation adds an amplifier to the test system; selective amplification reduces the measurement bandwidth; and bootstrapping requires using a signal to drive the reference point of the op amp's power supplies.

![Feedback separates an op amp's distortion products from the test signal by developing a signal \( V_{err} \) equal to the difference between input and output signals.](image-url)
MEASURING OP-AMP DISTORTION

Noise seldom limits op-amp-distortion measurement. Only in very low-distortion op amps does noise impose a limit on distortion analyzers. Amplifier noise is almost never a problem for spectrum analyzers because they are highly insensitive to noise.

Translate to ground

First consider how feedback separates the amplifier-distortion products from the test signal. This consideration is fundamental to each of the measurement circuits that follow. You can visualize the signal separation most easily with a voltage follower (Fig 1). In Fig 1, input signal \( V_{IN} \) drives the op amp’s input to produce output signal \( V_{OUT} \), and a simple loop equation shows that

\[
V_{OUT} = V_{IN} - V_{ERR},
\]

where \( V_{ERR} \) is the differential-input error signal of the op amp.

As trivial as this equation seems, it holds the answer to measuring op-amp distortion with high resolution. The equation states that the output signal, \( V_{OUT} \), is a replica of the input signal, \( V_{IN} \), except \( V_{OUT} \) does not include the input error signal \( V_{ERR} \). Thus, any distortion the amplifier introduces is in \( V_{ERR} \).

Measuring \( V_{ERR} \) instead of \( V_{OUT} \) removes any effects of signal-generator distortion and reduces the dynamic range required of your test equipment. The op amp’s open-loop gain and common-mode rejection attenuate whatever test signal remains in \( V_{ERR} \).

Distortion measurement with Fig 1’s setup requires additional processing of the signal \( V_{ERR} \). Signal \( V_{ERR} \) rides on the input signal \( V_{IN} \). Consequently, any ground-referenced measurement of \( V_{ERR} \) still includes the test signal \( V_{IN} \).

The instrumentation amplifier in Fig 2 references \( V_{ERR} \) to ground and increases the signal level presented to the analyzer. Finding a low-distortion instrumentation amplifier is easier than producing a better signal generator and a better signal analyzer. This instrumentation-amplifier alternative serves the measurement of intermediate levels of distortion in feedback amplifiers.

After measuring distortion using the setup in Fig 2, you must adjust your results. These adjustments transform the distortion percentage measured in \( V_{ERR} \), \( THD + N_M \), to the equivalent percentage present in \( V_{OUT} \), \( THD + N_0 \). (THD + \( N_M \) is the measured valve and THD + \( N_0 \) is the corresponding output distortion and noise.)

\[
THD + N_0 = (V_{ERR}/V_{OUT})THD + N_M.
\]

When using a spectrum analyzer, adjusting the THD result as you calculate it is the easiest way to go. Taking this tack necessitates two changes. THD expresses distortion as the ratio of the rms sum of the distortion products to the signal fundamental:

\[
THD = \sqrt{V_1^2 + V_2^2 + V_3^2 + \ldots} \times (100\%) / V_1.
\]

Here, \( V_1 \) represents the fundamental component of the signal, and \( V_2, V_3, V_4 \) and so forth represent the distortion components. For the measurement shown in Fig 2, the magnitude of \( V_{OUT} \) substitutes for the fundamental \( V_1 \) to correct for the smaller fundamental signal present in \( V_{ERR} \). Also, the harmonic amplitudes measured require adjusting to account for the gain they receive from the instrumentation amplifier. For this adjustment, divide the overall THD equation by the instrumentation amplifier’s differential gain, \( A_{DIFF} \).

\[
THD_{OUT} = \sqrt{(V_2^2 + V_3^2 + V_4^2 + \ldots)} \times 100\%/A_{DIFF} V_{OUT}.
\]

For the unity-gain amplifier under test, subtraction obviously separates the op amp’s distortion from the test signal. However, this condition is a coincidence unique to the voltage follower. In other op-amp configurations, the signal translation of \( V_{ERR} \) does not subtract the op amp’s output from the input signal.

Fig 3 shows the generalized, noninverting, feedback configuration along with the equations relating \( V_{ERR} \) to \( V_{OUT} \). Here, a feedback network attenuates the effect of \( V_{OUT} \) on \( V_{ERR} \). Thus, the amplifier-distortion products reflected in \( V_{ERR} \) are smaller than those in \( V_{OUT} \).
As before, you must separate the \( V_{\text{ERR}} \) signal from the common-mode test signal in Fig 3’s circuit. The first method for this separation is translation to a ground-referenced signal (Fig 4). Distortion measurement with this configuration is easiest to see by considering the circuit to be an extension of Fig 2’s voltage follower. In Fig 4, the voltage-divider action of the feedback network presents a signal \( V_{\text{OUT}} R_1/(R_1 + R_2) \) to the amplifier’s inverting input. For the voltage follower, this signal was the full \( V_{\text{OUT}} \). Now, the feedback signal is attenuated, and a simple loop equation shows that for Fig 4,

\[
V_{\text{ERR}} = V_{\text{IN}} - \left( \frac{V_{\text{OUT}} R_1}{R_1 + R_2} \right).
\]

Fig 4’s circuit amplifies \( V_{\text{IN}} \) and its distortion in producing \( V_{\text{OUT}} \). Thus, subtracting \( V_{\text{OUT}} \) from \( V_{\text{IN}} \), as with Fig 2, would not remove the generator’s distortion for Fig 4. However, subtracting an appropriately attenuated \( V_{\text{OUT}} \) from \( V_{\text{IN}} \) does remove this distortion. Fig 4 has a gain of \((R_1 + R_2)/R_1\). Then, feedback attenuates \( V_{\text{OUT}} \) by the inverse of this gain or \( R_1/(R_1 + R_2) \).

For a distortion-analyzer measurement like that shown in Fig 4, first compensate the result for the smaller fundamental measured through \( V_{\text{ERR}} \). Multiply the measured \( \text{THD} + N_M \) result by \( V_{\text{ERR}}/V_{\text{OUT}} \) as before. This calculation yields the input \( \text{THD} + N_{IN} \) result, which you then multiply by the \( 1/\beta = (R_1 + R_2)/R_1 \) of the op amp’s configuration.

\[
\text{THD} + N_{IN} = \frac{V_{\text{ERR}} (R_1 + R_2)}{V_{\text{OUT}} R_1} \cdot \text{THD} + N_M
\]

\[
= \frac{R_1 + R_2}{R_1} \cdot \text{THD} + N_{IN}.
\]

You must also adjust your results for spectrum-analyzer measurements using Fig 4’s setup. Once again, you discard the measured fundamental because it does not represent the output signal. Then, substitute \( V_{\text{OUT}} \) for fundamental amplitude \( V_{\text{IN}} \) in the THD equation and divide this equation by \( A_{\text{DIFF}} \) to remove the effect of the instrumentation amplifier’s gain. For Fig 4, also make a gain adjustment for the circuit’s gain of \( 1/\beta = (R_1 + R_2)/R_1 \).

\[
\text{THD}_{\text{OUT}} = \frac{(R_1 + R_2) \sqrt{(V_{\text{IN}}^2 + V_{\text{IN}}^2 + V_{\text{IN}}^2 + \ldots)}}{V_{\text{OUT}} A_{\text{DIFF}} V_{\text{OUT}}} \times 100\%.
\]

Signal separation extends to inverting case

For the generalized inverting amplifier, distortion resolution is even greater (Fig 5) than for the noninverting amplifier. The most significant improvement with inverting circuits actually results from removing the instrumentation amplifier of Fig 4. The inverting configuration of Fig 5 removes common-mode voltage from the op amp’s input and avoids the added amplifier along with the added amplifier’s distortion.

For the inverting circuit in Fig 5, the relationship between input and output distortion is not as obvious as with Fig 4’s circuit. Previously, the feedback network relayed a large signal to the amplifier’s input. But inverting circuits keep this input near zero voltage, balancing \( V_{\text{IN}} \) and \( V_{\text{OUT}} \) at the amplifier’s input. Both signals influence the voltage at the inverting input through the feedback network. To find the result, consider the two signals separately using superposition. This exercises the feedback network as a voltage divider driven from each end. Then, the amplifier input signal is

\[
V_{\text{ERR}} = \frac{V_{\text{IN}} R_2}{R_1 + R_2} V_{\text{OUT}} R_1.
\]
MEASURING OP-AMP DISTORTION

Fig 5—Inverting circuits also separate distortion and test signals. And these circuits obviate the previous measurement amplifier along with its distortion.

Although not immediately obvious, the distortion introduced by \( V_{\text{IN}} \) still cancels in this \( V_{\text{ERR}} \) signal. The above equation shows that signal \( V_{\text{IN}} \) influences \( V_{\text{ERR}} \) directly in the first term of the equation and then indirectly through feedback in the second term.

In the direct path, \( V_{\text{IN}} \) contributes to \( V_{\text{ERR}} \) through an attenuation of \( -R_2/(R_1+R_2) \). Added to this contribution is the \( V_{\text{IN}} \) component transmitted through \( V_{\text{OUT}} \). In this path, \( V_{\text{IN}} \) and its distortion products first receive a forward gain of \( -R_2/R_1 \) to produce \( V_{\text{OUT}} \). Feedback then attenuates \( V_{\text{OUT}} \) by a factor of \( -R_2/(R_1+R_2) \).

The total gain of this path is the product of the forward gain and the feedback attenuation, or \( R_2/(R_1+R_2) \). This product has the same magnitude as the attenuation of the direct path above, but these two gains have opposite polarities. Thus, the direct and feedback distortion effects of \( V_{\text{IN}} \) again cancel in the \( V_{\text{ERR}} \) signal.

Fig 5's measured results require two adjustments to account for the THD_OUT of the amplifier’s configuration. These adjustments follow directly from the Fig 4 results and use the same equations. One adjustment accounts for the smaller fundamental actually measured and the other corrects for the 1/\( f_0 \) gain that the harmonics included in the measurement don't receive. For distortion-analyzer measurements using Fig 5’s setup,

\[
\text{THD} + N_0 = \frac{V_{\text{ERR}}(R_1+R_2)}{V_{\text{OUT}} R_1} \text{THD} + N_{\text{M}}
\]

\[
= \frac{(R_1+R_2)}{R_1} \text{THD} + N_{\text{IN}}.
\]

And for spectrum-analyzer results,

\[
\text{THD}_0 = \frac{(R_1+R_2)\sqrt{V_1^2 + V_2^2 + V_3^2 + \ldots}}{R_1 V_{\text{OUT}}} \quad (100\%).
\]

With no common-mode voltage, the inverting connection of Fig 5 provides no information about CMRR-related distortion. This result is desirable for applications having no common-mode signal, and the result proves useful even where such a signal is present. The absence of CMRR distortion in Fig 5 permits separating the gain- and CMRR-distortion effects.

First, a distortion measurement with the inverting circuit of Fig 5 yields the gain-related distortion, \( \text{THD}_A \). Then, distortion measurement with the noninverting connection of Fig 4 provides the combined gain and common-mode distortion \( \text{THD}_{\text{ACM}} \). Subtraction of the two THD results, in rms fashion, reveals the common-mode distortion (\( \text{THD}_{\text{CM}} \)). In equation form, this distortion is

\[
\text{THD}_{\text{CM}} = \sqrt{\left(\text{THD}_{\text{ACM}}\right)^2 - \left(\text{THD}_A\right)^2}.
\]

The signal analyzer’s loading at the op amp’s summing junction also influences the measurement in Fig 5. Connecting the analyzer’s input capacitance to this junction can affect both measurement bandwidth and frequency stability. Capacitance at the input of an op amp produces response peaking.

This capacitance reduces measurement bandwidth to no more than \( f_0 = \sqrt{f_c/(2\pi R C_1)} \). Here, \( f_0 \) is the peak frequency, \( f_c \) is the unity-gain crossover of the op amp, and \( C_1 \) is the capacitance at the op amp’s input. A bypass capacitor around \( R_2 \) counteracts the response peaking. For 45° phase margin, the value of this capacitor is \( 1/\sqrt{2\pi R f_c/C_1} \).

References


Author’s biography

Jerald G Graeme is the manager of instrumentation-components design for Burr-Brown Corp in Tucson, AZ. Jerry directs a linear-IC-development group. He obtained a BSEE from the University of Arizona and an MSEE from Stanford University. His spare time interests include photography, scuba diving, and woodworking.

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Advanced techniques tackle advanced op amps' extremely low distortion

Jerald Graeme, Burr-Brown Corp

The second part of this 2-part series describes how to measure the distortion of more complex amplifier circuits and how to handle the highest-performance op amps.

Selective amplification offers an alternative to the added amplifier described in Part 1 of this series. This alternative moderates, rather than negates, the limitations of signal generators and signal analyzers. In addition to separating distortion and test signals, selective amplification makes the amplifier distortion signal dominant in the measurement; however, it also reduces measurement bandwidth.

As with signal separation, the selective-amplification approach is easiest to understand starting with a voltage-follower connection. Fig 1 shows a bootstrapped feedback network added to a voltage follower. In Fig 1, the common-mode rejection of the amplifier-under-test replaces the instrumentation amplifier used before. However, taking this tack moves the measurement back to the amplifier's output.

Resistors $R_1$ and $R_2$ form a feedback network that produces gain for $V_{ERR}$ but not for $V_{IN}$. Signal $V_{ERR}$, which includes the amplifier's distortion products, appears across resistor $R_1$. There, this signal produces a feedback current that goes to resistor $R_2$. This operation develops an error-signal gain, $A_{ERR} = 1 + R_2/R_1$, for $V_{ERR}$ alone.

Input signal $V_{IN}$ does not experience this amplification because $R_1$ is bootstrapped rather than grounded. The resulting output signal for Fig 1 is

$$V_{OUT} = V_{IN} - ((R_1 + R_2)/R_1) V_{ERR}.$$
MEASURING OP-AMP DISTORTION

significance diminishes in proportion to the gain V_{ERR} receives. Similarly, this gain moderates the dynamic range demands on the signal analyzer. Thus, selective amplification raises the amplifier-distortion signal above the measurement floor of your instruments.

Following the measurement, a THD calculation removes the effect of the selective gain. Divide the measured distortion by the distortion gain of \( (R_1 + R_2)/R_1 \). For Fig 1 the output-referred distortion for a voltage follower is:

\[
\text{THD} + N_0 = \frac{R_1}{(R_1 + R_2)} \text{THD} + N_{IN} = \text{THD} + N_{IN} \\
\text{OR} \\
\text{THD}_{OUT} = \frac{R_1 V}{(R_1 + R_2)} V_{IN}^2 + V_{IN}^4 + \ldots.
\]

At first blush, you'd think that maximizing the selective gain would achieve the greatest measurement accuracy. However, measurement bandwidth declines because of feedback-factor reduction as this gain increases (Ref 1). Because the op amp is now part of the measurement system, the amplifier’s bandwidth limits resolution of higher-order distortion harmonics. Thus, you should choose the selective gain for Fig 1’s setup to be as large as possible within your bandwidth constraints. Note that the low-value feedback resistors avoid adding noise.

Generalizing selective gain

The selective-gain approach of Fig 1 extends to generalized noninverting and inverting op-amp configurations. The generalized noninverting version in Fig 2 has R_3’s added gain for selectively amplifying distortion products. Resistors R_1 and R_2 set the normal closed-loop gain presented to V_{IN}. As usual, this gain is simply \( A_{CL} = 1 + (R_2/R_1) \). V_{ERR} experiences greater gain because it develops a feedback current through R_3, as well as through R_1. The resulting error-signal gain relates the parallel combination of resistors R_1 and R_2 and is \( A_{ERR} = 1 + R_3/(R_1 || R_2) \). The proper choice for R_3 makes V_{ERR}’s distortion dominant at the amplifier’s output.

The distortion measurement’s resolution remains unchanged between Fig 1 and Fig 2. These circuits differ by the closed-loop gain, A_{CL}, supplied to V_{IN} and its distortion, but practical limits equalize the results. As A_{CL} increases, the magnitude of V_{IN} diminishes to maintain a given output-signal level. Thus, the magnitude of the input-signal distortion decreases by the same amount that its gain increases. The resulting output distortion arising from V_{IN} is, then, unchanged in magnitude from that of Fig 1. Adding R_3 keeps this distortion in the background by ensuring sufficient additional gain for the distortion products of V_{ERR}.

Dynamic-range constraints of the signal analyzer are also independent of A_{CL} in Fig 2. The relative levels of the fundamental signal and the distortion signals determine this range. For a given test condition, the output level is fixed and is essentially the level of the fundamental signal. To reduce dynamic-range requirements, raise the level of the distortion signal by amplifying V_{ERR}. This amplification results from either the intended closed-loop gain of the circuit or from this gain in conjunction with the selective gain R_3 provides. However the gain occurs, it raises the relative proportion of V_{ERR} in the output signal. As long as V_{ERR} receives sufficient gain, you can easily dis-

Fig 2—Adding R_3 extends selectively amplifying V_{ERR} to measuring the distortion of a generalized noninverting amplifier.

Fig 3—Selective amplification of an inverting amplifier follows directly from the noninverting case of Fig 2.
tistinguishing amplifier-distortion products in the output signal.

However, you must limit the gain you choose for
$V_{ERR}$, or amplifier-response roll-off will restrict measurement of higher-frequency harmonics. The gain applied to $V_{ERR}$, not that applied to $V_{IN}$, sets the amplifier's bandwidth. To determine your measurement's bandwidth, calculate the feedback factor, considering $R_c$ to be grounded rather than bootstrapped. Then, for the circuit in Fig 2,

$$\beta = \frac{R_1}{R_c + (R_1 || R_2)}.$$

This feedback factor defines a measurement-bandwidth limit of $\beta f_c$, where $f_c$ is the unity-gain crossover frequency of the op amp. Beyond this limit, higher-order harmonics are attenuated in the measurement. Thus, again, you should consider a balance between test-equipment error suppression and higher-frequency resolution when choosing $R_c$.

**Accounting for gain differences**

However, determining the output-referred distortion still requires separating the $A_{CL}$ and $A_{ERR}$ effects on the circuit in Fig 2. Selectively amplifying the distortion signal makes its effect dominant in the measurement. You must again adjust the measured distortion to account for the difference in signal and distortion gains. To adjust the measurement result, remove the selective gain that the amplifier distortion receives. In Fig 2, resistors $R_1$ and $R_2$ supply a gain of $A_{CL} = 1 + \frac{R_2}{R_1}$ to both $V_{IN}$ and $V_{ERR}$. $R_c$ supplies additional gain to $V_{ERR}$. This added gain $(1 + \frac{R_2}{R_c})$ amplifies only the distortion signal. To compensate, divide the measured distortion result by this added gain.

$$THD + N_0 = \frac{R_1}{(R_1 + R_c)} \cdot THD + N_M = \frac{(R_1 + R_c)}{R_1} \cdot THD + N_{IN}$$

OR

$$THD_{OUT} = \frac{R_1 \sqrt{(V_{out}^2 + V_{out}^2 + V_{out}^2 + ...)}}{(R_1 + R_c)} \cdot \frac{V_{IN}}{(100\%)}$$

The selective amplification in Fig 2 translates directly for inverting op-amp configurations. To convert Fig 2 to an inverting amplifier, simply switch the circuit connections to the common return and the input signal (Fig 3). This switch returns the op amp's noninverting input and $R_c$ to ground and causes $V_{IN}$ to drive $R_1$. As before, resistors $R_1$ and $R_2$ set the gain, $A_{CL}$, presented to $V_{IN}$, and resistor $R_c$ boosts this gain to a higher level, $A_{ERR}$, for $V_{ERR}$. This higher gain determines the feedback factor and resulting measurement's bandwidth.

The only way Fig 3 differs from Fig 2 is in the common-mode input signal of the amplifier. In the noninverting circuit in Fig 2, input signal $V_{IN}$ is a common-mode signal to the amplifier's inputs, and it exercises nonlinearities in the amplifier's CMRR. The inverting circuit in Fig 3 removes this common-mode signal from the amplifier's inputs. Then, only the gain nonlinearity of the amplifier influences the amplifier's distortion. This difference permits you to separate gain and CMRR distortion effects.

**Combining the two methods**

Selective amplification in the inverting case offers another alternative. Both selective amplification and signal separation work in inverting circuits. However, the combination places greater demands on measurement bandwidth. Selective amplification obviates the instrumentation amplifier used before. To eliminate the instrumentation amplifier, Figs 1 and 2 move the signal measurement to the op amp's output. There, signal separation is compromised because the full test signal remains in the measurement.

This compromise is unnecessary for inverting configurations. As mentioned before, inverting configurations do not require the instrumentation amplifier for the signal-separation measurement. Thus, with inverting configurations you need not move the measurement to the amplifier's output. Instead, signal separation and selective amplification combine at the amplifier's input (Fig 4). There, $R_c$ develops a feedback current with $V_{ERR}$ just as before.
MEASURING OP-AMP DISTORTION

However, the circuit in Fig 4 does not rely on \( R_2 \) to convert this feedback current to an amplified output error. Instead, a second resistor, \( R_4 \), added at the amplifier's input, does this job. The feedback current produced in \( R_4 \) conducts through \( R_1 \) to produce the desired amplification right at the amplifier's input. At the top of \( R_4 \), the signal is \(- (1 + R_4/R_3) V_{\text{ERP}}\). This amplified error signal remains free of the large test signal present in the amplifier's output. As before, this separated error signal permits measurements free from signal-generator distortion and eliminates large dynamic-range requirements.

The distortion measured in Fig 4 requires three adjustments for converting it to output-referred distortion. First, compensate the difference in measured and actual fundamental signals as in previous signal-separation measurements. Then, make two gain adjustments. The measured signal receives a measurement gain of \((1 + R_4/R_3)\) but does not receive the circuit closed-loop gain of \( A_{\text{CL}} = (1 + R_4/R_3) \). To compensate, divide the measured distortion by the measurement gain and multiply it by \( A_{\text{CL}} \).

\[
\text{THD+N} = \frac{R_4 (R_3 + R_2) V_{\text{ERP}}}{R_3 (R_3 + R_2) V_{\text{OUT}}} \text{THD+N}_M
\]

OR

\[
\text{THD}_{\text{OUT}} = \frac{R_4 (R_3 + R_2) \sqrt{V_1^2 + V_2^2 + V_3^2 + \ldots}}{R_3 (R_3 + R_2) V_{\text{OUT}}} (100\%)
\]

Fig 4 introduces an added attenuation to the circuit's feedback factor, restricting measurement bandwidth. In addition to the normal feedback attenuation of \( R_1 \) and \( R_2 \), a second feedback attenuation results from \( R_4 \). \( R_3 \) and \( R_1 \) also produce a loading effect on the attenuation of \( R_1 \) and \( R_2 \). The net Fig 4 feedback factor is

\[
\beta = \frac{R_1 R_3}{R_1 R_3 + R_2 R_1 + R_3 R_1 + R_2 R_3 + R_1 R_3}
\]

The relationship of bandwidth to gain bandwidth, \( BW = \beta GBW \), then determines the bandwidth for the circuit in Fig 4. For the specific components of Fig 4, \( \beta = 0.0043 \) and \( GBW = 10 \text{ MHz} \) for \( BW = 43 \text{ kHz} \).

Because of the low feedback factor, this measurement's bandwidth is below the 80 kHz desired for audio applications. Other choices for \( R_1 \) and \( R_2 \) offer higher feedback factors to improve bandwidth, but such choices lower the selective gain. With less gain, the distortion signal's level is closer to the test equipment's measurement floor. Because of this compromise, you should use the circuit in Fig 4 only where signal-generator distortion must be separated from the test signal. In other cases, the basic selective-gain configuration offers a better compromise.

The input capacitance of the signal analyzer, \( C_1 \), alters the feedback factor in Fig 4. This capacitance bypasses \( R_1 \) and can cause gain peaking or even oscillation. Such problems occur only if the break frequency of the bypass, \( 1/2\pi R_1 C_1 \), is within the amplifier's closed-loop bandwidth. In this case, add a compensating capacitor in parallel with \( R_2 \) to roll off the gain peaking. Choose this capacitor to break with \( R_1 \) at the same frequency that \( C_1 \) breaks with \( R_1 \parallel (R_2 + R_3) \). Then, the feedback-divider action of the \( R_2 \) and \( R_4 \) legs remains approximately constant with frequency.

Gain variation extends resolution

Some op amps' distortion-measurement requirements exceed test equipment's capabilities even when you use the preceding methods. When your op amp
has low distortion over wider bandwidths, or just extremely low distortion, you need variable test configurations to characterize fully its distortion-versus-frequency performance.

First, low distortion levels automatically rule out the basic signal-separation approach of Part 1 because that approach requires an instrumentation amplifier of even lower distortion than the op amp under test. Instead, use selective amplification, which places measurement bandwidth and measurement resolution in competition. You must maintain measurement bandwidth to around 80 kHz to resolve harmonics important to the audio range. This bandwidth limits the selective amplification to a gain of $g = \frac{GBW}{80kHz}$.

However, your setup need not maintain full bandwidth at every test frequency. The amplitude of distortion harmonics drops as their frequencies get further away from the fundamental's frequency. Because of this decline, a measurement bandwidth that spans only five or six harmonics is sufficient. A smaller measurement bandwidth permits the use of higher selective gains to better resolve the lower distortion levels encountered at lower frequencies. Higher test frequencies require the full bandwidth, but they also cause correspondingly higher amplifier distortion. Accordingly, higher test frequencies require less selective gain, extending measurement bandwidth. Thus, the gain/bandwidth compromise of selective amplification yields to distortion measurement with varied gains.

The OPA627, for example, requires three selective-gain steps, each step providing a different gain/bandwidth combination. Fig 5 details this gain variation, which revolves around the THD$_{IN}$- vs-frequency plot. As this plot shows, op-amp distortion typically rises at higher frequencies, where measurement bandwidth is most needed.

**Power-supply bootstrapping for noninverters**

Signal separation is a complete solution only for inverting configurations. Using a power-supply bootstrap avoids limitations in noninverting solutions. Given care to avoid ground loops, the bootstrapping approach separates the common-mode signal, extending signal separation to the noninverting case.

To permit an optimal analyzer connection, power-supply bootstrapping moves the circuit's common from the normal circuit ground to the op amp's noninverting input (Fig 6). As odd as it may seem to consider an op amp's noninverting input to be the common, the common of a circuit is a relative point that you can define to be anywhere you choose. This connection retains the common-mode swing for the amplifier but removes that swing relative to common and, thus, removes it from the analyzer's input.

Theoretical niceties aside, redefining the common introduces ground-loop errors. The effects of these errors depend on the sensitivity of the circuit to voltage drops in its connecting lines. In Fig 6, the element most sensitive to such voltages is the signal analyzer because it measures a small signal superimposed on a larger one. For this reason, the figure shows the signal analyzer returned to the circuit's new common. Fig 6 makes the power-supply connections vulnerable to line drops, but the power-supply rejection of the op amp attenuates the resulting voltages.

For Fig 6, the test-equipment demands again decrease by a factor of $1/(1/A + 1/CMRR)$. However, the measurement made in Fig 6 requires adjustment to account for the reduced fundamental measured. For this reason, the figure shows the signal analyzer returned to the circuit's new common. Fig 6 makes the power-supply connections vulnerable to line drops, but the power-supply rejection of the op amp attenuates the resulting voltages.

For Fig 6, the test-equipment demands again decrease by a factor of $1/(1/A + 1/CMRR)$. However, the measurement made in Fig 6 requires adjustment to account for the reduced fundamental measured. For this figure, the relevant signal swing is that across the load resistor, or $V_{IN}$. Therefore, multiply the measured distortion by $V_{ERR}/V_{IN}$.

The actual adjustment made depends on the type of signal analyzer used. Measurements made with a distortion analyzer directly produce a THD+N percentage. Simply multiply this percentage by $V_{ERR}/V_{IN}$ and Fig 6's output distortion plus noise is then

$$\text{THD+N}_0 = \frac{V_{ERR}}{V_{IN}} \text{THD+N}_M = \text{THD+N}_IN.$$
MEASURING OP-AMP DISTORTION

You must measure the magnitude of V_{ERR} separately because distortion-analyzer outputs do not normally indicate this magnitude.

When you measure distortion with a spectrum analyzer, no separate measurement is required. Spectrum analyzers display the magnitudes of the fundamental and harmonic signals individually. You can then calculate distortion from the fundamental THD equation. Multiply this equation by V_{ERR}/V_{IN}, where V_{ERR} is equal to and therefore replaces V_{IN}, and V_{IN} remains in the denominator. Then, the spectrum analyzer result for Fig 6 is

\[ \text{THD}_{\text{OUT}} = \sqrt{V_{1}^2 + V_{2}^2 + V_{3}^2 + \ldots} \]

(100%).

Bootstrapping resolves noninverting cases

The convenience of Fig 6 extends to the generalized noninverting amplifier. As Fig 7 shows, power-supply bootstrapping again permits directly measuring V_{ERR} with a grounded signal analyzer.

Only one difference separates the measurements of the two circuits. The greater gain of Fig 7 results in a larger load signal V_{LOAD}. This gain also amplifies V_{ERR}, making the distortion in V_{LOAD} greater than that measured in V_{ERR}. You can adjust the measured distortion later to compensate for the effect of this gain. Finally, the added gain further reduces the performance requirements of the test equipment. For a given level of V_{LOAD}, V_{IN} is smaller for Fig 7 than for Fig 6. Thus, with Fig 7, V_{IN}’s reacting with the amplifier’s CMRR produces a smaller V_{ERR} signal. The noninverting configuration reduces the signal measured by a factor of V_{LOAD}/V_{ERR} = 1/(1/\beta + 1/\text{CMRR}).

Consider Fig 7 with the common return first at the top and then at the bottom of the signal generator. This change makes no difference in the equations relating amplifier voltages to the V^+ and V^- supply terminals. For both configurations, the V_2 - V^- and V_2 - V^+ equations are the same as those for Fig 6. Amplifier feedback forces V_1 = V_2 to again extend these equations to Fig 7’s input. Thus, whether bootstrapped or not, the amplifier distorts the input signal.

Fig 7’s greater gain produces a different output result than Fig 6. To define V_{OUT} relative to V^+ and V^-, first determine the load voltage, V_{LOAD}. You can find this voltage from the loop formed by the load resistor with resistors R_1 and R_2. The input signal, V_{IN}, appears across resistor R_1, producing a feedback current of V_{IN}/R_1. This current flows in R_2 to develop a voltage of V_{IN}R_2/R_1. Adding the voltages on R_1 and R_2 shows the voltage on the load to be V_{LOAD} = (1 + R_2/R_1)V_{IN}. This result portrays the familiar response of a noninverting op-amp configuration and is independent of Fig 7’s redefined common. Thus, the bootstrapping does not affect the load voltage and the corresponding amplifier output current.

Similarly, the loops relating V_{OUT} to V^+ and V^- remain unchanged. With the common on either side of the signal generator, the output voltages with respect to the amplifier supply terminals are

\[ V_{OUT} - V^- = V_{LOAD} + V^- \]
\[ V_{OUT} - V^+ = V_{LOAD} - V^+ \]

Thus, both input- and output-signal conditions are independent of the Fig 7 common connection, and the bootstrapping does not change the amplifier’s distortion products.

You must convert the distortion measured in Fig 7 to output-referred distortion. In Fig 7, the circuit amplifies the distortion products in V_{ERR} by 1/\beta to produce greater distortion signals in V_{OUT}. This effect changes the correction factor to V_{ERR}/\beta V_{IN}. However, because the same gain amplifies the input signal, V_{IN}, the final correction factor becomes \beta V_{ERR}/V_{IN} = V_{ERR}/V_{IN}. Thus, Fig 7’s correction equations are the same as Fig 6’s.

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Multi-Output Models-3, 4, or 5 outputs (Partial Listing)

<table>
<thead>
<tr>
<th>Size (HxWxL)</th>
<th>Total Watts</th>
<th>Output Voltage Range/Max. Amps</th>
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<td>2-6V/25A</td>
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Single Output Models (Partial Listing)

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<tr>
<td>5x8x15.5&quot;</td>
<td>3000W</td>
<td>2-4V/700A</td>
</tr>
</tbody>
</table>

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MEASURING OP-AMP DISTORTION

ping and selective amplification achieves even greater distortion resolution. This way, you can test the very lowest distortion amplifiers with a distortion analyzer. This particular amplifier-and-analyzer combination is the only case where noise becomes a limit to op-amp distortion measurement. And for a spectrum analyzer, the ambient noise of the test environment requires your careful attention to avoid coupling stray noise into your circuit. With either type of analyzer, selective amplification expands distortion resolution for the bootstrapped voltage follower.

The benefits of power-supply bootstrapping and selective amplification combine in Fig 8. In this circuit, the only signal developed at the amplifier's output is the amplified error signal:

\[ V_{\text{OUT}} = -(1 + R_2/R_1)V_{\text{ERR}}. \]

A signal analyzer measures this amplified signal referenced to ground with no interference from the test signal. In addition, the amplified distortion signal conveniently overrides the background noise of the signal analyzer and the measurement environment. This convenience does not extend to the general noninverting case because added gain there restores the test signal to the amplifier's output.

Other characteristics of the measurement shown in Fig 8 follow directly from earlier results. Selective amplification reduces the measurement bandwidth from \( f_c \) to \( \beta f_c \). Here, \( f_c \) is the unity-gain bandwidth of the op amp. The feedback factor is \( \beta = R_1/(R_1 + R_2) \). Fig 8's test-equipment requirements are the same as for the bootstrapped follower of Fig 6. As with that circuit, the distortion and dynamic-range requirements of the test equipment decrease by a factor of \( 1/(1/A + 1/\text{CMRR}) \). Because the selective amplification amplifies both the amplifier's distortion products and the background signal, \( V_{\text{ERR}} \), it does not improve this factor. The attenuated generator distortion present in \( V_{\text{ERR}} \) gets amplified along with the amplifier distortion products. The relative significance of generator distortion is unchanged. Similarly, the selective gain amplifies both the maximum and minimum signals to be resolved by the analyzer. Thus, the dynamic range of the measurement is also unchanged.

For the same reasons, results measured with the circuit in Fig 8 translate output-referred distortion with the same equations as those used in Figs 6 and 7.

**References**


**Author’s biography**

For Jerald Graeme’s biography, see Part 1 of this series on pg 133.

---

WHAT'S COMING IN EDN

Instrument designers and test-and-measurement companies are constantly on the prowl for new ways to make measurements simpler and more accurate. EDN Magazine’s March 2, 1992, Special Report investigates new measurement techniques and a few of the products that implement them.

In the same issue, check out the staff-written Technology Update on ANSI’s progress with establishing standards for the FDDI (Fiber Distributed Data Interface) using twisted-pair wiring.
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Specifications

<table>
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<tr>
<th>INPUT (Continuous)</th>
<th>28DC515-150</th>
<th>26DC515-150 (Transient)</th>
</tr>
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<td>22.34 VDC (28 VDC NOM)</td>
<td>17.34 VDC (Available)</td>
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<td>CURRENT LIMIT</td>
<td>(KNEE)</td>
<td>10% FL</td>
<td>85% FL</td>
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</table>

| INITIAL SETTING @ Vin NOM, F.L. (MAX) | ±0.5% | ±0.5% |
| LINE REGULATION (MAX) | 0.1% | 0.2% |
| LOAD REGULATION (MAX) | 0.1% | 0.4% BAL |
| TOTAL VOLTAGE CHANGE (MAX) | 1.0% | 2.0% CROSS |
| INCLUDES: LINE, LOAD, CROSS, TEMP., AND INITIAL SETTING |

| OUTPUT RIPPLE and NOISE (MAX) | 60mV p-p | 90mV p-p |
| (20MHZ BW, MIN-F.L, Vin NOM) |     |     |

| TRANSIENT RESPONSE (TYP) | 500mV/80µS | 200mV/40µS |
| 33% LOAD CHANGE |     |     |

| OVERVOLTAGE PROTECTION (MAX) | 6.9V | 17.0V |
| (AUTO RECOVERY) |     |     |

| EFFICIENCY | (Vin NOM, F.L.) | >80% |
| OPERATING FREQUENCY | 250KHz |

<table>
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<tr>
<th>TEMPERATURE RANGE</th>
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</table>

<table>
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<tr>
<th>BASEPLATE</th>
</tr>
</thead>
</table>

| -55°C TO -85°C (Operating) | F.L | F.L. (150W) |
| -55°C TO +100°C (Derate) | 8.0A | F.L. (115W) |
| -55°C TO +100°C (Derate) | 9.0A | 2.0A (105W) |

| RISE TIME (TYP) | 200µS | 400µS |
| TURN ON OVERSHOOT | 0% | 0% |

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| MIL-STD-810, METHOD 507, PROC.1 |

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| MIL-STD-810, METHOD 514 |

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| 11.5 OZ (MAX) |

<table>
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<th>ISOLATION</th>
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</table>

| INPUT/OUTPUT |
| 100 VDC |
| PINS/CASE |
| 200VDC |
| OUTPUT RETURNS |
| COMMON |

Mechanical

TOLERANCES (UNLESS OTHERWISE SPECIFIED)

| XX +/- .02 |
| XXX +/- .010 |

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<table>
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<tr>
<th>Model</th>
<th>SPECmarks™</th>
<th>Performance Increase</th>
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<td>POWERserver 340</td>
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</tr>
<tr>
<td>POWERserver 560</td>
<td>89.3</td>
<td>24%</td>
</tr>
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</table>

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<th>Features</th>
<th>American Arium</th>
<th>Tektronix'</th>
<th>Hewlett Packard'</th>
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<tr>
<td>High price</td>
<td>NO</td>
<td>YES</td>
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</table>

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American Arium's new single card capture system for the ML4400 Logic Analyzer featuring 100 and 200 MHz synchronous and 1 GHz asynchronous data capture. With 100 channels of 100 MHz synchronous capability per capture card, plus the powerful features of the ML4400, Paladin delivers the maximum capability available today for state and timing measurements on high-performance µP-based designs.

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David A Johnson, David Johnson and Associates, Littleton, CO

The circuit in Fig 1 operates off a 120V ac line and is cheaper and smaller than more common circuits that consist of a small iron-core transformer, a bridge rectifier, a filter capacitor, and a voltage regulator. The circuit transfers power from the 120V ac line to a voltage-regulator circuit by discharging a capacitor through a small high-frequency transformer twice each power-line cycle. A bidirectional discharge circuit comprising two small SCRs, CR1 and CR2, and two current-steering rectifiers, D1 and D2, provides the power switching. A low-cost and common speaker impedance-matching transformer reduces the voltage and provides isolation. SCRs work better than triacs in this design because triacs require more gate drive and higher holding currents than do SCRs.

The resistor-divider network R1 to R3 defines a voltage trigger point of approximately 140V for the two SCRs. Each time C1 discharges, the circuit induces voltage spikes in the primary winding of the transformer. The transformer translates the pulses to its secondary winding, where D3 and D4 rectify and C2 filters the pulses. An inexpensive 78L12 3-terminal regulator provides voltage regulation. With the components in Fig 1, the circuit supplies a 12V output and a maximum current of 15 mA. The circuit will operate with an input as low as 108V ac.

EDN BBS /DL_SIG #1083

To Vote For This Design, Circle No. 746

---

Fig 1—Smaller and cheaper than many other off-line power supplies, this low-power circuit transfers power from a 120V ac line to a voltage regulator by discharging a capacitor through a small, high-frequency transformer.
**Split supply operates from a single cell**

Mitchell Lee, Linear Technology Corp, Milpitas, CA

Batteries power many portable instruments, but many cells are usually necessary to directly implement a split supply. The circuit in Fig 1 uses a micropower dc/dc converter to provide ±5V from just one alkaline or NiCd cell. The circuit outputs 100 mW from a fresh cell and 50 mW when the cell's voltage drops to 1.05V. The circuit provides the output power in any current combination; for example, 5 mA from each output, 10 mA from one output, or 7 mA from one output and 3 mA from the other. This flexibility is especially useful for op-amp supplies in which the load current returns to ground. In this case, only one side of the split supply delivers high currents at any given time.

The LT1073 micropower dc/dc converter contains a switching element and regulating loop to maintain a ±5V output over a wide range of load currents and over the full life of the battery. If loading on the positive output exceeds the loading on the negative output, R₁ and R₂ feed back to pin 8 and maintain regulation. If the negative output is more heavily loaded, D₁ and Q₁ provide feedback to pin 8. Positive output regulation is less than 0.2% for loads from 2.5 to 7.5 mA. Negative output regulation is 2% for the same loads. Cross regulation is acceptable with a load imbalance as high as 10 to 1. You can extend cross regulation by adding the optional zener diodes, D₂ and D₃. The positive output cross regulation is 0.8% with a 2.5-mA load. The negative output cross regulation is 4% with a 2.5-mA load.

Efficiency with a 1-mA load on each output is greater than 75% over the 1.05 to 1.5V input range. Although the circuit suits 1-cell inputs, operation is also possible with two or three cells. When using more cells, the available output power will be somewhat higher.

**Fig 1—To produce a split supply from a single cell, this circuit uses a micropower dc/dc converter to supply ±5V and any 10-mA current combination.**
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**SPECIFICATIONS (typ)**

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CIRCLE NO. 73
Synchronous switch mutes line noise

M J Salvati, Flushing Communications, Flushing, NY

A variety of line-operated devices, such as neon lamps, SCRs, triacs, and fluorescent lamps, produce powerful RF signals that may interfere with nearby radio receivers. The circuit in Fig 1 improves the intelligibility of the recovered audio by muting the audio path during the noise-pulse interval. This scheme works only when the noise pulse arises from a single dominant nearby noise source. However, the circuit has an advantage over simpler clipping circuits because it doesn’t require a steady signal amplitude to operate properly. Also, unlike RF and IF noise blankers, the entire circuit is external to the receiver. Thus, using this circuit doesn’t require you to modify existing receivers.

Power-line-related noise generally occurs at a repetition rate of twice the local power-line frequency. Because the same line power drives the noise blanker and the noise source, the output of the bridge rectifier will be frequency and phase coherent with the noise pulses.

The circuit applies a rectified signal to the Schmitt input, pin 5, of the 74HC4538 dual monostable multivibrator. The first monostable delays the blanking pulse that the second monostable produces. This delay, which you can vary using the position potentiometer, lets you position the blanking pulse to coincide with the noise pulse in the audio signal.

The width potentiometer of the second monostable lets you adjust the blanking pulse to the minimum width sufficient for effective blanking while minimizing distortion. The blanking pulse appears at the inverted output of the second monostable. This normally high output level keeps the p-channel FET cut off. When the blanking pulse appears, this output goes low, and the FET conducts, thus shorting the audio-signal path. The RC filter at pin 9 of the second monostable also helps minimize distortion of the recovered audio by slowing the fast rise and fall times of the blanking pulse.

Fig 1—The position adjustment of this noise-muting circuit lets you align the blanking pulse to coincide with the audio-signal’s noise pulse. The width adjustment helps minimize distortion.

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Large capacitor serves as battery backup

Michael Grimm, Maxim Integrated Products, Sunnyvale, CA

A large capacitor—on the order of 0.1F—can replace your backup battery in certain applications. Though limited in storage capacity, the capacitor offers sufficient backup for low-dissipation equipment in which typical power outages last from a few seconds to several hours. The simple implementation that Fig 1 shows combines the capacitor with a battery-switch-over IC, a device that monitors the supply and switches the load to the battery voltage when the main supply fails or brownouts out.

The Fig 1a circuit includes various features to ensure proper operation of the switch-over IC. The 100-kΩ resistor, whose current comes from the main supply, keeps D1 forward biased and ensures the typical VBE drop of 0.6V across D1. The resistor maintains a safety margin of one VBE against droop in the VDD supply. D2 prevents this resistor from discharging the capacitor during backup. You can increase the margin by adding diodes in series with D1.

Fig 1b improves on the original circuit by replacing D1 and D2 with R2 and Q1, respectively. In Fig 1a, the charging path via the diode has a time constant that postpones the availability of backup power following power on. For Fig 1a, the power delay would be 10-kΩ × 0.1F = 1000 sec, or more than 16 minutes. Fig 1b divides this delay by the transistor’s beta, which is typically 100.

Spice model mimics reference

Joe Buxton, Analog Devices Inc, Santa Clara, CA

Seemingly simple dc components can cause simulation inaccuracies if you don’t have correct models for them. For example, the common practice of modeling a voltage reference using a Thevenin equivalent circuit doesn’t produce accurate simulations under dynamic and transient conditions. When driving a successive-approximation ADC, step changes in load current cause voltage disturbances at the reference output. The reference’s recovery time after this disturbance affects the accuracy of the ADC’s result. Other non-ideal reference characteristics include load and line regulation, current limiting, temperature coefficients, turn-on and turn-off conditions, and short-circuit current.
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EDN February 17, 1992 • 161
The macromodel in Fig 1 and Listing 1 (which is also posted on the EDN BBS (617) 558-4241,300/1200/2400,8,N,1—from main menu, enter (s)ig, <s/d_sig>, rk1087) for the REF-01 10V voltage reference includes features to account for some of these real-world characteristics. You can apply many of the concepts and techniques used to create this model to creating more accurate models of other simple dc devices.

An important feature of this model is its temperature sensitivity. By including the temperature coefficient for R1, which creates the model's internal 1.23V reference in conjunction with I1, the output voltage varies linearly with temperature. The thermal noise of R1 also models the reference's output noise. The value of R1 that this models uses was calculated from the data sheet's output-noise specification. C1 sets the dominant pole and the slew rate of the reference, and thus controls the turn-on and transient-load settling times. The model's output stage sets the impedance and controls current limiting. EDN BBS /DL_SIG #1087

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Fig 1—Simple dc components, such as voltage references, need accurate models. This REF-01 model includes the temperature coefficient for R1, so that the output voltage varies linearly with temperature. The model does not include second-order, nonlinear drift effects.

**Listing 1—Spice REF-01 model**

```plaintext
* * * NODE NUMBERS
* * *
* VIN GND TRIM VOUT
* .SUBCKT REF01 2 4 5 6
* 1.23V REFERENCE
* I1 4 10 1.22889E-6
R1 10 4 1000E3 [TC = 3E-6]
G1 4 10 2 4 73.9E-12
F1 4 10 VS 61.5E-9
* INTERNAL OP AMP
* G2 4 11 10 19 2E-3
R2 4 11 150E6
C1 4 11 2.1E-10
D1 11 12 DX
V1 2 12 1.3
* SECONDARY POLE
* G3 4 13 11 0 1E-6
R3 4 13 1E6
* * OUTPUT STAGE
* ISY 2 4 0.38E-3
FSY 2 4 V1 -1
G4 4 14 13 0 25E-6
R4 4 14 40E3
R7 17 19 14.2602E3
R8 19 4 2E3
R9 19 5 50E3
R10 5 4 1E12
Q1 16 14 17 QN
VS 18 17 DC 0
L1 18 6 1E-7
* * OUTPUT CURRENT LIMIT
* Q2 15 2 16 QN
R6 2 16 21
R5 2 15 18E3
C3 2 15 1E-6
G5 14 4 2 15 1
* .MODEL QN NPN(IS=1E-15 BF=1000)
.MODEL DX D(IS=1E-15)
.ENDS REF01
```

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Listing—Temperature measurement program

```
70 INTEGER I
80 Dm=728: HPIB address of multimeter (OM.)
90 OUTPUT Dm:"10" RS DRIVING:.../ L. resistance 5.5 digit resolutions auto
100 FOR I=1 TO 10000
110 OUTPUT Dm:"14" 7:3 50k ohm range (100µA bias); single trigger.
120 ENTER Dm/(100µA) Read value from DMM.
130 OUTPUT Dm:"99" 7:3 50k ohm range (100µA bias); single trigger.
140 ENTER Dm/(100µA)
150 OUTPUT Dm:"14" 7:3 50k ohm range (100µA bias); single trigger.
160 ENTER Dm/(100µA)
170 IF H<173 OR T>5500 THEN H=0 1
180 PRINT USING "Temperature in Kelvin. T: ,00,0000.D,000";"T";H-73;
190 NEXT I
200 OUTPUT Dm:"01" 1 For routine display
210 LOCAL Dm 1 Return DMM to local mode.
220 END
```

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Program mirrors brilliant circuit

Jim Williams's brilliant circuit in DI #945, “Transistor sensor needs no compensation” (EDN, April 25, 1991, pg 180), uses a transistor as a temperature transducer. It eliminates trimming by measuring the base-emitter voltage of the transistor at two different currents, and then uses the difference in VBE to calculate temperatures.

For automated measurements, connect the transistor directly to a computer-controlled multimeter such as the HP-3478A and select the resistance function. The meter sources a test current through the transistor, measures the resulting voltage, and returns a reading. The HP-3478A produces a 100-µA test current in the 30-kΩ range and 10 µA in the 300-kΩ range. A simple test program that makes measurements in both ranges can then calculate the temperature from:

\[ T(\text{°K}) = \frac{(V_{\text{BE}}(100 \, \mu A) - V_{\text{BE}}(10 \, \mu A))}{199 \, \mu V}. \]

The following HP-Basic program (Listing) makes two such measurements and averages them to eliminate drift. The measurement takes about 1.3 sec. An assortment of 2N2222A and 2N4401 transistors generated readings that varied over a 1°C range—not quite as tight as Mr. Williams reports.

Carl Spearow, Senior Engineer
Sundstrand Corp
4747 Harrison Ave
Rockford, IL 61105

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The latest trend in digital electronics is the introduction of numerous IC's operating on regulated 3V or 3.3V power supplies. This is a logical development to increase circuit densities and to reduce power dissipation. In addition, many systems are directly powered by two AA cells or 3V Lithium batteries. Clearly, analog IC's which work on 3V with good dynamic range to complement these digital circuits are, and will be, in great demand.

Many Linear Technology operational amplifiers work well on a 3V supply. The purpose of this design note is to list these devices and their performance when powered by 3V. The op amps can be divided into two groups: single and dual supply devices. The single supply op amps are optimized for, and fully specified at, a 5V positive supply with the negative supply terminal tied to ground. Input common mode voltage range goes below ground, and the output swings to within a few millivolts of ground while sinking current. Members of the single supply family are the micropower LT1077/LT1078/LT1079 single, dual and quad op amps with 40µA supply current per amplifier, the LT1178/LT1179 dual and quad with 13µA per amplifier. The LT1006/LT1013/LT1014 single, dual and quad have faster speed and lower voltage noise, at the expense of 300µA per amplifier.

The performance of these devices at 3V is quite similar to the 5V specs. Clearly, input voltage range and output voltage swing have to be reduced by 2V since the supply is 2V less. Offset voltage change from 5V to 3V is determined by the power supply rejection ratio specs. At 114dB or 2µV/√Hz the degradation in offset voltage is only 4µV (= 2V x 2µV/√Hz). Input bias and offset currents, voltage and current noise, as well as offset voltage drift with temperature, are practically unchanged compared to the 5V specifications.

Table I summarizes the performance of the low cost grades of these single supply devices at 3V. One note of caution: the minimum operating voltage for the LT1013/LT1014 is 2.95V. All other devices work on lower supplies, ranging from 1.7V to 2.6V.

Table I. Single Supply Op Amps: Low Cost Grade Specifications $V_S = 3V, \mathrm{OV}$. $T_A = 25^\circ \mathrm{C}$.

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<th>LT1077CN8</th>
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<th>LT1178CN8</th>
<th>LT1006CN8</th>
<th>LT1179CN8</th>
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<td>—</td>
</tr>
</tbody>
</table>
The LT1101 micropower (= 75µA) instrumentation amplifier completes the single supply family. Again, this in amp in 8 pin packages is fully specified at 5V. Minimum supply voltage is 1.8V; the performance change in going from 5V to 3V supply is minimal.

The second group of devices are dual supply op amps, i.e., the common mode input voltage and the output swing are limited to a diode voltage (= 600mV) above the negative supply terminal for proper operation. In addition, dual supply op amps are traditionally optimized for ±15V operation. Thus, reducing the total supply voltage to 3V represents a significant change. Table II lists the performance of four op amps: the LT1008 and LT1012 are actually fully tested at reduced supplies. The LT1097 and LT1001 performance is inferred from device evaluation data. Dual versions in 14 pin packages are also available: the LT1002 is a dual LT1001; the LT1024 is a dual version of the LT1012.

In most 3V applications the single supply op amps of Table I are more flexible and desirable, since no special biasing is needed to shift the input and the output into the operating range. However, the offset voltage drift with temperature performance of the dual supply devices is better. And, most importantly, when pico-ampere input bias currents are needed, the LT1008/LT1012/LT1097 have no competition. The op amps of Table I are all at least 6nA. The traditional ways of achieving pico-ampere bias current are not available either: JFET input or CMOS chopper-stabilized op amps do not function at 3V supply.

Figure 1 shows an application using the LT1078 to monitor the condition of the 3V battery. One output warns that the battery voltage is dropping, the other output shuts the system down as the battery voltage falls below the threshold value.

![Figure 1. Low Battery Detector with System Shutdown](image)

Table II. Dual Supply Op Amps at \( V_S = 3V \), \( V_O = 0V \). \( T_A = 25°C \). Low Cost Grade Electrical Characteristics.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>LT1097CN8</th>
<th>LT1008CN8</th>
<th>LT1012CN8</th>
<th>LT1001CN8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Voltage</td>
<td>20 100</td>
<td>40 180</td>
<td>25 120</td>
<td>40 150</td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>0.3 1.3</td>
<td>0.3 1.6</td>
<td>0.3 1.3</td>
<td>0.3 1.3</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>40 280</td>
<td>40 150</td>
<td>40 200</td>
<td>600 3500</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>40 260</td>
<td>30 150</td>
<td>30 200</td>
<td>350 3200</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>0.65 0.85</td>
<td>0.65 0.85</td>
<td>0.65 0.85</td>
<td>0.75 0.90</td>
</tr>
<tr>
<td></td>
<td>2.3 2.2</td>
<td>2.3 2.2</td>
<td>2.3 2.2</td>
<td>2.2 2.1</td>
</tr>
<tr>
<td>Output Swing</td>
<td>0.62 0.8</td>
<td>0.62 0.8</td>
<td>0.62 0.8</td>
<td>0.55 0.7</td>
</tr>
<tr>
<td></td>
<td>2.25 2.1</td>
<td>2.25 2.1</td>
<td>2.25 2.1</td>
<td>2.2 2.05</td>
</tr>
<tr>
<td>Voltage Gain ( R_C = 10K )</td>
<td>600 250</td>
<td>500 200</td>
<td>500 200</td>
<td>300 150</td>
</tr>
<tr>
<td>0.1Hz to 10Hz Noise</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.35</td>
</tr>
<tr>
<td>Minimum Supply Voltage</td>
<td>350 2.4</td>
<td>380 2.4</td>
<td>380 2.4</td>
<td>390 1.9</td>
</tr>
<tr>
<td>Supply Current</td>
<td>560</td>
<td>600</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>500</td>
<td>500</td>
<td>500</td>
<td>600</td>
</tr>
</tbody>
</table>

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The 5071A atomic clock is five times as accurate as its predecessor, which held the record as the world's most accurate clock. Though the vendor does not guarantee the instrument to run that long, if the clock kept going for 1.6 million years, it would lose <1 sec. Averaged for >5 days, its stability is better than two parts in $10^{11}$. Like its predecessors, the clock uses cesium-beam technology, but it achieves full accuracy within 30 minutes of turn-on. After warmup, the stability specs apply over a range of temperature and humidity; most extremely accurate instruments meet their specs only under laboratory conditions. $54,000; high-performance cesium-beam tube, $12,000. Delivery, 16 weeks ARO.

Hewlett-Packard Co, 19310 Prunedge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 405

Logic-Debugging Tool

- Includes 32-bit digital comparator with individual masks
- Provides programmable scope trigger

The LA-32 logic debugger is a battery-powered, handheld tool for testing μP-based systems that operate at clock frequencies to 24 MHz. It incorporates a 32-bit comparator with programmable masks and set points; a generator that produces pulse trains having programmable pulse widths, pulse spacings, and numbers of pulses; and an autoranging frequency counter that can take its input from any of the instrument's inputs or the comparator output. The unit, which includes a 16-character LCD, can display 32 channels at once and can produce a scope trigger upon satisfaction of conditions that you specify. In the autoselect mode, the unit automatically configures the pins of its chip clip to match the pinouts of popular EPROMs. $379; cables and adapters, $50 to $75.

Logix Inc, 1725 Roselawn Ave W, St Paul, MN 55113. Phone (612) 646-2324. Circle No. 406

Waveform Analyzer With Real-Time DSP Capability

- Incorporates processor rated at 25 Mflops
- Cross-correlates two 16-ksample records in <1 sec

Using the 683 DSP board, the 6100 waveform analyzer performs signal-analysis 300× as fast as similar units not so equipped. The instrument executes more than 50 mathematical operations. It can calculate an 8k-point FFT in msec and cross-correlate a pair of 16-ksample records in <1 sec. The heart of the board is a 32-bit floating-point DSP μP slaved to the analyzer's CPU. The two processors exchange data via DMA and simultaneous register transfers. The analyzer, which accepts plug-in front-end modules, handles signals to 1 GHz. You can install the DSP board in the analyzer. $2995.

Analogic Corp, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX (508) 532-6097. TLX 6817144. Circle No. 407
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**Flash-converter-based data-acquisition board.** The ANA100 half-length ISA-bus board includes an 8-bit, 2.5-μsec flash ADC and a DAC with full-scale output ranges of 2.5, 5, and 10V. $99. BSoft Engineering Inc, 444 Colton Rd, Columbus, OH 43207. Phone (614) 491-0832. FAX (614) 497-9971. Circle No. 409

**Clamp-on, true-rms digital ammeters.** The 30 series permits investigating problems such as false tripping of breakers protecting nonlinear loads. They measure to 700A and handle signal components to 10 kHz. The meters also measure frequency. Model 33 can also calculate and retain the minimum, maximum, and average values of a long sequence of readings. Model 31, $179; Model 33, $249. John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. TLX 185102. Circle No. 410

**Data-acquisition system.** The L-Tech data-acquisition module connects to the serial port of a Macintosh or an MS-DOS-based PC. The unit includes two 14-bit ADCs that make 100,000 conversions/sec. The menu-based software supports many processing functions including averaging and FFTs with or without windowing. $1995. Onsite Instruments, 855 Maude Ave, Mountain View, CA 94043. Phone (415) 964-9800. FAX (415) 964-9808. Circle No. 411

**Test station for mixed-signal ICs.** The mixed-signal ATS performs digital testing to 400 Mbits/sec with 100-ps/sec accuracy. For analog testing, the system's noise floor is at least 100 dB below full scale. Analog measurements beyond 1 GHz are possible. $630,000 for a 224-pin configuration. Integrated Measurement Systems Inc, 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117. FAX (503) 644-6969. Circle No. 412

**Data-acquisition and processing system.** The Presys 1000 system has a self-diagnostic capability that simulates the ADC's output using 16-bit counters. System with 64 channels, 500-ksample/sec ADC, 128-ksample FIFO buffer, and computer interface, $14,200. Deliv-
Software for disk-drive test and fault diagnosis. The GR228X focused-application package allows suppliers of disk drives and data-storage peripherals to test the devices on the vendor’s GR228X test systems. From $210,000. Delivery, 12 weeks ARO. GenRad Inc, 300 Baker Ave, Concord, MA 01742. Phone (508) 369-4000, ext 2101.

Handheld ESD tester. The model 611 Zapmaker tests devices and systems for susceptibility to electrostatic discharges (ESD). The unit supplies human-body-model waveforms in accordance with draft standard MIL 1686B. Previously, competitive units used resistor and capacitor values taken from the MIL standard but did not comply with the standard’s waveform requirements. $7250. Delivery, 8 to 12 weeks ARO. Keytek Instrument Corp, 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. FAX (508) 657-4903.

Programmable video generator. The Astro VG-815 generator allows comprehensive evaluation and testing of CRT displays. It works with displays whose horizontal-scan rates range from 10 to 180 kHz and pixel frequencies range from 5 to 135 MHz. From its front panel, you can make the generator store or recall 40 programs or patterns. The unit has RS-232C, TTL, and analog interfaces. $5350 to $18,950. Team Systems, 2934 Corvin Dr, Santa Clara, CA 95051. Circle No. 415

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MS-Windows driver for IEEE-488 bus. The Driver-488/Win dynamic-link library helps you integrate the control of IEEE-488 instruments into MS-Windows applications. The driver, which supports Microsoft and Borland languages, allows multiple tasks to access the same IEEE-488 interface card simultaneously. $195; with interface card, $385. IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093.

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Graphics Accelerator

- Attaches to the SBus in SPARCstation desktops
- Stand-alone tower chassis contains 40-MHz i860 CPU

The ViCOM VT is a graphics accelerator for desktop SPARCstation computers. A stand-alone chassis contains the company’s ViCOM VX VMEbus graphics board and a VMEbus to SBus adapter. The adapter attaches to the SBus in a SPARCstation computer. The graphics board contains a 40-MHz i860 CPU and a 2M x 8-bit frame buffer that is compatible with Sun’s GX frame buffer. The accelerator drives Sun’s 1152 x 900 and 1280 x 1024-pixel 19-in. monitors. In addition, the chassis has a VMEbus expansion slot that accepts the company’s ViCOM MVX board. The ViCOM MVX has four i860 CPUs, which boost the accelerator’s performance from 40 to 160 MIPS and from 80 to 320 peak single-precision

Mflops. ViCOM VT, $32,000; ViCOM VX, $24,000; optional ViCOM MVX, $30,000.

Stand-Alone Single-Board Computer

- Contains an 8- or 16-MHz 80C186EB µP
- Has four iSBX expansion ports and 512 kbytes of static RAM

The SBX-C186EB stand-alone single-board computer (SBC) for embedded applications contains an 80C186EB µP and an 80C187 coprocessor, which run at 8 or 16 MHz. The board has as much as 512 kbytes of static RAM and 512 kbytes of EPROM or flash EPROM. Other features include an 8570 real-time calendar clock, an interrupt controller, five 16-bit counter/timers, 32 parallel I/O ports, two serial I/O ports, a watchdog timer, and power-fail detection. Its four iSBX expansion ports attach to a variety of off-the-shelf SBX modules. You can develop programs in assembly code or Borland’s C++ language. An optional extended temperature range is available for -40 to +85°C operation. 8-MHz version, $425; 16-MHz version, $465.

RLC Enterprises, 4800 Templeton Rd, Atascadero, CA 93422. Phone (805) 466-9717. FAX (805) 466-9736. Circle No. 420

Solid-State Disk Emulator

- Transfers data at 4 Mbytes/sec on the ISA bus
- Nonvolatile-memory capacity ranges from 2 to 56 Mbytes

The Blue Flame III card emulates a solid-state disk drive in 386 and 486 ISA bus computers. Each card contains from 2 to 56 Mbytes of nonvolatile memory. The card is mapped to the host’s I/O space and accepts 14 1M x 9-bit or 4M x 9-bit single in-line memory modules. You can install 16 cards in a system to provide a maximum capacity of 896 Mbytes/drive. The cards have a 16-bit data path and can transfer data on the ISA bus at 4 Mbytes/sec. Onboard rechargeable NiCd batteries provide backup during power interruptions, and an optional external battery provides battery backup that exceeds 100 hours. A wall-mounted power supply lets you switch off the host computer without losing data. A device driver, which occupies less than 1 kbyte of RAM, runs with PC-DOS, MS-DOS, and Concurrent DOS. $595 for a 2-Mbyte version.

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* Up To 512K Of Battery Backed Static RAM
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* Program Controlled Dip-Switch And LED's
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**Tape backup system.** The SSCH40 4-mm digital-audio-tape backup system supports VAX cluster computers. It backs up 96 Gbytes on a 12-cartridge magazine and as much as 192 Gbytes, using a dual-drive loader configuration. The tape loader utilizes a robotic arm to insert and remove tapes in HP's 8-Gbyte, 4-mm tape drive. The system resides in a 19-in. enclosure and transfers data to and from the host at a sustained rate of 732 kbytes/sec. System with 8-Gbyte, 4-mm drive, ST01 channel card, and a 12-cartridge magazine, $15,340. Emulex Corp, Box 6725, Costa Mesa, CA 92626. Phone (800) 854-7112; (714) 662-5600. Circle No. 422

**19-in. rack-mount computer.** Versions of the rackmountable CRM/816 industrial computer have 10, 14, or 16 ISA bus slots or 10 or 14 EISA bus slots. Modular bays let you install as many as eight 5¼-in. peripheral devices such as hard-disk, floppy-disk, and tape drives. Dual 70-cfm fans cool the chassis, and a 22-cfm fan cools the power supply. You can lock a front-panel door to prevent unauthorized access. Powersupply options range from 250 to 350W when using 120V ac power input. A 14-slot ISA bus version having a 250W power supply, from $1295. Diversified Technology Inc, Box 748, Ridgeland, MS 38958. Phone (601) 856-4121. TLX 585326. Circle No. 423

**2.6-Gbyte tape drive.** The Ciera 2.6 tape drive offers 2.6 Gbytes of storage on an 8-mm tape cartridge. The subsystem comes with a host adapter, which fits in a workstation's expansion slot; it also provides cable, software, and documentation. The drive transfers data at 800 kbytes/sec and supports Novell and Unix client/servers. $6995. Cipher Data Products Inc, 10101 Old Grove Rd, San Diego, CA 92131. Phone (619) 693-7713. Circle No. 424

**Motion controller.** The DMC-120-10 STD Bus board has a µP that controls two independent axes of motion. The µP decodes position feedback signals, generates velocity profiles, and provides a PID (proportional-integral-differential) filter for the control-loop error signal. You specify the position, speed, and acceleration for each axis using 2-letter ASCII commands. The controller produces motor drive signals in the ±10V range. $585. Galil Motion Control Inc, 575 Maude Ct, Sunnyvale, CA 94086. Phone (408) 746-2300. FAX (408) 746-2315. Circle No. 425

**SCSI host adapters.** The DTC 3182 and DTC 3282 host adapters support direct-memory-allocation transfers on the 16-bit ISA bus. They control seven SCSI devices; the DTC 3282 controls four additional floppy-disk drives. The

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boards feature scatter-gather or bus-master transfers on the host bus and operate with DOS, OS/2, Unix, Xenix, and Netware software. Features include a custom µP, a SCSI chip, and a 15-byte FIFO buffer to provide continuous data transfer to each drive. DTC 3182, $159; DTC 3282, $189 (OEM qty).

Data Technology, 500 Yosemite Dr, Milpitas, CA 95035. Phone (408) 262-7700. FAX (408) 942-4052. TWX 910-338-0232.

Industrial PC card. The 5016 Micro PC is a half-length ISA bus card containing an IBM PC/AT-compatible computer. It operates over the industrial temperature range of -40 to +85°C. One solid-state disk contains DOS 3.31, and two additional solid-state disks are available for adding RAM and EPROM. The card has 4 Mbytes of dynamic RAM, as well as a COM1 serial port, keyboard port, speaker port, watchdog timer, calendar/clock, and coprocessor socket. $595. Octagon Systems Corp, 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 430-1500. FAX (303) 426-8126. Circle No. 427

Fiber-optic data-link adapter. The AC40 adapter permits devices having an RS-485 port to communicate over a fiber-optic link. It also has a host fiber-link port, and a repeater fiber-link port. Features include 115.4-kbaud communications; 4-km distance between nodes; ST style fiber-optic connectors; and 2- or 4-wire hook-up to the RS-485 port. The unit comes in a metal enclosure. $550. Opto 22, 43044 Business Park Dr, Temecula, CA 92590. Phone (800) 321-6786; (714) 695-9299. FAX (714) 695-2712. Circle No. 428

Industrial printer. The IP-80 printer uses a 9-pin dot-matrix mechanism to print bidirectionally at 200 eps. It mounts in control panels or on a standard 19-in. rack. The unit has a Centronics parallel port, a 4-kbyte buffer and 24 resident fonts; an RS-232C serial port is optional. $2395. Dianechart Inc, 101 Round Hill Dr, Rockaway, NJ 07866. Phone (201) 625-2299. FAX (201) 625-2449. Circle No. 429

Communications modules. The E-PAK family of modules extends the capabilities of the company's VMEbus single-board computers. The Model D contains a Zilog Z16C35 IC to manage four synchronous serial I/O ports at 1 Mbps. The Model E has a 78C500 32 IC to communicate with an Ethernet 10Base-T network. The Model F contains both Model D and F functions. The Model G has a Cirrus CL-CD180 IC to manage 16 asynchronous serial I/O ports. Model D, $560; Model E, $485; Model F, $795; Model G, $485 (100). Performance Technologies Inc, Computer Products Div, 315 Science Pkwy, Rochester, NY 14620. Phone (716) 256-0200. Circle No. 430

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• Emulates a stripline
• Has a 50Ω impedance
The FCN260 half-pitch (0.05-in.) pc-board connector emulates a stripline circuit. The design minimizes crosstalk to 3.8% max at a 1-nsec rise time by confining the signal conductor with a ground plane. Characteristic impedance, achieved by controlling the dimensions, construction, and insulator permittivity, equals 50Ω ± 10%. Connector construction consists of large ground planes on the center line and a metal ground shell around the plug. This construction maintains signal integrity across the board and eliminates the need for dedicated ground contacts—all contacts function as signal contacts. The connector is available in a 100-pin version. Plug-and-jack pair, $0.20 per mated line (2500).
Fujitsu Microelectronics Inc, Electronic Components Div, 3545 N First St, San Jose, CA 95134. Phone (800) 642-7616; (408) 922-9000. Circle No. 393

Surface-Mount Transformers
• Feature a low profile
• Have a 300- to 3500-Hz response
TS3000 Series surface-mount transformers meet FCC Part 68 regulation. Their mounted height is 0.32 in. The units are designed for dry-circuit, 600Ω line applications. They have a ±0.5-dB frequency response of 300 to 3500 Hz over a -45 to +7-dBm power-level range. The transformers are available for both coupling and hybrid applications. They feature 0.5% max distortion, 26-dBm return loss, 60-dB min longitudinal balance, and 1500V rms dielectric strength. The transformers are constructed from materials that have a UL 94V-0 flammability rating. Units with pins for through-hole-mounting applications are also available. The units measure 0.87 × 0.66 × 0.32 in. and weigh 0.2 oz. Approximately $3 (OEM qty).
Microtran Co, Box 236, Valley Stream, NY 11582. Phone (516) 561-6050. FAX (516) 561-1117. Circle No. 394
Oh no. Please, not now. Not with manufacturing release next week.

The Prototype Doesn't Work.

Six ASICs, fifteen PLDs and the whole thing's gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

The Prototype Doesn't Work.

Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

The Prototype Doesn't Work.

And my performance review comes up next month. Maybe they'll just forget about all this, right? Yeah. Sure.

The Prototype Doesn't Work.

Wait. What about that glitch in the handshake on the first pass? Couldn't reproduce it. Maybe it just reproduced itself.

The Prototype Doesn't Work.

These are just a few of the reasons Tek makes a complete line of scopes, logic analyzers and signal sources. Instrumentation that can quickly get to the core of your prototype's problems. Whether they're digital, analog or software. Because even when your prototype doesn't work, Tek does. Talk To Tek/1-800-426-2200
Ethernet transceiver. The ENT-4312 transceiver allows you to establish a 10BaseFL data link or fiber-optic inter-repeater link (FOIRL) through a user-selectable switch. Various interface options are available via an onboard SQE (signal-quality-error) switch. Other features include ST or SMA type connectors and a set of seven diagnostic LEDs, which indicate link status jabber, collision, receive, transmit, SQE, and power. The transceiver measures 1.75 x 0.92 x 3.8 in. and weighs 2.34 oz. $295. Lancast, 10 Northern Blvd, Unit 5, Amherst, NH 03031. Phone (800) 752-2768; (603) 880-1833. FAX (603) 881-9888. Circle No. 395

DC/DC converters. NMA surface-mount dc/dc converters are housed in a J-ledged package, which measures 11.81 x 11.81 x 6.09 mm. The units accept 5 or 12V inputs and offer outputs of ± 5, ± 9, ± 12, or ± 15V. Each output provides 1W of output power. The converters feature 1000V dc isolation, 80% efficiency, and operate over a -50 to +85°C range with no derating. $19.50. International Power Sources Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7434. FAX (508) 879-8669. Circle No. 396

Multichip module socket. This multichip-module socket is designed for a 256-pin, 0.65-mm, 45 x 45-mm body. It's suitable for high-density test and burn-in applications and features a novel lid, which simultaneously distributes a uniform mating force along all four package sides. Insulators are made of PPS (polyethersulfone), and contacts are beryllium copper with gold over nickel plating. $162.92 (100). Nepenthe, 2475 E Bayshore Rd, Suite 800, Palo Alto, CA 94303. Phone (800) 637-3684; (415) 496-6666. FAX (415) 856-8650. Circle No. 397

Extraction tool. The CT-2102 tool accommodates 4-sided plastic-leaded-chip-carrier (PLCC) packages having from 20- to 124-pin leads spaced on 0.05-in. centers. The tool precisely borders the object chip only—without interference with any components surrounding the PLCC socket. $16. Methode Electronics Inc, 1700 Hicks Rd, Rolling Meadows, IL 60008. Phone (800) 322-6864; (708) 392-3500. Circle No. 398

Coaxial attenuator. Model PE7022 is a 50Ω, 100W coaxial attenuator. Designed for operation over a dc to 1.5-GHz range, the device is available with attenuation values of 6, 10, 20, 30, and 40 dB. The attenuator features a built-in heat sink. VSWR equals 1.15:1 max, and operating range spans -65 to +125°C. $350. Pasternack Enterprises, Box 16759, Irvine, CA 92713. Phone (714) 261-1920. Circle No. 399
Flat-panel touch system. Modular/1 and Modular/2 infrared touch systems are available with software-based, hardware-based, or RS-232C controllers. Each controller is equipped with digital circuitry and provides plug-and-play capability. Both systems feature servo-loop circuitry that compensates for environmental factors. Programmable amplification makes both systems impervious to severe ambient light conditions. Modular/1, $285; Modular/2, $289 (100).

Carroll Touch Inc, Box 1309, Round Rock, TX 78680. Phone (512) 388-5614. FAX (512) 244-7040.

Pulse transformers. Housed in a package measuring 0.65 x 0.85 x 0.2 in., these pulse transformers suit either through-hole or surface-mount applications. The units meet applicable provisions of MIL-T-21038 and are characterized for operation over a -55 to +125 °C range. They support 2500V /μsec and feature rise times of less than 100 nsec. $25 (OEM qty). Delivery, stock to eight weeks ARO.

Controlex Corp, 16005 Sherman Way, Van Nuys, CA 91406. Phone (818) 780-8877.

Coaxial attenuators. Series 2082 5 and 10W coaxial fixed attenuators are designed for dc to 18-GHz operation. Standard units with SMA connectors are available in 3-, 6-, 10-, and 20-dB attenuation values. The 5W unit is also available in 30-dB versions. The manufacturer uses no hazardous beryllium oxide in constructing the device. 5W version, $77; 10W version, $162. MA/COM, Control Components Div, 21 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-4111. FAX (603) 424-6580.

R and C networks. MRGF Series resistor networks come in 16-pin SOIC packages and feature resistor values from 33Ω to 2.2 MΩ. Five circuit configurations are available: as many as 8 isolated double-ended resistors or 15 single-ended resistors with a common tap; ladder networks; divider networks; and terminator arrays. Temperature coefficient equals ±200 ppm/°C, and power rating at 70°C measures 500 mW/package. $0.30 (10,000). Delivery, eight weeks ARO. Raltron Electronics Corp, 2315 NW 107th Ave, Miami, FL 33182. Phone (305) 593-6033. FAX (305) 594-3973.

Circle No. 403

Miniature shunts. SNM Series microshunts mate with 0.018-in. square headers with pins located on a 0.05 x 0.1-in. grid. The terminals can pass through the shunt so the shunt can accept any post that has a minimum height of 0.12 in. The shunts are available with gold or tin plating over the phosphor-bronze contacts. From $0.088.

Samtec Inc, Box 1147, New Albany, IN 47151. Phone (800) 726-8329; (812) 944-6733.

Circle No. 404

High performance LCR meters from SRS. 0.05% accuracy, 100 kHz frequency.

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CIRCLE NO. 87
Low-Power, High-Speed 12-Bit ADC

- Includes on-chip S/H amplifier
- Has 750-ksamples/sec speed

The 12-bit AD7886 A/D converter combines a fast sampling rate of 750-ksamples/sec with 350-mW power consumption. The ADC features a triple-pass flash architecture that provides a data-access time of 57 nsec and a total conversion time of 1 µsec. These characteristics make the device suitable for use in high-frequency instrumentation applications. Other guaranteed ac characteristics include integral nonlinearity of ±2 LSB (max), a S/N ratio of 65 dB, and total harmonic distortion of −75 dB. Second- and third-order intermodulation distortion are typically −80 dB. The AD7886 operates from ±5V supplies and offers pin-strappable input spans of 0 to 5V, 0 to 10V, and ±5V. Package options include 28-pin DIPs and plastic leaded chip carriers. From $55 (1000).

Analog Devices, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 821-4273.

Circle No. 359

8-Channel, 12-Bit Data-Acquisition System

- Has a programmable multiplexer
- Sampling rate is 100 kHz

The MAX180, a 100-kHz data-acquisition system, includes a 12-bit ADC, a 6-MHz track-and-hold (T/H) amplifier, a −5V (25-ppm/°C) reference, a parallel µP interface, and an 8-channel multiplexer. The multiplexer allows independent programming of each channel for either differential or single-ended inputs, and unipolar 5V or bipolar ±2.5V operation. The T/H amplifier’s bandwidth allows undersampling of periodic signals having bandwidths exceeding the ADC’s sample rate. You can use a reference input supplied by the internal reference or an external source. The internal reference value and the system offset are adjustable to allow nulling of the overall system offset and gain errors. The MAX180 interfaces to 8- or 16-bit buses and operates from 5 and −12V supplies. The device is available in 40-pin DIPs and 44-pin plastic leaded chip carriers. From $17 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No. 359

Dual Op Amp With Micropower Sleep-Mode

- Reduces current drain to 45 µA
- Has industry-standard pinouts

Suiting a range of applications such as cordless telephones, portable computers, and handheld equipment, the MC33102 dual op amp features a “sleep” mode that reduces current drain to approximately 45 µA/amplifier. Triggered by an input signal, each amplifier changes to the “awake” mode in 4 µsec when output current exceeds 160 µA. The device returns to the sleep mode when the output current drops below its threshold. Each amplifier consumes approximately 75 µA when operating in the awake mode, with a ×10 improvement in bandwidth and slew rate. You can also use the device as a micropower amplifier. ESD clamps protect the inputs. A drop-in replacement for many other dual op amps, the MC33102 comes in 8-pin DIP and SO packages. $1.60 (10,000).

Motorola Semiconductor, EL340, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3615. FAX (602) 897-4193.

Circle No. 360
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OUR NEW PARTNERSHIP IS AS HOT AS IT GETS.

CIRCLE NO. 54
Communications controller. The COM20010, a token-passing communications controller, is targeted for high-speed data highways in factory process controls and building automation applications. You can use the device with coaxial, twisted-pair, or fiber networks. The controller interfaces with Intel, Motorola, Zilog, and NEC microcontrollers. A 1k x 8-bit RAM handles message storage. The device supports as many as 255 nodes at a data rate of 2.5 Mbps. From $11.36 (1000). Standard Microsystems Corp, Component Products Div, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100.

Light sensor. Linking directly to a microprocessor (µP), the TSL220 light-to-frequency converter converts small changes in light intensity to digital signals. The device, which has a dynamic range of 118 dB, typically produces a 100-kHz signal in office desk lighting and 1 Hz in darkness. An external capacitor can adjust the output frequency for a given light level to match the sensor to the input frequency range of a µP. $4.61 (1000). Texas Instruments Inc, Semiconductor Group (SC-91086), Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 700; outside US and Canada, (214) 995-6611, ext 700.

Triport bus exchanger. The IDT 73720 is a 16-bit triport bus exchanger for interbus communication in multiway interleaving memory systems and in high-performance multiplexed address and data buses. The device, which features a maximum port-to-port delay of 6.5 nsec, supports bidirectional read and write operations between the CPU and two memory ports, eliminating bus contention. 68-pin plastic leaded chip carrier, $9.70 (100). Integrated Device Technology, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674.

Smartcard microcontrollers. The ST16623 and ST16301 combine an 8-bit CPU with on-chip ROM, RAM, EEPROM, and hardware and software security features. The 16623 and 16301 offer 6 and 3 kbytes of ROM, 224 and 126 bytes of RAM and 3 and 1 kbytes of EEPROM, respectively. The devices have a 5-MHz operating speed and are available in die or micromodule form. ST16301, $2.78; ST16623, $3.82 (5000). SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290.

Servo driver/controller chip set. This 2-chip set is for 2.5-in. hard-disk drives. The SSI-32H510 servo driver is for systems employing linear or rotary...
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voice-coil motors. The SSI-32H6520 servo controller provides four areadetection circuits and includes embedded-servo burst processing, fault-detection logic, D/A circuitry, and a CPU/DSP bus interface. Driver and controller chips in 36- and 44-pin SO packages, $3.50 and $5.50, respectively (10,000). Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110. FAX (714) 669-8814.

Circle No. 365

**SCSI disk controller.** The AIC-8010 automated SCSI controller is for 1.8-, 2.5-, and 3.5-in. SCSI and SCSI-2 disk drives. Key features include automating SCSI operations through hardware implementation and control, full-track data access without µC intervention, automated buffer management, constant-density recording with embedded servo control, and 88-bit Reed-Solomon error correction. The AIC-8010 supports SCSI-2 data transfers of 10 Mbytes/sec and disk NRZ data rates of 36 MHz. In a 100-pin quad flatpack, $18.95. Adaptec, 691 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 945-8600.

Circle No. 366

**Graphics chip.** Compatible with existing MS-DOS programs, the OTI-087 24-bit color chip can increase graphics performance as much as 10 times and boost the speed of Windows programs as much as 5 times over existing VGA chips. The chip obtains its speed by communicating directly to 80386 and 80486 CPUs over the 32-bit local bus, instead of through the 16-bit AT bus. Available in a 160-pin quad flatpack, $31 (1000). Oak Technology Inc, 139 Kifer Ct, Sunnyvale, CA 94086. Phone (408) 737-0888. FAX (408) 737-3838.

Circle No. 367

**12C EEPROMs.** Compatible with the 2-wire FC bus, the XL24C04 operates from a 5V supply and features a Vl'l' lockout to ensure data integrity during power-up and power-down cycles. The companion XL24C04-3 has a range of 2.7 to 5.5V for battery operation. Internally organized as 256 x 8 bits, the lowpower devices draw only 1 mA (active) and 2 µA (standby). A 16-byte page-write mode and a self-timed write cycle minimize the total-per-byte write time. In 8-pin DIP and SO packages, the XL24C04 and XL24C04-3, $1.49 and $1.94, respectively, (10,000). Exel Microelectronics, Box 49038, San Jose, CA 95161. Phone (408) 432-0500. FAX (408) 434-6444.

Circle No. 368

**Dual-port video RAMs.** Available in two versions, these 2-Mbit video RAMs can handle the high-speed data and fast display-refresh rates inherent in advanced graphics applications. Both the fast-page version (µPD482234) and the hyper-page version (µPD482235) include dual ports. With one port for the CPU and one for the display, processor efficiency is doubled. The devices come in 40-pin SOJs and ZIPs, and 44-pin...
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Guideware Corp, 2483 Old Middlefield Way, Suite 224, Mountain View, CA 94043. Phone (415) 969-6851. Circle No. 371

Configuration-And Data-Management Software
- Has an X-Window graphical interface
- Supports software, electronic, and mechanical engineering projects
The Teamnet Unix-based configuration- and data-management tool tracks and controls files around an NFS (Network File System) Network. The software is based on an Openlook graphical user interface. The software resolves file sharing and edit conflicts using a 2-phase mechanism for checking in changes and managing your work area. File-merge capabilities allow a visual side-by-side comparison of conflicting file changes. A virtual-copy capability improves software performance in creating work areas, checking in changes, and building baselines. License, from $3000.

TeamOne Systems Inc, 710 Lakeway Dr, Sunnyvale, CA 94086. Phone (408) 730-3500. Circle No. 372

Numeric Computation Software
- Allows sparse-matrix approach to problem solving
- Allows visual and audio analysis
Matlab version 4.0 expands the software’s analysis and presentation capabilities. Flexible File I/O allows you to import and export large data sets. To improve the software’s ability to solve problems using these large data sets, the tool offers sparse-matrix algorithms that define computation time as a function of the nonzero elements in the matrix. The software solves problems written in the company’s programming language, allowing you to bypass traditional program/compile/debug cycles. Debugging features that bypass the traditional include breakpoint control, context changing during debugging, and single stepping. Application toolboxes provide special functions for DSP, filter, and control-system design and analysis, among others. You can output audio data or create color 3-D surfaces, mesh plots, contour plots, scatterplots, and a host of other graphical representations. The software will be available in early 1992, and it runs under X Windows. $2995.

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We’ve applied our minds to the needs of home appliance designers and come up with four new microcontrollers specifically for applications such as hot pot, coffee maker and battery charger. Providing all core functions in a 28-pin package, our 17K microcontrollers are more efficient and more economical than standard chips.

17K microcontrollers also require significantly less programming time. Running in the MS-WINDOWS™ V3.0 environment, our exclusive SIMPLEHOST™ debugger offers full screen and source-level debugging. For even greater speed to market, we provide one-time PROM types for all four microcontrollers.

Instead of going out of your way to design around a standard device, use the microcontrollers that go out of their way to suit your system. For information on the 17K Series, contact NEC today.

<table>
<thead>
<tr>
<th>Device</th>
<th>µPD17134A</th>
<th>µPD17135A</th>
<th>µPD17136A</th>
<th>µPD17137A</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM (bits)</td>
<td>1024 x 16</td>
<td>2048 x 16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM (bits)</td>
<td></td>
<td>112 x 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O port</td>
<td></td>
<td>22 lines (including one input, one sense input and 8 N-ch open-drain lines)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog input</td>
<td>4 channels (usable as port pins)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer</td>
<td>8-bit timer: 2ch Basic interval timer/Watchdog timer: 1ch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial interface</td>
<td>1 channel (usable as a port pin)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stack</td>
<td></td>
<td>5 levels</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-on reset</td>
<td>Provided</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>System clock</td>
<td>RC oscillation</td>
<td>Ceramic oscillation</td>
<td>RC oscillation</td>
<td>Ceramic oscillation</td>
</tr>
<tr>
<td>Instruction execution time</td>
<td>8µs (2MHz)</td>
<td>2µs (8MHz)</td>
<td>8µs (2MHz)</td>
<td>2µs (8MHz)</td>
</tr>
</tbody>
</table>
DC-DC Converter Transformers and Power Inductors

These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

- Operation over ambient temperature range from -55°C to +105°C
- All units are magnetically shielded
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- Transformers have input voltages of 5V, 12V, 24V and 48V. Output voltages to ±00V.
- Transformers can be used for self-saturating or linear switching applications
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The tools acquire data from IEEE-488, VXI, or RS-232C instruments or from the vendor's own plug-in data-acquisition boards. $245 to $4995. National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-9488; (512) 794-0100. Circle No. 381

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Texas Instruments Inc, Information Technology Group, Box 869305, MS 8404, Plano, TX 75086. Phone (900) 836-5236, ext 1400. Circle No. 383


Test tools for software development. Software Testworkes uses an OSF/Motif user interface and runs on X Window System workstations. The software consists of two tool suites: STW/COV is a test-coverage analysis suite, and STW/REG automates software testing. A minimum configuration allows three users. $18,300. Software

Research Inc, 625 Third St, San Francisco, CA 94107. Phone (415) 957-1441. FAX (415) 957-0730. Circle No. 385

Raster-image software. Jetview Plus and Jetview Professional allow you to retrieve, view, and print raster images. Both packages sense a raster file's format before loading the file. Once loaded, you can measure lines and angles or print to output devices that have appropriate drivers. Jetview Professional includes adds such file-manipulation features as de-skewing, rotating, cropping, or file conversion. From $995. Houston Instrument, 8500 Cameron Rd, Austin, TX 78753. Phone (512) 835-0900. Circle No. 386

Localtalk network debugger. Local­peek works like a telephone tap on a Macintosh network to create and analyze network statistics. The software keeps such statistics as network utilization, and evaluates error packets such as cyclic redundancy check/checksum, overruns, underruns, and transmit errors. Decoders within the software allow you to look inside error packets and discern the source of the errors. $495. The AG Group Inc, 2540 Camino Diablo, Suite 202, Walnut Creek, CA 94596. Phone (510) 957-7900. FAX (510) 957-2479. Circle No. 387

Network backup software. Arcserve 4.0 backup and restore package for Novell networks achieves backup speeds of more than 20 Mbytes/minute. Features include automated tape rotation for removing files that you don't use for a specified period of time, and a disaster recovery feature that rebuilds all or part of a network by reading a stored database from the backup tape. DOS-based software, from $295 for five users. Cheyenne Software Inc, 55 Bryant Ave, Roslyn, NY 11576. Phone (516) 484-5110. Circle No. 388

Fortran compiler for System 7. Fortran version 3.0 makes use of the Macintosh System 7 features such as AppleEvents, Publish and Subscribe, aliases, and virtual memory. In addition to optimized code for 68000-based microprocessors and Cray pointers, the software adds such debugging features as heap validity checking, useful error dialogues, and execution window tracing. From $495. Language Systems Corp, 441 Carlisle Dr, Herndon, VA 22070. Phone (703) 478-0181. Circle No. 389

Text continued on pg 204
If you can’t instantly see why our digital/analog DSOs are better than HP or Tek...

<table>
<thead>
<tr>
<th>Feature</th>
<th>Fluke PM 3394</th>
<th>Tek® TDS Series</th>
<th>HP® 545xx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog/Digital Combination</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>Limit Test</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Template Test</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>Analysis Functions Int., Diff., Hist., Filter, FFT</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>FFT</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>4 Channels</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Analog Display</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
</tbody>
</table>

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**CIRCLE NO. 107**

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In Georgia: (404) 279-7377
In Dallas: (214) 480-8345

CIRCLE NO. 109
Abstracting analog information. This 224-pg collection, *The Best of Analog Dialogue*, consists of application articles, tutorials, and problem-solving products judged by readers as the most helpful and useful. The collection, which covers 25 years, is arranged in chronological order and has an index. Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. FAX (617) 821-4273. Circle No. 351


**Instrument Handbook.** *The Monitor & Control Handbook* presents data sheets, illustrations, specifications, and applications for a line of LED and LCD digital panel meters, printers, process monitors, and calibrators. Also included is a summary guide for data-acquisition boards, dc/dc power converters, and other data-conversion products. The 210-pg publication highlights a series of hybrid digital voltmeters in a choice of 30 colors, including red, green, yellow, amber, orange, and blue. Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-5000. FAX (508) 339-6356. Circle No. 352

**Digital-signal-processing databook.** This databook describes DSP products for commercial and military applications and includes application notes. It also summarizes 1- and 2-D filters, multipliers, signal synthesizers, and special-function devices. Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1047; (407) 724-5704. Circle No. 353

**Switching and linear supplies.** The 1992 catalog of power supplies provides specifications, mechanical drawings, and prices for more than 1300 standard power supplies, power systems, and accessories. In addition to the large selection of standard-switching and linear supplies, the 208-pg publication introduces eight product series. Lambda Electronics Inc, 515 Broad Hollow Rd, Melville, NY 11747. Phone (516) 694-4200. Circle No. 354

**Catalog of small-sized pc boards.** The 88-pg *Micro PC Catalog* discusses a line of small pc boards and accessories that operate over an extended temperature range. The book provides technical information and pricing for control and expansion boards, cables, displays, keypads, terminal boards, and other items for configuring a system. Octagon Systems Corp, 6510 W 91 Ave, Westminster, CO 80030. Phone (303) 430-1500. FAX (303) 429-8129. Circle No. 356

**Trimmer capacitor catalog.** This 26-pg catalog describes RF and microwave trimmer capacitors and tuning devices. The capacitor-selection guide provides profiles that show the size of units. The catalog concludes with prototyping kits that let you identify and evaluate products discussed in the publication. Johanson Manufacturing Corp, Rockaway Valley Rd, Boonton, NJ 07005. Phone (201) 334-2676. TWX 710-987-8367. Circle No. 357
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Moduflex switchers form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. These subunits and assembly hardware are pre-approved by safety agencies so that certifications can automatically apply to custom models. Additional advantages include first piece delivery within two weeks and the elimination of engineering costs for qualified "OEM" requirements using stock modules.

FM Series are corrected to produce a 0.99 power factor. The resultant input current waveform is nearly a perfect sine wave compliant to the harmonic requirements of IEC 555-2.

Modular construction permits high volume manufacturing with an outstanding quality level and at competitive cost.

FEATURES

- 0.99 power factor.
- 5 watts per cubic inch.
- 600-2000 watts output.
- 120 kilohertz design.
- TUV/VDE, UL, CSA.
- All outputs:
  - Adjustable
  - Fully regulated
  - Floating
  - Overload and short circuit proof
  - Overvoltage protected
- Standard features include:
  - System inhibit
  - Fan output

MODEL SELECTION

Input modules are available in ratings of 600, 1000, and 2000 watts with corresponding code letters of C, E and G. Refer to Power Code Table.

Output modules are available in ten types ranging in nominal power from 75 to 2000 watts. Refer to Output Code Table for codes and nominal power output.

<table>
<thead>
<tr>
<th>Input Power Codes</th>
<th>Watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>600</td>
</tr>
<tr>
<td>E</td>
<td>1000</td>
</tr>
<tr>
<td>G</td>
<td>2000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Codes</th>
<th>Nominal Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>J</td>
<td>75</td>
</tr>
<tr>
<td>K</td>
<td>150</td>
</tr>
<tr>
<td>G</td>
<td>300</td>
</tr>
<tr>
<td>L</td>
<td>300</td>
</tr>
<tr>
<td>M3</td>
<td>400</td>
</tr>
<tr>
<td>M4</td>
<td>500</td>
</tr>
<tr>
<td>M5</td>
<td>600</td>
</tr>
<tr>
<td>M6</td>
<td>750</td>
</tr>
<tr>
<td>M7</td>
<td>1000</td>
</tr>
<tr>
<td>M9</td>
<td>2000</td>
</tr>
</tbody>
</table>

The Table of Ratings for the various types of output modules lists the maximum current for each type as a function of corresponding voltage rating.

Ratings in the shaded area are Preferred and are stocked for fast delivery.

Note: When computing output load power, multiply the fraction of actual current to max. rated current by the nominal power rating of the output module.

RATINGS OF OUTPUT MODULES

<table>
<thead>
<tr>
<th>Nominal Power</th>
<th>75W</th>
<th>150W</th>
<th>300W</th>
<th>400W</th>
<th>500W</th>
<th>600W</th>
<th>750W</th>
<th>1000W</th>
<th>1500W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Volts</td>
<td>J</td>
<td>K</td>
<td>G</td>
<td>L</td>
<td>M3</td>
<td>M4</td>
<td>M5</td>
<td>M6</td>
<td>M7</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>150</td>
<td>200</td>
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<tr>
<td>1</td>
<td>3.3</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>150</td>
<td>200</td>
</tr>
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<td>2</td>
<td>5</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>150</td>
<td>200</td>
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<tr>
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<td>12</td>
<td>20</td>
<td>24</td>
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<td>50</td>
<td>62</td>
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<td>31</td>
</tr>
<tr>
<td>7</td>
<td>28</td>
<td>2.5</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>14</td>
<td>18</td>
<td>21</td>
<td>27</td>
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<tr>
<td>8</td>
<td>36</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>8</td>
<td>11</td>
<td>14</td>
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<td>9</td>
<td>48</td>
<td>1.5</td>
<td>3</td>
<td>6</td>
<td>6</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>16</td>
</tr>
</tbody>
</table>

HOW TO ORDER

Select the letter F for power factor correction, then select the letter M to designate the series. Choose the desired configuration of output modules and list the configuration code. Insert the power code letter and follow with the output code numbers for each individual output. Enter a dash and from the option table insert the sum of the option codes. See example below.

<table>
<thead>
<tr>
<th>OPTIONS</th>
<th>Option Code</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Power Fail Monitor</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Cover (600W only)</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>End Fan Cover (600W only)</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>Top Fan Cover (600W only)</td>
</tr>
</tbody>
</table>
SPECIFICATIONS

**INPUT**
90-264 VAC, 47-63 Hz.
190-264 for 2000W units.

**POWER FACTOR**
0.99 at full load.

**HARMONIC CURRENTS**
Compliant to IEC 555-2.

**INPUT SURGE**
230 VAC - 75A max.
115 VAC - 40A max.

**HOLDUP TIME**
20 milliseconds from loss of AC power.

**OUTPUTS**
See model selection table.

**ADJUSTABILITY**
±5% trim adjustment.

**OUTPUT POLARITY**
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

**LINE REGULATION**
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

**LOAD REGULATION**
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

**MINIMUM LOAD**
Main output requires a 10% minimum load for full output from auxiliaries. Main output is #1 on 600W and 1000W units and #2 on 2000W units.

**REMOTE SENSING**
On all outputs except type J modules.

**RIPPLE & NOISE**
1% or 100mV pk-pk, 20 MHz bandwidth.

**OPERATING TEMPERATURE**
0-70°C. Derate 2.5%/°C above 50°C.

**COOLING**
A min. of 10 LFS cooling air directed on cooling surfaces over the 600W units for full rating. Two test locations on chassis rated for max. temperature of 90°C. 1000W and 2000W models have built-in ball bearing fan.

**TEMPERATURE COEFFICIENT**
±0.02%/°C.

**EFFICIENCY**
70% to 80%.

**SAFETY**
Units meet UL 1950, CSA 22.2 No. 234, IEC 950, EN 60 950, VDE 0804, VDE 0805, VDE 0806. Certifications in process.

**DIELECTRIC WITHSTAND**
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

**SPACING**
8 mm primary to secondary.
4 mm primary to grounded circuits.

**LEAKAGE CURRENT**
3.5mA max.

**EMISSIONS**
Units meet FCC 20780 Part 15 Class A and VDE 0871 Class A for conducted emissions. Compliance with Class B limits by use of additional external filter.

**DYNAMIC RESPONSE**
Peak transient less than ±2% or ±200mV for step load change from 75% to 50% or 100% max. ratings.

**RECOVERY TIME**
Recovery within 1%
M0, M4, M5, M6, M7, and M9 modules - 200 microseconds.

**UNDERVOLTAGE**
Protects against damage for undervoltage operation.

**OVERVOLTAGE PROTECTION**
Standard on all outputs.

**OVERLOAD & SHORT CIRCUIT**
Outputs protected by duty cycle current foldback circuit with automatic recovery. Auxiliaries have additional backup fuse protection.

**THERMAL SHUTDOWN**
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

**SOFT START**
Units have soft start feature to protect critical components.

**FAN OUTPUT**
Nominal 12 VDC @ 12 watts maximum.

**INHIBIT**
TTL compatible system inhibit provided.

**SHOCK**
MIL-STD 810-D Method 516.3, Procedure III.

**VIBRATION**
MIL-STD 810-D Method 514.3, Category 1, Procedure I.

**MECHANICAL**
600W - Case 1. - 2.5 x 5.05 x 12
1000W - Case 2. - 5.05 x 5.05 x 12
2000W - Case 3. - 5.05 x 8 x 12

**POWER FAIL MONITOR**
Optional circuit provides isolated TTL and VME compatible power fail signal providing 4 milliseconds warning before main output drops by 5% after an input failure.

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CIRCLE NO. 52
Sports science and high-tech training equipment have helped our Olympic athletes, but a shortage of funds hinders the program.

JAY FRASER, Associate Editor

Before a rifle or pistol shooter at the US Olympic Training Center pulls the trigger, the coach knows where the bullet will hit the target. Engineers from the Sports Science Division and outside companies have developed a solid-state-laser aiming device that weighs less than two ounces. It's mounted on the gun and directs an infrared beam at the target. A video camera picks up the beam and displays it on a monitor. The coach can determine where the shooter is aiming before the shot is fired.

During bad weather US Olympic rowers train indoors with computerized ergometers. These machines simulate the resistance of water to an oar. They record not only force and stroke rate, but also speed, time, distance, and caloric energy consump-
Sports scientists measure a runner’s oxygen consumption, heart rate, and other physiological indicators.
tion. The ergometers can be connected to a monitor that generates a display of boats racing each other. Some colleges use these devices to stage competitions with other schools in the off-season.

One of the unique facilities at the training center in Colorado Springs, CO, is the swimming flume. It’s the aquatic equivalent of a wind tunnel. Pumps circulate water through the flume, so someone swimming in it remains in place. The speed and temperature of the water can be controlled, and a window on one side allows the swimmer to be observed and videotaped. It’s the only such flume in the US.

The engineers and scientists who work with the US Olympic Team are using sophisticated technical equipment to measure and analyze everything from the angle of a sprinter’s feet to the force of a boxer’s uppercut. The difference between winning and losing in the Olympic Games is sometimes only a fraction of an inch or a fraction of a second. It’s crucial for today’s athletes to find some way to gain an edge over their competitors. Sports science and high technology can often provide that edge.

America was slow to understand the importance of technology to training, but after the 1976 Olympic Games Congress finally realized that the US team needed help. That summer, the Soviet Union finished first overall with 125 medals. America came in second with 94. And tiny East Germany, with a population of only 17 million, almost edged out the US by winning 90.

The success of the Eastern Bloc countries was largely credited to their extensive sports-science programs, which they had begun in the 1950s. Convinced at last of the need for a similar program for US athletes, Congress passed the Amateur Sports Act in 1978. This legislation was far reaching. It made the US Olympic Committee (USOC) solely responsible for the administration, development, and selection of teams for the Pan-American and Olympic Games. It also funded a variety of research grants and established training centers at Lake Placid, NY, and Colorado Springs.

At the Lake Placid center, athletes train for winter sports in addition to boxing, rowing, canoeing, and kayaking. The much larger center at Colorado Springs deals with all other Olympic sports. Its 33-acre campus encompasses dormitories for 600 athletes and coaches, five gymnasiums, a weight room, an outdoor track, a shooting complex, and the water flume. The center also operates a nearby velodrome and roller-skating racing track.

In order for American athletes to receive technological support and services equivalent to those that Eastern Bloc athletes enjoy, a Sports Science Division was established at the Colorado Springs center. It comprises five departments: psychology, physiology, biomechanics, computer science, and engineering and technology. The main purpose of the division is to analyze and evaluate athletes’ performances to help them maximize their efforts.

The engineers and scientists in the Sports Science Division use high-speed video cameras, laser timing systems, and various sensing devices such as ergometers in their work. One of their on-going projects is refining the data-acquisition system they use to monitor an athlete’s aerobic capacity, muscle strength, lung function, and heart rate. From time to time the staff hauls its equipment to Lake Placid to test the athletes there. In 1990 they provided 8640 evaluations for US athletes.

The director of the Engineering and Technology Department is Andrew Zolnay. He studied medicine before he earned his PhD in nuclear engineering from Ohio State Uni-
versity (Columbus, OH). Then he worked at Lawrence Livermore National Laboratory (Livermore, CA) where he designed instrumentation to detect and measure radiation. In his spare time he tinkered with the prototype of a data-acquisition system he had devised for use with athletes.

Zolnay had long been involved in rowing, so his system was specifically designed for that sport, although it could be adapted for others. The basis of the system he envisioned was a series of sensors attached to the athlete and the boat. The sensors would take data every sixtieth of a second and transmit it to a video camera. The data would be encrypted on the video tape to make a correlated record of the image of the athlete with the measurements of his or her performance.

Zolnay organized a team of volunteers at Lawrence Livermore to help him develop his prototype. "I had a reputation for being able to convert more scientists to peaceful purposes than all the demonstrators combined," he says with a smile. He also contacted the USOC and offered the system to them. He received some encouragement, but not much.

Then the head of the Sports Science Division and a colleague took a trip to East Germany to study their athletic programs. When they asked the rowing coach how he trained his teams, he described using a data-acquisition system very similar to Zolnay's. After the two American officials returned to Colorado Springs, they quickly offered Zolnay the directorship of the Engineering and Technology Department. He accepted.

Zolnay feels strongly that the primary purpose of his department isn't to design pieces of hardware. "Engineering's function here is not to build gizmos and widgets for other people," he says, "but to be involved in the actual analysis of sport from the viewpoint of rigorous engineering discipline. That way you get answers to some of the puzzling problems that occur in sport, rather than thinking that the only thing that wins medals is team spirit or some other nebulous concept."

Soon after he arrived at the Colorado Springs center, Zolnay had a chance to apply some engineering thinking and optimization theory to a training situation. "I went down to weightlifting, and a biomechanist was taking 3-D video photographs of the athletes as they lifted and was digitizing the trajectory of the bar. The staff then compared the trajectories to those of medal-winning weightlifters and tried to duplicate them. I told him that even if you duplicate the trajectories of successful weightlifters perfectly, at best you're only going to be as good as the person you're duplicating. And the idea in the Olympics is not to be "as good as" but to be better.

"You have to calculate the optimum trajectory for each athlete," Zolnay explains. "You have to take into account the body dimensions, muscle strengths, linkages, and bone dimensions and sizes of each individual. Then you can say that for this particular athlete, this is the optimum."

Intermingling disciplines

The functions of the departments within the Sports Science Division often overlap and intermingle. Tanya Wheeler, head of the Computer Science Department, says, "We're very much integrated. My department works closely with the others. We find out what they need, and we try to design software that lets the engineers optimize their use of the equipment." Wheeler's background reflects the integration of the disciplines. She holds degrees in both sports science and computer science from the University of Western Ontario.

Because its needs are so specialized, the Computer Science Department can't buy much software off the shelf. Wheeler and her staff have written almost all the pro-

For biomechanical analysis, a runner with markers attached to her body is videotaped, and a stick figure is generated from the image.
grams the Sports Science Division uses. They even work closely with the psychologists. “We’ve written some applications for statistical analysis to help the psychologists,” says Wheeler. “They maintain a very personal one-on-one level of consultation with the athletes, but we provide an avenue for them to get some of the basic information they need.”

When an athlete arrives at the Colorado Springs training center, the first step in the testing and evaluation process is usually a lengthy interview with someone on the Sports Science staff. “I listen carefully to all aspects of their performance as they see it,” says Zolnay. “An athlete’s sense of what’s going on is more sensitive than anything I can ever build.”

The athlete may get a physical and dental exam, advice about nutrition, and psychological counseling. The athlete also goes through a series of laboratory and field exercise tests to measure his or her respiration, heart rate, power, and efficiency. One of the methods the engineers and scientists of the Sports Science Division use to evaluate an athlete’s performance is to create computerized representations of the athlete’s movements.

To analyze a runner’s style, markers are placed on his head, shoulder, hip, knees, and feet. As he runs on a treadmill, he is videotaped with a high-speed camera. The image is digitized and a computer program connects the dots corresponding to the markers to generate a stick figure for display. The figure can be run in slow motion or stopped for closer examination.

The stick figure may reveal aspects of an athlete’s movements that aren’t readily apparent. Correcting flaws will improve performance and reduce the risk of injuries. For example, Mark Fenton, an Olympic race walker, was videotaped, and his computer image showed that his stride was too long. By shortening it slightly to keep his feet closer to his center of gravity, he improved his time in the 20-km race by approximately 5%.

After the tests are finished, people from departments other than engineering and technology might be called in to help evaluate the results. When the evaluation is complete, a sports scientist will sit down with the athlete and coach and suggest how they could improve their training program. Then they return home. Few athletes stay at the Colorado Springs center for an extended length of time.

Both Zolnay and Wheeler are reluctant to claim credit for any athlete’s success because so many factors besides input from the Sports Science Division are involved. But some athletes have shown dramatic improvement after visiting the Colorado Springs center.

“There are some specific instances of athletes who have come through here and improved by leaps and bounds,” says Wheeler. “We hope we can say we were a small part of that improvement. For example, with some of the figure-skating athletes we’ve been able to determine that they have so much angular acceleration going into a jump that they should be able to rotate four or five times before they land. When we tell them that they might say, okay, maybe I’ll try it. Then they try it and do it. We were able to provide a little bit of information that helped them, but it’s their success. They’re the ones who worked for it.”

The annual budget for the Sports Science Division is less than $2 million. Although Congress established the USOC, it doesn’t fund it. No tax money goes to support the US Olympic team.

The USOC raises some funds by licensing the Olympic symbols to companies for use on their products. The companies pay royalties to the USOC on sales. The USOC also has 40 corporate sponsors, firms that make donations of either cash or equipment. (The amount of the donation necessary to qualify as a corporate sponsor is confidential.) Otherwise, America’s Olympic effort depends on donations from individuals.

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pitifully underfunded," says Zolnay. "I have less staff and re­sources here than I had with the volunteers back at Lawrence Liver­more. This is ludicrous." Right now the entire engineering and technol­ogy department consists of him, a senior design engineer, and "two thirds of a research assistant."

Asked what the USOC would need to bring the American effort in sports science up to that of other countries, Zolnay quickly replies, “Fifty million dollars to build a 5­story sports science building, an en­tire floor for each discipline of the division, along with the instrumen­tation required to do a first-class analysis, and the appropriate staff.”

Today a total of 28 people work full time for the Sports Science Division. By contrast, the Soviet Olympic team is supported by a staff of more than 1800. Before Ger­many’s reunification, the East Ger­man team had more than 500 people working with it.

The USOC’s budget constraints are almost certain to create prob­lems in the future. Because the Sports Science staff is so small, it only has the time and resources to work with America’s elite athletes. The younger, developing athletes may not get the level of training they’ll need to compete successfully someday against world-class ath­letes from other countries.

Underlying the immediate prob­lems of lack of funding and person­nel is the deeper problem of lack of national commitment. “It’s just an excuse when people from the US say other countries do much better because they pay their athletes,” says Zolnay. “We have the re­sources here, but they’re squan­dered. Things like facilities and training, diet and nutrition, techni­cal support, and respect for sport all have to come together. We just don’t have the discipline to use what we have. It’s sad.”

(Since this article was written, Andrew Zolnay has left his position with the USOC by mutual consent.)
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Manage a software engineering team already involved in the design, development and implementation of software requirements for cluster tool systems.

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ASIC—application-specific integrated circuit
ATE—automatic test equipment
ATPG—automatic test-pattern generator
BILBO—built-in logic-block observer
BIST—built-in self test
CAE—computer-aided engineering
CD—compact disc
CMOS—complementary metal-oxide semiconductor
CMRR—common-mode rejection ratio
DAC—digital-to-analog converter
dFT—design for test
DMM—digital multimeter
DUT—device under test
ECL—emitter-coupled logic
EC—European Community (Belgium, Denmark,
France, Germany, Greece, Ireland, Italy, Luxembourg,
The Netherlands, Portugal, Spain, and the UK)
EDIF—Electronic Design Interchange Format
EFTA—European Free Trade Association (Austria,
Finland, Iceland, Norway, Sweden, and Switzerland)
FFT—fast Fourier transform
FPGA—field-programmable gate array
HDL—hardware description language
JFET—junction field-effect transistor
JTAG—Joint Test Action Group
NRE—nonrecurring engineering
PECL—positive emitter-coupled logic; referenced to 5V
PLA—programmable logic array
PLD—programmable logic device
PLL—phase-locked loop
rms—root-mean-square
SMT—surface-mount technology
SMU—source-measure unit; four instruments in one:
a voltage source, a voltmeter, a current source, and a
current meter
THD—total harmonic distortion
TPG—test-pattern generator
TTL—transistor-transistor logic
VCO—voltage-controlled oscillator
VHDL—VHSIC Hardware Description Language
VHSIC—very-high-speed integrated circuit

This list includes acronyms and abbreviations found in EDN's Special Report, Technology Updates, and feature articles.
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Book and software unravel the intricacies of the chaos theory

In James Gleick's book Chaos: Making a New Science, he tells a story about quantum physicist Werner Heisenberg. On his deathbed, Heisenberg declared that he would have two questions for God: Why relativity and why turbulence. He said, "I really think He may have an answer to the first question."

Chaos theory may not answer the second question, but it does offer a way to model the behavior of non-linear systems, in which quantities vary over time or change from place to place in a manner that is not strictly proportional. The equations for such systems generally cannot be solved or added together. These equations model the real world—instead of idealizing it—by including nasty non-linear variables such as friction.

In such seemingly random systems as the weather, the swinging of a pendulum, the fluctuations in wildlife populations, and even the bobbling of stock prices and the dripping of a faucet, researchers have discovered patterns. Universal laws appear to be buried in what scientists once viewed as turbulence and disorder—an impenetrable quality of the real world.

Science writer Gleick worked with Autodesk to create James Gleick's Chaos: The Software, a series of six interactive programs that bring to life the relationships he described in his best-selling book.

Computers played a crucial role in the founding of the science of chaos. Instead of merely speeding problem solving, scientists used computers as tools—much as biologists use microscopes and engineers use oscilloscopes—to explore the graphical landscapes generated by seemingly simple equations.

The programs in this package are fully realized versions of the programs that gave rise to the most important discoveries of the science of chaos. The six programs are the Mandelbrot sets, magnets and...
conditions may throw the system off into a different region.

One drawback to this software package is that it’s slow. To draw an image, the program paints the screen four times going from a coarse to an increasingly fine resolution. On my coprocessor-less 286-based computer, the first screen takes about 9 sec, the second 25 sec, the third 1 minute and 25 sec, and the fourth almost 6 minutes. However, you don’t have to wait for the program to finish an image before you make a change to that image or start a new one.

Chaos runs on IBM PC/XT, PC/AT, PS/2, and compatible computers that have an EGA or VGA display and 640 kbytes of memory. Autodesk recommends a math coprocessor, although one is not required. The software package includes the illustrated 238-pg manual, 5½- and 3½-in. program disks, and quick-reference cards.

—Julie Anne Schofield


Finding a map and a compass for leaders and managers

Author Stephen R Covey has taken the ideas from his book The Seven Habits of Highly Effective People and applied them to the arts of leadership and management in an excellent book, Principle-Centered Leadership. Covey’s approach is fundamental. He is more concerned with character than personality, with principles than practices. Covey writes: “Practices are the what to do’s, ... Principles are the why to do’s.”

If you’re looking for a map to guide you across the managerial terrain, Covey refuses to provide one for you. Business terrains change daily, making maps quickly obsolete. However, if you’re looking for a metaphysical compass with which to lead your people, you’ll find one in this book. That compass is constructed from Covey’s seven habits, which urge you to be principle-centered instead of procedure-centered; procedures can change but fundamental principles won’t.

Skeptics may immediately see the potential flaw in this reasoning: people have different ideas about what constitutes a fundamental principle. Covey notes, however, that certain fundamentals are shared by all. These principles include fairness, equity, justice, integrity, honesty, and trust. Few could argue the point. Who wouldn’t like to work at a company governed by these principles?

Such a world sounds utopian, though. At first glance, aligning the corporate world with the true North of fundamental principles sounds impossible and that may well be the case. Instead, Covey urges you to make these principles work at your company by internalizing and living them yourself.

Many people feel that things would be great if only that bozo over there or those clowns in that other department would shape up. Covey’s philosophy won’t let you off the hook that easily. You can always choose your response to any situation, and your choice should be based on these fundamental principles, not emotions or unthinking adherence to procedures. At a stroke, Covey puts you at the center of all of your problems and makes you the sole solution. His ideas are at the very least thought-provoking.

Unfortunately, the book is not without flaws. It sometimes resembles a patchwork because several of its chapters were created by contributing authors. The topics ramble from you, to business, to your family, and then to educational institutions. One chapter in the book seems to be little more than an advertisement for the Covey Leadership Center; it talks about who the center has worked with but says nothing about what was done.

In addition, small offers appear at the bottom of several pages in the book, urging you to call a toll-free number to obtain free worksheets or audio cassettes. I wish that those worksheets had been included in the book, perhaps in appendices. I can only conclude that Covey took this approach to obtain names for his newsletter’s and leadership center’s mailing lists. The offers are free so the inconvenience isn’t great. Even so, I liked the book.—Steven H Leibson


What should we get our hands on?

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