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Special Report: Achieve blazing data transit with FDDI pg 88
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SPECIAL REPORT

FDDI stations 88

Increasing network demands are straining the throughput of first-generation LANs. To meet high-performance requirements, network designers are starting to adopt the 100-Mbps Fiber Distributed Data Interface (FDDI). Unfortunately, FDDI stations don't come cheap.—John Gallant, Associate Editor

DESIGN FEATURE

EDN’s DSP-chip directory 104

The tools needed to develop applications that use digital signal processing (DSP) continue to improve. Now, a choice of operating systems and interfaces to host operating systems is making DSP available to more applications.—David Shear, Contributing Editor

TECHNOLOGY UPDATES

SCPI instruments will ease ATE development 39

Engineers who want to minimize test-system development time and maximize system flexibility should use SCPI instruments whenever possible.—Maury Wright, Regional Editor

Serial EEPROMs: Serial memory offers cheap frills 57

You don't need a byte-wide interface or large devices to add a little nonvolatile memory to your system. Serial EEPROMs are an inexpensive option that offer a few extras.

—Richard A Quinnell, Regional Editor

Continued on page 7
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Today’s programming systems don’t take advantage of engineers’ inherent spatial-reasoning abilities.

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Ask for literature package M14A013.
VME BOARD TOPS 1.1 BOPS PERFORMANCE

A single V-C40 VME board from Ariel Corp sets a VME peak-performance mark—as much as 1.1 billion operations per second (BOPS). Additionally, it can move data at rates as high as 1.3 Gbytes/sec. The 6U VME board holds as many as four TI TM320C40 32-bit floating-point DSP processors along with as much as 64 Mbytes of local dynamic RAM, and 8 Mbytes of static RAM (2 Mbytes per CPU). You can hook up processors and multiple boards in a number of multiprocessing configurations. Each board has six special byte-wide DMA communications ports, three of which are brought off board for 12 communications links, each capable of moving 20 Mbytes/sec. The board has a proprietary 24-bit bus for linking to analog converter cards. The board functions as both a VME bus master and slave and costs $20 per million operations. Ariel Corp, Highland Park, NJ, (908) 249-2900, FAX (908) 249-2123.—Ray Weiss

PALM-SIZE INDUSTRIAL PC OPERATES FROM –40 TO +85°C

Suitable for use in rugged environments that present extreme temperatures, the 5012 Micro PC needs no keyboard, monitor, or disk drives to operate. With DOS embedded in its ROM, this computer includes two 512-kbyte solid-state data-storage locations that you can populate with RAM and EPROM. Housed on a pcb-board, the computer comes with a built-in EPROM programmer, 1 Mbyte of dynamic RAM that you can expand to 2 Mbytes, a watchdog timer, battery backup for RAM, and a battery-backed calendar/clock. This board also contains ports for a printer, a keyboard, a speaker, and two serial ports. The basic board costs $495, and you can order enclosures starting at $45. Octagon Systems Corp, Westminster, CO, (303) 430-1500, FAX (303) 426-8126.—J D Mosley

MULTIPLY-ACCUMULATE UNIT ENHANCES SERVO CONTROLLER

An embedded multiply-and-accumulate unit (MAU) highlights a range of features of the HPC46100 16-bit microcontroller from National Semiconductor. Running off a 40-MHz system clock, the MAU provides 32-bit results from 16-bit, signed-integer multiply-and-accumulate operations in 400 nsec. Peripheral functions such as an 8-bit ADC with 6-µsec conversion, three independent timers with separate frequency- and duty-cycle control registers, a programmable UART, and 1 kbyte of onboard RAM tailor the microcontroller to such embedded servo applications as found in automotive-chassis and hard-disk drive control. The ADCs convert as many as eight single-ended channels or four differential-channel pairs. You can trigger the converters for single readings, or you can perform these operations continuously. Eight dedicated registers let you store single-channel data for average reading calculations. The onboard UART can operate in synchronous or asynchronous modes and offers multiple character widths and stop bits, status reporting, error detection, an addressing mode, and diagnostic testing. The µC is upward-source-code-compatible with the HPC family of controllers and includes such other features as watchdog logic, vectored interrupts, and HALT and IDLE power-down modes. Available development tools for the $23 (1000), 14 x 14-mm, 80-pin device include a development system, serial hook hardware, logic-analyzer interface board, HP logic-analyzer disassembler, and cross-development system. The device comes in a plastic quad flatpack. National Semiconductor, Santa Clara, CA, (408) 721-5185.—Michael C Markowitz
COLOR PANEL-MOUNT DISPLAY INCLUDES 80386SX PC

Computer Dynamics's Color Displaypac includes an IBM PC-compatible 80386SX single-board computer and a color LCD with infrared touch screen in a panel-mount package. The integrated package measures 11.5 x 8.5 x 2 in., and the display screen is 10.4 in. wide. The display provides VGA color graphics and includes a fluorescent backlight. The single-board computer includes as much as 4 Mbytes of dynamic RAM, two RS-232C serial ports, keyboard and printer ports, and hard- and floppy-disk interfaces. The computer can boot MS-DOS from an onboard RAM/ROM disk. A configuration with 1 Mbyte of memory and a 16-MHz µP costs $6174. Computer Dynamics, Greer, SC, (803) 877-8700, FAX (803) 879-2030.—Maury Wright

MPLD COMBINES AS MANY AS 40 ALTERA EPLDs

Altera's Mask-Programmable Logic Device (MPLD) can replace as many as 40 of the company's erasable programmable logic devices (EPLDs) or up to 700 of its macro cells. Offered as a synthesis service, the company will take EPLD designs at the netlist level and synthesize them into a single mask-programmed device. The company guarantees results from working designs using EPLD circuits, letting engineers prototype, and even put out as initial products, EPLD-based designs. For size reduction, they can then have the design reduced to a single, foundry-programmed mask-based chip. The conversion process is automated and the company will guarantee layout timing as well as 95%—or better—fault coverage for supplied test vectors. Prototypes will be delivered within 6 weeks of receipt of the design. The cost is $0.06 per macro cell for production units; $20,000 to $60,000 for design conversions (NRE). Production units are delivered within 10 to 12 weeks. Initially, Classic and MAX 5000 EPLDs are covered, with MAX 700 devices added by the fourth quarter of 1991. Altera Corp, San Jose, CA, (408) 984-2800, FAX (408) 435-1394.—Ray Weiss

SOLID-STATE RELAYS SUIT LOW-CURRENT APPLICATIONS

The LH1500 family of <1A solid-state relays from AT&T Microelectronics each comprise a photodiode array, various switch control circuits, and DMOS switches. The relays use an LED for actuation control and an IC for the switch output. The family consists of 21 products, ranging in price from $1.25 to $4.75 (1000) and includes all the common switch forms: normally open, normally closed, and combinations of each. Each relay features 3750V of isolation, thereby meeting European standards and exceeding US standards. The relays are constructed on a dielectrically isolated process, which provides for breakdown voltages between 140 and 440V. Typical on-resistance varies from 2 to 23Ω. Special features of some of the relays include current limiting, make-before-break switching, and dual packaging. The relays come in either 6- or 8-pin DIPs or surface-mount gull-wing packages. Sample quantities are available now; production quantities will be available by the fourth quarter of 1991. AT&T Microelectronics, Allentown, PA, (800) 372-2447.—Anne Watson Swager

CMOS PLDs ACHIEVE 7.5-NSEC SPEED

Intel Corp's faster versions of its $10 85C244 24-pin and $6.10 (1000) 85C220 20-pin PLDs have programmable I/O structures, letting them emulate a variety of 20- and 24-pin PLD architectures. They have a 7.5-nsec input-to-output propagation delay and support clock frequencies as great as 74 MHz using external feedback. The parts consume 105 mA at maximum operating frequency and come in plastic leaded chip carriers. Intel Corp, Santa Clara, CA, contact local sales office.—Richard A Quinnell
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EDN October 1, 1991
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Juggling equation for better solution

Just as my subscription to EDN is reinstated, Peter Anderson shock
me with the equation on pg 31 of EDN (May 23, 1991), [which uses N to characterize a triode]. For example, the dual triodes 12AU7, 12BH7, and 5687 all have values of a \( \mu \) of 20, but only one may work properly in a circuit.

The value of \( \mu \) is the ratio of \( g_m \cdot MDSU / \cdot MDNM / to g_p \). You can double \( g_m \) and \( g_p \) or halve \( r_p \) by doubling the plate current, and the \( \mu \) is unchanged.

The point is that using the small-signal equation

\[ I_p = g_m V_g + g_p V_p, \]

where \( I_p \) is plate-current change and \( V_g \) and \( V_p \) are voltage changes, [would make a better basis for a Spice model.] The equation is related to the equation noted by Peter Anderson, but expresses the operating characteristics of a tube, a bipolar, or a FET device in a much more useful form. The above equation expresses the way we have to operate a [tube,] anyway. We set the plate current, then adjust the bias voltage with degeneration as needed to give that plate current.

Keats A Pullen Jr, PE
Kingsville, MD

Engineer should look for higher paying job

The author of the letter "Engineers' salaries should be professional" (EDN, March 14, 1991, pg 26) suggests that, as a member of the engineering profession, he ought, by that very fact, to be paid a commensurate salary.

The thought is very lofty, but the fact of the matter is that salaries, like most economic matters, are ultimately a question of supply and demand. I really can't imagine a doctor or a lawyer saying, "Gee, guys, I'm a professional. You ought to pay me more."

EDN October 1, 1991
How Fast Is A Flash?
A Direct Comparison

<table>
<thead>
<tr>
<th>Density</th>
<th>AMD</th>
<th>Fastest Competitor</th>
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</thead>
<tbody>
<tr>
<td>256K</td>
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<td>120ns</td>
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<tr>
<td>512K</td>
<td>90ns</td>
<td>120ns</td>
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<tr>
<td>1 Mbit</td>
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<td>120ns</td>
</tr>
<tr>
<td>2 Mbit</td>
<td>90ns</td>
<td>150ns</td>
</tr>
</tbody>
</table>

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications. Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

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National’s Linear Circuit

<table>
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<th>Location</th>
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<tbody>
<tr>
<td>Sept. 25</td>
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<td>Oct. 22</td>
<td>Houston, TX</td>
</tr>
</tbody>
</table>

Visa and Mastercard accepted.
Little known or appreciated outside the world of tool and die makers, machine tools were nevertheless crucial to industrial development. Now, engineering software assumes the crucial role of the machine tool of the next industrial revolution.

Engineering software is too important and too different from ordinary software to be left solely to programmers. Give a carpenter a problem, and he thinks of solving it with hammers and nails. Give a programmer a problem, and he thinks of solving it with written-out lines of code. Unfortunately, engineers do not think or express themselves in terms of language. Instead, they use visual symbols.

Although we associate programming with text files, that association is not a fundamental given. In reality, programmers' fixation on text is an artifact of the teletypewriter output of early computers. Today, textual programming is no longer mandatory; even inexpensive computers can handle complex graphics and symbols. Few good software tools take advantage of these capabilities to let engineers construct programs visually.

Proponents of textual ASIC and FPGA software tools say that the increasing complexity of today's devices is forcing engineers to abandon diagrammatic systems for textual ones. This false imperative rests on an unproven foundation. Text is not inherently more comprehensible, lucid, compact, and rigorous than diagrams are. Few developers seem to consider the possibility that more complex devices may lead to more powerful diagrammatic design systems.

Good engineers are in the 99th percentile for spatial ability, and good programmers are in the 99th percentile for linguistic ability. Thus, we often find software kluges masquerading as tools that let users mix textual and diagrammatic design. Such tools best suit designers who are exceptional in both spatial and linguistic areas, and not enough such people are available to do all the engineering that needs to be done.

Therefore, everyone who has a hand in developing software tools for engineers should become familiar with Harvard researcher Howard Gardner's Theory of Multiple Intelligences. Gardner has written several popular books on the subject, and his theories provide the scientific underpinning for the notion that engineers need visual—not textual—design tools. Engineering-tool companies need to research the mental activity of creative engineers and then develop new visual metaphors that support the ways engineers think.

References


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<table>
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<tr>
<th>Model</th>
<th>Speed (ns)</th>
<th>Packaging</th>
<th>Data Retention</th>
<th>Special Features</th>
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L = Low  LL = Low,Low  B = 3 Volt  X = Extended Temperature

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Engineers who want to minimize test-system development time and maximize system flexibility should use SCPI instruments whenever possible.

Maury Wright, Regional Editor

The SCPI (Standard Commands for Programmable Instruments, pronounced "skippy") standard promises to simplify the programming of automatic test systems. Companies complying with the standard will ensure that similar instruments from different manufacturers have similar command languages. Thus, a programmer would need to learn how to program a voltmeter, frequency counter, or other instrument only once.

Most major instrument makers plan to use SCPI in all their new products. SCPI-compatible GPIB (General-Purpose Instrument Bus) and VXIbus test instruments have started to ship, but most types of SCPI instruments are still scarce. If you can find a SCPI version of a test instrument that you need now, buy it. SCPI compliance should be a determining factor when you choose instruments for a test system, and SCPI products cost the same as their non-SCPI counterparts.

The SCPI standard defines an extensible command language for the remote control of instruments. The language was developed independently of the front-panel terminology specific to individual instruments. The language uses a consistent style and English-like mnemonics, both of which make the language readable and easy to use. For example, the following command will read the dc voltage from any SCPI instrument that can measure voltage:

MEASure:VOLTage:DC?

The language’s keywords can be written out in full or abbreviated to the 3- or 4-character strings indicated by the capital letters. Strings of keywords make up SCPI commands.

The creators of the SCPI standard sought to develop a language that offered what they termed vertical, horizontal, and functional compatibility. Vertical compatibility means that two instruments of the same generic instrument type, such as two digital oscilloscopes from different manufacturers, will have compatible command sets. A single software driver could control either instrument.

Horizontal compatibility refers to a situation in which two different types of instruments can perform the same measurement. For example, both frequency counters and digital oscilloscopes can measure the frequency of a signal. The horizontal-compatibility goal mandates that the same frequency-measurement command will properly investigate a frequency measurement in either type of instrument.

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<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>PROPAGATION DELAY (Max)</th>
<th>OUTPUT ENABLE (Max)</th>
<th>OUTPUT DISABLE (Max)</th>
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<td>5.2ns</td>
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<tr>
<td>Transceivers</td>
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<tr>
<td>Latches</td>
<td>4.2ns</td>
<td>5.5ns</td>
<td>5.0ns</td>
</tr>
</tbody>
</table>

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The SCPI standard

compatibility of specific features in different types of instruments. For example, the same frequency and sweep commands can control a spectrum analyzer and a RF source because both types of instruments can sweep in frequency.

SCPI allows instrument updates

Designers who use SCPI-compatible instruments exclusively will realize several benefits. First, updating an ATE (automatic-test-equipment) system with the best voltmeter available will require minimal changes in system and test software. Second, the time required to develop software for new ATE systems should drop because SCPI leads to reusable code. Third, programmers will be more efficient when using SCPI instruments because of the three types of compatibility and the fact that the language is easy to read and consistent in style.

SCPI poses no larger challenge to the first-time user than do the one-of-a-kind command sets currently common in instruments. Senior Electronics Engineer Mike Hanus of Sundstrand Power Systems (San Diego, CA) recently worked with a SCPI instrument for the first time. Hanus replaced a test set's programmable power source with a SCPI version. He reports that the software driver for the new source took no longer to write than did the original driver and that he wouldn't have had to write a new driver had the first source been SCPI compatible. Hanus says the experience has prompted him to write more modular code with the goal of reusing portions of his code for SCPI-compatible instruments.

Table 1—INPut subsystem commands

<table>
<thead>
<tr>
<th>Keyword</th>
<th>Parameter form</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPut</td>
<td>&lt; numeric_value &gt;</td>
</tr>
<tr>
<td>:ATTenuation</td>
<td>&lt; Boolean &gt; ONCE</td>
</tr>
<tr>
<td>:AUTO</td>
<td>AC:DC</td>
</tr>
<tr>
<td>:COUPLing</td>
<td>&lt; numeric_value &gt;</td>
</tr>
<tr>
<td>:FILTER</td>
<td>&lt; Boolean &gt;</td>
</tr>
<tr>
<td>[:LPAS]</td>
<td>&lt; numeric_value &gt;</td>
</tr>
<tr>
<td>[:STATE]</td>
<td>&lt; Boolean &gt;</td>
</tr>
<tr>
<td>:FREQquency</td>
<td>&lt; numeric_value &gt;</td>
</tr>
<tr>
<td>:HPASt</td>
<td>&lt; Boolean &gt; ONCE</td>
</tr>
<tr>
<td>[:STATE]</td>
<td>&lt; numeric_value &gt;</td>
</tr>
<tr>
<td>:FREQquency</td>
<td>&lt; numeric_value &gt;</td>
</tr>
<tr>
<td>:GAIN</td>
<td>&lt; Boolean &gt;</td>
</tr>
<tr>
<td>:GUArd</td>
<td>LOW/FLOAT</td>
</tr>
<tr>
<td>:IMPedance</td>
<td>&lt; numeric_value &gt; FLOAT/GROUND</td>
</tr>
<tr>
<td>:LOW [:STATE]</td>
<td>&lt; Boolean &gt;</td>
</tr>
</tbody>
</table>

The SCPI standard is independent of any physical interconnection specification. You will most often hear the term SCPI associated with VXIbus-based instruments and instruments that use the GPIB defined by the IEEE-488.1 specification. But SCPI works equally well on instruments connected to a controller via an RS-232C serial interface or any other interface.

Although the SCPI standard doesn't specify a physical interface, it does mandate the use of features defined in the IEEE-488.2 specification. The IEEE-488.2 standard defines controller functions, data formats, and status reporting—basically a common set of housekeeping commands for instruments. (See Ref 1 for more information on the IEEE-488.2 specification.)

Alan Hoffman, director of engineering at IOtech, points out that SCPI offers a way for manufacturers to standardize the commands used for board-level PC instruments. IOtech offers a line of GPIB controller cards for IBM PCs. The Power488 and Power488CT cards also feature SCPI-compatible test-and-measurement capabilities. The
The SCPI standard

Power488 costs $495 and includes 40 digital I/O lines in addition to the GPIB controller and driver software. The $595 Power488CT adds counter/timer features.

SCPI’s creators based the language on the generic instrument model in Fig 1 (see box, “SCPI Consortium controls standard,” for a history of SCPI’s creation). The SCPI standard defines a tree-like structure that has more than 20 major subsystems as the main branches. The squares in Fig 1 correspond to major subsystems of the SCPI language. Additional major subsystems handle special instrument capabilities such as calibration and diagnostics. The box, “Major SCPI subsystems,” lists the major command subsystems.

Look at Table 1 for a sample of a SCPI command subsystem taken directly from the specification. The INPut command lets you program the conditioning an instrument applies to an incoming signal. Keywords in square brackets indicate default paths through the SCPI tree structure. A program can use one or more of the command options for the instrument in use.

Instruments don’t need to implement commands from every SCPI subsystem. Instrument designers can choose the subsystems they

---

**SCPI Consortium controls standard**

A consortium of leading test-and-measurement instrument vendors defined SCPI and still controls the evolution of the standard. The consortium considers the standard to be “free and open”—any test equipment manufacturer can use SCPI commands in an instrument free of charge. The consortium continues to add to the SCPI standard to account for additional types of programmable instruments.

Customer demand led to the creation of SCPI. Sophisticated customers recognized that the time test programmers spent writing drivers for each new incompatible instrument was wasted. Hewlett-Packard reacted to the need for standardization among its varied instruments by creating its Test and Measurement Systems Language (TMSL), which the company introduced in August 1989. Simultaneously, a group of instrument vendors was contemplating a similar project. And for once in this intensively competitive electronics industry, the best possible thing happened. Hewlett-Packard contributed its TMSL work and joined the group of companies that went on to form the SCPI Consortium.

The consortium refined Hewlett-Packard’s work and added capabilities. Tektronix contributed its Analog Data Interchange Format (ADIF) standard. ADIF provides a standard way to store analog data such as waveforms. In addition, ADIF includes environmental data such as scaling information, instrument settings, and time and date stamps.

The consortium moved quickly and published the first version of the SCPI standard in April 1990. The second version was published in June of this year, and the consortium plans to publish an updated spec annually. The consortium meets every two months to discuss proposed additions to the SCPI standard. A private forum on the Compuserve dial-up service includes up-to-date information on proposals, meeting schedules, and newly approved commands.

The founding members of the consortium are Bruel & Kjaer (Naerum, Denmark), John Fluke Mfg Co (Everett, WA), Hewlett-Packard Co (Loveland, CO), Keithley Instruments Inc (Cleveland, OH), National Instruments Corp (Austin, TX), Philips (Almelo, The Netherlands), Racal-Dana (Irvine, CA), Tektronix Inc (Beaverton, OR), and Wavetek Inc (San Diego, CA). The consortium now has more than 20 members.

Any company can join the SCPI Consortium. Sponsor memberships cost $20,000 annually and include one seat on the consortium’s board of directors. A contributing membership costs $5000 annually and includes the right to vote on proposed additions to the standard. Five contributing members are elected to the board of directors each year. The $750 associate membership grants access to the private SCPI Compuserve forum only. SCPI Consortium meetings are open to the public, and anyone can propose additions to the standard.

For more information on SCPI and to buy copies of the standard ($50), contact

Fred Bode
Executive Director
SCPI Consortium
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The SCPI standard

need to control an instrument's features. The SCPI standard requires only that an instrument implement the SYSTem command subsystem.

Joe Mueller, a project manager at Hewlett-Packard and the company's representative to the SCPI Consortium, points out that SCPI allows for 100% control of an instrument's features. A typical instrument might implement 100 to 200 total SCPI commands, according to Mueller. The average user may need no more than a dozen commands to develop a specific test program.

The most frequently used commands are those in the MEASure

### Major SCPI subsystems

The following list describes the major subsystems that make up the main branches of the SCPI tree. The beginning capital letters indicate the subsystem's abbreviated form.

**CALCulate**—The CALCulate subsystem includes commands that control data-processing functions performed on data typically acquired by a SENSe command. For example, a CALCulate command can control the conversion of data from the frequency domain to the time domain.

**CALibration**—Commands in the CALibration subsystem control system-calibration functions.

**DIAGnostic**—The DIAGnostic subsystem includes all the service and diagnostic commands for routine maintenance and repair.

**DISPlay**—Commands in the DISPlay subsystem control the selection and presentation of textual, graphical, and TRACe information.

**FORMat**—The FORMat subsystem commands set the data format for transferring numeric and array information.

**INPut**—INPut subsystem commands control the characteristics, such as the attenuation, of a sensor's input ports.

**INSTrument**—INSTrument subsystem commands are used for instruments, such as a dual-channel power supply, that support multiple logical instruments.

**MEASure**—The MEASure subsystem defines a set of high-level instructions that are used to acquire data. This subsystem includes the most commonly used SCPI commands. The concept of horizontal compatibility defined in the SCPI standard is implemented in the MEASure subsystem.

**MEMory**—The MEMory subsystem commands manage the semiconductor memory instruments use to store various types of data.

**MMEMory**—MMEMory commands manage mass-storage devices, such as disk drives, that are inside instruments or directly connected to instruments.

**OUTPut**—Commands in the OUTPut subsystem control the characteristics of a source’s output port. For example, an OUTPut command can set the output source impedance of a signal.

**PROGram**—The PROGram subsystem commands provide control of one or more user-programmed tasks resident in an instrument.

**ROUTE**—ROUTE subsystem commands control instruments primarily designed to route signals. These commands also control signal routing on instruments that offer routing capability as a front end to input and output ports.

**SENSe**—The SENSe subsystem includes commands that directly set device-specific features before taking a measurement. An example of such a feature is an instrument’s filter bandwidth.

**SOURce**—SOURce subsystem commands set device-specific features, such as modulation controls, on a signal source.

**STATus**—The STATus subsystem commands add status-reporting structures to those defined in IEEE-488.2.

**SYSTem**—The SYSTem subsystem includes the functions not related to instrument performance, such as the characteristics of an instrument's communications interface. This subsystem forms the command base required in all instruments.

**TEST**—The TEST subsystem extends standard instrument self-test procedures beyond those defined in IEEE-488.2.

**TRACe**—Commands in the TRACe subsystem control the definition and manipulation of trace data.

**TRIGger**—The TRIGger subsystem commands serve to synchronize instrument actions with other events.

**UNIT**—The UNIT subsystem provides a way to change the units of measure associated with an instrument feature.

**VXI**—Commands in the VXI subsystem include the administration functions associated with VXIbus-based systems.
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The SCPI standard

subsystem. The MEASure subsystem enjoys special status although it is a major branch on the SCPI tree with the more than 20 other subsystems. The MEASure subsystem implements the horizontal compatibility the SCPI specification defines.

Hewlett-Packard's Mueller offers an example that illustrates the horizontal compatibility SCPI makes possible and the philosophy behind it. He describes the compatibility of an integrating digital voltmeter with a sampling digital voltmeter. A test programmer could use SCPI's capabilities to program the sampling meter to take 4012 samples to measure dc voltage.

A program that commanded the integrating meter to take 4012 samples, however, might receive an error as an answer because the integrating meter doesn't take samples. The instrument designer could be clever and use SCPI to design the integrating meter so that it would take a meaningful measurement after such a request. The SCPI standard doesn't require instrument manufacturers to take such precautions, however.

Mueller suggests a way to write the test program that ensures an accurate measurement from SCPI-compliant instruments. The reason the programmer set the number of samples was to limit the amount and frequency of the ac voltage rejection present in the dc voltage measurement. You could use a higher-level SCPI command to instruct either meter to account for 60-dB rejection at 52 Hz, for example. The instrument would then take the measurement in the best possible way.

The thousands of possible SCPI command combinations will always make exact compatibility of instruments impossible. No two instruments—not even two voltmeters—have the exact same measurement capabilities. But SCPI does provide the means to achieve the vertical, horizontal, and functional compatibility of the specification.

Unfortunately, little evidence now exists that indicates how well SCPI will work in practice. Hewlett-Packard offers a line of VXIbus instruments and a few GPIB instruments that use SCPI. But HP had a head start on the industry because much of SCPI was derived from the company's Test and Measurement System Language (TMSL).

Other companies that now offer SCPI products include the Fluke (Everett, WA) and Phillips (Almelo, The Netherlands) conglomerate. Between these two companies you can buy SCPI-compatible frequency counters, programmable power sources, and signal-switching systems. Finally, Wave­tek, San Diego offers a line of VXIbus instruments for signal generation.

Thus far, the best example of SCPI success can be found in the compatibility between the Wave­tek 1378 Synthesized Sweep/Function Generator ($3295) and Hewlett-Packard's E1440A generator ($5750). The products have a similar
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The SCPI standard

set of signal-generation capabilities and clearly demonstrate vertical compatibility. Bill Lee, Wavetek design engineer and the company’s SCPI Consortium representative, points out that the SCPI standard includes explicit commands that let the companies implement all the desired functions. Thus, the instruments were compatible.

Both Hewlett-Packard and Wavetek also offer VXIbus arbitrary-function generators based on SCPI. The function generators were not compatible at the time of introduction. Both companies found the SCPI standard lacking in a few key areas required to exploit all the capabilities of the instruments. So each company added to the spec in different places and planned to propose the new commands to the SCPI Consortium as formal SCPI changes. Both companies worked on the new commands in secret because neither wanted to disclose features of an unannounced product.

Wavetek engineers added commands to the TRACe subsystem to perform additional waveform functions. Hewlett-Packard engineers added similar capability in the SOURce subsystem. The resulting products were not vertically compatible. Both companies presented their propos-

For more information...

For more information on the SCPI-based products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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als to the committee, and a compromise ensued. Soon you will see revision B instruments from both companies that support the SCPI Consortium-approved compromise. The revision B function generators will be vertically compatible.

You can expect other conflicts to arise because of the competitive nature of the electronics industry and the constant influx of new products with new features. Also, the SCPI standard is admittedly short of commands that can control certain types of instruments, such as logic analyzers.

The SCPI Consortium, however, adds to the standard every two months. The consortium features an unprecedented level of cooperation in such a competitive industry. SCPI seems to be an idea with no drawbacks. Most major instrument vendors plan to use SCPI in all their new products, many of which will be introduced over the next year. Shortly, designers who don’t buy SCPI instruments exclusively will find the price, development time, and extensibility of their test systems lacking compared with SCPI-based systems.

Reference
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<table>
<thead>
<tr>
<th>Model Number</th>
<th>Paper Width</th>
<th>Columns Across</th>
<th>Dots / Inch</th>
<th>Dots / Line</th>
<th>OEM Price</th>
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<tr>
<td>PM1224</td>
<td>2.6 inches</td>
<td>18 to 37</td>
<td>100</td>
<td>224</td>
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<tr>
<td>PM1320</td>
<td>2.6 inches</td>
<td>23 to 58</td>
<td>150</td>
<td>320</td>
<td>$296</td>
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<tr>
<td>PM1416</td>
<td>4.5 inches</td>
<td>29 to 90</td>
<td>100</td>
<td>416</td>
<td>$443</td>
</tr>
</tbody>
</table>

1. This is the 500-piece OEM price. It is subject to change without notice.
2. The maximum number of columns depends on the font and size selected. The higher number is for 8 x 7 characters, approximately 16 characters/in.

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SERIAL EEPROMs

Serial memory offers cheap frills

You don’t need a byte-wide interface or large devices to add a little non-volatile memory to your system. Serial EEPROMs are an inexpensive option that offer a few extras.

Serial EEPROMs provide an opportunity to add nonvolatile memory to your system at very low cost, both in terms of price and system resources. Newer devices also have the ability to protect your data, speed the data-transfer rate, and operate at lower voltages.

As the name implies, you interact with a serial EEPROM by clocking addresses, data, and commands into a single data line. A complete interface requires from two to five wires, depending on the type of device you use. The most common interface type, Microwire (developed by National Semiconductor), uses four lines. Some devices add a status pin to bring the total to five. Alternatively, you can reduce the number of lines needed by tying together the data input and output lines (see box, "Interfacing alternatives"). The Philips interintegrated circuit (I²C) bus, running a close second to Microwire in availability, uses only two lines. Other available interfaces include UART-compatible devices that work with Motorola’s serial-pipeline interface (SPI).

The compact nature of the serial interface is vital if you’re trying to produce a minimal system and still provide nonvolatile memory. For many microcontrollers, the CPU’s address and data buses are not available outside of the IC, in order to conserve I/O pins.

Most microcontrollers offer parallel ports, however, and designers needing off-chip memory use those ports to generate the needed address and data bits. Interfacing to a conventional memory device would consume at least 8 bits of the parallel port, versus the 2 to 5 bits for serial memory. Using a microcontroller with on-chip EEPROM is a possibility, but CPU vendors such as Zilog admit that a 2-chip design is less expensive than a CPU with onboard EEPROM.

In addition to offering a compact interface, the serial EEPROMs themselves are compact. Almost all of them, regardless of their bit density, are available in 8-pin DIPs, and many come in small-outline (SO) packages. The variety of bit densities having a common physical interface gives you the option of changing the amount of memory in...
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Serial EEPROMs

your design to increase capacity or decrease cost without affecting board layout or wiring. If you use devices having the I2C interface, you may not need to change software, either, because the I2C command protocol uses a fixed-length address field.

Nothing in life is free, however, including the serial EEPROM’s advantages. There are a number of design considerations you must confront before deciding to incorporate serial EEPROM in your design. For example, using a serial interface extends the time required for memory access. In addition to the time needed to shift the data in and out, you must include the time to clock in a command code and an address for each transaction. Further, the serial protocols aren’t always amenable to the use of byte-oriented serial peripherals. Therefore, you’ll have software overhead for converting the serial data to parallel, and vice versa. Finally, storing data in an EEPROM requires a considerable amount of time, on the order of 10 msec (Ref 1).

Page mode speeds data storage

Manufacturers of serial EEPROMs have implemented a number of improvements addressing the first of these considerations: access time. Some offer clock rates as fast as 1 MHz, for example, reducing the time required for shifting data out. Manufacturers have also reduced the command and address overhead by giving some of the serial EEPROM the ability to perform both page-oriented write transactions and sequential reads. Devices with the sequential-read capability let you specify a single address, then read all the data between that address and the end of memory without further addressing.

Access time is not the only consideration, however. Serial EEPROMs, like all EEPROMs, have a limited service life. EEPROMs store their data on a floating gate in each memory location. During erasing and writing, charge moves to or from the gate using quantum mechanical tunneling through the surrounding insulators. Each time an EEPROM cell is erased or written to, some electrons may become permanently trapped in the insulator. Over time, these trapped electrons build up enough charge to prevent the cell’s proper operation. Using an EEPROM, therefore, requires careful attention to system design in order to minimize the number of erase/write cycles needed at a given memory location.

Manufacturers specify the lifetime of an EEPROM in terms of endurance: the minimum number of erase/write cycles a cell is guaranteed to provide. Read cycles do not affect a cell’s endurance. As shown in Table 1 (see pg 64), the endurance ratings of available serial EEPROMs range from 10,000 to 1 million cycles. Realize, however, that these are minimums; you may get a much greater lifetime in your application.

Endurance ratings vary

Ratings expressed by different manufacturers aren’t always directly comparable, though, because their test methods differ. The differing conditions result in differing test results. Operation at elevated

Packaging options abound for serial EEPROMs. Microchip Technology, for example, offers DIP, small-outline (SO), chip-on-board (COB), and bare die for its products.

Acronyms used in this article

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
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<tbody>
<tr>
<td>CPU</td>
<td>central processing unit</td>
</tr>
<tr>
<td>DIP</td>
<td>dual in-line package</td>
</tr>
<tr>
<td>EEPROM</td>
<td>electrically erasable read-only memory</td>
</tr>
<tr>
<td>EIAJ</td>
<td>Electronic Industries Association of Japan</td>
</tr>
<tr>
<td>I2C</td>
<td>interintegrated circuit</td>
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<tr>
<td>JEDEC</td>
<td>Joint Electron Device Engineering Council</td>
</tr>
<tr>
<td>SO</td>
<td>small-outline package</td>
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<tr>
<td>UART</td>
<td>universal asynchronous receiver/transmitter</td>
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</table>

EDN October 1, 1991
Serial EEPROMs

temperatures greatly speeds the cell's failure rate and decreases the endurance rating. Allowing a cell to rest between erase/write cycles, on the other hand, enables it to release some of the trapped electrons and extends its effective life. Therefore, when examining endurance ratings, be sure you know the conditions under which devices were rated.

If the EEPROM's endurance is a limiting factor in your designs, there are several steps you can take to extend your circuit's service lifetime. One possibility is to use a device with more capacity than you need. If you check for cell failure following each write operation, or use a counter to keep track of the erase/write cycles you've used, you can move your data into another section of memory if one section starts failing, then resume operation.

Alternatively, you may wish to use a nonvolatile RAM that offers a serial interface, such as the Catalyst CAT24C44 ($1.50) and the Xicor X24C4 ($1.11). These devices operate like a serial RAM, but have an EEPROM array backing the RAM array. If you need a nonvolatile copy of the data in RAM, you simply signal the device to copy the

Interfacing alternatives

Although there are a variety of interface methods for serial EEPROMs, only two are widely distributed: Microwire from National Semiconductor and the interintegrated circuit (I²C) from Philips. Each method has its own strengths and weaknesses.

Several fundamental differences exist between the two interfaces, the most obvious being the number of signals required. The Microwire interface uses four signals: data in, data out, chip select, and a shift clock. You activate the device by asserting chip select and clocking in an opcode and data address (if applicable). You then clock data in or out as applicable. The I²C bus uses only two wires, a clock and a data line. The I²C protocol calls for the bus master to send a slave address to activate the device desired, then the opcode and data. The slave device acknowledges reception of the address and each byte of opcode and data, then supplies any data requested. The I²C protocol prevents any contention on the shared data line.

You can reduce by one the number of I/O lines needed to connect to a Microwire device by tying the data-in and data-out lines together. This reduction is possible because the data-out line remains in a high-impedance state unless supplying read data. The danger in this approach is that the data-out line begins by supplying a dummy-zero bit as soon as the last address bit of the read command has entered the data-in line. If that address bit is high, the resulting bus contention may prevent the device from reading the address properly, or may result in excessive current being drawn into the device. Placing a current-limiting resistor in the connection between the data-in and data-out lines can help prevent damage, but may slow the data bus.

The two interfaces also differ in the way they indicate device status. Because EEPROMs require a relatively long time to complete erase or write operations (worst case can be as long as 10 msec), most serial EEPROMs offer a method of indicating when the operation is complete. Using this status indication can speed your overall access to the memory; you don't have to wait for the worst-case time period to elapse before using the EEPROM again.

The Microwire interface requires you to poll the data output line following an erase or write instruction. The line changes state to indicate the device's readiness. Some older devices use the interface developed by General Instruments. They communicate with a Microwire-like serial protocol, but have separate busy/status lines. They are handy if you wish to use an interrupt to signal the processor to the memory's readiness, rather than poll a status line. I²C-compatible devices don't offer any specific signal—they simply fail to acknowledge a command string if they are still busy.

The speed of the interface and depth of memory are other differences. The I²C specification limits the serial clock rate to 100 kHz. Further, its fixed addressing protocol limits the total amount of memory that can reside on a single bus to 16 kbytes. The fixed protocol is not entirely a disadvantage, however. It enables you to make your interface software independent of the EEPROM's bit density, allowing you increase or reduce memory without changing software. Microwire devices have a variable-length address, dependent upon their bit density.

The Microwire interface has no clock and addressing limits. Clock rates as high as 3 MHz are available, and the number of devices on a bus is limited only by your bus driver's capability. Recall, though, that each Microwire device needs a chip-select signal, so you'll need additional I/O ports to handle the additional memory.
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- ISO212, a combined signal and DC/DC power supply combination featuring low power consumption and a streamlined plastic ZIP package
- Low cost PWS740 and PWS750 multi-channel component power systems

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Burr-Brown's leadership spans thirty years in analog manufacturing and design innovation. The revolutionary capacitive isolation barrier is but one example.

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Burr-Brown Corp.
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*USA OEM prices in 1000s.
Serial EEPROMs

RAM into EEPROM. Similarly, you can load the RAM from the EEPROM array. This dual-array structure lets you make many changes to the contents of memory, using the EEPROM only when needed.

Another system consideration when choosing to use serial EEPROMs is the relative lack of standards for them. For example, the devices use a variety of interface protocols. Even with devices using the same protocol, there may be timing differences between manufacturers. Packaging is also nonstandard. The DIP versions of the EEPROMs are uniform, but interface protocols. Even with devices using the same protocol, there may be timing differences between manufacturers. Packaging is also nonstandard. The DIP versions of the EEPROMs are uniform, but surface-mount packages are diverse. There are two sizes of SO packages available, based on either the JEDEC or EIAJ standards. Although, by sizing the solder pads properly, you can accommodate either size device, the problem doesn't end there. The pinout of the SO packages is not standardized. Two pinout patterns are available, corresponding to the direction the manufacturers' die fit within the SO package. If you are looking at alternate sources for your design, therefore, be sure to check the package size and pinouts.

If you can get past the design considerations, you'll find that serial EEPROMs offer a range of special features. During the last two years, manufacturers have added features to increase the versatility of serial EEPROMs. One such feature is selectable word size. Many serial EEPROMs are organized as a series of 16-bit-wide registers, with some available in 8-bit widths. To give you more flexibility in choice, manufacturers now offer devices with a selectable organization, controlled by the logic level at an I/O pin.

Another frill is the ability to write-protect a section of memory. Most serial EEPROMs will protect memory from inadvertent write access when the supply voltage is low. Further, they have a software command to disable write access to a part. Both of these features are designed to prevent inadvertent writes to the memory when power is unstable and logic behavior is unpredictable. The newer write-protection feature is the ability to lock out a portion of memory during normal operation. Parts from International CMOS Technology, for example, have a pin-controlled write protect that prevents writing to the entire memory, letting you use it as a ROM. Some parts from Microchip, on the other hand, protect only the top half of memory, allowing you free access to the lower half. This type of write-protect scheme lets you create calibration tables or con-

For more information . . .

For more information on the serial EEPROMs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

***Atmel Corp***  
2155 O'Neal Dr  
San Jose, CA 95131  
(408) 432-0500  
FAX (408) 436-4300  
Circle No. 700

***Catalyst Semiconductor Inc***  
2251 Calle de Luna  
Santa Clara, CA 95054  
(408) 758-5700  
FAX (408) 980-4200  
Contact Krish Panu  
Circle No. 701

***Exel Microelectronics***  
2150 Commerce Dr  
San Jose, CA 95161  
(408) 432-5000  
FAX (408) 432-8710  
Contact Reggie Huff, x4656  
Circle No. 702

***Fujitsu Microelectronics Inc***  
Microelectronics Div  
3545 N 1st St  
San Jose, CA 95134  
(800) 642-7616  
(408) 622-9000  
FAX (408) 322-9044  
Circle No. 703

***International CMOS Technology Inc***  
2155 Lundy Ave  
San Jose, CA 95131  
(408) 454-6678  
FAX (408) 432-8105  
Contact Ed Nieda  
Circle No. 704

***Microchip Technology Inc***  
2555 W Chandler Blvd  
Chandler, AZ 85224  
(602) 345-3400  
FAX (602) 345-3200  
Contact David Lee  
Circle No. 705

***National Semiconductor Corp***  
2900 Semiconductor Dr  
Santa Clara, CA 95052  
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(408) 721-5000  
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Contact Bryan Liddiard  
Circle No. 706

***NEC Microelectronics Inc***  
Microelectronics Div  
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San Jose, CA 95134  
(800) 642-7616  
(408) 622-9000  
FAX (408) 322-9044  
Circle No. 707

***Oki Semiconductor***  
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Sunnyvale, CA 94086  
(408) 720-1900  
FAX (408) 720-1918  
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***Samsung Semiconductor***  
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San Jose, CA 95134  
(408) 854-7529  
FAX (408) 854-7873  
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***SGS-Thomson Microelectronics***  
1000 E Bell Rd  
Phoenix, AZ 85022  
(602) 887-6100  
FAX (602) 887-6101  
Contact John Green  
Circle No. 710

***Signetics***  
811 E Arques Ave  
Sunnyvale, CA 94086  
(408) 991-5386  
FAX (408) 991-2009  
Contact Joe Resendes  
Circle No. 711

***Xicor Inc***  
851 Buckeye Ct  
Milpitas, CA 95035  
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FAX (408) 342-0640  
Contact Rick Orlando  
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EDN October 1, 1991
How single-chip fuzzy logic can move your product to the head of its class

Need to make your product more intelligent? Fuzzy Logic is the solution of choice. Need to do it quickly and economically, with maximum flexibility? Then the NeuraLogix NLX230 Fuzzy MicroController™ is in a class by itself!

The NLX230 is a single-chip solution. One 40-pin package delivers Fuzzy Logic mastery to the most complex control problems.

The NLX230 is flexible. It can be easily configured for your specific control problem, usually in a matter of hours.

The NLX230 is fast. Its rule processing time is 30 to 40 times faster than typical software-based or software/hardware hybrid solutions.

The NLX230 is economical. In production quantities, this remarkable Fuzzy MicroController is priced under $4 per unit.

As the first true hardware based Fuzzy Logic controller, the NLX230 makes artificial intelligence available and simple. For most applications it can be an affordable high-performance replacement for 8-bit microprocessors. See how easily it adapts to your requirements; evaluate how the NLX230 can meet your demands with our low-cost Applications Development System.

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CIRCLE NO. 48

EDN October 1, 1991
Serial EEPROMs

figuration data, then lock them into the EEPROM.

A more flexible version of the write-protect scheme comes in the form of a programmable write-protect. This scheme, offered by several companies including Exel, National Semiconductor, Samsung, and SGS-Thomson, lets you select the beginning address of protected memory, thus protecting only the amount of memory you desire. This protection can be temporary or, by programming a special register, made permanent.

A unique data-protection scheme is available from Catalyst Semiconductor in its CAT33C704/804 series. These devices offer programmable write protection. Then, by programming the device with a password, you can convert the write-protected area of memory to read-protected memory, accessible only with the proper password. The remaining section of memory becomes write-protected. This secure-access feature is particularly useful if your EEPROM is to contain proprietary information, serial numbers, or access codes that you want to deny to the user.

Another relatively new feature of serial EEPROMs is low-voltage operation. Manufacturers have extended the operating voltage range of some serial EEPROMs to include typical battery voltages. Many now come in 3V versions, with some tolerating as low as 2.5V. Others, like the Exel parts, offer full operation to 3V and allow read-only operation as low as 2V.

Reference

Table 1—Representative serial EEPROMs

<table>
<thead>
<tr>
<th>Company</th>
<th>Part</th>
<th>Size (bits)</th>
<th>Organization (bits)</th>
<th>Interface compatibility</th>
<th>Serial clock rate</th>
<th>Supply current</th>
<th>Active (mA)</th>
<th>Standby (µA)</th>
<th>Endurance (cycles)</th>
<th>Data retention (years)</th>
<th>Operating voltage range (volts)</th>
<th>Package styles</th>
<th>Special features</th>
<th>Price (10,000) (DIP)</th>
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Notes:
1. Operating voltages have ±10% tolerance unless a range is shown.
2. DIPs listed are 8-pin, dual in-line packages unless noted. SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

EDN October 1, 1991
The FS700 LORAN-C frequency standard

10 MHz cesium stability

$4950

Cesium long term stability at a fraction of the cost
Better long-term stability than rubidium
Not dependent on ionosphere position changes, unlike WWV
Complete northern hemisphere coverage, unlike GPS.

The FS700 LORAN-C frequency standard provides the optimum, cost-effective solution for frequency management and calibration applications. Four 10 MHz outputs from built-in distribution amplifiers provide cesium standard long-term stability of $10^{-12}$, with short-term stability of $10^{-10}$ ($10^{-11}$ optional). Reception is guaranteed in North America, Europe and Asia.

Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ±360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.
<table>
<thead>
<tr>
<th>Company</th>
<th>Part</th>
<th>Size (bits)</th>
<th>Organization (bits)</th>
<th>Interface compatibility</th>
<th>Serial clock rate</th>
<th>Supply current</th>
<th>Standby current</th>
<th>Endurance (cycles)</th>
<th>Data retention (years)</th>
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<th>Package styles</th>
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**Notes:**
1. Operating voltages have ±10% tolerance unless a range is shown.
2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

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**Table 1—Representative serial EEPROMs (continued)**

**Notes:**
1. Operating voltages have ±10% tolerance unless a range is shown.
2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.
<table>
<thead>
<tr>
<th>Company</th>
<th>Part</th>
<th>Size (bits)</th>
<th>Organization (bits)</th>
<th>Interface Compatibility</th>
<th>Serial Clock Rate (MHz)</th>
<th>Supply Current Active (mA)</th>
<th>Standby (µA)</th>
<th>Endurance (cycles)</th>
<th>Data Retention (years)</th>
<th>Operating Voltage Range (volts)</th>
<th>Package Styles</th>
<th>Special Features</th>
<th>Price (10,000) (DIP)</th>
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<td>5 DIP, 14-pin SO</td>
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Notes:
1. Operating voltages have ±10% tolerance unless a range is shown.
2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.
Table 1—Representative serial EEPROMs (continued)

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<thead>
<tr>
<th>Company</th>
<th>Part</th>
<th>Size (bits)</th>
<th>Organization (bits)</th>
<th>Interface compatibility</th>
<th>Serial clock rate</th>
<th>Supply current</th>
<th>Active current (mA)</th>
<th>Standby current (µA)</th>
<th>Endurance (cycles)</th>
<th>Data retention (years)</th>
<th>Operating voltage range (volts)</th>
<th>Package styles</th>
<th>Special features</th>
<th>Price (10,000) (DIP)</th>
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Notes:
1. Operating voltages have ±10% tolerance unless a range is shown.
2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.
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<th>Serial clock rate</th>
<th>Supply current Active (mA)</th>
<th>Standby (µA)</th>
<th>Endurance (cycles)</th>
<th>Data retention (years)</th>
<th>Operating voltage range (volts)</th>
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EDN REPRINTS

A Designer's Guide to Linear Circuits

Volume I
This original, 186-page collection by Jim Williams offers a wealth of analog design information. It includes practical and efficient ways to use op amps, comparators, data converters, and other analog ICs.

Volume II

Surface-Mount Technology Design Project
This 48-page, four-color reprint follows the progress of EDN editor Steve Leitson as he designs a 2M-byte memory board using surface-mount technology. He includes typical problems you might encounter and objectively reports about both good and bad design decisions made along the way.

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CIRCLE NO. 39

EDN October 1, 1991
3½-in. optical drive offers MO and read-only modes

The OD-3000 optical disk drive lets designers buy optical technology in the increasingly popular 3½-in. form factor. The multifunction drive uses read/write MO (magneto-optical) technology and reads O-ROM (optical read-only memory) disks, whose features are similar to those of 5¼-in. CD-ROM disks. The drive stores 128 Mbytes on a removable optical disk that looks much like a 3½-in. floppy disk.

MO technology gives the OD-3000 several advantages compared with 5¼-in. products that use other types of rewritable optical media. MO technology uses magnetic-flux transitions to store data on the physical medium. The optical system writes to the disk using a laser beam to change the magnetic polarity of data bits on the disk. Likewise, the optical system reads data by sensing the reflection of the laser beam from the surface of the disk. Disks that use MO technology can withstand 10 million write cycles and still record data reliably. Other rewritable optical technologies typically limit media to 10,000 write cycles.

The drive can also read O-ROM disks that store prerecorded information, much like CD-ROM drives do. Mass duplication of O-ROM disks uses a stamping production technology. This technology is similar to the process used to make CD-ROM disks and audio record albums. Therefore, manufacturing costs of prerecorded O-ROM disks should soon drop to less than $2 each.

Both CD-ROM and O-ROM disks store data via pits in the physical medium’s surface. O-ROM offers some advantages compared with CD-ROM technology, however. CD-ROMs employ a long spiral track; O-ROM disks feature a format with tracks and sectors, like magnetic disks. The track-and-sector configuration results in superior seek times for computer applications. O-ROM technology also leads to a third type of medium that you can use with the OD-3000. Partial-ROM disks have O-ROM and rewritable technology mixed on a single surface. Users can add their own information such as graphics to the rewritable sections of a partial-ROM disk.

The OD-3000 features a 3000-rpm rotational speed, which minimizes latency during seek operation. The drive’s average rotational latency is 10 msec. The drive’s optic components are in two different physical locations to minimize seek time. The semiconductor laser, photodiode detector, lens, and prism are fixed in place away from the actuator arm. Only minimal optical components that provide focus and tracking functions reside on the actuator, resulting in a lower-mass actuator. The drive has a 42-msec seek time compared with specs greater than 60 msec for some optical drives.

Other key specs include 11W power dissipation during read/write operations and 2.6W when the drive is inactive. A Reed-Solomon error-correction scheme results in less than 1 error bit per $10^{12}$ bits. The drive can read data continuously from disk at 640 kbytes/sec and write data continuously at 203 kbytes/sec. Write operations require the erase, write, and verify passes common to all rewritable optical drives and...
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account for the slower speed.

The drive features a 128-kbyte buffer on the SCSI-2 controller. The controller can transfer buffered data to the host at 2 Mbytes/sec in asynchronous mode and at 5.3 Mbytes/sec in synchronous mode. The drive's MTBF spec is 30,000 power-on hours.

The key to the acceptance of 3½-in. optical drives will eventually be price. The OD-3000 costs $1050 (1000) and the rewritable disks cost $60 each. The company hopes to drop the prices by 50% or more within the next 18 months.

—Maury Wright
Teac America Inc, 7733 Telegraph Rd, Montebello, CA 90640, (213) 726-0303, FAX (213) 727-7621.
Circle No. 733

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**EDN's Editors' Choice**

On occasion, a new product will show a great deal of innovation and thus appear as an EDN Editors' Choice selection. To qualify for special coverage by our editors, an innovative product must:

- Offer significantly higher levels of performance in ways not previously available
- Solve a continuing problem much more effectively than its predecessor
- Exhibit a marked degree of cleverness, which differentiates it from earlier products
- Embody new technology that advances the state of the art or use older technology in a unique and innovative way.
Who's Behind The Simulation Acceleration Movement?

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GENRAD  

LSI LOGIC  
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COMPASS  
NEC  
SEATTLE SILICON  
EXPERTEST  

And Who's Leading It?

ZYCAD
Generator owes accuracy and versatility to DSP and arbitrary-waveform technology

Analogic Corp's 2030 harnesses technology not yet widely used in function generators to make daunting waveform-generation tasks seem rather straightforward. You can set it up to produce complicated waveforms with no more difficulty than you can get classical generators to output sine, square, and triangular waves. Moreover, the waveforms that the unit produces exhibit unusually low distortion and few artifacts. The firm accomplishes this feat by using digital technology—DSP technology—and playing tricks such as predistorting the samples fed to the unit's D/A converter to compensate for sampling effects and for the inherently nonideal transient response of the anti-imaging filter that follows the DAC.

Hidden within the half-rack-width enclosure is a Motorola 56001 DSP µP. The µP earns its keep; it executes algorithmic routines stored in ROM and fills the generator's dual-ported memory with samples that represent the output waveforms. The algorithms are much more compact than are point-by-point signal representations; therefore the generator can store an extensive waveform repertoire. If the individual waveforms stored this way don't meet your needs, you can add the waveforms to each other and multiply them by one another. Moreover, to remove artifacts that would otherwise appear, before routing the calculated waveforms to the DAC, the µP convolves them with the reciprocal of the output filter's impulse response.

This technique and other numeric sleights-of-hand let the generator produce a long list of modulated and swept-frequency waves—in addition to dc and the familiar sine, square, ramp, triangular, pulse, and pseudo-random-noise waveforms. The modulated waveforms include double-sideband AM (amplitude modulation) with full and suppressed carriers; single-sideband AM, also with full and suppressed carriers; FM (frequency modulation); phase modulation; exponentially decaying waves; the \( \sin(x)/x \) function; and both linear and logarithmic sweeps.

The sine-wave distortion level, although dependent on amplitude and frequency, is 80 dB below the output level at or below 100 kHz, regardless of amplitude. There are four amplitude ranges, from 10 mV to 10V full scale into an open-circuit. You can set the amplitude with 4-bit resolution, and you can select either 50Ω or 600Ω output resistance.

The generator's frequency range starts at 0.001 Hz and extends to 20 MHz for sine waves and to 5 MHz for pulses and for square, triangular, and ramp waves. Pulse rise time is approximately 15 nsec at and below 100 Hz; 10.0 to 10.4 µsec from 100 Hz to 1 kHz; 1 to 1.04 µsec from 1 kHz to 10 kHz; and 46

Adding and multiplying waveforms to produce even more complex waves is a snap with the block diagrams that appear on the bit-mapped, backlit LCD screen of the 2030 function generator. You make your selections using soft keys next to the screen.
Why make users do this?

When they can do this!

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disconnect the device, remove outer housing, reset the DIP switches, reassemble unit, and reconnect the device. Maximum downtime: 20 minutes.

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Panel-mounted and easily accessible, the Address Switch adds value to your product by replacing internal DIP switches on IC boards with instant access on the external housing. Available in a variety of colors to match your product, gang-mountable in virtually any configuration, the Address Switch uses the standard SCSI design to adapt readily to any product line.

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Don't you owe it to your product to stay competitive? Call us today at 708-360-3500, and we'll send you a Specifications Sheet describing the Address Switch in detail. Don't get left behind in the user-friendly race—the competition is already off and running.

"Switch Addresses with the Address Switch."

IBM is a registered trademark of the International Business Machines Corporation.
to 50 nsec from 10 kHz to 5 MHz. Peak pulse and square-wave overshoot is 0.1% and below 100 kHz and 0.2% above. You can set the output frequency of any waveform with a resolution of 1 part in 10^7 (0.1 ppm).

The vendor's earlier waveform generators relied heavily on algebraic definition of signals. If you could represent a signal as an equation and key it in, the generator would synthesize it. With the new instrument, which has a backlit, bit-mapped LCD screen, instead of fumbling with formulas, you make selections from menus of stored functions and from block diagrams of multiplication and addition operations. The unit has soft keys with functions designated by legends that appear on the screen, fixed-function keys, a numeric keypad, and, for those who prefer it to the keypad, a rotary control.

Because it incorporates the technology of a 12-bit-resolution arbitrary-waveform generator, the instrument can synthesize signals that are not in its library and that are not producible by manipulating the library functions. The vendor doesn't emphasize this arbitrary-function-generation capability, however. To use it, you must load waveform-definition files from an external source, such as a PC, via the unit's IEEE-488 or RS-232C ports. The generator includes both ports as standard equipment. The ports let you use terse commands to recall any of 15 complete setups from non-volatile memory. You can retrieve the setups manually by pressing a few keys. The unit costs $3995.

—Dan Strassberg
Analogic Corp., 8 Centennial Dr., Peabody, MA 01960. Phone (508) 977-3000. FAX (508) 531-1266. TLX 6817021. Doug Estrich.

Circle No. 731

EDN October 1, 1991
Stalking system performance is your goal. That's why Maxtor's 1.2GB SCSI Panther was designed to perform a data seek in just 13ms. No other drive in its class features such lightning speed.

Panther’s hunting prowess of 2ms track-to-track seek time stands out compared to Seagate's Wren 7 seek time of 2.5ms. And Panther outruns the competition with a 30Mb/sec. internal transfer rate.

Experience counts. Panther uses the reliable head disk assembly used in the Maxtor XT-8000, which boasts more than 300,000 units in the field. Panther shreds the competition with the widest range of available controllers, an MTBF of 150,000 hours, Novell certification and a highly competitive price.

Call about the full line of Panther drives that range from 1.2GB to more than 1.7GB capacity. If you're stalking performance, check out Panther's killer specs.

Call your nearest Authorized Maxtor Distributor.

<table>
<thead>
<tr>
<th>1GB-plus Disk Drive Comparison Criteria</th>
<th>Maxtor Panther P0-12S</th>
<th>Seagate Wren 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity (unformatted)</td>
<td>1.2GB</td>
<td>1.2GB</td>
</tr>
<tr>
<td>Seek Time</td>
<td>13ms</td>
<td>15ms</td>
</tr>
<tr>
<td>Track-to-Track</td>
<td>2ms</td>
<td>2.5ms</td>
</tr>
<tr>
<td>Internal Transfer</td>
<td>17.4 to 29.7Mb/s</td>
<td>15-23Mb/s</td>
</tr>
<tr>
<td>Maximum Seek</td>
<td>26ms</td>
<td>34ms</td>
</tr>
</tbody>
</table>

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PRODUCT UPDATE

Raster image accelerator IC renders fonts in real time

The D7001 IC renders outline fonts in real time for graphics display and printer applications. The device is the first IC in the company's RIDA (raster image device accelerator) family of ICs that accelerate the rendering of graphic objects. It can produce outline fonts scaled to any size fast enough for laser printers to print at speeds of 17 pages/minute and slower. The IC can also be used in mother board graphics applications to directly drive WYSIWYG display and printer engines.

The IC accepts Bezier curves, B-spline curves, and vectors. You can use the chip in TrueType, Postscript, and Intellifont page-description-language applications. Multiple filling algorithms handle both Roman characters and Kanji glyphs, and on-chip hardware compensates for pixel dropouts—a key feature for Kanji applications in which slight changes affect the meaning of glyphs. Scaling capabilities enable the chip to produce fonts ranging in size from 0.25 to 999.99 points.

Currently, most display and printer controllers use software or firmware to render fonts. The D7001 provides 1000-to-1 font-rendering acceleration compared with firmware- and software-based designs. The IC treats outline fonts as objects rather than using graphics primitives.

The IC uses on-chip parallel processors with pipelined hard-wired instruction sets (Fig 1). When producing 300-dpi-resolution fonts at 12 points, the IC can render more than 7500 cps. Such a speed lets you implement a printer controller without the traditional 1- or multiple-line font cache. In fact, the IC can essentially render fonts in real time and requires only an 8-kbyte single-character font cache.

The D7001 comes in a 144-pin quad flatpack. Samples cost $35. Expect production quantities to be available by year's end for $25 (1000). The company hopes to offer a companion IC next year that can accelerate the drawing of graphic images.—Maury Wright

Destiny Technology Corp, 300 Montague Expressway, Suite 150, Milpitas, CA 95035, (408) 262-9400, FAX (408) 262-0221.

Circle No. 730

![Fig 1](attachment:image.png)
Compact units feature brushless dc motors with integral controller and variable speed capability

These new Windjammer® blowers combine electronics, motor, and fan system in a compact, cost-effective package that operates from a standard 120 VAC input. An exclusive Lamb Electric design, they were developed from demanding, limited space applications such as business machines, medical equipment and materials handling applications.

Just 5.7" in diameter, the blowers have 1-, 2-, or 3-stage fans for performance from 75" H₂O vacuum at 0 CFM to 125 CFM at 0" H₂O. With one version, a 0 to 10 VDC signal from a sensor or other device will control motor speed and adjust air performance from 0 to 100%. Or, a second model provides manual speed control by means of a potentiometer located in the blower housing.

These blowers also feature low noise performance and are UL/CSA component recognized. Get complete details by contacting AMETEK, Lamb Electric Division, 627 Lake Street, Kent, OH 44240. (216) 673-3451. Fax: 216-673-8994. Telex: 433-2140. Cable: LAMETEK.
IC tester offers 200-MHz testing for analytical applications

The Logic Master ATS test station provides characterization of new chips, failure analysis, quality assurance, and low-volume production tests for devices requiring clock rates as high as 200 MHz. Proper device characterization requires clock rates and accuracy comparable to a production tester.

Although production testers can perform characterization and other applications, they often have two drawbacks. First, they are expensive—the demand for high clock rates, high accuracy, and high throughput place requirements on production test systems that are difficult to achieve at any price. Because the high throughput capability of a production tester is not used during characterization, the cost of a production tester is difficult to justify. Second, because production test-system software is designed for test engineers, it's not always easy for a design engineer to use when evaluating a new chip design.

This test station is priced at $2600 to $3200 per pin. It offers 200-MHz clock rates without multiplexing channels and data rates as high as 400 Mbits/sec. Standard system accuracy is ±500 psec. The system has 50-psec edge-placement resolution and ±100-psec stability and linearity, allowing you to fine-tune the calibration for special applications.

The test system uses the highest performance for the pin drivers and uses custom GaAs drivers and receivers. Other parts of the tester use ECL standard-cell devices, CMOS gate arrays, and FPGAs.

The GaAs drivers let you program driver rise and fall times between 1 and 3 nsec for 5V swings. For 600-mV signal swings, the rise and fall times are programmable from 500 psec to 1 nsec. Each driver and comparator is independent and can have its own drive and compare levels set with 10-mV resolution between -1.5 and +6.5V for drive high and -2.5 and +4.5V for drive low. Dual threshold comparators let you perform timing-window comparisons.

The tester also provides dynamic current loads for testing output pins under real-world load conditions and for testing the time required for 3-state outputs to switch to their high-impedance state. Two optional parametric measurement units (PMUs) are available for the tester. One is a “per-pin” PMU that uses comparators to test voltage or current levels to programmed limits. The other PMU analyzes and measures absolute current or voltage levels.

The tester operates with dual formats for channels running at twice the clock or data rate of other channels. This feature is useful when you need to test microprocessors and other devices with multiple phase clocks.

The system is hosted by a Sun workstation and has an Ethernet port for network operation. A 502-Mbyte hard disk is standard.

Software included with the tester provides simulator pattern conversion, system setup, pattern generation, and graphical waveform editing. The system has built-in soft-
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UPDATE

Hardware for measuring standard device parameters such as setup, hold, and propagation-delay times. Software is also available for translating test programs written for mainframe testers.

The test station is available in two versions. The ATS 1 supports 16 to 224 I/O channels and has 12 timing generators providing 24 timing edges. The ATS 2 supports 16 to 448 I/O channels and has 24 timing generators. Each channel in either system can select timing edges from 12 timing generators. A 128-I/O-channel system with 128k-deep pattern memory costs $360,000.—Doug Conner

Integrated Measurement Systems Inc, 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117. FAX (503) 644-6969.

Circle No. 732

JUST ASK

Have you been stumped by a design problem? Can't interpret a spec sheet? Ask EDN. Our editors are ready to help.

The Ask EDN column serves as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help.

Address your questions and answers to Ask EDN, 275 Washington St, Newton, MA 02158; FAX (617) 558-4470; MCI: EDNBOS. Or, send us a letter on EDN's bulletin-board system. You can reach us at (617) 558-4241 and leave a letter in the /ask_edn Special Interest Group.
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- Ideal for ATE applications
- Optical isolation
- Fast switching speed
- Adjustable turn-on times
- Low profile 6-pin mini-DIP
- Cost efficiency

Review the electrical characteristics below and call us for immediate application assistance:

<table>
<thead>
<tr>
<th>INPUT ELECTRICAL CHARACTERISTICS</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous Input Current (I_{in})</td>
<td>10</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>Input Current (Guaranteed Off)</td>
<td>10</td>
<td></td>
<td>mA_{DC}</td>
</tr>
<tr>
<td>Input Voltage Drop at (I_{in}) = 25mA</td>
<td>100</td>
<td></td>
<td>µA_{DC}</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OUTPUT ELECTRICAL CHARACTERISTICS</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
<td>FB00CD</td>
<td>FB00FC</td>
<td>FB00KB</td>
</tr>
<tr>
<td>Bidirectional Load Current (I_{LOAD})</td>
<td>±1.0</td>
<td>±0.50</td>
<td>±0.25</td>
</tr>
<tr>
<td>DC Load Current (I_{LOAD})</td>
<td>2.0</td>
<td>1.0</td>
<td>0.5</td>
</tr>
<tr>
<td>Bidirectional Load Voltage (V_{LOAD})</td>
<td>±80</td>
<td>±180</td>
<td>±350</td>
</tr>
<tr>
<td>DC Load Voltage (V_{LOAD})</td>
<td>80</td>
<td>180</td>
<td>350</td>
</tr>
<tr>
<td>ON-Resistance (R_{ON}) at (I_{LOAD}) max.</td>
<td>0.72</td>
<td>1.8</td>
<td>12.9</td>
</tr>
<tr>
<td>Turn-On Time (T_{ON})</td>
<td>600</td>
<td>800</td>
<td>500</td>
</tr>
<tr>
<td>Turn-Off Time (T_{OFF})</td>
<td>300</td>
<td>600</td>
<td>500</td>
</tr>
</tbody>
</table>

Notes:
1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).
2. Rated input current is 25mA for all tests.
3. Loads may be connected to any output terminal.
4. ON resistance shown is for the bidirectional configuration. The DC ON resistance is 1/4 of these values.

*For immediate application assistance call 1-800-284-7007.*

Teledyne Solid State, 12525 Daphne Avenue, Hawthorne, California 90250.
Good news for networks!
The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.

More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

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For technical literature and more information, call 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

THIS IS AMP TODAY.
Local-area networks (LANs) are becoming as congested as our nation’s highways. Packet data traveling on Ethernet LANs must share a single 10-Mbps pathway. Packet data on a Token Ring LAN migrate at 4 or 16 Mbps. These posted speed limits can cause severe data-traffic jams during peak activity periods. The slowdowns are not only frustrating, but in some cases they can bring network activity to a virtual halt. The most expedient option to alleviate congestion is to move data faster—an option that, if employed in highway management, would have disastrous consequences.

In 1982, the X3T9.5 committee of the American National Standards Institute (ANSI) recognized these impending logjams and set about defining a set of protocols that lets packet data whiz over a LAN at 100 Mbps. This super highway is the Fiber Distributed Data Interface (FDDI). The ANSI X3T9.5 standard for FDDI defines a dual counter-rotating ring LAN that uses a fiber-optic medium and a token-passing protocol. (For definitions of FDDI terms, see box, “Glossary of FDDI terms.”)

An FDDI LAN can stretch 100 km and connect more than 500 nodes spaced by as much as 2 km. In contrast, first-generation LANs such as Ethernet, defined by IEEE standard 802.3, and Token Ring, defined by IEEE standard 802.5, operate over a more limited distance. Ethernet can stretch only 2.5 km and connect as many as 1024 nodes spaced by as much as 0.5 km. Token Ring can stretch only 1.2 km and connect as many as 96 nodes spaced by as much as 0.46 km. FDDI’s long distance specification coupled with its 100-Mbps data transmission rate make it suitable as a fast-throughput backbone that can transport data between existing LANs via gateways, bridges, and routers (Fig 1). Any network manager who is experiencing or projecting network traffic overloads should consider the pros and cons of FDDI.

The FDDI specification conforms to a general, 7-layer hierarchical model for network communications called the Open Systems Interconnection (OSI) model (Fig 2). The FDDI spec describes both a physical layer that corresponds to the OSI model’s physical layer and a media-access-control (MAC) sublayer that corresponds to the lower half of the OSI model’s data-link layer. The spec also describes a Station Management (SMT) network supervisory function, which falls outside of the OSI model. The SMT function is implemented in software. This software resides on each station of the ring and creates logical paths between the physical layer and the MAC sublayer to permit SMT-to-SMT communications between stations. SMT software connects and disconnects the station to the ring, monitors network operations for reporting status to the host computer, isolates network faults, and detects conditions such as duplicate addresses that would inhibit ring operation.

Realizing that there would be considerable discussion about the types of fiber, connectors, and other interconnect hardware, the ANSI X3T9.5 committee decided to break the specification for the OSI physical layer into two sublayers—the Physical Medium Dependent (PMD) sublayer and the Physical (PHY) sublayer. The lower of the two sublayers, PMD, specifies the transmission wavelength to be 1300 nm. Both LEDs and lasers can emit light of this wavelength. The PMD sublayer spec recommends 62.5/125-µm
The FDDI standard defines a dual counter-rotating ring LAN that uses fiber-optic cable and lets packet data rocket to 100 Mbps. (Photo courtesy SBE Inc, concept and photography by Imagination)
The ANSI X3T9.5 FDDI standard defines a dual counter-rotating ring LAN that uses a fiber-optic medium and a token-passing protocol.

(core diameter/cladding diameter) multimode cable and has advice on using 50/125-, 85/125-, and 100/140-µm cable. The dispersion in multimode 62.5/125 micron cable is small enough to ensure FDDI's 10⁻⁹ bit error rate. Debate continues over cable size. The PDM document is written so that any size cable capable of 1300-nm transmission conforms to the FDDI standard as long as the cable also meets the optical power, channel bandwidth, and distance requirements.

**Trying to reduce cable costs**

However, fiber-optic cable isn't cheap, and the cost of the cable, as well as the light-emitting source, increases as the wavelength increases. In fact, the highest cost associated with implementing FDDI is the major drawback to its proliferation. Codenoll Technology Corp, an FDDI-node-controller vendor, has proposed using an 830-nm LED emitter and 830-nm multimode cable to reduce the high materials cost of an FDDI network. The wavelength does not meet the FDDI standard, but the company claims that the only effect of the wavelength change is the shortening of the maximum allowable distance between nodes from 2 to 0.5 km.

A working group of the ANSI X3T9.5 committee is trying to lower FDDI costs by developing a PMD spec that uses less-expensive shielded twisted-pair (STP) copper wire as the medium while maintaining FDDI speeds. The specification would specify a much shorter distance between nodes—probably less than 100 m—and replace optical transceivers and connectors with lower-cost STP connectors. STP is also attractive because many facilities already have STP copper wire installed for Ethernet LANs.

Because an ANSI standard for STP communication is not expected until late 1992, five companies—Advanced Micro Devices, Chipcom Corp, Digital Equipment Corp, Motorola Inc, and Synoptics Communications Inc—recently defined and published an STP standard for 100-Mbps data. Products conforming to this standard, which is open for public use, will be able to communicate with each other.

Copper wire costs much less than fiber cable, but...
metal-based networks are susceptible to electromagnetic interference and are less secure than fiber-optic communications—two of FDDI's big pluses. In addition, because FDDI's ring topology demands that each station operate as a repeater, nonstandard PMD implementations can't be used on the FDDI backbone.

**Group encoding limits bandwidth**

PHY, the upper sublayer of FDDI's physical-layer specification, defines a 4B/5B group-encoding scheme for representing 4-bit data and control symbols. The scheme doesn't use Manchester encoding, which is typical of other LAN protocols. Manchester encoding would require a 200-MHz clock to transmit 100-Mbps data. The 4B/5B group-encoding scheme requires the transmission of a 5-bit code word for each 4-bit symbol, thereby achieving a 125-Mbps rate. The code word is converted to a nonreturn-to-zero-inverted (NRZI) signal for network transmission. The PHY sublayer also defines how to decode the 4B/5B NRZI signal from the network into symbols that the station can recognize.

Because an NRZI signal has no transitions when all zeros are present in the data, the 4B/5B encoding scheme guarantees that data have no more than three consecutive zeros. Although the encoding scheme uses less bandwidth than Manchester encoding, clock recovery is more difficult. Therefore, instead of using one master clock to generate data as the IEEE 802 standards specify, PHY sublayer specifies that each station in the FDDI ring regenerate the data with a frequency-stable reference to prevent frequency-jitter from accumulating around the ring. Each station has a phase-locked loop, which clocks the received data into an accordion buffer, and a crystal-controlled frequency source, which clocks the data out of the buffer.

**MAC sublayer delivers frames**

The FDDI media-access-control (MAC) sublayer defines the token-passing protocol for data transmission over the ring. The MAC spec defines packet-frame fields such as headers, trailers, addresses, and cyclic redundancy checking (CRC). An FDDI information-packet frame comprises a preamble having 16 or more IDLE (5-bit group code of all 1s) symbols, a 2-symbol...
The PHY sublayer must decode a 4B/5B NRZI signal from the network into symbols a station can recognize.

Start-of-frame field, a 2-symbol frame-control field that identifies the packet type, a 16- or 48-bit destination address, a 16- or 48-bit source address, the information field, a 32-bit CRC field, a 1-symbol end-of-frame field, and a frame-status field. The maximum packet size is 4500 octets. (Ethernet has 1514 octets max, and Token Ring has 8191 octets max.)

Stations wanting to transmit data over the ring must first obtain a unique 6-symbol token. The Timed Token Rotation (TTR) protocol requires each station to measure the time elapsed since it last received this token. An initialization procedure guarantees fairness by establishing a target token-rotation time (TTRT) that each station must observe. When a station has the token, it can transmit synchronous data during the TTRT. If the next station receives the token before the previous station's TTRT expires, the station can transmit frames asynchronously during the leftover time.

The MAC sublayer is responsible for controlling the flow of data. Each station's MAC sublayer monitors a packet's destination address, copies the packet into the station's memory if the packet is addressed to the station, and then relays the packet to the next station on the ring. The sending station's MAC sublayer deletes the packet once it comes full circle.

Chip set implements FDDI sublayers

Three vendors currently offer chip sets that implement the FDDI MAC and PHY sublayers—Advanced Micro Devices, National Semiconductor, and Motorola. These chip sets interface directly to the logical-link control (LLC) sublayer of the OSI model's data-link layer. All vendors offering stations that connect to an FDDI network employ one of these chip sets. The stations implement the SMT functions in software or firmware. Most stations employ the media interface connector (MIC) defined in the FDDI PMD specification. The MIC is a shrouded fiber-optic coupling in which a male plug terminates the cable and a female receptacle resides on the FDDI module. Some stations employ an ST connector to reduce cost. The ST conne-

<table>
<thead>
<tr>
<th>Glossary of FDDI terms</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ANSI:</strong> American National Standards Institute.</td>
</tr>
<tr>
<td><strong>Backbone network:</strong> A primary network that interconnects two or more secondary networks via gateways, bridges, and concentrators.</td>
</tr>
<tr>
<td><strong>BNC:</strong> Baby n connector.</td>
</tr>
<tr>
<td><strong>bps:</strong> Bits per second.</td>
</tr>
<tr>
<td><strong>Concentrator:</strong> A node on the FDDI ring that provides connections for multiple FDDI stations to communicate with other stations on the dual ring.</td>
</tr>
<tr>
<td><strong>Connection management (CMT):</strong> That portion of the SMT software that controls station insertion and removal as well as the connection of a station's PHY and MAC sublayers.</td>
</tr>
<tr>
<td><strong>CRC:</strong> Cyclic redundancy checking.</td>
</tr>
<tr>
<td><strong>Data-link layer:</strong> The OSI layer that implements data transfer between two stations on an FDDI network.</td>
</tr>
<tr>
<td><strong>Dual-attachment station (DAS):</strong> A station that provides two physical attachments to accommodate the dual counter-rotating FDDI ring.</td>
</tr>
<tr>
<td><strong>Fiber Distributed Data Interface (FDDI):</strong> A standard for a 100-Mbps token-ring LAN based on a fiber-optic medium. The ANSI X3T9.5 standard employs a dual counter-rotating ring, which provides fault tolerance. FDDI conforms to the OSI model.</td>
</tr>
<tr>
<td><strong>IEEE:</strong> Institute of Electrical and Electronics Engineers.</td>
</tr>
<tr>
<td><strong>LAN:</strong> Local-area network.</td>
</tr>
<tr>
<td><strong>LED:</strong> Light-emitting diode.</td>
</tr>
<tr>
<td><strong>Logical link control (LLC) sublayer:</strong> The upper sublayer of OSI's data-link layer. The LLC sublayer controls the flow of data.</td>
</tr>
<tr>
<td><strong>Media access control (MAC) sublayer:</strong> The lower sublayer of OSI's data-link layer. The MAC sublayer is responsible for scheduling frames for data transmission over the FDDI ring.</td>
</tr>
<tr>
<td><strong>Media interface connector (MIC):</strong> The specified FDDI fiber-optic connector. The connector has two 2.5-mm ceramic ferrules within a shrouded assembly. An MIC plug terminates the cable, and an MIC receptacle resides on the FDDI attachment.</td>
</tr>
<tr>
<td><strong>Network layer:</strong> The OSI layer responsible for routing, switching, and internetworking access.</td>
</tr>
<tr>
<td><strong>Nonreturn to zero inverted (NRZI):</strong> A signal code that represents a logical 1 by a polarity transition and a logical 0 by no transition.</td>
</tr>
<tr>
<td><strong>Octet:</strong> A data unit comprising eight bits. An octet represents a pair of data symbols.</td>
</tr>
<tr>
<td><strong>Open Systems Interconnection (OSI) model:</strong> A general, 7-layer model that defines a hierarchy of services necessary to exchange information between</td>
</tr>
</tbody>
</table>
You can configure some FDDI node controllers, such as the V/FDDI 4211 Peregrine board for the VMEbus, as single- or dual-attachment stations. The Interphase Corp board uses the Advanced Micro Devices FDDI chip set.

You can configure some FDDI node controllers, such as the V/FDDI 4211 Peregrine board for the VMEbus, as single- or dual-attachment stations. The Interphase Corp board uses the Advanced Micro Devices FDDI chip set.

tor is a spring-loaded twist-and-lock coupling similar to a BNC connector.

FDDI permits two types of stations: Class A and Class B. Class A stations are dual-attachment stations (DAS), which have dual physical layers that connect to the primary and secondary rings in FDDI's dual counter-rotating ring topology. All the stations attached to the FDDI's dual-ring backbone must be Class A stations. A Class A station on the dual-ring backbone can function in one of three ways: as a node controller that adapts a computer or peripheral to the ring, as a concentrator that acts as the hub of a star topology when connecting multiple FDDI stations to the ring, or as an internetworking module, such as a gateway, bridge, or router. Class B stations are single-attachment stations (SAS) and have a single physical layer. They attach to a concentrator's SAS port (Fig 3) and can be node controllers or internetworking modules.

Although the FDDI specification doesn't prohibit Class A stations from transmitting data on both the primary and the secondary ring, this mode of operation isn't wise. Theoretically, you could double the data-transmission rate to 200 Mbps by using both rings, but you would defeat one of FDDI's most attractive features. FDDI's secondary ring is meant to provide fault tolerance, which is a critical need in high-performance applications. If a fault occurs in the primary ring, the SMT ring-management protocol recognizes that the TTRT is violated and notifies the network manager. The SMT software isolates the fault.

computers. The International Organization for Standardization (ISO) defined the model in 1979 as a framework for defining network protocols.

PC: Personal computer.

Physical (PHY) sublayer: FDDI's upper sublayer that corresponds to the OSI model's physical layer. This sublayer is responsible for delivering symbols from the MAC sublayer to the FDDI network.

Physical layer: The OSI layer that permits the physical connection of a station to a LAN.

Physical Medium Dependent (PMD) layer: FDDI's lower sublayer that corresponds to OSI's physical layer. The PMD sublayer specifies optical power, cable specifications, the MIC connector, and optical bypassing.

RAM: Random-access memory.

Ring management (RMT): That portion of the SMT software that manages a station's MAC sublayer. RMT software detects faults, such as duplicate addresses, at the MAC layer.

Shielded twisted pair (STP): Describes copper wire commonly used in LANs.


Single-attachment station (SAS): A station that offers one attachment to an FDDI network.

Station: An addressable node on an FDDI network that is capable of transmitting, repeating, and receiving information.

Station management (SMT): Describes the supervisory software that monitors an FDDI station and controls station activity.

ST connector: A fiber-optic connector employed in many fiber-optic LANs. The AT&T connector contains a ceramic ferrule encased in a twist-and-lock assembly similar to a BNC connector.

Target token-rotation time (TTRT): The maximum time an FDDI station has to transmit data on the ring. The TTRT is established by the lowest bidding station during an initialization process.

TCP/IP: The US Department of Defense's Arpanet suite of protocols for implementing the transport and network layers of the OSI model.

Token: A unique 6-symbol frame that circulates around the FDDI ring. A station must have the token to transmit data.

4B/5B: The symbol encoding method specified by the FDDI standard in which each set of four bits is encoded as five bits.
FDDI stations

and wraps the upstream primary ring into the downstream secondary ring to reconstruct a ring network.

Multiple failures on the ring can segment the network. In these rare cases, the network manager may have another ring-reconstruction option at his or her disposal. The PMD specification provides for an optional optical bypass switch that can be activated to bypass a Class A station completely. Activating the optical bypass switch would let the network manager service the faulty station off line.

FDDI stations can be node controllers, concentrators, or internetworking modules. Node controllers are adapter boards for popular computer buses, such as the ISA bus, VMEbus, and Multibus (Table 1). One of the three commercially available FDDI chip sets provides the PHY and MAC sublayers for the station. The board's PMD hardware determines whether the node controller is an SAS or a DAS. A node controller generally has a microprocessor unit and enough RAM to run the LLC sublayer and offload communications tasks from the host computer.

Some node controllers contain EPROM for SMT firmware; others download the SMT software into the onboard RAM. All of these boards communicate with the host at the network layer of the OSI model. Although the ANSI committee has not yet drafted protocols for the network layer, the TCP/IP suite of protocols is the most popular method for transferring files. FDDI node controllers support other network-layer protocols as well.

Concentrators play a crucial role in an FDDI network by letting you connect multiple stations to an FDDI backbone via one DAS port (Table 2). FDDI defines four types of concentrator ports: A, B, S, and M ports. The A and B ports provide the DAS connection to the dual ring. The M (master) and S (slave) ports let you cascade concentrators and SAS stations in tree topologies. A concentrator can have as many as 255 M ports. These ports can connect to the primary or secondary FDDI ring or to an S port on another concentrator.

Concentrators are either computer bus boards or stand-alone chassis containing expansion boards. Because a concentrator is a critical link for connecting

---

**Fig 3**—You can attach multiple Class B stations to an FDDI dual ring by using a concentrator. Class A stations have dual-attachment-station (DAS) ports, which connect directly to the dual ring.
<table>
<thead>
<tr>
<th>Company</th>
<th>Model</th>
<th>Computer Bus</th>
<th>Protocol support</th>
<th>Microprocessor unit</th>
<th>FDDI chip set</th>
<th>Connector type</th>
<th>Power</th>
<th>RAM buffer</th>
<th>Inter-operability tests¹</th>
<th>Price</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMC</td>
<td>1150</td>
<td>VMEbus (6U)</td>
<td>TCP/IP (onboard SMT firmware)</td>
<td>Am29000 A&amp;T (PHY), AMD (MAC), CMC (LLC)</td>
<td>ST (SAS or DAS)</td>
<td>32.5W</td>
<td>2 Mbytes</td>
<td>ANTC</td>
<td>$11,245 to $11,955</td>
<td>Link-level firmware interfaces to host-based TCP/IP. Microprocessor unit can implement network- and transport-layer protocols on board. Integrated SMT and SNMP software.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1050</td>
<td>VMEbus (9U)</td>
<td>TCP/IP (onboard SMT firmware)</td>
<td>Am29000 AMD</td>
<td>ST (SAS or DAS)</td>
<td>140W</td>
<td>1 Mbyte</td>
<td>ANTC, UNH</td>
<td>$8950 to $9950</td>
<td>Integrated SMT and SNMP software. Link-level firmware interfaces to host-based TCP/IP.</td>
<td></td>
</tr>
<tr>
<td>Codenet Technology Corp</td>
<td>Code-</td>
<td>EISA or ISA bus</td>
<td>TCP/IP</td>
<td>None AMD</td>
<td>MIC (SAS)</td>
<td>10W</td>
<td>128 kbytes</td>
<td>None</td>
<td>$4995</td>
<td>Optional support for 830-nm fiber. Optical bypass switch support.</td>
<td></td>
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<td></td>
<td>net-</td>
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<tr>
<td></td>
<td>9540</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMC</td>
<td>CL-386/ DAS</td>
<td>Multibus II (6U)</td>
<td>TCP/IP (end of 1991) (onboard SMT firmware)</td>
<td>80386 AMD</td>
<td>MIC (DAS)</td>
<td>45W</td>
<td>4 Mbytes</td>
<td>None</td>
<td>$7140 (100)</td>
<td>Optical bypass control. Two RS-232C serial ports.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CX-MBII</td>
<td>Multibus II (6U)</td>
<td>GOSP, TCP/IP (onboard SMT firmware)</td>
<td>80386 AMD</td>
<td>MIC (DAS)</td>
<td>NA²</td>
<td>4 Mbytes</td>
<td>NA</td>
<td>$11,280 to $12,280</td>
<td>Optical bypass control. Implements Intel's INa 960 Networking software.</td>
<td></td>
</tr>
<tr>
<td>Digital Equipment Corp</td>
<td>FDDI Controller 400</td>
<td>XMI bus</td>
<td>XTP, TCP/IP (onboard SMT firmware)</td>
<td>68020 Digital (licensed to AMD and Motorola)</td>
<td>MIC (SAS)</td>
<td>65W</td>
<td>1 Mbyte</td>
<td>ANTC, UNH</td>
<td>$19,900</td>
<td>Operates in VAX 6000 and VAX 9000 computers.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FDDI Controller 700</td>
<td>Turbo Channel bus</td>
<td>TCP/IP (onboard SMT firmware)</td>
<td>68000 Digital (licensed to AMD and Motorola)</td>
<td>ST, BNC (SAS)</td>
<td>20W</td>
<td>1 Mbyte</td>
<td>ANTC, UNH</td>
<td>$4500 to $6000</td>
<td>Operates in VAX 6000 and VAX 9000 computers. Board supports shielded twisted-pair connections.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Formation Inc</td>
<td>VME bus (6U)</td>
<td>TCP/IP (onboard SMT firmware)</td>
<td>Am29000 AMD</td>
<td>MIC (SAS or DAS)</td>
<td>35W</td>
<td>2 Mbytes</td>
<td>ANTC</td>
<td>$8500 (SAS) $9500 (DAS)</td>
<td>Optical bypass control. VRTX operating system. Optional Sun OS drivers.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Interphase Corp</td>
<td>Multibus I FDDI 2211</td>
<td>SNMP, TCP/IP, XTP (onboard SMT firmware)</td>
<td>Am29000 AMD</td>
<td>ST BNC (SAS or DAS)</td>
<td>42.5W</td>
<td>1.0 Mbytes</td>
<td>ANTC, UNH</td>
<td>$8995 (SAS) $10,995 (DAS)</td>
<td>Connection for dual PHY and dual MAC operation using two boards. Board supports shielded twisted-pair copper wire.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V/ FDDI 4211 Peregrine</td>
<td>VMEbus (6U or 9U)</td>
<td>SNMP, TCP/IP, XTP (onboard SMT firmware)</td>
<td>Am29000 AMD</td>
<td>ST BNC (SAS or DAS)</td>
<td>NA</td>
<td>1.0 Mbytes</td>
<td>ANTC, UNH</td>
<td>$8995 (SAS) $10,995 (DAS)</td>
<td>Connection for dual PHY and dual MAC operation using two boards. Board supports shielded twisted-pair copper wire.</td>
<td></td>
</tr>
<tr>
<td>SBE Inc</td>
<td>VCOM 100</td>
<td>VMEbus (6U)</td>
<td>TCP/IP, XTP (onboard SMT firmware)</td>
<td>68030 National Semiconductor</td>
<td>ST (SAS)</td>
<td>32.5W</td>
<td>4 Mbytes</td>
<td>ANTC</td>
<td>$4500 (100)</td>
<td>Runs Synertec's implementation of SMT. Two RS-232C serial ports. An optional mezzanine board provides DAS operation.</td>
<td></td>
</tr>
<tr>
<td>Summit Microsystems Corp</td>
<td>smFd-AT201</td>
<td>ISA bus</td>
<td>Onboard SMT firmware</td>
<td>None AMD</td>
<td>ST (DAS)</td>
<td>10W</td>
<td>128 kbytes</td>
<td>ANTC</td>
<td>$5950</td>
<td>Host-to-RAM block transfer rate is 3.0 Mbytes/sec (sustained).</td>
<td></td>
</tr>
</tbody>
</table>

Notes: 1. ANTC=Advanced Networking Test Center; UNH=University of New Hampshire. 2. NA=not applicable. 3. See box, "Glossary of FDDI terms," for definitions of other abbreviations.
FDDI stations

Multiple stations to the ring, some concentrators have fault-tolerant power supplies and let you insert and remove boards on the backplane while the power is on—a process called live insertion. In addition to the FDDI PMD, PHY, and MAC sublayers and the SMT function, concentrators also provide the Simple Network Management Protocol (SNMP) software for managing a TCP/IP network.

Internetworking modules let you integrate multiple disparate LANs onto an FDDI backbone—in effect creating a hybrid network (Table 3). A bridge is the oldest method for transparently interconnecting two networks. Bridges communicate at the data-link layer of the OSI model. An FDDI bridge reads each destination field in an FDDI frame to infer a destination address for the frame. By comparing this information with an address table, the bridge determines whether to ignore the frame or forward it to a station on an interconnected network.

Routers operate at the network layer of the OSI model. Routers forward data packets not based on the destination address but according to a network identi-

<table>
<thead>
<tr>
<th>Company</th>
<th>Model</th>
<th>Housing</th>
<th>Fault-tolerant power supply</th>
<th>Live insertion</th>
<th>Protocol support</th>
<th>Number of ports (max)</th>
<th>Power</th>
<th>Connector type</th>
<th>Inter-operability tests</th>
<th>Price</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Codenoll Technology Corp</td>
<td>Codenet-9041</td>
<td>EISA or ISA bus boards</td>
<td>No</td>
<td>No</td>
<td>SNMP, TCP/IP</td>
<td>12</td>
<td>10W</td>
<td>MIC (SAS or ST)</td>
<td>No</td>
<td>$1995</td>
<td>Optional support for 830-nm fiber. Runs on VRTX software.</td>
</tr>
<tr>
<td>Digital Equipment Corp</td>
<td>DEC concentrator 500</td>
<td>Standalone chassis</td>
<td>Yes</td>
<td>No</td>
<td>Protocol independent</td>
<td>18</td>
<td>120W (AC power)</td>
<td>MIC or ST</td>
<td>ANTC, UNH</td>
<td>$9000 to $52,500</td>
<td>Support twisted pair and thinwire.</td>
</tr>
<tr>
<td>Interphase Corp</td>
<td>Fiber hub 800</td>
<td>Standalone chassis</td>
<td>Yes</td>
<td>Yes</td>
<td>SNMP</td>
<td>8</td>
<td>NA</td>
<td>MIC (SAS or ST)</td>
<td>No</td>
<td>From $12,000</td>
<td>Support twisted pair and 830-nm fiber.</td>
</tr>
<tr>
<td>Network Systems Corp</td>
<td>FDDI concentrator</td>
<td>Standalone chassis</td>
<td>No</td>
<td>No</td>
<td>SNMP</td>
<td>16</td>
<td>150W</td>
<td>MIC or ST</td>
<td>ANTC</td>
<td>$3000 (chassis and motherboard) $2200 (2-port board)</td>
<td>Optional optical-bypass switch.</td>
</tr>
<tr>
<td>Summit Microsystems Corp</td>
<td>smFD-AT301</td>
<td>ISA bus boards</td>
<td>No</td>
<td>NA</td>
<td>Onboard SMT firmware</td>
<td>12M</td>
<td>10W</td>
<td>ST</td>
<td>ANTC</td>
<td>$12,900 (DAS plus four M ports) $6950 (4-M-port card)</td>
<td>Mapped to the ISA bus I/O space.</td>
</tr>
<tr>
<td>Synoptics Communications Inc</td>
<td>3000-05</td>
<td>Standalone chassis</td>
<td>Optional</td>
<td>Yes</td>
<td>SNMP (on-board SMT firmware)</td>
<td>40 SAS ports, 1 A/B port</td>
<td>480W</td>
<td>MIC</td>
<td>No</td>
<td>$4495 (housing) $14,995 (network management module) $7495 (4-M-port FDDI card) $4995 (4-M-port STP card)</td>
<td>Backplane accepts cards for connection to FDDI, Ethernet, and Token Ring modules. Optical bypass support. Three MAC sublayers permit dual homing to identify redundant links.</td>
</tr>
</tbody>
</table>

Notes: 1. NA=not applicable; ANTC=Advanced Networking Test Center; UNH=University of New Hampshire. 2. See box, “Glossary of FDDI terms,” for definitions of other abbreviations.
A question for designers who aren't yet using high-performance \( \mu \)PLDs.

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Ever feel like your system designs aren't quite up to speed, so to speak? It's probably not your fault. Because PLDs have typically forced designers to sacrifice performance to achieve higher integration.

But not any more.

Now, with Intel's \( \mu \)PLD family of programmable logic devices, you can finally achieve the higher integration you need—with the low total propagation delay you want.

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We'll send you everything you need to know about how to improve system performance. Without delay.
FDDI stations

Routers are more versatile than bridges: They also perform packet fragmentation and reassembly, packet control, and priority routing. In some cases, both bridge and router functions are appropriate for internetworking. In these cases, a hybrid bridge-router can provide routing services for two or more network-layer protocols or can implement a transparent datalink connection.

Table 3—Representative FDDI internetworking products

<table>
<thead>
<tr>
<th>Company</th>
<th>Model</th>
<th>Product description</th>
<th>Network Support</th>
<th>Power</th>
<th>Inter-operability tests¹</th>
<th>Price</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Equipment Corp</td>
<td>DEC bridge Bridge Ethernet, Appletalk</td>
<td>390W</td>
<td>ANTC, UNH</td>
<td>$25,000 to $45,000</td>
<td>Supports dual-homing to identify redundant links. Supports Internet protocol fragmentation. Self learning for as many as 4000 addresses. Supports spanning tree algorithm.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fibercom Inc</td>
<td>Ring Master 7200 Bridge Token Ring, Ethernet, DECnet, Novell</td>
<td>NA²</td>
<td>NA</td>
<td>$15,000</td>
<td>Maximum forwarding rate is 20,000 packets/sec. Filtering rate is 500,000 packets/sec. Supports Internet Protocol fragmentation. Self learning for as many as 4000 addresses. Supports spanning tree algorithm.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>In-net Corp</td>
<td>Fiber Talk 5000 Bridge Token Ring, Ethernet, DECnet</td>
<td>360W</td>
<td>ANTC</td>
<td>$17,500</td>
<td>Down-line loadable across networks. Filtering rate is 100,000 packets/sec. Forwarding rate is 8000 packets/sec.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FiberTalk 3000 Channel Bridging Unit Gateway Ethernet</td>
<td>360W</td>
<td>ANTC</td>
<td>$35,000</td>
<td>Down-line loadable across networks. Connects an IBM 360/370 mainframe computer to an FDDI ring. Software provides Telnet Virtual Terminal, File Transfer Protocol, and Electronic Mail services.</td>
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<td>500W</td>
<td>ANTC</td>
<td>$30,000</td>
<td>400-Mbps, 6-card backplane. Ethernet forwarding rate is 15,000 packets/sec/port. Supports the Spanning Tree Algorithm. Dynamically learns packet addresses.</td>
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<td>Bridge-router Ethernet, DECnet, Appletalk, Novell, T1, T3</td>
<td>500W</td>
<td>ANTC</td>
<td>$23,000</td>
<td>FDDI-to-FDDI bridge. Single-board chassis. Ethernet forwarding rate is 15,000 packets/sec/port. Supports the Spanning Tree algorithm. Dynamically learns packet addresses.</td>
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<td>6800 Family</td>
<td>Bridge-router Ethernet, DECnet, Appletalk, Novell, T1, T3</td>
<td>500W</td>
<td>ANTC</td>
<td>$46,000</td>
<td>Supports the Spanning Tree algorithm. Deletes undeliverable packets on the network after a preset period. Dynamically learns packet addresses. 800 Mbps, 16-card backplane.</td>
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<td>Synemetics Inc</td>
<td>LANplex 5004 Bridge-concentrator Ethernet, Token Ring</td>
<td>NA</td>
<td>ANTC, UNH</td>
<td>$25,500</td>
<td>Backplane has three FDDI paths, three Token Ring paths, three Ethernet paths, and a VMEbus that operate in parallel. Backplane accepts 12 plug-in modules. Connects as many as 24 Ethernet segments to an FDDI network. Modules support line insertion.</td>
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<td>LANplex 5012</td>
<td>Bridge-concentrator Ethernet, Token Ring</td>
<td>NA</td>
<td>ANTC, UNH</td>
<td>$32,900</td>
<td>Backplane has three FDDI paths, three Token Ring paths, three Ethernet paths, and a VMEbus path that operate in parallel. Backplane accepts 12 plug-in modules. Connects as many as 24 Ethernet segments to an FDDI network. Modules support line insertion.</td>
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Notes: 1. ANTC=Advanced Networking Test Center; UNH=University of New Hampshire. 2. NA=not applicable.

EDN October 1, 1991
It's no bigger than this ad (6U VMEbus to be exact). It doesn't suck power like less efficient controllers. It's RISC-based for super performance. It connects single or dual attached stations from a single VME slot. It supports a variety of media, from fiber to twisted pair. It's ANSI X3T9 FDDI standard compliant. It's certified by the Advanced Networking Test Center™ and the University of New Hampshire Interoperability Lab (Interphase is a charter member of both).

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Because FDDI is a fairly new LAN standard and multiple versions of the SMT function exist, the issue of interoperability is a concern. To ensure that FDDI stations from various vendors operate together properly, two groups are testing these FDDI products. Both the Advanced Networking Test Center, which Advanced Micro Devices sponsors, and the University of New Hampshire (Durham, NH) have test centers that run a suite of tests on vendor products they connect to an FDDI cable installation. The test centers try to ensure that there is one worldwide FDDI rather than multiple versions that don't interoperate.

If you already have an FDDI LAN installed and need an analyzer to troubleshoot the network in real time, Digital Technology Inc offers the Lanhawk-5700 Network Analyzer family. The portable 5733 and 5732 analyzers cost $28,300 to $50,000 and passively couple into the ring. The analyzers monitor, analyze, and collect data on FDDI networks. They also let you collect traffic statistics to evaluate ring performance and maximize ring utilization.

Nice—but expensive

The high cost of FDDI networks necessitates a wait-and-see attitude, but if projected trends for the 1990s pan out, network administrators may soon be upgrading existing LANs to the 100-Mbps standard. For example, PCs are emerging that exceed the power of

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**Manufacturers of FDDI products**

For more information on FDDI products such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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FDDI stations

The FDDI chip set from National Semiconductor implements the VCOM 100 VMEbus node controller. The SBE Inc board has a microprocessor unit and enough dynamic RAM to execute SMT software as well as the network- and transport-layer protocols.

80386-based computers. These PCs can manage a sea of documents and images that were traditionally the province of mainframes and minicomputers. Many applications must send the images and data to multiple locations on a LAN that has insufficient bandwidth to handle such bit-heavy traffic. In addition, multimedia applications, which integrate voice, data, and video, require a bandwidth way beyond what Ethernet and Token Ring networks can offer.

Many analysts say FDDI deployment will occur in multiple stages. In the early stages, FDDI backbones will interconnect smaller token-ring LANs that employ existing STP copper wiring for horizontal distribution. In the later stages, companies having intensive graphics and CAD communications needs will invest in a full fiber-optic LAN. The attendant drop in FDDI-product prices will encourage the widespread use of FDDI networks.

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The tools needed to develop applications that use digital signal processing (DSP) continue to improve. Now, a choice of operating systems and interfaces to host operating systems is making DSP available to more applications.

David Shear, Contributing Editor

This year there are many new DSP parts that add to the array of optional word formats, peripherals, and memory sizes. Naturally these family members are created to fit an existing or perceived market. In the past, if your application didn’t fit easily within an existing device, you were out of luck. Now, almost all DSP manufacturers have programs that will let you configure your own DSP µP. You can select from the available peripherals and memory options, or you can use an ASIC approach and put a gate array on the DSP chip.

Before DSP µPs can move into general use, however, it is essential that the functions of the algorithm developer and the end-user-application developer are separated. It is hard enough for algorithm developers to keep up with DSP algorithm development. It is rare for them to have the luxury of maintaining expertise in the creation of end-user applications that use the latest whiz-bang graphical user interface.

Likewise, the end-user-application developer must be able to concentrate on his applications. He must not be distracted with new algorithms and DSP µPs. That is the algorithm-developer’s domain.

Ideally, a DSP operates as if it is just another peripheral. When the end-user-application developer uses a hard disk, he doesn’t have to know how the data is stored on the disk. He just wants to use the hard-disk function: store data and retrieve it later.

Using a DSP must be the same. The algorithms must be available via a well-defined and standard method. If the end-user application needs a modem or a fax, speech or an image compressed, or whatever, the developer must be able to call the DSP as if he were sending data to a disk.

Right now, if an engineer creating an end-user application wants the application to use a DSP µP, he must devote a significant amount of effort (and time) to create the DSP portion of the project. At the same time, he has less time to develop his product. It doesn’t make sense—in terms of time and effort—for him to spend months, or more, getting up to speed in DSP.

New software interfaces

Soon, software interfaces between your DSP µP and the end-user application will let you develop DSP code that the end-user-application developer can use off the shelf. A separate group, or even a separate company, can use the DSP functions that you create. OSPA (Open-Signal Processing Architecture) from Spectron Microsystems (Santa Barbara, CA) and VCOS from AT&T are two current interfaces.

OSPA is a set of interfaces and protocols that lets
your DSP μP communicate with an end-user application. You must use the Spox real-time, multitasking operating system on the DSP μP.

Spox was introduced by Spectron Microsystems three years ago. It was first introduced to run on TI's TMS320C30. Spox has grown in acceptance to include Motorola's DSP96002, Analog Devices' ADSP-21020, and TI's TMS320C40.

Spox runs on the DSP μP while the Spox Server runs on the host. The DSP functions that you write interface to the end-user application via the Spox Server. Host- and DSP-μP independence is achieved if you create OSPA-compatible DSP programs and use the Spox server. Your DSP μP can be transported to any computer that has a Spox Server for the host operating system.

Separate the experts

David Wong, president of Spectron Microsystems, says that Spox and OSPA separate the functions of the end-user-application developer and the algorithm developer (Fig 1). By using high-level commands and data-stream conventions described by OSPA, you can develop the application software and the real-time DSP functions independently.

Even if the end-user application moves to another host computer, the Spox server for the new host operating system lets you transport your DSP μP. You can also use more powerful DSP μPs as they become available to create more capable DSP solutions. The end-user-application developer will then be able to use the more capable DSP solution without modifying his code.

The near industry-wide acceptance of OSPA and Spox places them in a great place to become the standard. The host independence of OSPA and the DSP-μP independence of Spox further strengthens their positions.

VCOS is another approach to separate your efforts from the end-user application. Frank Ferro, DSP Marketing Manager at AT&T, says that VCOS is not intended to be an operating system that is all things to all people. It is an approach to implement AT&T's 32-bit floating-point DSP3210 on the motherboard of a PC or workstation.

The major emphasis of VCOS is to make the hardware implementation of the DSP3210 inexpensive and the software easy to create. The DSP3210 interfaces directly to Motorola and Intel μP buses and shares the host memory. This approach does away with the cost of high-speed static RAM (SRAM).

The VCOS kernel is a small program (fewer than 400 32-bit words) that runs on the DSP μP. It handles execution control, caching, and buffer I/O. The VCOS Application Server runs on the host, loads and links the DSP tasks, and performs all memory-management functions. A debugger and library are also included to ease development.

The DSP program is loaded into the internal RAM of the DSP μP. The internal RAM is used to run the program, usually in sections. The DSP μP has access to the host memory where it can store data. Taking over the slower host bus reduces the performance of both the DSP μP and the host μP. But AT&T claims that the performance of both is not reduced significantly.

Two workstations already have DSP μPs on the motherboard: Next Inc's Next and Silicon Graphics' Iris Indigo computers both have Motorola's DSP56001.

Many chip vendors feel that it is too early to place the DSP μP on the motherboard, and that add-in boards should be used for some time. The workstation market will see DSP chips on the motherboard first. The workstation market traditionally has proprietary systems and can make its own decisions about how to implement a DSP μP. Apple also has considerable control over what will end up on the motherboard of its Macs. The PC market is different—with so many different manufacturers, it will take some time before a consensus is reached.

Acronyms used in this article and in the chip directory

ADC—analog-to-digital converter
ALU—arithmetic and logic unit
ASIC—application-specific integrated circuit
CMOS—complementary metal-oxide semiconductor
CPU—central processing unit
CQFP—ceramic quad flat pack
DAC—digital-to-analog converter
DIP—dual in-line package
DMA—direct memory access
DSP—digital-signal processing
EPROM—erasable PROM
FFT—fast Fourier transform
FIFO—first in, first out
FIR—finite-impulse response
IC—integrated circuit
I/O—input-output
JTAG—Joint Test Action Group
μP—microprocessor
NMOS—n-type metal-oxide semiconductor
OSPA—Open-Signal Processing Architecture
PC—personal computer
PGA—pin-grid array
PLCC—plastic leaded chip carrier
PLL—phase-locked loop
PQFP—plastic quad flat pack
PROM—programmable read-only memory
QFP—quad flat pack
RAM—random-access memory
ROM—read-only memory
SOP—small-outline package
Spox—real-time multitasking operating system
EDN's DSP-chip directory

It is doubtful that the next year will bring a DSP µP to the mother board of a majority of computers. But watch for a number of announcements along these lines. Within a few years, applications will require these high speed devices.

DSP in real time

If you need a real-time operating system that can run directly on the DSP µP in embedded applications, you have the choice of Spox for floating-point chips and VRTX32 for Motorola's fixed-point DSP56001. Bryant Wilder, Motorola's DSP operations manager, says that VRTX32/DSP56000 from Ready Systems (Sunnyvale, CA) is the only real-time operating system available for fixed point DSP µPs. It is basically the same as the other versions of VRTX32, which have been available on a number of µPs for many years. Users of VRTX32 can use their existing tools and experience and just add the DSP56000 version.

High-level-language options grow

Whichever operating system you choose, you will still be able to take advantage of the productivity gains from using a high-level language. By far, the most common high-level language for DSP µPs is C. Nearly all of the floating-point DSP µPs have an ANSI C compiler. You can also use an Ada compiler. Eric West, C40 Marketing Manager at TI, says that the company plans to develop a Fortran compiler for the C30 and C40.

C is not standing still. ANSI C (more appropriately called Standard C) allows program transportability. But there are an ever growing array of C variations, Numerical C, Concurrent C, C++, C*, and GNU C, to name a few.

Numerical C is intended to make C more applicable to calculation-intensive applications, like DSP. Tim Counihan, strategic marketing manager for DSP at Analog Devices, says that Analog Devices is actively supporting Numerical C. He feels that the standard is well enough defined to produce a product. He does admit that Analog Devices will probably have to make some changes by the time a standard is available. The Numerical C Extensions Group (NCEG) is working within ANSI (X3J11.1) on a technical report, not a standard, so an actual standard is still in the future.

Other DSP-µP manufacturers are not supporting Numerical C yet. They are waiting for either their customers to request it or a standard to be available. TI says the company will definitely support Numerical C when it becomes a standard.

All of the C compilers for DSP µPs claim to be optimizing compilers. It is difficult to determine how well the optimizing compilers will work in your application. You will often have to optimize some sections of your high-level code by hand. On one recent project, a DSP consulting group was able to prototype the system with C code in a matter of hours. This C version proved the concept, but would only run at 12 frames/sec. The customer needed 15 frames/sec. The group spent three months optimizing the code to meet the 15 frames/sec requirement.

The Comdisco (Foster City, CA) DSP Procoder is an option to the company's Signal Processing Worksystem (SPW). The SPW is a block-diagram-based devel-

![Diagram](image)

Fig 1—Separating the DSP function developer from the end-user application developer lets each expert concentrate on his speciality.
opment system. The DSP Procoder will take a block
diagram of a DSP algorithm and create assembly code.
Comdisco claims the resulting code is production-
quality. The DSP Procoder presently uses Motorola’s
DSP56001. Other fixed-point DSP µPs will be used in
the future.

Multiprox is another option for SPWs used to parti
tion a block diagram to run on multiple processors.
When used with the Code Generation System, you can
automatically produce C code for multiple floating-
point DSP µPs. The generated code includes the inter-
processor-communication code to pass data between
the processors. The TMS320C30, TMS320C40, and
DSP96002 are supported.

**Need quadruples performance every 18 months**

As soon as you finish designing a product, you will
often be called upon to start the next generation. Rick
Rinehart, floating-point DSP marketing manager at
Texas Instruments, points out that the market window
today averages about 18 months. The market window
is the length of time from when a company introduces
a product until they begin ramping down production.
Each new generation of a product needs about a four
times increase in performance to remain competitive.
The improvements in design and processes used to
build ICs will double performance every three years.
Rinehart feels the only way to meet the quadrupling
performance needs of their customers is with parallel
processing.

Making products that can see, talk, and listen is
difficult. Much of that type of development is possible
today, but it requires expensive parallel processing
systems. Prices will continue to drop until today’s ex-

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ADSP2100 FAMILY

16-BIT FIXED-POINT CMOS DSP µP

AVAILABILITY: The ADSP2100/A, 2101, 2102, 2106, 2111, 2112 are in production now. The 21msp50 and the 21msp51 are now sampling.

COST: ADSP2100, $45 (1000); 2101, $36 (1000); 2102, $34 (5000); 2105, $9.90; 2106, $11.39 (25,000); 2111, $48 (1000); 2112, $46 (5000); 21msp50, $57 (1000); 21msp51, $40 (25,000).

SECOND SOURCE: None.

DESCRIPTION: The ADSP2100 family ranges from the 2100 with no on-chip memory and an off-chip Harvard architecture to the 21msp51 with program and data ROM, data RAM, and peripherals, including an analog-to-digital and digital-to-analog converter and host interface port on-chip. The data memory has a 16-bit width, but the program memory has a 24-bit word width to control the parallel operations. Low-voltage versions are now sampling.

FEATURES: 60-, 77-, 80-, 100-, 125-, and 167-nsec cycle-time versions.
Separate on-chip program and data buses. On-chip memory:
The 2100/A has no on-chip memory. The 2101 has a 2k x 24-bit program RAM and a 1k x 16-bit data RAM. The 2102 has a 2k x 24-bit program ROM or RAM and a 1k x 16-bit data RAM. The 2105 has a 1k x 24-bit program RAM and a 512 x 16-bit data RAM. The 2106 has a 1k x 24-bit program RAM or ROM and a 512 x 16-bit data RAM. The 2111 and 21msp50 have a 2k x 24-bit program RAM and a 1k x 16-bit data RAM. The 2112 has a 2k x 24-bit program ROM or RAM and a 1k x 16-bit data RAM. The 21msp51 has a 2k x 24-bit program RAM, 2k x 24-bit program ROM, and a 1k x 16-bit data RAM.

Separate program and data buses brought off the chip only on the 2100/A. All other parts combine program and data buses off the chip.

Off-chip memory capacity: The 2100/A has 32k x 24-bit program and 16k x 16-bit data memory capacities. All others have 16k x 24-bit program and 16k x 16-bit data memory capacities.

Boot memory controller loads program from external byte-wide EPROM (except 2100/A).

On-chip peripherals: The 2100/A has no on-chip peripherals. The 2101 and 2102 have two serial I/O ports and a timer; the 2105 has one serial I/O port and a timer. The 2111/2 have two serial I/O ports, a timer, and a host interface port. The 21msp50 has two serial I/O ports, a parallel I/O port, a timer, and a 16-bit ADC/DAC (linear codec).

Multiplier/accumulator accepts 16-bit fixed-point input and creates 32-bit fixed-point results within a 40-bit accumulator. 16-bit ALU. 32-bit bidirectional barrel shifter. 40-bit accumulator.

Multiplier/accumulator, ALU, and shifter are separate blocks connected by the 16-bit R-bus and the data bus.

Zero-overhead looping.

Only the 2100/A has a 16 x 24-bit on-chip cache.

Direct, indirect, immediate, circular, and bit-reversal addressing modes.

Two address generators.
No on-chip DMA. Serial port and codecs have auto buffer, which transparently transfers data to and from memory.

16-level hardware stack. Status stack limits interrupts to four levels of nesting on the 2100/A, seven levels on the others.
Four external interrupts on the 2100/A; three external interrupts on others.

The 2100/A has only hardware wait states. Others have only software-programmable wait states.

No on-chip emulation port.

Only the 21msp50 has power-down mode to CMOS standby levels. The 2101, 2105, 2106, 2111, and 2112 have an idle mode, which lowers power until an interrupt is detected.

Packaging: 2100/A, 100-pin PQFP and 100-pin PGA. 2101/2, 68-pin PGA and 88-pin PLCC. 2105/6, 68-pin PLCC. 2111, 100-pin PQFP and 100-pin PGA. 21msp50/1, 100- and 132-pin PQFPs, 144-pin PGA.

HARDWARE

Full-featured in-circuit emulator.
Low-cost in-circuit emulator board.
Demo board.
Evaluation packages.
Third-party support: Contact Analog Devices for a list of third-party vendors.

SUPPORT

C compiler.
Simulator.
Macroassembler/linker.
Application libraries.
Upcoming Numerical C.

SOFTWARE

Full-featured in-circuit emulator.
Low-cost in-circuit emulator board.
Demo board.
Evaluation packages.
Third-party support: Contact Analog Devices for a list of third-party vendors.

EDN October 1, 1991
**16-BIT FIXED-POINT CMOS DSP µP**

**AVAILABILITY:** The DSP16, 16A, and 16C are in production. The DSP1610 and 1616 are sampling with production starting in 1992.

**COST:** DSP16, $9.60; DSP16A, $16.70; DSP1610, $125; DSP1616, $35 (10,000).

**SECOND SOURCE:** None.

**DESCRIPTION:** The members of the DSP16 family have long been the fastest fixed-point DSP chips. The DSP16A has a 25-nsec cycle time. The DSP16A and DSP16C also have the largest on-chip program memory at 12k x 16 bits. Many applications that would require external ROMs with other DSP chips can fit within the DSP16 family’s on-chip memory. The DSP16C has an A/D and a D/A converter on chip. The DSP16C also has a 4-pin JTAG interface, which assists in testing tightly packed boards. A 3.3V version of the DSP16A is available. The DSP1610 and 1616 are enhanced versions intended for digital cellular telephones.

**FEATURES:** 25-, 33-, 55-, and 75-nsec cycle-time versions. The DSP16C has 38.5- and 76.9-nsec cycle-time versions. Separate on-chip program and data buses.

On-chip memory: The DSP16 has a 2k x 16-bit program ROM and a 512 x 16-bit data RAM. The DSP16A and 16C have a 12k x 16-bit program ROM and a 2k x 16-bit data RAM. The DSP1610 has a 512 x 16-bit boot ROM and an 8k x 16-bit dual-port RAM. The DSP1616 has a 12k x 16-bit ROM and a 2k x 16-bit dual-port RAM.

The program ROM on the DSP16 can be replaced with as many as 64k words of external memory.

The program ROM on the DSP16A and 16C can be replaced or augmented with as many as 64k words of external memory.

The DSP1610/1616 can access two external 64k address spaces.

Parallel and serial I/O port.

The DSP16C has an on-chip codec.

The DSP1610 and 1616 have an on-chip timer.

The multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 36-bit accumulator.

32-bit ALU

Only the DSP1610 and 1616 have a 36-bit barrel shifter and bit-manipulation instructions.

Two 36-bit accumulators.

Zero-overhead cache looping as many as 127 times.

15-word instruction cache.

Immediate, register-indirect, and circular addressing modes.

No on-chip DMA.

Single-level hardware stack is software expandable into main memory.

One external interrupt.

DSP1610 has hardware and software wait states. DSP1616 has software wait states.

DSP1610 and 1616 have on-chip emulation ports.

The DSP16A, 16C, 1610, and 1616 have power-down mode.

The DSP1616 will run from 3.3 to 5V.

Packaging: DSP16 and 16A, 84-pin PLCC or 133-pin PGA.
DSP16C, 100-pin PQFP.
DSP1610, 132-pin PQFP.
DSP1616, 100-pin PQFP or PLCC.

**HARDWARE**

Development system with in-circuit emulation.

Evaluation board that plugs into a PC.

**SOFTWARE**

Assembler/linker.

Simulator.

Application library.

Third-party support includes filter-design packages. Contact AT&T for a list of third-party vendors.
**DSP56156**

**16-BIT FIXED-POINT CMOS DSP µP**

**AVAILABILITY:** Now.

**COST:** 40 MHz, $104.50 (180); 60 MHz, $135.85 (180).

**SECOND SOURCE:** None.

**DESCRIPTION:** The 56156 is a 16-bit subset version of the 56001. It is intended for cellular telephone and other communication applications. It has a built-in codec and phases-locked loop. Development tools are similar to the 56001 and the 96002. The 56156 has been available to select customers and is now moving into general availability.

**FEATURES:**
- 33- and 50-nsec cycle-time versions.
- Three address buses and three data buses.
- On-chip memory includes a 2k x 16-bit program RAM and a 2k x 16-bit data RAM.
- ROM-based version (DSP56156ROM) contains a 12k x 16-bit program ROM.
- Separate external program and data memory spaces. Each can address 64k x 16-bit locations.
- Can load program from external EPROM.
- Asynchronous and synchronous serial I/O ports.
- Parallel port can interface with a host µP.
- Has on-chip PLL.
- On-chip, sigma-delta voice-band codec.
- Multiplier accepts 16-bit data and returns 40-bit results to 40-bit accumulator.
- ALU performs arithmetic operations on 40-bit data and logical operations on 16-bit data.
- No barrel shifter.
- Two 40-bit accumulators.
- Zero-overhead looping.
- Immediate, direct, indirect, circular, and bit-reversed addressing modes.
- No DMA support.
- Two external vectored interrupts.
- Has on-chip emulation.
- Low-power mode.
- Packaged in a 112-pin CQFP.

**HARDWARE**

Application-development system includes in-circuit emulator.
Contact Motorola for a list of third-party vendors.

**SUPPORT**

Macro cross-assembler.
Linker.
Application-development board.

**SOFTWARE**

EDN October 1, 1991
24-BIT FIXED-POINT CMOS DSP µP

AVAILABILITY: Now.
COST: DSP56001: 27 MHz, $52.00 (180) and 33 MHz, $62.40 (180); DSP56002: in PGA, $166 (180) and in CQFP, $91 (180).
SECOND SOURCE: None.

DESCRIPTION: The 56001 provides one 24-bit data word and two 56-bit accumulators. This extended precision lets the chip process 16-bit data more easily than the 16-bit machines can. The 24-bit word width eases scaling, and the 56-bit accumulators prevent overflow. The 24-bit data width suits digital audio applications. The 56002 is a high-speed, low-power, low-voltage version of the 56001, which is 100% software compatible, and includes a PLL and on-chip emulation.

FEATURES: 60- and 74-nsec cycle-time versions.
Three address buses and four data buses.
Separate address buses for program ROM and the two data RAMs.
Separate data buses for program ROM, the two data RAMs, and global data.
On-chip memory includes a 512 x 24-bit program RAM, a 32 x 24-bit boot ROM, dual 256 x 24-bit data RAMs, and dual 256 x 24-bit data ROMs.
ROM-based version (56000) available.
Three separate memory spaces (X, Y, and P). Each can address 64k x 24-bit locations.
Can load program from external EPROM.
Asynchronous 8-bit serial I/O port.
Synchronous 8- to 24-bit serial interface.
Parallel port can interface with a host µP.
56002 has on-chip PLL.
Multiplier accepts 24-bit data and returns 48-bit results to 56-bit accumulator.

ALU performs arithmetic operations on 56-bit data and logical operations on 24-bit data.
No barrel shifter.
Two 56-bit accumulators.
Zero-overhead looping.
Immediate, direct, indirect, circular, and bit-reversed addressing modes.
Two address generators.
No DMA support.
System stack is 15-levels deep, but can be read by program to extend stack into main memory.
Two external vectored interrupts on 56001, three on 56002.
Hardware and software-programmable wait states.
Only the 56002 has on-chip emulation.
Low-power mode.
56002 operates on 2.0 to 5.5V power supplies.
Packaging: 56001, 132-pin CQFP or 88-pin PGA. 56002, 132-pin PGA, CQFP, or PQFP.

HARDWARE

APPLICATION-DEVELOPMENT SYSTEM INCLUDES IN-CIRCUIT EMULATOR.
CONTACT MOTOROLA FOR A LIST OF THIRD-PARTY VENDORS.

SUPPORT

SOFTWARE

C COMPILER.
GNU C COMPILER AND SOURCE-LEVEL DEBUGGER.
MACRO CROSS-ASSEMBLER.
LINKER/LIBRARY.
SIMULATOR.
CODE TRANSLATOR FROM TMS320C10 TO 56001.
THIRD-PARTY SUPPORT INCLUDES FILTER-DESIGN SOFTWARE, AND VRTX32/DSP56001 REAL-TIME OPERATING SYSTEM.
**μPD77C25**

**16-BIT FIXED-POINT DSP μP**

**AVAILABILITY:** The 77C25 is available now. A 3V operation version is planned for 1992.

**COST:** 77C25, $9 (5000); 77P25, $45 (1000); 77P25C, $20 (1000).

**SECOND SOURCE:** Oki Semiconductor (Sunnyvale, CA) also makes the 7720.

**DESCRIPTION:** The 77C25 is an upgrade of the 7720, which was one of the first successful DSP chips. The basic architecture is out of date and its memory can’t be expanded off chip. The manufacturer says there is still interest in new 77C25 designs because of the chip’s low cost. The 77P25 is an EPROM version of the 77C25. The 77P25C is a one-time-programmable version.

**FEATURES:**
- 100- and 122-nsec cycle time.
- Single address bus only for program memory.
- Pointers address data memory.
- Single data bus for both program and data.
- On-chip memory: The 77C25 has a 2k x 24-bit program ROM, a 256 x 16-bit data RAM, and a 1k x 16-bit data ROM. The 77P25 has the same memory as the 77C25, but replaces ROM with EPROM.
- No external memory expansion.
- One 8-bit serial I/O port.
- Parallel I/O port.
- Multiplier accepts 16-bit fixed-point data and produces 31-bit fixed-point results within two 16-bit accumulators.
- 16-bit ALU.
- No barrel shifter.
- Two 16-bit accumulators.
- No zero-overhead looping.
- No address generators.
- No on-chip DMA controller.
- 4-level stack stores the program counter during subroutines and interrupts and is not expandable.
- Single external interrupt.
- No wait states.
- No on-chip emulation port.
- No low-power mode.
- Packaged in 28-pin DIP, 28-pin PLCC, 44-pin PLCC, and 32-pin SOP.

**HARDWARE**

**SUPPORT**

**SOFTWARE**

Evaluation kit for application development also functions as in-circuit emulator.

Assembler/linker.

Third-party simulator available.
24-BIT FIXED-POINT CMOS DSP \( \mu P \)

**AVAILABILITY:** 100- and 122-nsec versions available now.

**COST:** $27 (1000).

**SECOND SOURCE:** None.

**DESCRIPTION:** The 77220 is a scaled-down version of the 32-bit floating-point 77230. The chip size and pin count are reduced by using 24-bit data and removing the floating-point exponent hardware. The 24-bit word width suits the digital audio market. The instruction set is a subset of the 77230 and is source-code compatible with the floating-point device. The vendor says the 77220’s architecture is optimized for adaptive filter applications. The 77P220R EPROM version and the 77P220L one-time-programmable version are for prototyping and low-volume applications.

**FEATURES:**
- 100- and 122-nsec cycle-time versions.
- Separate on-chip program and data buses.
- On-chip memory includes a 2k x 32-bit program ROM, dual 256 x 24-bit data RAMs, and a 1k x 24-bit data ROM.
- Off-chip memory can be expanded to 8k x 32-bit program memory and 8k x 24-bit data memory.
- One serial I/O port.
- Parallel I/O port can be used as host \( \mu P \) interface.
- Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results within a 47-bit accumulator.
- 47-bit ALU.
- 47-bit bidirectional barrel shifter.

**HARDWARE SUPPORT**

Evaluation kit and PC evaluation board.

**SOFTWARE**

Assembler/linker.
Simulator.
ST18930/31/32/42

16-BIT FIXED-POINT CMOS DSP µP

AVAILABILITY: Now.

COST: ST18930, $15 (10,000); ST18931, $75 (100); ST18942, $35 (10,000); ST18R942, $80 (100). The ST18932 is only available for ASIC designs.

SECOND SOURCE: None.

DESCRIPTION: The ST18 family consists of four devices. The ST18930 and 31 are CMOS versions of the NMOS original with a few enhancements and twice the speed. The ST18932 is a core for custom DSP µPs. The CMOS ST18942 offers further enhancements in its arithmetic capabilities, addressing modes, and I/O functions. All family members can operate on complex and double-precision data. The ST18932 and 42 have a 32-bit ALU and 16-bit data buses.

FEATURES: The ST18930 and 31 have 80-nsec cycle times. The ST18932 has a 50-nsec cycle time. The ST18942 has a 100-nsec cycle time.

Two address buses and four data buses on chip.

On-chip memory: The ST18930 has a 3k x 32-bit program ROM, a 192 x 16-bit data RAM, a 128 x 16-bit data RAM, and a 512 x 16-bit data ROM. The ST18931 has the same memory as the ST18930, but without ROM. The ST18942 has a 4k x 32-bit program ROM, two 256 x 16-bit data RAMs, and a 512 x 16-bit data ROM. The ST18R942 is a ROMless version of the ST18942 and has two 256 x 16-bit and one 128 x 16-bit data RAMs.

64k x 32-bit external program memory (except ST18930). The ST18930 and 31 have 4k x 16-bit external data memory space. The ST18932 has 8k x 16-bit external data memory. The ST18942 and ST18R942 have 64k x 16-bit external memory.

Only the ST18942 has both a serial I/O port and a parallel I/O port.

ST18932 and 42 multipliers accept 16-bit fixed-point data and return 32-bit fixed-point results to 32-bit accumulator. The ST18930 and 31 return 16-bit results.

In complex mode, the multiplier multiplies two complex numbers in two cycles.

HARDWARE

16-bit ALU in ST18930 and 31. 32-bit ALU in ST18932 and 42.
16-bit bidirectional barrel shifter in ST18930 and 31. 32-bit bidirectional barrel shifter in the ST18932 and 42.
ST18930 and 31 have two 16-bit accumulators. ST18932 and 42 have four 32-bit accumulators.
Zero-overhead looping.
Immediate, direct, indirect, and circular addressing modes.
ST18942 has on-chip DMA.
ST18930 and 31 have a 1-level, ST18932 has a 2-level, and ST18942 has an 8-level hardware stack for interrupts and subroutines. All can be expanded into main memory with software.
Three external interrupts on the ST18930 and 31 and eight on the ST18932 and 42.
Hardware and software-programmable wait states. Only the ST18932 has on-chip emulation port.
Low-power mode.
Packaging: ST18930, 48-pin DIP and 52-pin PLCC. ST18931, 124-pin PGA. ST18942, 160 PQFP. ST18R942, 160 PQFP and 144-pin PGA.

SUPPORT

Software

Macroassembler/linker. Simulator.

EDN October 1, 1991
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16-BIT FIXED-POINT CMOS DSP µP

**AVAILABILITY:** The C10, C15, C16, C17, E14, E15, E17, P15, P17, P14, LC15 (3.3V), and LC17 (3.3V) are available now. The C14 will be available in the fourth quarter of 1991.

**COST:**
- C10 (20 MHz), $4.90; C10 (25 MHz), $6; C14, $9; E14, $45; P14, $22; C15 (20 MHz), $7; C15 (25 MHz), $8; E15 (20 MHz), $35; E17 (25 MHz), $45; P15, $20; C16, $9; E17, $38; P17, $20 (1000).

**SECOND SOURCE:** Microchip Technology (Chandler, AZ) for the C10, C14, and E14. No second source for other parts.

**DESCRIPTION:** This first generation of the vendor's DSP family was introduced in 1982. Although this family is difficult to use and slower than similar devices, the chips' cost—which has dropped to $3 in high volumes—and the large body of associated software and expertise will keep this family going.

**FEATURES:**
- 114-, 160-, 200-, and 280-nsec cycle-time versions. Separate on-chip program and data buses.
- On-chip memory: The C10 has a 1.5k x 16-bit program ROM and a 144 x 16-bit data RAM. The C14, C15, and C17 have a 4k x 16-bit program ROM and a 256 x 16-bit data RAM. The E14, E15, and E17 have a 4k x 16-bit program EPROM and a 256 x 16-bit data RAM. The C16 has an 8k x 16-bit program ROM and a 256 x 16-bit data RAM. P1X versions are one-time programmable.
- Program and data buses are combined off chip.
- 4k x 16-bit total external memory, except the C16, which has 64k x 16-bit external memory, and the C17, which has no external memory.
- On-chip peripherals: The C10, C15, and C16 have parallel I/O. The C14 has serial and parallel I/O. The C17 has two serial I/O ports, parallel I/O, and a compander.

**MULTIPLIER:** Accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.
- 32-bit ALU.
- 16-bit left barrel shifter.
- Single 32-bit accumulator.
- No zero-overflow looping.
- No DMA.
- 4-level hardware stack except the C16, which has an 8-level hardware stack.
- Single external interrupt.
- No wait states.
- No on-chip emulation.
- LC1X devices operate at 3.3V.

**PACKAGING:**
- C10, 40-pin DIP or 44-pin PLCC.
- C14, 40-pin DIP or 44-pin PLCC.
- P15, 40-pin DIP or 44-pin PLCC.
- C16, 64-pin QFP.
- C17, 40-pin DIP or 44-pin PLCC.

**HARDWARE SUPPORT SOFTWARE**

- In-circuit emulator.
- Evaluation module.
- Software-development system.
- In-circuit emulator.
- Evaluation module.
- Software-development system.
- Many third-party support tools. Contact Texas Instruments for a list of third-party vendors.
- Assembler/linker.
- Simulator.
- Application library.
- Many third-party support tools.

Texas Instruments Inc
Semiconductor Group, SC-001
Box 809066
Dallas, TX 75380
(800) 336-5236, ext 700
Circle No. 678

Newer family members have additional memory and peripheral options. EPROM (TMS320E1X) and one-time-programmable (TMS320P1X) versions are also available. 3.3V versions of the C1X family are now available.
16-BIT FIXED-POINT CMOS DSP µP

**AVAILABILITY:** The C25, C26, and E25 are available now. The C50 and C51 are sampling now and will be in production in the fourth quarter of 1991.

**COST:** C25 (33 MHz), $14; C25 (40 MHz), $15; C25 (50 MHz), $17; E25, $55; C26, $16; C50, $130; C51, $40 (1000).

**SECOND SOURCE:** None.

**DESCRIPTION:** These chips make up the second generation of the vendor’s DSP family. They offer higher performance than the first-generation chips and are easier to use. For many applications, the C25’s price has dropped to a point where the chip is replacing the C1X. The C5X parts are enhancements to the C25. They use the same basic core architecture as the C25, but have double the performance level, additional on-chip peripherals, and expanded memory. An EPROM version of the C25, the E25, is also available.

**FEATURES:** The C2X chips come in 78-, 98-, and 125-nsec cycle-time versions. The C5X chips come in 55- and 70-nsec cycle-time versions.

On-chip memory: The C25 has a 4k x 16-bit program ROM and a 544 x 16-bit data RAM. The C26 has a 1.5k x 16-bit program RAM with boot ROM to load programs from external memory and a 544 x 16-bit data RAM. The C50 has a 9k x 16-bit program/data RAM and a 1056 x 16-bit dual-access RAM. The C51 has an 8k x 16-bit program ROM, a 1k x 16-bit program/data RAM, and a 1056 x 16-bit dual-access RAM.

Program and data memory are combined off chip.

The C2X and C5X can address 64k x 16-bit programs and 64k x 16-bit data memories.

The C25 and C26 have one serial port each. The C5X has two serial ports.

Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.

32-bit ALU.

The C5X has a separate 16-bit parallel logic unit for manipulating bits without affecting the contents of the accumulator.

16-bit left barrel shifter.

Single 32-bit accumulator.

Next-instruction-repeat looping. Only the C5X has zero-overhead block looping.

Immediate, direct, indirect, and bit-reversal addressing modes. C5X also has circular addressing.

No DMA.

8-level expandable hardware stack.

C5X has a 1-level-deep shadow RAM, which stores some registers.

C2X has three external interrupts; C5X has five.

Hardware wait states. C5X also has software-programmable wait states.

The C5X has an on-chip emulation port.

The C2X is source-code compatible with the C5X.

The C5X has a JTAG interface.

The C25 and C26 have an idle mode. The C5X has a power-down mode.

Packaging: C25 and C26, 68-pin PGA or PLCC. C50, 132-pin QFP.

**HARDWARE SUPPORT SOFTWARE**

Both the C2X and C5X have an in-circuit emulator.

Both also have a software-development board for PCs.

Many third-party support tools. Contact manufacturer for a list of third-party vendors.

C compiler for both C25 and C5X.

Source-level debugger for C5X.

Assembler/linker.

Simulator.

Application library.

Many third-party support tools.
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32-BIT FLOATING-POINT CMOS DSP μP

**AVAILABILITY:** The ADSP21020 is available now.
**COST:** $147 (1000).
**SECOND SOURCE:** None.

**DESCRIPTION:** This device is the vendor’s first floating-point DSP μP. It has an off-chip Harvard architecture and is similar to the fixed-point 2100 family. On-chip emulation supported via a JTAG port. The device conforms to the IEEE-754 floating-point standard.

**FEATURES:**
- 40-, 50-, and 66-nsec cycle-time versions.
- One 32-bit and one 24-bit address bus.
- One 40-bit and one 48-bit data bus.
- Seven 40-bit additional buses in the CPU.
- Separate program, and data buses (off-chip Harvard Architecture).
- 4G x 40-bit external data memory and 16M x 48-bit external program memory.
- One 32-bit timer.
- IEEE-754 32-bit and 40-bit floating-point format.
- Multiplier accepts 32-bit and 40-bit floating-point data and returns 32-bit or 40-bit results. 32-bit fixed-point operands produce 64-bit fixed-point products. The multiplier also incorporates dual 80-bit fixed-point accumulators.
- ALU accepts 32-bit and 40-bit floating-point data and returns 32-bit or 40-bit results. 32-bit fixed-point operands produce 32-bit results.
- Parallel multiplier and ALU operate in single cycle.
- 32-bit bidirectional barrel shifter.
- 32 40-bit register-based accumulators.
- Zero-overhead looping.
- 32 x 48-bit instruction cache.
- Cache optimizes performance by selecting only 3-bus-operation instructions for storage in cache. Cache can be frozen to keep often-used instructions in cache.
- Register, direct, indirect, immediate, relative, circular buffer, and bit-reversed addressing modes. Two independent address generators.
- The hardware stack is 20 deep and can be expanded into main memory.
- Four external vectored interrupts.
- Four bidirectional I/O flags.
- Hardware and software programmable wait states.
- JTAG support of in-circuit emulation.
- Idle state for low-power mode.

**HARDWARE SUPPORT SOFTWARE**

**HARDWARE**
- Full-speed in-circuit emulator.
- Demo board for PCs.
- Evaluation package.
- Third-party support: Contact Analog Devices for a list of third-party vendors.

**SUPPORT**
- Optimizing ANSI C and Numerical C compilers.
- Source-level debugger for ANSI C and Numerical C.
- Simulator, assembler, linker, PROM splitter.
- Application libraries.
- Third-party support includes Spox, filter-design packages with code generation, and block-level algorithm development packages.
DSP32C/3210

32-BIT FLOATING-POINT CMOS DSP µ.P

AVAILABILITY: The DSP32C is available now. The DSP3210 is sampling now with production by the fourth quarter of 1991.

COST: DSP32C, $70 (1000). DSP3210, $50 (100,000).

SECOND SOURCE: None.

DESCRIPTION: The DSP32C has one of the simplest architectures of the 32-bit floating-point DSP chips. It uses a single 4M-word linear-memory space instead of the separate program and data memory common in other DSP chips. The single address bus and single data bus can be accessed as many as four times per cycle. Each internal memory can be accessed as many as two times per cycle. The DSP3210, along with the VCOS operating system, is intended for use on the motherboard of PCs and workstations, where it shares memory with the host.

FEATURES: 80- and 100-nsec cycle-time versions. Single address and data buses. Each can be accessed as many as four times per cycle to imitate separate buses. DSP32C has three on-chip 512 x 32-bit RAMs. Optional ROM-based DSP32C replaces one RAM with a 4k x 32-bit ROM. DSP3210 has two 1k x 32-bit RAMs and a 256 x 32-bit boot ROM.

The DSP32C can address as much as 4M x 32-bits of external memory. The DSP3210 can address 4 Gbytes of external memory. All memory is a general resource; both program and data can exist anywhere.

Data addressable as 8-, 16-, or 32-bit words. DSP3210 can load program from external EPROM. The DSP32C has on-chip serial and parallel I/O. The DSP3210 has serial I/O, timer, DMA controller, and a 32-bit bus interface that is compatible with Motorola and Intel µPs.

The serial I/O is a double-buffered port that allows concurrent input and output of 8-, 16-, 24-, or 32-bit data widths. The DSP32C has an 8- or 16-bit parallel I/O port that an external µP can control. Proprietary 32-bit floating-point format.

Single-cycle conversion to/from nonstandard DSP32 floating-point format from/to IEEE-754 floating-point format. Multiplier accepts 32-bit floating-point data and creates 45-bit floating-point results. Separate floating-point adder accepts 40-bit floating-point data and creates 40-bit floating-point results.

Fixed-point ALU accepts 16- or 24-bit data. Does not have a barrel shifter. Four 40-bit accumulators. Zero-overhead looping. As many as 2048 repeats of a block with a maximum size of 32 words. Immediate, memory-direct, register-direct, register-indirect, and bit-reversal addressing modes.

DMA can be used with both the serial I/O and the parallel I/O. No hardware stack. 1-level-deep shadow RAM of some registers. Two external interrupts. Hardware wait states. DSP3210 has software-programmable wait states.

No on-chip emulation port. Only the DSP3210 has a low-power mode. DSP32C packaged in a 164-pin PQFP, 133-pin PGA, or 68-pin PLCC (microcontroller version, no external memory).

HARDWARE

In-circuit emulator.
IBM PC-based development board.
VME bus-based development board.
Many third-party support tools, including the HP64773 in-circuit emulator from Hewlett-Packard. Contact AT&T for a list of third-party vendors.

SOFTWARE

Optimizing C compiler.
Assembler/linker.
State simulator.
VCOS operating system.
Many third-party support tools.

SUPPORT

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Raytheon
DSP96002

32-BIT FLOATING-POINT CMOS DSP µP

COST: 96002 (33 MHz), $368; 96002 (40 MHz), $441.
SECOND SOURCE: None.

DESCRIPTION: The 96002 is an architectural superset of the fixed-point 56001. The 96002 continues Motorola's emphasis on precision. The 96-bit accumulators will support future double-precision parts. The 32-bit floating-point device conforms to the IEEE-754 floating-point standard. The dual 32-bit external buses support glueless multi-96002 systems. The external buses can access external memory and peripherals or communicate with a host µP. A revision of the 96002 provides some enhancements, including increased speed and letting the internal RAM act as an instruction cache. It will remain software compatible with the existing 96002.

FEATURES: 50-, 60-, and 74-nsec cycle-time versions. 50-nsec cycle-time version scheduled for the fourth quarter of 1991.
Three 32-bit address buses and five 32-bit data buses on chip. Separate address buses for program and the two on-chip RAMs. Separate data buses for program, the two on-chip RAMs, global data, and DMA.
On-chip memory includes a 1k x 32-bit program RAM, a 64 x 32-bit boot ROM, dual 512 x 32-bit data RAMs, and dual 512 x 32-bit data ROMs.
On-chip boot ROM loads program from external byte-wide EPROM.
Revised version will let the internal 1k x 32-bit program RAM function like an instruction cache.
Two complete 32-bit external expansion ports for memory and I/O.
Three separate memory spaces (X, Y, and P). Each can address 4G words.
Each memory space is divided into eight 0.5G-word areas. Each can be programmed to either the A or B expansion ports.
Two host interfaces allow interface to µP or other 96002s. No other on-chip peripherals.

HARDWARE
Hardware evaluation system includes in-circuit emulator. Some third-party hardware products are available. Contact Motorola for a list of third-party vendors.

SOFTWARE
Optimizing C compiler.
Assembler/linker.
Simulator.
Application library.
GNU C compiler and source-level debugger.
Third-party support includes optimizing C compiler, block-level diagraming language, filter-design software, and Spox.

IEEE-754 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and returns 44-bit results. Multiplier accepts 32-bit integer data and returns 64-bit results.
32-bit bidirectional barrel shifter.
Ten 96-bit or thirty 32-bit register-based accumulators.
Zero-overhead looping.
Immediate, direct, indirect, circular, and bit-reversal addressing modes.
Two address ALUs.
Supports DMA. Uses its own internal bus and doesn't cycle-steal. Can use all of the addressing modes, including bit-reversal, with the DMA controller.
The stack is 15 levels deep and can be expanded into main memory.
Three external vectored interrupts.
Hardware and software-programmable wait states.
Serial debug port for in-circuit debugging.
Low-power mode.

EDN October 1, 1991
**µPD77240**

**32-BIT FLOATING-POINT CMOS DSP µP**

**AVAILABILITY:** The 132-pin PGA package is available now. The PQFP will be available in 1992.

**COST:** $75 (1000).

**SECOND SOURCE:** None.

**DESCRIPTION:** The µPD77240 is a 32-bit CMOS floating-point DSP chip. The internal instruction and data ROM are preprogrammed with math matrix routines. It has two external buses: one for data addressing up to 16M x 32-bit, and the other for instruction addressing up to 64k x 32-bit. The vendor says the architecture suits adaptive filter applications.

**FEATURES:** 90-nsec cycle time.
Separate on-chip program and data buses.
On-chip memory: 2k x 32-bit program ROM (preprogrammed), dual 512 x 32-bit data RAMs, and a 1k x 32-bit data ROM (preprogrammed).
External memory expansion: 64k x 32-bit program memory and 16M x 32-bit data memory.
Separate external program and data buses.
The 77240 has no on-chip peripherals.
Proprietary 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and creates 55-bit floating-point results.
Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results.

**HARDWARE**

Evaluation kit, which includes an in-circuit emulator.

**SOFTWARE**

Assembler/linker.
Simulator.

**SUPPORT**

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**32-BIT FLOATING-POINT CMOS DSP µP**

**AVAILABILITY:** The C30 and C30-27 are available now. The C30-40, C31, and C31-27 are sampling now.

**COST:** C30, $160; C30-27, $125; C30-40, $210; C31, $70; C31-27, $55 (1000).

**SECOND SOURCE:** None.

**DESCRIPTION:** This device is the floating-point member of the vendor’s TMS320 family. It was the first sub-100-nsec 32-bit floating-point CMOS DSP. It is not code compatible with the fixed-point chips. The C30 is available in a slower, lower-cost version called the C30-27. The C31 is object-code compatible with the C30 and C30-27, but has only one serial port, one parallel port, and one timer. This feature reduction decreases the chip size and pin count, which allows TI to offer a floating-point DSP for $35 in high volume.

**FEATURES:**
- 50-, 60-, and 74-nsec cycle-time versions.
- Four 24-bit address buses and three 32-bit data buses. Two 32-bit and two 40-bit additional buses in the CPU. Separate program, data, and DMA buses.
- Each internal RAM and ROM allows two accesses per cycle. Any of the separate memories can be used for program or data. Two on-chip 1k x 32-bit RAMs and an on-chip 4k x 32-bit ROM.
- 24-bit external memory-address bus provides 16M x 32-bit total address space.
- 13-bit external I/O address bus provides 8k x 32-bit I/O ports, which are mapped into the 16-Mbyte address space. Two 8-, 16-, 24-, and 32-bit serial I/O ports. Two 32-bit timers. Proprietary 2’s-complement 32-bit floating-point format.
- Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point result. 24-bit integers result in 32-bit fixed-point results.
- ALU operates on 40-bit floating-point and 32-bit fixed-point data.

**HARDWARE SUPPORT SOFTWARE**

**HARDWARE**
- Full-speed in-circuit emulator for PCs and Sun workstations.
- Evaluation module plugs into a PC.
- Significant third-party support. Contact Texas Instruments for a list of third-party vendors. Hewlett-Packard has a version of the HP64700 in-circuit emulator for the C30.

**SOFTWARE**
- Optimizing ANSI C compiler. Source-level debugger and code profiler. (PC or Sun).
- Assembler/linker. Simulator. (PC or Sun).
- Application library.
- Third-party support includes Spox, Ada compiler, filter-design packages, and block-level diagraming language.

**EDN October 1, 1991**

129
**TMS320C40**

**32-BIT FLOATING-POINT CMOS DSP μP**

**AVAILABILITY:** Samples available now. Production quantities in 1992.

**COST:** Samples cost approximately $500. $250 (5000).

**SECOND SOURCE:** None.

**DESCRIPTION:** This device was designed for applications that require the performance of parallel processing. It is upward compatible with the C30, but adds six 32-bit FIFO dual-buffered communication ports, two complete 32-bit external buses, an analysis module that supports multiprocessor debugging via a JTAG interface, and a 4G-word address space. The chip also features single-cycle conversion to and from the IEEE floating-point standard and a cycle time of 40 nsec. Each communication port can transfer data to and from another C40 at 20 Mbyte/sec without any external logic.

**FEATURES:**
- 40- and 50-nsec cycle time.
- Four 32-bit address buses and three 32-bit data buses.
- Two 32-bit and two 40-bit additional buses in the CPU.
- Separate program, data, and DMA buses.
- Each internal RAM and ROM allow two accesses per cycle.
- Any of the separate memories can be used for program or data.
- Two on-chip 1k x 32-bit RAMs and a 4k x 32-bit ROM.
- Dual 32-bit external buses. Each has a 31-bit address, so the 4G-word memory is equally divided between the two buses.
- Six independent 32-bit communication ports for glueless communications between C40s. Separate 8 x 32-bit FIFOs for input and output buffering.
- No on-chip serial ports. Two 32-bit timers.
- Proprietary 2’s-complement 32-bit floating-point format.
- Single-cycle conversion from and to the IEEE-754 32-bit format.
- Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point data. 24-bit integers result in 32-bit fixed-point results.
- ALU operates on 40-bit floating-point and 32-bit fixed-point data.

**HARDWARE**

- Development system includes in-circuit emulation via JTAG interface.
- 4-processor host-independent evaluation board.

**SOFTWARE**

- Optimizing ANSI C compiler with parallel-processing runtime support.
- Source-level debugger. Assembler/linker.
- Simulator.
- Application library.
- Third-party support includes Spox with drivers for parallel processing.

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EDN October 1, 1991

CIRCLE NO. 69
15 New High Speed Op Amps.

No Sacrifice For Speed. Not with Linear's new family of high speed op amps. LT1122, 1220, 1221, and 1222 provide 12 bit performance with nsec settling and bandwidths to 45 MHz. The LT1224, 1225 and 1226 are general purpose parts with the capability to drive unlimited capacitive loads. LT1190, 1191 and 1192 are video speed op amps with differential gain and phase errors of 0.1% and 0.06°. The LT1223, 1229 and 1230 are single, dual and quad current feedback amplifiers with high output drive current (50mA) and professional video quality differential gain and phase.

LT1228 is a high speed gain controlled amp with guaranteed operation down to ±2V or 4V single supply and output swing to within IV of the rails.

LT1122 is a JFET input op amp which slews 80V/µs. LT1193 and 1194 are video differential input amplifiers with programmable or fixed gain powered from single 5V or ±5V supplies with ±50mA output drive.

Singles and duals are available in 8-pin DIP and 8-pin SOIC package, quads in 14-pin. For data sheets and a comprehensive 132 page application note contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. Or call 800-637-5545.

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*12 Bit Settling Time
32-BIT FLOATING-POINT CMOS DSP µP

**AVAILABILITY:** Now.
**COST:** 34325 (25 MHz), $137; 34325 (20 MHz), $124 (10,000).
**SECOND SOURCE:** None.

**DESCRIPTION:** The ZR34325 is a vector-signal processor, which is a DSP chip that operates on complex data and large blocks of data with single high-level instructions. The instruction set includes a single instruction to calculate an FFT, FIR filter, IIR filter, and other complex functions. The highly specialized architecture is optimized to perform these functions quickly. The architecture also eases programming because the programmer doesn’t have to write code for complex DSP functions. The 32-bit floating-point data conforms to the IEEE-754 standard.

**FEATURES:**
- 80- and 100-nsec cycle-time versions.
- Single address and data bus.
- Vector instructions generally take longer to execute than to fetch, so little speed penalty is incurred with this simple bus architecture.
- High-level instructions, such as those to calculate FFTs and FIR and IIR filters, simplify programming.
- 256 x 32-bit coefficient dual-port ROM and 128 x 32-bit dual-port RAM on chip.
- No on-chip program memory.
- Internal memory can be directly accessed by external device. 16M x 32-bit memory space.
- No on-chip peripherals.
- IEEE-754 32-bit floating-point format.
- Multiplier accepts 32-bit floating-point data and creates 44-bit results.
- Three ALUs: two floating point and one integer. 32-bit floating-point data can be added to 32 bits with one ALU and to 44 bits with the other.
- 24-bit bidirectional barrel shifter.
- Two 32-bit accumulators.
- No zero-overhead looping.
- Direct, indirect, register, immediate, circular, and bit-reversed addressing modes.
- Address generators for internal RAM and ROM.
- On-chip DMA.
- Slave mode opens chip to external access.
- Hardware stack maintained in main memory.
- Single external interrupt.
- Hardware wait states.
- No on-chip emulation port.
- No low-power mode.
- Packaged in an 84-pin PGA or 84-pin QFP.

**HARDWARE**

| Hardware-development-system board. | VME bus-based product for development. | Third-party hardware available. |

**SUPPORT**

| Assembler/linker/simulator (MS-DOS and VAX/VMS). | Application library (MS-DOS and VAX/VMS). | Ada Compiler for VAX/VMS. |

**SOFTWARE**

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(408) 986-1314
FAX (408) 986-1240
Circle No. 686
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High-frequency VCOs top 100 MHz

Di Paolo Franco
Ericsson Fatme, Rome, Italy

VCOs that use surface-acoustic-wave (SAW) filters have higher operating frequencies and higher pull ranges than do circuits that use crystal oscillators. Figs 1 and 2 present two practical realizations of SAW-filter-based VCOs. The circuits' operating frequencies are 140 and 181 MHz, respectively. The differences between the two figures stem from that fact that two types of SAW filters are available. Fig 1's circuit uses a SAW filter that has 180° of phase shift. The filter in Fig 2 has a phase shift of 0°. Both circuits draw about 20 mA and operate from a 5V supply.

Fig 1—This oscillator is based on a 180° phase-shift SAW filter and has a free-running frequency of 140 MHz.

Fig 2—This oscillator is based on a 0° phase-shift SAW filter and has a free-running frequency of 181 MHz.
DESIGN IDEAS

Each circuit's operating frequency is solely dependent on the SAW filter's passband center frequency, which can be higher than 1000 MHz. The SAW filters have a pull range near 500 ppm when the BBY31 varactor diode's control voltage, $V_{\text{CONTROL}}$, varies by 4V.

These circuits' typical p-to-p voltage when driving a 50Ω load is 600 mV. The spectrum of the output signals is such that all the harmonics are below 25 dB with respect to the carrier. The variation with temperature when the circuits run in the free-running mode is 100 ppm, which is typical for SAW filters.

Crystal oscillators tend to be more stable over their operational frequency range than are SAW-based oscillators. However, that range is limited compared with the range of SAW-based oscillators. SAW filters are available with center frequencies starting at 120 MHz. The components cost of Fig 1 and Fig 2, without the SAW filter, is about $1 each. SAW filters cost about $25. EDN BBS DI #1030

To Vote For This Design, Circle No. 746

Three transistors convert ac to dc

Stephen Theobald
Bang & Olufsen, Harboøre, Denmark

The 3-transistor ac-to-dc converter in Fig 1 features a better frequency response and higher accuracy than most op-amp-based designs. The circuit runs from a 5V supply. $Q_1$ and $Q_2$ form a standard amplifier to buffer the input from the output. $Q_3$ bootstraps the collector load of $Q_2$ to provide current drive for the rectifier diodes. Current drive is essential for high accuracy. $Q_3$ also provides a low-impedance take-off point for the dc feedback to $Q_1$. Using an RF transistor for $Q_2$ ensures a wide bandwidth. The transistor's critical parameter is $C_{\text{off}}$, which is less than 2 pF at a $V_{\text{CE}}$ of 2V.

The Fig 1 circuit was tested at frequencies as high as 300 kHz. The circuit's low-frequency response is limited to 1 kHz. By multiplying the capacitor values by a constant, you can convert frequencies lower than 1 kHz provided that the time constants of the rectifier stage prove acceptable. The maximum output voltage is approximately 800 mV before limiting occurs. $R_1$ ensures stability for the circuit. The resistor isn't necessary if the driving circuit's impedance is greater than 300Ω. EDN BBS DI #1033

To Vote For This Design, Circle No. 747

![Circuit Diagram](image)

Fig 1—To ensure accuracy, $Q_1$ of this ac-to-dc converter bootstraps the collector load of $Q_3$ to provide current drive to the rectifier diodes.
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Truly incredible... superfast 3ns GaAs SPDT reflective or absorptive switches with built-in driver, available in PC plug-in or SMA connector models, from only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits’ latest innovative integrated components?

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**SPECIFICATIONS (typ)**

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**Mini-Circuits**
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

CIRCLE NO. 71
Data-Transfer Program  
- **Converts Macintosh to DOS**  
- **Requires no hardware or software modifications**

The PC version of Common-Link, a Macintosh-to-DOS utility, lets you format Macintosh disks in your IBM PC or compatible drive. The software runs under Microsoft Windows 3.0. No special hardware is needed to perform conversions. The software shows listings of two directories of files side by side on the screen. On one side are the Mac files resident on a Mac disk in the drive; on the other side are the DOS files in a selected directory on the hard drive or on a disk in another drive. Files are copied from one side to the other; conversions take place automatically. Because Mac files have three parts and DOS files have one, during Mac to DOS transfers, tutorial notes pop up with prompts to let the user select the appropriate conversion level. In DOS-to-Mac transfers, the DOS files are placed in a dummy Mac file. The software comes on a DOS disk and is loaded on the DOS computer. No hardware modification is needed for either machine, but both machines must have 1.44-Mbyte disk drives. $199.

**Pacific Micro**, 201 San Antonio Circle C250, Mountain View, CA 94040. Phone (415) 948-6200. FAX (415) 948-6296. Circle No. 351

**Software Development Systems Inc**, 4248 Belle Aire Lane, Downers Grove, IL 60515. Phone (708) 971-8170. Circle No. 352

Visual Programming Tool  
- **Object-oriented, visual system**  
- **Imports C, Pascal, Fortran code**

This version of Prograph 2.5 can graph code, including interfaces. It allows you to import existing C, Pascal, or Fortran code and build interactive front ends to existing applications. It incorporates a database engine for multiuser access to tables, indices, and data types. The software is compatible with the Macintosh System. The system lets you define program classes and modules graphically. Modules are defined as data-flow diagrams, using processing nodes. Prograph has an interface builder for the automatic generation of interface objects from a set of supplied System Classes. Prograph 2.5, $495; C and Pascal interfaces, $75 each; Fortran interface, $149.


C Compiler And Source-Level Debugger  
- **Connect DOS or Unix computer to target hardware**  
- **Software provides source-level debugging on target system**

The Crosscode C compiler and Freeform source-level debugger are tailored specifically for Motorola MVME-165 VME CPU and 68000-series evaluation boards. The tools provide source-level debugging directly on the target system. The debugger includes a transparent-monitor program for the evaluation boards. The monitor can retrieve the target system's register contents and other information for the debugger, thereby eliminating the need for a hardware emulator. You can use the debugger to connect any MS-DOS or Unix computer directly to the target hardware through an RS-232C cable. The tool can debug fully optimized code in real time and can run on a laptop. It is integrated with the compiler; the compiler includes an ANSI-standard C compiler, a macro relocating assembler, linker, librarian, download, symbol listing routines, and startup routine. The tools come bundled together. $3490.

**Software Development Systems Inc**, 4248 Belle Aire Lane, Downers Grove, IL 60515. Phone (708) 971-8170. Circle No. 352

**Qualita Inc**, 7101 Wisconsin Ave, Suite 1386, Bethesda, MD 20814. Phone (301) 907-6700. FAX (301) 907-0905. Circle No. 354

Memory-Management Software  
- **Manages multiple memory resources**  
- **Compatible with MS- and PC-DOS**

386Max and Bluemax memory-management tools are compatible with MS-DOS and PC-DOS. The tools enhance DOS's abilities by providing advanced automatic memory configuration and optimization. The software provides expanded and extended memory compatibility with LIM EMS 4.0, XMS 2.0, VCPI, and VDS. The software recovers available memory resources and automatically relocates resident software into previously unused memory regions. Automatic ROM caching improves system performance. Video RAM and ROM, other adapter RAM and ROM, and the system ROM BIOS are located within the reserved-memory region. Both tools automatically recover the monochrome area of DOS memory. The 386Max identifies and recovers unused filler patterns within the ROM BIOS; Bluemax automatically compresses the PS/2 BIOS and provides an additional 80 kbytes of contiguous reserved-memory RAM. Both tools configure Micro Channel Architecture adapters. The tools also perform ROM caching and resident software instantiating and can swap the fastest system memory into the first megabyte of memory. The tools require 1 kbyte of memory. The tools come bundled with the ASQ system analyzer and memory-management tutorial and the 386Cache disk-cache program. The cache program loads its executable DOS into high DOS while leaving track buffers in conventional memory. 386Max, $130; Bluemax, $155.


EDN October 1, 1991
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You asked for an integrated set of CAE/CAD design tools which could deliver every aspect of your engineering design needs at an affordable price. CAD Software offers the highest performing design system for your PC. Schematic capture, logic simulation, printed circuit board design, auto-routing, thermal analysis, and computer aided manufacturing are all within the PADS Design system.

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PADS-PCB sets the standard for affordable high performance PCB design. A one mil database, 30 layers, automatic design rules checking, SMD ability, excellent interactive routing, and a set of ECO routines which ensure fast accurate changes, are just some of the features which have made PADS-PCB the #1 selling PC based PCB design system.

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EDN October 1, 1991
CIRCLE NO. 72
See Us at Wescon Booth #1428
**NEW PRODUCTS**

**COMPUTERS & PERIPHERALS**

**Industrial 80486 Single-Board Computer**
- Has eight SIMM sockets for as much as 32 Mbytes of DRAM
- Operates at 25 or 33 MHz

The QPC-5160 single-board computer (SBC) for a passive ISA bus backplane contains an Intel 25- or 33-MHz 80486 µP. It also has eight SIMM (single-inline-memory-module) sockets for as much as 32 Mbytes of dynamic RAM (DRAM). Memory options are 1, 2, 4, 8, 16, or 32 Mbytes. In addition, the hardware supports the LIM 4.0 specification. You can expand the memory to 64 Mbytes, using a piggy-back daughter board. The SBC's DRAM features page-mode and 2-way interleaved access modes, and the daughter-board's memory has a 4-way interleaved access mode. The company designed the SBC to withstand harsh industrial conditions. The board also features a shadow RAM. Board with 4 Mbytes of DRAM (25 MHz), $3795; (33 MHz), $4195.

**Qualogy Inc., 109 Bonaventure Dr, San Jose, CA 95134. Phone (408) 434-5200. Circle No. 355**

---

**VORTEX™ Concentrates I/O for top 'C40 performance**

Harness the awesome power of TI's TMS320C40 digital signal processor to your AT or compatible computer — the Vortex system board from ASPI is all you need!

The Vortex is particularly well-suited for prototyping and implementing multiprocessor configurations. The six 'C40 communication ports allow direct processor-to-processor communication; almost any number of Vortex Boards can be linked quickly and easily by just plugging them together.

Besides the main TMS320C40 processor, a Vortex Board has a TI TMS320C31 floating-point processor. The 'C31 can be used with the 'C40 for I/O processing or filtering, or for entirely separate functions. This gives the Vortex a total floating-point capacity of 83 MFLOPS.

The Vortex will accommodate up to 2 Mbytes of SRAM, and works with ASPI's daughter boards — including a 64 Mbyte DRAM board, digital audio interface and general A-D/D-A systems.

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Atlanta Signal Processors, Inc. • 770 Spring Street Atlanta, GA 30308 USA (404) 892-7265 • FAX: (404) 892-2512

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**QIC Tape Drives**
- Connect to SCSI port on Macintosh computers
- Have capacities ranging from 150 to 525 Mbytes

The latest models of the Panther Tape Backup System are compatible with Apple's Macintosh Macplus, SE, SE 30, MAC II, IICX, IICI, and portable computers. Because the 5¼-in. drives employ the SCSI bus, you can attach them directly to the computer's SCSI port without using a host adapter board. The drives have capacities ranging from 150 to 525 Mbytes. The 525-Mbyte model can back up the entire tape in less than 45 minutes. Backup and restore rates range from 5 Mbytes/minute to 12 Mbytes/minute. The drives perform file-by-file and image backups, and they are compatible with the A/UX operating system. The
units use DC 6000 or equivalent tape medium, and the MTBF is 80,000 hours. Bit error rate is less than $10^{-13}$. 150-Mbyte drive, $2145; 525-Mbyte drive, $2695.

**Tandberg Data Inc.,** 2649 Townsgate Rd, Suite 600, Westlake Village, CA 91361. Phone (805) 495-8384. Circle No. 356

**386 Personal Computer**
- **Employed by AMD's 40-MHz 80386 µP**
- **Has 4 Mbytes of DRAM and one 64-kbyte cache RAM**

The 386WB-40SL ISA bus personal computer employs AMD's 40-MHz 80386 µP. The computer comes with 4 Mbytes of dynamic RAM, a 200-Mbyte hard-disk drive, a 14-in. super VGA monitor, a 1-Mbyte VGA Freedom Card, and 64 kbytes of cache RAM. The RAM is expandable to 64 Mbytes. In addition, the computer has FCC Class B approval, a parallel port, and two serial ports. Other features include a mouse, and DOS 4.01 and Windows 3.0 software. A 6-month GE on-site service contract, which is optionally expandable to five years, is also available. $2999.

**Bell Computer Systems,** 6615 Valjean Ave, Van Nuys, CA 91406. Phone (818) 909-3501. Circle No. 357

**80386 Mother Board**
- **Employed by AMD's 40-MHz 80386 µP**
- **Has 64-kbyte cache RAM expandable to 128 kbytes**

The 386 Cache 40 Mini-AT mother board uses AMD's 40-MHz 80386 µP. It has 64 kbytes of cache RAM that’s expandable to 128 kbytes. You can install as much as 32 Mbytes of dynamic RAM, using single inline memory modules. The board has eight 16-bit ISA bus expansion slots and a socket for an 80387 coprocessor. A shadow RAM for the system BIOS and video BIOS increases the execution speed as much as three times. The mother board runs Windows, OS/2, MS-DOS, Unix, Xenix, and Novell software. Performance figures include a 63.6 Landmark Speed (1.14), 8.55 Power Meter MIPS (1.5), and a Norton SL rating (4.5) of 48. $855.

**Pioneer Computer Inc.,** 49066 Milmont Dr, Fremont, CA 94538. Phone (415) 623-0808. Circle No. 358

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**Looking for a way to reduce shorting potential in a modular jack?**

**We've got it covered.**

Because contacts are exposed in most modular jacks, the chance of a thousand volts jumping from the jack to the nearest conductor is very real.

Molex's 41314 series of modular jacks greatly reduce the risk of shorting because their top is covered by the jack's plastic housing. This cover not only protects, but adds an extra margin of design flexibility by allowing PCBs to be stacked together more closely.

Each Molex Modjack must pass three functional tests, including on-line hi-pot testing. Jack contacts are plated after stamping, eliminating bare edges in critical areas. Molex Modjacks also meet all FCC 68.5 and UL 1863 requirements.

Assembly to board, both robotic and manual, is more efficient because contact tails lock securely into housing, assuring precise location.

For the widest selection of modular jack sizes, types and configurations, contact Molex.

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**Bringing People & Technology Together, Worldwide**

[Image: Molex logo]

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CIRCLE NO. 74
Technical calculations made easy!

Now it's easier than ever to perform faster, more reliable engineering and scientific calculations.

- Windows graphics features make Mathcad 3.0 the simple solution to complex analytic needs. Dialogs, pull-down menus, and mouse point-and-click capabilities make it easy to combine equations, text, and graphics right on your screen and print it all in a presentation-quality document.
- Symbolic calculations with a simple menu pick. Use expressions resulting from symbolic derivations in your numeric calculations or for further symbolic manipulation.
- Mathcad works on PC DOS, PC Windows, Macintosh, or UNIX. More than 120,000 engineers, scientists, and educators already use Mathcad for a variety of technical applications. Applications packs are also available to customize Mathcad for particular disciplines, including electrical, mechanical, and civil engineering and advanced math.

Quad Op Amp

- Offset voltage is 50 μV
- Bias current is 100 pA

According to the company, the OP-497 is the industry's highest precision quad op amp. Guaranteed specifications at 25°C include 50 μV maximum offset voltage with offset drift of 0.5 μV/°C; maximum bias current of 100 pA (450 pA at 125°C), and 2000V/mV minimum open-loop gain. The maximum per-channel supply current is 625 μA. The low offset voltage and high gain eliminate offset trims and additional gain stages in many designs. The super-beta input stage includes bias-current cancellation circuitry that maintains low (pA) bias current over the full operating temperature range. This action contrasts with traditional FET-input amplifiers whose bias current is initially low but typically doubles for every 10°C rise in temperature. Other features include a supply-voltage operating range of ±2 to ±20V, and a 120-dB PSRR and CMRR. The common-mode range extends to within 1V of the operating supply. The quad op amp is available in industrial and military temperature ranges. Package options include 14-pin plastic.
"We saved over $19,000 at the demo!"

CAPS® is a productivity-boosting engineering tool that helps you find, select, and specify ICs and semiconductors faster and easier than ever before.

"The microfilm system we purchased for IC and semiconductor search and selection just wasn’t working out. It was hard to use and there weren’t enough people using it to justify the cost. So, we decided to evaluate CD-ROM-based systems.

"While all this was happening, our purchasing people found a new IC vendor. They wanted to know if the new vendor made equivalents for some of our most commonly-used components. They thought we could get a better price. It would take us hours to find equivalents on the microfilm system, so we decided to challenge a couple of new CD-ROM-based systems.

"The first demonstration was a flop. Their system didn’t even include the new vendor. Needless to say, we weren’t impressed.

"Then Cahners came to demonstrate the CAPS system. In less than 20 minutes, CAPS found equivalents for the components we wanted. I figure we saved over $19,000 at the demo!

"Oh yes . . . we bought the system!"

— Frank Lucas
Test Engineering Manager
Welch Allyn
Data Collection Division

Updated monthly, the CD-ROM (Compact Disc – Read-Only Memory) based CAPS system gives you fast, easy, query-driven access to technical specifications and applications data for over 575,000 ICs and semiconductors made by nearly 500 companies worldwide. Best of all, CAPS provides instant access to hundreds of thousands of pages of complete, unabridged manufacturers’ datasheets, so you have everything you need right at your fingertips.
SONET Chip Set
- For STS-3 and STS-12 applications
- Satisfies both SONET and SDH requirements
This 3-piece chip set, consisting of the VP15301, VP15311, and VP15323, satisfies both SONET (Synchronous Optical Network) and SDH (Synchronous Digital Hierarchy) standards. Optimized primarily for STS-3 and STS-12 applications at 155 Mbps and 622 Mbps, respectively, the chip set is usable at other standardized rates and has been tested to comply with ANSI, CCITT, and Bellcore standards. The VP15301 is used for terminating the section overhead of SONET data streams. The VP15311 is used for terminating line overhead, and the VP15323 is used for processing and aligning SONET payloads to system timing. The VP15323 can also process concatenated data streams for handling asynchronous transfers and for SDH compatibility. Package options, which vary by chip and application, include an 84-pin plastic leaded chip carrier, a 144-pin plastic pin-grid array, and a 160-pin plastic quad flatpack. VP15301, VP15311 and VP15323, from $56, $90, and $69, respectively (2000).

Power Switching Regulator
- Output switch handles 5A
- Duty cycle is adjustable
Featuring an output-switch rating of 5A, the MC34167 switching regulator comes in a 5-lead TO-220 power package, which simplifies heat sinking. The regulator operates at a fixed frequency of 72 kHz. Because the timing components are on the chip, you don’t need an external resistor and capacitor to set the oscillator frequency. In addition to the oscillator and on-chip timing, the regulator contains a latching pulse-width modulator, a high-gain (80 dB) error amplifier, and a high-current (5A) output transistor. The duty cycle is adjustable from 0 to 95%. Protective features include cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. A low-power standby mode reduces current drain to 36 µA. In addition, the regulator has an internal resistor divider, which sets the output at a nominal 5.05V, eliminating the need for an external divider and providing an extra 50 mV to compensate for a 1% voltage drop in external wiring. The regulator is available in two temperature ranges; the MC34167T for 0 to 70°C operation, and the MC33167T for −40 to +85°C operation. MC34167T, $2.03; MC33167T, $2.19 (10,000).
NEW PRODUCTS
TEST & MEASUREMENT INSTRUMENTS

Enhancement For Jitter-Spectrum Analyzer
- Unit computes spectra of jitter in time measurements
- Instrument requires no external computer
When equipped with Option 040, the HP 5372A modulation-domain analyzer uses FFT techniques to determine the frequency spectrum of the jitter in a series of time measurements. The unit requires no external computer and works with jitter that has a bandwidth as high as 2 MHz. When the data stream is nonrepetitive, the analyzer does not require a clock. HP 5372A, $30,000. Option 040, $2000 (if installed by factory in new analyzer). Option 040 field upgrade for existing analyzers, $3000.
Hewlett-Packard Co, 19310 Prunetrade Ridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 365

Pocket-Size 3.5-GHz Counter
- Operates as long as five hours from NiCd battery
- Measures 3.4 x 3.8 x 1 in. and weighs 9 oz
The Model 3500 8-digit, 3.5-GHz frequency counter operates as long as five hours from a rechargeable NiCd battery. The unit, which offers a display-hold function, will operate while connected to its battery charger. Input resistance is 1 MΩ to 12 MHz; a second 50Ω input works from 10 MHz to 3.5 GHz. You can choose among three gate times, the longest of which gives 0.1-Hz resolution at 12 MHz. $3500.
Startek International Inc, 398 NE 38th St, Fort Lauderdale, FL 33334. Phone (305) 561-2211. FAX (305) 561-9133. Circle No. 367

68HC11 Emulators
- Interface to MS-DOS PCs via 115.2-kbps RS-232C link
- Work with µPs that generate a 3.3-MHz E-clock
There are two versions of the Icemaster 68HC11 in-circuit emulator: The Model 200 is a basic emulator; the Model 400 contains all of the basic unit's features and a 4k frame trace buffer, two real-time performance analyzers, and watchdog-timer support. Both emulators work with 68HC11s that generate a 3.3-MHz clock. You connect the instruments to an MS-DOS PC via an RS-232C link that supports host communica-

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Expansion Chassis
- Designed for EISA systems
- Includes a backplane
The PX1591 expansion chassis is designed for EISA/ISA systems. It includes a 13-slot, rack-mountable passive backplane and a 200W modular power supply. It also includes an expansion card module and one expansion card with the cables necessary to extend from the PCXI chassis to EISA/ISA desktop or rackmount PCs. The chassis provides EMI/RFI shielding, vibration protection, and industrial cooling with filtered fans. The unit accommodates as many as 10 function cards. $2395.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. Circle No. 362

Voltage Suppressors
- Will handle 300A
- Respond in 1 nsec max
Transguard multilayer-ceramic, transient-voltage suppressors have...
Announcing a night to recognize greatness

EDN's Innovation and Innovator of the Year Awards Ceremony

On the night of November 19 during Wescon, EDN will present the 1991 Innovation and Innovator of the Year awards at the Mark Hopkins Hotel in San Francisco. You are invited to show the finalists that you support greatness in innovation by attending the awards ceremony that is the culmination of their hard work. Through its Innovation Crusade, EDN hopes to inspire engineering professionals within the electronics field to reach for higher plateaus of inspiration and creativity.

The dedication and involvement of EDN readers, like yourself, have made the Innovation Crusade and awards ceremony a reality. By taking the time to nominate your peers and, in fact, select the winners, you show commitment to quality and creativity in electronics and are driving this crusade. But don’t stop there … order your ticket to the industry event of the year and show these innovators that greatness does not go unrecognized. All proceeds of the dinner will be donated to the EDN Scholarship Fund.

To receive a reservation order form to the EDN 1991 Innovation Dinner and Awards Ceremony, fax Pam Winch at (617) 558-4470.
COMPONENTS & POWER SUPPLIES

a current capability of 150 to 300A. These surface-mount varistors have a response time of 1 nsec max and are available in a variety of package sizes. These low-voltage devices have a circuit-operation capability ranging to 60 working volts. Clamping-voltage figures range from 15.5 to 30V. Transient-energy figures span a 0.3 to 1.2J range. $0.45 to $0.55 (1000). Delivery, six to eight weeks ARO.

AVX Corp, 3900 Electronics Dr, Raleigh, NC 27604. Phone (919) 878-6200.

Circle No. 363

Surface-Mount Resistors
- Rated for 250 mW
- Have a 0.1% tolerance

SMM0204 MELF-type surface-mount resistors are rated for 250 mW at 70°C. Resistance values range from 1.2Ω to 2 MΩ and tolerances range from 0.1 to 5%. Temperature coefficients vary from ±15 to ±100 ppm/°C depending on resistance value and tolerance. The resistors measure 0.142 x 0.059 in. and have end caps that are reflow and wave solderable. The units are color-banded for easy identification and are available on 8-mm tape-and-reel or bulk packaging. 10-kΩ with a 1% tolerance and a ±50 ppm/°C temperature coefficient, $0.023 (10,000). Delivery, stock to six weeks ARO.

Dale Electronics Inc, 2300 Riverside Blvd, Norfolk, NE 68701. Phone (402) 644-4247.

Circle No. 364

ULTRA-MINIATURE SURFACE MOUNT

DC-DC Converter Transformers and Power Inductors

These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The Inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

- Operation over ambient temperature range from -55°C to +105°C
- All units are magnetically shielded
- All units exceed the requirements of MIL-T-27 (+130°C)
- Transformers have input voltages of 5V, 12V, 24V and 48V. Output voltages to 300V.
- Transformers can be used for self-saturating or linear switching applications
- Schematics and parts list provided with transformers
- Inductors to 20mH with DC currents to 23 amps
- Inductors have split windings

Delivery—stock to one week

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CIRCLE NO. 83

EDN October 1, 1991
UNIVERSAL PROGRAMMER

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FREE software updates on BBS.
Powerful menu driven software.

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CIRCLE NO. 325

8051

SEE EEM 91/92
Pages D 1300-1303

PC based emulators for the 8051 family
8031, 8032, 8051, 8052, IO/152/154, 1517/51/451/51G/51FA/51GB/517/53/537/
75/752, 852, 853, 854... more.

- PC plug-in boards or RS-232 box.
- Up to 33 MHz real-time emulation.
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