Special Report: EDN's µP/µC directory exposes unsupported benchmarks
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CIRCLE NO. 88

FLUKE
EDN November 22, 1990
SPECIAL REPORT
EDN's 17th Annual Microprocessor Directory 90

Benchmarks don't have to be confusing and deceptive. Application code that bears a resemblance to your software, consistently applied across a range of similarly configured microprocessor-based systems, can be useful in selecting your hardware.—Michael C Markowitz, Associate Editor

DESIGN FEATURE
Real-time programming—Part 6 197

Real-time applications are concerned with physically real processes that proceed in terms of real-world clocks. Thus, such applications must be able to link up with real-world time, as opposed to CPU or other internal computer time. Part 6 of this series discusses the two aspects of time that are involved: interval and time of day.—David L Ripps, Industrial Programming Inc

TECHNOLOGY UPDATES
VXIbus product directory: 43
Small products add big spark to test field

While the traditional test-and-measurement community reports quiet business, VXIbus products are growing in number and variety and are appearing in complete systems.—Brian Kerridge, European Editor

Vendors optimize ICs for state machines 61
Designing effective state machines requires choosing the right ICs. The evolution of state-machine controllers gives designers a wide range of products from which to choose.—John Gallant, Associate Editor

Continued on page 7
Embedded control challenge of the 90s:
Applications are increasingly burdened with the overhead of friendliness. Even so, users expect everything to happen immediately, if not sooner.
As a result, applications with embedded microprocessors need more computing power than ever. Our CY7C611 SPARC RISC controller gives you the power to create, at a price that fits your application.

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The B-2 stealth-bomber program costs a great deal of money, and the bomber may not be as invisible to radar as expected. Instead of relying on high-tech weapons systems, US defense and congressional planners should spend money on programs that pay higher dividends.
7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!

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You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
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12:00 pm: Lunch
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EDN November 22, 1990
RUGGEDIZED PCs FOR HARSH ENVIRONMENTS

The MDC family of ruggedized IBM PC-compatible computers from Mobiledata Communications Corp (Phoenix, AZ, (602) 678-3788) are designed for applications in harsh environments such as factories, remote locations, and inside vehicles. Three modular components—display, keyboard, and processor/storage-unit modules—make up the MDC family system. You can locate the keyboard and display modules as far as 15 ft from the processor/storage modules. The systems can operate in temperatures ranging from -40 to +85°C. The company has 8088- and 80386-based models with a choice of monochrome or color flat-panel displays. The company conformal-coats the pc boards used in the MDC systems to increase resistance to humidity and liquid spills. Prices range from $7425 for an 8088 unit to $10,500 for monochrome 80386 systems.—Maury Wright

SINGLE IC LETS YOU SCALE, ROTATE, AND ENHANCE IMAGES

The BT710 IC from Brooktree Corp (San Diego, CA, (619) 452-7580) sizes and rotates graphics for electronic imaging. The IC also lets you enhance the quality of black-and-white figures by converting them to 4-bit gray scale. The result of this gray scaling is an antialiased effect that increases the apparent resolution of the displayed image and makes it more readable. The IC can resize images to a minimum of 6% or a maximum of 7.5 x the original size.

Two on-chip DMA channels let the unit operate autonomously by reading and writing to image buffers without CPU intervention. The unit also performs address translation for rotated images and provides bit-aligned block transfers to window or frame buffers. The $132 (100) Bt710 is a 5V, 50-MHz CMOS IC packaged as a 132-pin pin-grid array. A $995 evaluation kit, the Bt710EVK, includes documentation, demo software, and an IBM PC/AT plug-in board that contains a BT710 IC. You can also order developer kits for IBM PC ($1990), Macintosh ($2490), and Sun ($2990) systems that include Pixelvu software for CCITT compression and decompression, image scaling, rotation, mirroring, and Boolean bitblt operations.—J D Mosley

MIL-PRODUCT DATABASE INCLUDES EDIF CAE INFORMATION

Although several component database systems exist, none except the Component Information System (CIS) from Expert Views Inc (Waltham, MA, (617) 890-0333) lets you transfer component data on MIL-spec components to your CAE system. The database supplies graphical-symbol information and specifications to CAE systems in both ASCII and EDIF 2 0 0 formats. A symbol compiler lets a company convert graphics information so that it complies with company-wide graphics standards. The CIS database system supplies the parts, CAE data, and specifications. Cost is $50,000 for a 1-year license, which includes quarterly updates.

You will also need parts-access and access-control software packages to use the system. View Master, the parts-access software, lets users examine components and specifications. The control software, Component Manager, lets managers customize the database by eliminating some products, adding specifications for others, and adding special or customized components. The View Master and Component Manager each cost $40,000, which is a 1-time payment. The system operates on networks with computers that run either Unix or VMS operating systems.—Jon Titus
**NEWS BREAKS**

**ALTERNATE-SOURCE AGREEMENT ON FUTUREBUS+ SILICON**

Philips Components-Signetics (Sunnyvale, CA, (408) 991-2000) and Texas Instruments (Dallas, TX, (800) 536-5236) have announced a joint development and alternate-source agreement for silicon support for the proposed Futurebus+ standard. Under the terms of the agreement, both companies will manufacture and market the Futurebus+ product family (designated FB2000 by Signetics and TFB2000 by TI), and both will use their own proprietary processes to manufacture the products. The 5-year, renewable second-source agreement is the third cooperative agreement between the companies in the past four years.—John A Gallant

**ARCNET CHIP AND µC COMPOSE COMPLETE LAN NODE**

Standard Microsystems Corp (Hauppauge, NY, (516) 273-3100) offers the COM20020 Arcnet IC that combines controller and transceiver functions in a single chip. The IC is for low-cost embedded applications such as process control, factory automation, medical equipment, and automobile LANs. Available in 24-pin DIPs and 28-pin plastic leaded-chip-carrier packages, the IC has a 2×8k-bits dual-port static-RAM buffer, a glue-free interface to most microcontrollers, and a variety of hardware diagnostics capabilities. The IC also has a command-chaining feature that speeds packet processing and enables it to support consecutive transmissions without host intervention. The $16.23 (1000) CMOS COM20020 operates from a single 5V supply and has an operating temperature range of -40 to +85°C.—Maury Wright

**COMPARABLY PRICED DP8392-LIKE CHIP USES LESS POWER**

Providing higher reliability because of its lower power consumption, the CS83C92C Ethernet/Cheapernet LAN transceiver from Crystal Semiconductor (Austin, TX, (512) 445-7222) is a comparably priced, plug-compatible version of National Semiconductor’s DP8392 chip. Powered by a single –9V supply, the chip requires a maximum current of 130 mA for transmission and 80 mA in its quiescent state, figures that are 28 and 39% lower than National’s specs of 180 and 155 mA, respectively. In addition, the chip will withstand more than 1000V of electrostatic discharge (ESD) on all pins and 3000V on most pins. National’s published specs indicate ESD failure when exposed to less than 500V. The chip includes squelch circuits that reduce noise when transmitting and receiving signals. A jabber timer disables the transmitter when the chip encounters illegally long packets of data. Compliant with ISO/IEEE 8802/3 requirements, the CS83C92C sells for $18 (1000) and comes in 16-pin DIPs and 28-pin plastic leaded-chip-carrier packages.—J D Mosley

**OPEN HARDWARE DESCRIPTION LANGUAGE COLLECTS SUPPORT**

Cadence Advanced CAE Div’s (San Jose, CA, (408) 727-0264) efforts to put the Verilog hardware description language into the public domain have begun to bear fruit. Both Zycad Inc (Menlo Park, CA, (415) 688-7400) and Ikos Systems (Sunnyvale, CA, (408) 246-1900) have translators that let you convert Verilog models, circuits, and stimuli into their own hardware-accelerated simulation formats. Verilog models are available from Sun Microsystems (Mountain View, CA, (415) 960-1300), which offers an Sbus model package, and from RISC International (San Jose, CA, (408) 428-1000), which offers a library of about 120 models. The CAD/CAM Group (Cupertino, CA, (408) 725-0204) generates Verilog models from its design-entry system, and Synopsys (Mountain View, CA, (415) 962-5000) and VLSI Technology (San Jose, CA, (408) 434-3000) use the models to drive their logic-synthesis tools.—Michael C Markowitz
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<td>65511</td>
<td>32 I/Os, 2x8-bit timers, watchdog timer, serial I/O</td>
<td>4KB</td>
<td>128B</td>
<td>40-DIP 64-PLCC/QFP</td>
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<tr>
<td>65512</td>
<td>32 I/Os, 3x8-bit timers, 1x16-bit timers, serial I/O</td>
<td>8KB</td>
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<td>40-DIP 64-PLCC/QFP</td>
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<tr>
<td>65P512</td>
<td>Same as 65512 with 24 additional I/Os</td>
<td>8KB</td>
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<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>65513</td>
<td>Same as 65512 with 24 additional I/Os</td>
<td>8KB</td>
<td>128B</td>
<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>65524</td>
<td>Same as 65512 with 2x8-bit PWM, 8-bit A/D, additional ROM/RAM</td>
<td>16KB</td>
<td>384B</td>
<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>65P524</td>
<td>Same as 65512 with 2x8-bit PWM, 8-bit A/D, additional ROM/RAM</td>
<td>16KB</td>
<td>384B</td>
<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>66201V</td>
<td>48 I/Os</td>
<td>16KB</td>
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<tr>
<td>66P201</td>
<td>10-bit A/D</td>
<td>16KB</td>
<td>512B</td>
<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>66207</td>
<td>4x16-bit timers</td>
<td>16KB</td>
<td>512B</td>
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<td>66P207</td>
<td>2x16-bit PWM</td>
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<tr>
<td>66301</td>
<td>Serial interface</td>
<td>32KB</td>
<td>1KB</td>
<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>66P301</td>
<td>Transition detector</td>
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<td>64-SDIP/QFP 68-PLCC</td>
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<tr>
<td>66417</td>
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<td>66P417</td>
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<td>67620</td>
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<td>16KB</td>
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</tr>
</tbody>
</table>

**OKI Semiconductor**

EDN November 22, 1990

CIRCLE NO. 109
NEURAL STEPPING STONES FOR TOMORROW'S TECHNOLOGY—TODAY!

INTEGRATED CIRCUITS FOR ADAPTIVE LEARNING AND FAST PROCESSING

Micro Devices' MD1220 Neural Bit Slice (NBS) can propel you into tomorrow's real-time neural network systems—today!

Each device contains eight neurons with fifteen "hard-wired" synaptic inputs per neuron. For designs that require more synaptic inputs per neuron, expansion through "virtual" synapses is easily accomplished with modest additional hardware. MD1220s can be cascaded or paralleled to provide a neural network of practically unlimited size, with beyond 256 synapses per neuron.

After training under microprocessor control, the NBS (using 16-bit synaptic weights) processes eight digital inputs in only 7.2μs—performance equal to that of a dedicated 55 MIPS processor.

The device is ideal for use in image classification, target or speech recognition, signal processing, risk analysis, robotics, communications and sensor fusion applications. And it's a much faster solution than "simulated" neural networks operating under software control. Ideal for applications which defy algorithmic solutions, such as optimizations.

The MD1220 is an economically practical solution with its low price ($41 in 1K quantities) and easy design implementation. Designers can start working with it right away. For detailed specifications and application hints, contact Micro Devices today.

GET ACQUAINTED right away. An evaluation kit is available which includes a fully assembled XT/AT compatible circuit board with two MD1220 devices, sophisticated menu driven software, user manual and "broom balancing" fixture. The kit provides a step-by-step walkthrough of neural network configurations and training. Order an evaluation kit today—only $395.00 complete.

Micro Devices
30 Skyline Drive
Lake Mary, FL 32746-6201 USA
Telephone 407/333-4379
FAX 407/333-4479

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MEGA MEMORY.

SONY HIGH-DENSITY SRAMS

<table>
<thead>
<tr>
<th>MODEL</th>
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<td>CXK581000P*</td>
<td>128K x 8</td>
<td>100/120</td>
<td>DIP 600 mil</td>
<td>L, LL</td>
</tr>
<tr>
<td>CXK581000M*</td>
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<td>100/120</td>
<td>SOP 525 mil</td>
<td>L, LL</td>
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<tr>
<td>CXK581000TM*</td>
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<td>100/120</td>
<td>TSOP</td>
<td>L, LL</td>
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<td>CXK581000YM*</td>
<td>128K x 8</td>
<td>100/120</td>
<td>TSOP (reverse)</td>
<td>L, LL</td>
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<td>CXK581001P</td>
<td>128K x 8</td>
<td>70/85</td>
<td>DIP 600 mil</td>
<td>L</td>
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<tr>
<td>CXK581001M</td>
<td>128K x 8</td>
<td>70/85</td>
<td>SOP 525 mil</td>
<td>L</td>
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<tr>
<td>CXK581020SP</td>
<td>128K x 8</td>
<td>35/45/55</td>
<td>SDFP 400 mil</td>
<td>L</td>
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<tr>
<td>CXK581020J</td>
<td>128K x 8</td>
<td>35/45/55</td>
<td>SOJ 400 mil</td>
<td>L</td>
</tr>
</tbody>
</table>

*Extended temperature range available. L = Low power. LL = Low, low power.

MEGA COMMITMENT.

As you can see, Sony's more committed than ever to meeting your high-density SRAM needs. Just consider the enhancements we've made in a few short months. TSOP and TSOP-reverse packaging. Low data retention current. And extended temperature range. All based on our unique 0.8-micron CMOS technology and available in 32-pin DIP and surface-mount plastic packages.

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Finally, you get the industry’s best-rated documentation, integration support, regional technical staff and a full one-year warranty.

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Because turning 040 doesn’t have to slow you down.

---

<table>
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<tr>
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<th>COMPATIBILITY</th>
<th>68040 CPU</th>
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<td>DMA, SCSI, Floppy, Ethernet, Serial I/O</td>
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<td>CPU-33</td>
<td>DMA, DRAM, Serial I/O</td>
<td>CPU-40</td>
</tr>
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*Novell certification applies to the EtherStar LAN adapter which incorporates the Fujitsu chip set.

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Drop the B-2 bomber

In the chaotic budget deliberations in the US Congress, there is a bit of hope. Congress recently voted to drastically cut spending for the B-2 bomber. That decision is a good step in reducing both defense spending and the US's reliance on gee-whiz high-technology weapons systems. I'm most concerned about our reliance on and fascination with high-tech weaponry.

I'm sure some readers will respond that cutting the B-2 project will hamper US defense efforts and weaken our ability to respond to local actions such as Iraq's invasion of Kuwait. Anyone who believes that argument has been reading too many of the Department of Defense's self-serving pronouncements. The B-2 is a flawed product in search of a nonexistent mission.

The Air Force presents the B-2 as a plane that radar cannot detect, and today's radars cannot detect it, at least at long ranges. However, several recent photographs of the B-2 in flight show it refueling from a standard Air Force tanker aircraft. Such a tanker does show up on radar systems and presents a nice target.

The US has no stealth tankers. Also, developments in ultra-wideband (UWB) radar systems may advance radar technology to the point where practical radar systems can detect stealth aircraft. UWB radar has its own set of development and technology barriers, but the US's development of stealth aircraft will spur the development of UWB radar—both in the US and elsewhere.

The B-2 has other inherent limitations. Its turbofan engines emit a warm exhaust plume that can be detected by infrared sensors such as those on the USSR's MiG-29. The high cost of each B-2—over $500 million—means that the Air Force will be reluctant to commit the planes to action until all of the enemy's air defenses have been eliminated. So, why the need for a radar-invisible bomber in the first place? The DoD presents the B-2 as a flexible weapons system that can track down and destroy mobile weapons systems and command posts—the same mission established years ago for cheaper and pilotless cruise missiles.

For these reasons alone, the B-2 should be dumped. Congressional and defense leaders should trade the B-2 for other projects—several deserve more funding and more attention than they are getting now. Late last year, the Pentagon quietly shut down the SR-71 Blackbird program of high-altitude reconnaissance flights. Congress charged that the program was poorly managed and refused to continue funding it. Close-in photoreconnaissance might have given us more information about Iraq's recent strategies. The SR-71 is too valuable an asset to mothball. Instead of stopping the program, Congress should demand an action plan and get the Blackbird flying again.

In the present rush to cut defense budgets, let's be sure we're cutting the right programs and funding the programs that offer real defense benefits.
Things aren't always what they seem.

Some people would have you believe FPGAs are faster and denser than MAX™ EPLDs.

Funny how they never mention *in-system* performance, though.

When they talk about speed, they quote 100MHz flip-flop toggle rates.

When they talk about density, they recite raw gate counts.

Which could make your high-performance design highly disappointing.

But if you want to do more than just spin your wheels, consider MAX.

It’s the first family of programmable logic devices to provide both high speed and high logic density where it counts. At the system level.

Which means MAX can handle just about all your logic needs. In fact, a single 64-macrocell EPM5064...
can integrate anything from simple system glue logic right up to complex graphics coprocessors and LAN and memory controllers.

Or take the 68-pin MAX EPM5128. It's up to 50% faster and 100% denser than comparable FPGAs, thanks to its high-performance architecture and superior logic routability. But don't take our word for it—just take a look at the competition's benchmarks.

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We'll make sure you've got plenty of horses under the hood.
With more than 50 BiCMOS logic functions from Texas Instruments, you can beat tough bus-interface design challenges. Our free SamplePacs will show you how.

Specially designed for use in bus-interface applications, our growing BiCMOS logic family can make the difference in getting data on and off the bus faster. These advanced functions that combine the best of bipolar and CMOS can help you attain higher system performance levels.

Lowering power, maximizing speed
For example, our BiCMOS devices can help you minimize power dissipation and maximize speed. Disabled currents are reduced by as much as 95% and active currents by as much as 50% compared to advanced bipolar equivalents.
DIFFERENCE

In fact, your system power savings can amount to more than 25%, and you should experience reduced switching noise as well. Yet you can maximize system speed. Switching speeds are comparable to advanced bipolar devices and provide the high drive current required for today's industry-standard buses (48/64 mA commercial, 24/48 mA military).

Gaining even greater performance
If you need even lower power and higher speeds, our submicron Advanced BiCMOS (ABT) family is the choice for you. Planned devices include 8-, 9-, and 10-bit buffers/drivers, transceivers, latches, registers, and registered and latched transceivers.

Our broad BiCMOS family also includes unique functions that can help you more quickly meet the design challenges involved with incident wave switching, driving MOS memories, and system testability.

Assuring incident wave switching
Wider word widths and additional cards on backplanes are requiring higher drive currents to assure incident wave switching.

Our BiCMOS family delivers. With our low-impedance line drivers, you get more "instantaneous" current even when impedances are as low as 25 ohms. You minimize transition "flat" spots that can degrade speed or cause oscillation at the receiving devices.

Managing MOS memory loads
MOS memory array interfaces create the high-capacitive loading environments that can result in overshoot and undershoot conditions. As a result, system reliability suffers. To handle this situation, our BiCMOS memory drivers incorporate a series damping resistor output structure that delivers advanced system performance when driving 256K, 1M, and 4M DRAMS.

Building in testability with SCOPE
It is becoming more difficult to accurately test today's highly integrated boards and systems, but TI's BiCMOS family contains your solution: SCOPE™ (System Controllability and Observability Partitioning Environment) octals.

Used in place of standard octals, SCOPE devices allow specific circuitry within an assembled module, board, or system to be isolated for verification and debugging without manual probing. Currently, our BiCMOS family includes an octal buffer, transceiver, D-type latch, and D-type flip-flop.

TI's SCOPE products are the first to conform to the Joint Test Action Group (JTAG) specifications adopted by the IEEE 1149.1 Test Standards Committee.

Get your free SamplePac and sample our BiCMOS difference; call 1-800-336-5236, ext. 3008
You can take your choice of our BiCMOS SamplePacs containing a free BiCMOS device, our latest advanced logic brochure, plus appropriate product data. Just call the number given above, or use the return card to let us know which SamplePac you need to begin applying TI's BiCMOS difference.

CIRCLE NO. 136
These Fit The Occasion.

This immersible position sensor fits inside a hydraulic cylinder, using the fluid it resides in as a lubricant while saving space.

These heavy-duty "down-hole" sensor designs check the well casing diameter while working under extreme pressure and heat.

Use the same approach to angular displacement in hand held instruments as these gyro and fin position sensors, which bemoan on a missile design problem.

Drive-by-wire designs for automotive and heavy equipment designs make reliability problems a thing of the past.

Both spring loaded and magnetically coupled position sensors for truck engine applications must withstand extremes of vibration, temperature and exposure to highway dirt and grime.

They began with a need to fit in just the right place and function dependably under any conditions. They are available in as many shapes and sizes as the challenges they’re designed to meet. Their outstanding accuracy, feedback and environmental capabilities can be used to quickly solve your most demanding requirements for a potentiometric position sensor. Just sketch, spec or even hint at your requirements on a piece of paper and FAX it to us today at (714) 557-6240.
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It's not that we don't resp
we just see things

When it comes to medium frequency DSOs, how much you see depends on how much you can capture, how well you can analyze it, and how easily you can do the job.

Digital Storage Oscilloscopes from Fluke see things a little differently than DSOs from HP or Tek for one simple reason. They see more.

Thanks to the fastest real time sampling speeds available under $5,000, the new PM 3375 not only gives you full analog capabilities, it also lets you capture fast single shot events — with exceptional resolution.

But DSOs from Fluke don't just show you more. They also tell you more, by giving you the analytical power you need to extract a wealth of extra information from your signals.

Twice the sampling speed. Twice as easy.

Take our new medium frequency PM 3375, for example. With real time sampling at 250 MS/s, the PM 3375 samples every waveform more than 2½ times faster than any HP or Tek scope in its price range. So now you can accurately capture more types of signals, more precisely. Even fast single shot events to 25 MHz (@10 samples per period), with resolution to a full 4 ns.

You also get repetitive sampling to capture recurrent signals to 100 MHz. Plus an averaging mode to help reduce noise without also reducing bandwidth. Not to mention an envelope mode to monitor extremes of signal variation, such as tracking signal jitter or AM/FM modulation depth.

And like every DSO from Fluke, the PM 3375 is remarkably easy to operate. You can switch from digital to analog operation any time you want at the push of a button. AUTOSET lets you find your signal and fully set up your scope automatically. You can store up to 64 front panel setups in non-volatile memory. Even full remote is available.

Starting at just $2,390, Fluke DSOs stop at nothing to deliver superior performance.
Better analysis. Better value.

Of course the real advantage of DSO technology isn’t just seeing and capturing waveforms. It’s analyzing waveforms. Here, DSOs from Fluke really stand out. Smart cursors take you far beyond mere dV and dt measurements, to automatically calculate Vpp, Vrms, Vmean, Frequency, Period, Pulsewidth, Rise- and Fall-times and more. Get the whole picture on video. Free.

With prices ranging from $2,350 to $5,390, medium frequency DSOs from Fluke offer superior specs for unparalleled performance and value. Compare all five, including our high frequency DSOs, to HP & Tek by sending for our full comparison chart. Or watch them in action in our free video titled “DSOs With a Difference: Chapter III.” Just call 1-800-44-FLUKE ext. 77.

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<th>HP 54501A</th>
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<tbody>
<tr>
<td>Analog + Digital</td>
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<td>Yes</td>
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<td>Analog Bandwidth</td>
<td>100 MHz</td>
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<td>Max. Captured Freq. Single Shot Sig.*</td>
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<td>No</td>
<td>Yes</td>
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<tr>
<td>AUTOSET</td>
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<td>Beamfinder Only</td>
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<td>Setup Memory</td>
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<tr>
<td>Remote</td>
<td>Full</td>
<td>Data Only</td>
<td>Full</td>
</tr>
</tbody>
</table>

* 10 samples per period
** with automatic adjustment for probe factor

With all the new regulations surrounding electromagnetic compatibility (EMC), the best way to avoid costly delays is to locate problems as early as possible. Two new HP EMC solutions make that easy.

The HP 84100A Design Development Solution helps you correct problem areas at the design stage. It pinpoints hot spots on breadboards and prototypes using a spectrum analyzer with software memory cards that simplify troubleshooting.

The HP 84110A Pre-Production Solution gives you added confidence that your designs will pass compliance. It has all the analysis capability, software and accessories you need to uncover conducted and radiated emission problems before final EMI testing.

So, find out how to build EMC into your designs. For information about HP’s full line of EMC solutions and design training programs, call 1-800-752-0900. Ask for Ext. 1350, and we’ll send you our EMC Measurement Solutions fact kit.

There is a better way.

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*In Canada, call 1-800-387-3867, Dept. 502

CIRCLE NO. 79

EDN November 22, 1990
TECHNOLOGY UPDATE

VXIbus PRODUCT DIRECTORY

Small products add big spark to test field

While the traditional test-and-measurement community reports quiet business, VXIbus products are growing in number and variety and are appearing in complete systems.

Brian Kerridge, European Editor

VXIbus-product designers refuse to let low activity in the conventional test-and-measurement sector break their resolve. (VXI stands for VME extensions for instrumentation.) The twelve months since EDN's first survey of VXIbus products (Ref 1) has seen vendors consolidate product ranges and push the success of the VXIbus standard beyond doubt.

Recent additions to VXIbus instrument rankings include several high-end units, such as a 500-MHz digitizing oscilloscope, a time-interval analyzer with an 8-psec resolution, and a 1-mHz to 20-kHz frequency-response analyzer.

Just as encouraging as the growth of VXIbus products is the growth in the number and variety of turnkey automatic test equipment (ATE) employing VXIbus products. Blakell Systems offers a pc-board tester and 250V connectivity ATE; Giordano Associates markets a range of mobile ATE for analog, digital, and hybrid testing; and Kikusui has a functional test system. Other VXIbus-based systems include NH Research's in-circuit tester and power-supply ATE as well as Racal Instruments' range of radar test systems for measuring 20-GHz signals.

At the VXIbus module level, the principal vendors are Hewlett-Packard, Racal-Dana, and the Tektronix/Colorado Data Systems amalgamation. These companies each offer a wide variety of modules and chassis parts. Other module vendors include National Instruments, which specializes in bus control, and companies that offer a few specialist products each.

Hewlett-Packard made an early surprise launch into the B-size market and has recently expanded that range of products with nine products. Unit prices for all nine products are around $1000. The modules suit scanning and sensor monitoring in industrial applications.

Radar test systems from Racal-Instruments can measure transmitter and receiver parameters of 20 GHz. The systems use a screened RF and microwave enclosure.

Several of the modules include the company's System 10 bundled data-acquisition system. Priced at $5750, the system includes a 5 1/2-digit DMM, a 16-channel relay multiplexer for thermocouples, a 16-channel voltage multiplexer, and a 48-channel single-ended multiplexer. A B-size 9-slot enclosure houses all the cards and includes an IEEE-488 link to your PC. Labtech
Break Through 7ns

with BiCEMOS™ ECL

Speed Leadership
Design tomorrow’s fastest systems today. Our IDT10484 (4K x 4) will be the fastest high-density BiCMOS memory to run primary caches in ECL systems. At 7ns, the IDT10494 (16K x 4) is the fastest BiCEMOS 64K ECL SRAM available in volume production today.

In addition, we offer the densest BiCEMOS ECL RAM, the IDT10504 (64K x 4), at 12ns. And our new 12ns IDT10496RL (16K x 4) synchronous self-timed SRAM (STRAM) offers registered inputs, latched outputs, and self-timed write for easier system design.

Each of our ECL SRAMs is available today in 10K, 100K, and 101K configurations in 300mil SOJ and 400mil Sidebraze DIP packages.

Technology for the '90s
We engineered BiCEMOS technology to offer the best of both worlds: the low power consumption of CMOS with the high speed of bipolar technology.

Count on our BiCEMOS ECL to take you through the 7ns speed barrier for 64K densities. We believe our BiCEMOS ECL will achieve speed increases of 20% a year every year for the next five years, making BiCEMOS the technology for the '90s.

Samples Available
Call or FAX us today for samples and a copy of the new BiCEMOS ECL Product Information booklet with information on designing with BiCEMOS ECL for ultra-high-speed systems.

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Max. Speed (ns)</th>
<th>Typ. Power (mW)</th>
</tr>
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<tbody>
<tr>
<td>IDT10484</td>
<td>16K (4K x 4) 10K ECL</td>
<td>7</td>
<td>700</td>
</tr>
<tr>
<td>IDT100484</td>
<td>16K (4K x 4) 100K ECL</td>
<td>7</td>
<td>500</td>
</tr>
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<td>IDT101484</td>
<td>16K (4K x 4) 10K ECL</td>
<td>7</td>
<td>700</td>
</tr>
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<td>IDT10490</td>
<td>64K (64K x 1) 10K ECL</td>
<td>8</td>
<td>420</td>
</tr>
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<td>IDT100490</td>
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<td>8</td>
<td>320</td>
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<td>IDT101490</td>
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<td>700</td>
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<tr>
<td>IDT100494</td>
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<tr>
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<td>700</td>
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<td>IDT10496RL</td>
<td>64K (16K x 4) 10K STRAM</td>
<td>12</td>
<td>1000</td>
</tr>
<tr>
<td>IDT100496RL</td>
<td>64K (16K x 4) 100K STRAM</td>
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<tr>
<td>IDT101496RL</td>
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<td>12</td>
<td>1000</td>
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<tr>
<td>IDT10504</td>
<td>256K (64K x 4) 10K ECL</td>
<td>12</td>
<td>800</td>
</tr>
<tr>
<td>IDT100504</td>
<td>256K (64K x 4) 100K ECL</td>
<td>12</td>
<td>600</td>
</tr>
<tr>
<td>IDT101504</td>
<td>256K (64K x 4) 10K ECL</td>
<td>12</td>
<td>800</td>
</tr>
</tbody>
</table>

BiCEMOS is a trademark of Integrated Device Technology, Inc.
TECHNOLOGY UPDATE

Notebook software from Laboratory Technologies (Wilmington, MA) controls the system.

Hewlett-Packard's B-size labors have still left the company time to develop C-size units. A 500-MHz digitizing oscilloscope is a significant addition to the range of instrumentation available in C-size VXIbus format. The oscilloscope comes in a 2-slot module. It has a vertical resolution of 8 bits, a record length of 1024 points, and a digitizing rate of 20M samples/sec.

C-size modules promise to be the most popular for professional systems, and Racal-Dana emphasizes these products. A high-end time-interval analyzer is a noteworthy addition to the company's range. The analyzer stores as many as 8000 samples on each of its 250-MHz-bandwidth input channels. The time-interval single-shot resolution is 8 psec. The $14,950 price is well below what you might expect to pay for equivalent performance in a stand-alone alternative.

Another important instrument addition is Schlumberger Technologies' C-size, single-slot frequency-response analyzer. The analyzer outputs sine, square, and triangular waves with frequencies of 1 mHz to 20 kHz. The analyzer measures both polar and Cartesian coordinates. It has an amplitude resolution of 0.1 dB over a 100-dB dynamic range and a phase resolution of 0.01°.

One of the promises the VXIbus has yet to deliver is lower product prices. HP's B-size modules cost $1000 and less, but prices for C-size units generally equate to what you'd pay for a rack-and-stack alternative. Vendors argue that although the price of individual VXIbus modules may be high, the complete system cost will be lower than that of rack-and-stack systems because of the common enclosure and power supply and simpler system integration. This last advantage is sure to bring a wry smile to the faces of case-hardened system integrators, who heard similar comments at the advent of IEEE-488. Nonetheless, the downsizing, module interoperability, and promise of a common command language must all result in cost benefits at some point. The fact is that while module, expect to pay close to $20,000.

VXIbus newcomers are often concerned about how well products from different vendors will function together. Novice system integrators will no doubt avoid the issue by purchasing all system components from a single vendor. HP, Racal-Dana, and Tektronix/Colorado Data Systems all have product ranges broad enough to let you make such a purchase. But this approach may indicate unwarranted caution on your part.

Because engineers exclusively pioneered the VXIbus, the specifications for the mechanical and electrical operation of bus modules are well defined. These same engineers, keen to test the compatibility of their designs, persuaded their companies to participate early on in product interoperability trials with competitor's units. Trials continue at the rate of three or four times a year, and the VXIbus Consortium considers organizing this activity a
The 8105i power-supply functional-test system from NH Research uses eight C-size modules for switching, transient analysis, and limit detection.

are now an instrument’s device-dependent commands will become common to instruments from all vendors. The development of the SCPI specification is under the auspices of the SCPI Consortium, which includes the same member companies as the VXI Consortium. The consortium publishes the SCPI document, which you can purchase for $75 by contacting Bode Enterprises.

primary responsibility. Currently only a few minor problems arise, which should inspire confidence that you can safely mix and match units from different vendors. Principal participants in interoperability testing include Colorado Data Systems, Fluke/Philips (Everett, WA), Hewlett-Packard, National Instruments, Racal-Dana, Tektronix, and Wavetek.

Software incompatibility between vendors’ VXIbus products is a prevailing system integrator’s headache, but a remedy is on the horizon. SCPI (pronounced skippy) stands for standard commands for programmable instrumentation. This specification continues from where IEEE-488.2 left off and applies equally to conventional instrumentation and VXIbus instruments. SCPI aims to standardize command codes for any operation that an instrument performs. What

Vendors with existing products are unlikely to backtrack on designs in order to implement SCPI. So some time will pass before the majority of VXIbus instruments conforms to the specification. Indeed, most IEEE-488-interface implementations have yet to catch up with IEEE-488.2 command syntax. Hewlett-Packard has a temporary edge on competitors in making its

Fig 1—The VXIbus product directory follows this organization.

EDN November 22, 1990
THE COMPLETE FAMILY OF µP SUPERVISORS

Pick Your Functions, Performance and Price

From 68040s to 8048s, Maxim has the supervisor for your microprocessor application. Maxim's MAX690 Family of supervisory circuits increases system reliability by monitoring the power supply and performing common µP "housekeeping" functions, such as power-on-reset, backup battery switching, watchdog timing, CMOS RAM write protection, power fail or low battery monitoring, and manual reset.

The supervisors require no external components when monitoring +5V systems, so they're easy to design in. Compact 8-pin or 16-pin DIP and SO packages save valuable board area.

<table>
<thead>
<tr>
<th>FUNCTIONS</th>
<th>MAX 690</th>
<th>MAX 691</th>
<th>MAX 696</th>
<th>MAX 697</th>
<th>MAX 699</th>
<th>MAX 700</th>
<th>MAX 701</th>
<th>MAX 790</th>
<th>MAX 791</th>
<th>MAX 1232</th>
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<td>Fixed Power-Up/Down Reset</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<td>Variable Power-Up/Down Reset</td>
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<td>✓</td>
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<td>✓</td>
<td>✓</td>
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<tr>
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<td>✓</td>
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<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Watchdog Timer</td>
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<td>✓</td>
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<td>✓</td>
<td>✓</td>
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<td>✓</td>
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<td>$3.55</td>
<td>$3.27</td>
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<td>$2.12</td>
<td>$2.17</td>
<td>$1.96</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

†Consult factory for pricing and availability.

5V Supervisor Uses Only 200µA

The MAX700 includes a 5V monitor, RESET and RESSET outputs, and debounced manual reset input, but consumes only 200µA.

Full-Function 5V Supervisor

The MAX690 features a 5V monitor, battery backup switch, watchdog timer, and a comparator for early power-fail warning or battery sending.

See For Yourself

For a free booklet describing Maxim's supervisory circuits in more detail, write Maxim Integrated Products 120 San Gabriel Drive, Sunnyvale, CA 94086, or call (408) 737-7600 (x 4000), or FAX (408) 737-7194.

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For more information on the VXIbus products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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FAX (508) 832-6097  
Circle No. 700

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9250 Brown Deer Rd  
San Diego, CA 92120  
(619) 530-0085  
FAX (619) 486-6267  
Circle No. 708

National Instruments Corp  
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Austin, TX 78730  
(512) 784-0100  
FAX (512) 794-8411  
Circle No. 716

Blakell Systems Ltd  
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Blanford Forum D’T11 7TE, UK  
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FAX (258) 480-183  
Circle No. 701

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Bradenton, FL 34208  
(813) 746-7515  
FAX (813) 746-8501  
Circle No. 709

NH Research Inc  
16601 Hale Ave  
Irvine, CA 92714  
(714) 474-7900  
FAX (714) 474-7062  
Circle No. 717

Bode Enterprises  
3389 Hercules Dr, Suite P3  
La Mesa, CA 92034  
(619) 697-7970  
Circle No. 702

Hewlett-Packard Co  
Box 301  
Loveland, CO 80539  
(303) 752-0900  
Circle No. 710

North Atlantic Industries Inc  
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Hauppauge, NY 11788  
(516) 582-6500  
FAX (516) 582-8079  
Circle No. 718

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Campbell, CA 95008  
(408) 371-0666  
FAX (408) 371-0672  
Circle No. 703

ICS Electronics Inc  
744 S Hillview Dr  
Milpitas, CA 95035  
(408) 283-5500  
FAX (408) 283-5896  
Circle No. 711

Quartzlock Instruments  
Gothic, Plymouth Rd  
Totnes TQ9 5LH, UK  
(039) 862062  
FAX (800) 867062  
Circle No. 719

C&H Engineering Inc  
8700 Shool Creek, Suite 107  
Austin, TX 78758  
(512) 467-7444  
FAX (512) 834-9165  
Circle No. 704

ILC Data Device Corp  
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(516) 567-5900  
FAX (516) 567-7358  
Circle No. 712

Racal-Dana Instruments Inc  
4 Goodyear St  
Irvine, CA 92718  
(714) 859-8999  
FAX (714) 859-2505  
Circle No. 720

Colorado Data Systems Inc  
3301 W Hampden Ave, Unit C  
Englewood, CO 80110  
(303) 782-1640  
FAX (303) 781-0253  
Circle No. 705

Kikusui International Corp  
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Torrance, CA 90603  
(213) 571-4662  
FAX (213) 542-4943  
Circle No. 713

Racal Instruments Ltd  
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Sloough SL1 6BE, UK  
(628) 644-455  
FAX (628) 620-107  
Circle No. 721

Datron Instruments Ltd  
Hurricane Way  
Norwich NR6 6IB, UK  
(603) 404-824  
FAX (603) 458-670  
Circle No. 706

Marconi Instruments Ltd  
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Dundeehive KY11 4BE, UK  
(383) 822-131  
Circle No. 714

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Beaverton, OR 97006  
(503) 950-004  
FAX (503) 690-1228  
Circle No. 722

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(408) 945-1477  
FAX (408) 945-9777  
Circle No. 707

Matris Systems Corp  
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(818) 992-6776  
FAX (818) 992-8221  
Circle No. 715

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FAX (252) 543-954  
Circle No. 723

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High Interest 518  Medium Interest 519  Low Interest 520
QUAD COMPARATORS
8ns, 18mW-ONLY $1.50*

♦ +5V Operation Cuts Power Drain and Heat Dissipation
♦ Input Range Includes Ground and Eliminates Need For Negative Supply
♦ Four Comparators in One Package Saves Board Space and Reduces Cost
♦ Separate AGND and DGND Minimizes Noise, Improves System Performance
♦ Dual Supply ±5V Capability Allows Bipolar Input Range

One Stop Shopping For High Speed/Low Power

Maxim's new MAX900 and MAX901 quad comparators can deliver both high speed and low power at a price that compares favorably to high speed single or dual equivalents. MAX900/MAX901 offer you propagation delays of only 8ns with a 5mV overdrive, power dissipation of 18mW per comparator (when powered from a +5V supply) and space saving 0.3" DIP or small outline (SO) packages - for only $1.50 per comparator.

Maxim’s High Speed Comparator Family

<table>
<thead>
<tr>
<th>Part Number</th>
<th># Comps</th>
<th>Logic</th>
<th>Delay (typ)</th>
<th>Latch</th>
<th>Package</th>
<th>Price</th>
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<td>4</td>
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<td>8.0ns</td>
<td>Yes</td>
<td>DIP, SO</td>
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<td>MAX901</td>
<td>4</td>
<td>TTL</td>
<td>8.0ns</td>
<td>No</td>
<td>DIP, SO</td>
<td>$5.98</td>
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<tr>
<td>MAX9685</td>
<td>1</td>
<td>ECL</td>
<td>1.3ns</td>
<td>Yes</td>
<td>DIP, SO, Can</td>
<td>$3.38</td>
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<tr>
<td>MAX9686</td>
<td>1</td>
<td>TTL</td>
<td>6.0ns</td>
<td>Yes</td>
<td>DIP, SO, Can</td>
<td>$2.31</td>
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<td>MAX9687</td>
<td>2</td>
<td>ECL</td>
<td>1.4ns</td>
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<td>DIP, SO, Can</td>
<td>$5.12</td>
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<td>MAX9690</td>
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<td>ECL</td>
<td>1.3ns</td>
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<td>TTL</td>
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<td>Yes</td>
<td>DIP, SO</td>
<td>$3.92</td>
</tr>
</tbody>
</table>

* MAX901, 1000-up F.O.B. USA price per comparator. † 1000-up F.O.B. USA

Call your Maxim representative or distributor today for applications information, datasheets and samples. Or, write Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194. Credit cards may be used for small orders.
VXIbus products SCPI compatible because SCPI was developed from the company’s in-house test-and-measurement system language, TMSL. All HP VXIbus modules are TMSL compatible. The company is in the best position to offer SCPI-compatible products once the specification is cast in stone.

If after all this striving for compatibility and standardization you remain unconvinced that products from different vendors can successfully work together in a single system, then a small number of system-integration services can offer consolation. These companies take overall responsibility for building and commissioning your system. Such companies include C&H Engineering, Marconi Instruments, Racal-Dana, and Tasco; their addresses are included in the For more information... box.

This box also includes some other addresses that are useful for VXIbus followers. Bode Enterprises publishes the VXIbus Newsletter, which costs $195 per year and features topical information about products and events. Another publication dedicated to VXIbus fans is VXIjournal. First issued in July 1990, it appears quarterly and is free to qualified readers.

The organization of this year’s VXIbus directory appears in Fig 1. All products fall into one of two main categories: computers or instruments. Further subdivisions lead to a recognizable product description. Chassis and software products do not appear in this directory. EDN plans to survey these product areas in future issues. The directory lists only products that are available now or will be available during the first quarter of 1991.

Reference

Table 1—VXIbus products

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Description</th>
<th>Model</th>
<th>Size</th>
<th>Key features</th>
<th>Price</th>
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<tr>
<td>CAL-AV Labs</td>
<td>Fiber interface</td>
<td>9210</td>
<td>C1</td>
<td>4 channels, TTL input to fiber output</td>
<td>$1500</td>
</tr>
<tr>
<td></td>
<td>Fiber interface</td>
<td>9211</td>
<td>D1</td>
<td>6 channels, TTL input to fiber output</td>
<td>$1750</td>
</tr>
<tr>
<td></td>
<td>Fiber interface</td>
<td>9912</td>
<td>C1</td>
<td>4 channels, fiber input to TTL output</td>
<td>$1300</td>
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<tr>
<td></td>
<td>Fiber interface</td>
<td>9915</td>
<td>D1</td>
<td>6 channels, fiber input to TTL output</td>
<td>$1750</td>
</tr>
<tr>
<td>Colorado Data Systems</td>
<td>Controller</td>
<td>73A-160</td>
<td>C4</td>
<td>12-MHz 80286/87 based, as much as 4M bytes of RAM, 20M-byte hard disk, 3½- and 5¼-in. floppy-disk drive, IEEE-488 port</td>
<td>$5200</td>
</tr>
<tr>
<td></td>
<td>Controller</td>
<td>73A-161</td>
<td>C3</td>
<td>Same as 73A-160 but only 3½-in. floppy-disk drive</td>
<td>$5200</td>
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<tr>
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<td>Digital I/O</td>
<td>73A-411</td>
<td>C1</td>
<td>48 opcodes, bidirectional TTL/CMOS-level lines</td>
<td>$2200</td>
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<tr>
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<td>Digital I/O</td>
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<td>C1</td>
<td>10 bytes, programmable as inputs or outputs</td>
<td>$1800</td>
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<tr>
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<td>Slot 0</td>
<td>73A-151B</td>
<td>C1</td>
<td>Resource manager, IEEE-488 port</td>
<td>$2700</td>
</tr>
<tr>
<td></td>
<td>Slot 0</td>
<td>73A-156</td>
<td>C1</td>
<td>Modular ATE compliant, IEEE-488 port</td>
<td>$2800</td>
</tr>
<tr>
<td>Hewlett-Packard</td>
<td>Controller</td>
<td>E1480A</td>
<td>C4</td>
<td>25-MHz 68030 based, as much as 16M bytes of RAM, IEEE-488 port</td>
<td>$9950</td>
</tr>
<tr>
<td></td>
<td>RS-232C/422 interface</td>
<td>E1324A</td>
<td>A1</td>
<td>19,200 baud</td>
<td>$650</td>
</tr>
<tr>
<td></td>
<td>Digital I/O</td>
<td>E1330A</td>
<td>B1</td>
<td>Quad 8-bit bidirectional TTL-level data</td>
<td>$600</td>
</tr>
<tr>
<td></td>
<td>Slot 0</td>
<td>E1405A</td>
<td>C1</td>
<td>Resource manager, IEEE-488 interface</td>
<td>$2800</td>
</tr>
<tr>
<td>ICS Electronics</td>
<td>Interface</td>
<td>5523</td>
<td>C1</td>
<td>56 I/O lines, power and control for OEM cards</td>
<td>$700</td>
</tr>
<tr>
<td>National Instruments</td>
<td>Controller</td>
<td>VXipc-386</td>
<td>C1</td>
<td>20-MHz 80386 based, as much as 8M bytes of RAM, 40M-byte hard disk, IEEE-488.2 port, optional 210M-byte hard-disk and 3½-in. floppy-disk drive in C2 module</td>
<td>$9000</td>
</tr>
<tr>
<td></td>
<td>Controller</td>
<td>VXipc-030</td>
<td>C2</td>
<td>Apple Mac SE/30 compatible, as much as 8M bytes of RAM, 80M-byte hard disk, IEEE-488.2 port</td>
<td>$14,800</td>
</tr>
<tr>
<td></td>
<td>Slot 0 card</td>
<td>GPIB-VXI</td>
<td>C1</td>
<td>Resource manager, IEEE-488-to-VXI interface</td>
<td>$3000</td>
</tr>
<tr>
<td></td>
<td>Slot 0 card</td>
<td>VXI-MXI</td>
<td>C1</td>
<td>Extends VXIbus to MXIbus</td>
<td>$1995</td>
</tr>
<tr>
<td></td>
<td>IBM PCI/AT-to-VXI interface</td>
<td>VXI-AT2000</td>
<td>C1</td>
<td>Includes plug-in PC card and slot 0 card linked by 2m cable, MXIbus and LabWindow software</td>
<td>$3800</td>
</tr>
<tr>
<td></td>
<td>IBM PCI/AT-to-VXI interface</td>
<td>VXI-AT2021</td>
<td>C1</td>
<td>Same as VXI-AT2000 but with SCO Xenix</td>
<td>$3800</td>
</tr>
<tr>
<td></td>
<td>IBM PCI/AT-to-VXI interface</td>
<td>VXI-AT2022</td>
<td>C1</td>
<td>Same as VXI-AT2000 but with SCO Unix</td>
<td>$3800</td>
</tr>
<tr>
<td></td>
<td>IBM PCI/AT-to-VXI interface</td>
<td>VXI-AT2023</td>
<td>C1</td>
<td>Same as VXI-AT2000 but with ISC 386ix</td>
<td>$3800</td>
</tr>
<tr>
<td></td>
<td>IBM PS/2-to-VXI interface</td>
<td>VXI-MC2000</td>
<td>C1</td>
<td>Same as VXI-AT2000 but for IBM PS/2 and DOS</td>
<td>$4500</td>
</tr>
<tr>
<td></td>
<td>IBM PS/2-to-VXI interface</td>
<td>VXI-MC2020</td>
<td>C1</td>
<td>Same as VXI-MC2000 but with OS/2</td>
<td>$4600</td>
</tr>
<tr>
<td></td>
<td>IBM 6000-to-VXI interface</td>
<td>VXI-MC6000</td>
<td>C1</td>
<td>Same as VXI-AT2000 but for IBM 6000 and AIX software</td>
<td>$4600</td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Digital input/output</td>
<td>1260-14</td>
<td>C1</td>
<td>96 bidirectional CMOS or TTL channels</td>
<td>$1795</td>
</tr>
<tr>
<td></td>
<td>Slot 0 controller</td>
<td>1260-00B</td>
<td>C1</td>
<td>Resource manager, IEEE-488-to-VXI interface</td>
<td>$3000</td>
</tr>
<tr>
<td></td>
<td>System controller</td>
<td>1265</td>
<td>C2</td>
<td>16- or 20-MHz 80386/87 based, as much as 8M bytes of RAM, 40M-byte hard disk, 3½-in. floppy-disk drive</td>
<td>$9000</td>
</tr>
</tbody>
</table>

Table continued
8x8 VIDEO CROSSPOINT SWITCH WITH BUFFERS
-ONLY $2.50*/CHANNEL

Connects Any Input to Any Output

Maxim's new MAX456 is the first monolithic 8x8 video crosspoint switch that routes standard video signals (NTSC, PAL, SECAM). With a digitally controlled 8x8 switch matrix, control logic, and eight 35MHz output buffers together in a 40-pin DIP or 44-pin PLCC, the MAX456 significantly reduces component count, board space and cost over discrete designs. Applications include video surveillance, imaging, visual automation, and video editing.

**MAX456 Eliminates Over 20 Components**

- Reduces Board Space up to 5X
- Reduces Cost 5X Compared to Discrete Designs
- Reduces Design and Layout Time
- Reduces Stray Capacitances
- Improves Reliability

Build Larger Crosspoint Arrays

Each MAX456 buffer output can be disabled under logic control. With three-state outputs, multiple MAX456s can be paralleled to form larger switch networks.

- **Eight Internal Buffers**
  250V/µs Slew Rate
  35MHz Bandwidth
  Buffer Disable Saves Power

- ±5V Power Supplies
- 80dB Off Isolation at 5MHz
- 70dB Crosstalk at 5MHz
- Serial or Parallel µP Interface

**MAX456 and MAX457s Drive 75Ω Loads**

Maxim also offers the MAX457, a dual 70MHz unity gain stable video amplifier. The MAX456 teams up with the MAX457 to drive 75Ω loads efficiently. Special pricing is available for MAX456/MAX457 combination purchases.

Call your Maxim representative or distributor today for applications information, data sheets, and free samples. Or, contact Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086, (408) 737-7600, FAX (408) 737-7194

* MAX456CPL, $19.98 1000-up
F.O.B. U.S.A price

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## TECHNOLOGY UPDATE

### Table 1—VXbus products (continued)

<table>
<thead>
<tr>
<th>Computer-hardware products (continued)</th>
<th>Vendor</th>
<th>Description</th>
<th>Model</th>
<th>Size</th>
<th>Key features</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slot 0</td>
<td>Tektronix</td>
<td>VX64520 C1</td>
<td>Resource manager, IEEE-488.2 port</td>
<td>$3200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slot 0</td>
<td>Tektronix</td>
<td>VX65520 D1</td>
<td>Resource manager, IEEE-488 port</td>
<td>$4250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System controller</td>
<td>Tektronix</td>
<td>VX64530 C2</td>
<td>16-MHz 80386/87 based, 2 M bytes of RAM, 40-Mbyte hard disk,IEEE-488 port</td>
<td>$11,750</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System controller</td>
<td>Tektronix</td>
<td>VX64535 C2</td>
<td>Same as VX64530 but 20-MHz 80386/87 based, 8 M bytes of RAM</td>
<td>$17,500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System controller</td>
<td>Tektronix</td>
<td>VX65530 D2</td>
<td>Same as VX64530 but D size</td>
<td>$18,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System controller</td>
<td>Tektronix</td>
<td>VX65535 D2</td>
<td>Same as VX64535 but D size</td>
<td>$24,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Universal Test Equipment</td>
<td>Controller</td>
<td>VX2000 A1</td>
<td>Specifically for control of this company’s modules</td>
<td>$725</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Universal Test Equipment</td>
<td>Display</td>
<td>VX3856 A1, B1</td>
<td>8-character, 14-LED segments; register based</td>
<td>$725</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Universal Test Equipment</td>
<td>Logic monitor</td>
<td>VX3872 A1, B1</td>
<td>Threshold programmable ±12V; low, high, pulse detection</td>
<td>$725</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Measurement instruments

| Analogic | A/D converter | DVX2502 B1 | 8-channel multiplexer, 200-kHz sampling, 16 bit | $3700 |
| Analogic | A/D converter | DVX2503 B1 | 8-channel multiplexer, 400-kHz sampling, 16 bit | $4500 |
| S/H amplifier | DVX2601 B1 | 16-channel multiplexer, 200-kHz sampling | $3800 |
| Anadigm | Universal counter/timer | 73A-541 C1 | 10 MHz, 100-nsec resolution, channels, time-tag storage | $2400 |
| Datron Instruments | Digital multimeter | 1362 C1 | 6½ digits, 1000 readings/sec, current and ratio | $4250 |
| EIP Microwave | Microwave frequency counter | 1231A C3 | 20 GHz, CW, or 50-nsec pulse | $12,700 |
| EIP Microwave | Microwave frequency counter | 1230A C3 | 26.5 GHz, CW, or 50-nsec pulse, 170-GHz option | $17,000 |
| Hewlett-Packard | Digital multimeter | E1329 A2 | 5½ digits, 14,000 readings/sec | $1200 |
| Hewlett-Packard | Digital multimeter | E1410 A1 | 6½ digits, 1450 readings/sec | $3500 |
| Hewlett-Packard | Digital multipler | E1411 A1 | Same as E1362A | $1800 |
| Hewlett-Packard | Oscilloscope (digitizing) | E1425 A1 | 500-MHz bandwidth, 4 channels, 20M samples/sec, 8 bit | $6950 |
| Hewlett-Packard | Power meter | E1416 A1 | 100 kHz to 50 GHz, –70 to +40 dBm, sensor option | $2500 |
| Hewlett-Packard | Universal counter/timer | E1339 A1 | 4 MHz, 200-nsec resolution, 4 channels | $900 |
| Hewlett-Packard | Universal counter/timer | E1333 A1 | 1 GHz, 1-nsec resolution, 3 channels | $900 |
| Hewlett-Packard | Universal counter/timer | E1420 A1 | 200 MHz, 2-nsec resolution | $3450 |
| Racal-Dana | A/D converter | 4070 C1 | 40-MHz sampling, 8-bit resolution, 16k bits of memory | $4966 |
| Racal-Dana | Digital multimeter | 4061 C1 | 8½ digits, 1000 readings/sec | $2600 |
| Racal-Dana | Microwave frequency counter | 2051 C2 | 6½ digits, 9000 readings/sec | $3595 |
| Racal-Dana | Microwave frequency counter | 2151 C2 | 20 GHz, 9 digits, 3 inputs | $4585 |
| Racal-Dana | Power meter | 4051 C1 | 200 kHz to 25.5 GHz, –60 to +25 dBm, sensor option | $3147 |
| Racal-Dana | Universal counter/timer | 2251 C1 | 1.3-GHz, 9 digits 1-nsec single shot resolution | $3250 |
| Racal-Dana | Time-interval analyzer | 2351 C2 | 250 MHz, 8-psec resolution, 8000-sample storage | $14,950 |
| Schlumberger Technologies | Frequency-response analyzer | 1270 C1 | Generates sine, square, triangle waves; 1 MHz to 20 kHz, 2-channel analyzer, 0.01 dB and 0.01° resolution | $12,200 |
| Tektronix | Digital multimeter | VX4236 C1 | 6½ digits, 1000 readings/sec | $3750 |
| Tektronix | Universal counter/timer | VX4223 C2 | 160 MHz, 1-nsec resolution, 2 channels, 1.3-GHz option | $3500 |
| Universal Test Equipment | Ammeter | VX3064 A1, B1 | 4½ digits, 6 ranges to 1A, 4-wire sense | $725 |
| Universal Test Equipment | Digital multimeter | VX3888 A1, B1 | 4½ digits; voltage, current, resistance register based | $725 |
| Universal Test Equipment | Digital voltmeter | VX3890 A1, B1 | 4½ digits, dc and ac rms and p-p voltage to 10 kHz | $725 |
| Veretest | LCR meter | 3100 C1 | Polar and cartesian coordinate output, 1 kHz to 1 MHz | $3000 |

### Sources

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Description</th>
<th>Model</th>
<th>Size</th>
<th>Key features</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Colorado Data Systems</td>
<td>Arbitrary-pulse generator</td>
<td>73A-270 C1</td>
<td>2 channels, 1600 programmable pulse durations</td>
<td>$3500</td>
<td></td>
</tr>
<tr>
<td>Colorado Data Systems</td>
<td>Arbitrary-waveform generator</td>
<td>37A-243 C1</td>
<td>0.8 Hz to 25 MHz, 12-bit verticalx16 bit horizontal</td>
<td>$4100</td>
<td></td>
</tr>
<tr>
<td>Colorado Data Systems</td>
<td>D/A converter</td>
<td>73A-256 C1</td>
<td>12 channels, 16-bit resolution, ±16.4V output</td>
<td>$4050</td>
<td></td>
</tr>
<tr>
<td>Colorado Data Systems</td>
<td>Resistance source</td>
<td>73A-342 C2</td>
<td>2 outputs, 100 to 41 kΩ, or 100 to 410 kΩ</td>
<td>$2000</td>
<td></td>
</tr>
<tr>
<td>Hewlett-Packard</td>
<td>D/A converter</td>
<td>E1329 A2</td>
<td>4 channels, 16-bit resolution, ±10V output</td>
<td>$1100</td>
<td></td>
</tr>
<tr>
<td>Hewlett-Packard</td>
<td>Function generator</td>
<td>E1440 A2</td>
<td>21-MHz sine, amplitude/phase modulation, sweep mode</td>
<td>$5750</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Arbitrary-pulse generator</td>
<td>3051 C1</td>
<td>2 channels, 1600 programmable pulse durations</td>
<td>$3920</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Arbitrary-waveform generator</td>
<td>3052 C1</td>
<td>1.5 Hz to 25 MHz, 10-bit verticalx16 bit horizontal</td>
<td>$4400</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>D/A converter</td>
<td>6065 C1</td>
<td>12 channels, 16-bit resolution, ±16.4V output</td>
<td>$4050</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Frequency standard</td>
<td>3351R C2</td>
<td>Rubidium source, stability &lt; 5x10⁻¹¹/ month</td>
<td>$10,950</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Frequency standard</td>
<td>3351E C2</td>
<td>Ovened crystal, stability &lt; 5x10⁻¹¹/ day</td>
<td>$2485</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Resistance source</td>
<td>4071 C1</td>
<td>2 channels, serial, 5-MHz bit-rate analyzer</td>
<td>$14,950</td>
<td></td>
</tr>
<tr>
<td>Racal-Dana Instruments</td>
<td>Universal controller</td>
<td>VX3996 A1, B1</td>
<td>10 to 1 MΩ, register based</td>
<td>$725</td>
<td></td>
</tr>
<tr>
<td>Veretest</td>
<td>Voltage and current source</td>
<td>3380 C1</td>
<td>Dual, bipolar, 8W, 250 µV to 38V, 20 µA to 1A</td>
<td>$3500</td>
<td></td>
</tr>
<tr>
<td>Wavetek</td>
<td>Arbitrary-waveform generator</td>
<td>1375 C1</td>
<td>1 MHz to 20 MHz, 12-bit verticalx16 bit horizontal</td>
<td>$4995</td>
<td></td>
</tr>
</tbody>
</table>

---

Table continued
The mil-spec solderless switch for land, sea or air.

Our QUIK-CONNECT™ module is physically separate from the switch. It can be pre-wired without solder and pre-checked for correct continuity. The QUIK-CONNECT™ module can then simply be pressed into place in the Vivisun Series 95 switch.

It's also compatible with NVIS night vision goggles per MIL-S-85762A. A unique optics system eliminates the glare. When voltages are trimmed, the switch is easily readable with the unaided eye. It's also readable in direct sunlight and deadface when not energized.

Compact and light. No other Mil-Spec switch can match it. Options: High-Impact Shock • Dustproof/Dripproof/Watertight/Splashproof • Split Ground • Standard Solder Terminations • EMI

Contact us today.

AEROSPACE OPTICS INC.
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 • Telex 75-8461 • Fax (817) 654-3405

Vivisun Series 95, the advanced QUIK-CONNECT™ solderless pushbutton switch.

VIVISUN 95™
MIL-S-22885/108
## Table 1—VXbus products (continued)

### Synchro/resolver instrumentation

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Description</th>
<th>Model</th>
<th>Size</th>
<th>Key features</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILC Data Device</td>
<td>Synchro converter</td>
<td>IAC-37001</td>
<td>C1</td>
<td>Synchro/digital and digital/synchro conversion, 16- or 20-bit resolution, 18-arc sec accuracy</td>
<td>$5950</td>
</tr>
<tr>
<td>North Atlantic Industries</td>
<td>Phase-angle voltmeter</td>
<td>VX2177</td>
<td>C1</td>
<td>3 mV to 300V, 10 Hz to 100 kHz, 0.25° accuracy</td>
<td>$7995</td>
</tr>
<tr>
<td>Transmagnetics</td>
<td>Digital/synchro converter</td>
<td>5410C-42</td>
<td>C1</td>
<td>7 single-speed channels, 1+2 multiplexed channels, 14-bit to resolver output</td>
<td>$8870</td>
</tr>
<tr>
<td></td>
<td>Synchron/digital converter</td>
<td>5410C-48-1</td>
<td>C1</td>
<td>4 channels, 18-bit to resolver output</td>
<td>$8870</td>
</tr>
<tr>
<td></td>
<td>Phase-angle standard</td>
<td>4510C-43</td>
<td>C1</td>
<td>5 single-speed channels, 1+2 multiplexed channels to 12- or 20 bit, respectively</td>
<td>$7483</td>
</tr>
<tr>
<td></td>
<td>Phase-angle voltmeter</td>
<td>5410C-47-1</td>
<td>C1</td>
<td>3 mV to 300V, 10 Hz to 100 kHz, 0.25° accuracy</td>
<td>$7950</td>
</tr>
<tr>
<td></td>
<td>Torque simulator</td>
<td>5410C-49-1</td>
<td>C1</td>
<td>Same as 5410C-31, but phase accuracy 0.1°</td>
<td>$7950</td>
</tr>
<tr>
<td></td>
<td>Torque simulator</td>
<td>5410C-51</td>
<td>C1</td>
<td>3 channels, 118V output from 12-bit input from input reference</td>
<td>$6850</td>
</tr>
</tbody>
</table>

### Miscellaneous instruments

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Description</th>
<th>Model</th>
<th>Size</th>
<th>Key features</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analogic</td>
<td>Solid-state multiplexer</td>
<td>DXV2701</td>
<td>B1</td>
<td>32 channels, ±10V input, 150-nsec switching</td>
<td>$995</td>
</tr>
<tr>
<td>CAL-AV Labs</td>
<td>Amplifier</td>
<td>9930</td>
<td>C1</td>
<td>4 channels, 500 MHz, 20-dB gain, 72-dB dynamic range</td>
<td>$3500</td>
</tr>
<tr>
<td></td>
<td>Amplifier</td>
<td>9931</td>
<td>D1</td>
<td>4 channels, 1 GHz, 14-dB gain, 65-dB dynamic range</td>
<td>$3700</td>
</tr>
<tr>
<td></td>
<td>Amplifier</td>
<td>9932</td>
<td>D1</td>
<td>6 channels, 500 MHz, 20-dB gain, 72-dB dynamic range</td>
<td>$5050</td>
</tr>
<tr>
<td></td>
<td>Amplifier</td>
<td>9933</td>
<td>D1</td>
<td>6 channels, 1 GHz, 14-dB gain, 65-dB dynamic range</td>
<td>$5350</td>
</tr>
<tr>
<td></td>
<td>Attenuator</td>
<td>9930</td>
<td>D1</td>
<td>4 channels, 1 GHz, 63-dB in 1-dB steps, 10W</td>
<td>$3100</td>
</tr>
<tr>
<td></td>
<td>Attenuator</td>
<td>9921</td>
<td>C1</td>
<td>4 channels, 1 GHz, 127-dB in 1-dB steps, 1W</td>
<td>$3500</td>
</tr>
<tr>
<td></td>
<td>Attenuator</td>
<td>9922</td>
<td>C1</td>
<td>6 channels, 1 GHz, 63-dB in 1-dB steps, 1W</td>
<td>$4400</td>
</tr>
<tr>
<td></td>
<td>Attenuator</td>
<td>9923</td>
<td>D1</td>
<td>6 channels, 1 GHz, 127-dB in 1-dB steps, 1W</td>
<td>$4900</td>
</tr>
<tr>
<td>Colorado Data Systems</td>
<td>MIL-STD-1553A/B bus</td>
<td>73A-453</td>
<td>C1</td>
<td>Bus controller, remote terminal, bus monitor</td>
<td>$3600</td>
</tr>
<tr>
<td></td>
<td>MIL-STD-1553A/B bus tester</td>
<td>73S-456</td>
<td>C1</td>
<td>2 channels, 8 channel option</td>
<td>$9500</td>
</tr>
<tr>
<td></td>
<td>Switch-relay</td>
<td>73A-355</td>
<td>C1</td>
<td>24 channels, dsp or spdt, 30V, 4A rating</td>
<td>$1900</td>
</tr>
<tr>
<td></td>
<td>Switch-relay</td>
<td>73A-356</td>
<td>C1</td>
<td>20 channels, dsp, 30V, 3A rating, 100 operations/sec</td>
<td>$1950</td>
</tr>
<tr>
<td></td>
<td>Switch-relay</td>
<td>73A-357</td>
<td>C1</td>
<td>32 channels, 30V, 4A rating, 100 operations/sec</td>
<td>$1600</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-master</td>
<td>73A-332</td>
<td>C1</td>
<td>40x2-wire channels, 80 channelsselc, 4-digit display</td>
<td>$2000</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-master</td>
<td>73A-372</td>
<td>C1</td>
<td>2x-4x2-wire channels, controlled via local bus</td>
<td>$1500</td>
</tr>
<tr>
<td>Hewlett-Packard</td>
<td>Amplifier</td>
<td>E1361A</td>
<td>B1</td>
<td>2x or 4x4, 10-MHz</td>
<td>$650</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-solid-state</td>
<td>E1351A</td>
<td>B1</td>
<td>16x2-wire channels, 16V input, 100-kHz scan rate</td>
<td>$675</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-solid-state</td>
<td>E1352A</td>
<td>B1</td>
<td>Same as E1351A but 32 single-wire channels</td>
<td>$1000</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-solid-state</td>
<td>E1353A</td>
<td>B1</td>
<td>Same as E1351A but with cold-junction compensation</td>
<td>$975</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-solid-state</td>
<td>E1354A</td>
<td>B1</td>
<td>6 channels, 1200 strain gauge</td>
<td>$1125</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-solid-state</td>
<td>E1358A</td>
<td>B1</td>
<td>8 channels, 3502 strain gauge</td>
<td>$1125</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/3, 4-wire</td>
<td>E1345A</td>
<td>B1</td>
<td>16x3-wire or 8x4-wire channels</td>
<td>$650</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/1-wire</td>
<td>E1346A</td>
<td>B1</td>
<td>48 single-wire channels, common low and guard</td>
<td>$800</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/3-wire</td>
<td>E1347A</td>
<td>B1</td>
<td>8 channels, 1200 strain gauge</td>
<td>$925</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/4-wire</td>
<td>E1355A</td>
<td>B1</td>
<td>8 channels, 3500 strain gauge</td>
<td>$925</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/RF</td>
<td>E1460A</td>
<td>C1</td>
<td>64x2-wire or 32x4-wire channels, 10-MHz bandwidth</td>
<td>$2400</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/RF</td>
<td>E1366A</td>
<td>C1</td>
<td>Dual 1x4, 500 characteristic impedance</td>
<td>$880</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/RF</td>
<td>E1367A</td>
<td>C1</td>
<td>Same as E1366A but 750 characteristic impedance</td>
<td>$850</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/RF</td>
<td>E1472A</td>
<td>C1</td>
<td>6 x 1-channel, 500 characteristic impedance</td>
<td>$2500</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/RF</td>
<td>E1473A</td>
<td>C1</td>
<td>6 x 1-channel expander for E1472A</td>
<td>$1500</td>
</tr>
<tr>
<td></td>
<td>Switch-relay</td>
<td>E1384A</td>
<td>B1</td>
<td>18 channels, 250V, 1A rating</td>
<td>$650</td>
</tr>
<tr>
<td></td>
<td>Switch-relay/microwave</td>
<td>E1388A</td>
<td>B1</td>
<td>18 channels, 250V, 3spdt, 500</td>
<td>$2100</td>
</tr>
<tr>
<td>ILC Data Device</td>
<td>MIL-STD-1553B interface</td>
<td>BUS-65522</td>
<td>B1</td>
<td>Bus controller, remote terminal, or bus monitor</td>
<td>$4995</td>
</tr>
<tr>
<td>Matrix Systems</td>
<td>Matrix switch-relay/RF</td>
<td>10081A-50</td>
<td>C1</td>
<td>4x8, 900 MHz, 7-segment status display, 500</td>
<td>$2750</td>
</tr>
<tr>
<td></td>
<td>Matrix switch-relay/RF</td>
<td>10081A-75</td>
<td>C1</td>
<td>Same as 10081A-50 but 750 characteristic impedance</td>
<td>$2750</td>
</tr>
<tr>
<td>Quartzlock Instruments</td>
<td>Attenuator</td>
<td>132VX1</td>
<td></td>
<td>1 GHz, 132-dB in 0.1-dB steps, 1.3W</td>
<td>£1800</td>
</tr>
<tr>
<td>Racial-Dana Instruments</td>
<td>Switch-relay power</td>
<td>1260-12</td>
<td>C1</td>
<td>20 channels, dsp, 50V, 1A rating</td>
<td>$3195</td>
</tr>
<tr>
<td></td>
<td>Switch-relay/RF</td>
<td>1260-20</td>
<td>C1</td>
<td>20 channels, dsp, 250V, 8A rating</td>
<td>$1695</td>
</tr>
<tr>
<td></td>
<td>MIL-STD-1553A/B bus</td>
<td>6051</td>
<td>C1</td>
<td>Bus controller, remote terminal, bus monitor</td>
<td>£4200</td>
</tr>
<tr>
<td></td>
<td>MIL-STD-1553A/B bus tester</td>
<td>6053</td>
<td>C1</td>
<td>2 channels, 8 channel option</td>
<td>£11356</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/2, 4-wire</td>
<td>1260-304</td>
<td>D1</td>
<td>40 channels, 1 x 40, 2 x 20, 41 x 10, 81 x 5</td>
<td>£1385</td>
</tr>
<tr>
<td></td>
<td>Multiplexer-relay/2, 4-wire</td>
<td>1260-35</td>
<td>C1</td>
<td>96 channels, 2 x 48, 2-wire to 8 x 64-wire</td>
<td>£2890</td>
</tr>
<tr>
<td></td>
<td>Switch-relay/relay/2-wire</td>
<td>1260-40A</td>
<td>C1</td>
<td>Configurable 4 x 24, 2 x 12, 1 x 12</td>
<td>£2200</td>
</tr>
<tr>
<td></td>
<td>Switch-relay/RF</td>
<td>1260-54</td>
<td>C1</td>
<td>1 GHz, 6 x 1x4 terminated trees</td>
<td>£2595</td>
</tr>
<tr>
<td>Tasco Electronics</td>
<td>ARINC-429 tester</td>
<td>TVX1429</td>
<td>C1</td>
<td>16 channels (8 transmit/8 receive)</td>
<td>£14950</td>
</tr>
<tr>
<td>Tektronix</td>
<td>Multiplexer controller</td>
<td>VX4400</td>
<td>C1</td>
<td>Controls the company’s TSI range of remote-switch cards</td>
<td>£3250</td>
</tr>
</tbody>
</table>

EDN November 22, 1990
The ARIES Chip Set does away with many significant design headaches, that's why. It collapses virtually all disk drive electronic functions onto just 4 chips, so you can accomplish your hard disk drive design in less space. And get your finished product to the market a lot sooner.

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SEAGATE TEC

SEAGATE QUALITY

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The third major factor that sets Seagate drives apart is our commitment. You see it in the inspired dedication of our employees: like our engineers, who apply the latest technology advances to our current models. In our assemblers and technicians, who are committed to producing defect-free products. And in our sales, customer service and technical support groups, who continually go the extra mile to ensure complete customer satisfaction.

But most of all, Seagate drives are built upon experience: the market insight and technical knowhow that can only come from selling more than 25 million drives since the industry’s inception. It’s the kind of experience you won’t find at any other disc drive company.

To be sure you’re getting Seagate quality and technology inside where it counts, make sure there’s a Seagate nameplate on the outside. For more information, contact Seagate at 800-468-DISC, or 408-438-6550.
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City ____________________________ State _____ Zip _______ Phone ____________

THE PATHWAY TO PERFORMANCE.

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All the features of HPBASIC, and more.
For less.

<table>
<thead>
<tr>
<th>HTBasic</th>
<th>BASIC FEATURES:</th>
<th>HP BASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td>IEEE-488 GPIB (HP-IB), RS-232 Instrument Control</td>
<td>YES</td>
</tr>
<tr>
<td>YES</td>
<td>Integrated Environment: Mouse, Editor, Debugger, Calculator</td>
<td>YES</td>
</tr>
<tr>
<td>YES</td>
<td>Supports 16 Megabytes of Memory (breaks DOS 640K barrier)</td>
<td>YES</td>
</tr>
<tr>
<td>YES</td>
<td>Engineering Math: Matrix Math, Complex Numbers</td>
<td>YES</td>
</tr>
<tr>
<td>YES</td>
<td>High Level Graphics: Screen, Plotter, Printer</td>
<td>YES</td>
</tr>
<tr>
<td>YES</td>
<td>Structured Programming with Independent Subprograms</td>
<td>YES</td>
</tr>
<tr>
<td>YES</td>
<td>Runs on Industry Standard Personal Computers</td>
<td>NO*</td>
</tr>
<tr>
<td>YES</td>
<td>Industry Standard Graphic Printer Support: Epson, IBM, lasers, etc.</td>
<td>NO</td>
</tr>
<tr>
<td>YES</td>
<td>Industry Standard Network Support: Novell, IBM, Microsoft, NFS, etc.</td>
<td>NO</td>
</tr>
<tr>
<td>YES</td>
<td>Industry Standard IEEE-488 Support: National Instruments, IOtech, etc.</td>
<td>NO</td>
</tr>
<tr>
<td>YES</td>
<td>Exchange data files with Industry Standard PC applications</td>
<td>NO*</td>
</tr>
<tr>
<td>YES</td>
<td>No-charge Telephone Technical Support</td>
<td>NO</td>
</tr>
<tr>
<td>YES</td>
<td>Instant on-line HELP system</td>
<td>NO</td>
</tr>
</tbody>
</table>

A Costly Situation. Every engineer needs the power and features of a “Rocky Mountain” BASIC workstation, but not everyone can have one. They simply cost too much. Fewer workstations, less productivity. The Best Way. TransEra HTBasic software provides the only way for serious technical computer users to turn their PC into a workstation without having to add costly hardware. Powerful workstations for everyone means greater productivity. Extraordinary Versatility. In addition, TransEra HTBasic works with the Industry Standard Personal Computer hardware, software, and networks. It even allows you to easily exchange data between your favorite DOS programs and the files you create in the BASIC workstation environment. All at a fraction of the cost of other solutions.

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CIRCLE NO. 1
The X-Window system revitalized interest in Unix by providing a software platform for friendly looking graphical user interfaces and multitasking applications. However, the hardware you select will determine how efficiently you can work.

The X-Window terminals look like workstations because they have GUls and they let you access workstation software. (See Table 1 for a comparative list of X-Window terminals.) But they don't have a CPU and must rely on the network host for computation and I/O. This means that the host CPU must deal with every keystroke and mouse click for every terminal on the network. As a result, each terminal added to the network can significantly decrease your system's performance. Using an X-Window terminal to access your Unix network is a good approach if you don't need to perform CPU-intensive tasks for extended periods.

Another reason to use X-Window terminals is that they cost several thousand dollars less than workstations. So, theoretically, you can run workstation software without the expense of purchasing a workstation. The catch is that most software vendors expect you to pay a licensing fee for each terminal on your network. And, although you may initially save a few thousand dollars, you may wind up paying more in licensing fees, even if you have no intention of running particular applications across the entire network.

Available with either a dual or a single monitor, the Series 2000 workstations from Intergraph run a variety of engineering applications.
Now...precision TTL-controlled attenuators accurate over 10 to 1000MHz and -55 to +100°C. Four models are available in the new TOAT-series, each with 3 discrete attenuators switchable to provide 7 discrete and accurate attenuation levels (see chart). Cascade all four models for up to 64.5dB control in 0.5dB steps. Custom values available on request. The 50-ohm TOAT-series performs with 6µsec switching speed and can handle power levels up to 0dBm. Units are housed in a rugged hermetically-sealed TO-8 package to withstand the shock, vibration, and temperature stresses of MIL-STD-883. Connector versions are available. Take advantage of the $59.95 (1-9 qty) price breakthrough to stimulate new applications as you implement present designs and plan future systems.
TECHNOLOGY UPDATE

X-Window

However, X-Window terminals can be indispensable if the application happens to be located on multiple machines from multiple vendors, as may happen with a project involving several departments or an engineering work group effort. Or, if your company has engineers who infrequently need to use a computer to do their jobs, it may be more economical to provide them with terminals rather than workstations. It's only when one application is running on one CPU for extended periods of time that workstations offer a clear advantage over terminals.

A workstation provides more power per individual than a terminal, and CAE tends to be MIPS hungry. So by turning to an X-Window-compatible workstation, you can contribute to the common good by localizing your number crunching and staying off the network until you're ready to share your results. (See Table 2 for a comparative list of X-Window workstations.) In addition, running an application solely on your workstation shields you from performance problems that may occur on the network.

You must be careful to compare similarly configured options when looking at price. Many workstation manufacturers promote units that sell for less than $5000, but these machines frequently have monochrome CRTs and minimal memory. Decide beforehand whether you'll need a SCSI port for external data storage or serial ports for peripherals such as scanners, plotters, or printers. An Ethernet port should be standard equipment for any X-Window-compatible terminal or workstation.

You can purchase an X-Window terminal from Graphon starting at $995 that will let you run X11 applications and tap into the CPU power of the network's Unix host. However, such terminals may have an unacceptably long response time if the host becomes inundated with server requests. And windowing terminals further load down the host with CPU-intensive, high-priority, interactive operations.

In addition, CAE drawings tend to be complex figures that you will probably want to display in color. So, expect to ante up at least a thousand dollars or more for a color CRT and increased memory. You can purchase terminals that are equipped to handle these complex drawings, such as Tekxpress from

---

Table 1—X-Window terminals

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model</th>
<th>Base price</th>
<th>Display</th>
<th>System memory</th>
<th>I/O ports</th>
<th>Special features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Graphon Corp</td>
<td>Graphon 21</td>
<td>$1995</td>
<td>21-in. 1280x1024-pixels, Mono</td>
<td>Uses host's memory</td>
<td>Ethernet, serial</td>
<td>Virtual memory; screen displays 2 full-size pages</td>
</tr>
<tr>
<td>IBM Corp</td>
<td>Xstation 120</td>
<td>$2525</td>
<td>12-in. 640x480-pixels, Mono</td>
<td>512k bytes (expandable to 8.5M)</td>
<td>Ethernet, serial, parallel</td>
<td>Can run simultaneously in a Token-Ring and an Ethernet LAN</td>
</tr>
<tr>
<td>Motorola Inc</td>
<td>Network Display Station</td>
<td>$2495</td>
<td>16-in. 1024x1024-pixels, Mono</td>
<td>2.5M bytes</td>
<td>Ethernet, serial</td>
<td>White phosphor CRT displays 105 dpi; 68000 µP</td>
</tr>
<tr>
<td>NCR Corp</td>
<td>XL X-Station</td>
<td>$3500</td>
<td>15-in. 1024x800-pixels, Mono</td>
<td>4M bytes</td>
<td>Ethernet, serial</td>
<td>Menu-driven set-up and configuration</td>
</tr>
<tr>
<td>Network Computing Devices</td>
<td>NCD19b</td>
<td>$2295</td>
<td>19-in. 1024x800-pixels, Mono</td>
<td>2MB bytes (expandable to 5M)</td>
<td>Ethernet, serial</td>
<td>Runs as much as 3 times faster than DEC VT-1000 X-Window terminal</td>
</tr>
<tr>
<td>Tektronix Inc</td>
<td>Tekxpress</td>
<td>$3995</td>
<td>14-in. 1152x900-pixels, Color</td>
<td>3MB bytes (expandable to 13M)</td>
<td>Ethernet, serial</td>
<td>Options include A-size tablet; has 3-year warranty</td>
</tr>
</tbody>
</table>

EDN November 22, 1990
X-Window

Tektronixs. However, they are more expensive; Tekxpress terminals start at $3495. In contrast, Series 2000 workstation from Intergraph provides 2-D and 3-D graphics from $15,900.

Soup up your PC for X

If you already have an 80386- or 80486-based PC, you may want to consider integrating it into your company's X-Window network. Several software vendors offer graphical operating systems that permit your PC to access the X-Window System while preserving DOS functions.

Santa Cruz Operation sells Open Desktop, a $995 package that provides an Open Software Foundation Motif GUI. The company's Unix System integrates V/386 with MS-DOS. Age Inc recommends plugging a TMS340-based graphics controller into your PC and using its $595 program, Xftware for Unix, to create an X11 workstation. Quarterdeck expects to release Desqview/X—a similar product with a DOS extender—before the end of 1990, which should cost about $250.

With the proliferation of 80386- and 80486-CPU PCs, it's becoming impossible to make practical distinctions between the processing power of workstations and PCs. For example, for $7399 you can buy Dell Computer Corp's 425E, a 25-MHz bus-based PC with a 330M-byte hard-disk drive. Or for $3999 you can buy a 25-MHz, ISA-bus, ME-486-ISA from Micro Express. The Intel CPU on both machines provides a benchmark of about 20 MIPS.

However, you probably won't want to settle for a standard PC display because your CRT's resolution is critical in an X-Window environment. A monitor with less than a megapixel display will prove inadequate to the rigors of windowing. Off-the-shelf PCs offer no more than 640 × 480- or 1024 × 768-pixel VGA resolutions.

Because of the resource-consuming graphic and system manipulations necessary to run X-Window, an unmodified PC will spend more time dealing with the X-Window environment than running programs. To alleviate these display problems, you can use a graphics accelerator board to reduce the system demands on your PC's CPU. Nth Graphics' accelerator board, XNth contains X-Window server software. As a result, you can switch between DOS and X-Window with a single keystroke. The

**Table 2—X-Window Workstations**

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model</th>
<th>Base price</th>
<th>CPU</th>
<th>Benchmarks</th>
<th>Display</th>
<th>System memory</th>
<th>I/O ports</th>
<th>Special features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Equipment Corp</td>
<td>Decstation 5000 M200 CX</td>
<td>$14,995</td>
<td>25-MHz MIPS</td>
<td>24 MIPS</td>
<td>19-in. 1024x864-pixels, mono</td>
<td>8M bytes (expands to 120M)</td>
<td>Ethernet</td>
<td>Turbochannel expansion bus; X-Window graphics subsystem</td>
</tr>
<tr>
<td>Hewlett-Packard</td>
<td>HP Apollo 9000 VRX</td>
<td>$15,000</td>
<td>33-MHz IBM60</td>
<td>66M floating-point operations/sec</td>
<td>19-in. 1280x1024-pixels, mono</td>
<td>9M bytes (expands to 64M)</td>
<td>Ethernet, SCSI, serial, parallel</td>
<td>Upgrade to 16 image planes and 270,000 3D vectors/sec</td>
</tr>
<tr>
<td>IBM Corp</td>
<td>RISC System/6000 Powerstation 320</td>
<td>$12,995</td>
<td>20-MHz power architecture</td>
<td>7.5 MIPS; 7.4 floating-point operations/sec</td>
<td>19-in. 1280x1024-pixels, mono</td>
<td>9M bytes (expands to 128M)</td>
<td>Ethernet, SCSI</td>
<td>Includes 355M-byte and 1.44M-byte drives; 8 MCA expansion slots</td>
</tr>
<tr>
<td>Intel Corp</td>
<td>Microsystem 3000</td>
<td>$11,995</td>
<td>25-MHz</td>
<td>5 MIPS</td>
<td>19-in. 1680x1200-pixels, mono</td>
<td>8M bytes (expands to 40M)</td>
<td>Ethernet, SCSI, serial, parallel</td>
<td>Includes 170M-byte drive, 80387 math coprocessor, 64x-cache</td>
</tr>
<tr>
<td>Intergraph Corp</td>
<td>Series 2000</td>
<td>$15,900</td>
<td>25-MHz</td>
<td>5 MIPS</td>
<td>19-in. 1194x884-pixels, color</td>
<td>16M bytes (expands to 64M)</td>
<td>XNS &amp; TCP/IP, SCSI, serial, parallel</td>
<td>Includes 200M-byte hard disk drive and 1.44M-byte floppy-disk drive</td>
</tr>
<tr>
<td>Mars Microsystems</td>
<td>Mariner 4i</td>
<td>$5995</td>
<td>25-MHz Sparc</td>
<td>16.8 MIPS</td>
<td>16-in. 1024x768-pixels, mono</td>
<td>9M bytes (expands to 96M)</td>
<td>Ethernet, 2 serial</td>
<td>Uses ISA bus; optional 80386 module lets you run DOS applications</td>
</tr>
<tr>
<td>Solbourne Computer Inc</td>
<td>S4000</td>
<td>$8995</td>
<td>40-MHz Sparc</td>
<td>25.5 MIPS</td>
<td>19-in. 1152x900-pixels, mono</td>
<td>8M bytes (expands to 64M)</td>
<td>Ethernet, 2 serial, 1 audio</td>
<td>Optional graphics accelerator adds hardware support for PEX</td>
</tr>
<tr>
<td>Sun Microsystems</td>
<td>Sparstation SLC</td>
<td>$4995</td>
<td>26.5-MHz Sparc</td>
<td>12.5 MIPS</td>
<td>17-in. 1152x900-pixels, monop</td>
<td>9M bytes (expands to 16M)</td>
<td>Ethernet, SCSI, serial</td>
<td>No base unit; CPU components housed in display</td>
</tr>
<tr>
<td>Tektronix Inc</td>
<td>XD88/35</td>
<td>$31,995</td>
<td>25-MHz 88100</td>
<td>21 MIPS, 2.5M floating-point operations/sec</td>
<td>16-in. 1280x1024-pixels, color</td>
<td>9M bytes (expands to 168M)</td>
<td>Ethernet, SCSI, 4 serial, parallel</td>
<td>Includes image processing and accelerated 3D graphics</td>
</tr>
</tbody>
</table>
AT&T provides all your end-to-end transmission solutions with our full line of fiber optic, copper cable and connecting components.

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X-Window board contains a 10-MIPS CPU and three custom graphics µPs. Modules are available for both IBM PC/AT and EISA buses. Xth is $1995 with 1024 x 768-pixel resolution or $2995 for 1280 x 1024 pixels.

Of course, you should carefully weigh the relative costs of your alternatives. Unless you currently own a PC that you can upgrade to an X-Window-compatible workstation, it would probably be more cost effective to purchase a fully configured workstation than to build your own on a PC chassis from commercially available components. This fact is especially true since so many vendors offer X-Window-compatible workstations with greater processing power than PCs provide.

Even chip-maker Intel has entered the workstation arena by offering X-Window-compatible workstations for OEMs based on the company's 80386 and 80486 µPs. Rival IC manufacturer Motorola is also producing a series of RISC-based X-Window hosts under the name Multipersonal Computer. Prices range from $23,985 for a configuration that accommodates three to six active terminals.

Whether you decide to go with

**GUI wars make a mess of X-Window**

Although the X-Window system provides a stable platform for applications using a graphical user interface (GUI), a battle is raging between proponents of two interfaces: Open Software Foundation's (OSF) Motif and Unix International's Open Look.

The X-Window system is different from other windowing environments because it does not include a window manager. Accordingly, the window manager provided by the GUI you select will determine the appearance and behavior (or look-and-feel) of the applications you run and the way in which you interact with the operating system.

X/Open, an international consortium formed in 1984 to specify open-system requirements based on de facto industry standards, has declined to pledge its allegiance to either GUI—at least for the moment. Part of the organization's problem is that both Unix International and OSF are active members.

IBM, Digital Equipment Corp (DEC), Hewlett-Packard (HP) and several other vendors formed OSF in May 1988 as a neutral supplier of hardware-independent, open-system software technologies. OSF selected Aix (IBM's version of Unix) as the basis for an operating system called OSF/1, which uses a modular Unix kernel. OSF then defined the Motif interface, which behaves similarly to IBM's OS/2 Presentation Manager, but includes a 3-D look developed by HP and a tool kit of dialog boxes, scroll bars, and buttons (provided by DEC and HP).

Even more notable, Motif-based software can run on non-Unix systems that have a compatible tool kit. Texas Instruments expects to announce an X-compatible workstation this year that uses the Motif GUI.

In contrast, Unix International has elected to standardize a version of Unix that combines Berkeley Unix and AT&T's System V Unix, a move spearheaded by Sun and AT&T. Unix International operates as a membership-run industry trade association to plan and develop future versions of Unix.

Sun developed the Open Look GUI, which Unix International endorsed in April 1988. When you purchase AT&T's Unix System version 4, you get Open Look for no additional charge. Open Look runs on more than 20 hardware platforms from vendors such as Sun, DEC, HP, and IBM.

Although both Open Look and Motif comply with X/Open guidelines and have comparable features, the two interfaces remain incompatible. Both GUIs include window managers, graphical tool kits, and file managers. Because the internal functions of these GUIs are quite similar, technical differences arise mainly in the look-and-feel of the two interfaces.

As a result, there are only a few off-the-shelf software applications for both interfaces. For example, in July, Graytech Software proclaimed that its $2950 CAD X11 software was the first available workstation-independent CAD program running under X-Window. Just as in the early days of PCs, the most prudent way to select a GUI is to find an application program you like and then adopt the interface recommended by the vendor. However, X-Window philosophy dictates that client applications should not depend upon the presence of any particular window manager. So as the number of available applications grow, expect your choice of GUIs to be more a matter of personal preference than technical necessity.
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EDN November 22, 1990  CIRCLE NO. 186 67
X-Window

terminals or workstations, the X-Window system is going to make Unix more usable. You will be able to access the power of Unix, without needing to learn all of the difficult commands that make many people run away in frustration. So with that issue resolved, you need only decide whether you want the optional autonomy of doing your own work without being affected by the network, or whether you can handle being a slave to the host computer.

Acknowledgment

Special thanks to Glenn Seiler and Michael Joplin of Texas Instruments and Dr Georges Grinstein, director of the Graphics Research Lab and Institute for Visualization & Perception Research at the University of Lowell (Lowell, MA).

References


For more information

For more information on the X-Window hardware and software discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN’s Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

<table>
<thead>
<tr>
<th>Company</th>
<th>Address</th>
<th>Telephone</th>
<th>Fax</th>
<th>Circle No.</th>
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<tr>
<td>Age Inc</td>
<td>Suite 226</td>
<td>(619) 565-7373</td>
<td>(619) 565-7490</td>
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<tr>
<td>Dell Computer Corp</td>
<td>9505 Arboretum Blvd, Austin, TX 78759</td>
<td>(512) 338-4400</td>
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<td>No. 651</td>
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<tr>
<td>Digital Equipment Corp</td>
<td>146 Main St, Maynard, MA 01754</td>
<td>(508) 492-5111</td>
<td></td>
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<tr>
<td>Graphon Corp</td>
<td>1980 Concord Dr, Dept 190, San Jose, CA 95131</td>
<td>(415) 772-7495</td>
<td>(415) 455-8400</td>
<td>No. 653</td>
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<tr>
<td>Graytech Software Inc</td>
<td>2172 Menomini Ave, Wheaton, IL 60187</td>
<td>(708) 682-4000</td>
<td>(708) 682-9047</td>
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<tr>
<td>Hewlett-Packard Co</td>
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<td>(800) 752-0900</td>
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<tr>
<td>IBM Corp</td>
<td>1133 Westchester Ave, White Plains, NY 10004</td>
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<tr>
<td>Intel Corp</td>
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<td>Box 1080, Mars, PA 19046</td>
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<td>Micro Express</td>
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<tr>
<td>Motorola Inc</td>
<td>Computer Systems Div, Cupertino, CA 95014</td>
<td>(800) 535-1224</td>
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<tr>
<td>NCR Corp</td>
<td>3325 Platt Springs Rd, West Columbia, SC 29169</td>
<td>(800) 525-9227</td>
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<td>Network Computing Devices Inc</td>
<td>350 N Bernardo Ave, Mountain View, CA 94043</td>
<td>(415) 694-6050</td>
<td>(415) 961-7711</td>
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<td>Nth Graphics Ltd</td>
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<td>(512) 624-7552</td>
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<td>150 Pico Blvd, Santa Monica, CA 90405</td>
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<tr>
<td>Texas Instruments</td>
<td>Box 1900, Santa Cruz, CA 95061</td>
<td>(408) 425-7222</td>
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<tr>
<td>Tektronix Inc</td>
<td>Box 14689, Portland, OR 97215</td>
<td>(800) 225-5434</td>
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<td>Sun Microsystems Inc</td>
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<td>(415) 961-1234</td>
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<td>Texas Instruments</td>
<td>Box 655012, M 57, Dallas, TX 75265</td>
<td>(214) 396-5236</td>
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Second, consider our new ultra-high speed SRAM capabilities. As you scan the chart above, keep in mind even higher speeds will be available soon.

<table>
<thead>
<tr>
<th>MODEL</th>
<th>CONFIG.</th>
<th>SPEED (ns)</th>
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</thead>
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* For Intel 80386. ** O/E

EDN November 22, 1990
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low pass dc to 1200MHz

<table>
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<th>MODEL NO.</th>
<th>PASSBAND, MHz (loss &lt;1dB)</th>
<th>fcc, MHz (loss 3dB)</th>
<th>STOP BAND, MHz (loss&gt;20dB)</th>
<th>VSWR</th>
<th>PRICE</th>
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high pass dc to 2500MHz

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<td>DC-800 800</td>
<td>710</td>
<td>720</td>
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bandpass 20 to 70MHz

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<tr>
<th>MODEL NO.</th>
<th>CENTER FREQUENCY, MHz</th>
<th>PASSBAND, MHz (loss &lt;1dB)</th>
<th>fcc, MHz (loss 3dB)</th>
<th>STOP BAND, MHz (loss&gt;20dB)</th>
<th>VSWR</th>
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narrowband IF

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<th>VSWR</th>
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<td>51, 94</td>
<td>6, 193-1000</td>
<td>1.7</td>
<td>18.95</td>
</tr>
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</table>

CIRCLE NO. 102
The Analog Behavioral Modeling option for the PSpice Circuit Analysis package allows you to describe analog components, or entire circuit blocks, using a formula or look-up table. Linear blocks may be described using either a Laplace transform or a frequency response table. Once defined, you can use these blocks in all PSpice analyses, including DC, AC, and transient.

Modeling entire blocks of circuitry is a powerful aid in designing a system from the top down. You can describe a functional block by its behavior without worrying about how that function will be implemented. Later on in the design process, you can replace the block with the actual circuitry.

Another application is the modeling of electronic components which are not built into PSpice. The photo shows an example of simulating the DC characteristics of a 3/2-power-law device.

Since its introduction over six years ago, MicroSim's PSpice has sold more copies than all other SPICE-based programs combined. PSpice provides broad capabilities, accurate results, diverse options, and availability across a wide range of computer platforms. PSpice includes an extensive device library of 3,000+ analog parts and 1,300+ digital parts, at no extra charge.

Besides Analog Behavioral Modeling, PSpice provides the following options:

**Digital Simulation**: simulation of mixed analog/digital circuits with feedback between the analog and digital sections.

**Monte Carlo Analysis**: calculates the variations in a circuit's performance allowing for component tolerances. This option performs statistical analyses: Monte Carlo, Sensitivity, and Worst Case.

**Probe**: acts as a "software oscilloscope" to provide an interactive viewing and processing environment for simulation results (see photo).

**Parts**: is a parameter extraction program allowing the extraction of device model parameters from data sheet information.

PSpice is available on the PC (running DOS, Protected Mode DOS, or OS/2), Macintosh II , Sun 3, Sun 4, and SPARCstation, DECstation 2100, 3100, and 5000, and the VAX/VMS families.

In addition to the Circuit Analysis package, the PSpice family of products also contains the Circuit Synthesis package, which consists of our two filter synthesis products: Advanced Filter Designer and Standard Filter Designer. Filter Designer is an interactive design aid for synthesizing and analyzing active filters. Features include:

- Analysis of low pass, high pass, band pass, and band reject filter types.
- Synthesis of all available filter types using Butterworth, Chebyshev, Inverse Chebyshev, and Elliptic (Cauer) functions.
- Capability to synthesize arbitrary transfer functions and delay equalization filters (only available in Advanced Filter Designer).

Each copy of our Circuit Analysis and Circuit Synthesis programs comes with MicroSim's extensive product support. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022 or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

20 Fairbanks • Irvine, CA 92718 USA • FAX (714) 455-0554
The price of the CodeStalker 386 in-circuit emulator (ICE) should raise eyebrows. At $9995, this ICE costs only a third as much as some in-circuit emulators for Intel's 80386 µP. This price includes support of real-time trace and 33-MHz operation of the target system. Although in a few areas the ICE's features have been scaled back to hold its price down, the instrument's capabilities meet the needs of the majority of designers who build systems around Intel's popular 32-bit processor. Unlike some low-cost debugging tools, the product is not an adjunct to an ICE—it is an ICE.

In one very important area, the ICE gives ground to no product: It downloads code from a host PC at a transfer rate of 250k bytes/sec. This speed results from a host-to-emulator fiber-optic link. Using the link, a host PC can fill the ICE's 448k-byte emulation memory in less than 2 sec. Moreover, the link's ohmic isolation eliminates the possibility of either the target or the emulator injecting noise into the other unit.

Using the optical link requires that you plug an interface card into the host PC's I/O bus. If you don't choose to do so, you can connect the ICE to a PC or an ASCII terminal via a 19.2k-bps RS-232C link. This link runs at the same speed as the host links of many other ICES—less than 1% of the speed of the optical link. You don't use a terminal link for downloading, so, with a terminal, RS-232C's lower speed is not a handicap. Compared with traditional methods, the optical link speeds downloads by a factor of more than 100.

The unit's real-time trace capability is good, but not astounding. The trace buffer holds 4k 32-bit frames. For each of the four hardware breakpoints, you can specify a breakpoint address and cycle type. Although the hardware doesn't support complex breakpoints, the ICE does support an unlimited number of software breakpoints. Furthermore, the emulator offers a "background" mode of program operation. In this mode, the target system's DMA and interrupt routines remain active even when the ICE has halted operation of the main program.

The ICE is housed in a small enclosure with the pod projecting from it on short ribbon cables. The 80386 emulation processor is mounted in a special socket on the pod. The socket has pins that project out the back of the pod board and plug into the target system's µP socket. If your target presents data to the µP's data lines at times other than when a valid address strobe exists, you can interpose a buffer board between the pod and the target. Then, instead of just plugging in the pod, you plug a 2-board sandwich into the target. The buffer board adds 6 nsec of delay. It is included in the price of the ICE, and the vendor ships one with each unit.

Also included is the vendor's source-level debugger, which is enhanced to work with the fiber-optic link. The debugger permits downloads at the link's full speed. It works with C compilers from Borland, Microsoft, Manx, Intel, and others. Production shipments of the ICE are scheduled to begin December 15, 1990.

—Dan Strassberg

Softaid Inc, 8930 Rte 108, Columbia, MD 21045. Phone (800) 433-8812; in MD, (301) 964-8455. FAX (301) 596-1852.

Circle No. 732
PRODUCT UPDATE

DSP boards for Macintosh II and SE CPUs target graphics and modeling applications

The MacDSP family of three boards for the Apple Macintosh IIx, IICx, IICi, IIFx, and SE/30 computers targets computationally intensive applications such as DSP, array processing, and graphics. The boards interface to the systems through Nubus or the Macintosh PDS (Processor Direct Slot). They include a 5M-byte/sec DMA bus interface that enables programs and data to be transferred between the Macintosh and MacDSP local memory without interrupting MacDSP program execution.

The MacDSP boards include AT&T's 32-bit DSP32C, which features a peak performance of 32M flops. The boards include up to 4M bytes of zero-wait-state static RAM, and are available with up to eight A/D channels. In standard benchmarks, the products execute algorithms for a 1k real FFT in 1.66 msec, a 128-tap FIR filter in 8.56 μsec, a 5 x 5 matrix multiply in 8.32 μsec, and a 256 x 256 convolution (9 x 9 kernel) in 0.71 msec.

The first member of the family, known as MacDSPAP, targets memory-intensive array processing applications such as image processing, 3-D modeling, graphic animation, and Postscript acceleration. The board offers peak performance of 32M flops and includes 64k to 1M bytes of zero-wait-state SRAM. You can also specify this board with Nubus or PDS interfaces, and it includes two 16M-bit/sec serial DMA ports.

The third member of the family, the MacDSPXKC, targets multi-channel signal- and image-processing applications such as speech recognition, robotics, and medical instrumentation. The board only fits in Macintosh II family computers and employs a modular architecture based on daughter cards. The board includes 64k bytes to 4M bytes of zero-wait-state SRAM and 1, 2, or 8 A/D channels with sample rates as high as 1 MHz. The product has a Nubus interface and two 16M-bit/sec serial DMA ports.

A C-language development system for the boards includes a compiler, assembler, simulator, and linker. The tools run under Apple's Macintosh Programmer's Workshop. You can also buy the company's Version 2.0 signal-analysis package for the board family. Based on the Macintosh interface, the software enables users to acquire data, operate on that data using a variety of signal-processing functions, and display the results in real time.

Release 2.0 enhancements include overlapped FFTs that boost time-bandwidth resolution, and continuous data processing that enhances signal detection and eliminates missing data samples. Release 2.0 can also send data that has been processed on board to a D/A converter for audio output; provides enhanced cursor measurement; and scrolls through captured data frame by frame or sample by sample.

With 1M bytes of memory, a 32M-flop version of the MacDSPAP costs $4995. A 24M-flop version of the MacDSPXI with 64k bytes of memory costs $2895. And the 256k-byte 32M-flop version of the MacDSPXKC costs $2895. All three boards are available immediately from stock. Upgrades to version 2.0 of the MacDSP software are free; for new users, the software costs $495. The C-language development environment costs $1500.

—Maury Wright

Spectral Innovations Inc, 4633 Old Ironsides Dr, Suite 450, Santa Clara, CA 95054. Phone (408) 727-1314. FAX (408) 727-1423. Circle No. 737

WHAT’S COMING IN EDN

EDN Magazine’s December 6, 1990, issue will begin the second part of our semiannual Product Showcase. The issue’s staff-written features will cover ICs in laptops, video games, phones, and avionics; distributed power systems; active cooling devices; and DSP software and applications. The issue will also include reviews of ICs and semiconductors, power sources, hardware, and software.

EDN’s December 20, 1990, issue will conclude the Showcase with coverage of CAE, components, test and measurement products, and computers and peripherals.

EDN November 22, 1990

Zilog's integrated universal serial communication controller (Z16C31™) combines two 32-bit full duplex DMA channels with a powerful single-channel USC cell. And that means efficient bus access, sophisticated buffer management, higher throughput, a greatly reduced CPU workload, and considerably lower cost for complex data communications applications.

Fast, multi-protocol operation.
Zilog's USC cell gives you 10 Mbits/sec speed for multi-protocol operation. It also gives you 32-byte RX and TX FIFOs for improved latency and up to 32-byte block moves. There's a Time Slot Assigner for multiplexing in ISDN/T1 applications, a flexible 16-bit bus interface — multiplexed or non-multiplexed — for easy CPU interconnect, and a daisy-chain interrupt structure for simpler interrupt handling. And, best of all, the USC can reduce the CPU workload as much as 60%.

Integrated buffer management.
The USC's two 32-bit DMA channels provide for 32-bit addresses and 16-bit data word transfers... and they allow full duplex operation at 10 Mbits/sec. The two simple DMA modes, normal and buffered, mean your design can be tailored to common buffer management schemes. The two chained DMA modes, array chained and link array chained, reduce CPU overhead in advanced buffer management schemes. The daisy-chain DMA priority structure makes it easy to design multiple USC systems.

Versatility and reliability.
The USC's flexible, multi-protocol design lets you adapt your system to a variety of networks as interconnect standards evolve. The USC supports ten protocols and eight data encoding formats, including asynchronous, bit and byte synchronous, HDLC, isochronous, Ethernet and MIL-STD 1553B. And it all comes to you off the shelf, backed by Zilog's proven quality and reliability. To find out more about the USC or any of Zilog's growing family of Superintegration™ products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away.

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EDN November 22, 1990 CIRCLE NO. 143 81
PRODUCT UPDATE

Wide-bandwidth linear optocoupler operates over a dc to 100-kHz range

The IL300 linear optocoupler suits power supply, medical sensor, audio signal interfacing, process control transducer, and telecommunication applications. The device employs internal compensation circuitry to achieve 0.01% servo linearity over an operating bandwidth of dc to 100 kHz. Gain-stability figures vs temperature and time equal 0.005%/°C and 0.05%/hour, respectively. In addition, the coupler features a peak withstand test voltage of 7500V ac for 1 sec and a common-mode rejection ratio of 100 dB.

The IL300 consists of an AlGaAs infrared LED and feedback and output photodiodes configured in a bifurcated arrangement. The feedback photodiode captures a percentage of the LED’s radiated flux and generates a control signal that is part of a servo loop; the loop controls the LED’s drive current. This technique compensates for the LED’s nonlinear time and temperature characteristics. The output PIN (positive-intrinsic-negative) photodiode produces a signal that is linearly related to the error-loop optical flux created by the LED. The feedback and output PIN photodiodes are matched to accurately track the output flux of the LED to ensure the time and temperature stability of the input-output gain.

Total package dissipation for the optocoupler is 250 mW, and the operating range spans −55 to +100°C. The unit is housed in an 8-pin plastic DIP, which features a standard lead configuration. The coupler is also available in surface-mount designs; version IL300G features a lead-bend configuration conforming to VDE 0805/0806 specifications. $2.10 (1000).

—Tom Ormond
Siemens Components Inc, Optoelectronics Div., 19000 Homestead Rd., Cupertino, CA 95014. Phone (408) 257-7910. FAX (408) 725-3339.

Circle No. 733

ZIP MATES

Magna/PAC® power distribution capacitors are specifically designed to provide more capacitance per ZIP and to achieve higher board density. At the same time consolidating the voltage equalization and decoupling function.

Magna/PAC replaces conventional, individual 2 pin-decoupling capacitors, and is available in lengths up to 10 inches with pinouts to accommodate any ZIP arrangement. With a maximum capacitance of 3.0 µF per linear inch, Magna/PAC can be used as a capacitor array to decouple noisy and power hungry ICs and to minimize sag. It’s coated with a dielectric grade epoxy insulation system, meeting UL 94-VO for flammability, and withstands the temperature extremes and solvents used in wave soldering and board cleaning.

Magna/PAC from Rogers. The perfect ZIP mates.

Board Courtesy of Symbolics, Inc.

Also available through Mektron Europe, Ghent Belgium and Rogers Inoue Corp., Nagoya, Japan.
Magna/PAC is a registered trademark of Rogers Corporation.
Epoxy insulation meets UL94VO Rating.

Technology for tomorrow built on TQC today.

ROGERS
Rogers Corporation
Circuit Components Division
2400 South Roosevelt Street
Tempe, AZ 85262
Tel: (602) 967-9524
Fax: (602) 967-9385

CIRCLE NO. 40

EDN November 22, 1990
You don't need a forklift, a strong back, and a keen sense of balance to put an entire microwave lab on your desk. All you need is CAE design software from EEsof.

Our tools realistically simulate just about every piece of equipment in the lab—right there in your very own office. From devices to circuits to subsystems. You'll be able to create better products with more functions and higher yields. Explore new concepts. Work on projects that wouldn't even be possible if you relied solely on the lab.

And you'll do it fast. From idea to finished prototype in days or weeks instead of months or years.

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Field-proven in a broad spectrum of applications and certified by the world's safety agencies, here are versatile, rugged power tools for your design needs. Choose voltages up to 48V dc; power up to 1500W; ac or dc input. Features include active soft-start, remote voltage control, overvoltage protection, current limiting and built-in EMI filtering. The 600W and 1500W models provide for current-share paralleling. Kepco's switchers are also available in low-cost open frame and pc-card styles for OEM applications. Please request our catalog.

Power tools

For your free copy of Kepco's new 56-page catalog, "Kepco Switching Power Supplies for the '90s" (#146-1692), call/fax/write Dept. LWT-12, Kepco, Inc., 131-38 Sanford Avenue, Flushing, NY 11352 USA
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The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face.

Interphase delivers those solutions.

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Interphase has long led the industry in high-performance VMEbus peripheral controllers, and that same leadership is now evident in networking node controllers. Interphase has FDDI, Token-Ring and Ethernet solutions for virtually any VMEbus system application challenge.

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Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

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The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

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CIRCLE NO. 147
Is it limiting your system performance?

Trying to analyze the adverse effect of jitter and isolate the failure using Random Sampling has been a problem. International Test Instruments (ITI) offers you the solution — Continuous Time Ordered Measurements using the Digital Timing Analyzer (DTA).

The DTA measures and stores up to 524,000 continuous intervals at data rates up to 20 MHz*. It can store these individual measurement values in the order they occurred at resolutions as fine as 50 ps. Interval deviations exceeding the accepted boundaries can be isolated and the events surrounding the interval can be easily analyzed.

Find out how the DTA and its application software** can help you pinpoint the problem area, determine the proper compensation and reduce the jitter that limits your system performance. For a no-obligation demonstration or to receive more information, call:

EDN November 22, 1990
In fact, the 80C186EB provides the lowest power consumption of any 16-bit integrated microprocessor. Intel achieved this feat in three ways. First, the 80C186EB is designed to run on as little as 3 volts. Next, its power management capabilities allow the processor and peripherals to be placed in various degrees of power-down. And finally, its fully static design can vary operating frequency from 0 to 16 MHz to efficiently meet specific power consumption and speed requirements.

Simply put, the 80C186EB uses only the current needed—and not a microamp more.

All this translates into longer operating time under battery power for portable...
applications. So some applications that could never be portable before, can be portable now.

And the 80C186 Family doesn't stop with the 80C186EB. Its new modular design allows for quick product proliferations to suit your application-specific needs.

So call Intel at (800) 548-4725. Ask for Literature Packet #LA59, and we'll send you the 80C186 "Solutions for Success" materials with information on the entire 80C186 Family and development tools. Do it today. Your applications will consume less power tomorrow.
Benchmarks don’t have to be confusing and deceptive. Application code that bears a resemblance to your software, consistently applied across a range of similarly configured microprocessor-based systems, can be useful in selecting your hardware.

Michael C Markowitz, Associate Editor

Most microprocessor vendors use benchmarks as a drunken man uses lampposts—for support rather than illumination.

—Adapted from Andrew Lang, Scottish author

Benchmarks can help you pick from among a multitude of microprocessors and microcontrollers. Unfortunately, to simplify choosing a µP, benchmarks have become a single-number figure of merit for both vendors and designers. This number is—at best—confusing and—at worst—deceiving.

The Systems Performance Evaluation Cooperative (SPEC), a consortium of computer and workstation vendors, was established to develop a suite of consistent and well-defined benchmarks. SPEC has recommended that you not use a single-number figure of merit because it can’t provide enough information. Despite SPEC’s urgings, users, vendors, and the press have endeavored to make SPEC’s 10-benchmark suite more palatable by simplifying the benchmarks into a single figure of merit. In recognition of our tendencies toward simplification, SPEC provided the Specmark (calculated as the geometric mean of the individual benchmark tests) to ensure that the “proper” single number be used—or misused.

Consider the vaunted IBM RS/6000 workstation, powered by IBM’s America superscalar microprocessor. (Because IBM isn’t making this microprocessor available at the chip level, we’ve excluded it from our directory.) This µP fetches four instructions at a time from its cache. Under certain circumstances, the processor can dispatch all four instructions in one cycle.

At the workstation roll-out, IBM proudly pointed to a workstation Specmark almost double that of other RISC-processor-powered workstations. Closer inspection of the individual SPEC benchmarks that constitute the Specmark reveals that the IBM workstation’s performance is most impressive in two of the floating-point

There are three kinds of lies: lies, damned lies, and benchmarks.
—Adapted from Benjamin Disraeli, British statesman

Although benchmarks can provide useful information, they don’t always tell the whole truth. (Photo courtesy Siemens Components Inc)
Remember that what you want from a benchmark and what the vendor wants from a benchmark are not the same.

performance tests. Integer performance, though, is comparable to other RISC workstation benchmarks (Fig 1). IBM uses a floating-point multiply/accumulate instruction to enhance the execution of many floating-point applications.

Supplementing a microprocessor's instruction set with a special-purpose instruction isn't necessarily bad. If the code you are trying to run uses that particular instruction, you'll get higher performance. On the other hand, if you blindly accept a vendor's performance claims, you may end up selecting a processor optimized for operations you'll never use.

**Benchmarks can confuse or illuminate**

Getting vendors to provide you with multiple benchmark results only eliminates part of the confusion. When Intel announced its 80960CA superscalar, it compared the µP against its own 80960KA, Motorola's 68030, and AMD's 29000 using a suite of nine integer benchmarks (Dhrystone 1.1, Buffer Copy, Annealing, PI, Quicksort, Bubblesort, Integer Matrix Multiply, CCIT Image Compression, and a Bezier Curve calculation).

Intel reported all results normalized to the 68030. The benchmarks showed the 960CA to be from 2 to 10.8 times faster than the 68030. The geometric mean of all nine benchmark programs indicated the 960CA was 3.9 times faster than the 68030. The 29000 results ranged from 0.4 to 1.7 times faster than the 68030, with a geometric mean of 1.0.

A knockout by the 960CA, right? Maybe, but AMD said the 29000 had both hands tied behind its back. AMD claimed the benchmark was rigged by Intel's choice of the STEB Standalone Evaluation Board. AMD said the board is a low-performance design that supports neither burst-memory accesses nor simultaneous access to instructions and data. Worse, AMD charged that, although Intel replaced the board's 120-nsec memory with the same 35-nsec chips they used in evaluating the 960KA, Intel did not reprogram the board's wait-state switches to take advantage of the 29000 board's faster memory.

In response to what they saw as improper benchmarking, AMD requested copies of the individual programs from Intel. AMD then recompiled the code using the current release of its HighC29K C compiler at full optimization. (Intel's report did not say which compiler version it used.) Then the company reran the code on the STEB board, as well as on three high-performance YARC Systems' 29000-based boards. One of the YARC boards ran at 33 MHz and had a data memory of 512k bits of 2-way interleaved 35-nsec static RAM. AMD's testing showed the 33-MHz, 29000-based YARC board was somewhat faster than the 960CA on most of the benchmarks—even though you can't buy a 33-MHz 29000.

**Benchmarks measure the whole system**

The lesson to learn from the 960CA vs 29000 contest is that benchmarks don't just evaluate the µP's performance, they also measure the effect of all of the peripheral components. Therefore, it is imperative that when you see benchmark data, you ask about the hardware configuration, clock rates, and memory speeds—and make sure programmable features, such as wait-state switches, are set properly. Fortunately, as feature sizes shrink, caches and data RAM are migrating onto the processor, making specsmanship of this sort less prevalent.

However, using simulations to benchmark performance will never disappear. Intergraph recently announced its Clipper C4 µP and "Fourth-Generation" compiler. As a superscalar design, the C4 contains both integer and floating-point execution units to allow the processor to issue two instructions per cycle. The design also includes pipeline stages within the floating-point unit so the µP can run faster—a technique called superpipelining.

When testing time came, the actual devices weren't available. So Intergraph decided to simulate small segments of the SPEC benchmarks that they believe are representative of integer, scalar floating-point, and vector floating-point applications. They used 23 in-
structions from the Espresso routine for the integer benchmark. The scalar floating-point benchmark was composed of 21 instructions from the Spice program. To measure vector floating-point performance, they used 34 instructions from the inner loop of the Linpack benchmark.

Running on the C4 software model at 50 MHz, these snippets of simulated code allow Intergraph to claim a peak performance of 94 MIPS and 33.3M floating-point operations per second (flops) by executing 1.88 Linpack-inner-loop instructions per clock. Better still, the company uses these results to compare performance to two other theoretical machines: a pure superscalar and a pure superpipelined machine. To achieve 94 MIPS and 33.3M flops performance, a “pure superscalar machine” that executes 1 instruction per cycle would have to run at 94 MHz. Alternatively, a “pure superpipelined machine” running at 25 MHz would have to execute 3.7 Linpack-inner-loop instructions per clock. While all this sounds pretty impressive, you must remember whence these numbers originate. The C4 example demonstrates that small benchmarks are even easier to manipulate than large ones. Dhrystone is a small standard benchmark that has been abused almost to the point of being meaningless. Rumors abound about compilers that sense Dhrystone source code and output canned, hand-optimized executable programs. Since the Dhrystone benchmark is small, it also fits neatly into a 16k-byte cache, eliminating time-consuming cache misses. And, the Dhrystone benchmark spends 30 to 35% of its run time doing string copies and string compares, often ignoring the results. Therefore, compilers that sense when computation results aren’t subsequently used can skip instructions and grossly skew benchmarks.

Software improves hardware performance

Tuning optimizing compilers is fair game. If a vendor finds execution bottlenecks and adjusts his compilers, obviously the benchmark code will execute faster. These optimization decisions may be at the expense of typical code, however. For example, vendors can rewrite run-time libraries with the Dhrystone character-string manipulation in mind. Then, they adjust the optimizing-routine selection instructions to favor benchmarking code. SPEC’s 10 benchmarks come close to being a “good” set. But even these benchmarks, developed by representatives from many system and workstation vendors, are imperfect. First, they are system benchmarks. Any extrapolation to any one component—microprocessor included—is dangerous.

Second, the SPEC benchmarks were selected and written to eliminate caching the program in fast memory. These benchmarks were larger than 32k bytes because, at the time they were selected, system caches were smaller than 32k bytes. Today, there are systems with 512k-byte caches. If your programs are larger than 512k bytes, the SPEC benchmark results may not represent the performance you are likely to see with your code.

Third, because the SPEC benchmarks only measure CPU and memory performance, they ignore I/O, graphics, and multitasking. Some embedded applications have little use for these features, but other applications might be I/O- or graphics-bound—and the wrong time to find out is after you’ve committed your design.

Fourth, SPEC wanted to provide a portable and
If possible, get the vendors to benchmark all or part of your application code.

freely distributable set of benchmarks to the market quickly. There was fast agreement among the members that a Spice simulation offered a useful, universal measure of scalar floating-point performance. However, according to John Mashey, Vice President of Systems Technology at Mips Computer Systems and SPEC committee member, the Spice input deck included in the benchmark suite was supplied by Hewlett-Packard and
wasn't examined by the organization. Mashey laments that this Spice deck isn't as floating-point intensive as a typical Spice run.

Finally, the last problem with the SPEC benchmarks—indeed with any benchmarks—is that as the computers and systems get more powerful, the benchmarks take less and less time to run. Eventually, the time measurements of each program vanish into the
noise of the system. Whereas the total reference run time on the VAX-11/780 was almost 19 hours, IBM’s RS6000 ran the timed portion of the benchmarks in just over 29 minutes.

SPEC’s next software revision will push the capabilities of the coming generation of systems. The organization also hopes to include benchmarks to measure I/O performance. Of course, revising its benchmarks will just provide a new target for the microprocessor and system vendors. And, vendors might try to play the old-revision game (use old-revision results if they are more favorable to your goals). As difficult as it may be, SPEC should attempt to move the targets far enough out that it might take four or five generations of systems to make the benchmarks obsolete.

As with many consumables, let the buyer beware. Manufacturers can get benchmarks to say anything they want. General Motors could claim their cars get 60 miles per gallon—by letting the engine idle and rolling the car down a long hill. Fortunately, the Environmental Protection Agency acts as an independent watchdog, performing uniform tests to ensure consistency. The engineering community has no such independent watchdog. SPEC, chartered to develop consistent tests, is largely a case of the fox guarding the chicken coop.

Mashey disagrees with that characterization of SPEC. Rather, he sees a bunch of foxes guarding one chicken—each wanting to make sure the other foxes don’t get his dinner. SPEC is a consortium composed largely of vendors. It doesn’t have to be that way. You can and should get involved in creating the benchmarks and monitoring the results by contacting SPEC, c/o Waterside Associates, 39510 Paseo Padre Pkwy, Suite 350, Fremont, CA 94538. (415) 792-2901.

References

Acknowledgment
We’d like to thank Michael Slater, whose valuable biweekly newsletter, the Microprocessor Report (Sebastopol, CA, (707) 823-5004) provided the inspiration and some of the information for this article.

Article Interest Quotient (Circle One)
High 512 Medium 513 Low 514
COP800

AVAILABILITY: Now.

COST: Less than $1 to $5 for standard parts in high volume.

SECOND SOURCE: Sierra Semiconductor.

CORE: Sierra uses the COP800 core for custom designs. National designs with a configurable-controller approach using a set of microcontroller building blocks.

Description: 8-bit CMOS single-chip family in which varying amounts of memory, peripheral functions, and I/O surround a purposely simple core. The program and data memory are treated separately so the COP800 has a Harvard architecture.

II-DATA-MOVEMENT INSTRUCTIONS

- Add, add with carry, and subtract with borrow.
- Logicals include rotates, shift compares, and conditionals.
- Decimal correct.
- Increment and decrement.

Bit manipulation: set, reset, and test individual bits in data memory, which includes those in data registers and I/O ports.

V-POWER-SAVING INSTRUCTIONS

- Halt mode, which is entered by setting data bit and exited by reset or low-to-high transition on the CKO pin.

Note: 1. Program-branch decisions are implemented in skip-the-next-instruction manner.

Specification summary: 15-bit program counter (PC) can address 32-byte program memory, which can include data and data tables. All data, control, and I/O registers are mapped into data-side memory space. Two bidirectional 8-bit and two unidirectional 4-bit I/O ports max. Each I/O pin has software-selectable options to adapt the chip to specific applications. On-chip peripheral functions include software-selectable I/O of as many as 39 I/O pins, 3-wire serial I/O, 16-bit timer/capture with encoder register and auto reload, and an 8-source interrupt. Maximum speed is 1-µsec instruction cycle (most instructions take one cycle). Clock for 1-µsec cycle is 10 MHz. Operates over 2.5 to 6V range and draws 9 mA running full speed at 1-µsec cycles, but less than 1 µA when halted.

Hardware notes: 1. Diagram shows basic COP800-family architecture. Each member of growing family has an emulator part that replaces standard masked-ROM with EEPROM or EPROM.

2. Sierra says cost of ASIC design can be as low as $40,000 up front (16 weeks' time), meaning ASICs can be cost competitive for 100k quantities.

SUPPORT

Cross-assembler for IBM PC and other computers. Form-fit emulators are available for every member of the family. These parts are 2-chip hybrids or single-chip EPROMs or EEPROMs.

EDN November 22, 1990
PIC 16C5X FAMILY

AVAILABILITY: Now.
COST: Under $1.50 in volume.
SECOND SOURCE: None.

Description: A family of single-chip CMOS EPROM-based microcontrollers that use only 33 single-cycle/single-word instructions. The family offers various amounts of I/O, RAM, and one-time programmable EPROM. Oscillator frequency ranges from dc to 20 MHz. Although it qualifies for the RISC moniker based on its 33 instructions, using the label to describe it is risky, if not confusing. The family only has a 2-stage pipeline without delayed branches or load delay slots rather than a 4- or 5-stage pipeline with delayed branches and load delay slots. The chips have a 2-address instruction format rather than the 3-address instruction format typical of RISC machines. Also, the PIC family must be programmed in assembly language—there are no compilers.

Microchip Technology Inc
2355 W Chandler Blvd
Chandler, AZ 85224
Phone (602) 963-7373
For more information, Circle No. 352

Status: To date, 75 million PICs have been sold worldwide, generally in high-volume, low-end consumer, personal computer, and automotive applications. CMOS one-time programmable versions were introduced in 1989 and are embedded in more than 1000 designs.

HARDWARE

CHARACTERISTICS

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract.
Logicals.
Rotate right and left, decimal adjust.
Swap halves.
Bit set and clear.

II—DATA-MOVEMENT INSTRUCTIONS
All RAM (general- and special-purpose registers) accessible by direct or indirect addressing.
Page addressing.
Move file.

III—PROGRAM-MANIPULATION INSTR
Skip if zero (for comparisons and bit tests).
Move literal to W.
Call subroutine.
Goto routine.

IV—PROGRAM-STATUS-MANIP INSTR
Can bit test on status-register carry, decimal carry, and zero.

V—POWER-SAVING INSTRUC
Sleep stops oscillator, CLRWDT clears watchdog timer. Tris instructs 3-state ports. Option loads option register.

Specification summary: Split-memory Harvard architecture with 12-bit-wide program EPROM and 8-bit-wide data registers. See table for EPROM and RAM sizes. Not expandable in memory because the microcontrollers are intended for self-contained, stand-alone applications. Power consumption ranges from less than 1 µA with the clock stop to 30 mA at 20 MHz.

PIC 16C5X CMOS microcontrollers

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<th>Part number</th>
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</table>

Hardware notes:
1. 12-bit-wide instruction word allows single-cycle execution of all instructions.
2. All current devices are fully static, silicon-gate CMOS designs that feature an 8-bit real-time-clock counter, watchdog timer, and 2-level program-counter-save stack for subroutine nesting.
4. A lower-cost RC-oscillator version is also available for applications that aren’t timing critical.

HARDWARE

Support

SUPPORT

Software

Microchip offers two IBM PC-hosted development systems. One, the Pik-Pak is a low-end development system that allows for assembly, execution, debugging, and analysis of microcode. The $495 price includes programmer and UV-erasable samples. The Pic-ICE development system ($2495) offers full-speed emulation to support real-time code development. The system includes in-circuit emulation pod with an 8k capture-tracer buffer, programmer, and diagnostic demo board. High-volume programming support is available from Microchip, Data I/O (Redmond, WA), and Logical Devices (Fort Lauderdale, FL).

Picaca cross-assembler is an IBM PC-hosted software tool that offers full-featured macro and conditional assembly capability. Picsim simulator software allows simulation of the PIC16C5X products on an instruction level. The simulator allows single-step, execute-until-break, and trace modes. Pico emulator software offers an interface with pull-down menus.

EDN November 22, 1990
**8048 FAMILY**

**AVAILABILITY:** Now.

**COST:** Masked-ROM parts are less than $2 in high volume (100k). EPROM parts cost $18 (100). CMOS parts cost as little as $3 (100k). Windowless-PROM parts cost $8 (5000).

**SECOND SOURCE:** Toshiba, NEC, Signetics/Philips, National Semiconductor, Oki, Fujitsu, UMC (Taiwan), with volume spread out among suppliers.

**CORE:** Zymos has been using 80C49 as a core for ASICs for several years. Others are following because 8048/49 combines popularity with small core size.

**Description:** Broad family of single-chip controller-type µ.Cs, including a version that can function as a slave (8041). Basic models don't have serial communications ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

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**HARDWARE CHARACTERISTICS**

**SOFTWARE**

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**I—DATA-MANIPULATION INSTRUCTIONS**

Arithmetic and logic.

- Bit set and reset.
- Two working banks of 8-bit registers.

**II—DATA-MOVEMENT INSTRUCTIONS**

Both internal and external RAM are fully accessible by instruction set.

- Indirect and direct data fetches.
- 8-level stack with expansion capability.
- Two vectored interrupts.
- Two programmable flag bits under software control.

**III—PROGRAM-MANIPULATION INSTR**

- Decrement and skip if zero.
- More than 20 conditional branches.

**IV—PROGRAM-STATUS-MANIP INSTR**

- Status word is fully accessible and is stored in the stack.

**Specification summary:** Split-memory architecture with 1k to 4k bytes of program ROM or EPROM on chip and 64 to 256 bytes in separate space, also on chip. I/O has its own space and instructions to operate directly on I/O ports. All spaces are expandable: program memory to 4k bytes, data memory to 256 bytes, I/O to unlimited amounts. I/O can use 8080/85 peripherals. Devices have 8-level stack for subroutine nesting and interrupt response. Dual banks of working registers allow rapid context switching. Family members execute their 1- and 2-cycle instructions at 1-cycle times ranging from 1.36 to 15 µsec. NMOS 5V technology in 40-pin DIP and 44-pad chip carriers; UV-erasable ROMs (EPROMs) and windowless PROM parts are available. CMOS versions available with idle and power-down features and optional flatpack packages. The 8049KB can drive four 10-mA LEDs.

---

**HARDWARE SUPPORT**

**SOFTWARE**

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From Intel: Intel plays down 8048 support, saying that there are now numerous third-party OEM suppliers of PC-hosted emulators for the 8048 family.

From NEC: Ekakit 84C-1 stand-alone emulator (less than $2000).

From others: Because of the broad-based popularity of this family, dozens of independent sources of development and application software exist, including support on universal development systems from Tektronix (Beaverton, OR) and Applied Microsystems (Redmond, WA).

Program library: Insite Library contains a variety of application programs.

---

**8-BIT NMOS AND CMOS**

Intel Corp

Embedded Controller Operation

5000 W Chandler Blvd

Chandler, AZ 85226

Phone (602) 961-8051

For more information, Circle No. 353

**Status:** Intel is still bullish about the 8048. However, Intel chose the 8051 over the 8048 as the kick-off core for ASICs and says it has no definite plans to use the 8048 as an ASIC core.

---

**HARDWARE CHARACTERISTICS**

**SOFTWARE**

---

**DATA MANIPULATION INSTRUCTIONS**

- Arithmetic and logic.
- Bit set and reset.
- Two working banks of 8-bit registers.

**DATA MOVEMENT INSTRUCTIONS**

- Both internal and external RAM are fully accessible by instruction set.
- Indirect and direct data fetches.
- 8-level stack with expansion capability.
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- Two programmable flag bits under software control.

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Program library: Insite Library contains a variety of application programs.

---

**MEMORY (bytes) | Package pins**

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<thead>
<tr>
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*Also available in 44-lead PLCC package.
8051/8052 FAMILY

AVAILABILITY: Now for 8051, 80C51, 80331, 80C31, 8751, 87C51, 80C32, 80C51FA, 87C51FA, 80C51FB, 8032, 8052, and 87C51FC.

COST: $2.30 (2k) for 8051; $3.33 (1k) for 8751; $3 (2k) for 80C51; $2.95 (2k) for 8052; $4.40 (1k) for 87C51; $4.90 (1k) for 87C51FA; $5.00 (1k) for 87C51FB; and $6.70 (1k) for 87C51FC.

SECOND SOURCE: Siemens, Signetics/Philips, Fujitsu, Oki, and Harris.

83C51FA, 87C51FA, 83C51FB, S7C51FB, 8032, 8052, and 87C51FC.

$4.90 (2k) for 83C51FA; $4.50 (1k) for 87C51FA; $5.00 (1k) for 87C51FB.

8051/8052 FAMILY

CORE: Intel's ASIC Components Group is using the 8051 as its starting point. It is the same supplier's widely used 8048 family. Architecturally, it features Intel's µP core. Signetics/Philips has the 80C51 core in its ASIC library.

Description: Expandable single-chip controller, an enhanced version of the same supplier's widely used 8048 family. It has Intel's µP core and $6.70 (1k) for 87C51FC.

Status: Generally thought of as the leader among the more powerful 8-bit single-chip µCs. This family faces stiff competition from high-end 8-bit µCs, such as Mitsubishi's 50740 version of the 6500/1, Motorola's 68HC11, NEC's 7811, Hitachi's 647180, and National's COP800, as well as from 16-bit µCs, such as Intel's own 8096 and National's 1004. The 8051 is among the most widely used cores in market-specific µCs.

8-BIT NMOS AND CMOS

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Hardware notes:
1. The 14 members of the 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip ROM.
2. The 8051's Boolean-processor capabilities refer to the way instructions make use of the CPU's program-status word is fully accessible via software. Status bits in timer and UART are also software accessible.
3. The 8051 family faces stiff competition from high-end 8-bit µCs, such as Mitsubishi's 50740 version of the 6500/1, Motorola's 68HC11, NEC's 7811, Hitachi's 647180, and National's COP800, as well as from 16-bit µCs, such as Intel's own 8096 and National's 1004. The 8051 is among the most widely used cores in market-specific µCs.

Specification summary: Expandable single-chip µC. Split-memory architecture has 4k- to 8k-byte ROM on chip and 128 to 256 bytes of RAM on chip. Each memory is expandable externally to 128k bytes. Four 8-bit ports on chip, but only one of these remains a port when you use all off-chip expansions and on-chip special functions. On-chip special functions include full-duplex hardware UART (to 500k baud), two or three 16-bit timer/counters, and interrupt system to service these internal functions along with two external interrupts with 3- to 7-µsec latency. Instructions are a superset of the 8048's, with pagd addressing eliminated. At 12-MHz clock frequency, most instructions take 1 µsec; multiply or divide requires 4 µsec. 8051 is also available in CMOS (80C51) with 12- or 16-MHz performance and idle/power-down modes.

Software:
From Intel: ASM-51 and PL/M-51, both containing a relocation and linkage utility, are available for the IBM PC and Intel microcomputer development systems.

From others: Many third-party software suppliers offer C compilers for 8051 with special features suited to microcontroller applications. Three such compilers are Micro Computer Control's (Hopewell, NJ) for $1495, Archimedes Software's (San Francisco, CA) for $851, and Franklin Software Inc's (San Jose, CA) for $895. All are hosted on IBM PC.
Mitsubishi Fast SRAMs

When You Need Fast Cache.

Reality is, no matter how fast you design your systems, customers always want them faster. To stay ahead, you need fast access to ultra-fast SRAM access times. And, Mitsubishi helps you lead the cache memory race with fast, 15ns Static RAMs in 28-pin SOJ, DIP and flat packages.

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Set your sights on Mitsubishi's fast Static RAMs for cache subsystems and pick the speed that will get you to market quick. And, to get to market in strength, turn the page. You'll quickly discover our volume production capabilities.
Mitsubishi Static RAMs.

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Mitsubishi offers the production quantities you need and the speeds you want. Plus, we give you through-hole and surface-mount packaging options.

<table>
<thead>
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<th>Part No.</th>
<th>Organization</th>
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<tr>
<td>M5M5178</td>
<td>8K x 8</td>
<td>15, 20, 25, 35, 45, 55</td>
<td>DIP, SOJ, Flat Pack****</td>
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<td>M5M5180</td>
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<td>20, 25</td>
<td>DIP, SOJ, Flat Pack</td>
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<td>M5M5187</td>
<td>64K x 1</td>
<td>15, 20, 25, 35, 45, 55</td>
<td>DIP, SOJ</td>
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<td>M5M5188</td>
<td>16K x 4</td>
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<tr>
<td>M5M5189</td>
<td>16K x 4 (/OE)</td>
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<tr>
<td>M5M5257</td>
<td>256K x 1</td>
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<td>M5M5258</td>
<td>64K x 4</td>
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<tr>
<td>M5M51001</td>
<td>1M x 1 or 256K x 4</td>
<td>35, 45</td>
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<tr>
<td>M5M51004</td>
<td>256K x 4 (/OE)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* 600 mil  ** 300 mil  *** TSOP: Thin small outline package; also available in reverse pin-out.
**** Flat package available in 25ns speeds and faster.
Some new products subject to availability.
When you need less.

When you need to pack more memory in less space and reduce power, Mitsubishi offers standard and soon, fast SRAMs in TSOP (thin-small-outline packaging). Static RAM packaging can't get any smaller than the TSOP, since it's virtually the size of the die.

Our TSOP SRAMs take up only half the surface area and are four times smaller in volume than equivalent pin-count, standard surface-mount packages. And, with a profile half that of standard surface-mount packages (1.2mm) and a low standby current (20µA to 50µA), TSOPs are perfect for portable, handheld, battery-backed applications.

So, if your design requires a lot of static RAM or just a little, call Mitsubishi for some action. We'll bring your vision to reality. Mitsubishi Electronics America, Inc., Electronic Device Group, 1050 E. Arques Ave., Sunnyvale, CA 94086. 1-800-624-8999 ext. 178C.
Even though they’re Power Factor Corrected, the power supplies you’re now using could ban your products from Europe after 1992. They might keep you from doing business domestically, too.

Your PFC supplies might not meet IEC 555-2 because they have too much current circulating in third and fifth order line current harmonics.

Pioneer supplies have less than 5% total harmonic current content. They feature built-in >.99 active Power Factor Correction, meet proposed IEC 555-2, all applicable international safety and EMC standards, and are available from 250 to 2000 watts, in single or multiple outputs. Delivery for most models in OEM quantities is 60-90 days.

P.S. — We apologize for not having brought you this information earlier. But the word is out. We’ve been shipping our PFC supplies worldwide for more than two years. So call us now at 800-233-1745, or 800-848-1745 in California.
EDN November 22, 1990

TMS370 FAMILY

AVAILABILITY: Now.

COST: ROM-based devices range from $3.50 to $11 (100k) depending on program memory, peripherals, and on-chip EEPROM mix.

SECOND SOURCE: None.

Description: Software-compatible family of CMOS µCs with on-chip EEPROM and peripheral support functions. Modular design architecture provides flexible reconfiguration and reduction in product design time. Various family members incorporate an 8-channel, 8-bit A/D converter, enhanced timers, serial peripheral interface, serial communications interface, EPROM, EEPROM, and ROM. Instructions typically perform combined load, operation, and store functions, increasing system performance and code efficiency. Form-factor emulator versions replace ROM with EPROM or EEPROM and allow prototyping and small runs.

Hardware note:
Diagram reflects the TMS370x5x, which supplements the 370Cx1x's single 16-bit timer, serial peripheral interface, programmable timer, 128-bit SRAM, and optional 256-bit EEPROM with a second 16-bit timer, a serial communications interface, memory expansion ports, another 128 bits of SRAM, and an 8-channel 8-bit ADC. The 370Cx3x contains a programmable timing module with watchdog timer, a miniserial communications interface, an 8-channel 8-bit ADC, 256-bit SRAM, and optional EEPROM.

From TI: XDS/11 is a IBM-PC-driven interactive development system ($2850). It provides full-speed, in-circuit emulation and debugging functions. XDS/22 development system ($8250) adds extended breakpoint, trace, and timing functions to the XDS/11 system. A design kit ($370) lets you analyze the feasibility of using the TMS370 family for your application. EEPROM programmer ($1250) comes with power and interface cables, software, and sockets for the 370 family and EPROMs such as the 2732, 2764, 27128, and 27256.

From others: ElectroRent provides rental use of TI tools for IBM PCs. Logical Devices (Fort Lauderdale, FL) has a TMS370 microcontroller module for AllPro programmers.

From TI: Cross-assembler, linker, full ANSI C compiler, and C source debugger available on IBM PCs and DEC VAXs under VMS.

From others: Allen Ashley (Pasadena, CA) supplies an assembler/linker and Intermetrics (Cambridge, MA) offers a C compiler that runs on IBM PCs. Macrochip Research (Carrollton, TX) has an assembler and midrange emulator for both IBM and Macintosh personal computers. P&E Microcomputer Systems (Woburn, MA) provides an integrated assembler and simulator for IBM PCs.

TMS370 family matrix

<table>
<thead>
<tr>
<th>370Cx</th>
<th>370Cx32</th>
<th>370Cx50</th>
<th>370Cx52</th>
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<tbody>
<tr>
<td>ROM</td>
<td>8k</td>
<td>8k</td>
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<td>FFE</td>
<td>4k</td>
<td>8k</td>
<td>4k</td>
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<tr>
<td>Data EEPROM</td>
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<tr>
<td>RAM</td>
<td>128</td>
<td>256</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>Timer 1, watchdog</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>timer</td>
<td></td>
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<tr>
<td>Timer 2</td>
<td></td>
<td></td>
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<tr>
<td>Serial peripheral interface</td>
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<tr>
<td>Serial communications interface</td>
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<td></td>
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<tr>
<td>A/D port</td>
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<tr>
<td>I/O links</td>
<td></td>
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</tr>
<tr>
<td>Package</td>
<td>32 DIP/PLCC</td>
<td>68 PLCC</td>
<td>68 PLCC</td>
<td>68 PLCC</td>
</tr>
</tbody>
</table>

8-BIT CMOS

Texas Instruments Inc
Microprocessor and Microcontroller Products Div
Box 809066
Dallas, TX 75380
Phone (800) 232-3200
For more information, Circle No. 355

Status: Supports real-time applications that may previously have required analog, bit-slice, or multiple controllers. The alterable nonvolatile memory allows the µC to retain critical data without power. The vendor offers 16 function modules that it will configure for your application if your volumes exceed 50,000.

Software: Supports real-time applications that may previously have required analog, bit-slice, or multiple controllers. The alterable nonvolatile memory allows the µC to retain critical data without power. The vendor offers 16 function modules that it will configure for your application if your volumes exceed 50,000.

Hardware characteristics: Flexible reconfiguration and reduction in product design time.

Software: Supports real-time applications that may previously have required analog, bit-slice, or multiple controllers. The alterable nonvolatile memory allows the µC to retain critical data without power. The vendor offers 16 function modules that it will configure for your application if your volumes exceed 50,000.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8 x 8-bit multiply, 16 x 8-bit divide, and BCD.

II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Application to many instructions.
Indexing via B register.
16-bit moves.

III—PROGRAM-MANIPULATION INSTR
Call and return. Trap. Bit test and jump on both I/O and memory. Conditional jumps using program-counter-relative addressing.

IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, overflow, and interrupt enable. Instructions to change carry and interrupt enable.

Specification summary: The programmable timer module uses the on-chip dual-ported RAM to store its commands as well as the timer values. This module allows input capture on as many as 6 pins, 4 of which have a programmable prescaler. The TMS370 CMOS family members use a 5V supply over the oscillator frequency range of 2 to 20 MHz and over the temperature range of -40 to +85°C. The application program, register file, and peripheral file share memory space.
Motorola and NCR have a joint ASIC pact to use CMOS 6805 as a core along with NCR's similar 6502 µP core. SGS Thomson has ST6 core, which has architecture somewhat similar to the 6804's.

SECOND SOURCE: Harris, Hitachi, and SGS Thomson.

COST: $1 to $8. CMOS parts are more expensive than NMOS ones.

AVAILABILITY: Now for most models. Motorola can build customer-specific versions in as little as six months. Family offers various amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 4 MHz. Some parts contain an on-chip A/D converter, EEPROM, serial I/O, and software security. Customer-specified microcontrollers use this core for mixing and matching of peripherals to reduce cost for specific customer applications.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test. Bit tests can be made on all I/O and direct-page memory bits. 68HC05 has 8 x 8-bit multiply.

II—DATA-MOVEMENT INSTRUCTIONS
Relative addressing allows data relocation. Temporary indexing within the 256-location limits of 8-bit index.

III—PROGRAM-MANIPULATION INSTRUCTIONS
18 conditional branches, including branch of interrupt line test. Mostly the same conditional branches as the 6800, but with more emphasis on branch-upon-bit and interrupt tests. Only 15 levels of subroutine nesting, including interrupt returns; 31 levels on certain new parts.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Instructions for manipulating bits in status register and timer.

V—POWER-SAVING INSTRUCTIONS
CMOS 6804s and 6805s have Stops and Wake instructions and will safely reset themselves when the clock is reapplied.

Specification summary: Common-memory architecture in which instructions, data, I/O, and timers all share the same memory space. This scheme allows bit manipulation and rotation of I/O. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most 6805s. New 68HC05s have a 2.1-MHz internal bus speed. Some, like the 68HC705C8, are available with a 4-MHz bus speed. Some parts offer program security, on-chip 5V EEPROM, A/D converter, serial peripheral interface, serial communications interface, timers, PWM D/A converter, LCD drivers, DTMF generators, and other customer-specified peripherals. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs, SOICs, and shrink DIPs; 44-, 52-, and 68-pin PLCCs; and other fine-pitch packaging options.

HARDWARE SUPPORT

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733.

From SGS Thomson: Interactive development software.

From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has cross-assemblers for 6805 and 6804 that run on IBM PCs and compatibles. Introl (Milwaukee, WI) provides cross-compilers and cross-assemblers. C cross-compiler with macro cross-assembler from Bytecraft Ltd (Waterloo, Ontario, Canada).

From Harris: Single-board evaluation kit that interfaces to IBM PC via RS-232C line.

From SGS Thomson: INICE4-8 development and emulation system.

From others: A number of third-party companies, including Sophia Systems (Santa Clara, CA) and American Automation (Tustin, CA), provide hardware emulators for the 6805 family. Most of these emulators interface to IBM PCs.

From Motorola: The less costly M68705EV5 (HMOS) and M68HC05EV5 (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.

Hardware notes:
1. Diagram is for nonexpandable Model P2 in a 28-pin package.
2. Comparison of 6805 with 6800: Stack is only 64 bytes deep. Only one accumulator. Index register can only span 256 memory locations. However, family supports a 16-bit offset addressing mode, thus the µP can access 256-byte tables anywhere within the memory space. Program counter is as long as 14 bits in some members of this family. Only one 4-bit timer counter.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Special pin initiates program.
4. Harris has ROMless emulator versions (68EM05/C4/D2) for prototyping and low-volume production. Harris brings all ROM access buses out for direct interfacing to industry-standard EPROMs. Available in 40-pin piggyback for 2764.
5. Motorola currently has five field-programmable 68HC05 versions with on-chip EPROM instead of mask ROM to permit development and low-volume production.
Proprietary advanced VFD technology now allows Noritake to offer a broad line of super-smart dot character and dot matrix vacuum fluorescent display modules that will satisfy the most demanding requirements.

- **HIGH VISIBILITY**
- **LOW POWER**
- **SURFACE-MOUNT TECHNOLOGY**
- **LONG-TERM RELIABILITY**
- **5Vdc POWER SUPPLY OPERATION**
- **WIDE TEMP. RANGE: -40°C TO +85°C**

The models shown are typical of the broad selection available on an immediate delivery basis. Contact our nearest sales office or representative for counsel on the best Noritake VFD for your application, as well as for details on costs, custom designs, deliveries, etc.
New controller provides simultaneous control of two, independent power supplies.

The PIA 3200 Controller allows a user to set the voltage and output current, and measure or read back the set values. A pair of fully isolated channels provide for the control of two independent, regulated power supplies such as the PAK series of burn-in switchers, and high-current PAD-L/LP supplies.

An advanced GPIB interface function and sequence control mode, used for programmable control, enables DC power supplies to be compatible with automated measuring systems and provides for up to 56 settings of the output voltage, output current, overvoltage and voltage drop protection for each channel. The programming format conforms to IEEE-488.

The sequence control mode permits storage of each DC power supplies' settings and execution times, up to a maximum of 256 steps per sequence, via the GPIB interface. Storage and recall of up to six sequence patterns between any consecutive addresses can also be achieved. Normal speed mode is 50 msec-130 min/step; high speed mode is 0.2 msec-999.8 msec/step.

DC switchers offer low-noise, high power in a compact package.

New, low-noise DC CC/CV power supplies combine high current, small size and high power density for systems or bench applications. Output voltages range from 0-6 to 0-60 VDC with capacities of 350 W, 700 W and 1000 W.

Power densities of the PAK series range up to 2.5 watts per cubic inch. A typical 1000 W supply is packaged in a 19-lb. 5" x 8" x 14" enclosure.

Overall efficiency of 80% reduces power consumption, system heat radiation, and cost per watt. Line and load regulation averages ± 0.30% over the full input range. Ripple is typically 2% of nominal output at full load current.

New 50 W, 150 W and 300 W modular electronic loads can test multiple output power supplies, batteries, capacitors, and process control I/O ports.

These rack-mounted loads are ideally suited for use in systems applications such as burn-in power supply testing and battery and capacitor discharge tests.

A single rack mount, for example, accommodates up to eight 50-watt, four 150-watt, two 300-watt loads or various combinations up to 600 W. Depending upon the capacity, input voltages may range from less than 2 to 60 VDC.

The constant current, contact voltage and constant resistance modes may be remotely controlled using external voltage. Computer control for the PLZ-WU series is available using the GPIB bus.

New software-controlled power test systems provide fast, flexible test solutions without expensive programming.

The KITS (Kikusui Intergrated Test Systems) software package, built around National Instruments Lab Windows®, is a powerful window-oriented, menu-driven environment with interactive development capabilities that allows the user to plug in a variety of programmable instruments from various manufacturers. Directly available from Kikusui are digital scopes, electronic loads, AC & DC power sources and hi-pot test systems. The system provides optimal instrument control, ease of programming and simplified characterization of the Unit Under Test (UUT). In addition to running tests, this combination hardware/software system offers the necessary tools to analyze, display and store test parameters and data.

Kikusui International

19601 Mariner Avenue, Torrance, CA 90503
800/545-8784 or 213/371-4662

Kikusui International
6801/6301/68HC11

AVAILABILITY: Now.
COST: From less than $3 to $20 (1k).
SECOND SOURCE: Hitachi, SGS Thomson, and Toshiba. Hitachi sources the 6801 and calls the part 6301. SGS Thomson sources the 6801. Toshiba is a second source for 68HC11 devices.

Description: 6801 is a large, expandable, single-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8 x 8-bit multiplication, and a multifunction 16-bit timer. 68HC11 has a second 16-bit-wide register; an 8-function timer; a 2-function pulse accumulator; an enhanced UART (SCI); a 1-MHz serial shifter; an 8-channel, 8-bit A/D converter; and a 512-byte EEPROM. One-time-programmable/mask versions include as much as 24k-bit on-chip EPROM/ROM and built-in device selects and bank switching circuits for as much as 20-bit addressing.

HARDWARE CHARACTERISTICS SOFTWARE

- I—DATA-MANIPULATION INSTRUCTIONS
  - Arithmetic and logic. Instructions to take advantage of 2 accumulators, including 8 x 8-bit multiply. 68HC11 has additional 16-bit operations, integer and fractional divides, and bit manipulation.
  - II—DATA-MOVEMENT INSTRUCTIONS
    - Can reach the first 256 locations of memory with short instructions. Can list-process efficiently with the index register (2 on 68HC11) and can add accumulator to index register within a 64-byte range. Relative addressing allows data relocation. Has 16-bit load and store.
  - III—PROGRAM-MANIPULATION INSTRUCTIONS
    - Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM. Eight levels of prioritized, vectored interrupts (21 on 68HC11).
  - IV—POWER-SAVING INSTRUCTIONS
    - Instructions for storing status register or transferring to or from accumulator. 68HC11 has additional active bits related to stop mode.

Software notes:
1. 6801 has all 6800 µP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set with 88 additional op codes.

Hardware notes:
1. Diagram is for 6801. See table for other family members.
2. Motorola provides one-time-programmable versions of some HC11 family members that have EPROM program memories in inexpensive windowless packages for one-time programming in moderate-volume production (to 1Ok).
3. Motorola’s 68HC11 is a much enhanced 6801. 68HC11A8 has a 512-byte EEPROM; 68HC811E2 has a 2k-byte EEPROM; 68HC711E9 has a 12k-bit EPROM; 68HC711K4 has a 24-kbit EPROM.

SUPPORT SOFTWARE

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 891-3733. C compiler runs on Unix System V for 68HC11. For the least expensive approach, use 6801 parts with Lilbug monitor in on-chip ROM (MC6801L1).
From SGS Thomson: Interactive development software.
From others: Cross macroassemblers and linking loaders, some relocatable, run on popular minis and personal computers. For example, C compiler from Archimedes (San Francisco, CA) runs on the IBM PC ($995) and DEC VAX ($3995 to $5995).

EDN November 22, 1990
6500/1, 65C124, 65C265, 50740, 37700

8-BIT (AND 16-BIT) NMOS AND CMOS

Rockwell International
Digital Communications Div
4311 Jamboree Rd
Newport Beach, CA 92658
Phone (800) 854-8099; in CA (800) 422-4230
For more information, Circle No. 358

Mitsubishi Electronics America Inc
1050 E Arques Ave
Sunnyvale, CA 94086
Phone (408) 730-5900
For more information, Circle No. 359

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545
For more information, Circle No. 360

AVAILABILITY: Now for all NMOS and most 8-bit CMOS parts.
COST: Prices range from $2 to $20 according to complexity of part and volume. Volume leader Mitsubishi's prices range from $4 to $60.
SECOND SOURCE: NCR (licensed) and California Micro Devices for Rockwell NMOS parts. Western Design Center (WDC) has licensed a number of suppliers worldwide for its CMOS designs.
CORE: Standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, and several others. Widely used because of compact 6502 die size.

Description: There are three different sources for single-chip versions of the 6502 µP: the original 6500/1 NMOS family from Rockwell, the new 65C124 and -13 CMOS family from WDC, and the 50740 CMOS family from Mitsubishi. Most parts are 100% software compatible with 6502, although in some cases enhanced instructions such as bit manipulation have been added. Because of the small size of the 6502 core, many parts take a standard-cell ASIC approach. Vendors claim these 1-chip sets have a speed advantage over competing single-chip devices due to the 6502's 2-cycle bus and pipelining.

Status: Mitsubishi's 50740 Series is a top volume leader among 8-bit µCs. Mitsubishi's explanation for the part's success is its use in Japanese consumer products. Standard or custom 50740s are found in products from Hitachi, JVC, Sanyo, and Minolta.

HARDWARE

CHARACTERISTICS

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports.
Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset.

II—DATA-MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset is limited to 8 bits in 2 CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables.

III—PROGRAM-MANIPULATION INSTRUCTIONS
Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits.

Specification summary: Single-chip nonexpandable and expandable versions of 650X family. Have 2k- to 16k-byte ROM, 64- to 512-byte RAM, as many as 52 I/O lines, and one or more 16-bit programmable interval timers, as well as two or more programmable interrupts (plus the 650X's NMI interrupt). Family options (Rockwell) include RS-232C port and bus expansion. Operates from 5V, 500 mW and has separate 5V supply to keep 64 static bytes of RAM alive (50 mW required). Wide variety of package types and sizes from various suppliers. Full MIL-spec temperature-range devices from WDC.

Software notes:
1. 6500/1 instruction set is identical to that of previous 650X family devices such as 6502, with the exception of bit-manipulation instructions for some devices. No new instructions added to handle new on-chip features such as timers and I/O because the µP handles them as if in external memory space.
2. Mitsubishi chips have some added instructions.
3. WDC's 65C134 adds some instructions and an operating voltage range of 1.8 to 5.25V.

SUPPORT

From Rockwell: Because the 6500/1 emulator runs on LCE system and Aim-65 (Dynatemp, Irvine, CA), you can use existing 6502 programming development software. A debugging monitor is available for all 6500/1 and 6500/11 devices, and the macroassembler supports enhancement instructions. Cross software available.
From Mitsubishi: Cross software for MS-DOS. (Has plans for a C compiler and Forth interpreter.)
From WDC: Many software packages available from third parties for the W65C02/W65C816 µPs.

From Rockwell: R6500/1 personality card ($996), which plugs into LCE System ($1250) uses emulator part, the 64-pin 6500/1E (75$). Backpack part will be ROMless 40-pin R6500/1EAB ($42), into which you can plug industry-standard EPROMs.
From Mitsubishi: Debugging machine PC4000E ($1000) with in-circuit-emulator (ICE) cards for each device model ($750 to $1500).
From WDC: Toolbox Design System ICE for W65C124 runs on an Apple II GS host and can communicate with an IBM PC via a serial port ($4995).

Hardware notes:
1. Diagram favors initial Rockwell 6500/1 version. Most other versions are more complex.
2. Mitsubishi 740 Series parts are all CMOS and have as many as 16k bytes of ROM and 512 bytes of RAM. Some models have special functions such as UARTs, 8-bit A/D converters, LCD drivers, or high-voltage (-35V) outputs. Some have 56 pins of I/O.
3. Mitsubishi's new CMOS M37700 version has an 8-bit external/16-bit internal data bus, much like the 68C816 version of the 6502 µP. On chip, it can have as many as 32k bytes of ROM, 2k bytes of RAM, eight 16-bit timers, 2 UARTS, 1 watchdog timer, and an 8-channel 8-bit ADC. Memory is expandable to 16M bytes off chip.
4. WDC's first part, 65C124, has been joined by 65C134—a 6502 core µP—which includes a low-power LAN connection and UART.

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4. WDC's first part, 65C124, has been joined by 65C134—a 6502 core µP—which includes a low-power LAN connection and UART.
Thanks to us the government knows this is not an enemy sub.

Here in the lonely depths off America's coast, sophisticated listening devices assure our defense forces a passing butterfly fish is not an enemy intruder.

On board each device are ITT Cannon microminiature connectors.

In fact, you'll find Cannon microminiature connectors performing in some of the nation's most critical projects, under some of the world's most demanding conditions.

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FAX: (714) 754-2142.
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**Z8, SUPER8**

*AVAILABILITY:* Now for ROMless and 1k-, 2k-, 4k-, and 8k-byte parts; 2k- and 8k-byte EEPROM; and one-time programmable at 8, 12, 16, and 20 MHz. Sharp and Zilog have CMOS now. SGS Thomson has 4k-byte EPROM and 8-byte ROM.

*COST:* Less than $3.50 for NMOS Z8 in volume. $3.60 for NMOS Super8 in volume. (28-pin version for $1.) Less than $5 for CMOS ZB.

*SECOND SOURCE:* SGS Thomson (licensed); Sharp for both NMOS and CMOS; VLSI Technology for CMOS.

**Description:** Z8 is a single-chip μC that is a composite of many machines. You can’t necessarily use its powerful features simultaneously, a common problem with single-chip units. Not really compatible with supplier’s ZBO or ZBOO because architecture is so different; closest to ZBOO. However, slave ZB versions interface to ZBO and ZBO000 buses. Super8 version has more of everything: more data and program memory, more on-chip peripherals, more instructions.

**HARDWARE CHARACTERISTICS**

**SOFTWARE**

I—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, and subtract with borrow.

Multiply and divide added to Super8 version.

Logicals: AND, compare, complement, OR, and exclusive OR.

Rotates and swaps.

II—DATA-MOVEMENT INSTRUCTIONS
Address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative.

Block transfer: load constant autoincrement, load external autoincrement.

Load: clear, load, load constant, load external, and pop and push.

III—PROGRAM-MANIPULATION INSTRUCTIONS
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, jump relative conditional, and return.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS
Set, reset, and complement of carry flag.

**Note:** Ability to set, reset, and test any bit or combinations of as many as 8 bits lets any byte function as a user flag register.

**Specification summary:** Unique architecture with 3 memory spaces: program memory (0, 2k, 4k, or 8k bytes in internal masked ROM; rest to 64k bytes can be external), data memory (to 64k bytes external), and CPU register file (256-byte space that includes 124 general-purpose working register/accumulator). Executes 129 instructions at 0.5 to 3.0 μsec at 8-MHz internal clock (16-MHz oscillator). Has built-in duplex UART (96k bps) and two 8-bit timers, each with 6-bit prescaler. Enhanced Super8 has 352 bytes of on-chip data and control registers, 256 of which are general purpose. New multiply and divide instructions on Super8. Its on-chip peripheral functions include DMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has 600-nsec interrupt response with 37 interrupt sources.

**Software note:** The data- and program-manipulation instructions use the working registers in the CPU. The instructions that apply to the external data RAM are essentially just loads and stores. (There is a similarity to RISC philosophy.)

**Development**
Development packages are available from JK Engineering (Singapore, 65-744-8414). In the US, IAM (Sacramento, CA) distributes JK Engineering’s products. Development packages in various configurations are also available from Zilog Inc (Campbell, CA) and Inner Access (Belmont, CA). Emulation packages are available from Orion Instruments (Redwood City, CA), Microtek (Beaverton, OR), Creative Technology (Atlanta, GA), and Sophia Systems (Santa Clara, CA). This list isn’t exhaustive.

Software development tools are available from Allen Ashley (Pasadena, CA), Avocet (Rockport, ME), Relational Memory Systems (San Jose, CA), and Western Wares (Norwood, CO). You can purchase compiler software from Micro Computer Compilers (Hopewell, NJ), 2500 AD (Buena Vista, CA), and Inner Access (Belmont, CA). This list isn’t exhaustive.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
(408) 370-8000

For more information, Circle No. 361

**Status:** According to Zilog, Z8 volume is growing at a compound annual growth rate of 35%. and ZB has had several hundred design wins (many in Far East); some of these design wins are now going into production. Meanwhile, second-source SGS Thomson has turned its CMOS efforts to its ST9, a proprietary enhancement of the Z8, which SGS Thomson uses for an ASIC building block.
TMS 7000 family matrix

<table>
<thead>
<tr>
<th>Model</th>
<th>ROM (bytes)</th>
<th>RAM (bytes)</th>
<th>Clock (MHz)</th>
<th>I/O</th>
<th>Interrupt levels</th>
<th>Timers</th>
<th>Serial port</th>
<th>Power required</th>
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<td>128</td>
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<td>13 bit</td>
<td>UART</td>
<td>2.5-6.0</td>
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<td>13 bit</td>
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<td>70C02</td>
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<td>256</td>
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<td>32</td>
<td>6</td>
<td>21, 21, 10 bit</td>
<td>UART</td>
<td>2.5-6.0</td>
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<td>6</td>
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<td>6</td>
<td>21, 21, 10 bit</td>
<td>UART</td>
<td>2.5-6.0</td>
</tr>
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</table>

Hardware note:
Supplier uses a "strip-chip" architecture to keep registers and control elements in isolated, self-contained modules in silicon, then uses a single layer of metal to interconnect chip. This approach is similar to the cell-library, semicustom approach and useful for the same reason. Changes can be made easily, which helps TI bring out new models or give large customers special variants.

Texas Instruments Inc
Microprocessor and Microcontroller Products Div
Box 809066
Dallas, TX 75380
Phone (800) 232-3200
For more information, Circle No. 362

Status: Primary supplier TI has switched its emphasis to CMOS models with expanded features. Low-end devices (70CT20/40) offer an alternative for designers who are using 4-bit µPs but seek a low-cost 8-bit alternative.
WHY MORE COMPANIES ARE PLUGGING US INTO THEIR DESIGNS.

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EDN November 22, 1990
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Company ___________________________ Address ___________________________
City ___________________________ State __ Zip ___________________________
Phone ___________________________

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**8085AH/80C85**

**AVAILABILITY:** Now.
**COST:** Prices for these older multisourced parts have dropped to $1 and below, with prices as low as $0.65 for volume purchases. CMOS parts, especially faster ones, are more expensive. Radiation-hardened CMOS parts are very expensive ($300 to $800).

**SECOND SOURCE:** 8085: NEC, Toshiba, and Mitsubishi. 80C85: Harris, Newbridge Microsystems, and Oki. Harris supplies nuclear-radiation-hardened CMOS to military and aerospace customers.

**CORE:** Newbridge offers 80C85B macrocells in its ASIC library.

**Description:** Based on the older 8080 µP, this family has proven to be a good general-purpose, midrange µP, though not the most efficient one for small programs. 8085 executes 8080 instructions, but with simpler hardware. Z80 (see pg 120) is an enhanced 8080 but has different package pinouts and bus operation. The new 8086 (see pg 128) is only vaguely software compatible, but the 8-bit-bus 8086 version of 8086 can interface to 8080 and 8085 peripherals.

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### HARDWARE CHARACTERISTICS 8-BIT NMOS AND CMOS

#### I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic and logic.

#### II—DATA-MOVEMENT INSTRUCTIONS
Uses 3 pairs of so-called general-purpose registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can perform multiple indexing with these, but takes additional steps compared with classical index-register concept. 8085 has two additional instructions—RII and SIM—that interface with new serial-I/O pins and interrupt system.

#### III—PROGRAM-MANIPULATION INSTR
Uses stack pointer to create LIFO stacks in external RAM for unlimited subroutine nesting. All GP registers can be incremented and decremented. Multiple-interrupt capability. Bus controls allow addition of DMA.

#### IV—PROGRAM-STATUS-MANIP INSTR
Software access to status register.

**Specification summary:** Common instruction and data architecture (64k bytes) with optionally separate I/O space (256 addresses). Three 16-bit pointer registers allow efficient addressing of 64k-byte main-memory space. 78 basic instructions with 2-µsec (typ) register-to-accumulator addition-execute time. 8085A has on-chip clock and needs only 5V, 5-MHz and CMOS versions of the 8085A available. The Newbridge Microsystems (Calmos) version officially supports the extended 8085 instruction set.

---

**Hardware note:**
The 8085 differs from the 8080 in that the 8085 has an on-chip clock, needs only a 5V supply, and has relaxed memory-access time. But because it multiplexes the lower 8 bits of address on data bus, it's not pin compatible with 8080. New pins gained by multiplexing implement address-latch strobe, four additional interrupts, and two serial-I/O lines. For small "few-chip" µP systems, a designer can use 8155/56 and 8555/8755 combo chips with built-in address latches.

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**EDN November 22, 1990**

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**HARDWARE SUPPORT SOFTWARE**

Most of the vendors of third-party µP development systems have included 8080/8085 development components as a routine part of their catalogs. Typically, these systems use IBM PCs as hosts.

Most of the many companies that supply 8080/8085 development systems also supply the software. Also, many software houses have 8080/8085 software in every conceivable category.
Z80

8-BIT NMOS AND CMOS

Zilog Inc
Intelligent Peripheral Controllers Product Line
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-9000
For more information, Circle No. 364

Status: By far the most successful 8-bit µP. The Z80 is still being used in new designs but may be superseded by the new enhanced versions. Of these, the Zilog Z180/Hitachi 64180 seems to be the most popular, but the Zilog Z280 represents the greatest Z80 enhancement. The Z80’s momentum will probably last for the rest of this century, especially in ASIC-core form.

Hardware notes:
1. Support chips include peripheral interface, timer, serial communications, and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. All Z80 enhancements are in CMOS. The first is the Zilog Z180/Hitachi 64180, to which many Z80 designers are converting. The second is the supplier’s Z280, which boosts the Z80 into minicomputer performance. In addition, the NEC 78XX single-chip device is similar. Most are covered elsewhere in this directory.

Software notes:
A variety of software supports the Z80 including assemblers and cross-assemblers, software simulators, high-level-language compilers, the venerable CP/M operating system (Digital Research), and the MS/X operating system, which is popular in Japan. Other third-party suppliers include 2500 AD, Archimedes, Avocet Systems, Enertec, Huntsville Micro, Softaid, Software Development Systems, Microtec Research, and Z-World. Contact nearest Zilog sales office for more information.

Hardware

8-BIT MANIPULATION INSTRUCTIONS
8-bit arithmetic and logic
16-bit arithmetic BCD add and subtract.
Nine types of rotate and shift directly on any register or memory location.
Can set, reset, or test bit in any register or memory location.

II—DATA-MOVEMENT INSTRUCTIONS
8- or 16-bit register or memory loads.
Two index registers allow indexed addressing.
Extensive memory-block move/search commands.

III—PROGRAM-MANIPULATION INSTRUCTION
Uses 16-bit stack pointer with LIFO stack with RAM.
Relative-jump capability. Interrupt capability with three types of selectable response.

IV—PROGRAM-STATUS-MANIP INSTRUCTION
Seven flag bits, including arithmetic and overflow, can be stored and tested.

Specification summary: Upwardly compatible with 8080A software but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 0.5 to 1.8 μsec (1.5 μsec avg) for 8-MHz Z80 and 1.0 to 5.5 μsec (2 μsec avg) for 4-MHz Z80A. 6-, 8-, 10-, and 20-MHz versions are also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires single-phase clock and one 5V supply at 60 mA for Z80, 90 mA for Z80A. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. CMOS-type parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 μA in power-down (clock-stopped) mode. NMOS and CMOS versions available in DIP, quad flatpack, and PLCC.
# The MOST 80C51 Microcontroller Derivatives in the World

## Philips Components-Signetics

**80CXXX = ROM-Less**

**83CXXX = Masked ROM**

**87CXXX = EPROM/OTP**

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<th>OTP &amp; EPROM</th>
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<th>RAM (bytes)</th>
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<th>TIMERS</th>
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<td>X</td>
<td>2K</td>
<td>64</td>
<td>2 + 3/8</td>
<td>X</td>
<td>1</td>
<td>24 Pin Skinny DIP</td>
<td>A28, F24, N24</td>
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<td>64</td>
<td>2 + 5/8</td>
<td>X</td>
<td>1</td>
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<td>2</td>
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<td>512</td>
<td>4</td>
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<td>32K ROM, 512 RAM, WD</td>
<td>A44, B44, F40, K44, N40</td>
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</tbody>
</table>

**Footnotes**

1. No ROM-less derivative available
2. 80C31, 80C32 = ROM-less
3. 80C51, 80C52 = Masked ROM
4. 87C51, 87C52 = EPROM/OTP
5. Piggyback available for EPROM development

**Abbreviations**

- A/D = Analog-to-Digital Converter
- PWM = Pulse Width Modulation
- WD = Watchdog Timer to reset the microcontroller
- T2 = Capture/Compare Counter/Timer with High Speed Outputs
- I2C = Inter-Integrated Circuit Serial Communications Bus
- OSD = On Screen Display
- D/A = Digital-to-Analog Converter
- CAN = Controller Area Network Serial Communications Bus
- CCU = Cryptographic Calculation Unit

**Package Types**

- A = Plastic Leaded Chip Carrier (PLCC)
- B = Plastic Quad Flat Pack (PQFP)
- N = Plastic Dual In-line Package (PDIP)
- F = Windowed Ceramic Dual In-line Package (CDIP)
- K = Windowed Ceramic Leaded Chip Carrier (CLCC)
- T = Plastic Very Small Outline Package (VSO)

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<th>COMPANY</th>
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<tbody>
<tr>
<td>ARCHIMEDES</td>
<td>2159 Union Street</td>
<td>C - COMPILER FOR 8051 FAMILY</td>
</tr>
<tr>
<td>SOFTWARE</td>
<td>San Francisco, CA 94123</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(415) 567-4010</td>
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<tr>
<td>FRANKLIN SOFTWARE</td>
<td>888 Saratoga Ave. #2</td>
<td>C - COMPILER FOR 8051 FAMILY</td>
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<tr>
<td></td>
<td>San Jose, CA 95129</td>
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<tr>
<td></td>
<td>(408) 296-8051</td>
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<tr>
<td>METALINK</td>
<td>325 E. Elliot Road, Suite 23</td>
<td>MICROICE + EMULATOR</td>
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<td></td>
<td>Chandler, AZ 85225</td>
<td>SUPPORTS 80C51 MICROCONTROLLER FAMILY</td>
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<tr>
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<tr>
<td>NOHAU</td>
<td>51 E. Campbell Ave.</td>
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<td></td>
<td>(408) 866-1820</td>
<td></td>
</tr>
</tbody>
</table>

**PROGRAMMING SUPPORT CONTACTS**

- **BP Microsystems**
  10681 Haddington, Suite 190
  Houston, TX 77043
  (800) 225-2102

- **DATA I/O Corp.**
  10525 Williams Road N.E.
  P.O. Box 97046
  Redmond, WA 98073-9746
  (206) 867-6899

- **GTEK, Inc.**
  P.O. Box 2310
  Bay St. Lewis, MS 39521-2310
  (800) 262-4385

- **Logical Devices, Inc.**
  1201 Northwest 66th Place
  Ft. Lauderdale, FL 33309
  (305) 974-0967

- **Logical Systems**
  P.O. Box 6184
  Syracuse, NY 13217-6184
  (315) 478-0722

- **Needham's Electronics**
  4535 Orange Grove Ave.
  Sacramento, CA 95841
  (916) 924-8037

- **North Valley Products**
  P.O. Box 32889
  San Jose, CA 95152
  (408) 929-5345

- **Stag Microsystems**
  528-5 Weddell Drive
  Sunnyvale, CA 94086
  (408) 988-1118
### Z180, HD64180

**8-BIT CMOS**

**AVAILABILITY:** Now for 6-, 8-, and 10-MHz parts.

**COST:** For 10-MHz Z180, $12 (100) and $8 (1000). For 6-MHz HD64180, $7 (100) and $6 (1000).

**SECOND SOURCE:** None.

**CORE:** Zilog and Hitachi consider the basic Z180 and 64180 a standard cell for building high-integration µPs and µCs.

**Description:** Jointly developed enhancement of Z80 with various peripheral functions such as memory management (to reach larger, 1M-byte memory space), 2 DMA channels, 2 serial ports, and timers added on CMOS CPU chip. Z-suffix versions are totally compatible with Z80-family peripherals chips. Both Z- and R-suffix devices interface to the 6600 and Intel 80xx series buses.

**Status:** CMOS enhancements to the widely used Z80. Has on-chip memory-management unit (MMU), multiple DMA channels, and UART. These chips don’t have sophisticated big-computer features, such as separate MMU, multiple DMA channels, and UART. Both the Z180 and 64180’s MMUs translate between the Z80 64k-byte address space and their own 1M-byte space. These families have received a boost from all Z80 users and third-party supporters of the venerable Z80.

### HARDWARE CHARACTERISTICS

**SOFTWARE**

<table>
<thead>
<tr>
<th>I—DATA-MANIPULATION INSTRUCTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unsigned 8 x 8-bit = 16-bit multiply.</td>
</tr>
<tr>
<td>Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>II—DATA-MOVEMENT INSTRUCTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Immediately addressed locations.</td>
</tr>
<tr>
<td>Block output to I/O. Must set up MMU bank registers to translate between 64k bytes of Z80 and 512k bytes external.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>V—POWER-SAVING INSTRUCTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep command disconnects processor from clock. Interrupt or reset will reconnect.</td>
</tr>
</tbody>
</table>

**Specification summary:** Object-code compatible with Z80 (and 8080, 8085). Pipelined CPU. On-chip MMU generates 19 bits (512k-byte external physical address space) in the DIP package and 20 bits (1M-byte external) in surface-mount packages. 2-channel direct-memory-access controller, 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (Z-suffix versions are matched to Z80-family peripherals). CMOS versions provide 50 mW at 4-MHz operation; lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

**Hardware notes:***

1. Diagram is for basic core. Both Zilog and Hitachi are expanding upon this core.
2. The 64180x is a single-chip version of the 64180 and adds 16k bytes of one-time-programmable EPROM, 512 bytes of RAM, 54 I/O pins, a 16-bit timer, and a 6-channel analog comparator. It comes in 84-pin PLCCs, 80-pin flatpacks, and 90-pin shrink DIPs. Because of EPROM, Hitachi bills this style µC as a zero-turnaround-time part, saying it is cost-effective in volumes as great as 10k. Hitachi also sells the part in windowed 84-pin leadless chip carriers to aid development.

**Software notes:**

1. Only new instructions beyond Z80 instructions listed.
2. The MMU adds base registers to Z80 16-bit addresses to produce the 19-bit addresses needed externally.
3. Trap interrupt can be used both for catching undefined op codes and for letting users extend instruction set.

**HARDWARE SUPPORT**

**SOFTWARE**

**Microtec Research** (Santa Clara, CA) supplies macroassembler, utilities, Pascal, and C compilers (to run on IBM PC and DEC VAX hosts). Avocet (Rockport, ME) and Allen Ashley (Pasadena, CA) have announced IBM PC-based assemblers. Hitachi provides help so that the additional 64180 instructions can be treated as macros on a Z80 macroassembler. Boston Systems Office (Waltham, MA) offers a VAX-hosted assembler ($1200). Software compatible with CP/M (Digital Research) and MSX (Microsoft) operating systems (latter being result of project for Japanese market).

**American Automation** has cross software to go with development hardware (assembler, C compiler, and debugger). Archimedes (San Francisco, CA) offers a C compiler ($995 for IBM PC; $3995 for MicroVAX; and $7995 for VAX).
6800/6802, 6809/6309

AVAILABILITY: Now.
COST: As with other mature µPs, costs have dropped, in this case to a case prices might rise again.
SECOND SOURCE: Hitachi and SGS Thomson.

Description: The 8-bit 6800 CPU was the original part in the family named after it. That family has been broadened to include not only the 2-chip 6802/6846 and 6809 covered here but also the single-chip 6801, the low-end single-chip devices, and the 6804 and the 6805. Note, however, that new CPU members aren’t precisely compatible with the original 6800, especially at the low and high ends. Even the 6809 is only software compatible with the original 6800 at source-code level.

HARDWARE

<table>
<thead>
<tr>
<th>Part</th>
<th>Description</th>
<th>Clock speed (MHz)</th>
<th>ROM x(8)</th>
<th>RAM x(8)</th>
<th>Cost (100 qty)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6800</td>
<td>CPU needs 2-phase clock</td>
<td>1-2</td>
<td>—</td>
<td>—</td>
<td>$4-$5</td>
</tr>
<tr>
<td>6802</td>
<td>CPU clock &amp; RAM</td>
<td>1-2 (4-MHz ext)</td>
<td>128</td>
<td>—</td>
<td>$4-$5</td>
</tr>
<tr>
<td>6809</td>
<td>CPU</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>$5-$6</td>
</tr>
<tr>
<td>6309</td>
<td>CPU CMOS</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>$9.50</td>
</tr>
</tbody>
</table>

Hardware notes:
1. Diagram shows 6800 and 6802. The 6809 has another 16-bit index and a second “user” stack pointer, which make the 6809 more powerful than the 6800; these additional resources give the 6809 many more instructions. On simple benchmarks, the 6809 is 270% faster than the equivalent-speed 6800, programs in 42% fewer instructions, and uses efficiency of 16-bit addressing increases throughput. Instruction set has 59 mnemonics and 7 addressing selections for a total of 1464 instruction patterns. Instruct on stops µP until it gets go-ahead signal from interrupt line.

From Motorola: Emulators range from low-cost (hundreds of dollars) boards to HDS-300 system (about $5000) plus personality modules ($5000). Support systems and OEM boards available from Motorola Semiconductor Div, 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-6900 or (602) 438-3500.

From others: Tektronix and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola’s “Micromodule” 8-bit boards.

SOFTWARE

From Motorola: You can obtain software free for downloading over phone lines by calling (512) 440-3733. The basic assemblers and other tools are for IBM PC.

Two versions of Basic are available for the 6809: Basic-M and BasicO9. The latter is designed to be fast and to permit structured programming. A Pascal compiler diskette is available.

8-BIT NMOS AND CMOS

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000
For more information, Circle No. 387

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest µP families. Among its progeny are the 68000 family of CMOS µPs, the 6809 family of CMOS µPs, and the 6801, 6802, 68HC11, and 68HC12.

The 6800 is now old in a market that is rapidly changing, and is not recommended for new designs; we retain it in the directory for reference. But the newer 6802 and 6809 continue to be shipped in volume. For new designs, Motorola steers designers either upwards to the 16-bit µPs 68000 family (6808 has an 8-bit bus) or downwards to the 68HC11.

HARDWARE

CHARACTERISTICS

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

Arithmetic and logic.

Instructions to take advantage of two accumulators.

6809 has unsigned 8 x 8-bit multiply with 16-bit product.

II—DATA-MOVEMENT INSTRUCTIONS

Can reach the first 256 locations of memory with short instructions.

6800 can use four index registers for merging three source blocks into one destination block.

Can autoincrement and autodecrement by 1 or 2 directly and indirectly.

Page zero can be software relocated during program execution, effectively increasing its size.

Indexing uses the “true indexing” relationship between base and offset (0, 5, 16 bits) rather than the 6800 relationship.

Can utilize the user stack for Polish-notation operations or interpretative languages.

III—PROGRAM-MANIPULATION INSTR

Has PDP-11-type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM.

Does not have vectored interrupt but can achieve function with software or with 6828 priority interrupt controller.

6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs.

IV—PROGRAM-STATUS-MANIP INSTR

6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction.

V—POWER-SAVING INSTRUCTIONS

6309 has SYNC and CWA1 to put CMOS CPU in sleep mode. Sync instruction stops µP until it gets go-ahead signal from interrupt line.

Specification summary for 6800: Common-memory architecture with 16-bit (64-byte) memory space for instructions, data, and I/O; all data 8 bits wide. Instruction set patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 µsec. NMOS circuitry requires 5V supply, 500 mW; housed in 40-pin DIP. Versions with $5 to +125°C range also available.

Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upwardly compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing increases throughput. Instruction set has 59 mnemonics and 7 addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-independent operations executing in 1 µsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page-zero register is retained but can be software relocated anywhere in memory via programmable register. The chip requires one 5V supply. Two versions, each in 40-pin DIP.
To put VGA graphics on your motherboard, you need a cost-efficient, highly integrated, powerful solution that uses minimal board space. You need the new CL-GD5320 Enhanced VGA-Compatible Graphics Chip from Cirrus Logic.

Use it to incorporate full 16-bit or 8-bit VGA into low-cost personal computers. You only need two industry standard 256K x 4 DRAMs and as few as five other ICs. Whatever memory speed you select — 80ns, 100ns, or 120ns — you’ll get a complete VGA display system with greater performance than systems using a more expensive solution with 64K x 4 DRAMs.

You don’t sacrifice features. You get 16-bit and 8-bit support for the VGA graphics standard, and full, register-level backwards compatibility. For maximum performance, it has an 8/16-bit CPU interface, independent video and DRAM clocks, internal FIFOs, and page mode DRAM access. And it will interface to both analog (PS/2 and multi-sync) and TTL monitors.

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Call 1-800-952-6300. Ask for dept. LM22.
Stag's ZL30A offers total PLD programming support

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- Stand alone or remote control operation
- Comprehensive device library
- Handler interface capability to support DIP or PLCC/LCC devices
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- Compatible with CUPL* software compiler
- RS232C, IEEE-488 and handler control interface ports standard
- Expansion modules accommodate 40 pin DIP and a range of surface mounted devices
- Stringent in-program checks including continuity and connect tests are automatically performed to guarantee error free stand alone or handler operation
- Supports Test Vectors
- Turn Key handler interface kits
- Worldwide sales and service support.

Stag Microsystems, Inc.
1600 Wyatt Drive
Santa Clara, CA 95054
Tel: (800) 227-8836
Tel: (408) 988-1118

Headquarters:
Western Regional Office
Stag Microsystems, Inc.
3060 Wyatt Drive
Santa Clara, CA 95054

Eastern Regional Office
Stag Microsystems, Inc.
3 Northern Blvd., Ste. B1
Amherst, NH 03031

Tel: (800) 222-222-222
Tel: (603) 673-4386

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GAL is a trademark of the Lattice Corp.
CUPL is a trademark of Assured Technologies.
6502/6500X

AVAILABILITY: Now.
COST: WDC's CMOS prices range from $4 in lower speed, high volume to $31.35 for high speed, lower volume.
SECOND SOURCE: WDC created and licensed most of the CMOS designs. It has licensed Rockwell, California Micro Devices, NCR, ITT-Intermetall in West Germany, and about 20 other companies.
CORE: WDC has developed the semicustom 6502 core as NCR and others now use it. Many suppliers now specify it as part of their cell libraries.

Description: Original design team's goal was to achieve as much PDP-11-style addressing capability as would fit in an economical chip. Because of the µP's short 8-bit index registers, it is optimally suited only to applications requiring access of smaller blocks of memory, although it benchmarks ahead of most other 8-bit µPs with respect to its speed of execution of high-level languages, such as Basic and Pascal. New CMOS parts consume little power and have small economical die that gets still smaller with today's finer geometries. See 6500/1 for single-chip versions and 65SC16/802 for 16-bit internal version.

Notes on CMOS versions:
1. CMOS 65CX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
3. Decimal mode is automatically set off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
4. A BRK followed by interrupt is executed.
5. See instruction set for comments on new instructions.

HARDWARE

8-BIT NMOS AND CMOS

Originator of 6502 Commodore (Westchester, PA) no longer sells chips to the merchant market. WDC developed CMOS version.

Western Design Center Inc
2166 E Brown Rd
Mesa, AZ 85203
Phone (602) 962-4545
For more information, Circle No. 368

Status: The falling share of market for this µP appears to indicate that it has reached the end of its life cycle. However, the architecture lives on in the form of single-chip versions (see 6500/1 and especially the 50740 in this directory) and ASIC versions. Some of these have very large unit volumes, so the 6502 architecture may remain, by volume, the leading 8-bit architecture in the world.

Notes on CMOS versions:
1. CMOS 65CX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
3. Decimal mode is automatically set off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
4. A BRK followed by interrupt is executed.
5. See instruction set for comments on new instructions.

HARDWARE

CHARACTERISTICS

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

Arithmetic and logic. Decimal mode via control bit in status register. Can operate on locations in memory space, which can be either RAM or I/O ports. CMOS parts have bit manipulation.

II—DATA-MOVEMENT INSTRUCTIONS

True indexed addressing, although index offset is limited to 8 bits in 2 CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables. CMOS parts have indexed-absolute indirect and zero-page indirect.

III—PROGRAM-MANIPULATION INSTR

Conditional branches with signed relative addresses. Nonmaskable and/or maskable interrupt, depending on model. CMOS parts have branches on bit test. Stack pointer for implementing 256-byte LIFO in external RAM.

IV—PROGRAM-STATUS-MANIP INSTR

Push and pull status register from memory stack. Set and clear carry, decimal mode, and interrupt bits. 6502 and 6512 have external input to one status bit, useful for handshaking with peripherals.

V—POWER-SAVING INSTRUCTIONS

Wait and Stop on 65C02, respectively, stop processor and disconnect clock to lower power consumption. New operating voltage range of 1.2 to 5.25V with an IOP of 0.1 µA/kHz at 2.8V.

Specification summary: Common-memory architecture with instructions, data, and I/O in same 64k-byte space; 57 instructions (68 for CMOS). Many instructions provide choice of 13 PDP-11-type addressing modes (for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mA supply. Some CMOS parts can run at 8-MHz clock frequency (125 nsec/cycle). CMOS parts require 4 mA/MHz for operation and 10 µA for standby. Although it supplies the µPs in DIPs and PLCCs, WDC recommends using the 44-pin PLCC for higher performance and reliability.

SOFTWARE

From California Micro Devices: 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).
From NCR: Monitor for use in conjunction with emulator. Supports breakpoints, change memory and registers, software trace, and real-time execution.
From others: Because the 6500 has been so widely used, there are innumerable sources of software at different language levels: for example, Byte Works (Albuquerque, NM), S-C Software (Dallas, TX), Roger-Wagner Publishing (El Cajon, CA), and 2500 AD (Aurora, CO).
8086/8088

**AVAILABILITY:** Now.

**COST:** Under $10 (1000) for NMOS 8086/88, under $15 (1000) for CMOS 8086/88. Siemens' NMOS parts are under $4.50 (1000).

**SECOND SOURCE:** For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, and OKI.

**Description:** The 8086, 8088, and their low-power CMOS implementations (80C86/80C88) share a 16-bit internal architecture that has a software base of more than 10,000 DOS applications. The 8088 (used in the original IBM PC and its clones) has an 8-bit external data bus to allow the manufacture of lower cost systems with full 16-bit software capability.

---

**8/16-BIT NMOS AND CMOS**

**Intel Corp**

Embedded Controller Operation

5000 W Chandler Blvd

Chandler, AZ 85226

Phone (602) 961-8051

For more information, Circle No. 369

**Status:** Next to the 8080/Z80 family, the 8086 family has been the most successful µ.P family. Its most visible application has been in the IBM PC and its many clones.

---

**HARDWARE CHARACTERISTICS**

**SOFTWARE**

I—**DATA-MANIPULATION INSTRUCTIONS**

8-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.

Logicals.

Bit, byte, word, and block operations.

II—**DATA-MOVEMENT INSTRUCTIONS**

Addressing modes include literal, relative (to register and to segment), register, base-plus index, and base-relative indexed.

Use of segment registers: Programmer can, through software, set up four areas in memory with four segment registers—a program area, a stack area, and two data areas. These areas need not be full 64k bytes, and they can overlap. Programmer can alter the four area locations by modifying the segment-register contents.

III—**PROGRAM-MANIPULATION INSTR**

Has call, jump, and return instructions both inside program segments and to different segments. Intra-segment call and jump use self-relative displacement for position-independent code. Conditional jump upon Boolean functions of flags within ±128 bytes of instruction. Iteration control of loops, a repeat prefix for rapid iteration in hardware-repeated string operations.

**Note:** Jumps can occupy varying amounts of execution time, because with BIU's instruction prefetch, the program counter can be ahead of itself.

IV—**PROGRAM-STATUS-MANIP INSTR**

In addition to 8080/85 flags: overflow, interrupt enable, direction (for strings), and single-step trap flags.

**Specification summary for 8086/88:** 16-bit CPU that can reach 1 M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 µsec with 5-MHz clock (0.37 µsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry, requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch eight pins from minimum to maximum external system mode. Harris CMOS 8086 dissipates only 10 mA/MHz when running; clock can be stopped for 500 µA standby.

---

**HARDWARE SUPPORT SOFTWARE**

**From Intel:** iCE in-circuit emulator ($8495) supports 8086/8088 to 10 MHz. Emulators are hosted on IBM PC. All ICEs provide windowed, menu-driven, source-level display and µ.P debugging. Performance analysis tool (iPAT) consists of a hardware base unit; an interface to ICE, and host software for the IBM PC/XT and PC/AT. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 8086/8088.

From others: Because of popularity, family is widely supported by third-party universal development systems.
Panel of experts.

Brighter, sharper, clearer, and flicker-free. When it comes to displays for industrial and medical applications, see the experts: Fujitsu Component of America.

It didn't take much research to discover what computer users in heavy-duty industrial, medical, and mainframe environments want from their displays. A bright, reliable, and interference-free picture.

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Idea number one is the very first 16-gray scale AC-memory plasma display available anywhere. An easy design-in, it interfaces with a standard Paradise™ VGA card to provide 640 x 480 pixels of flicker-free, high contrast viewing in even the toughest EMI environments. And that holds true for over 50,000 hours of continuous operation.

Our big picture.

Our next bright idea was a 15” diagonal extended VGA display panel with 1024 x 768 pixels of bright, crystal clear image. Offering the same performance as our gray scale, it's also available with a standard AT-bus video controller, and TIGA™ compatibility.

Which brings us to our next idea: that choosing Fujitsu for your next design is one brilliant move. Our panel of technical experts can provide all the advice, design assistance, and support you need—every step of the way. Talk to an expert.

To find out how you can offer premium gray scale and extended VGA performance for a competitive price, call the experts at Fujitsu Component of America at 1-800-556-1234 (ask for ext. 238). Inside California, call 1-800-441-2345 and ask for ext. 238. It may be the brightest thing you'll ever do.

Product Selection Guide

<table>
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<th>Ports No.</th>
<th>Pixel/Format</th>
<th>Gray Scale</th>
<th>Screen Dia.</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPF8050HRUD-101</td>
<td>640 x 400</td>
<td>4</td>
<td>9”</td>
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<td>FPF8050HRUK</td>
<td>640 x 400</td>
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<td>10”</td>
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<td>FPF8050HFUGA*</td>
<td>640 x 400</td>
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<td>1024 x 768</td>
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<tr>
<td>FPF128102HRUF*</td>
<td>1024 x 816</td>
<td>1</td>
<td>18”</td>
</tr>
</tbody>
</table>

*Also available as a monitor.

Fujitsu Component of America, Inc.
3545 North First Street • San Jose, CA 95134-1804.

Every step of the way.®

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Z280

AVAILABILITY: Now.

COST: About $18 in large volumes.

SECOND SOURCE: None announced, but supplier claims it has strong interest from major European and Far East semiconductor houses.

CORE: Zilog is incorporating elements of Z280 in its megacell library, so it can rapidly put together new combinations. The company claims it can turn around a semicustom design using its megacells in a matter of days. However, it does not plan to offer ASIC tools to customers.

Description: Enhanced Z80 µP, upgraded to the point that it has most of the features of larger 16/32-bit machines. It has "privileged" system-control hardware and associated software for multitask, multitasking operating systems. It has memory management for virtual memory and incorporates cache to achieve high throughput with moderate-speed external memories.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000
For more information, Circle No. 370

Status: The Z280 became available in late 1987. Basically, the Z280 lets designers upgrade Z80-based PCs into multitask systems that have large virtual memories and, claims Zilog, high performance. Compared with other Z80 enhancements, such as the Zilog Z180/Hitachi 64180, the Z280 offers a greater performance edge. Zilog is also pushing the Z280 as an upgrade for dedicated systems using Z80s as embedded controllers.

Hardware notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. The integration not only lowers system cost, but provides a speed advantage: When all subsystems are on chip, the system speed automatically increases.

Software note: Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).
Well connected.

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Fujitsu Component of America, Inc.
3545 North First Street · San Jose, CA 95134-1804.

Every step of the way.™

EDN November 22, 1990
H8 FAMILY

AVAILABILITY: Now for production quantities of the H8/532. H8/520 is sampling.
COST: For 10 MHz, the H8/532 costs $18 (10,000) in masked ROM versions and $25 for one-time programmable versions.
SECOND SOURCE: None.
CORE: Hitachi considers the basic H8/500 CPU as a standard cell for building high-integration µPs and µCs.

Description: The H8/532 and H8/520 are the initial devices in the family. The 16-bit internal architecture will include various ROM and RAM sizes, as well as a mix of peripherals. All will be available in masked ROM and zero-turn-around-time, one-time programmable versions.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
43 arithmetic, logic, shift, and bit manipulation instructions. Includes 16-bit multiply and divide.

II—DATA-MOVEMENT INSTRUCTIONS
7 data transfer instructions with high orthogonality. You can independently specify addressing modes and data sizes in each instruction. Seven addressing modes: register direct, indirect, indirect with displacement, indirect with pre-decrement or post-increment; absolute, immediate, and program-counter relative. Five data types: bit, BCD, byte, word, and long word.

III—PROGRAM-MANIPULATION INSTR
11 branch instructions with 16 different conditions. Loop counter/condition code register termination.

IV—PROGRAM-STATUS-MANIP INSTR
7 control registers including 16-bit program counter and status register; 8-bit condition code register, as well as four 8-bit page registers used in maximum mode only.

V—POWER-SAVING INSTRUCTIONS
3 Power-saving modes: sleep instruction halts CPU; sleep with software standby bit in control register set halts CPU and clock—a nonmaskable interrupt or hardware reset resumes execution; if standby pin is held low, processor enters hardware standby mode—a hardware reset resumes execution.

Specification summary: The H8/532 is an integrated 8-bit µC. Among the onboard peripherals are 32k bits of ROM or EPROM, 1 k byte of RAM, 8 timers, 1 UART channel, 8 channels of 10-bit A/D conversion, 1 data transfer controller, 9 I/O ports, and glue logic that includes a clock generator and wait-state controller.

Hardware notes:
1. The H8/532 contains 32k bits of ROM and 1k bits of RAM. The chip offers a UART: three 16-bit free-run timers; an 8-bit timer; an 8-bit watchdog timer; an 8-channel, 10-bit ADC; and 3 external and 19 internal interrupts with 8 priority levels.
2. The H8/520 contains 16k bits of ROM and 512 bits of RAM. This chip features 2 UARTs. In addition to its two 16-bit free-run timers, the H8/520 offers both an 8-bit timer and a watchdog timer. This µC provides an ADC and interrupt structure like its sibling.

Software note:
Commonly used instructions have a short form: 1 byte shorter and executing 1 cycle faster than the corresponding long form.

HARDWARE SUPPORT SOFTWARE

Hitachi supplies a common base unit and personality modules for in-circuit emulation of all H-series devices (about $10,000). Evaluation boards (about $400) with in-line assembler and limited debug monitor are also available. Hewlett-Packard (Palo Alto, CA) and Sophia Systems (Palo Alto, CA) also offer development systems.

Hitachi supplies a complete development software chain including assembler, linker, loader, simulator, and C compiler for VAX and IBM PC hosts. Third-party vendors Microtec Research (Santa Clara, CA), Avocet (Rockport, ME), and Software Environments (Dallas, TX) also supply similar products.

EDN November 22, 1990
When it comes to custom keyboards for the next generation of desktop, laptop, and notebook PCs, nobody outscores Fujitsu for quality, durability, and touch.

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Of course, what makes our new keyboards the best choice is what has made our FKB4800 and FKB4700 keyboards the 101 standard—our attention to the extra details. Like our superior tactile feedback and reliability.

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78K SERIES

AVAILABILITY: Now.
COST: $5 - $10 (100,000).
SECOND SOURCE: None.

Description: The 78K Series is a family of 8/16-bit microcomputers with features for real-time applications. These µCs improve peripheral response and system speed while embedding intelligence in the peripherals and marrying the processor and peripherals through an interdevice data transfer facility.

HARDWARE CHARACTERISTICS SOFTWARE

HARDWARE

NEC Electronics provides an evaluation board with 32k bytes of RAM and ROM, an optional extended memory socket, and an RS-232C port. The Design kit includes a miniature-in-circuit emulator board and probe with 32k bytes of SRAM, a communications port, and an on-board monitor. The emulation kit includes ICE and probe.

SOFTWARE

In addition to support software for the development hardware, NEC provides a relocatable assembler, a structured assembler, and a C compiler.

NEC Electronics
401 Ellis St
Mountain View, CA 94043
Phone (415) 960-6000
For more information, Circle No. 372

Status: The K series of microcomputers is currently used in applications such as hard-disk drive control, audio, communication, and environmental control.
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*IndustryPack is a trademark of Greenspring Computers, Inc.
**65C816/65C802**

**AVAILABILITY:** Now.

**COST:** Prices range from about $4 to $32.

**SECOND SOURCE:** VLSI and California Micro Devices said to be main sources, but WDC says it has licensed others in US and abroad.

**CORE:** All suppliers are considering this as a µ.P megacell in their libraries.

**Description:** CMOS 8/16-bit µ.Ps featuring software compatibility with 6502/65C02. The -802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The -816 has a different pinout, but expands the addressing range of the 6502 from 64k to 16M bytes. Additional hardware enhancements on the -816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

**HARDWARE CHARACTERISTICS**

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<td>Western Design Center Inc</td>
<td>From Byte Works (Albuquerque, NM): The ORCA/M cross-assembly and utility package. C and Pascal compilers are also available.</td>
</tr>
<tr>
<td>II-DATA-MANEUVER INSTR</td>
<td>From Apple (Cupertino, CA): Assembler and debugger ($100) and C compiler.</td>
<td></td>
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<tr>
<td>II-PROGRAM-MANIPULATION INSTR</td>
<td>From others: Supporting products are also available from S-C Software (Dallas, TX); Roger-Wagner Publishing (El Cajon, CA); and 2500 AD (Aurora, CO).</td>
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**Hardware notes:**
1. Compare diagram with previous 650X family (see diagram pg 127) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits, and the 16-bit registers widened to 24 bits.
2. The -816’s control-bus outputs facilitate multiprocessing, caching, and virtual memory. The control-bus inputs let you abort instructions for virtual memory as well as control-bus access.

**Software notes:**
1. Upon reset, -802 and -816 are in 6502 emulation mode. To go to native (enhanced) mode, the E-bit must be reset to 0 via an exchange with previously reset carry-bit in status register.
2. Full-sized 16-bit registers may facilitate high-level-language compiler-writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help facilitate compiler writing. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Tendency of native (enhanced) mode coding to become trickier than 6502 due to tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

**Status:** Apple’s use of the 65C816 in the II/Gs upgrade provides a firm basis for hardware and software availability. Software support is growing as third-party houses that have supported the 6502-based Apple computers convert software to take advantage of the expanded memory and other capabilities of the 65C816.
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Not including CPU, DRAM, EPROM, and keyboard decoder.
80186/80188

AVAILABILITY: Now for 8-MHz 80186/188. Now for 10-, 12.5-, and 16-MHz 80C186/80C188. AMD will have 20-MHz part in fourth quarter 1990.

COST: Less than $10 (100) for 80186/188 in PLCC. Less than $18 for 10-MHz 80C186/C188 in PLCC.

SECOND SOURCE: AMD and Siemens.

CORE: Intel's ASIC group has incorporated the 80C186 in its cell library.

COST: Less than $10 (100) for 80186/188 in PLCC. Less than $18 for

AVAILABILITY: Now for 8-MHz 80186/188. Now for 10-, 12.5-, and 16-MHz 80C186/80C188. AMD will have 20-MHz part in fourth quarter 1990.

Description: The 80186, 80188, 80C186, and 80C188 are high-performance, highly integrated µPs. The 80186 family is completely upward compatible with 8086 object-code and contain 10 additional instructions. These embedded µPs integrate many common system components onto a single chip. The onboard peripherals include a clock generator, 2 independent DMA channels, a programmable interrupt controller, 3 programmable 16-bit timers, programmable memory, peripheral chip-select logic, and a programmable wait-state generator. Further enhancements to 80C186/C188 products include a fully static CMOS design, power-save mode, a DRAM-refresh control unit, a direct numerics interface, and a compatible mode.

Status: The 80C186 family of products is used in more than 3500 different customer applications.

Hardware notes:
1. Diagram is for 80C186.
2. The 80C186 is the 8-bit external-data-bus version of the 80C186. The 80C186 has all other 80C186 features except for the numerics interface.
3. The 80186 and 80188 do not have the DRAM-refresh control unit, power-save mode, or the direct numerics interface.
4. The 8087 math coprocessor supports the 80186/188; the 80C187 supports the 80186.

Software

From Intel: lICE186 in-circuit emulator ($10,618) supports 80186 to 10 MHz. ICE186 in-circuit emulator ($15,995) supports 80186/80C186 to 16 MHz. ICE188 ($8495) and ICE 188 ($9995) support 8-bit bus versions of the 80186 (80186/80C186). An evaluation board is also available ($400).

From others: The family is widely supported by third-party universal development systems.

Software

From Intel: Macroassembler, including linker, locator, mapper, and librarian. High-level-language compilers include PL/M, C, Fortran, and Pascal. iPAT performance analysis tool enables the analysis of real-time software execution in prototype systems. Analysis is performed symbolically, nonintrusively, and in real time with 100% sampling in the µP prototype environment.

From others: Because of a wide range of 8086- and 8088-based systems, in particular the IBM PC, there is third-party software of all sorts, enough to fill catalogs. Check with Intel and various trade journals.
Switching Regulator Allows Alkalines to Replace NiCads

Brian Huffman

In many applications it is desirable to substitute non-rechargeable batteries for chargeable types. This capability is necessary when the NiCads can’t be recharged or long charge times are unacceptable. Alkaline batteries are an excellent choice in this situation. They are readily available and have reasonable energy density. Compared to Alkalines, NiCads provide a more stable terminal voltage as they discharge. NiCads decay from 1.3V to 1.0V, while Alkalines drop from 1.5V to 0.8V. Replacing NiCads with Alkalines can cause unacceptable low supply voltage, although available energy is adequate. A boost type switching regulator obviates this problem, allowing Alkaline cells to replace NiCads. The circuit shown in Figure 1 accommodates the Alkaline cells widely varying terminal voltage while providing a constant output voltage.

This circuit is a step-up boost type switching regulator. It maintains a constant 6V output as battery voltage falls. The inductor accumulates energy from the battery when the LT1270 switch pin (VSW) switches to ground and dumps its stored energy to the output when the switch pin (VSW) goes off. The feedback pin (VFB) samples the output from the 6.19k-1.62k divider. The LT1270’s error amplifier compares the feedback pin voltage to its internal 1.24V reference and controls the VSW pin switching current, completing a control loop. The output voltage can be varied by changing the resistor divider ratio. The RC damper on the VC pin provides loop frequency compensation. The minimum start up voltage for this circuit is 3V. If a 3.3V start up voltage is permissible R1 and Q1 can be removed with Q2 replaced by a short.

**Figure 1. Low Voltage Circuit Provides Constant Output Voltage as Battery Discharges**

![Diagram of the circuit](image-url)
Bootstrapping the $V_{IN}$ pin off the output voltage allows the battery voltage to drop below the minimum start up voltage, while maintaining circuit operation. For example, with three C cells the battery voltage is initially 4.5V and operates down to 2.4V. With this bootstrapped technique the circuit provides a constant output voltage over the battery’s complete operating range, maximizing battery life.

Battery life characteristics are different for various cell types. Figure 2 compares battery life between AA, C, and D cells with a 6W load. In this application the power drain from the battery remains relatively constant. As the battery voltage decreases the battery current increases. The AA types discharge quicker than the C or D cells. They are physically smaller than the other cells, and therefore store less energy. The AA cells are 3 times smaller than the C cells and 6 times smaller than the D cells.

Current drain also influences cell life. Battery life significantly decreases at high current discharge. Slightly higher battery stack voltages permit surprising battery life increases. The higher voltage means lower current drain for a constant power load. Operating at just 33% less current the four C cells last 5 times longer than three C cells.

Battery life characteristics vary widely between manufacturers. Some manufacturers’ cells are optimized to operate more efficiently at lower current levels, making it wise to consult the battery manufacturer’s discharge characteristics.

Figure 3 shows Alkaline battery discharge characteristics for four D cells. A fresh cell measures 1.5V and operates down to 0.8V before the cell dies. The battery stack voltage drops quickly and then stabilizes until it reaches 3.2V; 0.8V per cell. There is no usable battery life beyond this point.

Figure 4 shows efficiency exceeding 85%. The diode and LT1270 switch are the two main loss elements. The Schottky diode introduces a relatively constant 7% loss, while the LT1270 switch loss varies with battery voltage. As battery voltage decreases, switch current and duty cycle increase. This has a dramatic effect on switch loss, because switch loss is proportional to the square of switch current multiplied by duty cycle. Therefore, at low input voltages efficiency is degraded because this loss is a higher percentage of the battery power drain.

If lower output current is desired, an LT1170, LT1171, or LT1172 can be used.
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**80286**

**AVAILABILITY:** Now for 8-, 10-, and 12.5-MHz devices. Now for 16- and 20-MHz versions from AMD and Harris. (Harris also offers a 25 MHz 80C286.) Now for CMOS 12.5-MHz 80C286.

**COST:** $10 (1000) for 8-MHz device; $13.50 (1000) for 12.5-MHz device. $30 (1000) for 12.5-MHz 80C286. Siemens charges $8, $12, and $21 (1000) for 8-, 12.5-, and 16-MHz devices, respectively.

**SECOND SOURCE:** AMD and Siemens. Harris for CMOS 80C286.

**Description:** The 80286 is upward compatible with the 8086 and 80188 and includes on-chip memory management and hardware support for multitasking, multitasking systems. A 4-level protection model provides task/task and user/operating-system protection. The 8-MHz 80286 is 8 times faster than the 5-MHz 8086 due to its pipelined architecture, 8-byte/sec bus and 3.5-nsec interrupt time. Used in the IBM PC/AT and its clones.

**Intel Corp**

3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

For more information, Circle No. 375

**Status:** Intel has de-emphasized the 80286 in favor of its 32-bit siblings, the 80386SX, 80386, and 80486. However, in spite of very low growth, the 80286 still has the highest volume in the 8086 family. Its popularity has been based on the IBM PC/AT. Since Intel has shown no inclination to let vendors second source the 80386, the 80286 should have a long life. Therefore, expect more enhanced 80286s, such as the 16- and 20-MHz versions from AMD and the CMOS version from Harris. Unfortunately for the second sources, the 80286's big sisters, the 80386SX, 80386, and 80486, are taking over many of its applications.

**HARDWARE CHARACTERISTICS SOFTWARE**

### I—DATA-MANIPULATION INSTRUCTIONS

8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.

Logical operations on bytes, words, and blocks.

### II—DATA-MOVEMENT INSTRUCTIONS

Addressing modes include literal, relative (to register and to segment), register, base plus index, base relative indexed, and register indirect.

Programmers can manipulate 16.383 segments in memory by means of memory-base descriptor tables and 4-segment registers. These segments can be between 1k and 64k bytes in length.

### III—PROGRAM-MANIPULATION INSTR

Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks.

Intragroup calls and jumps use self-relative displacement for position-independent code.

Intersegment calls and jumps use the memory-based descriptor tables to provide position independence of code.

Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.

Iteration control of loops.

String instructions, including repeat, for rapid iteration.

### IV—PROGRAM-STATUS-MANIP INSTR

8086 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible.

**Specification summary:** 16-bit CPU with 1G-byte virtual-address space per user, mapped onto 1M-byte physical-address space. Bus cycles execute in 250 nsec at 8-MHz clock frequency (200 nsec at 10 MHz), requiring 0.25 µsec for register-to-register moves at 8-MHz clock frequency, with 8-byte/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry in a large chip (335 x 339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has 2 operating modes: Real-address mode emulates 8086; protected virtual-address mode native to 80286.

Housed in a 68-pin Jedec type-A LCC, PLCC, and PGA.

**Hardware notes:**

1. Support chips for 80286: 82C828 clock, 82288 bus controller, 80287 floating-point numeric processor ($187.15 (1000) for 10-MHz version), and 82258 advanced DMA coprocessor.

2. High-integration chip sets for the IBM PC/AT are being offered by Chips and Technologies (San Jose, CA), Zymos (Sunnyvale, CA), VLSI Technology (Phoenix, AZ), Hudson & Supinger (Santa Clara, CA), Capital Equipment Corp (Burlington, MA), and Vis Technologies Inc (Sunnyvale, CA), as well as by Intel. These chips consolidate devices used around compute engines for the 80286.

**Software notes:**

1. Has high-level-language support instructions.

2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.

3. Trusted instructions can only be executed at highest protection levels.

From Intel: PICE-286 in-circuit emulator ($12,494) supports 80286 at 8 and 10 MHz. It is hosted on IBM PC/AT and PC/XT. ICE286 ($12,495) supports 80286 at 12.5 MHz. IPAT performance analysis tool includes a hardware base unit, an interface to the in-circuit emulator, and host software for the PC/AT and PC/XT. IPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 80286 in real and protected mode.

From others: A number of third-parties support the 80286 on their universal development systems.

**From Intel:** Macroassembler (ASM 286), which includes systems builder, binder, mapper, and librarian. Compilers for C, Pascal, PL/M, and Fortran. For applications running in virtual 8086 mode, any of Intel's 80286 software tools can be used. Hosts include PC-DOS and VAX/VMS. $750 for DOS version. Real-time operating systems (Intel's iRMX 286) available.

From others: Other operating systems and compilers being developed by third-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Coherent 286 (Mark Williams), Concurrent DOS (Digital Research), Unix System V (Digital Research), and OS/2 by Microsoft (Redmond, WA).

---

**Text continued on pg 147**
OrCAD has introduced the greatest product upgrade in its history. Memory limits, design restrictions, even boundaries between products are all disappearing.

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For more information, call (503) 690-9881

or write to OrCAD Sales Department, 3175 N.W. Aloclek Drive, Hillsboro, Oregon, 97124

CIRCLE NO. 104
A chip carrier socket that won't play "pop goes the circuit."

Our sockets are designed to get solidly into contact and stay in contact. No matter what the outside influences. Pop-out is simply not a problem.

Controlled contact interface angle in AMP HPT sockets ensures positive chip carrier retention. Our exclusive removable housing allows direct inspection of solder joints, and fast repair/replacement of contacts.

The contacts are High Pressure Tin, an AMP proprietary design which creates very high normal forces—a minimum of 200 grams per contact—for maximum retention and reliable interconnection. Short-signal-path contacts float in the housing to accommodate thermal expansion.

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Call the AMP Information Center at 1-800-522-6752 for literature on HPT PLCC Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

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Seven socket sizes are available, with carrier extraction tools provided for each size.
Choose from the widest selection of MOSFET predrivers in the industry. Whether your specification requires ultrafast low side driving, overcurrent protected high side driving, or overcurrent protected low side driving of 1 Amp to 100 Amp MOSFETs, we can supply the right product from our family of CMOS drivers to reliably meet your needs. For details contact: Micrel Semiconductor, 560 Oakmead Parkway, Sunnyvale, CA 94086. Or call (408) 245-2500.
MCS-96 FAMILY

AVAILABILITY: Now for 8096BH, 8097BH, 8097JF, and 8098.

COST: $5-$20.

SECOND SOURCE: None.

Description: Highly integrated 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes as much as 8k bytes of ROM/EPROM/OTP and 232 bytes of register-file. Also includes as much as 256 bytes of on-chip code RAM. I/O capabilities include an 8-channel, 10-bit ADC, full-duplex UART, 8-level priority interrupt, pulse-width-modulated output, high-speed I/O subsystem, four 16-bit software timers, as many as five 8-bit I/O ports, and 1 watchdog timer.

16-BIT NMOS AND CMOS

Intel Corp
Chandler Microcontroller and ASIC Div
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 376

Status: This earliest of the 16-bit µCs continues to maintain a large share of the 16-bit market. Intel has expanded the MCS-96 family to suit various segments of the market.

HARDWARE CHARACTERISTICS SOFTWARE

Hardware notes:
1. The NMOS MCS-96 family consists of parts available with A/D converter, 8- or 16-bit external bus. On-chip memory alternatives include ROM, EPROM, and one-time programmable versions. Packaging options include 68-pin PLCCs, 64-pin shrink DIPs, 48-pin DIPs, and 68-pin PGAs.
2. I/O subsystem has 4 high-speed capture inputs and 6 high-speed pulse outputs. Storage in 8-deep FIFO (inputs) and content addressable memory (outputs).
3. 16-bit watchdog timer allows recovery from hardware or software error.

1—DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide.
Logicals.
Bit, byte, word, and double-word operations.

II—DATA-MOVEMENT INSTRUCTIONS
Addressing modes include direct, immediate, indexed, indirect, and indirect with coartainment.
Load and store, push and pop.

III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns.
Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.
Iteration control of loops.

IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, and sticky bit (records previous value of carry during right shifts).
Can set and clear some bits.

Specification summary: 16-bit µC with split-memory architecture; 8k-byte ROM and 232 bytes of register-file RAM on chip. External memory expandable to 64k bytes, with data-bus dynamically programmable as 8 or 16 bits. Register-to-register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter; four 16-bit software timers; PWM output; five 8-bit I/O ports; full-duplex serial port; and high-speed pulse I/O ports. 16 x 16-bit multiply as fast as 1.75 µsec and 32/16-bit divide as fast as 3 µsec. In 48-pin DIP, 68-pin PLCC, or 68-pin PGA.

HARDWARE SUPPORT SOFTWARE

Programming support for EPROM versions supplied through Intel's line of universal PROM programmers as well as third-party programs from companies such as Data I/O, Stag, and Elan.

From Intel: Macroassembler (ASM-96), PL/M-96, and C-96 compilers. PL/M and C compilers supply hardware-control features such as interrupts. Each software package includes relocation/linkage utility (RL-96); library management utility (LIB-96); object-to-hex conversion utility (OH-96); and FPAL-96, a 32-bit floating-point utility. Software packages run on IBM PCs and compatible computers. $750 for a single-user license.

From Archimedes (San Francisco, CA): ANSI C-8096 compiler with additional features, such as control of Interrupt. Hosted on IBM PC ($995), MicroVAX ($3995), and VAX ($5995).

From Cybernetic Micro Systems (San Gregorio, CA): Graphics programming and simulation aids, which run on IBM PCs ($295 and $995, respectively).
HPC16000 FAMILY

**AVAILABILITY:** Now for 20- and 30-MHz parts.

**COST:** $5 to $25 in volume.

**SECOND SOURCE:** None.

**CORE:** The HPC family is core based. National says the family of standard parts is continuously growing.

**30-MHz versions.** The 30-MHz part’s shortest instructions are just 134 clock. Due to shrinking, new HPC16083 is offered in both 20-MHz and 30-MHz versions. The 30-MHz part’s shortest instructions are just 134 nsec over -55 to +125°C.

**AVAILABILITY:** Now for 20- and 30-MHz parts.

**HARDWARE CHARACTERISTICS SOFTWARE**

I—DATA-MANIPULATION INSTRUCTIONS

8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results.

Logical AND, OR, XOR, and compares.

Bit manipulation of all registers and through all 64k address space.

II—DATA-MOVEMENT INSTRUCTIONS

10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip.

Instructions include load, store, push, pop, and exchange.

III—PROGRAM-MANIPULATION INSTR

calls, jumps, returns, and conditional jumps implementing high-level-type constructs.

IV—PROGRAM-STATUS-MANIP INSTR

There is a carry-bit and several status registers. They may be manipulated as all bits in register space, and in 64k address space, they may be set, reset, and tested.

**Specification summary:** 16-bit CMOS µC and µP with memory-mapped architecture. External expandable memory. 16-bit-wide architecture includes data bus, ALU, and registers. Has 8 programmable 16-bit timers, 8 vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, 4 input-capture registers, 52 general-purpose I/O lines. Supply range is 4 to 5.5V. Available in industrial (-40 to +85°C) and extended (-55 to +125°C) temperature ranges (MIL-STD-883 now). In 68-pin plastic package.

<table>
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<tr>
<th>Commercial version</th>
<th>Industrial version</th>
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<th>RAM</th>
<th>I/O pins</th>
<th>Timer base counters</th>
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<tr>
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<td>HPC36003</td>
<td>ROMfess</td>
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<td>52</td>
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<td>8 input capture registers</td>
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</tr>
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<tr>
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<td>HPC36164</td>
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<td>52</td>
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<td>8 input capture registers and 8-channel ADC</td>
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<tr>
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<td>HPC36400</td>
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<tr>
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<td>256</td>
<td>56</td>
<td>4</td>
<td>HDLC &amp; DDA</td>
</tr>
<tr>
<td>HPC467164*</td>
<td>HPC367164</td>
<td>16.0k</td>
<td>512</td>
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<td>8</td>
<td>EPROM &amp; one-time-programmable device</td>
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<td>HPC46063MH</td>
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<td>80k</td>
<td>256</td>
<td>8</td>
<td>EPROM</td>
</tr>
</tbody>
</table>

**Hardware notes:**

1. Family is designed around common µP core for instruction-set consistency, with different models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are ADCs, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPROMs.

2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (ADCs, display drivers, EEPROM), COP5 4-bit µCs, 8050 8-bit µCs, and other HPCs for multiprocessing.

3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity, such as infinite loops.

4. Halt and idle modes provide additional power savings by stopping clock or disconnecting it.

5. Emulator parts are available for the HPC family.

6. HPC16083 and HPC16003 are MIL-883 and DESC-qualified.

**A designer's kit is available for less than $500. Supplier's HPC development system costs approximately $7000 for the HPC family. A high-end development system will be available from Hewlett-Packard as part of the HPC64700 in 1990. Both development systems can be used in conjunction with various hosts like IBM PC/ATs or HP9000 Series 300s. Dial-A-Helper is a 24-hr, on-line computer bulletin board service by National. It provides the latest information on all National µC chips (including development systems) and also specific application support. Call (408) 739-5582 for more information.**

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000
For more information, Circle No. 377

Status: HPC is a family of industrial controllers. Supplier's benchmarks (August '86 with HPC at 17 MHz) indicate that HPCs out perform other similar 8- and 16-bit controllers, such as Intel 8096, Motorola 68HC11, and 1370 on both throughput and ROM-program efficiency. NEC 78XXX and Zilog Super Z8 weren't mentioned. Dataquest numbers show the HPC as the largest selling 16-bit CMOS µC.

**SUPPORT**

Cross-assembler and C compiler to run on IBM PC. VAX (Unix/VMS) support is available, as is a symbolic debugger. Floating-point math and general math packages are currently available. Extensive application software is available for ISDN and SCSI.
Deep-seated quirks hidden within your complex designs. They can drive you crazy. Delay product time-to-market. And strain your design budget. But there is a solution.

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**80C166**

**Availability:** Now.

**Cost:** $25 (10,000)

**Second Source:** SGS-Thomson.

**Description:** The 80C166/83C166 is a 16-bit microcontroller for real-time applications. It uses a pipelined architecture and performs 8-, 16-, and 32-bit arithmetic and bit, byte, and word manipulations. You can freely allocate, within the internal RAM, any number of register banks with as many as 16 general-purpose registers. An interrupt controller with a peripheral event controller provides fast response to external events.

**Siemens Components Inc**

Integrated Circuits Div

2191 Laurelwood Rd

Santa Clara, CA 95054

Phone (408) 980-4518

For more information, Circle No. 378

**Status:** Siemens claims its 16-bit modular design works well in automotive, industrial-control, and data communications applications. The 80C166 uses the vendor's experience with highly integrated derivatives of the 8051. Changing peripheral modules and on-chip RAM and ROM sizes to suit particular applications will help the family grow.

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**HARDWARE CHARACTERISTICS SOFTWARE**

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**V—DATA-MANIPULATION INSTRUCTIONS**

- 8-, 16-, and 32-bit signed and unsigned arithmetic instructions including fast multiply and divide. Multiple-bit shift and rotate in one machine cycle. Direct bit-to-bit manipulation in internal RAM. Various loop-control instructions.

**II—DATA-MOVEMENT INSTRUCTIONS**

- Move instructions of byte or word in direct, immediate, indexed, and indirect with auto increment or decrement addressing modes. Flexible byte-to-word movements, system stack and user stack instructions.

**III—PROGRAM-MANIPULATION INCSR**

- Intersegment and intrasegment calls and jumps. Conditional jumps on 16 different conditions (including semaphoresupport). Software traps.

**IV—PROGRAM-STATUS-MANIP INSTR**

- You can change the current CPU priority to mask reactions on interrupts of lower priority. Hardware traps are issued on detected errors. A system-configuration register allows adjustment of the µP to various system requirements.

**Specification summary:** Single-chip microcontroller with external bus interface, as much as 32kb of ROM or flash EPROM, and 1k byte of RAM. Selectable 8- or 16-bit external data bus with programmable wait states or ready function. Chip uses 40-MHz crystal to run at 20 MHz. Most instructions execute in one machine cycle. Interrupt response takes 3 to 5 cycles. You can allocate 32 interrupt sources to 16 priority levels. The peripheral event controller steals cycles to implement fast, asynchronous data transmissions. The capture/compare unit consists of two 16-bit timers with 400-nsec resolution. A general-purpose timer unit contains three 16-bit up/down timer/counters with 400-nsec resolution. Another general-purpose timer unit offers two 16-bit up/down timer/counters with 200-nsec resolution. The 80C166 provides 76 I/O lines in four 16-bit bidirectional ports, one 2-bit bidirectional port, and a 10-bit input port. Two USART channels provide 625k-baud serial communication. An onboard ADC provides 10-bit resolution and 15-µsec conversion time.

**Hardware notes:**

1. The peripheral event controller services peripherals independent from the CPU. This controller module acts as an interrupt-driven DMA function between the CPU and peripherals.
2. The 80C166 is a task-oriented machine. The programmable interrupt priorities, a number of hardware and software traps, fast interrupt response time, and programmable register-bank allocation allow fast task switches.

---

**HARDWARE SUPPORT SOFTWARE**

---

Siemens supplies an 80C166 evaluation board with monitor and an emulator based on a bond-out chip. The board uses the IBM PC as a host.

**From Siemens:** A development package that includes a macro assembler, linker, locator, and library. A C compiler for ANSI standard C with additional support for 80C166-specific features. A software simulator that can simulate on-chip peripherals and an interrupt system allows debugging and software development. All software tools are IBM PC-based and are currently available.

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**EDN November 22, 1990**

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**RTX 2000**

**AVAILABILITY:** The RTX 2000-8 (8 MHz), the RTX 2000-10 (10 MHz), and the RTX 2001A-8 and -10 are available now in 84-pin PGA and PLCC packages. Military grades are also available.

**COST:** In 100-piece quantities: The 8-MHz RTX 2000 starts at $99, the 10-MHz version starts at $129, the 8-MHz RTX 2001A starts at $49, and the 10-MHz RTX 2001A starts at $76.

**SECOND SOURCE:** Zoran Corp (Santa Clara, CA).

**CORE:** Available in the Harris’s advanced standard-cell and compiler library.

**Description:** The RTX 2000 is a high-performance 16-bit μP with on-chip timers, an interrupt controller, a multiplier, and two 256-word stacks. The manufacturer claims that the chip offers a sustained performance greater than 10 MIPS because each instruction requires only one clock cycle for execution. The chip’s architecture lets designers add hardware accelerators and I/O devices that extend the chip’s basic structure. The CMOS RTX 2000 operates between dc and the maximum clock rate. Power consumption is typically 5 mA/MHz.

---

**16-BIT CMOS**

**HARDWARE**

1. Diagram shows basic RTX 2000 architecture. The 2001A is a smaller version that lacks the hardware multiplier.
2. The ASIC-bus interface lets designers extend the chip’s basic architecture with peripheral and I/O devices.

---

**SOFTWARE**

1. **DATA-MANIPULATION INSTRUCTIONS** Full set of math and logic instructions, which includes a single-cycle 16 × 16-bit multiplication operation as well as division and square-root operations. The architecture allows 16- and 32-bit shifts. You can directly manipulate the top element of either the return or the parameter stack.
2. **DATA-MOVEMENT INSTRUCTIONS** Access memory as bytes or words. Memory-to-stack or stack-to-memory operations require two cycles. Combine memory or I/O operations with ALU operations. Access memory in LSB-MSB or MSB-LSB order. “Streamed” memory access with automatic address update. Access to 1 M byte of memory space through page register.
3. **PROGRAM-MANIPULATION INSTR** Intrapage calls require one cycle; interpage calls take three cycles. Return operations require either zero or one cycle. Single-cycle conditional or unconditional branch operations. Conditional branches depend on the top-of-stack or on the index registers. Single-level software interrupt.
4. **PROGRAM-STATUS-MANIP INSTR** Flags include interrupt enable, interrupt pending, carry, complex carry, byte order, and boot. Automatic interrupt enable on return-from-interrupt operation.

**Specification summary:** 16-bit CPU with 1M-byte address space. Bus cycles execute in 100 nsec with a 10-MHz clock. All instructions execute in 1 or 2 cycles, and the memory bus is active during every cycle. Additional I/O bus for high-speed transfer operations occurring simultaneously with memory-access and processing operations. The architecture includes two 64-word stacks, both of which may be active when memory- and I/O-transfer operations take place. Harris claims a peak data-transfer rate of 80 bytes/sec. On-chip peripheral devices include three counter/timer units and a 16-bit multiplier. The 107,000 mips RTX 2000 and 80,000 mips RTX 2001A are housed in an 84-pin PGA or an 84-pin PLCC package.

**Software notes:**
1. The RTX 2000 directly executes Forth statements; consequently, no assembly language exists for this processor.
2. Harris claims that the stack architecture is flexible enough to enable the chip to efficiently run many popular computer languages. The chip contains a parameter and a return stack.

---

**HARDSWARE SUPPORT SOFTWARE**

**HARRIS SEMICONDUCTOR**

Box 863
Melbourne, FL 32902
Phone (407) 724-3800
For more information, Circle No. 379

**SECOND SOURCE:** Zoran Corp (Santa Clara, CA).

**从其他:** The MicroProcessor Engineering (Southampton, UK; US agency is AMICS Enterprises, Rochester, NY) Power Board is a standalone unit that furnishes a variety of I/O ports and 500k bytes of RAM. VME Inc (Milpitas, CA) offers VMEbus development systems and standalone boards based on the RTX. Silicon Composers (Palo Alto, CA) also offers a variety of systems. **From Harris:** The Real-Time Express Development System (10 MHz, RTXDS-10; $2995) runs from within an IBM PC or compatible. Harris also offers 8- and 10-MHz development boards (from $1495) for those who want to test their own development software.

**From others:** The MicroProcessor Engineering (Southampton, UK; US agency is AMICS Enterprises, Rochester, NY) offers VMEbus development systems and standalone boards based on the RTX. Silicon Composers (Palo Alto, CA) also offers a variety of systems.

**从其他:** Laboratory Microsystems (Marina del Rey, CA), Forth Inc (Manhattan Beach, CA), and others have software packages for the RTX 2000 μP. MicroProcessor Engineering’s Power Forth for its development board is an extended Forth-83 development environment.

**硬件:**
1. 电路图显示基本RTX 2000架构。2001A是一个较小的版本，但缺少硬件乘法器。
2. ASIC总线接口让设计者可以将外围设备和I/O设备扩展到芯片的基本结构上。

**软件:**
1. **数据操作指令** 包括单周期16×16位的乘法运算，以及除法和平方根运算。架构支持16-和32位的位移。可以直接操作返回堆栈或参数堆栈的顶部。
2. **数据移动指令** 访问内存作为字节或字。堆栈到内存或内存到堆栈的操作需要两周期。可以组合内存或I/O操作与算术运算。
3. **程序操作指令** 页内调用需要一个周期；页间调用需要三个周期。返回操作需要零到一个周期。
4. **程序状态操作指令** 标志包括中断使能、中断pending、进位、复杂进位、字节顺序和预定。

**规格摘要:** 16位CPU，1M字节地址空间。总线周期以100 nsec执行，时钟速度为10 MHz。所有指令以1或2个周期执行，内存总线在每个周期活跃。额外的I/O总线用于高速传输操作，同时进行内存访问和处理操作。架构包括两个64字的栈，只需一个或两个周期。数据传输率峰值为80字节/秒。内置的外围设备包括三个计数/定时器单元和一个16位乘法器。107,000 MIPS的RTX 2000和80,000 MIPS的RTX 2001A被封装在84引脚PGA或84引脚PLCC包中。

**软件注意事项:**
1. RTX 2000直接执行Forth语句；因此，不需要汇编语言此处理器。
2. Harris声称栈架构灵活，足以使芯片有效地运行许多流行的计算机语言。芯片包含一个参数和返回堆栈。
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FOR EMBEDDED SYSTEMS PROGRAMMERS. Our C compilers, Modula-2 Compilers,
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corporations and savvy independent consultants from San Francisco to
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of processors, on an even wider range of host systems. This
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FROM THE WORLD LEADER IN DIGITAL MULTIMETERS

FLUKE
TRANSPUTER FAMILY

AVAILABILITY: Now for 20-, 25-, and 30-MHz parts in PGAs, PLCCs, and POFPs.
COST: In 100 qty PGAs: T222, $57; T400, $84; T425, $167; T800, $278; T801, $334.
SECOND SOURCE: None, but also manufactured at parent company SGS-Thomson’s Carrollton, TX, fabrication plant.

Description: The Transputer family is a range of software-compatible 16- and 32-bit µPs. Each part has a CPU, on-chip SRAM (2k or 4k bits), timers, external memory interface, and 2 or 4 serial links. The links are 20M-bps DMA channels for communications and building multiprocessor systems. The serial links are DMA channels into the Transputer memory system and allow software processes to run on independent Transputers and communicate directly via the links. T8xx devices have an on-chip 64-bit FPU.

HARDWARE

I—DATA-MANIPULATION INSTRUCTIONS

Integer arithmetic, including multiply and divide. Logicals, shifts, and comparisons. T800 has on-chip IEEE floating-point add and subtract, multiply and divide, and square root, both 32 and 64 bits.

II—DATA-MOVEMENT INSTRUCTIONS

Memory-bandwidth block moves, 2-dimensional block moves for graphics bitblt. Load/store of local variables done relative to workspace pointer. Indexed load/stores available from address in A register. Immediate loads done 4 bits at a time. Large immediate values loadable from tables, instruction stream, or a sequence of special instructions.

III—PROGRAM-MANIPULATION INSTR


IV—PROGRAM-STATUS-MANIP INSTR

Error flag detects overflow. Test, set, clear, stop-on-error instructions. One error flag per task priority level. Instructions for checking array bounds.

Specification summary: Family of 16- and 32-bit µPs designed for multiprocessing. Unique in that they have the hardware and software links that allow them to be hooked to each other for parallel processing. Four full-duplex, 20M-bps serial links driven by on-chip, 8-channel DMA provide basic multiprocessor communication links as well as I/O. One 5-MHz external clock generates 20-MHz chip clocks, giving 50-nsec instruction cycle. Submicrosecond interrupt latency, procedure call, and task switch. Most instructions take 1 or 2 cycles. Integer multiply takes 38 cycles; divide takes 39 cycles (less than 2 µsec). Single-precision floating-point add takes 7 cycles (350 nsec), floating-point multiply takes 11 to 18 cycles (550 to 900 nsec), and floating-point divide takes 16 to 28 cycles (800 to 1400 nsec).

Hardware notes:
1. Diagram is for T425. T800 is the same but adds an FPU. T801 is the same as the T800 except that the external memory interface is a nonmultiplexed data/address bus instead of the T800 multiplexed bus. T222 is the same as the T800 except that it has a 16-bit internal architecture and the FPU has been removed. The T400 is a low-cost variant with 2 links and 2k bits of on-chip memory.
2. Unlike most 32-bit machines, there is no group of general-purpose registers. Instead, substantial on-chip RAM plays equivalent role.
3. ALU fed from 3 accumulators forming a small 3-deep stack, allowing compact implied addressing.
4. The four serial links allow arrays of Transputers in multiprocessing with no bus saturation, which is the reason speed increase is said to be linear when more µPs are added.

Software notes:
1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack.
2. Two priority-ordered process queues are each supported by front and back registers, indicating a linked list of processes ready to run. Event-based multitasking is fully supported by a real-time kernel in microcode.
3. Supplier’s Occam language said to facilitate programming multiple Transputer systems, but programmer must still study how best to partition task. Third parties have announced extensions to C to accomplish same ends.

SOUTH

SOFTWARE

Inmos supplies compilers for hosts such as IBM PC, VAX (VMS), and Sun systems. ANSI C, Fortran, Pascal, and Occam are the languages that Inmos supports. Available software-debugging tools include network debugger, breakpoint, and trace facilities. Third-party vendors support Ada, Modula 2, and Prolog, and operating system environments such as Heios, Linda, and Transldris.

EDN November 22, 1990 155
Z8000/Z16C00

**AVAILABILITY:** Now for NMOS Z8000 at 6 and 10 MHz. Now for CMOS Z16C00 at 10 MHz; 16-MHz version will be available late in 1990.

**COST:** $4.72 (10k) for Z8000 in PLCC package.

**SECOND SOURCE:** SGS-Thomson, and Sharp for Z8000.

**CORE:** Zilog has both Z8000 and Z16C00 as cores in its in-house ASIC library and plans to use Zbus for its systems on silicon. The company says that 160 x 160-mil Z8000 core is small enough to leave room for other functions on practical 400 x 400-mil ASIC.

**Description:** One of the first µPs to have architectural features of a modern microcomputer. Original 16-bit Z8000 comes in 40-pin package for addressing 64k-byte memory or in 48-pin package for addressing 8M-byte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit µP, offering best CPU speed, interrupt handling, character-string search, and block moves.

**HARDWARE CHARACTERISTICS SOFTWARE**

- **CLOCK:**
  - Osc 10 MHz
  - Ci
  - ~w~
  - !)
  - w
  - (J

- **SEGMENT POINTERS**

- **ADDRESS BUS (24)**

- **Hardware notes:**
  - Supplier has companion peripherals suitable for both processors: For Z8000, a range of DMA, FIFO, data ciphering (NBS), communications, and counter/timer parts.
  - For Z16C00, a system general logic unit—16C20—contains memory support, DMA, interrupts, and I/O. For 16C01, a CMOS dual MMU80210 addresses 128 segments compatible with the 8010 NMOS MMU.

**TEXT CONTINUED ON PG 161**

16/32-BIT NMOS AND CMOS

**Zilog Inc**

210 Hacienda Ave

Campbell, CA 95008

Phone (408) 370-8000

For more information, Circle No. 381

**Status:** The Z8000 has found most acceptance in real-time control applications, particularly military, according to Zilog. The company has added the Z16C00 16-bit CMOS microcomputer to the family for real-time embedded control applications. The company is licensing its 16-bit core for customer applications.

**HARDWARE SUPPORT SOFTWARE**

- **I—DATA-MANIPULATION INSTRUCTIONS**
  - Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed). Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n). Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulator.

- **II—DATA-MOVEMENT INSTRUCTIONS**
  - Eight addressing modes using general-purpose registers as indexers and stack pointers.
  - Comprehensive set of block-transfer and string-manipulation macroequivalents, including many dedicated to I/O space.

- **III—PROGRAM-MANIPULATION INSTR**
  - Call and call relative (± 4096 bytes).
  - System call using special system stack pointer.

- **IV—PROGRAM-STATUS-MANIP INSTR**
  - Set and reset flags, complement flags. Set-multiple-interrupt modes.
  - Tests for the micro-in and micro-out lines for multiple-microprocessor configurations.

**SPECIFICATION SUMMARY:**

- Common-memory architecture with optional separate I/O space and separate systems stack. Z8000 is 16-bit µP that has directly addressable memory space of 8M bytes (8001) using segment pointers, expandable to 48M bytes using the six available memory spaces and an MMU. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 µsec through 1 or 2 µsec to 7 µsec for 16-bit multiply, all at 10-MHz system clock (6 MHz also available). Eight large-computer-style addressing modes. NMOS, requiring one 5V supply (plus substrate-decoupling capacitor), in either 40- or 48-pin package. Z16C00 is a CMOS compatible version of Z8000 and can run same software.
Emulation power without compromise

**Power in selection**—System support for more processors than any other manufacturer in the world. Power in product range to match your needs—from economical basic configurations to fully featured systems.

**Power in performance**—Completely integrated capabilities include options such as versatile trace, performance analysis, EPROM programming, C source level debugging, over 100 personality modules with a common universal platform for different processors, C cross compilers, cross assemblers and more.

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Thanks to embedded lithium energy cells and low power consumption — about 250 nanoamps — Dallas timekeepers run for over 10 years with no external power.

There is no lithium consumption as long as system power is present. So assuming your equipment is occasionally turned on, the clock will run darn near forever.

And just to make sure you get every minute you've got coming, a freshness seal extends life by preventing lithium consumption until the equipment is first powered up.

Choose Your Interface

Recognizing that different designs need different approaches, we make clocks with four interfaces. If you didn’t know you needed an interface until after the fact, try our phantom. The phantom interface fits into existing circuitry and is invoked with software; it appears and disappears on command. So it won’t interfere with whatever else has to go on.

If you need the timer to mimic memory and sit on the memory bus, try our byte-wide interface, which fits into a memory socket. If you need an interface for a PC/AT/OS2 or EISA, we have a PC interface. And, of course, we offer a serial interface.

Now Pick Your Options

Have a look at our menu of selections.

Vital Memory

Many of our clocks provide what we call “vital memory,” special nonvolatile RAM that stores information essential to the operation of the equipment.

Such as setup or configuration data to get the system going after a power failure. Or information that helps you keep track of computers and components. Like serial...
number, password, type of add-in boards, or field service warranty information.

You can choose the amount of vital memory you need — from 50 bytes to 32K bytes.

**Watchdog Timer**

Some clocks have watchdog timers that restart the system when the microprocessor is out of control. Your system can wake up or go to sleep thanks to programmable alarms. You can even set an alarm to go off on important dates — like January 1, 2000.

**Easy Retrofit**

Your systems are already designed and built? No problem. Some of our clocks retrofit to existing designs. They sneak in under an EPROM or a RAM — no changes to hardware required.

So if you need time, there isn’t a better number to call.

---

### Timekeepers

<table>
<thead>
<tr>
<th>Product Name and Number</th>
<th>Type of Interface</th>
<th>NV SRAM Bytes</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Time Clock</td>
<td>Multiplexed</td>
<td>50</td>
<td>Replaces MC 146818A; MS-DOS compatible; programmable interrupts; square wave output. Meets MCA and EISA NV RAM requirements.</td>
</tr>
<tr>
<td>RAMified Real Time Clock</td>
<td>Bytewide Data/ Address Bus</td>
<td>4K/8K</td>
<td>See above, plus power monitor and cold starts computer from keyboard.</td>
</tr>
<tr>
<td>CPU Supervisory Stk</td>
<td>Conventional</td>
<td>8K/32K</td>
<td>CPU watchdog; programmable interrupts; square wave output; wake up interrupts.</td>
</tr>
<tr>
<td>Watchdog Timekeeper</td>
<td>Conventional</td>
<td>50</td>
<td>See above, plus power monitor and cold starts computer from keyboard.</td>
</tr>
<tr>
<td>RAMified Timekeeper</td>
<td></td>
<td>32K</td>
<td>Timekeeper built into a socket: mated SRAM converts to NV RAM.</td>
</tr>
<tr>
<td>CPU Supervisory Stk</td>
<td></td>
<td>8K</td>
<td>NV SRAM packaged with timekeeper.</td>
</tr>
</tbody>
</table>

### Chips

<table>
<thead>
<tr>
<th>Product Name and Number</th>
<th>Type of Interface</th>
<th>NV SRAM Bytes</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Time Clock Chip</td>
<td>Multiplexed</td>
<td>50</td>
<td>Replaces MC 146818A; MS-DOS compatible; programmable interrupts; square wave output. Meets MCA and EISA NV RAM requirements.</td>
</tr>
<tr>
<td>RAMified Real Time Clock</td>
<td>Bytewide Data/ Address Bus</td>
<td>4K/8K</td>
<td>Programmable interrupts; square wave output. Controller provides battery backup circuitry for SRAM.</td>
</tr>
<tr>
<td>Watchdog Timekeeper Chip</td>
<td>Conventional</td>
<td>50</td>
<td>Programmable interrupts; square wave output. Controller provides battery backup circuitry for SRAM.</td>
</tr>
<tr>
<td>Phantom Time Chip</td>
<td></td>
<td>2.0 to 5.5 volt operation: serial I/O for minimum pin count.</td>
<td></td>
</tr>
<tr>
<td>Serial Timekeeper Chip</td>
<td>3-Wire Serial</td>
<td>24</td>
<td>Battery backup circuitry for SRAM. Add-in real time clock uses same SRAM/EPROM signals.</td>
</tr>
</tbody>
</table>

---

The DS1386 RAMified Timekeeper guards against computer malfunction and mimics bytewide static RAM; it comes with 32K bytes of NV SRAM.

The DS1216 SmartWatch socket sandwiches between an EPROM and the printed circuit board and keeps perpetual time.

EDN November 22, 1990
A new and revealing look at HOLMBERG™ D-subminiature connectors.

Quality HOLMBERG™ connectors are now part of the Thomas & Betts product line. We show an X-ray view of one of the HOLMBERG™ D-subminiature connectors to emphasize that it's what's beneath the surface that makes the difference in a superior product.

Breadth of product line
- The HOLMBERG™ D-subminiature connector line has one of the widest available varieties of mountings and options — in both standard and high density configurations.

Quality from the inside out
- Full vertical integration assures top quality throughout the manufacturing process.
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- Factory and value-added centers provide fast turnaround and strict adherence to customer schedules. A perfect fit for today's Just-In-Time (JIT) manufacturing requirements.

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The addition of HOLMBERG™ connector products further strengthens our position as a broad line supplier of connector products. A close look at our company will reveal our strong financial position, our commitment to the future, and our ability to support your needs worldwide. Write for our Annual Report — it's like an X-ray of our company.

To take a close look at the HOLMBERG™ connector line, and for the location of our nearest stocking distributor, call 1-800-344-4744.

Thomas & Betts Corporation, Electronics Division
1001 Frontier Road, Bridgewater, NJ 08807, 201-685-1600
AVAILABILITY: Now from Allied-Signal Microelectronics Center, LSI Logic, and United Technologies Microelectronics Center (UTMC).

COST: Allied-Signal charges $760 (1000) for its part screened to 883C level B. The LSI Logic part costs $1334 (1000) screened to 883C in a PGA; a Class S part in a PGA costs $4406 (100). The 883C part from UTMC, screened fully to Standard Military drawings (SMD), costs $659 (100) for 12-MHz and $791 (100) for 16-MHz devices. For high-reliability and military-temperature screening only, the price is $555 (10 qty, 12 MHz) and $666 (10 qty, 16 MHz).

SECOND SOURCE: In negotiation.


Status: Allied-Signal 40-MHz device has been in production for 3 years. A 50-MHz version will extend performance to 6.0 MIPS on the integer DAIS (Digital Avionics Instruction Set) mix and to 4.1 MIPS on full DAIS instruction set. The Allied-Signal MMU chip and LSI Logic’s 1750A implementation that includes timers, counters, a hardware multiply, and a floating-point unit. Allied-Signal MMU chip and LSI Logic’s 1750A processor also in production. UTMC’s unit is in full production as an 883C product that conforms to the Defense Electronics Supply Center standard military drawing. UTMC offers the device to 10¹⁰ rad (Si) total-dose radiation hardness to meet data-sheet specifications.

HARDWARE CHARACTERISTICS

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, divide, and compare. Logicals and shifts. The instructions also provide bit-manipulation capabilities such as set, reset, and test. Single- and double-precision fixed floating-point and extended floating-point formats.

II—DATA-MOVEMENT INSTRUCTIONS
Instructions let you move data from register to memory, memory to register, between registers, and to the stack. Loads and stores in all formats plus test and set-bit operations.

III—PROGRAM-MANIPULATION INSTR
Conditional and unconditional jumps and branches. Calls are also supported. Stack management instructions suitable for high-level languages. Handles 16 levels of prioritized interrupts.

IV—PROGRAM-STATUS-MANIP INSTR
Emulation-mode status register accessible through I/O instructions. Instructions for accessing status, interrupt-mask, and fault registers.

Specification summary: The Allied-Signal version is a single-chip implementation that includes timers, counters, a hardware multiply, and a floating-point unit. The LSI Logic L64500 1750A implementation has a 16-bit CPU, expandable to 32 bits depending on the operation. The L64550 includes MMU with memory expansion to 1 M words, block-protect unit, memory-fault status register, bus-arbitration unit with 6 bus masters, start-up ROM interface, I/O port, trigger-go counter, and other options. Marconi’s MAS281 is a radiation-hardened 3-chip silicon-on-sapphire (SOS) module. The MAS31750 is a single-chip SOS version.

Hardware notes:
Diagram is for the UTMC 1750AR. Functions as a stand-alone RISC processor providing 8 MIPS at 16 MHz. In the 1750A operation mode, a throughput of 750k IPS at 16 MHz is achieved using the DAIS mix. Basic μP accepts 64k bytes of memory, expandable to 1M byte using an MMU.

Representative 1750A microprocessors

<table>
<thead>
<tr>
<th>Part number</th>
<th>Vendor</th>
<th>Technology</th>
<th>Price 883C</th>
<th>Price class S</th>
</tr>
</thead>
<tbody>
<tr>
<td>BX1750A</td>
<td>Allied Signal Microelectronics</td>
<td>CMOS</td>
<td>$750 (100)</td>
<td>—</td>
</tr>
<tr>
<td>L64500</td>
<td>LSI Logic</td>
<td>CMOS</td>
<td>$1334 (1000)</td>
<td>$4406 (1000)</td>
</tr>
<tr>
<td>MAS281</td>
<td>Marconi</td>
<td>CMOS/SOS</td>
<td>$1600 (100)</td>
<td>$8000 (20)</td>
</tr>
<tr>
<td>MAS31750</td>
<td>Marconi</td>
<td>CMOS/SOS</td>
<td>$2000 (100)</td>
<td>$10,000 (20)</td>
</tr>
<tr>
<td>1750AR</td>
<td>United Technologies Microelectronics</td>
<td>CMOS</td>
<td>$659 (100)</td>
<td>$1976–$3950 (100)</td>
</tr>
</tbody>
</table>

You can use an IBM PC with the software tools to provide interactive simulation and debugging of system configurations. Allied-Signal Microelectronics Center offers a development system for the A-S BX1750A that converts an IBM PC into a real-time, mappable monitor/debugger. An Ada source-level interface is under development. Tasco (Bellevue, WA) has an ICE pod for the HP 64000 development system. Call LSI Logic for contact phone numbers.

SUPPORT

Assemblers and compilers are available from several outside sources. Mikros Systems offers high-level debug software for its single-board computer/IBM PC system. UTMC offers a software package to aid in the development and debugging of system software and hardware. The software tool kit consists of a RISC or 1750 monitor, along with an interactive RISC simulator.
340X0 GRAPHICS µP FAMILY

AVAILABILITY: Now for 34010 and 34020. The 34082 floating-point unit is sampling now and is scheduled to be available in volume in the first quarter of 1991.

COST: The 34010 costs $23 (10k), the 34020 costs $89 (10k), and the 34082 floating-point unit costs $175 for samples.

SECOND SOURCE: Under active consideration.

Description: This 32-bit CMOS µP family is optimized for graphics-display systems. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular µP instructions, it has specialized instructions for pixel manipulation. 1-G-byte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits). The 34010 has a multiplexed, external 16-bit address/data bus; the 34020 is a full 32-bit machine. The 34020 is upwardly object-code compatible with the 34010 and features additional graphics-specific instructions.

32-BIT CMOS

Texas Instruments Inc
MOS Microcomputers
Box 1443, MS736
Houston, TX 77001
Phone (713) 274-2340
For more information, Circle No. 385

Status: Despite this µP family’s specialized slant toward CRT graphics, it does have a general-purpose Von Neumann architecture and instruction set. Also, some of its attributes can be equally applied to other, nongraphics applications. In particular, the µP can do rapid bit manipulation of a large local address field. A number of IBM PC-based board-level products incorporate this part. X-Window terminals are an example of an application in which this family’s graphics and general-purpose capabilities are utilized. One nongraphic area users are exploring is industrial control. In this area, the 340X0’s bit manipulation and low cost relative to other 32-bit µPs are attractive, according to TI (even for consumer-oriented uses such as arcade games).

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

General-purpose µP instructions: add and subtract, multiply and divide, rotate and shift, compare and logariths.

Special graphics instructions: add, subtract, and comparisons relating to x-y coordinates.

II—DATA-MOVEMENT INSTRUCTIONS

General purpose: move byte, move field, move register.

Special graphics instructions: move x half of register, move y half of register, pixel transfer, pixel block transfer.

III—PROGRAM-MANIPULATION INSTR

Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt.

IV—PROGRAM STATUS-MANIP INSTR

Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions.

Specification summary: 32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16 × 32-bit register files, hardware stack pointer, and 256-byte instruction cache. One of the 16-word register files contains a stack pointer and 15 general-purpose registers (the equivalent of the general-purpose registers found in nonspecialized µPs). Addressing modes of these registers are tuned to support high-level languages. Other register file is dedicated to CRT control as described in hardware note. Has 32-bit-wide address-data bus to support 1G byte of off-chip local memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A microcoded local-memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host µP. Fabricated in 5V CMOS and packaged in 88-pin PLCC. The 34020 is compatible with the 34010, but provides a 512-byte cache and supports 1M-bit video-RAM chips.

EDN November 22, 1990
Hermaphroditic Connectors
- Feature .050" centers
- 50 Ω impedance matched

The special contact design on Meritec's new CP50 Hermaphroditic connectors eliminates the need for separate male and female connectors. The 50 Ω impedance matched connectors feature .050" centers to maximize board real estate. Through hole, SMT and right angle configurations are available in sizes from 50 to 200 positions.

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- EMI/RFI shielded
- Impedance controlled

Meritec's economical new Shielded Performance Interconnects (SPI™) are ideal for fast logic, dense package applications which require low-noise crosstalk and high impedance control. The assemblies are EMI/RFI shielded and impedance controlled to the PC board. Available in straight or right angle configurations, the assemblies mate with .025" square or round pins and are side-to-side and end-to-end stackable on a .100" x .100" grid. The connectors are terminated to high speed subminiature braided shielded coax cable.

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Mark No. 61 on Inquiry Card
Mark No. 62 on Inquiry Card
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The OP-160 has a very fast slew rate of 1300V/µs and a unity-gain bandwidth of 90Mhz to meet the demands of your high-speed applications.
Settling time is only 75ns to 8 bits, 125ns to 12 bits. All of this performance requires only 6.5mA of supply current for cool, reliable operation in space-saving 8-pin DIP and SO-8 packages.

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If you require a dual high-speed amplifier, ask for PMI's OP-260.
68000 FAMILY

AVAILABILITY: Now for 68000 to 12 MHz, 68HC000 to 16 MHz, 68HC001 to 16 MHz, 68020 to 33 MHz, 68030 to 50 MHz, and 68040 at 25 MHz.

COST: For lower-frequency devices in 1000 qty, prices range from $5.50 for 68000 and $7.10 for 68HC000X to $47 for 68020 and $95 for 68030. Sample qty pricing for 68040 is $1.79.

SECOND SOURCE: Hitachi, SGS-Thomson, and Signetics/Philips all licensed with mask interchange for 16-bit parts. No second sources for logic for 68000 and $7.10 for 68HC00X to $47 for 68020 and $95 for 68030.

Description: 68000 architecture combines flexible 32-bit register set and large linear address space with powerful instruction set and flexible addressing modes. The 68040 is a full 68000-compatible µP containing an integer unit, floating-point unit (FPU), MMU, and instruction and data caches. The 68000 family will get a boost from its 68300 derivatives in embedded control. Signetics/Philips has the 68000 core in its ASIC library.

68000 FAMILY

Description: 68000 architecture combines flexible 32-bit register set and large linear address space with powerful instruction set and flexible addressing modes. The 68040 is a full 68000-compatible µP containing an integer unit, floating-point unit (FPU), MMU, and instruction and data caches. The 68000 family will get a boost from its 68300 derivatives in embedded control. Signetics/Philips has the 68000 core in its ASIC library.

Hardware notes:
1. Diagram of basic 16-bit 68000. Family offers growth path from 8-to 16- to 32-bit µPs. Performance results from multiple ALUs, 32-bit internal operation, and nonmultiplexed address and data buses.
2. Bottom-of-the-line 68008 has only 8-bit data bus and 20- or 22-bit address bus. 68010 is similar to 68000 but supports virtual memory. 68010 has 24-bit address bus. 68020 and 68030 are 32 bits throughout, including ALU and address and data paths. Both have instruction caches, and the 68030 also has a data cache and MMU. The 68040 adds an IEEE 754-compatible FPU.
3. Signetics/Philips 68070 includes 68000 CPU, two OMA channels, 68010 has 24-bit address bus. 68020 and 68030 are 32 bits throughout, and the 68030 also has a data cache and MMU. The 68040 adds an IEEE 754-compatible FPU.
4. Software notes:
   a. Five basic address modes are register direct, register indirect, immediate, absolute, and program-counter relative. Postincrementing, predecrementing, offsetting, and indexing can be added to these models.
   b. Can use eight 32-bit address registers as indexes or stack pointers. The eight 32-bit data registers can also serve as indexes.
   c. Branch and jump to subroutine. Branch conditionally.
   d. Link and unlink instructions invoking the address register as frame pointer (used to establish temporary local environments in structured programming).
   e. Seven levels of priority interrupts, including nonmaskable, with 256 possible interrupt vectors.

8/32-BIT, 16/32-BIT, 32/32-BIT

NMOS AND CMOS

Motorola Microprocessor Products Group
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 891-2000
For more information, Circle No. 386

Status: The success of the 68000 family is largely due to the Apple Macintosh II and the family's popularity in Unix-based workstations. The H8/332 is the other microprocessor in the legal battle that involves Motorola's 68030.

From third parties: Family widely supported by makers of universal µP development systems. Also, VMEbus system architecture is used in a range of applications with more than 150 independent suppliers of compatible products.

VersaDOS real-time operating system, system V/68 OS, CP/M-68K OS, concurrent DOS-68K OS, and VERTX real-time OS ($6775 from Honey Systems). Unix support from Motorola includes direct ports of Unix Systems V. X assembler for Exorax and VME/10, X-C compiler VME/10, and Exorax for VAX/780 available.

From third parties: Supplier has catalog listing outside support for family. New type of support software lets 68000 run MS-DOS (8086) programs using emulation from Phoenix (Norwood, MA) and Insignia (London, UK; offices in San Francisco) or by using binary translation from Hunter Systems (Palo Alto, CA).
SERIES 32000

AVAILABILITY: Now.
COST: $11.50 to $600 (1000) (see table).
SECOND SOURCE: None.
CORE: National Semiconductor is using the 32000 as the basis for its application-specific embedded processors.

Description: A 32-bit µP family in which various models feature differentiated address and data buses. The 32-bit core processor is highly symmetric; that is, its instructions and addressing apply regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It also has reputation for needing less memory space for programs. Some models offer instructions to support graphics and DSP. A slave processor interface lets you expand the CPU's capabilities.

HARDWARE

INSTRUCTION PIPELINE

LOADERS

ADDRESS UNIT

REGISTER FILE

EXECUTION UNIT

HARDWARE MULTIPLIER

INSTRUCTION QUEUE

ADDRESS UNIT

MEMORY MANAGEMENT UNIT

GRAPHIC SUPPORT LOGIC

DATA CACHE

BUS INTERFACE UNIT

SOFTWARE

DATA-MANIPULATION INSTRUCTIONS

All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals, and bit manipulation throughout memory space and CPU registers.

DATA-MOVEMENT INSTRUCTIONS

Intelligent string operations and bit-field handling allow efficient movements.

PROGRAM-MANIPULATION INSTRUCTIONS

Stack and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions.

APPLICATION-SPECIFIC INSTRUCTIONS

Graphics and digital signal processing.

Specification summary: 32-bit, "maxi-mini"-type pipelined architecture. Uniform addressing of as many as 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, and 32 bits, etc) and all register and memory locations. Performance of family ranges from ¾ to 10 MIPS (sustained).

Series 32000/EP family chips

<table>
<thead>
<tr>
<th>Device</th>
<th>DSP features</th>
<th>Bitbit support</th>
<th>On-chip peripherals</th>
<th>Buses</th>
<th>On-chip</th>
<th>Memory</th>
<th>(MIPS)</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>32FX16</td>
<td>Microcode</td>
<td>DMA</td>
<td>24 ADDRs, 16 data</td>
<td>mult.</td>
<td>None</td>
<td>15</td>
<td>$23.30</td>
<td>$33.60</td>
</tr>
<tr>
<td>32CG160</td>
<td>Microcode</td>
<td>DMA</td>
<td>24 ADDRs, 16 data</td>
<td>mult.</td>
<td>None</td>
<td>15</td>
<td>$38.90</td>
<td>$40.80</td>
</tr>
<tr>
<td>32CG160</td>
<td>Microcode</td>
<td>DMA</td>
<td>24 ADDRs, 16 data</td>
<td>mult.</td>
<td>None</td>
<td>15</td>
<td>$38.90</td>
<td>$40.80</td>
</tr>
<tr>
<td>32CGX20</td>
<td>DSP inter</td>
<td>DMA</td>
<td>32 ADDRs, 16 data</td>
<td>mult.</td>
<td>30</td>
<td>$135.70</td>
<td>$166.60</td>
<td></td>
</tr>
<tr>
<td>32CGX30</td>
<td>None</td>
<td>None</td>
<td>32 ADDRs, 16 data</td>
<td>mult.</td>
<td>30</td>
<td>$197.20</td>
<td>$206.00</td>
<td></td>
</tr>
<tr>
<td>32CGX30</td>
<td>None</td>
<td>None</td>
<td>32 ADDRs, 16 data</td>
<td>mult.</td>
<td>30</td>
<td>$197.20</td>
<td>$206.00</td>
<td></td>
</tr>
<tr>
<td>32CGX20</td>
<td>None</td>
<td>None</td>
<td>32 ADDRs, 16 data</td>
<td>mult.</td>
<td>30</td>
<td>$197.20</td>
<td>$206.00</td>
<td></td>
</tr>
</tbody>
</table>

SOFTWARE

From National: SYS32/20 converts IBM PC/AT into a Series 32000/EP development tool (from $3500). Development/evaluation boards are also available for each of the processors.

From others: ISE support for all the Series 32000/EP processors is available from Hewlett-Packard. Various vendors also offer turn-key solutions and/or design support for National Semiconductor's processors. Contact Series 32000/EP Marketing for details.

8/32-BIT, 16/32-BIT, 32/32-BIT

NMOS AND CMOS

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000
For more information, Circle No. 387

Status: The vendor recently introduced three family members: the NS2GX320, NS2FX16, and NS2CG160. Hardware and software integration techniques suit these processors for embedded applications such as page printers, facsimile machines, and multifunction office peripherals.

Hardware notes:
1. Dashed lines in diagram indicate optional modules for the 32000 family.
2. Floating-point chips (32081, 32181, and 32381) are examples of slave-type processors that vendor uses to extend CPU. These processors will be integrated on CPU when VLSI processing technology permits; they are transparent to programmer and recognize op codes not used by CPU.
3. Also available is the NS32580 that interfaces the CPU to the Weitek WTL3164 floating-point data path.

SUPPORT

From National: GNX (Genix Native and Cross) development-tools software includes assembler package and choice of C, Pascal, or Fortran compilers available for native (Sys32/50) and cross-development environments. Software that enables the 32FX16 and 32GX320 to operate as either a FAX modem or data modem is also available.

From others: Various Postscript and Postscript-compatible language interpreters, as well as related software support (fonts, PCL, etc) are available for laser-printer-controller designs. DOS-based development tools are available from Introl.
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VL 86C0X0 ARM

AVAILABILITY: Now for 86C010 and 86C020. VL86C050 I/O processor samples available now.

COST: $39 (100) for 86C010; $125 (100) for 86C020. 86C050 samples in PQFP $80.

SECOND SOURCE: Sanyo Semiconductor Ltd sources the 86C010.

CORE: Part of VLSI’s cell library. (Was designed by customer Acorn Computers using VLSI’s semicustom tools.)

Description: ARM stands for Acorn-RISC machine. The VL86C020 is software compatible with the -01. The second-generation chip includes a 4k-byte unified instruction and data cache on chip. The cache uses 64-way set-associative replacement with random replacement to provide a 93% hit rate. Current devices operate at 30 MHz with 35-MHz operation available by year end as the µP migrates into a 1.0-µm process technology. Low power consumption of 0.5W suggests the part for embedded-controller applications.

HARDWARE CHARACTERISTICS

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, logicals, and comparisons. Bit clear. Shifts (barrel shifter with ALU).

Il—DATA-MOVEMENT INSTRUCTIONS
Most data movements are by register-to-register instructions with option for multiple-register addressing. Only load and store operations to memory (typical of RISC). The VL86C010 includes a semaphore operation to support multiprocessing applications.

III—PROGRAM-MANIPULATION INSTR
Skip-type decision instructions (though old-fashioned, this simple approach can give fastest response in some cases). Branch instruction has option where combined PC and status register are copied in R14 data register for quick, simple return.

IV—PROGRAM-STATUS-MANIP INSTR
Usual status bits are combined with PC and mode-control bits in a 32-bit-long register. This combination allows all three elements to be saved in one fell swoop.

Specification summary: 32-bit CMOS Von Neumann (common memory) µP with RISC-style architecture. Has simple ALU with associated barrel shifter and set of 32 registers on CPU µP chip, 16 of which are accessible to programmer. Has some features expected in a large-memory-space machine: instructions and controls to handle virtual memory and caching; 32-bit external data bus and 26-bit external address bus allow linear addressing for external 64M-byte memory space (can be addressed on 8-bit or 32-bit-word basis). Only simple load and store instructions for external memory. 10- to 12-MHz, 2-phase clock gives 4- to 5-MIPS sustained performance with 10 to 12 MIPS max. Interrupt latency is 2.75 µsec max. No provisions for separate I/O addressing, so I/O must be memory mapped. Fabricated in 2-µm CMOS; chip is 230 mils on side, 0 to 70°C temperature range. Packaged in 88-pin JEDEC Type-B leadless ceramic chip carrier and plastic leadless chip carrier.

Software notes: 1. Only 44 instructions, in keeping with the literal RISC concept. 2. Simple RISC instructions are said to ease the task of writing efficient high-level-language compilers. 3. User and supervisory modes; supervisory mode entered by software interrupt.

Hardware notes:
1. In addition to the 86C010 µP, VLSI has an associated set of chips for memory (86C110), video (86C310), and I/O (86V410). For floating-point math, VLSI suggests one of the commercially available coprocessors.
2. Note the 27 registers. This number is less than on some RISC machines, but the registers do overlap, as is common in RISC, to speed interrupt service (overlapping gives automatic saving of data). Thus, a programmer sees 16 registers at most, and of these, 15 are general purpose.
3. Some provisions for memory management, including cache and virtual memory through abort-signal, mode-control bits.

HARDWARE SUPPORT

SOFTWARE

VLSI Technology Inc
8375 S River Pkwy
Tempe, AZ 85284
Phone (602) 752-8574
For more information, Circle No. 388

Status: The company supplies evaluation boards, assemblers, and C compilers directly. The architecture of the chip is targeted at the embedded-controller market and provides performance similar to most competing RISC processors at lower cost. VLSI’s goal is to sell the VL86C020 for less than $60 in high-volume production. The cost of the cache memory is included in the processor price. Cost is kept low because of small die size (approximately 280 mils square in a 1.0-µm process) and 160-pin plastic quad flatpack packaging. A dedicated coprocessor bus necessitates the high pin count. The 86C020 has found application in laser printers, network controllers, disk controllers, and graphics subsystems.
**80386**

**AVAILABILITY:** 16-, 20-, 25-, and 33-MHz versions in production (at four locations). 80386SX, 80376 sample availability now.

**COST:** In 1000 qty, $185 for 16-MHz 80386, $185 for 25-MHz 80386, $238 for 33-MHz 80386, $64 for 16-MHz 80386SX, and $91.25 for 20-MHz 80386SX. Low-power 16-MHz ($81) and 20-MHz 80386SX ($122.50) also available.

**SECOND SOURCE:** None.

**Description:** The 32-bit 386 family of µPs is compatible with the 8086 and 80286 families. Included are address-translation registers and a 32-bit address bus for as many as 4G bytes of physical memory and 64T bytes of virtual memory (the SX and 376 processors have only a 24-bit address bus). Runs DOS, Windows, OS/2, Unix, iRMX, and iRMK. Virtual 8086 mode allows direct execution of 8086 software under new 32-bit operating systems. The 386SX permits the manufacture of less expensive systems with full 386 software capability.

**HARDWARE CHARACTERISTICS**

**SOFTWARE**

**I—DATA-MANIPULATION INSTRUCTIONS**

Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter). Conversion between bytes, words, and double words. Arithmetic, including 16- and 32-bit operands and 32-bit signed and unsigned multiply and divide. (80387 math coprocessor has full IEEE-754 instructions, including all transcendental.)

**II—DATA-MOVEMENT INSTRUCTIONS**

String moves and gang push and gang pop of all registers. Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers).

**III—PROGRAM-MANIPULATION INSTR**

Repeat instructions based on flags. Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4G-byte memory space.

**IV—PROGRAM-STATUS-MANIP INSTR**

Flag instructions mostly same as on 8086 (contains four debug registers, allowing breakpoints on data or code accesses, even when in ROM).

**V—HLL AND OS INSTRUCTIONS**

Instructions for checking array bounds. Flag instructions mostly same as on 8086 (contains four debug registers, allowing breakpoints on data or code accesses, even when in ROM).

**VI—COMPLETE SPECIFICATION**

Instruction summary:

- **Address manipulation instructions**
  - Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter).
  - Conversion between bytes, words, and double words.
  - Arithmetic, including 16- and 32-bit operands and 32-bit signed and unsigned multiply and divide.
  - (80387 math coprocessor has full IEEE-754 instructions, including all transcendental.)

- **Data-movement instructions**
  - String moves and gang push and gang pop of all registers.
  - Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers).

- **Program-manipulation instructions**
  - Repeat instructions based on flags.
  - Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4G-byte memory space.

- **Program-status-manipulation instructions**
  - Flag instructions mostly same as on 8086 (contains four debug registers, allowing breakpoints on data or code accesses, even when in ROM).

- **HLL and OS instructions**
  - Instructions for checking array bounds.
  - Flag instructions mostly same as on 8086 (contains four debug registers, allowing breakpoints on data or code accesses, even when in ROM).

**Specification summary:** A more or less standard, "classical" 32-bit mini-computer architecture that has a basic register set similar to the previous 16-bit members of 8086 family so that it can directly run their machine code. It has added features that make it more general and suited to larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. Fabricated in 1.5-µm CMOS (supplies call it CHROMOS-III), the chip is expected to consume no more than 400 mA at 33-MHz external clock (18 MHz internal).

**Hardware notes:**

1. No on-chip cache, but 33-MHz 82385 cache controller ($422 1k) and 82395DX 16k-bit cache ($109 1k) can implement a cache.
2. On-chip MMU chip said to allow for memory management with no penalty in bus bandwidth (if off chip, supplier says, an extra cycle would be needed). Allows choices of segmentation or paging singly or in combination for multituser protection and for virtual memory.
3. The 80386 has its own math coprocessor, the 80387, which costs $497 for 33 MHz, $406.85 for 25 MHz (1000).
4. Along with the 80387 and 82385, the 80386 can use the 82380 32-bit peripheral combination chip that incorporates DMA and interrupt support and interval timers, etc.
5. The 80376 is compatible with the 868 programming model, but cannot run 8086 or real-mode programs. The chip has a 16-bit external bus.

**SUPPORT**

- From Intel: ASM-386 macroassembler ($600), RLL-386 binder and system software builder utilities ($600), and the MON-386 serially hosted debug monitor ($995). The C-386, Fortran-386, and PL/M-386 compilers (each $900) support 386 µP family protected-mode software cross development on D0S hosts. VAX/VMS kit support including ASM, RLL, compilers of choice, and VMS DB-386 incorporating a 386 system software simulator is also available on MicroVAX ($14,000) and VAX ($18,000) systems for cross-development.

- From others: Rapidly growing third-party support. Most important are MS-DOS and forthcoming OS/2 from Microsoft (Bellevue, WA). There are variations in DOS such as Concurrent DOS by Digital Research (Monterey, CA) UNIX and Unix 2 from AT&T (Morristown, NJ) and Zenna from Microsoft also available. Real-time executives offered by Ready Systems (Palo Alto, CA), JMI Software (Spring House, PA), and others. In addition, there are dual combinations of operating systems such as Unix-DOS, CTOS-DOS, and DOS-DOS.

**Note:** Some software depends on 386 mode.
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**80486**

**AVAILABILITY:** 25- and 33-MHz versions now in production.

**COST:** In 1000 qty, $760 (25 MHz) and $1003 (33 MHz).

**SECOND SOURCE:** None.

**Description:** The i486 CPU comprises an enhanced 80386 CPU, an enhanced 80387 math coprocessor, an 82385 cache controller, an 8-byte combined code and data cache, and a paging and memory-management unit. The i486 is binary compatible with 386/387 processor software but is 2 to 4 x faster because of enhanced execution pipelining and higher integration. The i486 CPU adds several new instructions that support caches and multiprocessor operating systems. A byte-swap instruction allows the i486 CPU to read data in either big- or little-endian format. A burst bus allows the i486 to fill the on-chip cache with 16 bytes of data in five clock cycles.

---

**HARDWARE CHARACTERISTICS SOFTWARE**

**I—DATA-MANIPULATION INSTRUCTIONS**
- Byte swap for converting between little- and big-endian data. Compare and exchange instruction. Exchange and add instruction. Floating-point instruction set from 387 math coprocessor added to i486 CPU.

**II—DATA-MOVEMENT INSTRUCTIONS**
- Information not provided by manufacturer.

**III—PROGRAM-MANIPULATION INSTR**
- Information not provided by manufacturer.

**IV—PROGRAM-STATUS-MANIP INSTR**
- Information not provided by manufacturer.

**V—HLL AND OS INSTRUCTIONS**
- Instructions for flushing and invalidating the caches.

**Specification summary:** A standard 32-bit architecture containing the same register set as its predecessor, the 386DX CPU. The 486 adds a small cache and floating-point processor as well as the instructions and control bits to support these features. The part is fabricated using a 1-µm process and consumes less than 700 mA at 25 MHz. The µP is packaged in a 168-pin ceramic PGA.

---

**Hardware notes:**
1. 8-byte unified instruction and data cache is located on chip. The cache lets the CPU read 16 bytes of code into the prefetch queue in one clock. A cache hit rate of better than 90%, for most applications, greatly reduces memory bus utilization for memory reads and improves system performance.
2. The Turbocache486 module ($299 for 64k-byte version and $399 for 128k-byte version at 33 MHz in 1000 qty; 25 MHz also available) is a complete second-level write-through cache controller and SRAM. The module contains the 82485 cache controller ($89 (25 MHz) and $99 (33 MHz in 1000 qty). The module’s look-aside design lets you add the module as an option much as the 387 was an option to 386 systems.
3. An on-chip MMU allows memory management identical to the 386DX CPU. The MMU allows segmentation, paging, or a combination of both for multituser protection and for virtual memory.

---

**HARDWARE SUPPORT SOFTWARE**

**ICE48633D In-circuit emulator ($49,000) supports the 486 µP to 33 MHz with real-time execution control over prototype 486-based systems.**

**ICD48625D in-circuit debugger ($250) is a hardware-assisted real-time debug monitor supporting 486 µP to 25 MHz.**

From Intel: Intel’s i486 assembler, compilers, system utilities, and software debuggers are intended for computer-system software development requiring access to the full native-mode architecture models of the 486 µP. ASM macroassembler ($600); RLL binder and system-software-builder utilities ($600); and C, Fortran, and PL/M compilers (each $900) support 486-family protected-mode software development by generating 486 instructions in code developed on DOS hosts. Language kits ($4500) including ASM, RLL, a compiler of choice, and the DB debugger are also available. VAX/VMS kit support including ASM, RLL, and a compiler of choice is available on MicroVAX ($14,000) and VAX ($18,000) systems for cross development.

---
CLIPPER

AVAILABILITY: Now for 25- and 33-MHz C200 chip sets and modules, the 211 CPU/FPU, 40- and 50-MHz C300 chipsets and modules, and the C311 CPU/FPU. The 40-MHz C4 will sample late this year.

COST: All 1000 qty: At 33 MHz, the C211 CPU/FPU costs $69, the C200 chip set costs $229, and the C200 module costs $424. At 40 MHz, the C311 costs $160, the C300 chip set costs $336, and the module costs $356. At 50 MHz, the C311 costs $191, the C300 chip set costs $495, and the C300 module costs $695.

SECOND SOURCE: Samsung Semiconductor.

Description: CMOS RISC-based µP has a dual-bus Harvard architecture. 3-chip set includes a CPU that incorporates a floating-point unit (FPU) and two cache/MMU chips: one for instructions and one for data. Available in first- and second-generation versions in modules, chip sets, and individual chips. The upcoming C4 is a superscalar implementation.

HARDWARE CHARACTERISTICS

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply, divide (32-bit integer and 32- and 64-bit IEEE floating-point operations done in floating-point unit), floating-point converts, negate, compare, logicals, including AND, OR, EXCL OR, and NOT. 32- and 64-bit shifts and rotates, including floating point.

II—DATA-MOVEMENT INSTRUCTIONS
Arithmetic favors register-to-register operations and avoids operations on memory other than register-to-memory movements. Nine addressing modes, including absolute, relative (with and without displacements), relative indexed, and PC (program-counter) indexed. Despite streamlined instruction set, architecture provides efficient string moves because execution control is switched over to macrocode ROM.

III—PROGRAM-MANIPULATION INSTR
Macrocode ROM is used for context-switching save and restore instructions that support entry and exit from interrupt and trap routines. Push, pop, supervisor, and user stacks (any register can be used as pointer).

IV—PROGRAM-STATUS-MANIP INSTR
Two status words, a user-program status word, and a privileged system status word, which can only be written in supervisory mode.

V—SPECIAL INSTRUCTIONS
Supervisory mode commands. Hardware supports 18 hardware traps and 128 supervisory calls. Software semaphores are supported for multitasking.

Specification summary: Modified RISC-type architecture in which the basic RISC instruction set is supplemented with boost from microinstruction ROM. The bus-bandwidth bottleneck is solved by having separate buses for instruction and data and putting a cache/MMU chip on each bus. Putting the caches on separate chips allows them to be large enough to generate hit rates greater than 90%. Partitioning also allows IEEE 64-bit floating-point operations to be incorporated on CPU chip so there is no off-chip delay. There is no need for CPU to have separate multiply-divide hardware because these operations can be done in the FPU. The chips are sold mounted with clock on a 3.5 x 4.5-in. multilayer-pc card with 96-pin DIN connector. C200 chips are also available separately.

Software notes:
1. Clipper's 164 instructions are a balance between 1-cycle-RISC and multicycle-CISC commands. The RISC takes care of the simpler, most frequently used instructions. The CISC macrocode takes care of complex instructions such as floating/integer conversion, character-string manipulation, save and restore registers, and trap/interrupt entry and return sequences.
2. C200 and C300 instructions are compatible.

HARDWARE

The Clipper Module card integrates the three Clipper chips into a functioning CPU. It provides the clock and program-counter wiring and a 96-pin DIN connector. User must provide the bus buffers externally. Intergraph supplies development systems that provide a 33-MHz Clipper CPU, 8M bytes of RAM, 156M bytes of hard-disk storage, and an Ethernet interface. Software includes Clix (which is based on Unix System V), a C compiler, a loader/debugger, and utilities.

SOFTWARE

A wide array of standards-based software is available from Intergraph, including Clix V.3.1 (based on Unix V.3.1) operating system; optimizing compilers for C, Fortran, and Pascal; RFS, NPS, and TCP/IP networking software; and X-windows windowing interface. More than 500 third-party packages are available, including compilers for Lisp, Ada, and other languages; tools and utilities; end-user application packages such as Word Perfect, Q-Calc, Q-Office +, Masterplan, and UniPlex II Plus; and the Ingres, Informix, and Oracle database programs.
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Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.
Here's another.

The NCR 53C700 SCSI I/O Processor…
So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

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As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

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NOW YOU CAN DESIGN A DEECO FLAT-PANEL TOUCHSCREEN IN NO TIME FLAT.

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With TouchAssist's menu-driven graphical interface, you just point and click.

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Lucas Deeco, a division of Lucas Durlston Corporation, 31047 Genstar Road, Hayward, CA 94544-7831

CIRCLE NO. 151
HYPERSTONE

AVAILABILITY: Delivery from stock.

COST: $150 (1000) for the 25-MHz part.

SECOND SOURCE: Zilog.

CORE: Zilog will use the Hyperstone µP as a 32-bit core in its library of µP cores.

Description: Hyperstone combines features of both RISC and CISC architectures. Although most instructions are 16 bits wide, some are 32 or 48 bits wide. Almost all instructions execute in a single cycle. The vendor claims that Hyperstone program code will be more compact than many CISC-architecture programs. The microprocessor uses a combination of pipelined load instructions, an internal decode/execute pipeline of two stages, and a proprietary look-ahead instruction cache to achieve high performance. In addition, on-chip DRAM and bus control simplify the interface between the µP and memory and peripherals.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
All instructions operate on 32- or 64-bit data. Most instructions are single cycle, but multiply and divide are multicycle. A barrel shifter provides left/right and signed/unsigned shifts. Two sets of arithmetic instructions are available: One set traps on overflow; the other only flags overflow. Logic instructions are AND, AND NOT, OR, XOR, and NOT. More powerful instructions include scaled index move, bound check, and scan leading zeros. IEEE-floating-point instructions execute by emulation.

II—DATA-MOVEMENT INSTRUCTIONS
Pipelined load/store architecture. Data types are byte and halfword (both signed and unsigned), 32-bit words, and 64-bit double words. Hyperstone contains single- and double-word move instructions.

III—PROGRAM-MANIPULATION INSTR
One unconditional and 12 conditional branch instructions provide program-counter relative delayed/undelayed branches. The µP executes dynamic branches via move or add instructions to the program counter. A call instruction creates a new variable-length stack frame in the register stack. A frame instruction restructures the stack frame for parameter passing. A return instruction returns control and restores the old stack frame. The µP handles overflow or underflow automatically.

IV—PROGRAM-STATUS-MANIP INSTR
One unconditional and 11 conditional trap instructions trap to supervisor state via a 64-entry table.

V—SYSTEM-LEVEL INSTRUCTIONS
Moves to special registers and setting the interrupt mask bit are only possible in supervisor mode.

Specification summary: The Hyperstone µP has a balanced set of instructions that make it useful as a universal processor. Since virtual memory is rarely used in embedded systems, Hyperstone doesn't include on-chip memory management. Demand paging via an off-chip memory-management unit is assisted.

SUPPORT

In-circuit emulator via an add-on board to the IBM PC. Add-on boards to the IBM PC and evaluation boards via an RS-232C port.

Hyperstone Electronics GmbH
AM Guckenbühl 10
7750 Konstanz
Germany
Phone (011) 49 075 316-7789
For more information, Circle No. 392

Status: The Hyperstone suits embedded-systems applications. Zilog recently announced its intention to use the Hyperstone in its library of µP cores. These cores form the base for microcontrollers for datacommunications, intelligent-peripheral-control, and disk-control applications.

Cross assembler/debugger on the IBM PC under MS-DOS. A C compiler is under development. Zilog is developing a behavioral model.
SPARC FAMILY

AVAILABILITY: See table.

COST: See table.

SECOND SOURCE: Fujitsu, Cypress, and Bit SPARC µPs are not hardware compatible. LSI Logic makes Fujitsu—and Cypress—compatible versions. All must run Sun Microsystems Inc (Mountain View, CA) SPARC software. Fujitsu, Cypress, LSI, Texas Instruments, and Philips/Signetics also provide SPARCµPs compatible controllers.

CORE: Fujitsu has made a start in this direction with a gate array. LSI Logic will also offer RISC elements in its ASIC library.

Status: L64811 supersedes the L64801. At least three vendors have signed up to produce SPARCstation 1 compatibles. Currently, more than 2000 applications run on SPARC hardware and numerous Sbus plug-ins are available. SPARC International (Sunnyvale, CA), a consortium of hardware and software vendors, creates and maintains open standards and multivendor compatibility of both SPARC-based machines and applications.

SPARC FAMILY

HARDWARE

ADDRESS GENERATION

DATA MANIPULATION

ALL BUSES 32 BITS UNLESS MARKED OTHERWISE

HIGH LOW ADDRESS

ALU

PROGRAM COUNTER (PC)

ADDRESS ALU

A REGISTER

ALU

CONTROL

NEXT PC AND SPECIAL REGISTERS

CONTROL

COPROCESSOR

EXTERNAL MEMORY

DATA

ADDRESS

INSTRUCTION pipeline

3-PORT REGISTER FILE

A REGISTER

B REGISTER

WRITE

ADDRESS GENERATION

SOFTWARE

CHARACTERISTICS

Functional unit

1. Diagram is for Fujitsu 86901. 86902—Fujitsu's embedded-control entry—is compatible with 86920 MMU and Weitek's 3170 floating-point unit. 86902 is missing 3 address-space-identifier lines and 3 of 4 hold inputs.

2. Cypress's SPARC embedded controller eliminates the user-defined coprocessor port and several control signals in addition to reducing the address bus to 24 bits and the address-space identifier to 3 bits.

3. LSI Logic's embedded SPARC comes without coprocessor ports. 4. Rather than redesigned parts, all embedded controllers are reduced-pin-count, crippled versions of existing parts.

Software note:

There are four stages (five in BIT µP) of pipelining. Optimizing compiler prevents pipeline breaks by inserting a delay instruction before branch instructions.

HARDWARE

SUN WORKSTATIONS

Sun workstations are adequate because Sun maintains software compatibility. Evaluation boards from Cypress and Fujitsu. Definicon and CAD/CAM International supply development boards. Call Cypress for company phone numbers. LSI Logic has a hardware-support program supplying a SPARCstation 1-compatible board with complete schematics, layouts, and films.

SOFTWARE

Vendors say they'll pass along Sun's optimizing compilers for C, Pascal, and Fortran as well as Sun's Unix operating system. Wind River Systems (Emeryville, CA) will provide a real-time operating system. A SPARC monitor is available from Bradley Forthwaite (Sunnyvale, CA).

32-BIT CMOS

Fujitsu Microelectronics Inc

Advanced Products Div

50 Rio Robles

San Jose, CA 95134

Phone (800) 523-0034

FAX (408) 943-9293

For more information,

Circle No. 393

Cypress Semiconductor

3901 N First St

San Jose, CA 95134

Phone (408) 943-2852

For more information,

Circle No. 394

Bipolar Integrated Technology (BIT)

Box 4750

Beaverton, OR 97076

Phone (503) 629-5490

For more information,

Circle No. 395

LSI Logic Corp

1551 McCarthy Blvd

Milpitas, CA 95035

Phone (408) 954-4985

For more information,

Circle No. 396

Description: Sun Microsystems defined SPARC at instruction-set and programmer’s model level and then entered into entirely separate joint agreements with silicon vendors with the intent of reaching 100-MIPS performance by 1990.

I—DATA-MANIPULATION INSTRUCTIONS

Add, subtract, multiply (step). Logicals and shifts.

III—DATA-MOVEMENT INSTRUCTIONS

Load and store to memory (in RISCs, only simple loads and stores used to external memory). Load and store to CPU registers. Load and store to floating-point registers. Load and store to coprocessor registers.

IV—PROGRAM-MANIPULATION INSTRUCTIONS

Call subroutine, branch conditional, save and restore, jump and link (128 hardware and 128 software traps, mostly user definable).

V—SYSTEM-LEVEL INSTRUCTIONS

Instruction-cache flush. Can set up system and user modes and associated protection.

Specification summary: Follows RISC philosophy of single-cycle instruction execution (averages 1.3 to 1.7 clocks per instruction). Family has a large number of on-chip registers to hold data being processed for rapid access, which also permits the fixed-length instructions to carry the two source and one destination addresses needed for single-cycle operations (register file has 3-port structure). On-chip registers are partitioned into seven 24-register groups that are overlapped at edges so that CPU can pass parameters between them. There are also eight global registers. Can address 4G bytes of direct address space and 256 pages of 4G-byte indirect space.

Representative SPARC family microprocessors

<table>
<thead>
<tr>
<th>Part number</th>
<th>Vendor</th>
<th>Function</th>
<th>Speed (MHz)</th>
<th>Available</th>
<th>Price</th>
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<td>—</td>
<td>—</td>
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<td>CY7C601</td>
<td>Cypress</td>
<td>Integer unit</td>
<td>25, 33, 40</td>
<td>Now</td>
<td>$349 (100)</td>
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<td>Cypress</td>
<td>Floating-point unit</td>
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<td>CY7C604</td>
<td>Cypress</td>
<td>MMU and single-processor cache controller</td>
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<td>Now</td>
<td>$491 (100)</td>
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<tr>
<td>CY7C605</td>
<td>Cypress</td>
<td>MMU and multi-processor cache controller</td>
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<td>4G Samples</td>
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<td>Ti</td>
<td>FPU</td>
<td>40</td>
<td>Samples now</td>
<td>$319 (1000)</td>
</tr>
</tbody>
</table>
0.99 Power Factor Corrected Switcher With Universal Input

1000 watt single and multiple output switch-mode power supplies operate from 120 VAC 15 Amp service, or as Universal Input from 90 to 264 VAC line without strapping. Units meet IEC 555-2 harmonic distortion and UL, CSA, VDE, EN, and FCC safety and EMI specifications. Other models operate from 48 VDC or 120/230 VAC. Contact: Qualidyne (619) 575-1100

Qualidyne CIRCLE NO. 163

Compact, Modular Switchmode Supply Meets Class B EMI

Compact power supplies can provide up to 400 watts with hundreds of volt/amp combinations of from 1 to 7 DC outputs. Units are available with in-line or side-mount I/O terminals and operate from 120/230 VAC. Options include Auto Current-Sharing with a isolated Power Supply Fail signal, ideal for N+1 use. Contact: Qualidyne (619) 575-1100

Qualidyne CIRCLE NO. 161

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Qualidyne CIRCLE NO. 162

EDN November 22, 1990
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At Micron Technology, we offer a full line of leading-edge RAM components in speeds and packages for virtually any application. But the memory business is more than just parts — it's people.

That's why we offer a total commitment to service and support, and a team of engineers and technical support personnel that are the most experienced memory professionals in the industry.

Because in the memory business there's only one point of view that counts. Yours.

Table:

<table>
<thead>
<tr>
<th>Component Family</th>
<th>Memory Size (Bits)</th>
<th>Org. (Bids)</th>
<th>Speed (MHz)</th>
<th>Features</th>
<th>Availability</th>
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<td>X3</td>
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<td>64K</td>
<td>x1</td>
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<td>X4 options: Write per bit</td>
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<tr>
<td>1MEG</td>
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<td>80-120</td>
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<tr>
<td>1MEG</td>
<td>x4, x8</td>
<td>90-120</td>
<td>X</td>
<td>X</td>
<td>CMSO, Fully static SDRAM, Serial input, Byte read transfer</td>
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<td>2MEG</td>
<td>x4</td>
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<td>CMSO, Fully static SDRAM, Serial input</td>
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<td>Triple Port DRAMs</td>
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<td>1MEG</td>
<td>x4, x8</td>
<td>90-120</td>
<td>X</td>
<td>X</td>
<td>CMSO, Two fully static SDRAMs, Transfer mask, Quad I/O Latch, Functional superset of 1MEG VRAM</td>
<td>X</td>
</tr>
</tbody>
</table>

Note: All options: write per bit, X4 options: Separate IC, I/O

2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3900
CIRCLE NO. 96

* Custom module and board-level product manufacturing services available.
R2000/R3000 FAMILY

DESCRIPTION: This RISC architecture was initially developed at Stanford University under the auspices of DARPA (Defense Advanced Research Projects Agency). The architecture supports as many as three tightly coupled processors.

Status: The R2000, R3000, and R3000A are multisourced, specification-compatible RISC µPs. Such workstation companies as Digital Equipment Corp., Silicon Graphics, Sony, and MIPS have selected the architecture as the one to build their RISC-based hardware on. The R3000 was selected by JIAWG (Joint Internal Avionics Working Group) as a standard for military avionics programs such as the Advanced Tactical Fighter.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Implements classic RISC load-store architecture where all data-manipulation operations occur on data in internal registers at the rate of one operation per cycle. Add, subtract, and logical operations, as well as multibit shifts, comparisons, and multiply and divide operations are in 3-operand format.

II—DATA-MOVEMENT INSTRUCTIONS
External memory is only accessed for simple loads and stores. Load and store to CPU registers. Processor supports loading and storing of unaligned 32-bit data.

III—PROGRAM-MANIPULATION INSTR
Processor contains a rich set of instructions for program manipulation and operating-system kernels. Has coprocessor interface to the MMU to support the virtual-memory system. The processor also contains instructions to manage program-control flow.

IV—PROGRAM-STATUS-MANIP INSTR
Exceptions can be initiated by interrupt, memory-access faults, and the floating-point coprocessor and are tracked by in-system control registers.

V—SYSTEM-LEVEL INSTRUCTIONS
Bits in the status register let the processor modify the system interface in order to perform memory-system diagnostics.

Specification summary: The R2000/R3000 implements a 5-stage pipeline to achieve a low average-clocks-per-instruction rate. Rich instruction set, sophisticated compilers, and high-frequency operation help the R2000/R3000 family achieve high performance. The IDT 79R3000 features a full cache controller, including on-chip tag comparison and direct control of the cache RAMs. LSI Logic's LR2000/3000/3000A includes thirty-two 32-bit general-purpose registers, on-chip cache control, on-chip memory management, and coprocessor interfaces for as many as three external coprocessors.

Representative R2000/R3000 family microprocessors

<table>
<thead>
<tr>
<th>Part number</th>
<th>Vendor</th>
<th>Speed (MHz)</th>
<th>Price</th>
</tr>
</thead>
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<td>IDT</td>
<td>20-40</td>
<td>$30 (10,000) General sampling in early 1991</td>
</tr>
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</table>

*ML versions available

Hardware note:
Diagram reflects R3000 architecture.

HARDWARE SUPPORT SOFTWARE

MIPS Computer Systems offers several machines for system development. The architecture is supported by a variety of tools, including logic-analysis tools from Tektronix, Arium, and Gould. IDT offers a line of CPU subsystems. IDT and LSI Logic also offer a range of development systems.

LSI Logic and IDT provide C, Ada, Pascal, Fortran, Cobol, and PL/I compilers for their CPUs. LSI also offers the System Programmers Package, an integrated toolkit for software and hardware development. The operating system RISC/OS is a merged AT&T System V.3 and Berkeley BSD 4.3 Unix including TCP/IP and NFS networking software. It includes the MIPS optimizing compiler as well as the MIPS symbolic debugger.

Refer to the RISCware directory from Synthesis Software Solutions Inc for a complete list of third-party software vendors.

1—DATA-MANIPULATION INSTRUCTIONS
Implements classic RISC load-store architecture where all data-manipulation operations occur on data in internal registers at the rate of one operation per cycle. Add, subtract, and logical operations, as well as multibit shifts, comparisons, and multiply and divide operations are in 3-operand format.

II—DATA-MOVEMENT INSTRUCTIONS
External memory is only accessed for simple loads and stores. Load and store to CPU registers. Processor supports loading and storing of unaligned 32-bit data.

III—PROGRAM-MANIPULATION INSTR
Processor contains a rich set of instructions for program manipulation and operating-system kernels. Has coprocessor interface to the MMU to support the virtual-memory system. The processor also contains instructions to manage program-control flow.

IV—PROGRAM-STATUS-MANIP INSTR
Exceptions can be initiated by interrupt, memory-access faults, and the floating-point coprocessor and are tracked by in-system control registers.

V—SYSTEM-LEVEL INSTRUCTIONS
Bits in the status register let the processor modify the system interface in order to perform memory-system diagnostics.

Specification summary: The R2000/R3000 implements a 5-stage pipeline to achieve a low average-clocks-per-instruction rate. Rich instruction set, sophisticated compilers, and high-frequency operation help the R2000/R3000 family achieve high performance. The IDT 79R3000 features a full cache controller, including on-chip tag comparison and direct control of the cache RAMs. LSI Logic's LR2000/3000/3000A includes thirty-two 32-bit general-purpose registers, on-chip cache control, on-chip memory management, and coprocessor interfaces for as many as three external coprocessors.

Representative R2000/R3000 family microprocessors

<table>
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<th>Part number</th>
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Refer to the RISCware directory from Synthesis Software Solutions Inc for a complete list of third-party software vendors.
29000 FAMILY

AVAILABILITY: Now for 29000 CPU and 29027 arithmetic accelerator.

COST: $88 for the 16-MHz 29000, $68 for the 16-MHz 29005, and $268 for the 16-MHz 29027 (1000). Parts are also available in 20- and 25-MHz grades.


Description: State-of-the-art implementation of RISC µ.P concepts with expected stress on obtaining as close to single-cycle operation as possible (even with branching) and an emphasis on keeping users' system costs down by bus timing, etc., which allows lower-cost external memories. Although their natures are similar, the 29000 and 29030 building-block families are intended for user-defined (microcoded) complex instruction sets, whereas the 29000 µ.P family has a regular, fixed, and purposely simple instruction set; moreover, the instruction set is decoded by logic. Companion compilers are an essential part of family.

32-BIT CMOS

Advanced Micro Devices (AMD)
901 Thompson Pi
Sunnyvale, CA 94086
Phone (408) 732-2400
For more information, Circle No. 401

Status: In the 2½ years since its introduction, the 29k has accumulated over 200 design wins, and 35 companies have announced 29k-based products. Areas of particular success for the RISC µ.P are high-end laser printers; X-terminals; graphics, including graphics controller boards, graphics accelerators, real-time image processing, and medical imaging; and network products, including protocol converters, network node controllers, FDDI networks, and ISDN-related systems.

Hardware notes:
1. Burst-mode addressing allows use of lower-cost video RAMs to replace more-expensive, high-speed, static CMOS RAMs, with only moderate loss in performance (14 MIPS sustained vs 17 MIPS).
2. There is a coprocessor interface to companion 29027 floating-point chip. The 29027 uses combinatorial logic, so operations take only five 29000 cycles.

Software notes:
1. Total of 115 instructions. All are not yet implemented in hardware; those that aren't cause traps.
2. Multiply and divide on the 29000 only does one step. The full multiply and divide instruction causes a trap operation at which a compiler can insert a software routine.

Specification summary: 32-bit CPU fashioned after RISC concepts; performs most frequently used, simple instructions in one cycle. Offered with companion compilers that take advantage of architectural simplicity and produce performance-optimized code. 29027 floating-point chip, in more CISC fashion, makes up for crudeness of math instructions (only partial multiplication and division instructions). Features that ensure uninterrupted flow in 29000's 4-stage execution pipeline are single-cycle branching with branch delays and a 512-byte branch-target cache. Main 192-register file has a 3-port configuration so instruction fields can specify sources for both operands and the destination for the result. 128 of the registers are addressed by a stack pointer that (in conjunction with the compiler) provides a type of caching that speeds procedure calling. External memory space is reached by 4G-byte virtual addressing with demand paging. An on-chip 64-entry MMU performs address translation in a single cycle and is flexible so users can choose memory strategy.

Hardware:

The EB29k is a PC plug-in execution board with software-development tools.

From others: Embedded Performance Inc, Hewlett-Packard, and Step Engineering all provide real-time in-circuit emulators for the 29000 family. Logic Analyzer interface is available from Bitware or Hewlett-Packard. Various VMEbus board products based on the 29k are available from Ironics. Behavioral simulation models are available from Logic Automation and Mentor Graphics. Design-verification and test-generation models are available from Teradyne. A list of third-party support products appears in the biannual Fusion29k Catalogue published by AMD.

Software:

AMD supplies the complete software tool chain. These tools include the ANSI standard HighC29k optimizing compiler with an assembler, linker, and ANSI standard libraries; floating-point-math libraries; and architectural and instruction-set simulators. The Xray29k source-level debugger is also available for the 29k. The Mon29k is a target debug monitor for system developers. All software support tools run on IBM PC/ATS and Sun-3 and Sun-4 workstations.

Other C compilers are available from Embedded Performance Inc, Metaware, Microtec, and Intermetrics. Pascal compilers are available from Metaware. The GNU tool chain, including the G++ and the debugger are available from Cygnus. Ada is available from Verdict Systems. Fortran is available from Yarc, Ready Systems, JMI, and Telenetworks provide real-time operating systems. A complete guide to third-party software products is published in the biannual AMD Fusion29k catalogue.

184 EDN November 22, 1990
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We offer 29 types with ratings from 0.1 to 33µF, and from 10 to 35V DC.

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  - Built-in fuse; 21 types.
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</table>

OKI Semiconductor
Transforming technology into customer solutions

785 North Mary Avenue
Sunnyvale, CA 94086-2909

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88000

**AVAILABILITY:** Both the 88100 CPU and the 88200 32-bit CMOS cache/memory-management unit (CMMU) are available now in 16-, 20-, 25-, and 33-MHz versions.

**COST:** The 88100 costs $168; the 88200 costs $198 (1000).

**SECOND SOURCE:** None.

**CORE:** Motorola’s architecture can incorporate as many as six special-function units into the 88100 chip.

**Description:** The 88000 RISC family encompasses the 88100—the CPU—and the 88200—the memory-management unit. The 88100 chip supplies full 32-bit registers, data paths, and addresses. Most instructions, including standard IEEE-P754 floating-point math operations, execute in one cycle or are put in a concurrent execution pipeline in one cycle. The companion 88200 cache/memory-management unit supports a demand-paged virtual-memory environment. The chip controls two 4G-byte logical address spaces—one for the user and one for the supervisor. The chip’s architecture supports multiprocessor operations.

**HARDWARE CHARACTERISTICS**

1. The 88100 includes 32 general-purpose registers.
2. The 88100 incorporates 16k bytes of cache memory as well as cache-control logic, memory-management logic, and bus-control circuits. Multiple CMMUs can operate in parallel. Both the 88100 and 88200 come packaged in 180-pin PGA packages. The chips operate over the 0 to 70°C temperature range.

**Software**

**SOFTWARE**

**From others:** Add-in boards are available for the IBM PC/AT from Opus (Cupertino, CA), for the IBM PS/2 from Prometa (Gainesville, FL), for the Apple Macintosh from Tektronix (Beaverton, OR), for the VMEbus from Force (Campbell, CA) and Tadpole (Cambridge, UK), and for the VAX from Avalon (Santa Barbara, CA).
80960

AVAILABILITY: Now for 10-, 16-, 20-, and 25-MHz 80960KA and KB in PGAs; 16- and 20-MHz plastic quad flatpack (PQFPs); 16-, 20-, and 25-MHz 80960MC in PGAs and QFPs; 16-, 25-, and 33-MHz 80960CA in PGA; and 16- and 25-MHz 80960CA in PQFP.

COST: Prices depend upon speed, package, and temperature range. In 1000s, prices range from $27 to $56 for the 80960KA, $35 to $73 for the 80960KB, $520 to $1058 for the 80960MC, and $81 to $122 for the 80960CA.

SECOND SOURCE: Internally sourced from three different Intel facilities.

Description: The 80960 is Intel's 32-bit family of µP chips that has been designed specifically for embedded-control applications. There are four upwardly compatible versions of the RISC-based architecture. The family includes the basic 80960KA core version, which provides 6 to 12 VAX MIPS (depending on frequency); the 80960KB, which includes an on-chip floating-point unit; the 80960MC, which comes with on-chip memory-management/protection and multiprocessor support; and the 80960CA, which features a software-configurable pipelined bus, 1.5k bytes of on-chip data RAM, a 1k-byte, 2-way set-associative instruction cache and a 4-channel chaining DMA processor.

Hardware notes:
1. The 80960 provides only one bus data for instructions and data. The bus multiplexes address and data information.
2. The basic 80960 chip includes 16 32-bit global registers and 16 32-bit local registers. The stack requires one global and three local registers for housekeeping operations.
3. The floating-point unit (80960KB) also includes four 80-bit registers, but can use any register.

From Intel: The EVQT960E ($960) with 256k bytes of zero-wait-state memory and the EVQT960F ($1960) with 256k bytes of zero-wait-state memory are serially hosted execution and prototyping boards for the 80960KA/KB. The EVA960KB board ($4500) is an IBM PC/AT-compatible board with onboard debug monitor and as much as 4M bytes of dynamic RAM. The EVXY960MC board ($9000) is a 25-MHz Multibus I development board for military and Ada applications. The EV9606CA ($3500) is an evaluation board for the 80960CA. The ICE960KB in-circuit emulator ($16,495) is available for the 80960KA/KB. The 85C960 is a bus-control chip for the KA/KB; the 27960CX/KX are high-speed burst EPROMs for the 80960KA/KB/CA, the 27C202 is a high-speed, 16-bit-wide EPROM for the 80960KA/KB/CA. The 82380 is a multifunction peripheral with timer - counters, 8 channels of OMA, and a 256-byte register cache, and a 4-input interrupt controller. The 80960KB includes the basic 80960KA core version, which provides 6 to 12 VAX MIPS (depending on frequency); the 80960KB, which includes an on-chip floating-point unit; the 80960MC, which comes with on-chip memory-management/protection and multiprocessor support; and the 80960CA, which features a software-configurable pipelined bus, 1.5k bytes of on-chip data RAM, a 1k-byte, 2-way set-associative instruction cache and a 4-channel chaining DMA processor.

Software:

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 403

Status: Since the 80960 family's introduction, the family has enjoyed widespread acceptance in a broad spectrum of commercial and military designs. The 80960 family played a role in legitimizing the 32-bit embedded-control market. Intel's approach is family oriented; not only is there a wide range of 32-bit CPU chips at different price/performance levels, but there are also 80960-specific support components such as the 27960 burst EPROM and 85C960 bus control component. Intel claims the total kit approach exists to serve embedded-control customers with an easy-to-design-with set of CPU and peripheral parts.
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Spectrum
1021 S. Wolfe Road
Sunnyvale, CA 94086
(408) 738-4387
### i860

**AVAILABILITY:** The 33- and 40-MHz versions are available now.

**COST:** The 33-MHz i860 costs $750 (1000).

**SECOND SOURCE:** None.

**Description:** The i860 CPU is a 64-bit µP designed to provide balanced performance across integer, floating-point, and 3-D graphics operations. The µP incorporates a RISC integer unit, a floating-point adder, a floating-point multiplier, an 8k-byte data cache, a 4k-byte instruction cache, paging functions, an MMU, and a 3-D graphics unit. The i860 runs Unix but is not designed to run 386 software.

**Status:** The i860 has amassed more than 50 design wins to date in supercomputer, minicomputer, 3-D graphics workstation, and application accelerator designs. Multiprocessor version of Unix/System V rel 4.0 is available.

---

### Hardware

#### 64/32-BIT CMOS

Intel Corp
Embedded Controller Operation
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051
For more information, Circle No. 404

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080
For more information, Circle No. 405

---

### CHARACTERISTICS

#### DATA-MANIPULATION INSTRUCTIONS

- Integer arithmetic, logicals, and shifts.

#### DATA-MOVEMENT INSTRUCTIONS

- 16-, 8-, and 4-byte floating-point loads and stores, with variable strides and autoincrement. 4-, 2-, and 1-byte integer loads and stores. Transfers between integer and floating-point registers. Special load instruction assists data caches. Pixel-store operation of 8 bytes.

#### PROGRAM-MANIPULATION INSTR

- Unconditional and conditional branches, both delayed and nondelayed forms. Single-cycle loop-control operation. Indirect call and indirect branch. Dual-instruction mode allows execution of two instructions per clock.

#### SYSTEM-LEVEL INSTRUCTION

- Data-breakpoint register for breakpoint debugging. Big-endian mode bit switches between access modes. Cache-control bits for cache locking and testing.

### SOFTWARE

#### HARDWARE

From Intel: Information not provided by manufacturer.

#### SUPPORT

From Intel: Fortran and C compilers.

From Others: Industrial Programming (Jericho, NY) offers a real-time kernel. Metaware (Santa Cruz, CA) offers three varieties of High C. Green Hills (Glendale, CA) sells Fortran and C compilers, DDC-I sells an Ada compiler, and Micro Focus (Palo Alto, CA) sells a Cobol compiler for the i860.
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<th>Product Category</th>
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<td>PWM Controllers</td>
<td>1 MHz, Additional Fault Protection, Synchronization</td>
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<td>Resonant Control</td>
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<td>Motor Control</td>
<td>BLDC Sensorless Commutation</td>
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</table>

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EDN November 22, 1990
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CIRCLE NO. 111
Real-time applications are concerned with physically real processes that proceed in terms of real-world clocks. Thus, such applications must be able to link up with real-world time, as opposed to CPU or other internal computer time. Part 6 of this series discusses the two aspects of time that are involved: interval and time of day.

David L Ripps, Industrial Programming Inc

Suppose you must send a stepping pulse to an electro-mechanical device. Such devices are very slow compared with computer operations; for the pulse to be effective, it must be on for at least, say, 50 msec. The requirements are thus

```
turn pulse on
pause 50 ms
turn pulse off
```

Suppose further that the stepping pulse toggles the AM/PM lamp on a display panel. The preceding sequence must be performed at noon and again at midnight. This requires not only the ability to generate a 50-msec interval but also the ability to place that interval at an exact time of day.

```
while displaying time
{
    wait until 12 AM (noon)
    turn pulse on
    pause 50 ms
    turn pulse off
    wait until 12 PM (midnight)
    turn pulse on
    pause 50 ms
    turn pulse off
}
```

Pause for a given interval

A pause request efficiently delays task processing for a specified interval. During the pause, the CPU is automatically available for other work. In C, a typical request is

```
pause (MS+25);
```

In `pause`, as in all other requests that require an interval specification, the interval consists of two parts. The first chooses the time units, MS in the example.
**Pause** can be an effective means to block a task until it receives a "go-ahead" command from some other task.

The include file MTOSUX.H defines the possible time units as:

- `msec` → `MS`
- `ten msec` → `TMS`
- `hundred msec` → `HMS`
- `seconds` → `SEC`
- `minutes` → `MIN`
- `hours` → `HRS`
- `days` → `DAY`

To one of these is added the number of such units, 1 to 255. Thus, the range for intervals is 1 msec to 255 days.

When the interval is 0, there is no limit to the wait; the pause could last forever. As you will see, however, a pause can be canceled by another task. Thus, `pause (0L)` really means "pause until canceled." The literal `NOEND` should be used instead of `0L` to make this case explicit.

For success, the pause function returns `NOERR` when the specified interval ran to completion or `TIMCAN` when the pause was canceled (by `canpau`). The failure values are `BADPRM` when an illegal interval is given or `QUEFUL` when the service could not be rendered for lack of internal resources.

Some further examples of the pause function are:

- `status = pause (250+ MS); /*pause for 250 msec*/`
- `status = pause (SEC+1); /*pause for 1 sec*/`
- `status = pause (NOEND); /*pause until canceled*/`

### The real-time clock

The OS maintains a tally of the number of milliseconds since the system was started to support time-dependent services, such as pause and terminate-with-future-restart. The physical source of this time base is a clock chip that generates an interrupt periodically. The clock period is installation dependent, with 5 to 20 msec as the normal range. Fractional periods, such as 16½ msec (60 Hz) or 1024 interrupts in 1000 msec, can be easily accommodated. A real-time clock interrupt is often called a "tick" as a reminder of its mechanical counterpart.

The period sets the "granularity" of the time base. (In reality, the OS is counting clock ticks, but keeping the tally in terms of milliseconds.) Thus, with a period of 5 msec, the tally remains constant for 5 msec and then increases by 5. As a result, although a service request will accept an interval of, say, 3 msec, it could take as long as 5 msec to recognize that the time has elapsed.

Pause for a specified interval of time is a fundamental facility that is provided by all real-time operating systems. Alternate names are `delay` and `sleep`.

### Alternate representations of time interval

The representation of time interval by the 2-element structure:

```
unit code; number of units;
```

is not unique to MTOS-UX. The proposed MOSI standard also specifies intervals in this way, but with a different set of unit codes (Ref 1).

```
implementation-dependent ticks
microseconds
milliseconds
seconds
minutes
hours
```

In Ada (a language designed for real-time applications), intervals are measured in units of seconds, with a precision that is implementation dependent. Thus, a 25-msec pause is

```
delay 0.025;
```

Some operating systems always measure interval in clock ticks; they do not offer any absolute time units. However, most physical events are known inherently in terms of real-world clock units, not arbitrary clock ticks. Thus, if you were to use clock ticks and (as could easily happen) the tick time had to be changed, all intervals in all tasks would have to be recomputed. Since there is a danger of missing some intervals, modern practice is to hide the tick time within the OS and have the tasks work with absolute time units.

### Pause for minimum time interval

In some real-time applications, there is a task that must run on every clock tick. Often that task has the job of sampling input data for changes. A common structure for such a task is as an initialization section (which is entered just once) followed by a cyclic section.
The cyclic section ends with a pause for a minimum interval and a branch back to itself.

```c
samptsk ()
{
    ... /* initialization section, if needed*/
    while (1)
    {
        ... /* cyclic section */
        pause (NXTICK);
    }
}
```

The literal `NXTICK` produces `MS + 1`. Because of the granularity of the real-time clock, a 1-msec pause is always canceled at the next clock tick (for any value of the clock period). The value `MS + 0` does not work, however, since for an interval of zero there is no pause at all.

Note that `samptsk` could have been composed with `trmrst` instead of `pause`, as was done in task `PdSA` in Part 4 of this series (EDN, October 25, 1990, pg 193). (A “first-time flag” would be needed to skip the initialization section after the first entry.) However, the overhead for pausing is always less than that for terminating and restarting a task so that `pause` is preferable in this special case. In general, if the cycle time of the task is greater than every clock tick and the cycle time must be added to the last start time of the task, the cycle must be maintained by `trmrst` rather than `pause`.

### Synchronization for exact time intervals

It is sometimes necessary to separate two events, such as the generation of a pair of outputs, `A` and `B`, by a given interval, say, 250 msec. A straightforward approach would be to output `A`, `pause(250 + MS)`, output `B`. However, because of the granularity of the clock, the pause interval is usually shorter than expected. (On average, half the current clock period is already over when a pause is issued. Thus, the average pause is half a clock period too short.)

When accurate intervals are required, it is best first to synchronize to the start of a clock period by issuing a pause for 1 msec. The sequence would then become `pause(NXTICK)`, output `A`, `pause(250 + MS)`, output `B`.

When a pause ends, the task becomes ready to run, but the actual resumption of task execution may be further delayed if there are Ready tasks of higher priority. Consequently, if a task needs an exact interval, it also needs a very high priority.

### Cancel pause

The primary purpose of `pause` is to block the requesting task for a given interval. Nevertheless, `pause` can also be an effective means to block a task until it receives a “go-ahead” command from some other task. The go-ahead is achieved by canceling the pause via a new service, `canpau`. Thus, the scenario for this mode of task-to-task coordination is

```
task T
```
```
pause (NOEND)
```
```
[task blocked] < monitor application to decide
```
```
task C
```
```
[both tasks continue independently]
```
```
[task blocked] canpau (tskTid)
```
```
[both tasks continue independently]
```

The argument of `canpau` is the identifier of a particular task. Thus, the coordination provided by `pause` / `canpau` is...

---

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All of the C examples in this series, plus applications of your own, can be run on a PC with a set of demonstration disks available from Industrial Programming Inc. The disks contain a full version of MTOS-UX for an IBM PC/AT or compatible. An application program is edited, compiled, linked, and loaded under MS-DOS. The MTOS-UX then takes over the hardware to execute the program in real time. At any time, you can enter an alt/dlt command from the console to return control to MS-DOS.

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Certain tasks must be synchronized with the clock portion of the TOD (time-of-day) clock/calendar string.

cancel pause is always directed toward one specific target task. More general methods to coordinate with any number of tasks or with a task whose identity is not necessarily known will be given in later parts of this series.

By stipulating a finite interval for the pause, you can ensure a limit to the wait in case the expected event that the monitor task is seeking never occurs. Task T can use the value returned by pause to determine whether C canceled the pause (value TIMCAN) or the maximum wait time was reached (value NOERR).

if (pause (250 + MS) == TIMCAN)
{ /*task continued via cancel pause for coordination*/
   ...
}
else
{ /*task continued at end of maximum wait limit*/
   ...
}

The argument of canpau must be the identifier of an existing task. If not, the function returns a failure value BADPRM. Of course there is no guarantee that the target task is actually paused when the cancel is issued. To provide this information, canpau returns NOERR when the specified task was paused and NOT-OUT when the task was not paused.

Time of day clock/calendar

Many applications must be aware of the real-world time and date. (The term “wall time” is often used to refer to real-world time.) Time and date may be needed as tags on console messages or may be the key for storing data. Wall time may also be a factor in deciding what processing to do or how to do it. For example, a traffic-control program may switch algorithms or parameters as predetermined periods of peak demand approach.

An OS must maintain clock and calendar information in either binary or ASCII-encoded form. For MTOS-UX, the information is kept as a time-of-day (TOD) clock/calendar string of the form

```
DD MMM YYYY HH:MM:SS 0
```

where

- `DD` = day in month, starting at 01
- `MMM` = abbreviated month name
- `YYYY` = year
- `HH` = hour, 00 to 23
- `MM` = minute, 00 to 59
- `SS` = second, 00 to 59

A sample string is

```
“11 NOV 1918 11:00:00”
```

The month names are JAN, FEB, MAR, APR, MAY, JUN, JUL, AUG, SEP, OCT, NOV, DEC. Since the terminal null counts as a character, the string length is 21, not 20.

Ada provides an example of a binary encoding of clock/calendar information. As specified in package CALENDAR (Ref 2), the runtime support system for Ada must be able to supply the date and time as

- `YEAR-NUMBER` is INTEGER range 1901 .. 2099
- `MONTH-NUMBER` is INTEGER range 1 .. 12
- `DAY-NUMBER` is INTEGER range 1 .. 31
- `DAY-DURATION` is DURATION range 0.0 .. 86.400.0
- `TIME` is private;

```
function CLOCK return TIME;
procedure SPLIT ( DATE : in YEAR NUMBER ;
                 MONTH : out MONTH NUMBER ;
                 DAY : out DAY NUMBER ;
                 SECONDS : out DAY DURATION );
```

Function `CLOCK` returns a snapshot of the internal time in a format that is hidden from the task (“private”). That internal time can then be partitioned into its binary components with procedure `SPLIT`.

Set clock/calendar

The OS must have a source from which it can initialize or derive its TOD values. If the system has support hardware, such as a battery-backed clock/calendar chip, the OS can obtain TOD information without any task-level help. Commonly, however, the TOD is set by task request. When the TOD is encoded as a string, a typical request could be

```
char todstg[21] = “4 JUL 1776 12:00:00”;
settod (todstg);
```
The argument of `settod` is the address of a null-terminated string of the form just shown. If the format of the string is not valid (for example, if the month name does not exactly match one of the 3-character abbreviations), the function fails and `settod` returns a value of `BADPRM`. A successful invocation returns a value of `NOERR`.

Once set, the string is automatically advanced each second. It is assumed that the `settod` is issued at the beginning of the given second. The TOD string may be set and reset at will by any task. This has no effect upon outstanding pauses, timed restarts, and other interval-based time processing. (Such processing involves the millisecond counter, not the TOD string.)

Get (read) clock/calendar

The current clock/calendar string may be read by issuing

```
gettod (todbfr);
```

The entire string (including the terminal null) is copied into the read-write buffer whose address is given by the argument. The string is guaranteed to be consistent; the clock/calendar is not permitted to change during the copy.

The following C task outputs the clock/calendar every minute.

```
cctask ()
{
    char ccstg[21]; /* clock/calendar str in g */
    while (pause (MIN + 1) == 0) /* pause 1 minute*/
    {
        gettod (ccstg); /* get time*/
        printf ("%s", ccstg); /* output to console*/
    }
}
```

Synchronization with TOD

Certain tasks—typically those that produce periodic reports and summaries—must be synchronized with the clock portion of the TOD clock/calendar string. MTOS-UX has a straightforward mechanism to perform this type of synchronization. For example, to pause until exactly 10:30, submit the request

```
syntod ("103000");
```

The argument must be the address of a null-terminated string of the form "HHMMSS". HH may be either a numeric value in the range '00' to '23' or '?' (match any). MM or SS may be '00' to '59' or '??'.

After invoking the service, the task is blocked until the given time string matches the TOD clock/calendar. This is a simple pattern match. Thus, if a wait for "103000" is issued at "103001", the task will wait until the next day. The string "??1500" waits for 15 minutes after the hour, while the string "????00" waits for the beginning of the next minute. The function returns a `NOERR` upon a successful call.

The function `syntod` is often invoked at the beginning of the repeated section of a periodic task, as `pause` was used at the end of the cycle in the sample task on pg 199.

```
reportsk ()
{
    ...
    while (1)
    {
        syntod ("000000"); /* wait until midnight*/
        ...
    }
}
```

Get system time

The tally of the number of milliseconds since the system was started is a 6-byte field of the form

```
struct timer
{
    short int u2; /* most significant 2 bytes of tally*/
    long int 14; /* least significant 4 bytes of tally*/
}
```

It may be copied into a given user buffer via

```
struct timer mbuf;
getime (&msbuf);
```

The function returns with `NOERR` unless there is a problem writing into the buffer. For write errors, the return value is `BADPRM`. The 6-byte value is guaranteed to be consistent, even if a clock interrupt occurs while the copy is being made.

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CIRCLE NO. 44

To sum up, the `pause` statement instructs the OS to block the requesting task for a specified interval of time (or "forever"). This permits a task to adjust its pace to the external physical world. During the pause the processor is available for work by other tasks. A paused task can be restarted upon the request of another task. This provides a private means of coordination, targeted to a specific task and hidden from all other tasks. Since the pause cannot extend beyond the original pause interval, the target task can impose a limit on its wait for coordination.

The OS accepts a time of day clock/calendar string from any task and thereafter updates it every second. The current value of that ASCII string may be retrieved at any time. A task may also request to be blocked until it matches a given time-of-day pattern, with "match any" as a possibility for the hour, minute, or second fields.

Part 7 of this series will discuss task coordination via event flags.

References

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(1) All data normalized to DECstation 3100. Comparable configurations tested. Geometric mean used to combine results. Performance will vary depending on applications and environment. (2) Graphics and windowing data measured using X11 perf benchmark. (CPU Integer and Floating Point performance measured from running SPEC V1.0 workload. (3) SPEC performance estimate based on SUN 4/330 results published by Sun Microsystems, Inc.

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- Provides automatic switching
- Eliminates need for mechanical switch

The LXT902 Ethernet 10Base-T media-access unit (MAU) provides automatic switching between twisted-pair LAN wires and attachment-unit interface cables. The device is 100% compliant with IEEE-802.3 draft 10 standards and is suitable for either internal LAN line-card or external MAU applications. The device's internal 10Base-T MAU mode allows capacitor coupling between the transceiver and the serial-interface adapter. Other functions include level-shifted data passthrough from one transmission medium to another; collision detection; signal-quality error testing; and automatic detection/correction of polarity reversal on the twisted-pair input. The device provides six status indicators and six LED drivers. LXT902NC, in a 28-pin plastic DIP, $14.97 (1000).

Level One Communications, 105 Lake Forest Way, Folsom, CA 95630. Phone (916) 985-3670. Circle No. 688

Video RAMDAC

- Suits windowing systems
- Has 110- to 170-MHz speed

The Bt463 RAMDAC combines true-color and pseudocolor graphics with hardware windowing functions. The windowing scheme supports arbitrary plane depths on a pixel-by-pixel basis. In addition, the size of each individual color map is variable from 16 to 512 addresses to match the needs of the application program. To identify the individual characteristics for each window, a window-type word accompanies each set of pixel and overlay data. The 4-bit word addresses an on-chip 16 × 24-bit RAM, which provides control to convert pixels from a virtual color-map index to a physical color-map index prior to sending it to the look-up table. The RAMDAC comes in a 169-pin pin-grid array and is available in speed

But all you really need to know is that they're made by NEC, a 24-billion-dollar company, and the fourth largest manufacturer of disk drives in the world. For more information, call 1-800-NEC-INFO.
grades of 110, 135, and 170 MHz. 135-MHz version, $317 (100).

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. FAX (619) 452-1249. TLX 383596.

Circle No. 689

Color Look-Up Table

• Provides 256 colors
• Handles pixel rates to 50 MHz

The SYCl76 look-up table integrates the functions of a 256 x 18-bit color look-up table, three 6-bit video DACs, and an asynchronous, bidirectional µP interface. The look-up table can display 256 colors simultaneously from a palette of 262,144 colors. The on-chip pixel word mask allows the changing of displayed colors in a single write cycle rather than by modifying the color look-up table. Available pixel rates range from 40 to 50 MHz. The device, which has TTL-compatible inputs and outputs, can directly drive singly or doubly terminated 75Ω transmission lines. In a 28-pin, 600-mil DIP, $4; in a 44-pin plastic leaded chip carrier, $4.50 (1000).

Syvanteke Microelectronics Corp, 1475 Saratoga Ave, Suite 150, San Jose, CA 95129. Phone (408) 252-7988. FAX (408) 252-7996.

Circle No. 690

Voltage Regulators

• Include built-in detector
• Current drain is only 3.5 µA

Combining the functions of voltage regulation and detection in one chip, the S-870 and S-88 series can provide extended battery life for portable equipment. The S-870 devices include voltage regulation, voltage detection, and delay circuitry. In addition to these functions, the S-88 devices include short-circuit protection and a power-off circuit. Both series feature a maximum current drain of only 3.5 µA, an operating voltage range of 1 to 15V, and an input-to-output voltage difference of only 0.15V. The output voltage is fixed internally, and detection is set to each output voltage. For an output of 3V ± 4%, five models in each series detect specific voltage ranges from 2.050 to 2.653V. For an output of 5V ± 4%, five models detect voltage ranges from 3.60 to 4.62V. The

All you need to know about 3.5" Winchester disk drives, inside

PC/AT and SCSI Interface

1" Height

56/180MB Capacity

Fast head positioning time 25ms

Power save and spin off mode (wattage as low as 0.5W)

It's nice to know that NEC disk drives have the most advanced technical features. And it's reassuring that they're consistently available, and with a DOA rate of less than 1%, and up to 100,000 hours MTBF rate that they're reliable.
S-870 series comes in a 5-pin SO package, and the S-88 series is available in an 8-pin SO package. S-870, $1.40; S-88, $1.84 (5000).

Seiko Instruments USA Inc, Semiconductor Products Group, 1150 Ringwood Ct, San Jose, CA 95131. Phone (408) 433-3208. FAX (408) 433-3201. Circle No. 691

High-Density Static RAMs
- 2M- and 4M-byte versions
- Have 45- to 100-nsec speeds
A pair of CMOS static RAM modules feature densities of 256k x 8 bits and 512k x 8 bits. Ranging in speed from 45 to 100 nsec, these parts are available in both commercial (0 to 70°C) and military (−55 to +125°C) grades. The operating current of the 4M-byte device is 140 mA max, and standby current is 5 mA max. Included in the devices are an address decoder and internal power-supply bypass capacitors. The static-RAM modules come in 32-pin, 600-mil plastic or sidebrazed ceramic DIPs. The 100-nsec, commercial grade 512k x 8-bit device in a plastic DIP, $395; the 55-nsec, military grade in a ceramic DIP, $1475 (100).

Elmo Semiconductor Corp, 7590 N Glenoaks Blvd, Burbank, CA 91504. Phone (818) 768-7400. TLX 698181. Circle No. 692

Wide-Bandwidth AGC Amplifier
- Signal-channel bandwidth is 160 MHz
- Gain-control bandwidth is 100 MHz
The CLC520 de-coupled amplifier features wide bandwidths and automatic gain control (AGC). The amplifier has a differential signal-channel input, a gain-control input, and a single-ended output. The signal channel features a −3-dB bandwidth of 160 MHz, a linear phase deviation of 0.5° to 60 MHz, and 0.04% signal nonlinearity at 4V p-p output. You can set the gain-control channel, which has a bandwidth of 100 MHz, for gains from 2 to 100 with an external resistor. The gain-control input provides more than 40 dB of voltage-controlled gain adjustment from the maximum gain setting. For example, you can set the amplifier for a maximum gain of 100 (40 dB) for a gain range from 40 dB to <0 dB. Other specifications include a slew rate of 2000V /µsec and −43 dB of feedthrough at 30 MHz. The CLC520 is available in 14-pin plastic and ceramic DIPs. From $9.26 (1000).

Comlinear Corp, 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500. FAX (303) 226-0564. TLX 450881. Circle No. 693

But all you really need to know is that they're made by NEC, a 24-billion-dollar company, and the fourth largest manufacturer of disk drives in the world. For more information, call 1-800-NEC-INFO.
NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

In-Circuit Tester For Circuit Boards
- Upgrades to add functional test capability
- Runs software for IEEE-1149.1 boundary-scan testing

The HP 3073 in-circuit board-test system allows manufacturers to purchase an in-circuit tester initially and, while preserving an initial investment in tester hardware, to upgrade to functional or combina-
tional (in-circuit and functional) testing later. The vendor believes that the addition of this product to its line creates the only tester family that includes both in-circuit and functional-test systems. The system also supports boundary-scan testing on boards designed according to the IEEE-1149.1 standard. A boundary-scan description language facilitates the design of tests for such boards. $205,000.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 801

Automatic Test System For VLSI ICs
- Expands to 512 pins
- Produces patterns at 400M bps/pin.

The 512-pin-max J971 VLSI-device test system has a top clock rate of 200 MHz, but can operate at 400M bps/pin—because each clock period can contain multiple signal transitions on each pin. To boost performance without using the large power supplies or liquid cooling of competitive systems, the vendor has replaced 90% of the ECL timing and data-formatting circuits with CMOS, using ECL only where CMOS can-

All you need to know about 5.25" Semicon disk drives, inside

120MB Full-height 5.25"

SCSI Interface

<.35ms Access time

40MB Half-height 5.25"

4.0MB/Second sustained transfer rate

Up to 220,000 hours MTBF

It's nice to know that NEC disk drives have the most advanced technical features. And it's reassuring that they're consistently available, and with a DOA rate of less than 1%, and up to 220,000 hours MTBF rate that they're reliable.
not provide the needed speed. Despite the limited use of ECL, minimum pulse width is 2.5 nsec, and edge-placement accuracy is ±250 psec. The system is modular in several ways. Not only do you buy pins in groups, but there are plug-in performance upgrades. $600,000 to $4,000,000.

Teradyne Inc, 30801 Agoura Rd, Agoura Hills, CA 91301. Phone (818) 991-2900. FAX (818) 707-2805. Circle No. 802

Tester For Mixed-Signal Devices And Assemblies
• Tests discrete devices, ICs, hybrid modules, and boards
• Handles linear, digital, and mixed-signal units
The SZ-M3600 test unit tests linear, digital, and mixed-signal devices, modules, and pc boards. It can perform digital testing to 50 MHz on units having as many as 256 pins. You can rapidly adapt its switching matrix, DSP capability, and load boards to specific parts. The product is designed for moderate-volume work such as incoming inspection and hybrid-module testing. Because the system is an upgrade of the vendor's smaller, benchtop testers, it can run programs originally developed for those units. The product also accepts card-level instruments to tailor it for specific uses. From $175,000. Delivery, 10 to 12 weeks ARO.

SemiTech International Inc, 56 Roland St, Boston, MA 02129. Phone (617) 628-8880. FAX (617) 628-8778. Circle No. 803

SZ Testsysteme GmbH, Postweg 5, D-8021 Amerang, W Germany. Phone 807 5170. FAX 807 51588. Circle No. 804

80386-Based Data-Acquisition Software
• Can use as much RAM as your computer holds
• Controls data acquisition, manipulation, and display
Viewdac software for data acquisition, and control and data analysis and display uses the full capabilities of the 80386- and 80486-based PCs. The package needs a PC that has at least 4M bytes of RAM, an 80387 coprocessor, 10M bytes of free space on its hard disk, and a display that conforms to IBM's EGA or VGA standards. The package's graphical user interface supports multiple windows and displays virtual instrument panels. You create applications by selecting functions from menus. The descriptions appear in words, however, not as icons. The software supports all memory 80386-based PCs, and the PC's hard
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For more information about how the AT8000A Power Sources and Loads can help you solve your ATE testing needs, call:
1 (800) 73-ELGAR

EDN November 22, 1990
disk can act as virtual memory. Hence, the package can create and manipulate very large data sets. Currently supported hardware includes analog and digital I/O cards from several firms. Through December 31, 1990, $1995; thereafter, $2495.

Keithley Asyst, 100 Corporate Woods, Rochester, NY 14623. Phone (800) 347-0033; in NY, (716) 272-0700. FAX (716) 272-0073.

Circle No. 805

Sun-4-Hosted 680X0 Development Tools

- Support 68020 and 68030 at 33 MHz with no wait states
- Connects to Ethernet using TCP/IP

You can use a Sun-4 workstation as the host for a suite of hardware and software development tools for the 68020 and 68030. The tools include the vendor's EL 3200 and ES 1800 in-circuit emulators and software tool sets named Validate/XEL and Validate/Unison. The EL 3200 supports both of the µPs clocked at 33 MHz with no wait states. It connects to the host via Ethernet using Transfer Control Protocol/Internet Protocol. Validate/XEL provides an ANSI C compiler, an assembler, a disassembler, source- and assembly-language debugging, instruction-set simulation, trace, and a history of commands and aliases. Validate/Unison includes several cross-development tools. EL 3200, from $30,000; ES 1800, from $12,500; Validate/XEL, $10,300; Validate/Unison, $7050.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; (206) 882-2000. FAX (206) 883-3049.

Circle No. 806

PLD Programmer

- Can expand to handle PROMs and microcontrollers
- Has 115k-bps RS-232C port

The logic-only version of the 2900 programming system supports PLDs of all types—programmable

When it comes to scopes, some companies talk a good line.

One company really has it. Designing a few scopes for "average" users leads to a line of average scopes. That's why Tek builds some 20 analog scopes and 24 DSO's. From 10 MHz to 40 GHz. From handhelds to lab scopes. From dependable basics to the advanced signal analysis of the DSA. Want a line with real substance? Call your Tek rep or 1-800-426-2200 for less talk and more Tek.

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array logic devices, generic array logic devices, erasable programmable logic devices, programmable electrically erasable logic devices, and field programmable logic device arrays. The devices can be in DIPs, LCCs or plastic leaded chip carriers (PLCCs). Included are a programming base (a hardware module) for DIPs and a library of programming routines for PLDs having 24 pins or less. You can purchase a PLCC/LCC base, matchbook adapters for different sizes of surface-mount packages, and libraries for the following device categories: PLDs to 28 pins, PLDs to 44 pins, EPROMs and EEPROMs to 44 pins, PROMs to 44 pins, and microcontrollers to 44 pins. Hence, by purchasing libraries, bases, and matchbooks, you can adapt the programmer to most programmable devices. The unit includes 128k bytes of RAM and an RS-232C port that operates to 115.2 kbps. $3995.

Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 882-1043.

Circle No. 807

68030 ICEs
- Three units support 16, 25, and 33-MHz-max clock speeds
- Permit emulation RAM expansion to 4M bytes

The HMI-200 series of in-circuit emulators includes three units that support the 68030 µP. The units perform identical functions, but one lets the µP operate to 16 MHz, another allows 25-MHz operation, and the third permits operation at 33 MHz. All units support real-time emulation with four complex break and trigger points, and all have a pair of 4k×104-bit trace buffers that can record 16 external inputs and a 32-bit time tag. Each unit’s standard emulation memory is 256k bytes, but you can expand the memory to 1M, 2M, or 4M bytes.

The vendor also supplies the Sourcegate high-level-language debugger. It works on code compiled from C, Pascal, Ada, and PL/M. It lets you display the source, assembly language and source, or assembly language only. 16-MHz unit, $13,000; 25-MHz unit, $18,000; 33-MHz unit, $21,000; debugger for IBM PC, $1500; software support for Sun and Apollo workstations, $3000.

Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. FAX (205) 882-6701. TWX 910-600-8258.

Circle No. 808

When it comes to DSOs, some companies aim towards banner specs.

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High Level Of Integration. The TEK-AT1 features an 80C286 at up to 20 MHz with system memory from 512 Kbytes up to 4 MBytes, two serial ports, one parallel port, a watchdog timer, a power failure detector, solid state disks with support for FLASH EPROMS, floppy and hard disk controllers.

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High-Resolution Monitors
- Produce both portrait and landscape images
- Provide 2048 × 2560- and 2560 × 2048-pixel resolution

The UHR-4820-P and UHR-4820-L high-resolution gray-scale monitors produce both portrait and landscape images. These monitors provide 2048 × 2560- and 2560 × 2048-pixel resolution, respectively. The video bandwidth of 500 MHz permits 2000- and 2500-line images to be refreshed 72 times/sec when operating noninterlaced. Improved light-output guns and enhanced CRT yokes produce a brightness of 60 fL at full gray-scale output and 0.25 fL at zero output, resulting in a brightness dynamic range of 240. Both displays use a 21-in. flat screen and feature a blue phosphor for film-like images. The FDP-2111 controller features a high-speed bus for transferring images between a video buffer and a frame buffer. The controller is available for PC/AT, Micro Channel Architecture, VME, and Macintosh computers. UHR-4820-L, $5400; UHR-4820-P, $5900; systems with monitor, controller, and software, from $19,000 (OEM qty). Delivery, 60 days ARO.

MegaScan Technology Inc, 42 South St, Hopkinton, MA 01748. Phone (508) 435-2600. FAX (508) 435-9166. Circle No. 810

Ethernet Controller Board
- Uses Am7990 Lance chip for the VMEbus
- FTP/Telnet protocol allows testing without host computer

The Enet-1 board is an intelligent Ethernet controller for the VMEbus. An AT&T Unix Streams emulator allows the development and downloading of custom protocols for running on a dedicated Ethernet communications processor. The

When it comes to DSOs, some companies duck the tough questions.

One company spells them out.

12 Tough Questions looks beyond banner specs to critical issues most DSO vendors don’t want you to ask. Acquisition, glitch detection, update rate, triggering — Tek’s sales engineers welcome the kind of questions that get to the facts of performance. Want a scope that has nothing to hide? Contact your Tek sales engineer, or call 1-800-426-2200 for a copy of 12 Tough Questions, free.

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Vishay Intertechnology has become a worldwide supplier of resistive devices, stress measurement products and complementary passive components. Now this resource — perhaps unmatched in scope and depth — is identified by a new symbol. It represents the unity and synergy available to you through a network of respected companies organized into four major business units in the electronic components industry and the Measurements Group in the field of stress measurement.

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Dr. Felix Zandman
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board supports thick-wire, thin-wire, or combined thick-wire and twisted-pair Ethernet networks. An optional second Ethernet interface provides redundancy for fault-tolerant or multiple-network applications. You can opt for SCSI and floppy-disk controllers via the company's Apex expansion bus, which connects to the board's 68020 µP. An AMD Am7990 LAN controller chip (LANCE) provides an interface with LANs. The File Transfer Protocol/Telnet Protocol permits testing without a host computer. The board's VIC068 VME-bus interface controller chip has message-passing registers and a DMA controller. The board provides as much as 4M bytes of dual-ported memory.

Radstone Technology, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; in NJ, (201) 391-2700. Circle No. 811

When it comes to DSOs, some companies let you stare at a video.

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The SMP Development Station allows you to implement customized processors with software commands.

For years, development stations for digital systems have been used to evaluate designs before custom hardware is produced. Now the modular SMP Development Station brings that development efficiency to RF and video systems.

The Signal MicroProcessor (SMP) is a software-programmable chip which processes RF and video analog signals with the same versatility and ease that the digital microprocessor processes data. The SMP Development Station is an evolving system of PC-based instrumentation modules that use the SMP as a massively parallel processing engine capable of handling RF and video signals with bandwidths up to 150 MHz. User interface and control of the SMP is provided through powerful and easy-to-use W.A.V.E.® data acquisition and analysis software. W.A.V.E.® runs on any IBM-PC/AT or 100% compatible personal computer.

The first SMP Development Station module is a 128-tap programmable transversal filter (PTF) which is useful for signal generation, extraction, modification and characterization. It has been used to verify the design of an LPI radar system, built-in network analyzers, multipath equalizers, pulse-shaping equalizers, magnetic read-head equalizers, programmable bandpass filters, smart scope triggers, anti-aliasing filters, synthesizers, waveform generators, spread-spectrum matched filters, interference cancellers, target simulators, and pattern matchers for signals and images.

Users can expect to have the SMP Development Station up and running in less than 1 hour.

WAVE® ELECTRONIC DECISIONS INCORPORATED
1776 East Washington Street Urbana, Illinois 61801
(800) 373-3628

CIRCLE NO. 37
as much as 512k bytes of RAM disk with battery backup. Other features include a watchdog timer, two RS-232C ports, a real-time clock with battery backup, a parallel-printer port, and a power-failure detector. A floppy-disk controller controls as many as two 3½- or 5¼-in. disk drives with capacities of 1.44M bytes. The board operates from 0 to 70°C, or from -40 to +85°C on an extended-temperature version. You can install the board in a passive backplane or use it as a stand-alone controller. $875.


Circle No. 813

Industrial PC/AT
- Comes in a 7×7.5×19-in. RETMA rack
- Uses a 16-MHz 80C286 CMOS CPU and 2M bytes of RAM
The MiniDAC SY4286, a half-card IBM PC/AT industrial computer, comes in a 7×7.5×19-in. RETMA rack or panel-mountable enclosure. The system features a 16-MHz CMOS 80C286 CPU; 2M bytes of RAM; an EGA graphics adapter; a 12-slot, 16-bit ISA passive backplane with eight user slots; and a 200W power supply. Other features include a shock-mounted 48M-byte 3½-in. hard-disk drive, a 1.44M-byte 3¼-in. floppy-disk drive, a SCSI host-adapter card, and two RS-232C ports with a printer-interface card. Options include a math coprocessor socket and an optional full card 13½-in. chassis. You only have to add a keyboard, a monitor, application-specific I/O modules, and software. $1995.

Ann Arbor Technologies Corp., Box 3083, Ann Arbor, MI 48106. Phone (313) 995-1360.

Circle No. 814

PC Input Device
- Consists of a glass tablet with 1000×1000 points
- You move the cursor by sliding your finger over the tablet
The UnMouse input device for the IBM PC replaces a mouse or a trackball. The tablet measures 3×4½ in. and remains stationary
You can now stack the deck in your favor. Macintosh has given the electronic designer powerful new tools to work with. And McCAD—the world’s leading desktop engineering software for the Mac—gives you the way to press those advantages when designing PCB’s. Put it all together and you have a CAD system that’s faster and that has more memory, storage and versatility.

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beside the keyboard. To move the cursor, you slide your finger over the glass tablet and click the mouse button by pressing lightly on the tablet. For example, if you touch the tablet in the lower-left corner, the cursor will immediately go to that location on the screen. The tablet has a resolution of 1000 x 1000 points so users can draw figures, annotate documents, or enter signatures. Templates to label keypad functions slide under the tablet’s glass. Twelve of the keypad’s 16 keys are programmed to emulate the PC function keys. The other four keys operate as Shift, Alt, Control, and Enter keys. The device has an RS-232C port, and it comes with a driver for both mouse-driven DOS and Windows programs. $235.

MicroTouch Systems Inc, 55 Jonspin Rd, Wilmington, MA 01887. Phone (800) 866-6873; in MA, (508) 694-9900. FAX (508) 694-9980. Circle No. 815

80386 Single-Board Computer

- As much as 4M bytes of RAM on IBM PC/AT expansion board
- Has controllers for floppy- and hard-disk drive

The Slot Board/386 is a single board computer on an IBM PC/AT expansion board. The board utilizes a 20-MHz 80386 µP and either 1M or 4M bytes of RAM. The board has a floppy- and a hard-disk controller as well as two serial ports, a parallel port, an 80387 socket, and two solid-state disk sockets. A shadow RAM provides fast execution of the BIOS and video display. The board runs on DOS, Unix, QNX, VRTX, OS-9000, and Flexos operating systems. You can expand the capabilities of the board by using the company’s family of MiniModules, which attach directly to the board’s IBM PC/AT bus-compatible header. The board consumes 10 to 12W typ and operates from 0 to 70°C. Board without RAM, $1170 (100).

Ampro Computers Inc, 1130 Mountain View/Alviso Rd, Sunnyvale, CA 94089, Phone (408) 784-2800. Circle No. 816
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

SCSI Manager And Interface For OS/2
- Supports multitasking under OS/2
- Provides interface to OS/2 layered device drivers

The ASW-1420 SCSI Manager software, version 1.21, works with the vendor's Advanced SCSI Programming Interface/2 (ASP/2) to provide multitasking facilities for as many as seven SCSI hard disks and other peripherals under OS/2. The SCSI Manager is essentially bus-independent; it can work with host adapters for the IBM PC/AT, Micro Channel Architecture, and EISA buses. The ASP/2 interface is directly compatible with Microsoft's Layered Device Driver (LADDR) architecture for OS/2. LADDR-compatible drivers are available for the vendor's SCSI-1 and SCSI-2 hard-disk drives. Several other manufacturers provide LADDR-compatible drivers for their tape, DAT (digital audio tape), CD-ROM, and WORM (write once, read many) drives so you can handle these devices under the ASW-1420 SCSI Manager. ASW-1420 version 1.21 costs $100 for a single license; OEMs can also license the object code.

Adaptec, 691 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 945-8600. Circle No. 738

Cross-Compilers, Source-Level Cross-Debuggers
- Work with Z80, 64180, and 6909 microcontrollers
- Support all ANSI/ISO C features

You can obtain Whitesmiths optimizing C cross-compilers and the CXDB source-level debugger for Zilog Z80, Hitachi 64180, and Motorola 6809 microcontrollers. The compilers provide all features of the ANSI/ISO C standard, as well as the vendor's chip-specific language extensions for each chip. These extensions add many low-level assembly-language features to the C-language capabilities so you can maximize use of all the features of each chip in your application. The source-level cross-debugger features a multiwindow user interface; control of target program execution through breakpoints and step control; access to both local and global symbols; and simulated I/O. You can get the debugger in two versions: the simulator version lets you execute and debug target code on a host computer; the emulator version works with several in-circuit emulators on the target system. The compilers run on IBM PCs and

Once it took this to protect 12 lines from surges.
CAE & SOFTWARE DEVELOPMENT TOOLS

compatibles as well as on Sun, Apollo, HP, and VAX/VMS workstations. PC version from $1800. CXDB debugger host version runs on IBM PCs and compatibles; $1500 for either the host or the emulator version.

Intermetrics Inc, 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-1840. FAX (617) 868-2843. Circle No. 739

Interactive Diagramming Tool

- Provides automatic level numbering
- Allows as many as 90 characters per label in any number of lines

The Robochart mouse-driven diagramming tool for IBM PCs and compatibles lets you create data-flow diagrams, flow charts, state-transition diagrams, and other similar documents. The tool automatically performs level-numbering of different nesting levels, and automatically updates objects that are linked across levels to reflect any changes you make. The tool allows as many as 90 characters per label, and you can arrange these in any convenient number of lines. You can copy, cut, or paste both single objects and groups of objects. Pop-up menus and Alt-key shortcuts make the tool easy to learn to use.

It can generate laser-printer output at 300 dpi, or send the output to a variety of graphics dot-matrix printers and pen plotters. $96.

Digital Insight, Dept R1, Box 2095, Evergreen, CO 80439. Phone (303) 674-5232. Circle No. 740

ROM Monitor/Debugger Has Built-In Serial Port

- Provides bidirectional communication through ROM socket
- Built-in driver can run at 115.2k bps

Romport is a hardware device that you plug into the 27XXX ROM socket of an embedded Motorola- or Intel-based microcontroller system. A phone-style connector on the device provides bidirectional serial communication with a host computer or dumb terminal at 115.2k bps. The device comes with a built-

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in communication program that lets you download programs into the system RAM or issue commands to a ROM-resident monitor or application program, then displays the results on the host computer or a dumb terminal. You can plug your own ROM monitor into the Romport, or use the vendor's Est-bug, which lets you set breakpoints, view a code and data trace, examine and change the contents of registers, disassemble machine code, and run menu-driven diagnostics. Est-bug comes with an interface to the Intermetrics (Cambridge, MA) XDB 5.0 source-level debugger. The Romport/Est-bug system will currently work with Intel 8086 and 80186 µPs and with members of the Motorola 68000 family; watch for versions that will work with other target processors. Romport, $495; Romport/Est-bug system, $1095 for a single license. Qty discounts available.

Embedded Support Tools Corp, 10 Elmwood St, Canton, MA 02021. Phone (617) 828-5588. FAX (617) 828-7941.

Circle No. 741

Virus Detector Checks
All Drives

- Scans automatically on cold or warm boot
- Scans whenever you insert a new diskette into a drive

Vi-Spy version 4.0 includes a 3k-byte TSR (terminate-and-stay-resident) component that automatically scans any diskette when you insert it into a drive. Also, whenever you issue a warm-boot command, the program advises you to open the door to drive A, and then it clears memory in order to prevent accidental boot-sector infections. If you’re using a hard disk, running the program from the autoexec file checks all hard-disk drives for all of the known viruses. If the program finds a virus, it tells you which one it found and which files are infected, and it recommends how to remove the virus. $250, includes one year of quarterly updates.


Circle No. 742

Backup System With Data Compression

- Works with four floppy disks as well as tape
- Uses advanced error-correction, data-compression algorithms

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simultaneously. The package includes a formatting routine that can format the floppy disks for 360k, 720k, 1.2M, or 1.44M bytes. The program is menu driven and provides context-sensitive on-line help. The proprietary compression algorithm achieves compression rates of 60% or more, depending on the type of data; error-checking-and-correction (ECC) routines ensure accurate recovery of data in the event of media flaws. An automation feature lets you create backup definitions that you can save on disk and call up from within the program. Alternatively, you can instruct a scheduler to perform these preconfigured backups automatically at specified time intervals, without operator intervention. Details of every backup performed are stored in a history file. $169.

Gazelle Systems, 42 N University Ave, Suite 10, Provo, UT 84601. Phone (801) 377-1288. FAX (801) 373-6933. Circle No. 743

Active-Filter Design Program
- Can analyze an unknown filter and identify its type
- Provides multiple modes of analysis

Active is a software package for the analysis and design of active filters that runs on IBM PCs and compatibles. The design sequence consists of defining the characteristics and performance of the filter you want; analyzing and synthesizing the filter; and determining the topology and component values of the filter. In the definition phase, you can define the location of the poles on the S-plane, specify the passband and stopband attenuation, or define the polynomial equation for the transfer function. In the analysis phase, you can plot the response in the frequency domain or the time domain; a filter recognizer feature can analyze an unknown filter and identify its type, 3-dB points, frequency, ripple, and other characteristics. You can also compare the filter you've designed with a similar, theoretically optimal filter. Finally, you can enter resistor values and let the program calculate capacitor values, or enter capacitor values and let the program calculate resistor values. The program runs with Hercules, CGA, or EGA graphics. $745.

Tatum Labs Inc, 3917 Research Park Dr, Suite B-1, Ann Arbor, MI 48108. Phone (313) 663-8810. Circle No. 744
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Foxboro/ICT, 199 River Oaks Pkwy, San Jose, CA 95134. Phone (800) 428-2224; in CA, (408) 432-1010. Circle No. 678

Power Rectifiers

- Are surface mountable
- Have a 2A current rating

Types PBYP35CT, 240CT, and 245CT Schottky power rectifiers are housed in 6.5 x 3.5 x 1.8 mm SOT-223 surface-mount packages. The devices have a center-tapped pair of diodes. The diodes are matched and each can handle an average current of 1A. Forward voltage drop at 1A measures 0.45V max and leakage current at the diode’s maximum reverse current is 100 µA max. To accommodate the needs of low-voltage switching-power-supply applications, the lines include devices with reverse voltage ratings of 35, 40, and 45V. The rectifiers are supplied on standard 12-mm tape ready for use on pick-and-place equipment. $0.32 to $0.52 (1000) Delivery, stock to eight weeks ARO.

Philips Components, Discrete Products Div, 45 George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500. Circle No. 680
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- **Features 108 pins**
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Tecorp International Inc, 19301 S Santa Fe Ave, Unit 102, Rancho Dominguez, CA 90220. Phone (213) 764-0040. FAX (213) 764-0033.

Circle No. 681

Display Module
- **Displays two lines**
- **Operates under µPC control**
The Model 3601-51-080 vacuum fluorescent module displays two lines of 40 characters. The characters are 0.24 in. high and are configured in a 5 × 7 matrix. In addition to 96 standard ASCII characters, the module displays 75 additional characters, including accented European letters; the module can also display three user-defined characters. Interface to the host is

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**IEE Inc., 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. FAX (818) 902-3723. Circle No. 682**

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- Ratings range to 4A

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*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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