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The new MAN-amplifier series... another Mini-Circuits’ price/performance breakthrough.

<table>
<thead>
<tr>
<th>MODEL</th>
<th>FREQ RANGE (MHz)</th>
<th>GAIN dB</th>
<th>MAX OUT/PWR dBm (typ)</th>
<th>NF dB</th>
<th>DC PWR 12V mA</th>
<th>PRICE $ ea.</th>
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<td>70</td>
<td>15.95</td>
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†† Midband 10f1 to fM/2, ± 0.5dB
† IdB Gain Compression
Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

Mini-Circuits
A Division of Scientific Components Corporation
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Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1 MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its “OFF” state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3n sec switching speed.

---

**SPECIFICATIONS**

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<th>SPECIFICATION</th>
<th>KSW-2-46</th>
<th>ZFSW-2-46</th>
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<td>3(typ)</td>
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<td><strong>above 500MHz</strong></td>
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<td>-5V on. OV off</td>
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---

**Connector versions**

-Packaged in a 1.25 x 1.25 x 0.75 in. metal case.

-Contain five SMA connectors, including one at each control port to maintain 3n sec switching speed.
DESIGN FEATURES

Special Report: Networking software 102

Network operating systems, file-sharing software, and application-development tools simplify the task of designing systems that harness distributed processing power. Using software products such as these, you can even partition an application’s executable code among heterogeneous systems.—Maury Wright, Regional Editor

Decade 90: The future of system design—Part 1 114

Designing systems with the next decade’s increasingly complex chips will require entirely new methodologies and techniques. This article is the first in a 5-part series that will explore the changes already taking place in system design and extrapolate those changes through the year 2000.—Steven H Leibson, Regional Editor

2M-byte diskettes need special tests for quality control 127

The bit density of 2M-byte diskettes is near the theoretical limit for longitudinal recording methods. Careful quality-control testing is therefore critical to error-free use of these diskettes in computer systems.—Jerome L Hartke, Media Sciences Inc

Single-chip µCs solve problems in pattern generation 139

In many applications, the single-chip µC provides a viable alternative to the traditional solutions for pattern-generation problems. The equipment required to apply µCs is inexpensive, and the development cycle for custom pattern generators is short—an attractive combination.—Chris Ghormley, ITT Federal Electric Corp

Modula-2’s design simplifies programming and compilation 147

Designing a computer language is punctuated by a series of tradeoffs and compromises. In designing Modula-2, Niklaus Wirth has achieved a better set of tradeoffs and compromises than has any other language designer.—Brian Anderson, Vancouver Community College

Continued on page 7
The first hermetic optocouplers certified to MIL-STD-1772 are from HP.

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CG08710
TECHNOLOGY UPDATE

You can choose from a variety of data-acquisition and -control boards for your Macintosh II, but you must know your requirements thoroughly to make an intelligent choice (pg 57).

In-circuit emulators ease development of hardware for 80386-based applications

Brand new, or significantly improved, 80386 in-circuit emulators are giving designers more to consider when selecting high-performance µPs for their new designs.—Dan Strassberg, Associate Editor

Gallium-arsenide digital ICs complement ECL families in high-speed applications

If your designs suffer from bottlenecks due to the speed limitations of ECL, you can advantageously add GaAs components to your ECL circuits despite GaAs’s higher costs.—John Gallant, Associate Editor

PRODUCT UPDATE

SMD multilayer varistors

DESIGN IDEAS

Tachometer measures low frequencies
Chopper amplifier stabilizes 3-amp system
Circuit converts pulse train to sinusoid
Pushbutton sequence disarms burglar alarm
Program divides 32-bit by 16-bit numbers

Continued on page 9
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Dept. 112
When doing design work, concentrate on solving the problem, not on using design tools such as CAE.—Jim Williams, Linear Technology Corp

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Engineering jobs in rehabilitation: Highly prized and hard to get.
—Deborah Asbrand, Associate Editor

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Unix in Europe will move full speed ahead...To terminal users, green still means go.

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Sam Shine, Proprietor

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Omron General Purpose Relays include our MY, MK, LY and MJ models.

Shown here are key specifications for some of Omron's most popular power and general purpose relays.

---

### Power Relays

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<th>G5D</th>
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### General Purpose Relays

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<td>UL, CSA, VDE, TUV</td>
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*No NC contacts

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EDN March 3, 1988

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...AND MORE

*Assumes EZ-PRO Development Station connected to MSDOS host.
JUST BECAUSE YOU'VE MADE IT...
...DOESN'T MEAN YOU'VE GOT IT MADE.

With a lot of ASIC vendors, your first prototype is just the beginning of a long journey into design revisions. And after the arduous task of making the thing work, you're still not sure the device can be mass produced.

Unless you're working with Fujitsu.

Because when we produce your prototypes, you can bet they'll meet your performance specs. And you can be absolutely certain you'll be able to produce the device in quantity. And on schedule.

Here's why. We've taken over 8,000 designs from concept through mass production. And over 99% of them have worked the first time. That's right.

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You see, we've been refining our design tools for the past fifteen years. And because they verify your input to worst case specs, as well as scrutinize every detail from spike analysis to bus contention, all the guesswork is eliminated. Our simulations are closely correlated to silicon (with a 99% hit rate). Plus, all prototypes and wafers are tested exactly like production units. So you know what you'll get. Before you get it.

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Combine these failsafe methodologies with our unprecedented quality assurance record, and you've got mass production with the highest quality available. Anywhere.

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How To Wring Workstation-Level

P-CAD's new Master Designer turns an ordinary PC into a full-fledged PCB workstation.

When you need to wring every drop of performance out of your next PCB design, you need Master Designer’s software.

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P-CAD’s Master Designer routes multiple layers simultaneously cutting the number of vias and subnets in half. So you’ll wring out cleaner designs and higher completion rates (up to 100%).

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back annotation, Master Designer also has an ECO processing option.

And Master Designer supports all PCB design technologies. Including SMT, with a library of over 3,300 symbols and 4,600 parts.

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If you're interested in wringing every penny out of your PCB design station instead of wringing your hands, ring P-CAD. Let P-CAD show you how to turn a PC into a high-powered workstation overnight.
If you think all low-cost frequency counters are inferior imitations of precision lab instruments, guess again. Fluke has a new 120 MHz counter that's a perfect fit for test systems, bench tops and budgets.

**Honest performance at only $995.**

The Philips PM 6666 counter delivers seven full digits of resolution at gate times of one second. More than 20 measurement functions. Automatic trigger-level setting. And first-rate input protection to 350V. All packaged in a rugged, shielded metal case.

Add full programmability with the GPIB/IEEE-488 option. A 1.1 GHz input. Or Philips' unique mathematically-controlled crystal oscillator timebase for precise measurements with no warm-up time.

All this performance is backed up by one of the most trusted names in instrumentation: Fluke, with service and support that's never more than a phone call away. So don't take chances. For genuine solutions to fit your test and measurement needs, come to Fluke. For more information and complete specifications, phone 1-800-44-FLUKE ext.77.
INSTRUMENT COMBINES DIGITAL SCOPE WITH LOGIC ANALYZER

The Omnilab 9240 from Orion Instruments (Redwood City, CA, (415) 361-8883) combines a 100-MHz digital storage oscilloscope with a 48-channel logic analyzer. As a digital scope, the instrument samples at rates as high as 204M samples/sec with 8-bit vertical resolution. For repetitive waveforms, the digital scope has an equivalent-time-sampling rate of 680M samples/sec on two channels.

As a logic analyzer, the instrument can support 48 state or timing channels at a 34-MHz clock rate. You can use eight logic-analyzer channels at asynchronous clock rates reaching 204 MHz. The instrument can trigger on state, range, sequential events, and timing or event counters. It permits you to operate 32 logic-analyzer channels and two digital scope channels simultaneously. The Omnilab 9240 uses an IBM PC/AT or compatible computer for control and display. It sells for $8900.—Doug Conner

SOFTWARE TRANSLATES DSP DATA INTO ASCII, HEX, AND BINARY

If you've been looking for a menu-driven PC-based program that can translate and transfer data acquired from digital instruments or incompatible data-acquisition programs, the Universal Translator from HEM (Southfield, MI, (313) 559-5607) may be the program you need. This software package translates data to and from digital-signal formats such as ASCII floating-point, hexadecimal, condensed hexadecimal, and binary formats. According to the manufacturer, the program will work with virtually all data-acquisition and -analysis packages for either input or output data. Its menu-driven format lets you establish input and output parameters. You can store your menu selections to automate repetitive translation tasks. The Universal Translator costs $195.—J D Mosley

FAMILY OF 3½-IN. WINCHESTERS STORES 40M TO 170M BYTES

The Prodrive family of 3½-in. hard-disk drives from Quantum Corp (Milpitas, CA (408), 432-1100) offers 40M- to 170M-byte capacities. You can specify the drives with SCSI (Small Computer Systems Interface), ESDI (Enhanced Small Device Interface), or IBM PC/AT-bus interfaces. The SCSI models include a 64k-byte read-ahead disk cache, and the IBM PC/AT models have a 16k-byte cache. The drives all have 19-msec average seek times. The vendor is shipping the 40M-byte (Model 40S) and 80M-byte (Model 80S) SCSI drives now; they cost $520 and $845 (2000), respectively. The models with the other interfaces and capacities will be available this summer.—Maury Wright

LCD-DRIVER IC HANDLES AS MUCH AS 100V

Designed for dichroic LCDs, the MIC8031 38-bit LCD-driver IC from Micrel (Sunnyvale, CA, (408) 245-2500) can accommodate as much as 100V on the drive circuits while providing a TTL-compatible CMOS interface to your logic circuits. The driver accepts serial data, which is loaded into a latch register on command. The IC's chip-select inputs allow you to use microprocessor control. You can use the on-chip oscillator to provide the backplane signal, or you can cascade multiple devices by employing a master frequency. The device detects the mode you're using and switches its internal dividers accordingly. The MIC8031 comes in a 44-position leadless chip carrier (LCC) specified over the military or industrial temperature range, or in a 48-pin DIP. Prices range from $54.50 (100) for the military-temperature LCC (MIC8031AQ) to $27.90 (100) for the 48-pin DIP (MIC8031CN).—Richard A Quinnell
NEWS BREAKS

VLSI MEMORY-TEST SYSTEM SPECS 100- AND 200-MHz TEST SPEEDS

The first commercially available 100-MHz VLSI memory-test system has been introduced by Advantest America (Lincolnshire, IL, (312) 634-2552). The T5381 Memory Test System performs both lab and production testing of ASICs and dual-port memory devices. With a general-purpose (AG) head in place, the unit provides 100-MHz testing. With an ECL (AE) head, it lets you perform 200-MHz multiplexed testing. The AG head offers 2-nsec output-transition times at 3V p-p; the AE head specs 0.5-nsec output-transition times at 0.8V p-p.

The unit comes with a dual timing generator. The main timing generator provides 24 timing edges, the other generator (the Sub-TG) provides 16. You can, therefore, assign as many as 40 independently programmable timing edges to any pin. The timing accuracy is ±700 psec. The T5381 includes a variety of output waveforms, including multiplexed RZ, NRZ, and XOR. By using two test heads, you can simultaneously test as many as 16 devices; each test head has 160 pins, and you can fit the heads with as many as 12 power supplies and four dc parametric test units. The ATE system costs $3 million to $6 million, depending on the number of heads.—J D Mosley

SYSTEM AUTOMATES FAILURE ANALYSIS FOR ICs

The 370 Failure-Analysis System from Tektronix (Beaverton, OR, (800) 835-9433) automates failure analysis for multipin semiconductor devices. The vendor claims this is the first automated failure-analysis system available for packaged devices with as many as 192 pins. In comparison with manual methods, the vendor says, this failure-analysis system can reduce test times from hours to minutes. The system comprises a Tektronix 370 curve tracer, a TSI 8150 test-system interface, a personal computer, application software, and a test fixture. You select setups from computer-driven screen menus. A 140-pin system, including the personal computer, costs $39,250; delivery is 12 weeks.—Doug Conner

SINGLE-OUTPUT 3000W SUPPLY MEASURES 5×8×13½ IN.

Bonar Powertec (Chatsworth, CA, (818) 882-0004) offers its Model 9R power supplies in 2, 5, 12, 15, 24, 28, 36, and 48V models. Each of these current-mode switchers generates 3000W and fits into a 5×8×13½-in. package, which has the same height and width as the industry-standard 1500W package and is only 4 in. longer. To achieve the 3000W rating, the vendor employs four inverters that operate in parallel. The multiple-inverter design also provides a level of fault tolerance for the systems the supplies are used in. If one of the four inverters fails, the supply can still operate at a reduced power level. For example, a 5V, 600A model can produce 500A with only three inverters operating. The company is shipping samples of the 9R series now; the single-piece price is $1800.—Maury Wright

RESISTIVE-OVERLAY TOUCHSCREEN FITS PS/2 COLOR MONITORS

If you have an IBM PS/2 computer with a Model 8513 analog color display, you can simplify data entry by adding a resistive-overlay touchscreen from Carroll Touch (Round Rock, TX, (512) 244-3500). Each add-on touchscreen unit has an antiglare overlay sensor, a cable, and a controller. Using analog resistive technology, the controller sends the host computer an X/Y-coordinate pair that identifies the exact contact location. The touchscreens cost $360 (100).—J D Mosley
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ETHERNET ANALYZER DETECTS GRADUAL NETWORK DEGRADATION

By allowing you to pinpoint and repair faults on Ethernet (IEEE-802.3) LANs before they cause the network to crash, the NQA network-quality analyzer from Logic Replacement Technology Ltd (Reading, UK, TLX 847395) helps minimize system down time. The analyzer measures the physical (layer 1) and data-link (layer 2) characteristics of the LAN without disturbing normal network traffic. It can also perform in-service time-domain-reflectometer tests.

By correlating the results of protocol analysis and physical-layer testing, the analyzer can pinpoint faults on particular network nodes. Unless you install a software option, the analyzer doesn't decode an Ethernet packet's data, so network security isn't at risk. However, the standard protocol analysis does allow you to build up a source/destination matrix of network activity, monitor individual station characteristics, or obtain general network statistics. The instrument has a touch-sensitive screen, soft-key control menus, and a 360k-byte, MS-DOS-compatible floppy-disk drive for program or data storage. You can choose an optional 40M- or 100M-byte hard-disk drive. The NQA costs approximately $25,000.—Peter Harold

ANGLO-AMERICAN AGREEMENT DEVELOPS HIGH-SPEED ECL GATE ARRAYS

Plessey Semiconductors Ltd (Swindon, UK, TLX 449637; in the US: Irvine, CA, (714) 472-0303) and Applied Micro Circuits Corp (San Diego, CA, (619) 450-9333) have joined forces to develop a new range of high-performance ECL gate arrays. Providing gate counts as high as 14,000 gates, these devices are expected to operate at power levels lower than any currently available ECL arrays. The arrays will be available as military-grade parts qualified to MIL-STD-883C and BS9000. Using Applied Micro Circuits' design and development expertise and Plessey's 1-µm triple-layer-metal HE1 bipolar manufacturing process, the initial parts will incorporate transistors with cutoff frequencies (F_T) in excess of 14 GHz. When manufacture is transferred to Plessey's submicron HE2 process, the transistor-cutoff frequencies will increase to 20 GHz. The first samples of the gate arrays are expected to be available during the fourth quarter of 1988.—Peter Harold

LASER PRINTERS FOR JAPANESE PCs START AT $1538

Japan's Mitsui Corp will introduce two laser-beam printers for personal-computer systems before the end of 1988. The first model, the LaserMate, can print 11 pages/minute. It costs $3615 and is intended for use with NEC's PC98 Series, Fujitsu's FMR Series, and Toshiba's J-3100 Series computers, as well as with the AX-format computers (IBM PC/AT-compatible, Japanese-language computers). The company plans to introduce the LaserMate in April. The low-end model will cost only $1538 (¥200,000) and will be available later this year.—Joanne Clay

TWO CCD IMAGE SENSORS EACH OFFER 2 MILLION PIXELS

NEC and Toshiba Corp have separately announced the development of high-density CCD (charge-coupled device) image sensors having a resolution of 2 million pixels. (The highest grade CCD image sensors that are currently available offer 400,000-pixel resolution.) NEC's sensor uses a conventional silicon substrate; the 16.5×10-mm chip incorporates 1035 vertical and 1920 horizontal effective pixels. The image sensor has a 63-dB dynamic range and a 74.25-MHz readout speed. Toshiba's device, which employs a photoelectric converter layer fabricated from amorphous silicon, has 1920 vertical and 1036 horizontal pixels. Its dynamic range is 72 dB; its readout speed is 74.25 MHz. Both companies plan to have the devices on the market in two years.—Joanne Clay
A STRIKING NEW COMBINATION OF SPEED, RESOLUTION, ACCURACY AND RECORD LENGTH!

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The RTD 710 lets you work with fast transients, from DC to 100 MHz, in standalone, semi-automated or fully automated test and measurement environments.

You can partition its 64K memory to store signals of different lengths. Acquire data simultaneously on two different channels. Switch sampling speeds up to five times in a single acquisition.

Add a TV triggering option for video applications. And choose from a variety of computer-based measurement packages.

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combiners

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With over 150 models, from 2-way to 48-way, 0°, 90° and 180°, a variety of pin and connector packages, 50 and 75 ohm, covering 2KHz to 4200MHz, Mini-Circuits offers the world's largest selection of off-the-shelf power splitter/combiners. So why compromise your systems design when you can select the power splitter/combiner that closely matches your specific package and frequency band requirements at lowest cost and with immediate delivery.

And we will handle your "special" needs, such as wider bandwidth, higher isolation, intermixed connectors, etc. courteously with rapid turnaround time.

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For detailed specs and performance data, refer to the MicroWaves Product Directory, Gold Book, or EEM. Or contact us for our free 64-page RF/IF Signal Processing Guide.
Expand your...
Enhance your design at any stage with RCA CMOS 6805 micros and SPI peripherals.

Your challenge is to increase system performance and capability while reducing board size.
Not an easy job. But certainly easier when you use our 6805 and 68HC05 micros and serial peripheral interface devices.

**Extend your micro's power.**
Many microcomputers rely on parallel I/O ports to communicate with peripheral devices. An inefficient method at best.

That all changes with the serial peripheral interface incorporated into our 68HC05 microcomputers.
This three-wire (plus device select) synchronous, full-duplex, serial communication system contains separate lines for input and output data, serial clock and device select. You don't have to sacrifice I/O ports to communicate off-chip: our 68HC05 micros can communicate with our own serial peripherals, the serial peripherals of other manufacturers, and even with other microcomputers via only three port lines.

**True design versatility.**
The real beauty of the SPI is that it eliminates limitations imposed by microprocessors.

For example, you can easily extend the amount of I/O or memory with SPI RAMs, I/O chips or shift registers. And the modular SPI bus gives you the ability to expand without losing lots of PC-board space. Reduced package sizes and minimized interconnect wiring lead to reduced board size.

And since you don’t need complex software to operate the bus, you save ROM space.

Right now, we can offer you a versatile family of peripheral devices, including 128-byte and 256-byte static RAMs, a real-time clock with RAM, an 8-bit programmable I/O port, and a 10-bit 8-channel A/D converter. And more parts are coming soon, including a digital pulse-width modulator and a serial bus interface chip for networking microcomputers. These serial peripherals are also compatible with other microcomputer types.

**Powerful family of micros.**
We can provide 6805 microprocessors for external memory address, but the heart of our SPI system is the 6805 Series high-speed CMOS microcomputers:

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**Easy to prototype, too.**
If you need another reason to choose our 6805 family, here it is: they’re so easy to prototype with our Piggyback! We have the 68EM05C4 and 68EM05D2 Emulators, custom 40-pin packages that contain the C4/C8 or D2 micros with a Piggyback EPROM socket.

When installed with a 27C64 EPROM, these devices together become functionally identical to a CDP68HC05C4, CDP68HC05C8 or CDP68HC05D2.

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EDN March 3, 1988
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The result is system throughput that's way ahead of anything else in the VME world.

Think about the possibilities for real-time applications. For the first time, you can squeeze every ounce of performance from every processor. With no wasted overhead. And no stalls. But that's only the beginning. The newest
you a different competition.

member of the VME/PLUS family, CPU-32, comes with EPROM, so there's no license required and no extra charge. CPU-32 also includes full support for real-time operating systems and UNIX 5.3. What this new technology means for you is unprecedented levels of speed and system throughput, exceptional reliability and - here's the best part - lower total system cost. And if that's not enough, we also offer a full set of off-the-shelf peripheral boards and software. All VMEbus compatible. And guaranteed to cut the wait states out of your design cycle.

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Behind the scenes of the standards process

The January 7 editorial ("Standards aren't always standard," pg 47) brought out some interesting points about standards and cautions on their use. I'm involved in standards development within my company and the IEEE. The process is fascinating but not without its problems.

Good standards are necessary but tough to produce. Producing a good standard requires knowledge of the environment in which it's to be used and limitations on its complexity. Keeping these guidelines in mind, systems of standards can be built to complement each other and to specify more complex functionality as it's needed. With this approach, individual documents remain tractable, and worldwide consensus is achievable in a reasonable length of time.

Good examples of this process are the ISO (International Organization for Standardization) OSI (Open Systems Interconnection) 7-layer model and the various ISO protocol standards built around it. Another example, and one that I've been involved with, is the IEEE-488.2 protocol standard that builds on the IEEE-488.1 bus standard. Yet another emerging standard with a lot of industry interest is the VXI Bus specification, building on the VME and Eurocard standards.

Another important aspect of workable standards is testability. Testing doesn't necessarily imply that a standard is deficient. It merely means that the standard has defined a required functionality but not a specific implementation. This procedure is necessary in order to give the standard stability and a lifetime that will allow the underlying technology to change.

It's difficult, if not impossible, to completely test a given implementation against a standard. But comprehensive testing can, and does, assure a higher probability of successful interoperation in the intended environment. Testing is a necessary function in the implementation of standards and has to be kept in mind as standard development proceeds so that clear, reasonable, and testable parameters are called out.

Bob Cram
Tektronix Inc
Beaverton, OR

Omission

MetaLink Corp was omitted from the company listing at the end of the article, "HLL cross compilers speed 1-chip software development" (December 24, pg 126).

For more information, contact:
Dave Yeskey
MetaLink Corp
Box 1329
Chandler, AZ 85244
(800) 638-2423;
in AZ, (602) 926-0797
TLX 4998050

Right product, wrong company

The January 7 Special Report on real-time operating systems incorrectly identified on page 123 the manufacturer of the FlexOS family of operating systems. Digital Research makes the FlexOS system.

The correct address is:
Digital Research Inc
4401 Great America Parkway,
Suite 200
SantaClara, CA 95054
(408) 982-0700

Digital Equipment Corp overlooked

I read with great interest the Special Report on real-time operating systems by Charles Small (January 7, pg 114). I could not help but notice his truly well-written and up-to-date treatment of the subject, and his omission of Digital Equip-
PMI's OP-44 also guarantees a 15 MHz GBW and full power BW of 1.5 MHz. And no compromises on accuracy...

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The OP-44 is available now ... in 883 too. Get the high-speed facts from our 12-page OP-44 data sheet. Circle the reader service number or call 1-800-843-1515.

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___ Please send me ____ Designer's Kit(s).
___ Please send more information.

Name ____________________________________________________________
Title ____________________________________________________________
Company __________________________________________________________
Address __________________________________________________________
City __________________ State ______ Zip _____________________________

*Pricing subject to change

EDN March 3, 1988

SIGNALS & NOISE

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___ Please send more information.

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Title ____________________________________________________________
Company __________________________________________________________
Address __________________________________________________________
City __________________ State ______ Zip _____________________________

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CIRCLE NO 3

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<table>
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<th>Characteristics/Logic Families</th>
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<th>HS-CMOS (74HC Series)</th>
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<tr>
<td>Prop. Delay Time (typ) GATE (CL = 15pF)</td>
<td>3.5ns</td>
<td>8ns</td>
<td>9ns</td>
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<tr>
<td>Max. Clock Freq. (typ) R-P-P (CL = 15pF)</td>
<td>150MHz</td>
<td>60MHz</td>
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<tr>
<td>Quiescent Power Diss. (typ GATE)</td>
<td>0.01µW</td>
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<td>Noise Margin Y/1Hz (min) (IL(max))</td>
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<tr>
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<tr>
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<td>2.4V</td>
<td>1.75-5.25V</td>
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*Data believed to be accurate and representative of each logic family.

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**CALENDAR**


Southcon, Orlando, FL. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 722-2965. March 8 to 10.


Modern Electronic Packaging (seminar), San Diego, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. March 15 to 17.

Microelectronic Packaging and Surface Mounting (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. March 18.

10th Annual Conference for Inventors and Entrepreneurs, Denver, CO. Rocky Mountain Inventors Congress, Box 4365, Denver, CO 80204. (303) 443-3818. March 18 to 19.

Compstan '88 (Computer Standards Conference), Arlington, VA. James Hall, National Bureau of Standards, Technology Building, Rm B266, Gaithersburg, MD 20899. (301) 975-3273. March 21 to 23.

Neural Networks for Artificial Intelligence, Arlington, VA. Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. (213) 394-8305. March 21 to 23.


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Spectrum

EDN March 3, 1988

CIRCLE NO 133
CALENDAR

Visualization Science in Engineering and Computing, Arlington, VA. American College of Radiology, Box 2348, Merrifield, VA 22116. (703) 648-8961. March 30 to April 1.

AFCEA (Armed Forces Communications Electronics Association)/Northern Virginia Chapter Annual Conference: Forecast to Industry, Arlington, VA. Gale Nellans, AFCEA/Northern Virginia Chapter, Box 5267, Springfield, VA 22150. (703) 971-9000. March 31 to April 1.


Microcircuit Interconnections and Assembly Methods (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 7.

Electrostatic Discharge (ESD): Concern or Over-concern? (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 12.

Hybrid Microcircuit Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 18.

Features:
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Product Description:
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Product Highlights:
1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Long-term stability is excellent and the CD and TD versions are 100% tested and guaranteed for 25 parts-per-million stability in a 1000-hour period.
3. Output noise of the AD588 is very low—typically 46μV p-p. A pin is provided for additional noise filtering using an external capacitor.
4. Precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than ±1μV and a fine-trim is available for applications requiring exact symmetry between the ±5V and ±5V outputs.
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GUEST EDITORIAL

BY JIM WILLIAMS, STAFF SCIENTIST, LINEAR TECHNOLOGY CORP

Should Ohm’s law be repealed?

When I was a kid, I lived near the Stearn family. They had a pool, shuffleboard and tennis courts, dogs, and a horse. They also had billiard tables, a pinball machine, and a darkroom. But what interested me most was what Dr Stearn had in the basement. There, sitting on a “scopemobile,” next to his workbench, was a Tektronix 535 oscilloscope. To say that I loved that oscilloscope is an understatement.

The pure, unbounded lust I spent towards this machine probably retarded the onset of my puberty, delaying sexual nascency by at least a year. It also destroyed my school performance. I read the mainframe manual instead of doing homework, and studied the small, easily hidden plug-in book in English class. I knew every 535 specification and all its operating modes. I lived for the 535, and I studied it. But, best of all, I used it.

Dr Stearn shared his electronics hobby—and his 535—with me. Oscillators, amplifiers, flip-flops, modulators, filters, RF stages—we circuit-hacked them all with ferocious intensity. And with the scope you could see what was going on. You shared the excitement Leeuwenhoek felt when he looked into his microscope.

The Tektronix 535 was a sublime masterpiece. In 1956, it was vastly superior to its competition. The triggered sweep worked unbelievably well, and the calibrated vertical and horizontal amplifiers really were calibrated. The scope had an astounding 15 megacycles (it was “cycles” then) of bandwidth, and it had something called “delayed sweep.” The plug-in vertical preamplifiers greatly increased the measurement capability. Using that scope inspired confidence that bordered on arrogance. It would make my circuits work, or so I thought.

One afternoon I couldn’t get a circuit to operate properly. The signals looked about right, but the performance was shaky, and odd effects abounded. I tested everything, but got nowhere. When Dr Stearn came by he listened, looked, and thought for a while. Then he moistened two fingers, and moved his hand around the circuit, lightly touching points as he watched the scope. He noticed effects and correlated them to his hand movements. When the scope’s display looked good he soldered a small capacitor between the last two points his fingers touched. To my amazement, the circuit now worked properly. I was dumbfounded and, probably because of my frustration and embarrassment, even a little angry.
Dr Stearn explained that my circuit was oscillating at perhaps a hundred megacycles, and he suspected he'd damped it by loading the right points. His finger dance had surveyed suspect points; the capacitor was his equivalent of the finger-loading capacitance. "That's not fair!" I protested, "You can't see 100 megacycles on the scope." He looked right at me and spoke slowly. "The circuit doesn't care about 'fair,' and it doesn't know what the scope can't see. The scope doesn't lie, but it doesn't always tell the truth." He then gave me a little lecture that has served me well, except when I'm foolish or frustrated enough to ignore it:

"Don't ever get too attached to a way of solving problems. Don't confuse a tool, even a very good one, with knowledge. Concentrate on understanding the problem, not applying the tool. Use any tool that will help move your thinking along, know how these tools work, and keep their limitations in mind—it's part of the responsibility of using them. If you stop thinking and stop asking questions and simply believe what the scope says, you're done for. When you do that, you're not listening to the problem, and you're no longer designing that circuit. When you substitute faith in an instrument, no matter how good it is, for your judgment, you're in trouble.

"It's a tricky trap; sometimes you don't even know you're falling into it. People are very clever at fooling themselves that way. We all want things to be simple and to go smoothly, but the circuit doesn't know that and it doesn't care." That lecture took place 32 years ago, and I'm still absorbing the advice.

Lately, I've been hearing a lot about CAD systems, computer-based workstations, and powerful software-modeling techniques. At Linear Technology, we have CAD systems, and they save tremendous amounts of time. They're very powerful tools, and we're learning to use them efficiently. It's a tough process, but the rewards are worth the effort.

Unfortunately, there are substantive and disturbing differences between what these tools are, and what some purport them to be. Promotional materials, which are admittedly suspect, boast of speed, ease of use, and the elimination of mundane and odious design tasks. Advertising explains the ease of generating ICs, ASICs, board functions, and entire systems in weeks, even hours. Reading further reveals the paths to this design nirvana—databases, expert systems, models, simulators, compilers, emulators, and a lot of other intellectual frou-frou.

Somewhere, such technological manna must coalesce to eliminate messy labs, pesky nuts and bolts, and, above all, those awful breadboards. Headaches vanish, fingers and the lab remain clean, the boss is thrilled, and you have time to go fishing. Well, such silliness is all part of the marketing game, and it's well known wherever money changes hands. Perhaps my acerbic musings are simply the fears of a bench hacker or a
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cantankerous computer technopeasant who is confronting the Computer Age. But I don't think so, because what I see doesn't stop at fast-talking ad copy.

Some universities are enthusiastically emphasizing "software-based" design and "automatic-design" procedures. Students and professors have shown me circuits they designed on their computers. Some of the assumptions and simplifications the design software makes are unusual. Some of the circuits are unusual, too.

Such excessively spirited CAD advocacy is also found in industry trade journals that have become enamored of CAD methods to the point of being cavalier. Articles tell readers how easy it is to use CAD tools. At times, you can't distinguish editorial copy from advertising. For example, a recent editorial entitled "Electronic design is now computer design" informs me that:

"For the most part, the electronic details—the concerns of yesteryear about Ohm's law and Kirchhoff's law, transconductance or other device parameters—have been worked out by a very select few and embedded in the software of a CAE workstation or buried deep within the functionality of an IC. Today's main-stream designers, whether they're designing a complex board-level product or an IC, don't need to fuss with electronics. They're mostly logic and system designers—computer designers—not electronics designers" (Ref 1).

Those ideas pave the road to intellectual bankruptcy, and they display the kind of arrogance Dr Stearn warned me about. CAD is being oversold, and it shouldn't be, because it's one of the most powerful tools ever developed for solving problems. But if too many users are led astray and disappointed—as some already have been—CAD-system purchases, acceptance, and use will slow. Thus, the irresponsible, self-serving advisories of some CAD vendors and enthusiasts may be partially self-defeating.

The associations being made between CAD tools and the actual generation of ideas based on knowledge and thought are specious, arrogant, and dangerous. They're arrogant because in their determination to streamline technology they simplify it, and Mother Nature loves to throw a surprise party. Technologically driven arrogance can be hazardous, as any Titanic passenger would tell you. They're dangerous because it's easy to confuse faith in tools with the true thinking and simple sweat that are integral to design. In our rush to design
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circuits and systems efficiently, we will cede the judgmental, inspirational, and even accidental processes that constitute much of engineering. At the same time, we'll eliminate excellence.

Most good designs are characterized by how the designer deals with the exceptions and imperfections. In my field, linear circuits, just about everything is an exception. You know about—or think you know about—a lot of the exceptions, but you're constantly learning about new ones. Unfortunately, you can get circuits to work properly without even realizing the exceptions and imperfections that are present. How sad it is that you could do better if only you knew what those exceptions and imperfections were. The linear-circuit designers I admire are those most adept at recognizing and negotiating with the exceptions and imperfections. Often they're not sure just what the specific design issues will be, but they have a marvelous sense of balance. They know when to be wary, when to use finesse, when to hack, and when to use computers. These people use CAD tools to produce superior work more efficiently, while others may be tricked into using CAD to produce mediocre designs efficiently.

CAD tools and techniques, although in their infancy, will indeed prove to be some of the most useful electrical-engineering tools ever developed. Although their usefulness in linear-circuit design is limited at present, they have had an impact on digital-IC and -system designs. For now, the best analog simulator we have is a breadboard. If you're listening, the answer, or at least the truth, is there.

I'm reasonably certain that breadboardless linear-circuit design is a long way off. I suspect the situation is similar for most engineering disciplines. The uncertainties, the surprises, and the accidents that yield fruitful results require sweat and laboratories. CAD saves time and eliminates drudgery. It can increase efficiency, but it does not eliminate the cold realities involved in making something work.

Where I work we bank on our ability to ship products that work properly. We believe in CAD as a tool, and we use it. We also use decade-resistor boxes, breadboards, oscilloscopes, pulse generators, alligator clips, screwdrivers, Ohm's law, and moistened fingertips. Like Dr Stearn back in 1956, we concentrate on solving the problem, not on simply using a tool.

Reference

1. Williams, Tom, “Electronic design is now computer design,” Editorial I/O (a Computer Design newsletter), January 1988, pg 1.
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A COMPANY WITH CHARACTER AND DRIVE
Vendors offer a range of data-acquisition and -control boards for the Macintosh II

Doug Conner, Regional Editor

With the right data-acquisition and -control board plugged into one of its six Nubus expansion slots, the Apple Macintosh II can perform almost any data-acquisition and -control task you could expect of a desktop system. The 68020-based system, which comes with a 68881 floating-point coprocessor, can support fast data acquisition as well as perform rapid analysis of collected data. At least five manufacturers offer a variety of data-acquisition and -control boards and software for the Macintosh II. Table 1 gives the key specs for a representative sample of these boards. To choose the right board for your application, you must know your data-acquisition and -control requirements thoroughly.

Sampling and throughput

One of your first considerations in choosing a data-acquisition board should be the sampling rate. If you require rates greater than 150k samples/sec, your choices are limited to just a few boards. Further, even if you do find a board that samples at a high enough rate for your purposes, your system's throughput might suffer if you try to maintain a high sample rate for millions of measurements.

The Macintosh II's Nubus allows any board to become a bus master, having direct access to the 1M to 8M bytes of memory resident on the mother board. This scheme lets the system maintain high throughput rates even without requiring large onboard data buffers, provided that the data-acquisition board is capable of performing the DMA transfers.

For high A/D-conversion speeds, consider Data Translation's Pegasus Series boards and GW Instruments' MacAdios II board. The Pegasus Series boards can provide sampling rates as high as 750k samples/sec. When you plug an optional high-speed module into the MacAdios II, the data-acquisition board can convert as many as 833k samples/sec. (Without the module, the MacAdios II converts 142k samples/sec.) Both the Pegasus Series and the MacAdios II have 12-bit resolution and can maintain their speeds while transferring data to system RAM, but they substantially tie up the Macintosh II's computing power because they lack DMA capability.
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To free up your computer while performing data acquisition, you can use National Instruments' real-time system-integration bus, which allows you to connect your National Instruments data-acquisition and -control boards to one of the company's DMA boards. The Nubus supports DMA transfers to 37.5M bytes/sec, freeing the Macintosh II's processor to perform foreground tasks, even data reduction, while data acquisition takes place in the background.

Applications in which you sample multiple channels may require that the channels be sampled simultaneously. In such applications, you'll not only need multiple S/H amplifiers; you'll need to be sure they can be synchronized. Some applications may also require the synchronization of digital or analog outputs as well as analog inputs. A number of the available boards can synchronize functions on a single board. National Instruments goes further—its real-time system-integration bus allows you to synchronize the A/D and D/A conversions across multiple boards in the Macintosh II.

**Getting the accuracy you need**

Once you've determined your sampling rate and synchronization needs, you'll need to determine the resolution and accuracy you require. Most data-acquisition and -control boards have A/D and D/A converters with 12- to 16-bit resolution, but you should examine the boards' accuracy specifications carefully. Just because a board uses a 12- or 16-bit D/A or A/D converter doesn't mean that the voltage readings or outputs are accurate to these values. For example, "16-bit accuracy" means that 1 LSB is equivalent to 153 µV on a 10V range. It takes careful design to achieve this kind of accuracy, and you'll have to exercise care to keep noise out of the input signal. Not every application will demand this much accuracy, but the incremental changes provided by 16-bit resolution can be useful in control and other applications.

Most boards require some type of calibration to achieve their specified accuracy. Ideally, a board should use an onboard reference to calibrate itself. Some boards allow you to check the calibration against an onboard reference voltage. In any case, the manufacturer should furnish you with a clear method of measuring the accuracy of the boards. Some boards require calibration, while others come with an onboard reference voltage.

### TABLE 1—REPRESENTATIVE DATA-ACQUISITION AND -CONTROL BOARDS FOR THE APPLE MACINTOSH II

<table>
<thead>
<tr>
<th>MANUFACTURER AND MODEL</th>
<th>MAX CONVERSION RATE (SAMPLES/SEC)</th>
<th>INPUT CHANNELS</th>
<th>INPUT PROTECTION</th>
<th>MAX CONVERSION RATE (SAMPLES/SEC)</th>
<th>RANGES</th>
<th>SETTLING TIME FOR A FULL-SCALE OUTPUT (µSEC)</th>
<th>Channels</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA TRANSLATION DT 2221-F</td>
<td>12 150k</td>
<td>16 SE, 8 DIFF</td>
<td>±35V OR ±20V NON</td>
<td>12 5</td>
<td>JUMPER: 0 TO 10V; ±5V, ±10V, ±2.5V, ±5V, ±10V</td>
<td>2 16 I/O</td>
<td>$1995</td>
<td></td>
</tr>
<tr>
<td>GW INSTRUMENTS MACADIOS II</td>
<td>12 142k</td>
<td>16 SE, 8 DIFF</td>
<td>±35V OR ±20V NON</td>
<td>12 9</td>
<td>JUMPER: 0 TO 10V; ±10V</td>
<td>2 8 INPUT, 6 OUTPUT</td>
<td>$1290</td>
<td></td>
</tr>
<tr>
<td>NATIONAL INSTRUMENTS NB MIO-16H</td>
<td>12 91k</td>
<td>16 SE, 8 DIFF</td>
<td>±35V OR ±20V NON</td>
<td>12 40</td>
<td>JUMPER: 0 TO 10V; ±10V</td>
<td>2 8 I/O</td>
<td>$1495</td>
<td></td>
</tr>
<tr>
<td>SCIENTIFIC SOLUTIONS LAB MASTER II-100</td>
<td>12 125k</td>
<td>16 SE, 8 DIFF</td>
<td>±35V OR ±10V NON</td>
<td>12 5</td>
<td>JUMPER: 0 TO 10V; ±10V</td>
<td>2 24 I/O</td>
<td>$1250</td>
<td></td>
</tr>
<tr>
<td>STRAWBERRY TREE COMPUTERS ACM 2-16-8A</td>
<td>16/12 225/25k</td>
<td>8 DIFF</td>
<td>±50V OR ±50V NON, ±150V FOR 1 SEC</td>
<td>12 35</td>
<td>JUMPER: 0 TO 10V; ±10V, ±50V</td>
<td>2 8 I/O</td>
<td>$1790</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- SPG = SOFTWARE-PROGRAMMABLE GAINS
- SPR = SOFTWARE-PROGRAMMABLE RANGES
- DIF = DIFFERENTIAL
- OP = OPERATING
- NON = NONOPERATING

EDN March 3, 1988
determining whether a board meets its accuracy specification.

To get the maximum accuracy out of an A/D converter, you may need to scale—amplify or attenuate—the signal before conversion takes place. Data-acquisition boards normally have at least one unipolar and one bipolar range. These reference voltages are usually jumper selectable. In addition, a software-programmable gain stage typically provides gains of 1, 2, 4, and 8 or 1, 10, and 100. Unless you'll always be using one voltage range, it's a good idea to choose a board on which the ranges you'll use regularly are software programmable.

If your application requires you to change voltage ranges while measuring different channels, you may be interested in a channel-and-gain-list feature, which some of the boards available for the Macintosh II have. This feature allows you to program the hardware to step repetitively through a series of channels and gains. Because the channel and gain changes are taking place on the fly, you don't have to interrupt the data-acquisition process for channel or range-change instructions.

You may also have to scale the board's analog outputs to meet your requirements. In addition, you'll need to know what current your application requires and what current the board can deliver. Most boards furnish between 2 and 15 mA of output current. If you're using a voltage output, but require more current drive than the board can supply, you'll need to add an external power buffer.

Even if a board does meet your current-drive requirements, line resistance may cause an unacceptable drop in voltage. Some boards provide voltage-sense feedback, which lets you deliver the correct voltage at the load. The voltage-sense feedback also allows you to add an external power buffer without incurring additional voltage-offset errors.

Most data-acquisition boards provide multiplexers that allow one A/D converter to service eight or 16 inputs. Some vendors offer options that allow their boards to accommodate more inputs. GW Instruments' GWI-Mux plug-in modules, for example, allow the company's MacAdios II to accommodate as many as 112 single-ended or 66 differential inputs. Choosing a board that meets your needs will allow you to monitor a number of external lines without having to add external multiplexers.

Most input multiplexers accommodate differential inputs, which are useful for reducing noise pickup.
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Access to the right technology

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TECHNOLOGY UPDATE

and ground-loop problems. When measuring signals over long lines or in noisy environments, you can use currents rather than voltages to transmit data. Currents are less sensitive than voltages to noise pickup and resistive drops in a line. A 4- to 20-mA current loop is the industry standard for this purpose, and many current-loop transducers are available. An added benefit is that the transducers are normally powered by the current loop, so the transducers require only two wires for signal and power. If you'll be using current-loop transducers, you should check whether your data-acquisition board will accommodate the current loop, or whether you'll need to use external circuitry to perform signal conditioning.

The type of A/D converter that a data-acquisition board uses will also affect the noise-rejection characteristics of the board. If your application requires a conversion rate higher than about 10k samples/sec, you'll probably need to choose a board with a successive-approximation A/D converter. Boards that have lower conversion rates sometimes use integrating A/D converters.

If a board's A/D converter is a successive-approximation type, any change in the input during the conversion cycle will add directly to the conversion error. To avoid this error, the manufacturer normally places an S/H amplifier in front of the A/D converter. In contrast, integrating A/D converters can average voltage changes over the entire conversion cycle, so they provide excellent noise-filtering performance. For example, Strawberry Tree Computers' ACM 2-16 board has a 16-bit integrating A/D converter that lets you filter out 60-Hz line noise by converting the signal over one power-line cycle.

Even if the waveform you're sampling doesn't have an appreciable amount of noise, it may have frequency components that are too high for your sampling rate. Anti-aliasing filters can limit the bandwidth of the incoming signal to no more than half the board's sample rate. If your data-acquisition board doesn't supply an anti-aliasing filter, you may need to add an external one.

It's also a good idea to consider how you can protect your data-acquisition board from damaging voltages. For analog inputs, the safe voltage range is typically ±35V when the power is on and ±20V when the power is off. Most boards come with protection against voltages in that range. If your application is likely to involve voltages greater than those, it's probably worthwhile to invest in additional protection to avoid the risk of destroying the board. In extreme cases, you may need to provide optical isolation of inputs.

If your application calls for digital I/O in addition to analog signals, you might be able to find a board that also supports the digital signals. Some of the data-acquisition and -control boards for the Macintosh II have dedicated input or output digital lines; others have programmable I/O lines.

Some manufacturers configure their data-acquisition boards to make certain measurements easy, and some offer options that help you complete a measurement setup quickly. For example, Strawberry Tree Computers produces a number of data-acquisition boards that already have cold-junction compensation and linearization for 10 thermocouple types. In addition, the company offers an optional isothermal terminal block, which reduces

For more information . . .

For more information on the data-acquisition and -control boards discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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TLX 981446
Circle No 716

GW Instruments Inc
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Cambridge, MA 02141
(617) 625-4996
Circle No 717

National Instruments Corp
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Austin, TX 78727
(512) 250-9119
TLX 765747
Circle No 718

Scientific Solutions Inc
6225 Coebrum Rd
Solon, OH 44139
(216) 349-4930
TLX 696692
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thermocouple errors where the leads connect.

If you use a data-acquisition board that's made to work directly with the types of signals or transducers you'll be using, you'll not only avoid adding external circuitry but you may find that the board manufacturer has already developed the application software you need. For example, GW Instruments offers the MacSpeech Lab II software for the MacAdios II. The software lets you perform such operations as FFTs and spectrograms, and it provides other analysis tools tailored specifically for speech analysis.

When considering data-acquisition boards, don't forget to pay careful attention to the available software. You may end up spending more money on the software than on the board itself. If you can find an application program that meets your needs, you'll spend a lot less time getting your data-acquisition and -control task running. GW Instruments, National Instruments, and Strawberry Tree Computers all offer application software for their boards.

Fortunately, the Macintosh II forces anyone who writes application programs to conform to a number of standards in order to use Apple's Toolbox software-development tools. These standards mean that all application programs for the Macintosh II will have many similarities, so you won't need an inordinate amount of time to become familiar with them. If you can't find an application program that meets your needs, you'll have to write your own program, using I/O routines supplied by the manufacturer of the data-acquisition board. In that case, you must make sure that the manufacturer's I/O routines are compatible with the language you're using.

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Article Interest Quotient
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High 509 Medium 510 Low 511

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* Processors supported by Microtek: 80386, 80286, 80186, 8086, 8088, 8008, 68020, 68010, 68000, 6809, 6809E, 6502, 280, ASC800, 8085, 8032, 8051, 8034, 8048, 8049, 8050, Z8, SUPER 6, 68HC11, 64180, 80515.

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In-circuit emulators ease development of hardware for 80386-based applications

Dan Strassberg, Associate Editor

Brand new, or significantly improved, 80386 in-circuit emulators (ICEs) are giving designers more to consider when selecting high-performance µPs for their new designs. Hardware designers, in particular, use ICEs to debug the circuits and microcode in target systems that surround µPs. Until now, however, some manufacturers have felt that the capabilities of the available 80386 ICEs have compared unfavorably with those of ICEs used with the 68000 series. These vendors feel that the new, more capable 386 emulators, together with the pervasiveness of 80386-based personal computers (which, they claim, make ideal development platforms for 386-based products), will greatly increase the percentage of dedicated 32-bit applications using the 386.

If you use the number of sockets filled as the measurement of success, Intel Corp’s 80386 is currently leading the pack of high-performance µP chips. The 386’s lead is the result of its overwhelming popularity in high-end personal computers and low-end workstations. But, if you look at the number of design starts for dedicated systems where unit volumes are usually modest, Motorola’s 68020—and now the 68030—are out in front.

Is it a 386 or a fast 8086?

Unless you just want to use it as a faster version of the 16-bit 8086, you need to take advantage of the 386’s protected mode. This mode can allow you to address more than 1M byte of memory while avoiding segmentation of memory into 64k-byte chunks, and it even lets you tap the chip’s full 32-bit power by utilizing all of the new instructions and built-in support for multitasking.

Until recently, Intel was alone in offering an 80386 in-circuit emulator with protected-mode support—the ICE-386. What was the only other 386 ICE, Microtek International’s Mice-32/80386, has, until recently, supported only the 386’s real mode. That mode allows the 386 to handle but a single task. Microtek ICEs are distributed exclusively in the US by Northwest Instrument Systems (NWIS).

Designers of high-performance systems can now base their products on the 386 knowing that they can turn to several sources for development tools that support the full range of the µP’s features. The short list of 80386 ICEs recently grew with the announcement of a new competitor, the HyperIce-386 from Microcosm, a company that has been building ICEs since 1982. Microcosm says that in June, the HyperIce-386 will support protected mode.

In addition, Microtek has announced that its 386 ICE now supports the chip’s protected mode. The protected-mode upgrade, included in all units shipped since February, involves replacing two pc boards and retesting the emulator. Installation takes less than a week, and NWIS will perform it free for US customers who return older emulators.

During 1988, other vendors of ICEs and development systems will announce products that support the 386. Because designers want to use more of the 80386’s capabilities than they can in the chip’s real mode, you can expect new 386 in-circuit emulators to support protected mode at their introduction, or very shortly afterward.

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spec'd for operation at three maximum clock frequencies—12.5, 16, and 20 MHz. There have been persistent rumors that Intel would announce a version spec'd for operation with a 24- or 25-MHz clock, but as of this writing, the only available chips in this range have been “manufactured” by performance-hungry users who have selected “hot” chips from lower-speed production lots.

Because of the unavailability of bona-fide faster-than-20-MHz chips, ICE manufacturers must use selected chips to prove that their products do indeed support clock rates above 20 MHz. Microtek and Microcosm, however, have taken different approaches to this verification question. Microcosm simply states that its emulator supports 25-MHz operation. Microtek claims that although it designed its units for 24 MHz, it won't guarantee 24-MHz performance until it can conduct tests using parts Intel specs to operate at the higher speed.

Who was that masked bit?

It's no mean feat to design an in-circuit emulator that can perform real-time monitoring of the memory and I/O transfers of a µP clocked at or near 25 MHz. (Real time—in ICEman parlance—means without inserting µP wait states.)

If, during debugging, a processor must drive a cable it doesn't normally drive, connecting an ICE can create its own set of problems. One such problem is “ground bounce.” If a large number of processor I/O lines go low simultaneously, the sudden change in current flowing through the inductance of the probe cable’s ground conductors can cause spikes with an amplitude of several volts on the µP's ground pin. If an emulator connects a µP to chips that do not also “see” the spikes, the system will probably misbehave, and device damage may occur.

To head off cable-related problems, vendors are using more active circuits in the probe, the part of an ICE that plugs into the target µP.

### Key Specs for Three In-Circuit Emulators for the Intel 80386 µP

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Intel ICE-386 MAX DESIGN</th>
<th>Microtek(1) MICE-32/80386</th>
<th>Microcosm HYPERICE-386</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Tested</td>
<td>16 AND 20</td>
<td>24</td>
<td>25 (1)</td>
</tr>
<tr>
<td>Max Tested</td>
<td>16 AND 20</td>
<td>24</td>
<td>25 (1)</td>
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<table>
<thead>
<tr>
<th>Wait States</th>
<th>At Max Tested Speed</th>
<th>With Target Memory</th>
<th>With Overlay Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>6</td>
<td>2</td>
<td>2</td>
<td>0</td>
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<tr>
<td>6</td>
<td>2</td>
<td>2</td>
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<table>
<thead>
<tr>
<th>Hardware Pipeline Mode</th>
<th>Debug Registers</th>
<th>None</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>2</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Probes Height Above Target Socket</th>
<th>IBM PC/AT, 1M TERMINAL OR COMPUTER (1)</th>
<th>TERMINAL OR COMPUTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2 IN.</td>
<td>1.375 IN.</td>
<td>1.05 IN.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overlay or Emulation Memory (Bytes)</th>
<th>BASIC 128k</th>
<th>256k</th>
<th>128k</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX</td>
<td>128k</td>
<td>1M</td>
<td>1.6M</td>
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<table>
<thead>
<tr>
<th>Triggering</th>
<th>Hardware Breakpoints</th>
<th>Software Breakpoints</th>
<th>No of Counters</th>
<th>State Machine?</th>
<th>No of Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Breakpoints</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>Y</td>
<td>4</td>
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<tr>
<td>Software Breakpoints</td>
<td>16</td>
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<tr>
<td>No of Counters</td>
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<tr>
<td>State Machine?</td>
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<tr>
<td>No of Levels</td>
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<table>
<thead>
<tr>
<th>Activity Monitored</th>
<th>Address (Bits)</th>
<th>Data (Bits)</th>
<th>Status (Bits)</th>
<th>Logic Probes (Bits)</th>
<th>Register Contents?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>32</td>
<td>32</td>
<td>8</td>
<td>8</td>
<td>N</td>
</tr>
<tr>
<td>Max</td>
<td>32</td>
<td>32</td>
<td>8</td>
<td>8</td>
<td>N</td>
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<table>
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<tr>
<th>Tracing</th>
<th>1/Code Branch</th>
<th>0</th>
<th>0</th>
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<tbody>
<tr>
<td>Wait States Added at Max Tested Speed</td>
<td>2k</td>
<td>2k</td>
<td>8k</td>
<td></td>
</tr>
<tr>
<td>Buffer Depth (Frames)</td>
<td>104</td>
<td>32</td>
<td>16</td>
<td></td>
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<tr>
<td>Nonintrusive?</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>Buffer Width (Bits)</td>
<td>32</td>
<td>32</td>
<td>134</td>
<td></td>
</tr>
<tr>
<td>Items Recorded (Bits)</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Address</td>
<td>32</td>
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<tr>
<td>Data</td>
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<tr>
<td>Status</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td></td>
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<tr>
<td>Logic Probes</td>
<td>16</td>
<td>8</td>
<td>16</td>
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<tr>
<td>Trace Control</td>
<td>None</td>
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<tr>
<td>Time Stamp</td>
<td>24 (%)</td>
<td>32</td>
<td></td>
<td></td>
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<tr>
<td>Pipeline Dequeue</td>
<td>N</td>
<td>Y</td>
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<table>
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<tr>
<th>Languages Supported</th>
<th>ASM, PLM, C</th>
<th>None (10)</th>
<th>ASM, PLM, C</th>
</tr>
</thead>
</table>

| US Price with Probe                 | $16,000 (11)  | $17,000   | $17,500       |

**Notes:**

1. NORTHWEST INSTRUMENT SYSTEMS IS THE EXCLUSIVE US DISTRIBUTOR FOR MICROTEK EMULATORS.
2. 25-MHz versions of the 80386 are currently obtained by customer selection. When Intel ships 24- or 25-MHz parts they may or may not perform identically with the selected devices.
3. None at 16 MHz. Above 16 MHz, debug registers.
4. RS-232C OR PARALLEL INTERFACE.
5. HARDWARE EXECUTION BREAKPOINTS PERFORM SAME FUNCTION BUT WORK IN ROM AS WELL AS RAM.
6. You can trigger on register contents by writing a macro and operating the emulator in single-step mode.
7. VIA RECOGNIZABLE CONDITIONS (TRACK POINTS) IN SOFTWARE.
8. 1 TO 65,536 CLOCK CYCLES. START/STOP WHEN BRANCH, JUMP, OR TASK SWITCH CHANGES PROGRAM FLOW.
9. CAN RESOLVE TIME INTERVALS FROM 10 µSEC TO 4.4 HOURS.
10. DOES NOT SUPPORT HIGH-LEVEL-LANGUAGE DEBUG DIRECTLY, BUT UNIVERSAL SYMBOLIC DEBUGGER SUPPLIED IS COMPATIBLE WITH OBJECT FILES CREATED FROM HIGH-LEVEL SOURCE.
11. OPTIONAL PROTECTIVE MODULE AVAILABLE.
socket. Placing a µP close to all of the devices it communicates with eliminates the effects of ground bounce by equalizing the ground potentials on all of the communicating chips.

In fact, Microcosm has placed overlay memory (also called emulation memory) in its probe and makes extensive use of surface-mount technology to limit the probe size. Microcosm points out that in most target systems, headroom above the board containing the µP is restricted by an adjacent board. Placing the processor board on an extender to gain room for a tall ICE probe can be impractical because high-speed logic boards are notoriously intolerant of the additional capacitance and inductance that extenders introduce.

Arrays add flexibility

Another feature of the Microcosm probe is its custom, 8000-gate, high-speed CMOS arrays which implement the trigger logic. These devices permit considerable flexibility in qualifying trigger conditions. For example, among the things that Microcosm claims the HyperIce-386 can do is bypass the 386's internal debug registers. Programmers will frequently use these registers during normal system operation even though they are not supposed to do so. According to Microcosm, competitive emulators don't operate correctly if the target system program uses the debug registers, whereas the HyperIce-386 does.

At clock speeds as high as 16 MHz, the HyperIce-386 also allows you to set breakpoints and halt emulation on the contents of registers—an extremely handy capability during debugging.

Hardware spoken here

In their current state of development, 80386 in-circuit emulators appear to be best suited for use by designers with a good grasp of both the hardware and software disciplines. Though the symbolic debuggers that accompany the ICEs support object code compiled by several compilers from source code written in high-level languages, and although you can control the emulators with macros or procedures reminiscent of those in C, effective use of the debuggers requires an understanding of assembly language as well as an appreciation of what the hardware is supposed to be doing. If you program only in a high-level language and never concern yourself with the contents of specific memory locations, be prepared to work yourself up a steep learning curve when you first use an 80386 ICE.

Source-level debugging in high-level languages is on the way, though it is unclear when it will arrive or how complete a solution it will offer. Because the kind of debugging you do with an ICE is very dependent on the target-system hardware, it’s hard to imagine debugging with tools that completely isolate you from the hardware.

It’s a new ball game

To minimize the amount of memory consumed by their code and to maximize execution, designers of dedicated applications using older, less capable chips frequently integrated the operating-system and application-program functions. The designers of the 80386 clearly envisioned application programs run-
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UPDATE

Using an active probe, Microtek's Mice-32/80386 permits operation of the target system with a 20-MHz clock. It operates in several modes, without inserting additional wait states.

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Circle 99 on reader service card
Gallium arsenide digital ICs complement ECL families in high-speed applications

John Gallant, Associate Editor

If your designs suffer from bottlenecks due to the speed limitations of ECL, you can advantageously add GaAs components to your ECL circuits despite GaAs's higher costs. Most digital GaAs devices provide input and output ports that are voltage compatible with popular ECL product lines (see box, "Take care when evaluating GaAs/ECL compatibility").

Gallium arsenide, with its intrinsic high electron mobility and semi-insulating properties, has long held promise as a high-speed digital technology. For much of the past 20 years, however, digital GaAs ICs had remained R&D curiosities because of manufacturing difficulties. But digital LSI/MSI GaAs devices became commercially available in 1984, and the number of products continues to grow. In addition, manufacturers are providing standard cells, gate arrays, and foundry services for producing custom devices.

Most GaAs devices find use in military applications, such as electronic warfare and radar systems. Such a system usually consists of an RF front end that converts received signals to baseband frequencies for digital signal processing. Because GaAs devices operate at frequencies that extend into the gigahertz region (silicon bipolar devices, such as ECL, are limited to about 500 MHz), the basebands can have very wide bandwidths. In fact, a GaAs system's high-bandwidth baseband can eliminate the need for an IF-conversion stage—and such a stage's cost.

Not all GaAs digital devices find their way into military products. The Cray III supercomputer (de-
signed for better than 10G-flops operation—more than eight times the performance of the 1.2G-flops, silicon-based Cray II) employs custom GaAs logic cells (fabricated at a Gigabit Logic foundry). In addition, GaAs laser-diode drivers are providing gigahertz bandwidths in fiber-optic communication circuits.

Diverse logic blocks

In 1984 Gigabit Logic and Harris Semiconductor introduced the first GaAs SSI circuits for the commercial market. Since these introductions, these vendors' GaAs offerings have evolved into standard MSI logic families. Devices in these families have loaded gate delays ranging from 100 to 150 psec and clock and data rates exceeding 2 GHz.

For example, the $150 (100) HMD-11016-1 IC from Harris is a binary counter that provides divide-by-2, -4, and -8 outputs when operating with clock frequencies from dc to 2 GHz. The ECL- and GaAs-compatible device has an asynchronous master clear and enable function, which permits the chip to be used as a down counter. The device comes in a 32-pin metal flatpack package and operates from -55 to +85°C.

Gigabit Logic continues to add MSI and LSI devices to its Pico Logic family. The 35-member family uses depletion-mode MESFETs in a source-coupled FET logic (SCFL) configuration similar to ECL.

One recent addition is the 16G040 clock- and data-recovery circuit, which interfaces with Gigabit's 10G041 time-division demultiplexer IC. The $194 (500) 16G040 contains the analog and digital circuitry necessary to implement a complete phase-locked loop for clock extrac-
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- Enhanced interrupt handling: 8 programmable priority levels, hardware context switching for 8 register banks, 8-channel macro service controller.
- 256-byte RAM, 16K-byte ROM on-chip; ROM-less version available.
- Two stand-by modes: halt and stop.
- Package: 84-pin PLCC.
tion from an NRZ data stream, and it contains the circuitry necessary for data retiming and regeneration (Fig 1).

The chip requires an external resonator (such as a ¼-wavelength tunable microstrip stub) for the on-chip VCO. The device comes in a C-leaded or leadless chip carrier for data rates to 800 M bps. An unpackaged die operates to 2.4 G bps, as does a hybrid module containing all external components and tuned to a specific user frequency.

Other additions are the $59.50 (100) 10G100, a 1.3-GHz expandable 4-bit adder, and the $55.00 (100) 10G101, a 1.4-GHz carry-look-ahead generator. These devices can perform 16-bit addition in 2.06 nsec. The devices operate from 0 to 85 °C and come in 40-pin leaded or leadless chip carriers.

Tachonics Corp serves as an alternate source for Gigabit's Pico Logic line. In addition, Tachonics is developing several of its own products, which integrate digital and MMIC products on the same chip. A prescaler, a comparator, and a switch driver are under development.

Triquint Semiconductor and NEC are also supplying standard GaAs logic ICs. Triquint's Q-Logic standard product line, which uses depletion-mode GaAs MESFETs, includes a 3-GHz, 4-stage ripple counter; a 1-GHz, 4-stage synchronous up/down counter; a 2-GHz, 4/5 dual-modulus divider; several 2-GHz multiplexer and demultiplexer devices with 4:1, 8:1, and 16:1 multiplexing capabilities; and 1.2-GHz, 12:1 multiplexer and demultiplexer devices. The devices use a BFL (buffered FET logic) configuration and interface with the 10K and 100K ECL families. They come in either IC flatpack or surface-mount packages. Prices range from $81 (100) for the dual/modulus divider to $298 (100) for the 12:1 demultiplexer.

NEC's standard GaAs product line, which uses depletion-mode GaAs MESFETs, includes a 3-GHz, 3-input NOR/OR gate; a 3.2-GHz D-type flip-flop; a 4.5-GHz T-type flip-flop; a 2-GHz, 4-stage ripple counter; 4:1 multiplexer and demultiplexer devices that operate to 2.5 GHz; and a 2-Gbps decision circuit that consists of an amplifier followed by a D-type flip-flop on the same substrate. The ECL-compatible devices come in hermetically sealed ceramic packages. Prices start at $160 for the NOR/OR gate, $170 for the T-type flip-flop, and $180 for the D-type flip-flop.

Multiplexers and demultiplexers that operate at speeds to 2G bps in optical transmission equipment are becoming available from Oki Semiconductor, which plans to have 2:1 and 4:1 multiplexer and 1:2 and 1:4 demultiplexer devices available in the spring. A 2-chip set will cost about $1250.

Anadigics also offers MSI GaAs parts. Its 4:1 frequency divider, the ADV3040, operates from 1 to 4 GHz. That device boasts a -130 dBc/Hz single-sideband phase-noise spec at a 10-kHz offset from the carrier. Prices range from $50.75 to $184 (100), depending on commercial or military grading.

LSI conserves real estate

GaAs digital ICs are not just limited to SSI and MSI logic functions. Many products with LSI complexity are available. For instance, Vitesse Semiconductor Corp sells a 4-bit µP, a microcontroller, and a static RAM. The devices use an enhancement/depletion-mode (E/D-mode) MESFET process (see box, "GaAs logic uses E MESFETs and D MESFETs").

The Vitesse µP is the $50 (100) VE29G01; it has a 14-nsec read/write cycle and is functionally equivalent to the Am2901C from Advanced Micro Devices (Sunnyvale, CA). The VE29G01 consists of a 16-word×4-bit dual-port RAM and a 4-bit ALU with associated shift...
ing, decoding, and multiplexing circuitry.

Vitesse's $90 (100) VE29G10A microcontroller, which achieves a 12-nsec min clock-cycle time, is functionally equivalent to AMD's Am2910A. It contains a 9-word x 12-bit stack and can address as much as 4K words of microinstruction.

The VE29G01 and VE29G10A are compatible with 100K ECL signal levels and have $V_{\text{REF}}$ inputs for adjusting to 10K and 10KH ECL signal levels. The devices use a single, 2V power supply and come in either a 52-pin leaded or leadless chip carrier.

The $165 (100) VS12G422E is a 256 x 4-bit static RAM with 3-nsec access time. It has inputs and outputs that are compatible with 100K ECL drive levels, and it requires only a single -4.5V power supply.

It operates from -55 to +125°C and comes in a 24-pin DIP that's pin compatible with the 100422 ECL RAM. A 5-nsec access-time version costs $83 (100).

GaAs RAMs are available from Gigabit Logic as well as from Vit-

**Take care when evaluating GaAs/ECL compatibility**

You can employ GaAs devices along with such ECL devices as those in Motorolla's (Phoenix, AZ) MECL 10K and 10KH families and National's (South Portland, ME) 100K line. These families, whose general characteristics are shown in Table A, contain devices that range from SSI logic functions to MSI functions such as registers, adders, multipliers, multiplexers, and RAMs. Level translators provide interfaces to TTL and CMOS families. (Introduced last year, Motorola's Eclips ECL family, whose flip-flop toggle rates reach 600 MHz, includes versions that are compatible with 10KH or 100K devices.)

The drive voltage levels (Fig A) of these families are similar, but not identical, and you must heed the differences when attempting to mix and match technologies or families. For example, some GaAs products purport to be ECL compatible but leave it up to you to determine which ECL family they're compatible with.

Moreover, you'll have to consider more than signal swing when evaluating compatibility. For example, Gigabit Logic's Pico Logic family furnishes output signal swings that exceed the input levels required by any ECL family. However, certain ECL parts require that the input voltage ($V_{\text{IH}}$) be no more positive than -0.6V; therefore, you might have to use some voltage-level shifting scheme when interfacing such parts with the Pico Logic family.

---

**TABLE A—CHARACTERISTICS OF THREE ECL FAMILIES**

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>10K</th>
<th>10KH</th>
<th>100K</th>
</tr>
</thead>
<tbody>
<tr>
<td>GATE PROPAGATION DELAY (nSEC)</td>
<td>1.5 TO 2</td>
<td>1</td>
<td>0.75</td>
</tr>
<tr>
<td>OUTPUT TRANSITION TIME (nSEC)</td>
<td>2.5 TO 35</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>FLIP-FLOP TOGGLE SPEED (MHz)</td>
<td>125 TO 200</td>
<td>250</td>
<td>400 TO 500</td>
</tr>
<tr>
<td>GATE POWER (mW)</td>
<td>25</td>
<td>25</td>
<td>40</td>
</tr>
<tr>
<td>SPEED-POWER PRODUCT (pJ)</td>
<td>37 TO 50</td>
<td>25</td>
<td>3</td>
</tr>
</tbody>
</table>

**Fig A—The transfer characteristics of the most popular ECL logic families have differences that must be accounted for when you interface them to GaAs devices.**
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esse, and Ford Microelectronics has a 64×1-bit dual-ported static RAM under development.

Available now is Gigabit's 12G014, a 256×4-bit static RAM that specs a 2.5-nsec read/write cycle time. Designed for high-speed cache applications, the device has pipelined input and output latches. The $99 (500) device requires three power supplies (nominally 5V, −3.4V, and −5.2V) and comes in either a 40-pin leadless or C-leaded chip carrier.

Many companies that offer standard GaAs product lines also offer standard-cell libraries for custom and semicustom designs. The standard-cell libraries consist of basic logic functions (inverters; NAND, NOR, and OR gates; latches; and flip-flops, for instance) and I/O cells that provide GaAs, ECL, CMOS, and TTL compatibility. The HMS standard cell library from Harris has approximately 40 cells. The cells use depletion-mode MESFETs in the company's BFL configuration. The customer can use CAE/CAD tools, based on software from Silicon Design Automation (San Jose, CA), which are portable and function on all major Unix-based engineering workstations. A 1-µm GaAs process, called Digi-2, provides gate propagation delays of 120 psec min

**GaAs logic uses E MESFETs and D MESFETs**

Gallium-arsenide process technology has progressed since the first GaAs digital ICs were introduced commercially in 1984. The more mature products are fabricated with depletion-mode (D) MESFETs. The basic FET consists of a metal gate placed between a source and a drain region. The transistor is formed in two ion-implantation steps: One places a shallow implant below the gate region to form the channel, and the other forms the source and drain regions. An n-doped depletion region under the gate of a D MESFET allows current to flow between the source and drain when no voltage is applied to the gate. Therefore, the device is normally on. A negative gate voltage causes the depletion layer or channel to narrow, reducing current flow until a gate voltage is reached at which current flow is pinched off.

In an enhancement-mode (E) MESFET, the region under the gate is doped so that the channel is pinched off when no voltage is applied to the gate. A positive voltage applied to the gate initiates current flow. D MESFETs have advantages over E MESFETs in that they can handle more current, tolerate larger signal voltages, and provide faster speeds. However, they use more power than E MESFETs because they are normally on. E MESFETs are more complicated and expensive to fabricate, but their lower power consumption makes them attractive.

Manufacturers of digital GaAs devices are now fabricating devices with D MESFETs and E MESFETs on a single chip to take advantage of the properties of each device. These devices are known as enhancement/depletion (E/D) MESFET devices. Chip designers use the two MESFET configurations to maximize the performance of logic blocks.

Some typical logic blocks are shown in Fig A. The buffered FET logic (BFL) scheme (a) uses D MESFETs exclusively to create a 2-input NOR logic cell. The diode is necessary to level-shift the output voltage to drive succeeding logic cells. In the capacitor-buffered FET logic (CBFL) scheme (b), a reverse-biased large-area diode is placed across the level-shifting diode to act as a speed-up capacitor. The direct-coupled FET logic (DCFL) scheme (c) places two E MESFETs at the source of a D MESFET to create a 2-input NOR gate. The scheme takes advantage of the positive and negative thresholds of the respective FETs so that level-shifting diodes are not required. The low-power FET logic (LPFL) scheme (d) uses an E MESFET and a level-shifting diode as an output buffer.
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In addition to SSI cells, Gigabit Logic’s SC1 GaAs standard-cell library contains a number of MSI cells, such as a 3:8 decoder, a 4-stage synchronous counter, and a 4:1 multiplexer. The cells have loaded gate delays from 50 to 150 psec and operate efficiently from 1 to 2 GHz. (Tachonics will become the second source for this library; its first SSI cells should be available by the end of this month.)

The SC1 cell family is compatible with the Pico Logic family so that users can convert breadboard designs to standard cells. Engineering workstations sold by Mentor (Beaverton, OR) and VLSI Technology Inc (San Jose, CA) support the cell libraries. A delivery of final prototypes occurs 16 to 26 weeks after the company receives schematics. Gigabit quotes a typical NRE cost of $75,000 for a 1000-gate, 1-GHz prototype.

Triquint’s Q-Logic standard cells also contain MSI functions such as encoders/decoders, multiplexer/de-multiplexers, counters, dividers, and prescalers. Users can design and simulate ASIC ICs on Daisy (Mountain View, CA) and Tektronix (Beaverton, OR) CAE workstations. A development schedule from design completion to delivery of prototype parts is typically 10 to 14 weeks. Prices are typically less than $250 (1000) each. Typical standard-cell NRE charges range from $55,000 to $65,000 for single circuit designs.

Shortening development time

Some manufacturers of digital GaAs products offer gate-array packages that give the designer flexibility along with shorter turnaround times and lower NRE costs than do standard-cell implementations. Vitesse Semiconductor has two GaAs gate arrays that allow the user to develop designs on either Mentor or Daisy workstations.

One array, the VSC1500, features 1500 2-input NOR equivalent gates. A structured-cell approach combines both high-speed logic cells and low-power cells, which lets the user obtain an optimum speed-vs-power tradeoff. A macro cell library defines the cell-interconnection patterns for a D flip-flop, with a 2-GHz toggle rate, that dissipates 45 mW or a D flip-flop, with a 500-MHz toggle rate that dissipates 4.1 mW. The array contains 84 high-speed cells and 592 low-power cells. Its 22 ECL inputs and 20 ECL outputs are compatible with 100K and 10KH signal levels. The array requires -5.2V and -2.0V power supplies.

The other gate array from Vitesse, the VSC4500, contains 4500 2-input NOR equivalent gates. D-type flip-flops with 1-GHz toggle rates dissipate 1.8 mW, and NOR gate delays are typically 160 psec. The array’s 120 I/O cells can interface with either TTL or ECL signal levels. The chip’s ECL I/O levels are compatible with 100K and 10KH levels, and the device requires only a -2V power supply when interfacing with ECL only. Both of the Vitesse gate arrays come in 0 to 70°C and -55 to +125°C versions. The VSC1500 and the VSC4500 cost from $200 to $300 (1000). NRE costs range from $55,000 to $70,000 for 10 prototype units.

Gain Electronics Corp offers a GaAs gate-array family with 1700, 3500, and 6000 2-input NOR equivalent gates: the GFL1700, GFL3500, and GFL6000, respectively. The GFL3500 features 864 internal logic cells and 140 I/O buffer cells. Each of the internal cells can be configured as four 2-input NOR equivalent gates. A macro cell library can interconnect the cells to configure a J-K flip-flop that clocks at 1 GHz and dissipates less than 6.9 mW. Unloaded gate delays are typically 150 psec for NOR functions. A design cycle, from logic entry to final mask tape, can be performed on an Apollo (Chelmsford, MA) or Mentor workstation. The output cells are compatible with ECL, TTL, and CMOS levels, and the device only requires a -2V power supply when interfaced with ECL devices. Typical NRE costs to develop customer-designed prototypes are $35,000, $50,000, and $75,000 for the GFL1700, GFL3500, and GFL6000 arrays, respectively.

Triquint’s TQ3000 gate array is a 3000-equivalent-gate array for designs with clock rates to 1 GHz. The company designs and develops ASICs that meet a customer’s dc and ac specs. Typical designs have 500 to 2500 logic gates and as many as 64 I/O lines. Typical engineering development cost for customer-designed prototypes is $77,000.

Ford Microelectronics Inc has a GaAs gate array consisting of 561 internal NOR gates that can be configured with one, two, three, or four inputs. Fabricated in a GaAs E/D process, the 21G06 gate array uses diode-FET-logic (DFL) circuitry. Thirty-four 100K ECL-compatible I/O pins can be configured as input, output, or bidirectional cells. A design kit is available for Daisy workstations. The array comes in a 48-pin ceramic leadless chip carrier that operates from 0 to 70°C. The gate array costs $540 (100) with a typical NRE charge of $75,000 for 10 prototype units.

Ford has designed some standard products with its gate array that are available in 48-pin packages. The 21G06-0003 consists of an independent 8:1 multiplexer and a 1:8 demultiplexer. Multiplexing and
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demultiplexing speeds range from dc to 700 MHz. The $225 (100) device dissipates 0.8W max. The 21G06-0002 is an 8-bit flow-through multiplier that yields a 16-bit result in 8 nsec in a data-setup mode and in 10 nsec in a synchronous mode. The $250 (100) device dissipates 1.1 W typ.

Foundry services

Customers seeking a viable GaAs vendor for fabrication of their own designs can employ various vendors' foundry services. When using the foundry service that Harris provides, for example, customers can use the supplied HMS cell library, circuit models, and layout rules. If you prefer to design your own standard cells or do a full custom layout, a MESFET model and circuit simulator are available through use of a Harris version of Spice called Slice. Alternately, customers may use a compliant FET model of their own choice. Once the design is completed, the customer prepares a tape for mask making. Harris then manufactures the device using either its Digi-1 or Digi-2 process. A full range of MIL-spec screening and radiation testing is available.

Gigabit's foundry services include training seminars, which allow customers to structure a design to meet their requirements. Customers have four process options to choose from: the depletion-mode MESFET (D-MODE), the low-power depletion-mode MESFET (LPD), the enhancement/depletion-mode MESFET (E/D), and the high-margin enhancement/depletion-mode MESFET (E/D). When a design is complete, the circuit layout data stored on magnetic tape or the actual masks are sent to the company for device fabrication.

Vitesse Semiconductor and Ford Microelectronics have agreed to provide alternate sourcing for foundry production of custom LSI, E/D GaAs ICs. Ford provides a set of layout design rules with information on layer definitions, mask polarities, and critical dimensions for designing with its E/D process. The company employs a circuit simulator, called Gassim, that runs under VAX/VMS version 4.2 or later and is based on Spice2G.5. The GaAs MESFET model is based on the Curtice (Ref 1) MESFET model with modifications to allow gate and channel current flow in either direction.

ITT's Gallium Arsenide Technology Center (GTC) offers foundry services to selected customers who are experienced in GaAs design techniques. GTC produces a range of GaAs chips and modules for military applications. The facility focuses on applications where both analog and digital functions are combined on the same chip.

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PRODUCT UPDATE

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Though small in size, the MLV multilayer varistors can protect sensitive I/O signal lines from voltage spikes caused by ESD, lightning, nuclear-electromagnetic pulse, or other transient phenomena. Precise control of the device's zinc oxide grain size and structure plus multilayer construction create devices with well-defined, repeatable breakdown voltages determined by design instead of by lot selection and testing.

The vendor offers varistors with two voltage ratings, with typical breakdown voltages of 7.8 and 18.5V and maximum clamping voltages of 15.5 and 30V, for logic and automotive applications, respectively. You can obtain the product in two case styles: a 1206 surface-mountable package and a conformally coated, axial-lead device. Varistors of either voltage rating absorb peak currents of 200A. The 1206 SMD absorbs 0.45J, and the axial-lead component absorbs 0.8J. Both package styles exhibit inductances of 1.7 nH. The SMD style exhibits 3.0 nF of capacitance, and the axial device exhibits 1.5 nF.

Though a 7.8V breakdown voltage may seem high for protecting 5V logic signals, most IC inputs and outputs incorporate ESD protection circuits that withstand transients of 500V or more. So limiting voltage transients to less than 16V keeps these spikes well below the devices' safety margins. In addition, the varistor safely dissipates very high energy levels, which could destroy an IC's ESD-protection circuits through heating effects.

The company says that the MLV's characteristics compare favorably with comparable protection devices, namely single-layer, metal-oxide varistors (MOV's) and zener diodes. In particular, the 1206-sized MLV can absorb four and a half times more energy than an 1812-sized MOV and about the same amount of energy as an 1812-sized zener diode with similar breakdown voltages. The MLV's 200A peak current rating greatly exceeds the MOV and zener diode ratings of 25A and 62.5A, respectively.

The SMD and axial-leaded versions of the MLV cost $0.49 and $0.54 (10,000), respectively.

—Steven H Leibson
AVX Corp, Box 867, Myrtle Beach, SC 29577. Phone (803) 448-9511. TWX 810-661-2252.
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Available in either 1206-sized SMD or axial-lead packages, the MLV multilayer varistor protects signal lines by clamping transient voltages and absorbing as much as 200A of transient current.

EDN March 3, 1988
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Of all the new products covered in EDN’s December 24, 1987, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN’s Express Request service, or refer to the indicated pages in our December 24, 1987, issue.

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When you plug the VBAT VME Bus-anomaly trigger board into an unused slot in a VME Bus-based system, it can monitor all activity on the bus (pg 76).
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Burr-Brown.
Circle No 603

ACCELEROMETERS
Model 3021 piezoresistive, full-bridge, silicon-based sensors monitor acceleration, vibration, and shock (pg 110).
IC Sensors Inc.
Circle No 602

SECURITY SYSTEM
The DS1207 Timekey is a postage-stamp-size security system that enables software developers and publishers to lease their products for a predetermined time period (pg 163).
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| | One Octal Transparent Latch 3-State |
| | One Octal D-Type Flip-Flop 3-State* |
| | One Octal Transparent Latch 3-State (Inverting) |
| | One Octal Inverting Transparent Latch 3-State |

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<th>6-10 weeks</th>
<th>11-20 weeks</th>
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<td>Toroidal</td>
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<td>36</td>
<td>36</td>
<td>21</td>
<td>0</td>
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<tr>
<td>Pot-Core</td>
<td>0</td>
<td>33</td>
<td>47</td>
<td>20</td>
<td>0</td>
</tr>
<tr>
<td>Laminate</td>
<td>0</td>
<td>40</td>
<td>30</td>
<td>30</td>
<td>0</td>
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</table>

| CONNECTORS | | | | | |
| Military panel | 0 | 0 | 63 | 37 | 0 |
| Flat/Cable | 10 | 55 | 20 | 15 | 0 |
| Multi-pin circular | 7 | 14 | 43 | 36 | 0 |
| PC (2-piece) | 8 | 23 | 54 | 15 | 0 |
| RF/Coaxial | 17 | 44 | 28 | 11 | 0 |
| Socket | 17 | 52 | 22 | 9 | 0 |
| Terminal blocks | 14 | 50 | 23 | 13 | 0 |
| Edge card | 5 | 52 | 33 | 10 | 0 |
| D-Subminiature | 9 | 57 | 26 | 8 | 0 |
| Rack & panel | 7 | 43 | 36 | 14 | 0 |
| Power | 0 | 72 | 14 | 14 | 0 |

| PRINTED CIRCUIT BOARDS | | | | | |
| Single-sided | 0 | 68 | 21 | 11 | 0 |
| Double-sided | 0 | 56 | 37 | 7 | 0 |
| Multi-layer | 0 | 29 | 58 | 13 | 0 |
| Prototype | 0 | 79 | 8 | 9 | 0 |

| RESISTORS | | | | | |
| Carbon film | 26 | 45 | 23 | 6 | 0 |
| Carbon composition | 35 | 34 | 24 | 7 | 0 |
| Metal film | 20 | 45 | 32 | 3 | 0 |
| Metal oxide | 12 | 59 | 13 | 6 | 0 |
| Wirewound | 4 | 31 | 31 | 34 | 0 |
| Potentiometers | 7 | 44 | 41 | 4 | 0 |
| Networks | 10 | 40 | 35 | 15 | 0 |

| FUSES | | | | | |
| Pull/button | 30 | 40 | 20 | 10 | 0 |

| SWITCHES | | | | | |
| Pushbutton | 17 | 48 | 13 | 22 | 0 |
| Rotary | 4 | 50 | 33 | 12 | 0 |
| Rocker | 15 | 50 | 20 | 15 | 0 |
| Thumbwheel | 6 | 44 | 19 | 31 | 0 |
| Snap action | 0 | 56 | 28 | 16 | 0 |
| Momentary | 5 | 58 | 16 | 21 | 0 |
| Dual in-line | 0 | 50 | 36 | 14 | 0 |

| WIRE AND CABLE | | | | | |
| Coaxial | 17 | 63 | 12 | 8 | 0 |
| Flat ribbon | 11 | 48 | 30 | 11 | 0 |
| Multiconductor | 14 | 52 | 29 | 5 | 0 |
| Hookup | 43 | 32 | 21 | 4 | 0 |
| Wire wrap | 38 | 25 | 31 | 6 | 0 |
| Power cords | 13 | 54 | 12 | 21 | 0 |

| POWER SUPPLIES | | | | | |
| Switcher | 4 | 44 | 26 | 26 | 0 |
| Linear | 0 | 41 | 35 | 24 | 0 |

| CIRCUIT BREAKERS | | | | | |
| General purpose | 6 | 35 | 29 | 30 | 0 |

| HEAT SINKS | | | | | |
| General purpose | 15 | 50 | 23 | 12 | 0 |

| RELAYS | | | | | |
| General purpose | 19 | 43 | 14 | 24 | 0 |
| PC board | 20 | 30 | 20 | 30 | 0 |

| RELAYS | | | | | |
| Dry Reed | 0 | 46 | 15 | 39 | 0 |
| Mercury | 0 | 43 | 14 | 43 | 0 |
| Solid state | 0 | 36 | 29 | 35 | 0 |

| DISCRETE SEMICONDUCTORS | | | | | |
| Diode | 37 | 15 | 27 | 12 | 6 |
| Zener | 32 | 25 | 18 | 14 | 7 |
| Thyristor | 12 | 29 | 24 | 29 | 6 |
| Small signal transistor | 24 | 19 | 33 | 19 | 5 |
| Power, bipolar | 6 | 47 | 13 | 20 | 7 |

| INTEGRATED CIRCUITS, DIGITAL | | | | | |
| Advanced CMOS | 10 | 19 | 33 | 33 | 5 |
| CMOS | 11 | 36 | 36 | 14 | 3 |
| TTL | 29 | 17 | 38 | 12 | 4 |
| LS | 24 | 36 | 24 | 12 | 4 |

| INTEGRATED CIRCUITS, LINEAR | | | | | |
| Communication/Circuit | 15 | 23 | 31 | 23 | 8 |
| OP amplifier | 25 | 33 | 21 | 17 | 4 |
| Voltage regulator | 15 | 40 | 20 | 20 | 5 |

| MEMORY CIRCUITS | | | | | |
| RAM 16k | 15 | 25 | 25 | 20 | 15 |
| RAM 64k | 13 | 35 | 22 | 17 | 13 |
| RAM 256k | 12 | 18 | 35 | 23 | 12 |
| RAM 1M-bit | 8 | 17 | 17 | 42 | 16 |
| ROM/PROM | 7 | 27 | 20 | 33 | 13 |
| EPROM 64k | 5 | 38 | 19 | 29 | 9 |
| EPROM 256k | 9 | 30 | 26 | 26 | 9 |
| EPROM 1M-bit | 7 | 13 | 33 | 34 | 13 |

| DISPLAYS | | | | | |
| Panel meters | 8 | 50 | 17 | 25 | 0 |
| Fluorescent | 11 | 45 | 11 | 22 | 11 |
| Incandescent | 22 | 45 | 0 | 33 | 0 |
| LED | 15 | 30 | 25 | 25 | 5 |
| Liquid crystal | 0 | 29 | 29 | 35 | 7 |

| MICROPROCESSOR ICs | | | | | |
| 8-bit | 22 | 17 | 39 | 17 | 5 |
| 16-bit | 11 | 17 | 39 | 28 | 5 |
| 32-bit | 7 | 26 | 47 | 20 | 0 |

| FUNCTION PACKAGES | | | | | |
| Amplifier | 20 | 30 | 30 | 20 | 0 |
| Converter, analog to digital | 13 | 20 | 40 | 20 | 7 |
| Converter, digital to analog | 17 | 17 | 33 | 25 | 8 |

| LINE FILTERS | | | | | |
| Ceramic monolithic | 22 | 37 | 22 | 19 | 0 |
| Ceramic disc | 22 | 44 | 19 | 15 | 0 |
| Film | 32 | 41 | 9 | 18 | 0 |
| Aluminum electrolytic | 30 | 41 | 18 | 7 | 4 |
| tantalum | 28 | 31 | 21 | 17 | 3 |

| INDUCTORS | | | | | |
| General purpose | 0 | 40 | 30 | 20 | 10 |

Source: Electronics Purchasing magazine's survey of buyers

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EDN March 3, 1988
Networking software and interprocess-communication schemes allow designers to devise systems capable of running transparent distributed-processing applications. (Photo courtesy Apollo Computer)
Network operating systems, file-sharing software, and application-development tools simplify the task of designing systems that harness distributed processing power. Using software products such as these, you can even partition an application’s executable code among heterogeneous systems.

Maury Wright, Regional Editor

Networking software now offers designers the tools necessary to implement networked systems that support the distribution of processing tasks among network resources. Products resulting from the ISO’s (International Standards Organization) network-standardization effort may be years away, but products available today offer bridges to future ISO-based networks. You can implement networks that distribute tasks among heterogeneous systems in addition to simplifying the implementation of departmental networks.

This software includes network operating systems, network file-system software, and network application-development tools. The products offer compatibility with de facto standard networking protocols such as TCP/IP (Transmission Control Protocol/Internet Protocol) for heterogeneous systems and NETBIOS for departmental networks.

Networked computer systems can provide users with two levels of connectivity. At the minimum level, they let you share files, use electronic mail, and share hardware resources such as disks and printers. At this level, any single application program can execute on only one computer on the network, but the program can access data from either its host system or from other network resources.

At the higher level, different computers on the network can execute different portions of code that, together, make up a single application program. In this type of distributed-processing environment, not only do different applications run on different nodes on the network, but one application can run partially on one node and partially on another. An application programmer allocates tasks to network resources and matches the processing-power requirements of a task with an appropriately powerful computer system on the network. At the end-user level, task execution is transparent.

Task allocation matches computing power

A distributed-database application serves as a good example of an environment that can exploit the capabilities of this type of distributed processing. In such a scenario, users access the database with a personal computer, and the PC furnishes the application software that lets the computer—and you—access the data. A minicomputer or mainframe, however, runs the database program that processes database queries. Likewise, in scientific applications, programmers can transfer computation-intensive tasks from a relatively slow workstation to a supercomputer.

Setting up a network that connects all IBM systems—from personal computers to mainframes—is a simple task. You simply buy IBM’s networking software,
Software based on layered protocols such as TCP/IP gives designers a way to implement heterogeneous networks now and convert to ISO-compatible protocols later.

which encompasses the entire product line. Digital Equipment Corp (Maynard, MA) offers similar capabilities for its systems. Other companies, such as Bridge Communications Inc (Mountain View, CA), Excelan Inc (San Jose, CA), Micom-Interlan Inc (Boxboro, MA), 3Com Corp (Santa Clara, CA), and Ungermann-Bass Inc (Santa Clara, CA) offer bundled hardware and software packages to ease the task of connecting specific, unlike systems.

The unfortunate reality is that off-the-shelf networking systems are available for only a limited combination of computer systems. In many instances, you may need to adapt network software to a system your company has designed, or an off-the-shelf system may not include features you require.

So, to implement your own network for heterogeneous systems, you must take into account two software issues. First, you have to implement software that connects like and unlike systems. And then, to achieve distributed processing, you have to devise an interprocess-communication scheme. Hardware-independent networking software with layers corresponding to the OSI (Open Systems Interconnection) model can simplify the design of a networking environment (for more information on the ISO/OSI model, see box, “Existing networks fit the ISO/OSI model”).

Several companies have concentrated their operating-system software-development efforts on personal-computer departmental networks. In truth, literally hundreds of vendors offer file- and printer-sharing software for MS-DOS-based personal computers. However, only a handful, such as Novell, Banyan, Western Digital, and Microsoft, offer hardware-independent software capable of supporting distributed processing, and only a handful are working on expanding their products to run on heterogenous systems.

Personal-computer LANs lack standards

Novell has captured the largest part of the market for network operating systems with Netware. This operating system costs $2195 and employs a client/server communication scheme. Such a scheme requires that one or more computers on the network be declared a dedicated file server. The client machines on the network access the server's files and resources.

Banyan Systems also takes a client/server approach with its network operating system, called Vines (virtual networking system technology). This OS costs $1895. Both Netware- and Vines-based systems offer connectivity to IBM SNA (Systems Network Architecture) and X.25 wide-area-network systems. Novell and Banyan have also devised proprietary methods for interprocess communications on their network operating systems. In addition, both systems use proprietary network- and transport-layer protocols.

Western Digital's Vianet Professional and Microsoft's Networks operating systems employ the NETBIOS network- and transport-layer protocols that IBM uses in its personal-computer LAN products. (Microsoft sells its networking software on an OEM case-by-case basis.) Networks based on NETBIOS use a peer-to-peer communication scheme: You don't have to designate any of the computers as a dedicated file server, and thus any networked system can share resources with any other system without having to bother with a file server. Banyan and Novell do offer add-on packages that allow NETBIOS software to run on their networks, however.

No one has yet applied any of these four operating systems extensively to achieve the high level of connectivity described earlier. A few application-development tools, such as the Oracle (Menlo Park, CA) relational database, are compatible with Netware's protocols, but primarily users run MS-DOS applications on their networked system and simply share files and resources.

Vendors plan open systems

Each of the four vendors wants to promote the use of its products for implementing distributed-application-processing systems, however. And, each vendor is developing plans to accommodate the new OS/2 operating system, which will include networking software for distributed processing.

As an option to its OS/2 operating system, Microsoft will offer a program called LAN Manager as well as MS-DOS-based software compatible with the LAN Manager. The LAN Manager will have enhanced capabilities for interprocess communications; Microsoft calls these enhanced capabilities Named Pipes. The Named Pipes facility will operate on the NETBIOS transport layer. It could be a year before Named Pipes is available, however.

In contrast, IBM has announced plans to use its APPC (advanced program-to-program communication) interprocessor communication scheme in its version of OS/2. Novell intends to support IBM's APPC scheme, but hasn't set a product-availability date yet. The vendor will integrate its proprietary client/server technology with the peer-to-peer operation of APPC. In fact, Novell says that it plans to support an open-
protocol technology with its file-server software, but has yet to announce any products.

Although neither Banyan nor Western Digital have published any definite plans concerning OS/2 support, Western Digital does plan to use the NETBIOS transport protocol. And, both companies are planning to adapt their network software to operating systems other than MS-DOS. Banyan, for example, has demon-

Existing networks fit the ISO/OSI model

For several years, the International Standards Organization (ISO) has been working on a set of standards for networking based on the OSI (Open Systems Interconnection) model. The standardization effort promises to simplify, for the computer engineer, the task of connecting and distributing files and applications among heterogeneous systems. But the ISO hasn't completed the standardization process, and software based on the standards may be five years away. Nonetheless, emerging products such as TCP/IP (Transmission Control Protocol/Internet Protocol) software fit the ISO/OSI model.

The ISO/OSI model defines a networking environment based on seven layers of hardware and software. Each layer of the model builds upon the layer below it, and has a defined interface with adjacent layers above and below. Although listed many times before, the seven layers are described below in hierarchical order.

1. The Physical Layer defines the mechanical and electrical characteristics of the physical connection between the computer and the network.

2. The Data Link Layer defines how network-interface hardware packs/unpacks bits into/out of groups called frames, for transmitting and receiving messages.

3. The Network Layer defines how computers route packets of information over the network. The packets consist of a group of data frames combined in a format that is also specified by this layer.

4. The Transport Layer defines how a computer combines packets to form messages, and how it addresses and connects to different devices on the network. This layer also defines protocols that ensure reliable message transfer between nodes.

5. The Session Layer defines how network application software sets up, manages, and terminates communications on the network. The definition includes concepts that allow the applications to interface to network devices with names rather than physical network addresses.

6. The Presentation Layer defines how network application software converts between the application's data format and syntax, and the way data is transferred over the network.

7. The Application Layer defines how network application software provides services such as file sharing, terminal support, and electronic mail.

The ISO/OSI model allows for flexibility in network implementations. For example, two networks can have different application layers and yet use the same lower six layers. Likewise, a network can have a single group of upper layers that can connect to different networks via multiple versions of lower layers.

Currently, networks based on the TCP/IP protocol can connect a variety of heterogeneous systems. And the protocol fits the ISO/OSI model. The TCP software is the transport layer, and IP software is the network layer. In general, vendors also include software that addresses layers 5, 6, and 7 when they claim a package to be TCP/IP compatible. For example, the FTP (File Transfer Protocol), Telnet (virtual terminal utility), and SMTP (Simple Mail Transfer Protocol) applications have become standard in TCP/IP networks.

The TCP/IP protocol evolved from the Department of Defense and has become a de facto standard in the US. Networks based on the protocol operate over a variety of physical media. Although the ISO hasn't chosen the TCP/IP protocol, the protocol also provides users with a bridge to products that will evolve from the ISO standardization effort. ISO-based session-, presentation-, and application-layer software will be adaptable to the TCP/IP transport and network layers, and TCP/IP-based applications will be portable to ISO transports.
New application-development tools simplify the task of spreading application code among distributed network resources.

strated Vines on a DEC VAX and plans to offer the operating system on DEC and Unix-based systems, but will not commit itself to specific product-introduction dates.

Western Digital already offers Vianet for some Unix- and Xenix-based environments. Moreover, Vianet's peer-to-peer software allows you to link personal computers and Unix systems. The company sells Vianet for MS-DOS systems for $150/node; pricing for Unix and Xenix systems is based on OEM agreements only, and depends on how you obtain the operating-system license and whether you port Vianet to your system or whether Western Digital does.

All of these four companies, well-versed in implementing departmental networks for personal computers, are well on their way to implementing heterogeneous systems, but vendors familiar with DoD networks based on the TCP/IP protocol are further along in linking both departmental and heterogeneous networks. Granted, each of the four vendors offers TCP/IP-compatible software that can act as a gateway, but a gateway server isn't adequate for heterogeneous-system distributing-processing applications: It only provides a means of transferring data between the two kinds of networks.

The TCP/IP protocol corresponds to the OSI's network and transport software (as does NETBIOS), but users have come to expect TCP/IP software packages to include file-transfer, electronic-mail, terminal-emulation, and other functions. You can buy TCP/IP software for virtually any hardware/operating-system combination (see box, "Macintoshes adapt to heterogeneous networks").

FTP Software offers TCP/IP-compatible software for IBM PCs and compatibles. The FTP Software TCP/IP package costs $400/station, and the programming library costs an additional $500. You can use the library to develop software for distributing applications across the network. Network Research Corp and The Wollongong Group also offer TCP/IP software for personal computers at a rate of $350/station and $395/station, respectively. In fact, the three companies (and other companies in the network industry) are also working on a NETBIOS interface for TCP/IP software. Such a product would make it possible for NETBIOS-based software to operate on TCP/IP networks.

Macintoshes adapt to heterogeneous networks

Since its inception, the Apple Macintosh has included an interface to the Appletalk network as a standard feature, but connecting the Macintosh to other systems has not been so straightforward. Several companies offer products that allow IBM PCs and compatibles to share files and printers with Macintosh systems on the Appletalk network using Appletalk-compatible software. Now you can also configure networks that connect Unix systems to IBM and Apple personal computers.

Apple offers a $399 Appletalk interface card for IBM PCs and compatibles and plans to offer software that will allow such computers to become "clients" on an Appletalk network. The Tops operating system (Tops is both the company's name and the name of its network operating system) can connect Macintosh computers, IBM and compatible personal computers, and Unix systems, such as workstations from Sun Microsystems and Pyramid Computers.

The Tops software costs $189 for Apple or IBM PCs and $895 to $2495 for Unix systems, based on the number of users. The software lets the different systems share files and printers. For IBM compatibles and Unix systems, such as the Tops Flashcard or a card from Tangent Technologies (Norcross, GA). And to connect your Unix systems, you must use an Appletalk-to-Ethernet bridge such as the one that Kinetics (Walnut Creek, CA) offers. You can connect Nubus-based Macintosh systems to Ethernet with a Kinetics board also. In a Tops-based network, IBM PCs and compatibles and Unix systems can provide the Macintosh with gateways to other networks.

Tops also offers TCP/IP software called Tops Terminal. The $189 software provides a full TCP/IP implementation for Macintosh, and allows you to connect the Macintosh to any computer in a TCP/IP-compatible network. You must have an Appletalk/Ethernet bridge or an Ethernet board to use the software.
Network Research Corp and The Wollongong Group offer TCP/IP software for other environments as well, including CAE workstations and supercomputers (Fig 1). VAX TCP/IP software, for example, which is available from both companies, costs $6000/station and $8000/station, respectively. Both vendors will also negotiate source licenses so you can adapt TCP/IP software to any system.

In addition, you can use de facto standard software to add to the functionality of TCP/IP networks. For instance, Sun Microsystems' NFS (network file system) provides transparent remote access to file systems on heterogeneous systems (Fig 2). Sun ships NFS with its workstations and also offers a version of the software for IBM PCs and compatibles.

In addition, Sun has made public the NFS protocols and sample source code for libraries that handle remote procedure calls (RPCs) and external data representations. Approximately 30 computer manufacturers have put NFS on their systems. The file system is capable of running on Berkeley Unix, AT&T Unix, and DEC Ultrix and VMS, as well as others. Many major universities have adopted NFS.

Programmers can develop distributed applications on NFS-based systems using the RPC facility, but the applications are dependent on a given network configuration. Apollo Computer's recent introduction of its NCS (network computing system) simplifies the task of developing distributed applications on TCP/IP and other networks.

The NCS software includes an RPC facility, a location broker, and the NIDL (network interface definition language) compiler. The location broker controls a database of services available throughout the network. The RPC run-time facility allows a local program to make procedure calls on remote nodes in the network.

![Diagram of TCP/IP-based network operating system](image-url)

*Fig 1—This TCP/IP-based network operating system from Network Research Corp runs on a variety of systems including personal computers, Unix-based systems, and DEC and IBM mainframes.*
Network operating systems are available for personal computers, but the systems lack standard methods of handling interprocessor communications.

The NIDL compiler generates code that allows local programs to call remote routines, and it generates the code that allows remote nodes to service those calls.

Apollo has announced NCS ports to systems from Ridge Computer (Santa Clara, CA), Cray Research (Mendota Heights, MN) Alliant Computer Systems Corp (Littleton, MA), Multiflow Computer Inc (Brandford, CT), Convex Computer Corp (Richardson, TX), DEC, Sun Microsystems, and to IBM PCs and compatibles. You can purchase the source code to the NCS software for a 1-time license fee of $1000.

Netwise Inc has similar application-development tools to offer. The company calls its code-generation tools the PDU (protocol data unit) and the RPC. The PDU compiler generates procedures that translate data into machine- and operating-system-independent formats. The RPC compiler generates source code for making remote procedure calls over the network.

The vendor has begun shipping TCP/IP-based software for systems from Cray Research, Convex Corp, Eixsi Ltd (San Jose, CA), Silicon Graphics Computer Systems (Mountain View, CA), IBM, Sun Microsystems, and DEC. The price of the PDU ranges from $1800 for a version compatible with the IBM PC to $60,000 for a Cray Research version. The RPC ranges in price from $1500 to $48,000 for the same systems. Netwise plans to continue to port the software to new machines. In addition, you can expect to see versions of the software for SNA/APPC, OSI, OS/2, and DEC's Decnet networks. The PDU and RPC compilers already generate code compatible with the ISO's standardization work.

article Interest Quotient (Circle One)
High 485 Medium 486 Low 487

Manufacturers of hardware-independent networking software

For more information on hardware-independent networking software products, contact the following manufacturers directly, circle the appropriate numbers on the information Retrieval Service card, or use EDN's Express Request service.

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| Apple Computer Inc | 20525 Mariani Ave, Cupertino, CA 95014 | (408) 996-1010 | 653
| Banyan Systems Inc | 115 Flanders Rd, Westboro, MA 01581 | (617) 888-1000 | 652
| FTP Software Inc | Box 150, Kendall Square Branch, Boston, MA 02142 | (617) 864-1711 | 653
| Microsoft Corp | Box 97017, Redmond, WA 98073 | (206) 882-8080 | 654
| Netwise Inc | 4745 Walnut St, Boulder, CO 80303 | (303) 442-8280 | 655
| Network Research Corp | 2580 N Rose Ave, Oxnard, CA 93030 | (805) 485-2700 | 656
| Novell Inc | 122 E 1700 South, Provo, UT 84601 | (801) 378-5900 | 657
| Sun Microsystems Inc | 2550 Garcia Ave, Mountain View, CA 94043 | (415) 960-1300 | 658

For more information, contact:

- Tops
  - 2560 Ninth St, Suite 220, Berkeley, CA 94710
  - (415) 549-5900
  - Circle No 659
- Western Digital Corp
  - 2445 McCabe Way, Irvine, CA 92714
  - (714) 474-2038
  - TWX 910-595-1129
  - Circle No 660
- The Wollongong Group Inc
  - 1129 San Antonio Rd, Palo Alto, CA 94303
  - (415) 992-7290
  - TWX 910-573-2085
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The world's smallest FETs, having feature sizes smaller than 0.1 µm, undergo testing at IBM's T J Watson Research Center. Devices such as these minuscule transistors promise to revolutionize system design by making it possible to design ICs incorporating as many as 1 billion transistors per chip.
Designing systems with the next decade’s increasingly complex chips will require entirely new methodologies and techniques. This article is the first in a 5-part series that will explore the changes already taking place in system design and extrapolate those changes through the year 2000.

Steven H Leibson, Regional Editor

Electronics occupies a unique engineering niche. Next year’s jets won’t fly twice as high or use half as much fuel, and except for the pinstriping, next year’s cars won’t differ markedly from this year’s. But semiconductor technology, the driving force behind most of today’s electronic design, rides upon a wave of ever-increasing capabilities.

Today, just 40 years after the invention of the transistor and 15 years after the appearance of the first 4- and 8-bit µPs, manufacturers have found a commercially practical way to put 1 million transistors on a single chip. Some industry experts predict that by the year 2000, engineers will be working with billion-transistor chips, which represent a thousandfold increase over today’s device density. Recent achievements in creating extremely small semiconductor devices indicate that these predictions will probably come true.

Although shrinking transistor geometries are already making increasingly complex systems possible, engineers are finding that the current design methods can’t manage the complexity of the new chips. To develop systems with the next decade’s denser chips, designers will have to take a completely new approach to system design.

Many forces are driving the development of greater and greater device densities. Data-processing applications seem to have an inexhaustible appetite for memory and processing speed. Space and military applications continue to need devices that combine increased functionality and reliability with reduced size and power requirements. Many earthbound systems, such as medical equipment, require as much reliability as do designs intended for space, and engineers currently achieve this reliability by using redundant circuits. Faster, more complex, better, and more reliable designs all require denser circuitry.

VHSIC program drives semiconductor technology

The Department of Defense initiated the VHSIC (very-high-speed IC) program in 1980 to ensure the ongoing development of faster, denser circuits for military projects. Phase I of the 9-year, billion-dollar VHSIC program prompted contractors to perfect 1.25-µm processes, based on optical lithography, at a time when 2- or 3-µm geometries were the state of the art. The VHSIC program requires participants to commercialize the technology they develop.

Meanwhile, many semiconductor vendors that didn’t
participate in the VHSIC program boosted their internally funded research on process development, in part to keep up with the growing capabilities of the VHSIC contractors. Many advanced commercial parts available now employ the 1.25-µm optical-lithography processes, which have resulted in ICs that achieve unprecedented heights of complexity and speed of operation.

Some IC vendors already offer parts, such as static and dynamic RAMs, manufactured with these advanced optical-fabrication processes. For example, the S128K8 from Inova (Santa Clara, CA) is a 55-nsec, 128k-byte static RAM that packs more than 4 million transistors onto one silicon die. It employs 1.2-µm geometries as well as redundant design to provide acceptable yields (Fig 1). The S128K8's design places 40 4k-byte blocks (which Inova calls slices) on the chip. A fully operational RAM requires only 32 functional slices. After the company has applied the first layer of metal interconnection, it performs wafer testing to identify bad slices, and disconnects them with a laser. The second layer of metal joins the remaining good blocks into a functional device.

**Advanced process technologies benefit all ICs**

Memories are not the only electronic components to benefit from the advancements in semiconductor-processing technology. Both Motorola (Phoenix, AZ) and LSI Logic (Milpitas, CA) will start producing gate arrays built with 1-µm drawn geometries this year. The largest member of LSI Logic's LCA100K family of gate arrays, the LCA100237, contains 236,880 gates. At four transistors per gate, the array holds 947,520—nearly 1 million—transistors. Motorola's HDC000 Max family of gate arrays includes the HDC105, which contains 104,832 gates—or more than 400,000 transistors—and can operate at system frequencies exceeding 100 MHz.

Although the demise of optical lithography has long been prophesied, continual improvements allowed the technology to carry the semiconductor industry through its first 40 years. Today, optical lithography allows manufacturers to fabricate chips with much smaller geometries than many people predicted it would. However, the 0.7- to 0.8-µm processes used to build the current crop of leading-edge, commercial ICs have finally pushed conventional mercury-vapor lithography to its true limits. (After all, the wavelength of blue light is about 0.5 µm.) To achieve geometries smaller than about 0.7 µm, manufacturers must turn to exposure methods that employ shorter wavelengths.

**Beyond optical lithography**

In fact, the Department of Defense revamped Phase II of the VHSIC program by reducing the minimum feature size for VHSIC II chips to 0.5 µm (the program's second phase originally specified 0.8-µm geometries), thus forcing contractors to develop alternative lithographic techniques. Researchers are busily creating a bevy of exotic lithographic techniques for half-micron chips.

In conjunction with TRW (Redondo Beach, CA), Motorola developed a 0.5-µm CMOS process for the VHSIC Phase II program. The process uses direct-write electron-beam (e-beam) lithography for two mask steps (Fig 2). Motorola built a 1k-bit static RAM as the first test vehicle for this process, and ICs from the
The 0.5-µm CMOS process developed by Motorola in conjunction with TRW for a VHSIC Phase II contract produces line widths as small as 0.25 µm.

Device's initial manufacturing run worked. By itself, Motorola's 0.5-µm process dramatically boosts the number of devices you can put on an IC. Circuit density increases by a factor of 14.7, although feature sizes are reduced by only a factor of 2.5 in comparison with the feature size obtained from the 1.25-µm process (Fig 3).

TRW plans to develop this 0.5-µm process much further as its part of the VHSIC Phase II contract. Using the 0.5-µm design rules on a piece of silicon measuring approximately 2x3 in. on a side will allow the company to build a "superchip" containing approximately 34.7 million transistors (Fig 4). TRW says it will build the first superchips before 1989.

Engineers at TRW abandoned conventional IC-design practices for the superchip project. The company doesn't expect to manufacture many superchips that have 34.7 million perfect transistors because of the ICs' extremely large size; defect densities on the raw silicon wafers make such an event unlikely. Instead, the company incorporated systems-level features, including extensive redundancy, in the superchip's design to circumvent defective regions on the device. Each time power is applied to the superchip, built-in self-test circuitry identifies the working modules and constructs a fully operational device from the properly functioning blocks.

An on-chip tool box

The superchip also carries the equivalent of tools and spare parts to repair itself. If a module on the superchip fails during operation, the self-test circuitry on the device can repair the damage by switching in a spare block. The company estimates that the superchip's self-healing capabilities give the component an expected life span of 50 years on Earth-orbital platforms. System specifications and applications often change over such a long lifetime, and engineers can also use the superchip's software-configurable architecture to build systems that reconfigure themselves for new applications.

Although direct-write e-beam lithography is the process of choice for today's experiments with half-micron chips, most IC vendors agree that production lines for 0.5-µm devices will probably use other lithographic processes. Even with the new photoresists developed for e-beam processes over the past few years, e-beam writers still take enormous amounts of time to draw the tiny lines on an IC.

GCA Corp (Andover, MA) has already shipped a wafer stepper that uses an excimer laser as the illumination source. The wafer stepper can fabricate 0.5-µm circuits. Other stepper vendors are close behind GCA. Some IC manufacturers are considering x-ray lithographies for half-micron (and smaller) devices. Further, one of the goals of the Department of Defense's MMIC (Monolithic Microwave IC, pronounced "mimic") program is to make ICs with 0.25-µm geometries manufacturable. The MMIC program is expected to bear fruit in the early 1990s. Semiconductor manufacturers show no signs of abandoning their quest for ever-smaller geometries and denser ICs.

As researchers continue to shrink device geometries,
The mathematical models describing transistor operation start to fall apart. Scientists at IBM’s T J Watson Research Laboratory in Yorktown Heights, NY, have fabricated ICs containing NMOS transistors built with 0.07-µm geometries in an attempt to discover whether such small devices would operate as transistors (Fig 5). About 75% of the structures on the test chips were operational.

Because of their tiny feature sizes, the 0.07-µm transistors operate from a 1V power supply and are cooled by liquid nitrogen to combat thermal noise. The thin gate oxide—it’s less than 50 Å (or fewer than 20 atoms) thick—necessitated the low power-supply voltage in order to prevent destruction of the oxide by high electric-field stresses. Although IBM’s researchers designed their devices for cryogenic cooling, they see no fundamental reason why FETs with 0.1-µm gate lengths can’t operate at room temperature as well.

The mathematical models for transistor operation suggested that devices scaled to such small geometries wouldn’t function. However, IBM’s transistors not only worked, but also exhibited excellent transconductance characteristics. The company claims that its e-beam lithographic process can write patterns as small as 0.02 to 0.05 µm onto a silicon wafer. IBM continues to conduct research on such small structures.

The device density in the TRW/Motorola CMOS process increased by a factor of 14.7 when geometries shrunk from 1.25 to 0.5 µm (a linear scaling of 2.5). A further reduction in linear feature size from 0.5 to 0.07 µm (a reduction of a little more than 2.5) could therefore produce an additional density increase of about 216 (14.7²). Apply that increase to the TRW superchip’s transistor count of 34.7 million and you arrive at a phenomenal 7.5 billion transistors on one 2x3-in. piece of silicon!

**Giga-scale integration**

So, by the end of the 90s, the combination of sub-micron geometries, expanding silicon die size, and redundant IC design promise to put billions and billions of transistors on a chip. However, few engineers are thinking about such giga-scale integration (GSI) today. Such tremendous ICs won’t find their way into every system—many designers will probably make do with a few million transistors per chip—but you should consider now how GSI will affect your designs and your design methods over the next decade.

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That is, you could put such systems on silicon if you had the proper tools. Most system designers don't have the tools necessary to build such incredibly complex ICs. TRW uses a combination of purchased and internally developed tools for the superchip project. Because even a GSI-level device couldn't incorporate all of the circuitry of today's most complex systems, such as the Cray 2, it's likely that at least some future systems will incorporate several GSI devices. Current CAE tools simply can't handle systems of that complexity, and today's design methodologies aren't capable of addressing such a monumental task. In addition, the test philosophies currently employed by most electronics companies virtually guarantee that systems built from such sophisticated components will be untestable, as will the components themselves. Today's chip- and system-level packaging schemes seem equally unable to cope with GSI devices.

All these inadequacies place electronics designers at a crossroads. They must choose whether to keep today's design methods, which will limit them to today's level of system complexity, or adopt new tools and technologies to progress to the next decade's level of system complexity. Current system-design techniques just will not work with tomorrow's IC complexity. Companies that plan to design future systems with the techniques they use now risk being left in the dust over the next decade.

The tools and methodologies that will allow engineers to create electronic systems from extremely complex components are already starting to appear in prototypical form. Although they're not yet ready to tackle GSI components or systems that incorporate them, these developments suggest the system-design trends of the 1990s. The remaining articles in this series will explore these emerging methods, technologies, and trends.

Reference

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2M-byte diskettes need special tests for quality control

The bit density of 2M-byte diskettes is near the theoretical limit for longitudinal recording methods. Careful quality-control testing is therefore critical to error-free use of these diskettes in computer systems.

Jerome L Hartke, Media Sciences Inc

The floppy-disk drives supplied with IBM PS/2 and similar computers provide storage capacity of 2M bytes (1.44M bytes formatted) on 3½-in. diskettes at a density of 17,000 bpi. At this density, which is not far below the theoretical limit for longitudinal recording on cobalt/ferric oxide media, certain performance characteristics have become critical. Thus, the quality-control departments of manufacturers and large-volume users need to develop effective methods of testing the diskettes in order to ensure error-free operation of the computers that use them.

Noise—a generic property of diskette subsystems—is classed as either random or systematic. Random noise originates mainly in the low-level electronics of the drive and competes with data signals recovered by the read/write head. At lower densities, standard design techniques yield adequate signal-to-noise (S/N) ratios. However, to provide a resolution of 17,000 bpi, the magnetic medium has to be very thin, and the read/write heads must have very small head gaps.

These requirements reduce the amplitude of both the recorded signal and the recovered signal.

The problem is aggravated by the systematic (non-random) noise produced by unavoidable minor imperfections in the disks' very thin magnetic coatings, and by further variations in thickness produced in the coating and burnishing operations. In double-density diskettes, these variations are unimportant, because they are only a very small fraction of the coating thickness. In high-density diskettes, however, these variations produce a significant amount of noise. The S/N ratios and bit-error rates of high-density diskettes are therefore not as good as those of the double-density (720k bytes, formatted) diskette subsystems of the PC/AT and compatible machines.

Test standardization is urgently needed

You can specify (and measure) noise in three different ways: as broadband analog noise, narrowband analog noise, and digital noise. However, there are no standard test methods, nor is there a standard reference material relating to the noise testing of diskette subsystems.

To ensure adequate performance of high-density subsystems, both users and manufacturers must agree on specifications and methods for noise testing. These specifications and methods will have to take into account not only the type of noise to be checked, but several other factors that can affect the test results.

For example, the drive used for testing is critical. A drive with a poor high-frequency response can mask the effects of noise. Also, the use of factory-preset write
Variations in coating thickness are unimportant in standard diskettes but become a significant source of noise in high-density diskettes.

currents for the drive, instead of the ANSI-specified test recording current, can yield misleading test results, as well as cause test-interpretation problems. Confusion occurs because of the difficulty of correlating actual results to those expected with the ANSI-specified write current. The drive’s head compliance can also influence results, because this compliance is a measure of how well the head and the medium “marry.” Incorrect head pressure can cause poor compliance and thus yield incorrect and misleading test results.

Broadband analog noise

Broadband analog noise is the summation of all noise sources within the bandwidth of the drive electronics. You can specify noise either as an rms value or as a peak-to-peak value. The peak-to-peak value is the more meaningful one for diskette testing, because you normally sample the data at the peaks of the analog output signals from the read/write head.

You can readily measure this value with any commercially available tester that embodies a peak-to-peak detector. A good approach is to measure the broadband noise averaged over an entire track that has been erased by dc. You’d then fill the same track with data and measure the average value of the recovered signal. For this measurement, you’d normally use track 79, which has the highest bit density and the lowest signal amplitude. The ratio of the two values provides a convenient figure of merit for the diskette.

Another approach to broadband-noise testing is the “extra-bit” test, for which there is an ANSI specification. You normally perform this test on every track to detect physical or magnetic anomalies, but it also happens to be an effective noise test.

To perform the test, you first write to a track at maximum bit density and measure the amplitude of the recovered signal. You then de-erase the track and probe each bit location to find the highest residual signal. Because this measurement senses the worst area on each track, the resulting noise values are usually higher than broadband-noise values that represent an average over the entire track.

The proposed ANSI diskette specifications allow residuals, or extra-bit levels, as large as 20% of the previously recorded signal. You’ll see from Fig 1, however, that although residual levels on double-density diskettes seldom exceed 10% of the previous signal, noise associated with the new high-density diskettes consistently does, and it occasionally reaches a value between 15 and 18% of the previous signal—very close to the proposed limit.

Narrowband analog noise

Narrowband analog noise is defined as the total amount of noise present in a narrow, controlled frequency range that is centered upon a particular frequency. One test of narrowband noise, for which an ANSI specification exists, is the overwrite test.

To perform this test, you first write a minimum-density, 125-kHz signal (called a 1F data pattern) on track 00 (the outermost track), and then measure the amplitude of the recovered signal. Without erasing, you then write a maximum-density, 250-kHz signal (called a 2F data pattern) onto the same track. Then you measure the amplitude of the residual 1F signal, using a narrowband filter to reject the much larger 2F signal now present. The overwrite value is the ratio of the residual 1F signal amplitude to the initial value of that signal (before you write the 2F pattern).

You can use this same technique to measure narrowband noise. You first write a 1F pattern and measure its amplitude. Then you de-erase the track and, using the same narrowband filter as for the overwrite test,
Fig 2—The slight jogs in extra-bit and broadband noise levels that occur between tracks 43 and 44 are related to internal changes in the bandwidth of the drive electronics.

measure the residual level of the 1F frequency. The ratio of the residual 1F noise to the initial 1F signal level provides a relative measure of diskette or drive performance. This ratio is independent of the bandwidth limitations of amplitude detectors and extra-bit detectors in the test equipment, and is also independent of the characteristics of any lowpass filters in the test system.

Digital noise

Digital errors consist of data pulses from the diskette that are displaced from the expected center of the bit cell. In the timing or phase-error specification, the amount of the displacement is expressed as a percentage of the full data window. For a 2M-byte, high-density diskette, the bit cell is 2 µsec wide, and the data window extends ±500 nsec from the center of the cell. Thus, a disk pulse that is displaced 500 nsec from the cell center constitutes a 100% window or phase error. Because the digital data pulses are related to the peaks in the analog waveform generated by the read/write head, amplitude noise distorts the waveform and changes the position of the peaks within the cell. You can see, therefore, that analog and digital noise are interrelated.

Another type of digital error results from the interaction of the densely packed magnetic flux changes on the diskette. These interactions also modify the analog waveform and give rise to the effect known as peak shift. Adjustments to the drive could exactly compensate for peak shift if the magnetic properties of the diskette were perfectly uniform and if the interaction with the drive were consistent. However, because neither of these ideals can be realized in practice, the jitter resulting from peak-shift effects leads to phase errors.

Although either phase-noise or peak-shift testing is possible, peak-shift testing provides only a track-average value. Phase-error testing, on the other hand, detects the worst error on each track and is therefore more effective.

Although no standards yet exist, two test methods are in current use. One of these is the phase-error test. You perform this on each track by first filling the track with a 2F worst-case, 16-bit pattern consisting of the hexadecimal digits B6DB (binary 1011 0110 1101 1011 1011 0110 1101 1011 ... etc). The pairs of 1s ensure that as many bit locations as possible are tested; the occurrence of an extra 1 at every fifth pair averages out the effects of any asymmetry in the head windings. After writing the pattern, you read the track and capture the largest phase error for display as a percentage of the 500-nsec window. You can think of this phase-error test as a digital equivalent of the extra-bit analog test.

The second test method is the phase-margin test. Again, you write a 2F worst-case, B6DB test pattern over the entire track. You then measure the bit-error rates that result from varying the width of the data window. If you plot error rate vs window size, both the threshold and shape of the curve can provide valuable information.

Practical applications of the tests

The method you choose for digital-noise testing will largely depend on your goals. If you want to test 100% of the diskettes in each outgoing (or incoming) batch, the phase-error method is probably preferable. It is fast enough to test every track and is adequate for initial qualification of the diskettes. To perform a more
Both users and vendors must agree on specifications and methods for noise testing of high-density diskettes.

Both rigorous test on selected samples, you can use phase-margin testing, which provides results that directly correlate with system performance. It is time consuming, however—it can take more than an hour to test all 160 tracks of a high-density disk. You’d therefore probably test only track 79 of your samples (the innermost track, which is most vulnerable to errors of all kinds).

Media Sciences Inc conducted tests of high-density diskettes manufactured by Fuji, Kao, Maxell, Sony, TDK, and Verbatim, using the Media Logic Model 2000 Evaluation System in conjunction with three different high-density drives: the Sony MP-F73W-00D, the Sony MP-F73W-01D, and the Teac FD-35HFN-22. Except where noted, use of either the factory-preset value of write current, or the ANSI Test Recording Current, yielded comparable results.

Although the tests revealed differences among drives and among diskettes from the sources mentioned above, these differences were often less than the variations between different samples from the same vendor. Consequently, the results that follow reflect the average level of performance that is now available. If you wish to rank diskette vendors, you should take into account not only the performance of evaluation samples, but also the spread, or distribution in performance, of each vendor’s products when delivered in quantity.

**Analog noise performance**

Fig 2 shows the typical analog-noise performance of the products tested. Track 79 is clearly the proper track for worst-case noise tests. Fig 2 also shows that extra-bit noise levels are higher than broadband-noise levels, because of the differences in detector bandwidths noted above. Narrowband-noise levels are the lowest, because the test uses a filter with a bandwidth of 6.5 kHz centered on 125 kHz. Overwrite is negligible compared to extra-bit and broadband noise.

Even though they cover different bandwidths, extra-bit, broadband, and narrowband tests all measure the same noise source. You would, therefore, expect the results of the three tests to differ only by scaling factors. The correlation displayed in Fig 3 verifies this assumption and establishes any one of the three tests as valid, provided that the bandwidth is properly controlled.

Narrowband analog noise measurements are the most readily controllable, because the bandpass filter is an integral part of the Model 2000 Evaluation System and is unaffected by changes in drive bandwidth. For this reason, the narrowband noise test is an effective track-79 test for quality-assurance or media-evaluation purposes. It is, however, too time consuming to be economically feasible as a production test on all tracks. On the other hand, extra-bit tests are already a part of production certification and can also serve as a noise test if the system bandwidth is at least 300 kHz.

**Digital noise performance**

Fig 4 shows the results of phase-error tests for digital noise, and Fig 5 shows the phase-margin tests. You’ll see that in both cases, the results depend on the write current, which, because it influences peak shift, also affects phase delay.

Both of these digital-noise test methods are valuable in a laboratory for accurately assessing error risk. The phase-margin test is particularly useful because it predicts error risk in a readily understandable format. A phase-error test on all tracks is potentially valuable as a 100%-inspection test, if the need for a high level of user
Phase-error and phase-margin tests conducted at the ANSI Test Recording Current are important to both quality-assurance and vendor-qualification programs, but you'll have to negotiate the precise specifications for each individual case, pending the issuance of a badly needed industry-wide standard. The appearance of such a standard, coupled with the availability of suitably equipped production certifiers, would support 100% phase-error testing and would significantly enhance user confidence in high-density diskettes.

What's to come

Diskette technology is clearly moving in the direction of greater storage capacity, and the specification and measurement of noise will become even more important for future products. The means by which we'll economically achieve greater capacity is still unclear, but several different approaches are in their experimental phase, and some show commercial promise.

The linear bit densities of 17,000 or more bits per inch currently employed in high-density, 3½-in. diskettes is near the theoretical limit for longitudinal recording on cobalt-doped ferric oxide particles. Vertical-recording techniques have successfully increased bit densities, but practical difficulties and cost considerations have not allowed vertical recording to progress much beyond the laboratory environment.

Two approaches to increasing diskette capacity, however, show promise. One is to increase track density beyond the current value of 135 tpi, and the other is to

---

**Fig 4**—Digital phase-error noise is greatest on track 79. The step between tracks 43 and 44 is caused by internal bandwidth changes in the drive electronics.

**Fig 5**—Phase-margin test results are easy for a user to understand. This test should be a part of all quality-assurance and media-evaluation programs.
Phase-margin testing provides results that directly correlate with system performance. It is also time consuming.

use new magnetic media that permit linear bit densities as great as 51,000 bpi. To increase track density, a closed-loop servo system for head positioning is a necessity. One popular technique is to define each track on the disk by means of a prerecorded pattern. This method requires users to purchase disks on which the servo patterns have been written by the manufacturer or bulk vendor.

Iomega was a pioneer of this embedded-servo technique with its Bernoulli Box. The Bernoulli effect is the creation of a partial vacuum between head and disk. This vacuum, caused by the high-speed rotation of the disk, is strong enough to pull the head close to the disk, while leaving a cushion of air between them that prevents damage. Iomega's present 20M-byte (unformatted) product stores data at a density of 21,000 bpi; a plastic shell encloses the 5½-in. diskette, which spins at 1800 rpm.

Eastman Kodak and Data Technology Corp have jointly announced 12M-byte drives and diskettes. Embedded-servo techniques achieve 333 tpi on the 5¼-in., cobalt ferric oxide diskette. The diskette spins within a hard plastic case at approximately 600 rpm—lower than the speed at which the Bernoulli effect occurs. A variable-speed drive maintains the 22,000-bpi recording bit density almost constantly over all tracks.

Konica's 10M-byte product also uses a closed-loop servo system to achieve a track density of 480 tpi. The Konica diskettes have a soft jacket and operate at densities less than 18,000 bpi. NEC has announced a 3½-in., 6M-byte flexible diskette that uses a servo sampling system.

Manufacturers are also using new magnetic materials such as barium ferrite and metal powders. Toshiba offers a 3½-in., 4M-byte diskette and drive using barium ferrite to achieve a density of 35,000 bpi. Sony recently unveiled a 2-in., 2M-byte disk and drive that employ metal powders to achieve densities as great as 51,000 bpi. Neither the Toshiba nor the Sony product requires closed-loop servos, but the Sony product, derived from that vendor's still-frame video project, spins the diskette at 3600 rpm to use the Bernoulli effect.

New techniques can't eliminate noise

However successful new techniques may be in cramming more data into less space, noise will always be the principal limiting factor. Thus, the search for ways to reduce its effects is going on in parallel with the search for ways to increase data density.

Eastman Kodak has used one promising approach to noise reduction in its 47-mm still-frame video system. It uses nonlinear pre-emphasis to boost higher-frequency and lower-amplitude signals during recording. Playback de-emphasis then returns these signals to their original state and, in the process, suppresses playback noise. Similar but less sophisticated techniques (such as Dolby and dbx) have been used for many years in the audio and broadcast industries.

Although the success of new products and technologies will depend just as much upon cost and multiple sourcing as on the technical factors relating to reliability and high performance, noise is clearly an emerging reliability criterion. Standardized methods for its specification and measurement must evolve, not only for today's 2M-byte diskettes, but also for tomorrow's products.

Author's biography

Jerome L. Hartke is founder and president of Media Sciences Inc, an independent test laboratory serving both manufacturers and users of flexible diskettes. Dr Hartke holds a BSEE and an MS in physics from Kansas State University and a PhD in physics from the University of Illinois. He has served as a research scientist in solid-state physics for Xerox and other corporations, and has served several semiconductor and microwave manufacturing companies in various executive capacities.
Single-chip µCs solve problems in pattern generation

In many applications, the single-chip µC provides a viable alternative to the traditional solutions for pattern-generation problems. The equipment required to apply µCs is inexpensive, and the development cycle for custom pattern generators is short—an attractive combination.

Chris Ghormley, ITT Federal Electric Corp

By using nothing more than one IC and some input switches, you can develop circuits that provide highly functional simulation capabilities. Moreover, you can readily simulate missing portions of a system and thereby validate a design’s performance. Although the following design examples might seem rather specialized, the operational principles involved are general enough to allow you to apply them in the solution of a number of pattern-generation problems.

The rationale for using a µC

The µC, readily available and low in cost, allows you to quickly design simulator instrumentation that you can adapt to specific applications merely by making program alterations. The simulation instruments feature simple designs and low component counts, so they are highly portable and draw little power. In fact, you can often power them from the circuit under test.

Although µCs can’t handle fast signals, they do accommodate low-kilohertz signals. When speed is not the primary criterion, the µC can produce patterns that are not only useful but interactive. By employing simple input-control devices (such as DIP switches), you can use the µC to generate patterns from selected tables or to compute new patterns that depend on switch-selected input parameters. Of course, the input to the µC-based simulator can come from other sources, such as a host µP system. This host-µP capability allows you to invoke high-level commands for a distributed-processing-type pattern-generation application that requires multiple microcomputers.

Several manufacturers produce prototype or small-production-run types of single-chip µCs that incorporate EPROM instead of the masked ROM used in high-volume µC applications. Some of these units include piggyback sockets to accommodate an external EPROM; others, such as the Motorola 68705P3, incorporate the reprogrammable memory on the same die as the µC itself. Today, a number of low-cost development tools (ranging from simulator/debuggers to cross-assemblers) are available for the 6805 µC family.

So much for why you should use a µC-based simulator. It’s time to look at some examples of how you can use the µC.

Positioning an object

The flexible control structures of single-chip µCs allow you to easily program the devices to generate cyclic-type patterns. Optical-encoder simulation is one example of an application that can take advantage of
When speed is not the primary design criterion, the μC can produce patterns that are both useful and interactive.

This pattern-generation capability. Many systems in a wide variety of industries use incremental optical encoders to determine the position and velocity of physical objects. For example, these encoding devices might measure a conveyor’s belt speed or they might be part of a closed-loop control system for a robotic arm.

When you’re developing a physically large system in the lab, you can manipulate a real encoding device to simulate the portion of the system that uses the optical encoder. If you use this brute-force type of simulation, however, it is difficult to accurately simulate a precise velocity or to cause the encoder to rotate through an exact number of revolutions. This shortcoming can cause problems when you have to generate precise patterns to ensure that the detector/demodulator portion of the system is immune to false detection and responds to phase reversals correctly.

Well-logging instrumentation trucks illustrate an application requiring a simulator that provides precise pattern generation. These trucks use optical encoders to totalize the amount of cable payout and to measure the direction and velocity of the cable’s movement. The simulator must produce two differential digital signals in quadrature at a rate of 600 cycles/ft of wire-line displacement.

**Fig 1a** illustrates one implementation of an encoder simulator. The phase relationship between the two output signals (**Fig 1b**) contains direction information; the velocity is directly proportional to the frequency of the waveforms. The circuit generates waveforms

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**Fig 1**—To accurately measure the direction and velocity of cable payout in well-logging applications, this optical-encoder simulator circuit (**a**) provides 11 discrete speeds having an accuracy within 0.5%. The phase relationship between the two output signals (**b**) contains direction information; the velocity is proportional to waveform frequency.

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EDN March 3, 1988
having frequencies as high as 6 kHz and provides 11
discrete speeds whose accuracy is better than 0.5%.
The circuit provides this performance by using the
onboard counter/timer to generate phase-transition in-
terrupts. Most µCs incorporate some type of counter/
timer that's useful for generating such rate-critical
patterns.

**Offers multiple operating modes**
The circuit provides both continuous and pulse oper-
ating modes. The continuous operating mode maintains
speed very accurately and allows you to introduce phase
reversals by simply changing the state of the direction
switch. The pulse operating mode allows you to generate
a precise number of bidirectional pulses—performance
that's analogous to rotating the shaft of an
optical encoder exactly \( n \) times. The circuit's totalizer
output makes it easy to test the decoding system's
displacement accuracy. There's a very compelling ra-
tionale for using the µC-based simulator in this pattern-
generation application—it offers a quick, straightforward firmware solution in place of a potentially
time-consuming, multichip hardware design.

Couple a µC with a UART and you'll wind up with a
very powerful serial-data simulator (Fig 2). The µC in
this circuit operates in two modes. In one mode, it
analyzes the data-frames output from a jet-engine's
control unit; in the second mode, the µC uses four
integral test patterns to simulate the same control unit.
In the analysis mode, five indicators can display format
characteristics and signal conditions.

If you select a µC that has onboard serial-communica-
tions capability (like the MC68701), you can implement
this circuit without using the UART. Units that incor-
porate peripheral functions, such as a full 8-bit UART
or a multichannel 8-bit A/D converter, just increase the
applicability of the single-chip µC to specialized pat-
tern-generation problems.

A single-chip µC's capability doesn't stop with serial-
type pattern generation. Such a µC can also be quite
useful in other applications.

Some cases require parallel-type data patterns; two
good examples are simulation of the discrete outputs of
an instrumented high-power amplifier and the gener-
ation of test vectors for programmable logic circuits.
Many such applications do not require at-speed pattern-
geneneration. Fig 3 illustrates a µC-based circuit that
simulates a bus master for a Motorola I/O Channel bus.
Because the I/O Channel is an asynchronous bus, the
network can serve as a functional, although slow, bus
counter.

**Fig 3's circuit can perform diagnostics on as many as
four peripherals in a single test session. The**
MC68705G2 µC incorporates four I/O pins that can sink
enough current to drive LED displays directly. This
drive capability permits the convenient display of diag-
nostic information without requiring the use of addi-
tional hardware. By using a low-cost µC to exercise the
bus for burn-in and peripheral testing on the production
line, you avoid the need to dedicate expensive VME
CPU cards to such tasks.

Parallel data-stream simulation is another application
that's well suited for the µC. You can, for example,
replace the front end of a data-acquisition system with
a µC that uses look-up tables containing typical or
test-pattern data. This type of simulator is especially
A µC’s capability doesn’t stop with serial-type pattern generation—the µC can also be quite useful in other applications.

useful when the data-acquisition system is measuring a random-type quantity—a situation often encountered in the measurement of differential pulse-height spectra in nuclear-instrumentation tools. In such cases, you can quantify the system’s functionality and accuracy by substituting fixed patterns for the random data to track data flow from the A/D converters to the final log.

As an example of such data-acquisition applications, Fig 4 shows how a µC-based simulator can replace two A/D converters in a spectral Litho-Density tool. Here, the data itself (rather than the relative speed of acquisition) is the important factor for test and development purposes. The simulator provides six different switch-selectable parallel data patterns that you can select by using a DIP switch. Each pattern is designed to highlight a particular fault in the data-processing circuitry.

You can use code to generate four of the outputs because the patterns are quite simple; you must use data tables to generate the remaining two patterns. The LED indicates the completion of a frame of data for any given pattern. For applications involving short periods of data collection, the LED’s off time allows an operator to merely count a few frames of simulation. The circuit lets you connect a totalizer to document longer periods of data collection. This design is very simple, takes little time to fabricate, and is most useful in the laboratory. After circuit development is complete, you can employ this simulator in the manufacturing department for use in production-line troubleshooting and quality control.

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**Fig 3**—Because the application doesn’t require at-speed pattern-generation, this µC-based circuit can simulate a bus master for the Motorola I/O Channel bus. Although somewhat slow, the circuit can perform diagnostics on as many as four peripherals in a single test session.
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In many cases, you can readily move your µC-based simulator tool from the development lab to the production floor.

Fig 4—When intrinsic data is the important factor, rather than the relative speed of acquisition, µC-based simulators can be especially useful. This circuit illustrates how you can use a µC to replace two A/D converters in a spectral litho-density tool.

In high-speed applications, pattern generators, such as Hewlett-Packard’s 8175A or the 9100 system from Tektronix, may provide the most effective solution for design analysis. Both instruments are excellent tools that can produce very fast data rates for demanding applications. Unfortunately, this type of equipment is not available in many laboratories.

Couple an IBM PC (or a compatible computer) with a parallel I/O card and provide some programming, and you have an excellent pattern-generator/ analyzer tool that’s especially useful when you have to graphically display high-speed data. If the project cannot bear the programming costs, several reasonably priced, menu-driven pattern generators are available for the PC; these generators are easy to configure. If this option is still too expensive, you can design an all-hardware system to generate high-speed patterns. The all-hardware design usually has a moderate parts count; unfortunately, it may also consume much of your design time, especially when system data rates approach 25 MHz.

(Ed Note: US readers may obtain program listings for an optical encoder simulator and a spectrum simulator by sending a self-addressed, stamped envelope ($0.39 postage) to Software Listings Editor, EDN, 275 Washington St, Newton, MA 02158).

Author’s biography

Chris Ghormley is a senior engineer at ITT Federal Electric Corp (Vandenberg Air Force Base, CA), where he designs µP-based control systems for high-power command transmitters. In his spare time, Chris enjoys building and flying radio-controlled model aircraft.

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Modula-2's design simplifies programming and compilation

Designing a computer language is punctuated by a series of tradeoffs and compromises. In designing Modula-2, Niklaus Wirth has achieved a better set of tradeoffs and compromises than has any other language designer.

Brian Anderson, Vancouver Community College

Modula-2 gives you the same ease of programming and readability as Pascal, all of the power of C, most of the power of Ada, and more consistent syntax than any of them. Whether you're working on large applications programs, operating systems and utilities, or embedded microcomputer controllers, Modula-2 can easily provide the facilities that you need.

A persistent myth haunts the computer industry: the belief that it is possible to design a computer language that is all things to all people. Ada is one product of this myth—its designers have added so many fancy features to the language that compiler construction is difficult, validation is even more so, and gaining a good command of the whole language is virtually impossible.

The magic of Modula-2 is that it encompasses most of the strengths of Ada without overburdening either the programmer or the computer system. Modula-2 is a small language with a consistent yet elegant structure. Because it has facilities for creating separate compilation units (modules) and also has good low-level and multitasking capabilities, you can use the language to handle a remarkably diverse set of problems with relative ease.

Develop a taste of Modula-2

Developing a program written in Modula-2 is a bit like designing a complex electronic system, say for the VME Bus, from several simpler circuit boards. You'd like, where possible, to use off-the-shelf VME circuit boards because they are cost effective—they need no development time and are already well debugged. Although, in special cases, you might have to design your own VME board from scratch, a large part of the hardware-design effort involves choosing and integrating existing circuit boards. In the same way, you build every Modula-2 program from one or more modules, of which there are four kinds: definition and implementation modules (which together make up a global module); program modules; and local modules.

The global module is like the sample hardware circuit board; it can come already designed and debugged by the compiler supplier (or other third party), or you can create your own specialized modules. A global module comes in two parts: the definition module and the implementation module. The definition module is like a specification sheet—it describes exactly what the module does, and it may also define the data on which the module operates. It contains no code. The implementation module does the work; it contains the code, and it may contain additional data definitions. The compiler will detect inconsistencies between the definition and
Modula-2 gives you the readability of Pascal, the power of C, and more consistent syntax than either of them.

implementation modules, and will not compile any implementation that does not adhere to the specifications given in the definition module.

The other two kinds of building blocks are program modules and local modules. Every Modula-2 program is a program module. The hardware analogy would be the mother board in your electronic system. IMPORT statements "plug" global modules into your program module. Each global and program module must reside in a separate file so that it can be separately compiled.

A local module, on the other hand, has most of the same characteristics as a global module, but doesn't reside in a separate file; instead, it's embedded into either a program or implementation module. The closest hardware analogy to the local module would be a daughter board; and, like daughter boards, local modules are of limited use.

A simple example will suffice

The program module in Listing 1 follows Kernighan and Ritchie's example: It displays "Hello, World!" on the standard output device (usually a video screen) and then halts. The keyword MODULE identifies this as a program module, with the programmer-chosen name Hello (which must be repeated at the end of the module). The IMPORT statement accesses a global module called InOut, which provides rudimentary console and file input/output functions in a portable, standardized manner. Wirth originally described the InOut module, and it comes as part of all Modula-2 systems.

Understanding the design philosophy helps

Modula-2 has only 40 keywords; consequently, it's easy to learn. The syntax borrows heavily from Pascal, but is much more consistent and often more elegant. The core language contains no input/output functions of any kind, but delegates that task to individual global modules. Wirth included language features in Modula-2 that make ad hoc language extensions virtually unnecessary, because a properly designed global module can easily provide any facility that you may desire—the language itself remains intact.

The only real impediment to software portability is some variation between the libraries of global modules provided by different compiler vendors. This concern is minor; I developed a 68000 crossassembler on a Z80 Modula-2 system (see Dr. Dobb's Journal, April, May, and June 1986), and was then able to adapt the crossassembler to two new environments (MS-DOS and Atari-ST) in only a few days.

LISTING 1—EXAMPLE OF A PROGRAM MODULE

MODULE Hello;
  FROM InOut IMPORT
    WriteString, WriteLn;
BEGIN
  WriteString("Hello, World!"); WriteLn;
END Hello.

Every Modula-2 compiler comes with a library of precompiled global modules, mainly for input/output, common mathematical, file-management, data-conversion, and other system functions. The kernel of this library consists of several modules that Wirth postulated in his book describing the language; the other modules may vary from compiler to compiler. Several international groups are now cooperating to establish a standard library, however.

An example of how to create a global module will be helpful at this point. Assume that you require a module to compute geometric functions—the volume of a sphere, the area of a square, etc. The definition module will specify the functions that you need. You should write this part of the global module first; actually, the compiler won't allow you to compile the implementation module unless you've successfully compiled the definition module.

The structure of the definition module (Listing 2) is very similar to that of the program module (Listing 1), but it has two distinguishing characteristics: the use of the keyword DEFINITION and the lack of executable statements. The definition module merely specifies to the compiler (and to the programmer) just what functions the module will perform. Each procedure heading indicates first what parameters the function will use, and then what type of value the function will return. The compiler will insist that the corresponding procedure in the implementation module adhere to this specification. Although the comment line—enclosed by (* and *)—has no meaning to the compiler, it ought to help you understand just what the associated function does.

Notice that, unlike Pascal, Modula-2 does not use the keyword FUNCTION. If the procedure is to return a value, that value's type follows the parenthesized parameter list. The EXPORT statement specifies which procedures or data will be available for use by other
modules. The latest Modula-2 definition has dropped this redundant feature and automatically exports everything in the definition module; however, many compilers still require an explicit export statement.

Before the module can do any useful work, you must write the implementation part (Listing 3). The structure of the implementation module mirrors that of the definition module, except that it uses the keyword IMPLEMENTATION and includes executable statements. Notice that the definition and implementation modules must have the same name; they reside in two different files that both carry the module name, but have different file extensions (in this example, the files are GEOMETRY.DEF and GEOMETRY.MOD).

Inside the implementation module

The Geometry module, though simple, introduces all of the important features of a global module. Although it would be possible to use a constant declaration for pi, calculating pi will illustrate the use of import lists and provide an introduction to a module body (or initialization).

The body of an implementation module (between BEGIN and END) is executed only once, before the main program begins execution—you could say that the compiler causes it to start automatically. If there are several global modules, the body of each is executed in an order determined by the compiler. The module’s body is often referred to as the initialization part, because it establishes the starting conditions for the module—in this example, setting the value of pi. To calculate pi, the Geometry module needs the arctan-function PROCEDURE, which therefore has to be imported from the math library (MathLib0). This library also contains other trigonometric and logarithmic functions, as well as functions to convert real numbers to and from integers.

One major role of modules is to encapsulate procedures and variables. Variables declared within the module (like pi) are static—that is, they exist as long as the program is running. Their value does not change between invocations of the procedures within the module.

Modules also provide visibility walls. Objects defined within a module are not available outside that module unless they are exported, as was done in the definition module. Similarly, no external objects are available inside the module unless they are imported (as arctan was imported into the implementation module).

This visibility wall solves two problems associated with large software projects. First, it decreases the likelihood of name clashes (accidentally using the same name in two different contexts), because the scope of each module is separate. Second, a wall makes it impossible for another programmer to deliberately use your data in some way that you never intended. If an object (procedure or data) is not exported, it cannot be used outside the module in which it is defined. If you happen to use the same name in two different modules, the compiler will keep the associated objects separate.

It’s possible to export a data type without revealing any details of its nature; such types are declared

LISTING 2—EXAMPLE OF A DEFINITION MODULE

DEFINITION MODULE Geometry;

EXPORT QUALIFIED
  AreaSquare, AreaCircle, VolumeCube, VolumeSphere;

PROCEDURE AreaSquare (side : REAL) : REAL;
(* Given length of a side, return the area of a square *)

PROCEDURE AreaCircle (radius : REAL) : REAL;
(* Given the radius, returns the area of a circle *)

PROCEDURE VolumeCube (side : REAL) : REAL;
(* Given length of side, return volume of a cube *)

PROCEDURE VolumeSphere (radius : REAL) : REAL;
(* Given radius, return volume of a sphere *)

END Geometry.
Modula-2 encompasses most of the strengths of Ada without overburdening either the programmer or the computer system.

OPAQUE, and the process is called opaque export. You can create variables of this type in another module, and pass them as parameters, but you can only use these variables with the procedures exported from the module where the type was defined. A common example of an opaque export is the FILE type, which is usually implemented as an FCB (file control block). You'll need to refer to the FCB when you want to open, read, or write to the file, but you don't need to know the FCB's internal structure. Opaque export ensures that you can't unwittingly corrupt the components of the FCB.

Local modules act much like global (library) modules, except that they don't reside in a separate file. Although they are usually embedded into program or implementation modules, they may even be embedded into procedures. I have found little use for this feature, but will present the classic application—a random-number generator. This example is from the Hochstrasser compiler manual.

A random-number generator processes a seed to generate the pseudorandom number that it will return. This pseudorandom number then becomes (or is used to derive) a new seed. You should be able to guarantee that the seed will not be altered by other procedures within your program, and that the seed will continue to exist between invocations of the random-number gener-

LISTING 3—EXAMPLE OF AN IMPLEMENTATION MODULE

IMPLEMENTATION MODULE Geometry;

FROM MathLib0 IMPORT
arctan;

VAR
pi : REAL;

PROCEDURE AreaSquare (side : REAL) : REAL;
(* Given length of a side, return the area of a square *)
BEGIN
RETURN (side * side);
END AreaSquare;

PROCEDURE AreaCircle (radius : REAL) : REAL;
(* Given the radius, returns the area of a circle *)
BEGIN
RETURN (pi * radius * radius);
END AreaCircle;

PROCEDURE VolumeCube (side : REAL) : REAL;
(* Given length of side, return volume of a cube *)
BEGIN
RETURN (side * side * side);
END VolumeCube;

PROCEDURE VolumeSphere (radius : REAL) : REAL;
(* Given radius, return volume of a sphere *)
BEGIN
RETURN (4.0 / 3.0 * pi * radius * radius * radius);
END VolumeSphere;

BEGIN
(* module initialization *)
pi := 4.0 * arctan (1.0);
END Geometry.
ator. A local variable in a procedure will hide the seed from other procedures, but its value becomes undefined when the procedure finishes executing. A global variable retains its value, but other procedures may inadvertently change it. However, because the module's structure defines the lifetime of variables independently of their scope, a local module can give the seed an ongoing lifetime but a scope that is limited to the module.

The initialization part (Listing 4) sets the value of the seed before the main program starts executing. Because the variable rand is declared outside the Random procedure, it isn't a local variable. Variables declared in local modules are just like other global variables, except that they are not available outside the module unless there is an explicit export statement. In this example, the EXPORT statement gives you access only to the procedure that returns the next pseudo-random number in the sequence; there is no way that you can alter the seed, which remains hidden within the local module.

Data types extend the language

As you would expect, all of the data types available in Pascal are also available in Modula-2, including INTEGRER, CHAR, and BOOLEAN, along with data-structuring facilities such as ARRAY, RECORD, SET, and POINTER types. Modula-2 also includes some new data types that extend the language in several ways. For example, there is an unsigned-integer data type called CARDINAL. More important, however, are the new types that allow low-level access to the computer hardware. Besides these new data types, Modula-2 provides many additional facilities for manipulating these types.

The BITSET type allows you to treat the contents of a memory location as a collection of bits, and is a small but significant extension to Pascal's set facility. The Modula-2 syntax for sets (and BITSET) more closely follows standard mathematical notation: For a 16-bit computer, a BITSET with the least significant bit (LSB) and most significant bit (MSB) set to 1 would be expressed as 15, 0. You can alter BITSETs by means of the standard procedures INCL and EXCL. INCL (b, 5) sets bit 5 of the BITSET b; EXCL (s, 3) clears bit 3 of

| SET UNION     | {15, 1, 0} + {14, 2, 1} | → {15, 14, 2, 1, 0} |
| SET DIFFERENCE| {3, 2, 1, 0} - {0}       | → {3, 2, 1}         |
| SET INTERSECTION| {15, 1, 0} * {14, 2, 1} | → {1}              |
| SYMMETRIC SET DIFFERENCE | {15, 1, 0} / {14, 2, 1} | → {15, 14, 2, 0} |

Fig 1—Modula-2 allows you to perform logical operations on individual bits of a computer word, a feature that can make low-level access to the hardware much easier than in Pascal.
You build every Modula-2 program from four kinds of modules called definition, implementation, program, and local modules.

the BITSETs. BITSETs can be manipulated by Boolean operators, characterized in Modula-2 as set union (OR), set difference (mask), set intersection (AND), and symmetric set difference (XOR). Fig 1 shows an example of each of these operations.

The utility of BITSETs is further enhanced because Modula-2 allows the relaxation of the usual type checking by way of so-called type-transfer functions. Type transfers force the compiler to interpret data in a different way. The statement BITSET (i) interprets the integer variable i as a collection of bits, which you can then set or test in subsequent statements.

Every Modula-2 compiler includes a module named SYSTEM that specifies any low-level, hardware-dependent features. Two examples of such hardware-dependent features are the ADDRESS and WORD types, which let you define the number of bits in a memory address and the width of a computer word, respectively.

All Modula-2 compilers have some basic definitions in

An annotated Modula-2 bibliography

There's no dearth of books on Modula-2; indeed, if you're a newcomer to the language, you'll find too many to make an easy choice. The following list distinguishes the reference works from the tutorials and may help you to find the book that best suits your purpose. All the books listed assume some previous programming experience, which is unfortunate, because Modula-2 is an excellent first programming language. You should be able to find most of these books in any bookstore that has a respectable computer section.

Wirth, Niklaus, Programming in Modula-2, second and third editions, Springer-Verlag, New York, NY. This authoritative language definition, includes good coverage of programming generally and Modula-2 specifically. It also contains many useful example programs. This book is a must for everyone who is serious about learning Modula-2. The index is poor. The third edition covers revisions and clarifications to the original language, but is otherwise identical to the second edition. Many commercial compilers have not implemented the third-edition changes, or have implemented only some.

Kaplan, Ian, and Mike Miller, Modula-2 Programming, Hayden Book Co, Hasbrouck Heights, NJ. This beginner's text is probably the easiest book from which to learn the language. All the basics are covered; advanced topics such as multiprocessing, low-level facilities, and advanced programming concepts are omitted.

Knepley, Ed, and Robert Platt, Modula-2 Programming, Reston Publishing Co, Reston, VA. This introduction to Modula-2 is intended for the experienced programmer and lacks the step-by-step approach needed by those new to programming. The topical organization is fairly good, and the coverage is balanced. It uses a simple word processor as an extended example.

Ogilvie, John W L, Modula-2 Programming, McGraw-Hill, New York, NY. This excellent introduction to Modula-2 for the experienced programmer covers all aspects of the language, including the clarifications, changes, and extensions from the third edition of Wirth's book. It contains many examples, and it has five appendixes, a glossary, and an index.

Gleave, Richard, Modula-2 for Pascal Programmers, Springer-Verlag, New York, NY. This book is short, well organized, and lives up to its title quite well. All new concepts are explained with the aid of examples. It is based on Volition System's compilers (which I believe are now sold by Pecan), and it contains a fair index.

Sale, Arthur, Modula-2 Discipline & Design, Addison-Wesley, Reading, MA. This solid textbook approach to learning Modula-2 from scratch is a fairly thorough and even treatment of all aspects of the language and includes a description of several compilers. It stresses program design through step-wise refinement, formal correctness proofs, and the analysis of language construct semantics.

Kaare Christian, A Guide to Modula-2, Springer-Verlag, New York, NY. This is the best book on Modula-2 for programmers with a reasonable amount of experience with Pascal or C. The author provides many insights into the power of the language through useful examples. The
the SYSTEM module. In addition, the language definition allows compiler implementors to put additional machine-specific features in the module, such as gaining direct access to the CPU registers. Another candidate for the SYSTEM module would be a CODE procedure that allows in-line machine code; the preferred approach to integrating assembly language routines, however, is to use the standard assembler and then link the resulting object modules in the program module.

Using the facilities of the SYSTEM module guarantees portability problems. However, if you want direct access to the hardware, you usually have no other option. You should restrict your use of such nonportable features to one module of your program, and then clearly label that module as machine specific.

Modula-2 includes all of Pascal's loop and decision constructs, but with a more consistent syntax. WHILE, REPEAT, and FOR allow loops to be terminated at the top or bottom only; a new LOOP statement, with an optional EXIT, allows infinite loops as

book covers all aspects of the language, including systems programming and hardware.

Ford, Gary A, and Richard S Wiener, Modula-2—A Software Development Approach, John Wiley & Sons, New York, NY. This book takes a more rigorous approach than many of the volumes listed above, and emphasizes software engineering. It provides very good coverage of the entire language and includes many useful examples.

Schmidt, Herb, Advanced Modula-2, Osborne/McGraw-Hill, New York, NY. There is nothing particularly advanced about this book. This volume really is, in fact, a good collection of standard algorithms cast in Modula-2 code. It includes sorting/searching, queues/stacks/lists/trees, and simple statistics.

Ward, Terry A, Advanced Programming Techniques in Modula-2, Scott, Foresman and Co, Glenview, IL. This is a collection of code fragments (with text) taken from several magazines. It contains several extensive bibliographies, and it also describes the complete Modula-2 syntax through a series of lists and tables.

Sincovec, Richard F, and Richard S Wiener, Data Structures Using Modula-2, John Wiley & Sons, New York, NY. Although this book seems to mirror Wirth's book (see above), the emphasis is very different; these authors look at real applications of the algorithms. For example, polynomial arithmetic and sparse matrices are developed as examples of linked list applications. Under stacks and queues, you'll find an example of adaptive numerical integration using the trapezoid method and Simpson's method.

Wirth, Niklaus, Algorithms & Data Structures, Prentice-Hall Inc, Englewood Cliffs, NJ. This is Wirth's famous Algorithms & Data Structures=Programs, re-cast in Modula-2. The coverage of standard algorithms includes searching/sorting, recursion, queues/stacks/lists/trees, and hashing. Besides presenting and explaining the code, it often gives detailed mathematical analyses and results of empirical tests. Although Wirth has updated some sections based on recent discoveries, I feel this book is worthwhile only if you don't have his earlier (Pascal-based) volume.

Sincovec, Richard F, and Richard S Wiener, Software Engineering with Modula-2 and Ada, John Wiley & Sons, New York, NY. This book isn't on Modula-2 and therefore doesn't cover the language itself, but it does give excellent insights into using Modula-2 on large programming projects. The book presents its main topics (software engineering, specification, design, style, methodology, and testing) in the context of Modula-2 and Ada. A simple spelling checker serves as a programming example.

Pomberger, Gustav, Software Engineering and Modula-2, Prentice-Hall International, Englewood Cliffs, NJ. Although this book covers the complete Modula-2 language (including a descriptive chapter and reprinting Wirth's Modula-2 report), its main focus is software design. Some of its topics include choosing a language, the software life cycle, modular programming and team-software development, and project management. It's a well-organized and thorough presentation.
Modula-2 is a small language that contains only 40 keywords; consequently, it's easy to learn.

well as loops that terminate in the middle. Listing 5 shows an example of each type of loop. Note that Modula-2 does not use the keyword BEGIN in these loops; however, the END statement is always required (whether there is one statement or many in the loop).

In Modula-2, the IF-THEN-ELSE statement also has an optional ELSIF part, which prevents multiple ELSE IF statements from marching off the right side of the page. Again, these constructs don't use BEGIN but do require END statements. The Modula-2 CASE statement, too, includes an ELSE part—something that standard Pascal lacked. Listing 6 shows examples of these constructs.

When students start to program in Pascal, one of the first things they learn is that a semicolon separates one statement from the next. Nevertheless, they often have trouble determining what constitutes a statement. Students have come up with variations of the following in a nonfunctioning program when they dutifully put a semicolon between each "statement":

```
IF <condition> THEN;
BEGIN
<some statements>
END;
```

Of course, the statements are always executed (regardless of the condition), because the semicolon after the THEN terminates the IF statement. This problem could not occur in Modula-2, because only an END can terminate an IF statement. In the example below, the compiler interprets the semicolon as just another (null) statement and ignores it.

```
IF <condition> THEN;
<some statements>
END;
```

Summing up Modula-2's salient features

Modula-2 has many desirable characteristics, of which the most important is the ability to decompose a problem into separately compilable modules. The language provides strict control over data typing and access to data items. Furthermore, the compiler provides cross-module checking (a feature not available in C or Fortran) to ensure that each module passes the correct number and type of parameters to the next module. And finally, Modula-2 provides the flexible access to hardware often needed for systems programming and for embedded-controller applications.

Before buying a compiler, you'll want to know something about the products available. The remainder of

---

**LISTING 5—EXAMPLES OF LOOP STRUCTURES**

```
WHILE x > epsilon DO
  x := x - y[i];
  INC (i); (* built in function replaces i := i + 1 *)
END;

REPEAT
  x := x * factor;
UNTIL x >= y;

FOR i := 20 TO 0 BY -1 DO (* If BY omitted, assumes 1 *)
  x[i] := 0.0;
END;

LOOP
  ReadInt (x); (* Read an Integer from Console *)
  IF x < 0 THEN
    EXIT;
  END;
  sum := sum + x; (* could also use INC (sum, x); *)
END;
```
this article consists of some observations that I have gradually collected as I tried to choose the best systems to work with—they do not constitute a detailed review of the available microcomputer implementations of Modula-2. For books about Modula-2, refer to the box, "An annotated Modula-2 bibliography."

You’ll find three classes of Modula-2 compilers. The first class is based on the original 4-pass compiler, which Wirth’s group at ETH (Eidgenossische Technische Hochschule, Zurich, Switzerland) developed. This compiler was first implemented on the PDP-11, and later on Lilith and many other microcomputers. The 4-pass compilers are very reliable and produce very good code; they are, however, a bit slow.

The second class is based on Wirth’s 1-pass compiler, also from ETH. Naturally, these compilers are faster, but some compromises were necessary to allow compilation in one pass over the source code (for example, you need FORWARD declarations for mutually recursive procedures). The original 1-pass compiler was implemented on Lilith (Wirth’s bit-slice microcomputer). It was fast, compact, and produced tight code. Moving this design to other computers has not always been wholly successful; for instance, when ETH ported it to the 68000, the object code of the compiler increased from 26,050 bytes to 83,450 bytes, and execution times were proportionately longer. Although Wirth concluded that the 68000 architecture is ill-suited to running compilers, it may be that the 1-pass compiler is too heavily dependent on the special features of the Lilith.

The third class includes what can only be described as “everything else.” The majority of commercial compilers are ports of one of the ETH designs; however, a few companies have elected to design their compilers independently. It’s impossible to generalize about these.

A compiler should adhere completely to the language definition (Programming in Modula-2, by Niklaus Wirth, second or third edition). Wirth did provide for extensions in two ways: extra library modules and extensions to the internal pseudomodule, SYSTEM. You shouldn’t tolerate other extensions because of their adverse effect on portability. A compiler should also produce code that is compact and executes quickly. It’s an added bonus if the compiler itself is also fast. The compiler manual should provide a description of the language as implemented, as well as a description of all library modules that come with the system. Table 1 contains a summary of evaluations (including a Sieve benchmark) based on the previous criteria.

Compilers for the IBM PC

The MS-DOS compiler from Logitech Inc (Redwood City, CA) is a solid implementation of the ETH 4-pass compiler. Even the stripped-down version for $89 is very complete. For a few dollars more, you can have useful utilities and 8087 support. The Logitech compiler produces reasonably good code and seems to be essentially bug free. The package includes one of the best programming editors that I have used—it is fast and has all of the features that programmers need. The manual is well organized and complete, but the index is poor. The Logitech compiler is the best one in its class.

The company has recently released the third version of this compiler, which brings it into line with Wirth’s third-edition changes. A further enhancement is an intelligent linker, which links in only those procedures that are referenced (not a complete library). This feature should reduce the size of executable files. Unfortunately, Logitech did not respond to my request for a review copy, so I cannot judge how successful the changes are. However, the Logitech compiler has always been a solid product, and there is no reason to believe that the latest version would be anything less.

Modula Corp’s (Provo, UT) port of Wirth’s 1-pass compiler is a disappointment to me. Although this MS-DOS compiler is fast (linking is fast, too), the generated code size is at least 50% larger than that of the Logitech product. Being a new product, this compiler contains a few bugs—after one week of use, I uncovered a bug that Modula Corp hadn’t seen before. The accompanying manual is excellent. If you’re in a hurry and don’t mind the $300 price tag, buy this

---

**LISTING 6—IF . . . THEN . . . ELSE STRUCTURE**

```
IF x = y THEN
 done := TRUE;
ELSIF x = 0 THEN
 underflow := TRUE;
ELSE
 x := x * delta;
END;

CASE code OF
 1 : Process;
 2 : Repeat;
 3 : Abort;
ELSE
  Error;
END;
```
All of the data types available in Pascal are also available in Modula-2, along with some new data types for low-level access to the computer hardware.

compiler; if you want the best results (smallest code and fastest execution) at a reasonable price, choose Logitech.

The Modula-2 Software Development System (M2SDS) from Interface Technologies (Houston, TX) is a complete MS-DOS programming environment, including clock, calculator, ASCII chart, editor, compiler, linker, and other utilities. M2SDS includes a syntax-directed editor, which responds only to special control codes: If you want a FOR loop, type Alt-F; if you want a PROCEDURE call, type Alt-P (and then fill in the blanks). If you're an experienced programmer or a good touch typist, you probably won't want this system—the syntax-directed editor is just too restrictive. For the beginner, however, it’s perfect.

The editor acts as the first compiler pass. The compiler and linker are fast and produce tight code which, however, may execute very slowly. The Sieve runs very quickly (second fastest of all MS-DOS compilers), but a program to strip the high bit from all characters of a Wordstar file took 10 times longer than the same program compiled by the Logitech compiler. (I suspect that Interface Technologies isn't making proper use of buffering, but rather is calling the operating system on each read/write request.)

The latest release has corrected many of the bugs from which earlier versions suffered; nevertheless, the system often crashed when I used the back-tab key to move through the source text. I haven’t seen the latest manual because it was being revised and reprinted when the company sent me the new evaluation disks. The original manual was fairly good, but could benefit from a better index and some reorganization.

The 2-pass MS-DOS compiler from Farbware (Wilmette, IL) implements the complete Modula-2 language, with some nice extensions. The compiler is reasonably fast (faster than Logitech's, but slower than Modula Corp's or Interface Technologies'), but several problems make this package unacceptable. First, the manual is incomplete (half of it is on disk) and not well organized. Second, the system uses the DOS linker, which means that you have to specify all object files.

### TABLE 1—MODULA-2 COMPILER SUMMARY

<table>
<thead>
<tr>
<th>Implements Standard Language</th>
<th>Supplies Standard Library</th>
<th>Execution Speed (Sieve) (SEC)</th>
<th>Code Size (Sieve)</th>
<th>Compile and Link Speed (Sieve) (SEC)</th>
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<tr>
<td>Logitech</td>
<td>Yes</td>
<td>20</td>
<td>13k</td>
<td>50</td>
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<tr>
<td>Modula Corp</td>
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<td>23</td>
<td>19k</td>
<td>10</td>
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<td>Interface Technologies</td>
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<td>10k</td>
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<td>NO²</td>
<td>42</td>
<td>26k</td>
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<tr>
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<td>NO⁴</td>
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<td>5k</td>
</tr>
<tr>
<td>Hochstrasser</td>
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<td>NO⁶</td>
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<td>5k</td>
</tr>
<tr>
<td>Turbo</td>
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<tr>
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<td>NO¹⁰</td>
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<td>MacMeth</td>
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<td></td>
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<td>19</td>
</tr>
</tbody>
</table>

NOTES:
1. INCLUDES SEVERAL EXTRA DATA TYPES.
2. OMITS SUPPORT FOR PROCESSES AND INTERRUPTS (SUPPLIED VIA NONSTANDARD MODULES).
3. USES AUTOMATIC REGISTER VARIABLES TO SPEED EXECUTION—PREVENTS STANDARD ADR PROCEDURE FROM BEING USED ON SIMPLE VARIABLES.
4. INCLUDES SEVERAL DUBIOUS EXTENSIONS; OMITS SUPPORT FOR PROCESSES AND INTERRUPTS (SUPPLIED VIA NONSTANDARD MODULES). OMITS MONITORS.
5. ALTERS OR OMITS SOME LOW-LEVEL FACILITIES.
6. DUE MOSTLY TO NONSTANDARD FILE MODULES.

STANDARD LANGUAGE MEANS NO EXTENSIONS OR OMISSIONS THAT DO NOT CONFORM TO WIRTH. THE STANDARD DOES PERMIT EXTENSIONS TO THE SYSTEM MODULE.

STANDARD LIBRARY TO INCLUDE AT LEAST TERMINAL, INOUT, FILESYSTEM, AND MATHLIB AS DEFINED BY WIRTH.

HARDWARE: IBM PC/XT WITH 20M-BYTE HARD-DISK DRIVE. Z80 S100 WITH 1.2M-BYTE 8-IN. FLOPPY-DISK DRIVES. ATARI 520-ST WITH 800K-BYTE 3.5-IN. FLOPPY-DISK DRIVES. MAC PLUS WITH 800K-BYTE 3.5-IN. FLOPPY-DISK DRIVES.
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Every Modula-2 compiler includes a module named SYSTEM that specifies any low-level, hardware-dependent features.

found that I was constantly getting UNRESOLVED REFERENCE errors because I had forgotten that module X imports module Y, which imports module Z. Other Modula-2 linkers find all the files for you from the import lists. Third, the code produced is both too large and too slow. There is considerable potential here, however, and the company plans to improve both the manual and the compiler.

Workman & Associates (Pasadena, CA) offers FTL Modula-2 for IBM PCs and compatibles. FTL stands for "faster than light," which is a claim that this compiler can usually fulfill. This nicely integrated system consists of an editor, a compiler, and a linker. Compiling and linking can both be done from the editor; if either the compiler or the linker detects an error, it will return you to the editor with the cursor positioned at the source-code line that caused the error.

The original FTL Modula-2 was written for the CP/M operating system, and the MS-DOS version suffers from that lineage in at least two ways. First, the library was rather hastily ported from the CP/M version, and the haste shows. Second, the manual consists of two separate booklets: One of these is generic and covers both versions of the compiler; the other is an MS-DOS supplement. Neither booklet contains the definition modules for the library—an omission that I find unacceptable, considering how often you need to consult these modules when you're coding.

FTL Modula-2 contains some dubious extensions that can only hamper portability; it also has a few omissions that may frustrate advanced users. Although the compiler does produce very good code (fastest and smallest code generated by any MS-DOS compiler), there is no disk buffering in the Files library module.

Because of this restriction, a program to convert a Wordstar file to plain ASCII took more than eight times longer to execute than the same program compiled with the Logitech compiler. When I rewrote the program to do its own disk buffering, the performance improved by a factor of 16. This compiler would have great promise if the vendor were to improve the library and the user's manual and were to adhere more closely to the language definition. The current version is limited to the small-memory model; a version for the large-memory model is reportedly coming soon.

Workman & Associates also offers a CP/M version of FTL Modula-2, which isn't as fast as the MS-DOS version. The CP/M version is a 1-pass compiler developed independently in Australia. It is fast, but the necessary linking step is quite slow. The manual suffers from the same deficiencies as does the MS-DOS version (split into reference manual and CP/M supplement and lacking library definitions). The package includes a fairly decent programming editor (available in Modula-2 source code for an extra charge). When I tried to compile a large program (which compiled properly on Hochstrasser's compiler), FTL froze up solid after an OUT OF MEMORY message. The latest version is little changed from the one I purchased 18 months ago—the company seems to be concentrating on the MS-DOS version.

Hochstrasser Computing AG (Rebhaldenstrasse 27, 8704 Herliberg, Switzerland) offers a solid implementation of the ETH 4-pass compiler. In some ways (module size, procedure size), it is less restrictive than the Logitech compiler. It produces excellent code (often better than Turbo Pascal) and is very complete—including source code for the library—but implements processes and interrupts in a slightly nonstandard (though quite usable) fashion. This is the first Modula-2 compiler that I used, and is still the one that I prefer for CP/M. It follows the second edition of Wirth's book. The manual, though not as comprehensive as Modula Corp's, is well organized and complete.

The CP/M Turbo Modula-2 from Echelon Inc (Los Altos, CA) is a port of Wirth's latest compiler, which produces M-code in one pass. A second pass is required to produce native Z80 code. Native code is faster than M-code, but takes up more room in memory. The compiler and linker are quick and produce fast-executing, tight code. Because it was originally developed by Borland, the compiler has many nonstandard extensions, both to the language and to the library; a compiler switch allows Turbo Modula-2 to emit a warning when most nonstandard extensions are used (a few extensions do pass unnoticed). When producing native Z80 code, the size of the program that it can handle is somewhat smaller than the other CP/M compilers. It also contains some bugs: HALT won't work from module initialization (it acts like RETURN), and mixing M-code and native code sometimes causes unpredictable results (though the manual says that such a mix is allowed). The manual is excellent.

Compiler for the Atari 520-ST

TDI Software Inc (Dallas, TX) offers a good implementation of the ETH 4-pass compiler, which allows access to most of the operating system and graphics features of the Atari. This package includes the best linker that I've seen; it optimizes by scanning through
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Compiler for the Macintosh
Macmeth from Modula Corp is another implementation of Wirth's 1-pass compiler that a team from ETH ported to the Apple Macintosh. This development system employs the usual Macintosh environment, but is not as slick as other Macintosh compilers; for instance, after starting the compiler or linker, you receive prompts for file name and options in much the same manner you would expect if you were operating under CP/M. The editor is also crude by Macintosh standards. The compiler is fast, as is execution speed of the generated code, but, after linking, the code size is far too large. It does includes an excellent run-time symbolic debugger.

Author's biography
Brian Anderson is an instructor in the Electronics Dept of Vancouver Community College (British Columbia, Canada), where he teaches courses in telecommunications. He has been involved in both the hardware and the programming sides of the computer industry for more than a decade, and has contributed many articles to Dr. Dobb's Journal and BYTE. In his spare time he enjoys playing the guitar and reading.
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Tachometer measures low frequencies

Ricardo Jimenez-G
Mexicali Technological Institute, Mexicali, Baja California, Mexico

The Fig 1 tachometer lets you measure heartbeats, respiratory rates, and other low-frequency events that recur at intervals of 0.33 to 40.96 sec. The circuit senses the period of $f_{IN}$, computes the equivalent pulses per minute, and updates the LCD accordingly. (Although the decimal readout equals 60$f_{IN}$, the circuit doesn't actually produce a frequency of 60$f_{IN}$.) The computation involves counting and comparison techniques and takes 0.33 sec.

To understand the circuit's operation, suppose a reset pulse arrives at pin 15 of IC1, setting $Q_1$ and $\bar{Q}_1$ low. Then, the first $f_{IN}$ pulse drives $Q_1$ high, which opens the IC3A gate and allows 100-Hz pulses to drive the counter IC6. The next $f_{IN}$ pulse drives $Q_1$ low and $\bar{Q}_1$ high, which simultaneously freezes IC6 at a count of N by turning off the 100-Hz pulses. The same $f_{IN}$ pulse opens the gate IC8A, which allows 18-kHz pulses to drive the IC7 counter.

Each time IC7 reaches a count equal to that of IC6, the IC7-IC8 comparator produces a pulse that increments the display counter IC11 and resets IC7 via IC10. Thus, IC7 counts at a rate of 18 kHz without interruption and resets to zero after every N counts. (N is proportional to the period of $f_{IN}$.) This process terminates at 6000 counts, when the BCD counters IC9 (count of 100) and IC10 (count of 60) produce a pulse at pin 11 of IC10 that resets IC7, IC6, IC8, and IC9. The reset at pin 15 of IC1 drives $Q_0$ (pin 3) high, which in turn resets the display counter and updates the display.

An $f_{IN}$ of 1 Hz, for instance, sets IC4 to a binary count of N=100. Consequently, IC7 counts 60 times from 0 to 100 during the 6000-count interval, producing a readout of 60. Similarly, $f_{IN}$=1.25 Hz produces N=80 and sets the readout to $6000/80=75$ pulses per minute.

To Vote For This Design, Circle No 746

Fig 1—This tachometer circuit generates a readout, in pulses per minute, by measuring the period $T$ of $f_{IN}$ and solving the equation $f=\frac{60}{T}$. 

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Chopper amplifier stabilizes 3-amp system

Robert Pease
National Semiconductor Corp, Santa Clara, CA

A chopper-stabilized amplifier can greatly improve the voltage offset and drift for a single op amp, but a differential-input stabilizing amplifier—IC₄ in Fig 1—can do the same for a complete 3-amplifier system. IC₄ forces the system's output offset to zero by sensing the input offsets of IC₁ and IC₃, subtracting a fraction of the IC₁ offset, and canceling the resulting quantity with a servo-adjusted offset at IC₃.

In the system shown, IC₁ is the output amplifier for a current-output D/A converter, IC₂ performs a sample/hold function, and IC₃ is an output summing amplifier. (This offset-cancellation scheme suits two, three, four, or more inverting amplifiers, but the author does not believe it is applicable for noninverting amplifiers.) The example features inexpensive op amps that spec 10-mV max V_{os}, yet the output offset measures 50 µV. The drift is only 0.5 µV/°C, in contrast with the 30-µV/°C max drift you would obtain using low-temperature-coefficient LF411As. You can also use lower-drift LM607s or µA714s, but these devices settle six times more slowly than the quicker, driftier LM347s.

You may consider drift in the second or third amplifier negligible if your first amplifier has high gain. But if the output amplifier is a power device, this stabilization approach can improve system accuracy by chopping out large offset and thermal errors contributed by the power amplifier, along with the drift and offset from the other amplifiers.

Note that the sample/hold circuit in Fig 1 allows you to demultiplex the D/A-converter signal to other channels. (The signal of one such channel reconnects to the system at V_{IN}.) Such an arrangement allows a step change at IC₁'s output while IC₂ is in the hold mode (S₂ open). Unless you make a provision to freeze IC₁'s output by disabling its clock (S₁ closed), the resulting change in IC₂'s load current can introduce a substantial error in the stabilizing loop. With the clock disabled, the output drift consists of about 1 µV/sec from IC₄ plus an additional 10 µV/sec from IC₂.

If your circuit doesn't include a sample/hold function, you can use a low-drift LM607 or LM11A op amp in

---

**Fig 1—Addition of the stabilizing circuit** (within the dotted lines) eliminates offset at V_{out} by adjusting the offset at IC₄ to null the combined offsets of IC₁ and IC₃.

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place of the LM669. Although slightly inferior to the LMC669 in offset and drift, these amplifiers offer advantages: The LM11A's input offset current is only 10 pA from 0 to 70°C, and the LM607, although its input offset current is 1 nA, offers considerably lower noise in a low-impedance circuit.

Correct operation of the Fig 1 circuit depends on proper values for the gain resistors R₁-R₄. You can calculate the values easily using Eq 7, derived in the following algebraic manipulations.

Referring to the general, simplified schematic of Fig 2, let

\[ R = R₄ + R₃ = R₆ + R₇, \]

where \( R \) is much greater than \( R₁, R₂, \) or \( R₃ \). For each amplifier, assume that \( Iₛ \) is much less than \( Vₒs/R₁ \) or \( Vₒs/R₂ \), etc. Then, the output voltage of each amplifier is

\[
V₄ = V₁(K + 1) + (V₁ - V₃) \left( \frac{KR₁}{R} \right) \tag{1}
\]

\[
V₅ = V₂ \left( L + 1 + \frac{LR₂}{R₁} \right) - LV \tag{2}
\]

\[
V₆ = V₃ \left( M + 1 + \frac{MR₃}{R} \right) + (V₅ - V₁) - MV₅, \tag{3}
\]

where the respective input offset voltages are \( V₁, V₂, \) and \( V₃ \). By neglecting the signal terms and substituting Eq 1 into Eq 2, then Eq 2 into Eq 3 and collecting like quantities, you obtain an equation for the output \( V₆ \) in terms of the input offset voltages:

\[
V₆ = V₃ \left( M + 1 + \frac{MR₃}{R} \right) + V₁ \left( ML(K + 1) + \frac{MLKR₁}{R} - MR₃ \right) - V₂ \left( L + 1 + \frac{LR₂}{R} \right).
\]

The desired condition is \( V₆ = 0 \). Therefore,

\[
V₆ = aV₃ + bV₁ - cV₂ = 0, \tag{4}
\]

where

\[
a = M + 1 + \frac{M}{N} + \frac{MR₃}{R} - \frac{MLKR₁}{R},
\]

\[
b = ML(K + 1) + \frac{MLKR₁}{R} - MR₃,
\]

\[
c = M \left( L + 1 + \frac{LR₂}{R} \right).
\]

Rearranging Eq 4 yields

\[
V₃ \left( \frac{a}{a + b} \right) + V₁ \left( \frac{b}{a + b} \right) = V₂ \left( \frac{c}{a + b} \right).
\]

Noting that

\[
V₇ = V₁ \left( \frac{R₆}{R₄ + R₆} \right) + V₃ \left( \frac{R₄}{R₄ + R₆} \right), \tag{5}
\]

and

\[
V₈ = V₂ \left( \frac{R₇}{R₆ + R₇} \right), \tag{6}
\]

you can see that IC₄ nulls the effect of op-amp offset voltages by forcing \( V₇ \) to equal \( V₈ \). Simply choose

\[
R₄ = R \left( \frac{a}{a + b} \right),
\]

\[
R₅ = R \left( \frac{b}{a + b} \right),
\]

\[
R₇ = R \left( \frac{c}{a + b} \right),
\]

\[
R₆ = R \left( \frac{a + b - c}{a + b} \right)
\]

and substitute into Eqs 5 and 6 to get the desired relationship:

\[
V₇ = V₁ \left( \frac{b}{a + b} \right) + V₃ \left( \frac{a}{a + b} \right) = V₂ \left( \frac{c}{a + b} \right). \tag{7}
\]

In Fig 1, for example, \( R₁ = 10 \, kΩ, R₂ = 5 \, kΩ, R₃ = 10 \, kΩ, R₆ = 100 \, kΩ, K = 0.625, L = 1.0, M = 0.4, \) and \( N = 1.0 \), yielding \( a = 1.815, b = 0.635, \) and \( c = 0.85 \). Therefore, \( R₆ = 65.31 \, kΩ, R₇ = 34.69 \, kΩ, R₄ = 74.08 \, kΩ, \) and \( R₅ = 25.92 \, kΩ \). All gain resistors should have a tolerance of ±1% min for the offset subtraction to work; ±0.1% is even better.

**To Vote For This Design, Circle No 750**
Circuit converts pulse train to sinusoid

Frantisek Michele  
Brno, Czechoslovakia

The Fig 1 circuit lets you convert a serial pulse stream (or sinusoidal input) to a sinusoidal output at \( \frac{1}{2} \) the frequency. By varying the frequency of \( V_{\text{IN}} \), you can achieve an output range of \( 10^7 : 1 \) from about 100 kHz to less than 0.01 Hz. The output resembles that of a 5-bit D/A converter operating on parallel digital data.

Counter IC\(_1\) generates binary codes that repeatedly scan the range from 00000 to 11111. The output amplifier adds the corresponding XOR gate outputs (\( V_{\text{DD}} \) or ground), weighted by the values of input resistors R\(_1\) through R\(_4\). The 16 counter codes 00000 to 01111, for instance, pass unchanged to the XOR gate outputs and cause \( V_{\text{OUT}} \) to step through the half-sinusoidal cycle from maximum amplitude to minimum amplitude.

Counter output Q\(_0\) goes high for the next 16 codes, causing the XOR gates to invert the Q\(_0\) through Q\(_5\) outputs. As a result, \( V_{\text{OUT}} \) steps through the remaining half cycle from minimum amplitude to maximum amplitude. The counter then rolls over and initiates the next cycle. You can change the R\(_1\) through R\(_4\) values to obtain other \( V_{\text{OUT}} \) waveforms. \( V_{\text{DD}} \) should be at least 12V to assure maximum-frequency operation from IC\(_1\) and IC\(_2\).

Pushbutton sequence disarms burglar alarm

John McCluskey  
Jet Propulsion Laboratory, Pasadena, CA

The alarm circuit of Fig 1 is suitable for use in a vehicle or for guarding a residence. To regain entry, you disarm the circuit by pressing the pushbutton switches S\(_1\)–S\(_9\) in a programmed 7-digit sequence (one of 16,384 such sequences). The Abel design file Listing 1 programs the PLA IC\(_2\), which includes a 3-bit state machine that decodes the disarming sequence.

Controls include an on/off key switch (S\(_0\)), an arming switch (S\(_a\)), multiple door and window switches (S\(_1\)–S\(_9\), S\(_a\)), and a pushbutton sequence disarms burglar alarm.
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SPECIFICATIONS

<table>
<thead>
<tr>
<th>MODEL</th>
<th>FREQUENCY MHz</th>
<th>GAIN, dB (min.)</th>
<th>MAX POWER OUTPUT dBm (typ)</th>
<th>NF dB (typ)</th>
<th>PRICE $</th>
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<td>20</td>
<td>+17**</td>
<td>7.0</td>
<td>219.00</td>
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</tbody>
</table>

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CIRCLE NO 107

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with which you can connect more switches in series), and the combination switches ($S_1$-$S_4$). You should construct a tamper-proof outside box that contains only the combination switches and the red/green status LEDs, making sure that a thief (or an engineer!) can't destroy the circuit from the outside box. The combination switches can withstand 120V ac, 60 Hz. Applying this fault voltage to an external-status LED line triggers

Fig 1—This burglar alarm can be deactivated by pressing the correct 7-digit sequence on pushbutton switches $S_1$-$S_4$. 

EDN March 3, 1988
Full 32-bit performance for less than $30? Believe it.

That's right. The Z320 breaks the buck-a-bit barrier. And you don't have to give up a thing. Just think of the possibilities. All that performance available for a whole new range of applications. Like yours. But we know the Z320 probably sounds a little too good to be true.

What's the catch?

There isn't any. The Z320 gives you everything you expect from a 32-bit chip. In fact, the Z320 offers plenty you don't get with most of the high-priced 32-bit offerings: a dual-ported cache for instructions and data, a demand paged virtual memory management system, dual execution in the six-stage pipeline with two ALUs, dual-port access to a large general purpose register file, programmable wait states, and bus-width for two areas in memory, I/O and interrupts, bus scaling that allows cost memory, to mention just a few.

How can you do it so cheap?

First of all, the Z320's H-MOS technology is less expensive. And the smaller PLCC package and lower transistor count give you savings without giving up crucial performance. In short, the Z320's technology offers full 32-bit performance for the price of the aging 286.

Why are you doing this?

The real question is, "Why isn't anybody else producing an affordable 32-bit microprocessor?" We designed the Z320 to open the door to 32-bit performance for any cost-sensitive applications that can use 32-bit engines as peripheral processors or as embedded, non-programmable processors. Laser printers, copiers, synthesizers, for instance.

There's a lot more to tell you about the unbelievable Z320. But affordable 32-bit performance, off the shelf, backed by Zilog's proven quality and reliability ought to give you something to think about. Contact your local Zilog sales office or your authorized distributor today. We'll make a believer out of you. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

The choice is clear.

Zilog
the alarm and blows a fuse by driving current through one of the zener diodes D1 and D2, thereby protecting IC2.

To disarm the circuit, enter the combination or use S9 to turn the alarm off, then on. Either action should activate the red (disarmed) status LED. To reset the alarm, open S9, close all window and door switches, and initiate the armed state by pressing S6 or S4. The switch-debouncing networks provide positive feedback to the switch inputs.

---

**LISTING 1—PLA PROGRAM**

module ONE_CHIP_ALARM
flag '-r3','-T4','-W7,6,8,12,13,14,15,16,17,18,19'
title 'One Chip Combination Alarm, John McCluskey'

ALRM device 'PL6V8R'; "Lattice GAL16V8 reprogrammable PAL"

Clk pin 1; "State machine clock input"
SW1 pin 2; "Switch 1, Active High input"
SW2 pin 3; "Switch 2, Active High input"
SW3 pin 4; "Switch 3, Active High input"
SW4 pin 5; "Switch 4, Active High input"

ALRM1 pin 6; "Alarm input, active high [switch opens]"
ALRM2 pin 7; "Alarm input, active high [switch opens]"
ALRM3 pin 8; "Alarm input, active high [switch opens]"

ALARM OFF pin 9; "Input, turns alarm OFF, active low"
OE pin 11; "Output Enable (grounded)"

ALARMLOW pin 12; "combinatorial output, active low"

ALARMHI pin 13; "combinatorial output, active high"

Q2 pin 14; "registered output, State machine bit 2"
Q1 pin 15; "registered output, State machine bit 1"
Q0 pin 16; "registered output, State machine bit 0"

DISARMED pin 17; "combinatorial output, active high"

ARMED pin 18; "combinatorial output, active high"

CLKOUT pin 19; "combinatorial clock output (fed back to pin 1)"

SW = [SW4,SW3,SW2,SW1]; "Switch push vector"
Q = [Q2,Q1,Q0]; "state machine vector"
S0,S1,S2,S3,S4,S5,S6,S7 = 7,6,5,4,3,2,1,0; "machine states"

STEP1 = 1; "combination of lock is defined here"
STEP2 = 2; "each step has 4 possible values, 1, 2, 4, or 8"
STEP3 = 4; "so the total number of combinations is 16384"
STEP4 = 8;
STEP5 = 1; "The combination may changed at anytime by reprogramming"
STEP6 = 2; "the GAL16V8"
STEP7 = 4;

equations
CLKOUT = SW1 # SW2 # SW3 # SW4 # !ALARM OFF;

ARMED = (Q != S7); "These complimentary outputs drive a bi-color LED"
DISARMED = (Q == S7); "Which indicates ARMED, DISARMED, or power failure"

"The alarm outputs are programmed as an RS flip flop, to make the"
"alarm condition self latching when a door/window switch is opened"
"Once latched, the alarm can be reset only by grounding the ALARM OFF"
"input, or by putting the state machine Q into state S7 (DISARMED)"

!ALARM LOW = ALARM OFF & DISARMED & (ALRM1 # ALRM2 # ALRM3 # ALARM HI);
ALARM HI = ALARM OFF & DISARMED & (ALRM1 # ALRM2 # ALRM3 # !ALARM LOW);

"The finite state machine Q typically starts from state S0 and is incremented"
"up to state S7 (the DISARMED state) by the correct sequence on the switch"
"vector. Turning the alarm OFF forces Q to state S7"
Meeting tough specs like WS6536E (weapons) and DoD 2000 is as easy as saying KEMET®.

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KEMET Electronics Corporation

EDN March 3, 1988
Program divides 32-bit by 16-bit numbers

Ashmead Ali  
Caribbean Industrial Research Institute, Trinidad and Tobago

The re-entrant, 8085 assembly-language program shown in Listing 1 performs division of 32-bit by 16-bit unsigned numbers. Register BCDE (B contains the most significant byte) holds the dividend and quotient; register HL holds the remainder. Memory locations DIVS and DIVS+1 (the latter holds the least significant byte) store the 16-bit divisor. This program is an adaptation of Intel's 16-bit by 16-bit divide algorithm—see Intel’s 8080/8085 Assembly Language Programming Manual, Chapter 6, pgs 6 to 10.

To Vote For This Design, Circle No 747

---

**LISTING 1—32-BIT BY 16-BIT DIVIDE ROUTINE**

<table>
<thead>
<tr>
<th>DIV:</th>
<th>LHL D DIVS</th>
<th>; negate the divisor</th>
<th>RAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOV</td>
<td>A , L</td>
<td>MOV A , L</td>
<td>MOV D , A</td>
</tr>
<tr>
<td>CMA</td>
<td>MOV L , A</td>
<td>CMA MOV A , C</td>
<td>MOV A , C</td>
</tr>
<tr>
<td>MOV</td>
<td>A , H</td>
<td>MOV L , A</td>
<td>MOV A , B</td>
</tr>
<tr>
<td>CMA</td>
<td>MOV H , A</td>
<td>CMA MOV A , B</td>
<td>MOV B , A</td>
</tr>
<tr>
<td>MOV</td>
<td>L , A</td>
<td>MOV H , A</td>
<td>MOV A , L</td>
</tr>
<tr>
<td>SHLD</td>
<td>DIVS</td>
<td>SHLD DIVS</td>
<td>RAL</td>
</tr>
<tr>
<td>LXI</td>
<td>H , O</td>
<td>LXI H , O</td>
<td>MOV L , A</td>
</tr>
<tr>
<td>MVI</td>
<td>A , 33D</td>
<td>MVI A , 33D</td>
<td>MOV A , H</td>
</tr>
<tr>
<td>DVO:</td>
<td>PUSH H</td>
<td>PUSH H</td>
<td>RAL</td>
</tr>
<tr>
<td>Push</td>
<td>D</td>
<td>PUSH H</td>
<td>MOV H , A</td>
</tr>
<tr>
<td>Push</td>
<td>H</td>
<td>DVO: PUSH H</td>
<td>POP PSW ; restore loop counter (A)</td>
</tr>
<tr>
<td>LHL D DIVS</td>
<td>XCHG</td>
<td>LHL D DIVS</td>
<td>RAL</td>
</tr>
<tr>
<td>POP</td>
<td>H</td>
<td>POP H</td>
<td>DCR A ; decrement it</td>
</tr>
<tr>
<td>POP</td>
<td>D</td>
<td>POP D</td>
<td>JNZ DVO ; shift remainder right and return in HL</td>
</tr>
<tr>
<td>JNC DVI</td>
<td>; underflow, restore (HL)</td>
<td>JNC DVI</td>
<td>ORA A</td>
</tr>
<tr>
<td>XTHL</td>
<td></td>
<td></td>
<td>MOV A , H</td>
</tr>
<tr>
<td>DVI:</td>
<td>POP H</td>
<td>POP H</td>
<td>RAR</td>
</tr>
<tr>
<td>Push</td>
<td>PSW</td>
<td>Push PSW</td>
<td>MOV H , A</td>
</tr>
<tr>
<td>MOV</td>
<td>A , E</td>
<td>MOV A , E</td>
<td>MOV A , L</td>
</tr>
<tr>
<td>MOV</td>
<td>A , D</td>
<td>MOV A , D</td>
<td>MOV L , A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RET</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>END</td>
</tr>
</tbody>
</table>
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NEW PRODUCTS
INTEGRATED CIRCUITS

CMOS DTMF CHIPS
• Detect either 12 or 16 standard digit tones
• Operate from a standard 5V supply

CD2202E, 2203E, and 2204E dual-tone multifrequency (DTMF) receivers are fabricated with low-power CMOS technology on EPI substrates, which greatly reduces the possibility of their experiencing latch-up problems under normal operating conditions. Each of the three devices runs off a standard 5V supply and requires only an external crystal for operation. Suitable for telephone-company central-office use, the 2202E and 2203E detect either 12 or 16 standard tones and produce either hexadecimal or binary-coded 2-of-8 4-digit output code. The 2204E—intended for use with workstations, remote telemetry, and voice-response systems—detects 16 DTMF tones and produces only 4-digit hexadecimal output code. All three devices employ switched-capacitor filter technology, and thus each have approximately 40 filter poles for the input analog signal. A 3.58-MHz TV colorburst crystal serves as a frequency reference. The 2202E and 2203E come in 18-pin DIPs; the 2204E comes in a 14-pin DIP. 2202E, $4.13; 2203E, $4.29; and 2204E, $3.71 (100).

GE/RCA Solid State, Box 2900, Somerville, NJ 08876. Phone (201) 685-7106.

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SEMICUSTOM ICs
• Are bipolar tile arrays
• Include Schottky diodes

QuickChip 2K Series semicustom ICs expand the circuit design possibilities of systems requiring Schottky TTL buffers, sample-and-hold circuits, high-speed comparators, fast-recovery amplifiers, and active mixers. The new series comprises two arrays: the 2K-30, for small, high-performance circuits, and the 2K-130, for larger, more complex circuits. The addition of Schottky diodes to analog bipolar arrays enables designers to more easily implement functions that were previously very difficult to achieve, such as switching or clamping circuits. The QuickChip arrays feature two types of Schottky diodes: unguarded diodes, for applications requiring minimum capacitance, and guarded diodes, for circuits requiring low leakage current and high breakdown voltage. The 2K-30 chip contains two full tiles and two half tiles, surrounded by diodes and transistors. The 2K-130 chip contains ten full tiles and six half tiles, which make it suitable for larger, high performance circuits. 2K-30, $2.75 to $3.50; 2K-130, $7.50 to $9.50.

Tektronix Inc, Box 500, Beaverton, OR 97077. Phone (800) 835-9433.

Circle No 352

COMPARATOR
• For high-speed successive-approximation ADCs
• 32-nsec propagation delay

The NE/SE5105 is a precision high-speed comparator incorporating an output latch. It is pin and function compatible with PMI's (Santa Clara, CA) CMP-05 and Raytheon's (Mountain View, CA) RM4805 comparators. For a 5-mV input overdrive, the comparator has a propagation delay of 32 nsec. The input-offset voltage specification is 100 µV, and the input-offset current equals 3 nA. The NE5105 has a large-signal input resistance of 1 GΩ, allowing you to realize a constant input-offset current over the device's full differential input voltage range. The comparator has a voltage gain of 26,000. Its power
dissipation is 100 mW. The NE/SE5105’s output and its latch-enable input are both TTL compatible. Versions in commercial and automotive temperature ranges are available. $2.50 (1000)

Philips, Components Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 353

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 354

LASER DRIVER

- Suitable for systems that require modulation to 600M bps
- Replaces custom high-frequency designs in fiber-optic systems

Applications for the LDC-600 laser driver and controller include digital fiber-optic communications, digital video, local-area networks (LANs), and optical-signal generation. You can also use the device as a stable dc constant-light controller. When used in a subsystem and coupled to a compatible laser diode, such as the Tektronix LDM-1301, the unit controls and maintains preset optical power while providing a current source for regulating a thermoelectric heater/cooler. You can mount the 1.5×2-in. laser driver on a standard circuit board. The unit features band-gap-referenced current sources that enable it to maintain all operating parameters over its rated temperature range. A slow start/stop function guards laser systems from possible damage when the power is suddenly turned on or off. $349.

Tektronix Inc, Electro-Optic Components Group, MS 13-810, Box 500, Beaverton, OR 97077. Phone (503) 627-4220.

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Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 310-371-9541.

Circle No 357

12-BIT SEQUENCER

- Features 33-word stack
- Provides 50-nsec operating speed

The CMOS ISP9110 12-bit µP sequencer features a 33-word stack that increases the onboard programming capability of a digital signal-processing system. The unit is compatible with the industry standard 2910. The chip provides 16 microinstructions, a 12-bit address width, and a 50-nsec speed. You can obtain the unit in a 40-pin plastic DIP, 44-pin PLCC, 40-pin ceramic DIP, or 40-pin side-brazed DIP. From $5 (100).

GE/Solid State, 10600 Ridgeview Ct, Cupertino, CA 95014. Phone (408) 996-5703.

INQUIRE DIRECT

QUAD 12-BIT DAC

- Features maximum gain error of ±5 LSB
- Provides maximum nonlinearity of ±0.5 LSB

The AD644 quad 12-bit DAC, which provides system-level integration in a single monolithic chip, can replace as many as 15 discrete ICs. Each DAC in the device has ±0.5-LSB clock. An external 550-kHz clock provides a 15-µsec conversion time. You can order the converter in an 18-pin plastic or ceramic DIP. Commercial grade, $6 (100).

Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 310-371-9541.

Circle No 357

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California
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Telex: 9102400972

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IE 1021 1121 42
NL 1021 1121 42
FR 1021 1121 42
DE 1021 1121 42
IT 1021 1121 42
ES 1021 1121 42
SE 1021 1121 42
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Elan Digital Systems
California
Tel: 800-541-ELAN
Telex: 9102400972

CIRCLE NO 17

EDN March 3, 1988
four DACs are functional, an ATE application can, during calibration, read data stored in the DAC latches. A reset command returns the DAC outputs to zero. The IC operates from ±12V and 5V supplies and features 400-mW power dissipation typ. Industrial grade, in a 28-pin DIP, $60.80; in a 44-pin LCC, $70.18 (100). Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TLX 174059.

Circle No 358

DUAL DRIVERS
- Each feature 2A output-current capability
- Provide 5 to 46V output supply voltage range

The industry standard L298 and the TLP298, an improved functional replacement, are high-current drivers for either full or half H-bridge applications. The units are suitable for use with inductive loads such as relays, solenoids, and dc motors in positive-supply applications. Both the L298 and the TLP298 have TTL-compatible inputs and 3-state outputs. The totem-pole outputs provide bidirectional drive currents to 2A at 5V to 46V. You can configure each unit as two, independent, full-H reversible drive channels or as four half-H channels. The drivers have input-protection diodes to guard against damage from ESD. The TLP298 consumes as little as one-half the output supply current of the L298 and switches nearly three times more quickly. The drivers come in 15-lead plastic power-tab packages. $5.70 (100).

Texas Instruments Inc, Semiconductor Group (SC-782), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 359

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CIRCLE NO 19

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8-CHANNEL DRIVER

- 35V/350 mA per channel
- Fully protected against output faults

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Sprague Electric Co, Box 9102, Mansfield, MA 02048. Phone (617) 853-5000.

Circle No 360

AUDIO AMP

- Suitable for use in car radios
- Features two complementary-output audio amplifiers

You can operate the TDA7350 audio power amplifier as a 12W/12W stereo amplifier or as a 24W bridge amplifier. The unit has fully complementary output stages that require no bootstrap capacitors; you need only add five external components to configure a stereo amplifier. The bridge amplifier, which does not demand external components for oper-
tion, runs from 8 to 18V supplies. When the unit is operating at 1 kHz on a 14.4V supply, either of its amplifiers typically delivers output power of 11W into a 2Ω load, 8.5W into a 3.2Ω load, or 6.75W into a 4Ω load; in each instance, the maximum distortion equals 10%. When operating at the same supply voltage, the unit features 0.04% typ distortion at 1 kHz for a power level of 0.1 to 4W into a 4Ω load, and 0.05% typ distortion for a power level of 0.1 to 6W into a 2Ω load. A muting circuit eliminates turn-on and turn-off noise, and a standby function lets you disable the unit. The unit features protection against thermal overloads, load-dump transients, and open-circuit ground connections, and its outputs feature protection against ac and dc short-circuits to either the ground or positive-supply rail. $2 (1000).

SGS-Thomson Microsystems, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131. Circle No 361

SGS-Thomson Microsystems, 1000 E Bell Ave, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976. Circle No 362

TELEPHONE IC

- Provides SLIC functions for telephone exchanges or PABXs
- Cancels longitudinal signals on the line to provide 60-dB balance

When combined with the vendor's MV3000 subscriber-line audio circuit (SLAC), the SL373 subscriber-line interface circuit (SLIC) provides a complete interface between a telephone line and a telephone exchange or PABX. The unit feeds power to the line, performs 2- to 4-wire conversion, performs 2- to 4-wire conversion, detects ring-trip and loop conditions, and operation of a ground key. You can program these functions to accommodate different telephone networks. The unit provides 60-dB typ balance by canceling telephone-line longitudinal signals. It feeds power to the line via an on-chip switch-mode regulator. In the constant-current feed mode, this regulator limits the IC's power dissipation to 1W; as a result, you do not have to provide heat sinks for the unit. £10.93 (1000).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 36251. TLX 449637. Circle No 363

Plessey Semiconductors, 9 Parker, Irvine, CA 92718. Phone (714) 472-0303. Circle No 364
NEW PRODUCTS

COMPUTERS & PERIPHERALS

MINISTREAMER

- Can store 250M bytes on a single reel
- Supports the 6250-bpi GCR recording format

The Ministreamer Model 1260 GCR streamer is a desktop 9-track streaming tape drive that can store as much as 250M bytes on a single tape reel. It supports the high-density, 6250-bpi GCR recording format. It also incorporates multiple operating speeds to maintain a constant data-transfer rate of 80k bytes/sec—the maximum speed supported by an IBM PC’s DMA channel. A µP controls all tape motion, and the self-calibrating reel servo system requires no field adjustments. A quartz crystal provides the master speed reference for performance at 12.5, 25, or 50 ips.

I/O CONTROLLER

- 4-channel serial I/O controller
- Handles async, bisync, or bitsync protocols

The ATcomm4 is a 4-channel serial I/O controller for the IBM PC, PC/AT, and compatibles. A Z8530 SIO device handles async, bisync, and bitsync protocols. Full-duplex DMA circuitry for each channel can transfer serial data at 1.5M bps. A 10-MHz iAPX-186 µP provides programmable intelligence for a variety of serial I/O protocol applications including SNA, X.25, SDLC, and HDLC. A 512k-byte onboard dynamic RAM is accessible from the onboard µP, the serial I/O DMA channels, and the IBM PC bus or the PC/AT bus. The PC host can access the board, using either extended or expanded addressing modes. Bidirectional FIFO registers provide a cross-port interrupt mechanism informing the host or the board that data is present in the shared RAM. $1395.


Circle No 367

DATA ACQUISITION

- Board for the IBM PS/2 Models 50, 60, and 80 has 12-bit ADC
- 64-sample FIFO and DMA transfers data to the host

The MC-DAS 1612 is a data-acquisition board for the IBM PS/2 Models 50, 60, and 80. It contains a 12-bit successive-approximation A/D converter whose conversion time is 8.5 µsec. Onboard autocalibration and an automatic zeroing process achieve 98 dB of common-mode noise rejection. The board has a 64-sample FIFO and performs burst-mode DMA transfers as an I/O slave. All connections to the board are brought out through a 37-pin D shell connector that’s accessible at the rear of the computer. The throughput in single-channel and autoscan modes is 80,000 samples/sec. In the normal mode where the board converts noncontiguous channels, the throughput is 50,000 samples/sec. It has two TTL digital-
input and two TTL digital-output lines along with one analog-output channel. Four independent 16-bit timer/counters let you program in either binary or BCD code to count up or down. $995.

Scientific Solutions, 6225 Cochran Rd, Solon, OH 44139. Phone (216) 349-4030. TLX 466692.

Circle No 368

COMPUTERS

- Support four to 10 users
- Use a custom VLSI 32-bit CPU

Suited to small offices, 210 Series 32-bit computers run the vendor's Office Network Exchange Plus, a departmental software system. Each of the computers contains three custom VLSI chips: a 32-bit CPU, a custom-integrated memory controller (CIM), and a virtual-memory-management unit (VMMU). The CIM provides data and address management for the CPU; the VMMU organizes the data space into segments, which facilitates shared access of data. Each program can use as much as 2G bytes of virtual memory space. The Model 211 executes approximately 0.7 MIPS; you can configure it with an optional 8k bytes of cache memory to achieve execution of 1 MIPS. You can select a 37M-, 68M-, or 142M-byte fixed-disk storage unit for integration into the system. $17,130 for Model 211 with 32-bit CPU, 2M bytes of memory, six asynchronous communications ports, a peripheral controller, a 37M-byte hard disk, an integrated streaming tape drive, and an HVS 6 Plus operating system.

Honeywell Bull Inc, 300 Concord Rd, Billerica, MA 01821. Phone (617) 671-2517.

Circle No 369

PC COPROCESSOR

- Provides 50 MIPS of parallel processing power
- Runs standard compilers and raster-imaging software

The Leonardo add-in coprocessor board for the IBM PC/AT or compatibles provides you with five IMS-
T414 or -T800 Transputers. The Transputers are linked in a pipe topology; each Transputer is linked to its immediate neighbor by two Transputer links. This topology leaves the Transputers at either end of the pipe with two Transputer links unconnected to the pipe. The master Transputer, at the head of the pipe, uses one of these links to communicate with the AT Bus via an Inmos link adapter and 2k bytes of dual-port RAM. This interface can transfer data between the co-processor board and the AT Bus at 800k bytes/sec and can generate host interrupts. You can connect the remaining Transputer links at either end of the pipe to other Leonardo boards or to external systems. The master Transputer comes with as much as 4M bytes of RAM, and each of the four slaves features 256k bytes of local RAM. The board runs Inmos Transputer development software; C, Pasc, Fortran, and Occam compilers; and the vendor's Pablo raster-to-vector encoding and decoding language for scanned graphics. A version with five T414 Transputers, 1M byte of master RAM, and 256k bytes of RAM for each slave, $6500.

Simulation Technology AS, Sandakerveien 35B, Torshov, 0401 Oslo 4, Norway. Phone (2) 156710. Circle No 370

DISPLAY TERMINAL

- Features a 15-in. flat screen with 75-Hz refresh rate
- Paper-white display produces letter-quality characters

The HCT is an alphanumeric display terminal that produces letter-quality characters on a paper-white background. It emulates HP's 2392/A and 2394/A terminals and is compatible with HP's 700/9x series of computers. Its 15-in. flat screen provides approximately 90 in. of viewable area and has a 75-Hz refresh rate to reduce flicker. The detachable keyboard has single-stroke keys that can activate a displayable calculator, calendar, file system, or notepad. A help key retrieves instructions for using the desktop accessories. The device also includes a battery-operated clock, 16k bytes of nonvolatile memory and 16k bytes of display memory, which can store 10 to 12 forms in a form-cache application. It can dis-
play either 80 or 132 columns. Communications take place through RS-232C and RS-422 ports at rates as high as 38.4k baud. $795.

Cumulus Technology Corp, 2650 E Bayshore Rd, Palo Alto, CA 94303. Phone (415) 856-8800. Circle No 371

SWITCH/CONCENTRATOR

- Interconnects as many as eight X.25 lines
- Concentrator gives six X.25 lines access to X.25 trunk line

The ACS 8250 is a packet switch and line concentrator for X.25 network communications. When used as a switch, the unit interconnects as many as eight X.25 lines. When used as a concentrator, it permits six interconnected X.25 lines to access a high-speed X.25 trunk line. It concentrates outward-bound packets and sends them to the packet network at 64k bps, and it directs incoming network packets to the correct local destination. A 68000 µP handles protocol processing. It features a 512k-byte dynamic RAM for buffering and routing. The unit supports LAPB (link access protocol B); a password-protected network-management facility provides on-line status and statistics. You can link multiple units together via Ethernet segments to create a customer-premises network. $6500.

Advanced Computer Communications, 720 Santa Barbara St, Santa Barbara, CA 93101. Phone (805) 963-9431. TWX 910-334-4907. Circle No 372

8-IN. WINCHESTER

- 2.8G-byte model fits in same space as 10½-in. disk drive
- Drive has an average access time of 18 msec

The MK-388FA is an 8-in. Winchester disk drive. The basic model provides 720M bytes of storage. It employs a head-disk-assembly design and a dedicated servo surface. The device features an average access time of 18 msec and can transfer data at 2.4M byte/sec. Extensive VLSI chips, a landing zone, and a fail-safe autoretract feature help the
drive achieve an MTBF of 35,000 hours. It has a standard SMD interface with built-in diagnostics. The unit is available in a 5¼-in. high, 19-in. wide, 2-drive rack subsystem with a built-in power supply. This subsystem provides 1.4G bytes of storage. Two rack subsystems occupy the same space as a single 14- or 10¼-in. disk drive and supply 2.8G bytes of storage. Basic unit, $3995; rack subsystem, $8335 (OEM qty).

Toshiba America, Disk Products Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (714) 583-3108. Circle No 373

RS-232C INTERFACE
- Provides optical isolation for RS-232C lines
- Retransmits data bidirectionally at 19.6k baud

The IM-232-8 is an 8-line isolating interface for computer systems using EIA RS-232C and CCITT V.24 communications protocols. The model provides 1500V optical isolation between input and output ports that eliminates common-mode voltages and ground loops. The unit also functions as an RS-232C repeater, which doubles the length of the communication line. As a repeater it can retransmit data bidirectionally at rates to 19.6k baud. The unit has LEDs that monitor the status of the data lines without loading them. It’s powered from a standard 120V ac line and consumes 4W. Packaged in an impact-resistant ABS plastic package measuring 5¾×6¾×2¼ in., it weighs 3.5 lbs. A surge-protection option, which absorbs transient overvoltages, is also available. $148.

Peradata Technology Corp, 17 Birch St, Lake Grove, NY 11755. Phone (516) 588-2216. Circle No 374

IMAGE SCANNER
- Performs overhead scanning
- Adapts to ambient light

The N-205 image scanner provides user-selectable resolution to 200 dots/in. and employs an image sensor that performs overhead scanning of documents. The unit adapts to ambient-light conditions. You
COMPUTERS & PERIPHERALS

don't have to obtain additional hardware in order to use it with Macintosh computers or with an IBM PC or compatible. It interfaces with your computer via an RS-232C port that has a switch-selectable 19,200-baud max data-transfer rate. You can also use its Centronics-compatible bidirectional parallel port to transfer data. The scanner's desktop-publishing software lets you input a scanned image, call it up on your terminal, edit it, and print it. You can purchase the unit with Front Page Personal Publisher, PC Paintbrush Plus, or optical-recognition software for use with the IBM

PC or compatibles, or you can obtain it with Haba Personal Publisher software for use with the Macintosh. Scanner without software, $695.

Chinon America Inc, 6374 Arizona Circle, Los Angeles, CA 90045. Phone (213) 216-7611.

Circle No 375

EVALUATION BOARD

- Stand-alone board executes ADSP-2100 DSP algorithms
- Board has 2k×16 bits of data memory

The ADDS-2160 is a stand-alone evaluation board that executes DSP (digital-signal-processing) algorithms for the ADSP-2100 DSP chip. The board consists of an ADDS-2100, 4k×24 bits of program memory, and 2k×16 bits of data memory. An 8088 µP that runs the board provides system debugging.

The board has both digital and analog interfaces. Two RS-232C ports connect the board to a terminal and host computer for program development. You can use an onboard codec, microphone port, speaker jack and amplifier, and a 12-bit D/A converter for linear predictive coding and echo cancellation. You can also add an A/D converter through an expansion port. $1950.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577. TLX 174059.

Circle No 376

Design Engineers; you've never seen this before!

BEI Motion Systems Company introduces their brand new modular optical encoder with an installation time so impressive that no shims, set screws, epoxies, alignment or oscilloscopes are required!

That's right. A new economical optical encoder that never needs alignment. Not a kit, these fully self-contained, modular encoders feature quick, effortless installation in less than 60 seconds by "untrained" hands!

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To learn more about optical encoders, send for your copy of their new data sheet. You've never seen anything like it before either!

CIRCLE NO 27

BEI Motion Systems Company introduces an economical optical encoder that never needs alignment. Installation is quick and effortless.

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CIRCLE NO 28

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

DC/DC CONVERTERS
• Feature 6.6 W/in.² power density
• Spec 500V dc I/O isolation

DPS/DPD Series single- and dual-output dc/dc converters comprise 14
models that deliver 5, 9, 12, ±12, and ±15V outputs from 5 and 12V
inputs. Each of the converters employs MOSFET technology and fea-
tures input filtering, short-circuit protection, 500V dc input/output
isolation, and a -25 to +71°C nonderated operating range. The
devices’ 10⁶-hour MTBF and 80% efficiency rating makes them suit-
able for µC, process-control, tele-
communication, and ATE applications. $24 (OEM qty).

Semiconductor Circuits Inc, 49
Range Rd, Windham, NH 03087.
Phone (603) 893-2330.
Circle No 380

PHOTOSENSOR
• Contains a phototransistor and
a current amplifier
• Features 850-nm peak optical
sensitivity

The P-1-Darlington miniature
photosensor assembly measures
only 1×0.25 in. It combines a high-
sensitivity phototransistor with a
1-stage optical current amplifier to
provide an optical sensor that can
directly drive programmable con-
trollers, industrial computers, or
most logic families. The photosensor
has a peak optical sensitivity of 850
nm, so it is compatible with both
incandescent and infrared sources.
It features a 12-ft scanning range, a
200-µsec response time, an 8° field
of view, 100-mW max power dissipa-
tion, and a -30 to +100°C operating
range. The sensor has a threaded
steel body for easy mounting, and
comes with 6 ft of waterproof, flex-
ible shielded cable. From $40.

Scanning Devices Inc, 108 Elm
St, Waltham, MA 02154. Phone
(617) 891-8991.
Circle No 381

SUPPRESSORS
• Provide transient protection for
power and data lines
• Meet all applicable FCC regula-
tions

Meeting all FCC regulations, the
Model 120KMP1 and 120KMP2 suppressors provide transient protec-
tion for both ac power lines and data
lines using telephone-style modular
plugs. They are housed in an EMI/RFI-shielded metal case and operate
to 50k baud. The signal-line portion
of the 120KMP1 can accommoda-
te two RJ 11 (6-position) modu-
lar plugs, and the 120KMP2 can
accept two RJ 45 (8-position) plugs.
The maximum clamping voltage is
340V peak. This section can also
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TURN TO PAGE 223
Precision performance even in limited space. Designed with a right angle lead exit, this ultra compact gage head is ideal for measurement in miniature fixturings and of small inside diameters. AC-powered, it features excellent linearity and a gaging range of ±0.010”.

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Grid Scale: 3/8" x 3/8"

COMPONENTS & POWER SUPPLIES

shunt 400A to ground and can handle 1500V transients. Operating line requirements are ±185V at 200 mA. In the ac line section, both units provide two standard 3-prong female sockets. The maximum line-to-neutral clamping voltage is 335V at 500A and 375V at 3000A. This section exceeds the line-surge standards of IEEE-587, Category B. 120KMP1, $80; 120KMP2, $87 (100).


Circle No 382

DC/DC CONVERTER

- Six-sided shielded case eliminates RFI problems
- Features wide-range input operation

The Model 28D5.1000 pc-board-mountable dc/dc converter accepts 18 to 54V dc inputs and provides isolated ±5V outputs. The output currents are 1.1 and 0.9A. The converter features a shielded transformer and a 6-sided shielded case. The output stage has protection against load feedback-spike damage. Its key specs include a line and load regulation of 0.05%, 20 mV p-p output noise, 500V dc isolation, and 8-hour min short-circuit protection. The minimum efficiency specs at 60% and the operating range spans -25 to +80°C. The converter carries a 5-year warranty. $126. Delivery, stock to six weeks ARO.

Calex Mfg Co Inc, 3555 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911.

Circle No 383

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The device, which is housed in a 6-pin package, can scan tiny magnetic fields to determine the position of a metal object. Operating with a constant control current, the device emits a voltage in direct proportion to the prevailing magnetic field. The sensors register movement to a fraction of a millimeter within the scanned magnetic field.

The device’s package has a 0.8-mm mounted height. Its operating range spans -40 to +150°C. $15.60 (100). Delivery, eight to 10 weeks ARO.

Siemens Components Inc, Special Products Div, 186 Wood Ave South, Iselin, NJ 08830. Phone (201) 321-3400.

Circle No 385

GLOBE MOTORS

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For over 40 years, first as Globe Industries, then as TRW Motor Division, we’ve maintained a reputation for high quality products and responsive customer service. Now, as Globe Motors, we’re stronger than ever, and ready to help you find a solution for any motion application. Whether it involves precision movement of a mechanical component, instrument, air or fluid, Globe Motors has the right device, including a wide selection of AC and DC motors/gearmotors, fans and blowers, pumps, limited rotation torquers, and linear and rotary actuators.

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TLX: 228224

CIRCLE NO 31
COMPONENTS & POWER SUPPLIES

LINE FILTERS

• Contain an active filter to suppress line interference
• Available in single- and 3-phase versions

Trakorb line filters contain an active filter that detects and suppresses line interference. A 4-kV spike with a rise time of 5 nsec on a 240V line supply is typically suppressed to 50V. Apart from suppressing line interference, the filter also protects lines from indirect lightning strikes. Single-phase and 3-phase devices are available for 110, 240, and 440V line supplies. The single-phase versions have current ratings between 1.5 and 30A; the 3-phase delta versions have current ratings between 3 and 30A. The filters are available in packages for pc boards or chassis-mounting. Single-phase versions, £10.50 to £23.25; 3-phase versions, £23 to £45.60 (100).

Power Conversion Ltd, Fir Tree Lane, Groby, Leicester LE6 0FH, UK. Phone (0533) 878881. TLX 341401.

Circle No 386

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Behlman does, all day long. Our STD and KB Series AC Power Sources are designed to deliver up to 150% of rated power. This means you never have to derate a Behlman, or worry about power factors or overloads. And with 50% more power being available to the load, these models are more cost effective, versatile and reliable.

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POWER SUPPLY

• Can drive A/D converters, op amps, and other analog devices
• Available with a companion mounting kit

You can order the Model 22-40 dual power supply with a compatible mounting kit (MK22/08B). The encapsulated supply, which is suitable for powering analog circuits, has a dual tracking output of ±15V at ±50 mA. It has line and load regulation of ±0.1%, and a noise and ripple spec of <2 mV rms. It features short-circuit-protected output voltage that is factory set to within 0.5% accuracy. You can obtain the supply with 100, 115, 220, 230, or 240V ac inputs. With 50-Hz lines, you must derate the outputs by 50%. The supply's case measures 1.75×2.25×1 in. and includes a molded-in, threaded insert that facilitates pc-board mounting. Model 22-40, $58; Model MK22/08B, $23.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 269888.

Circle No 387
The Ultimate Complement

EDN magazine for technology in depth.
EDN News for news of products, technology, and careers.
Together, they provide complete coverage of electronics for engineers and engineering managers worldwide.
μP PROGRAMMER

- Programs 8748, 8741, 8742, 8748H, 8749, and 8749H
- Plugs into PC bus

The 8748 MPU programmer fits in any I/O slot in an IBM PC or other PC bus-based computer. It programs the following μPs in addition to the 8748: 8741, 8742, 8748H, 8749, and 8749H. It can program and verify locations beginning at specific addresses in the μP's ROM space. Using the menu-driven software supplied with the unit, you can determine whether a chip has been programmed, load data to a buffer in host memory from a binary file on disk, modify the buffer, and save the buffer contents to disk. Also accompanying the unit is software which converts data in the following formats to binary: Intel and Tektronix Hex, and Motorola S record.

$295.
Avocet Systems Inc, Box 490, Rockport, ME 04856. Phone (800) 448-8500; in ME, (207) 236-9055.
Circle No 390

OSCILLOSCOPE

- Works as 50-MHz analog scope or 20M-sample/sec DSO
- DSO stores 4k samples/channel

You can use the 2210 either as a conventional dual-trace analog scope with 5-mV/div sensitivity and bandwidth of 50 MHz or as a digital storage oscilloscope (DSO) with 8-bit vertical resolution, a 20-MHz sampling rate, and 4k-point horizontal resolution. In the DSO mode, the unit can display low frequency waveforms in the roll or triggered-roll modes, or it can freeze them on the screen. An external clock input, which accepts frequencies as high as 10 MHz, allows you to control data sampling and to synchronize sampling with occurrences in the equipment under test. You can collect 1k or 3k samples prior to triggering a sweep; in the pretrigger mode, a bright dot on the display denotes...
the trigger point. $2195.

Tektronix Inc, Box 1700, Beaverton, OR 97077. Phone (800) 835-9433 ext 170.

Circle No 391

SWEEP GENERATOR

- Covers 10 MHz to 20 GHz
- Holds harmonics to $-60 \text{ dBc}$ from 2 to 20 GHz

The Model 6311 programmable sweep generator works with the vendor's automatic amplitude analyzer and autotester to form a scalar network-analysis system. The generator covers a frequency range of 10 MHz to 20 GHz and, in the fast-sweep mode, performs a sweep in 15 msec. When the instrument is producing a constant-frequency output, its frequency accuracy is typically $\pm 3 \text{ MHz}$; during sweeps, its accuracy is $\pm 20 \text{ MHz}$ typ. Its power levels are accurate to $\pm 0.5 \text{ dB}$ from 0.01 to 2 GHz. From 2 to 20 GHz, the unit holds harmonics and subharmonics to $-40$ and $-60 \text{ dBc}$ min, respectively. The vendor claims that you can calibrate the instrument in 15 minutes by using a counter interfaced to the sweep generator via the IEEE-488 bus, and a power meter. $21,950. Delivery, 60 days ARO.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401. Phone (201) 934-9050.

Circle No 392

DEVICE PROGRAMMERS

- Feature support programs that reside in socketed EPROMs
- Edit fuse maps in RAM via RS-232C port

The Palpro 2X family of dedicated PLD programmers supports 20- and 24-pin PLDs, EPLDs (erasable PLDs), PLAs, and IFL (integrated fuse logic) and PAL devices. The Palpro 2X Model A supports 20-pin devices from Monolithic Memories Inc, National Semiconductor Corp, and Texas Instruments. The Palpro 2X Model B supports 20- and 24-pin...
devices from these vendors. The Palpro 2X Model C supports 20- and 24-pin devices from Advanced Micro Devices, Lattice, Cypress, and Signetics. The device-support programs that run on a programmer’s internal µP reside in a socketed EPROM. To add support for a new device, you replace the EPROM with a new one supplied by the vendor. A RAM buffer stores fuse maps; you can edit these maps by using an ASCII terminal connected to the programmer’s RS-232C port. The units accept JEDEC files and are compatible with files produced by the following compilers: Palasm, Amaze, Help, Plan, Abel, Cast, and Cupl. $595 to $995.

Logical Devices Inc, 1321 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (800) 331-7766; in FL, (305) 974-0975. TLX 383142.

Circle No 393

**FUNCTION GENERATOR**

- Has two waveform memories that contain 8k×12-bit words
- Outputs arbitrary functions at 100 nsec/point

The AFG 5101 modular arbitrary-function generator contains two waveform memories, each of which has 8k×12-bit words. Via its D/A converters, it can generate a new value as often as every 100 nsec or as seldom as every 999.9 sec. The unit can also produce sine, square, and triangular waves to 12 MHz. To simplify definition of arbitrary waveforms, the generator’s permanent memory contains 1000-point sine, square, triangular, and ramp waveform segments. You can edit these segments and position them at points of your choosing within the waveform memories. If you define the end points of waveform segments, the generator can draw straight lines and interconnect them. The instrument can also generate logarithmic, linear, and arbitrarily shaped sweeps; you can select these sweeps and program their starting and stopping points and rates from the panel or via the IEEE-488 interface. $3395. Delivery, 14 weeks ARO.

Tektronix Inc, Box 1700, Beaverton, OR 97077. Phone (800) 835-9433, ext 170.

Circle No 394
100-MHz SCOPES

- Provide cursor-controlled time and voltage readout
- Allow storage and recall of 20 setups

The 2245A and 2246A oscilloscopes incorporate four 100-MHz-bandwidth channels, two of which provide 2-mV/div sensitivity and 2% max amplitude-display error. By positioning the cursors, you can obtain on-screen numeric readouts of voltage and time. On the 2246A, the cursor settings follow changes in sensitivity, vertical position, and trigger point. Both units offer an automatic-setup feature, which puts a trace on the screen with a minimum of control manipulation. The 2246A also provides on-screen menus from its internal firmware. Further, the 2246A allows you to store 20 control-panel setups and recall them at the touch of a button. 2245A, $1795; 2246A, $2395.

**Tektronix Inc, Portable Instruments Div, Box 1700, Beaverton, OR 97077. Phone (800) 835-9433, ext 170.**

**Circle No 395**

SCSI-BUS TESTER

- Emulates SCSI devices and performs synchronous tracing
- Handles synchronous transfers at 4.5M bytes/sec

You can control the DSC-202 SCSI-bus analyzer/emulator from an external ASCII terminal or computer. The tester can trace activity on the SCSI bus without affecting bus operation; it can record 32,000 56-bit-wide events and display them in several formats, including one which resembles Pascal source code. You can use combinations of strobe and control lines to qualify data for storage. For asynchronous mode, the maximum data rate is 1.5M bps; for synchronous mode, it's 4.5M bps. With optional firmware, you can program the unit to initiate transac-
tions on the bus or to receive data from it. You can fit several test routines into the tester's 1k-byte EEPROM and retain them after you remove power, or you can load test programs totaling 30k bytes into the unit's static RAM via either of the two RS-232C ports. $8950.

Ancot Corp, Box 1141, Palo Alto, CA 94301. Phone (415) 327-1525.

Circle No 396

**DISASSEMBLER**

- Supports DSP56000 family of signal processors
- Fits the vendor's 1240 and 1241 logic analyzers

The 12RM99 Option 15 DSP56000/1 Mnemonics ROM pack plugs into the vendor's 1240 and 1241 logic analyzers. It provides instrument setup and disassembly postprocessing for debugging and code optimization in systems that use the Motorola DSP56000/1 digital-signal processors running at speeds as high as 10.25 MIPS. You can use the logic analyzers' time-correlated display to freeze real-time interactions between independently clocked system modules on the logic-analyzer screen. $400.

Tektronix Inc, Box 12132, Portland, OR 97212. Phone (800) 245-2036.

Circle No 397

**TRANSIENT RECORDER**

- Incorporates MS-DOS computer that uses 10-MHz 80286
- Can include 40M-byte hard disk

The PSO 5070 is a 40-lb, 4-channel digital storage oscilloscope with differential inputs, 64k words of memory for acquired signals, a choice of three A/D converters, and an 80286-based personal computer with a 10-MHz clock rate and 640k bytes of RAM. The oscilloscope can acquire data at 20M samples/sec with 8-bit resolution and at 2M samples/sec with 10- or 12-bit resolution. The computer incorporates a 1.2M-byte floppy-disk drive and, optionally, a 20M- or 40M-byte hard-disk drive. Further, the scope can run data-analysis applications such as Asyst, Asystant, and ILS. $8000 to $11,000.


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RF SIMULATION

- Offers new sparse-admittance matrix-reduction feature
- Lets you perform VSWR measurements and analysis

You can use the enhanced simulation program Touchstone version 1.6 for the design, analysis, and optimization of microwave/RF circuits. A new sparse-admittance matrix-reduction feature permits this version of the simulation program to use computer memory more efficiently than did earlier versions and speeds up the analysis of large, complex circuits. You can include as many as 250 variables and equations in a circuit file; other new features and capabilities include a sweep progress indicator, print- and plot-interrupt facilities, and the ability to make VSWR measurements and to simulate stripline-cross and stripline-curve elements. The network-analyzer interface now works with the Wiltron 360 vector network analyzer, as well as with the HP network analyzers supported by earlier versions of the program. The program runs on IBM PCs and compatibles, VAX computers, HP 9000 Series 300 machines, and Apollo and Sun workstations. From $9900.

EEsof Inc, 5795 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 881-7530.
Circle No 400

EDIF INTERFACE

- Lets you convert any P-CAD schematic net list to EDIF
- Provides property-name and character mapping

NX-EDIF converts a schematic net list generated by the vendor's P-CAD IBM PC-based products into an EDIF file for transfer to ASIC vendors, to pc-board service bureaus, or to an HP PCDS (printed-circuit-board design system) workstation. The program allows you to translate P-CAD attributes (part-packaging information symbols) into symbols that the target system can use. You can also remove individual P-CAD characters from the output file or translate them into different characters in the output file. $500.

Personal CAD Systems Inc, 1290 Parkmoor Ave, San Jose, CA 95128. Phone (408) 971-1300. TLX 3717199.
Circle No 401

ANALYSIS OPTIONS

- For RS/1 package
- Let you read data directly from HP test equipment

QCA, RPL Toolkit, Graphic Writer, and CLI are four options for the vendor's RS/1 data-analysis package, which runs on HP 9000 Series 300 computers. The QCA option provides a wide range of quality-control and manufacturing functions, such as control charts, sam-
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portions of the files containing potential matches and can highlight the potential matches. When run on a 12-MHz PC/AT, the program searches through approximately 18,000 characters/sec. In order to use this program, you must have 128k bytes of memory available and your machine must run DOS version 2.0 or later. Golden Retriever, $99; Golden Retriever Pup, for use with floppy disks only, free ($5 shipping charge).

SK Data Inc, Box 413, Burlington, MA 01803. Phone (617) 229-8909.

Circle No 403

MACHINE MONITOR

- Monitors manufacturing equipment in real time
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The TEAM (Technical Equipment Analysis Manager) computerized maintenance-management system is written in C and can run on a variety of host computers, from IBM PC/ATs or compatibles to workstations and mainframes. The program monitors the operation of a plant's equipment and alerts operators or maintenance staff when a unit malfunctions. It also indicates the status of other equipment affected by the malfunctioning unit and generates a report that can help engineers to analyze and correct the problem. You can enter commands that will cause the program to call technicians or supervisors at home after hours. The program maintains a complete work history on each monitored unit of equipment and can generate a wide variety of reports to aid in planning maintenance schedules, job costing and accounting, and material management. You can purchase individual modules of the program or the complete maintenance-management system. Prices for the complete system start at $10,000 for PC licenses, $28,000

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for workstation licenses, and $38,000 for mainframe licenses.

Logic Sciences Inc, 11000 Wilcrest, Houston, TX 77099. Phone (713) 879-0536. Circle No 404

ADA SYSTEM

• Allows development of Ada software on Apollo workstations
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Domain/Ada is a set of high-performance tools for the development of programs written in Ada. It consists of an Ada compiler (derived from the Verdix Ada Development System), a source-level debugger, library-management tools, a runtime system, and a wide variety of program-development utilities. The package has been validated by the AJPO and fully complies with ANSI/MIL-STD-1815A. The package gives you access to Domain system facilities and to user-written routines in Pascal, Fortran-77, or Domain/C. Compiler error messages provide concise descriptions of errors and offer cross-references to the Ada reference manual. A library of utility packages includes complex arithmetic routines, mathematical functions, sorting routines, and string-handling routines. $6000.

Apollo Computer Inc, 330 BillERICA RD, Chelmsford, MA 01824. Phone (617) 256-6600. Circle No 405

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Silicon Compiler Systems Corp, 2045 Hamilton Ave, San Jose, CA 95125. Phone (408) 371-2900. Circle No 406
DRAFTING PROGRAM

- Dual modules create mechanical and schematic drawings
- Libraries include electrical and mechanical symbols

The MGI/CADD3 2-dimensional drafting program consists of two modules, one for schematic capture and one for architectural and mechanical drawings. The program's eight symbol libraries contain electrical, electronic, logic, place-planning, scheduling, hydraulic, and piping and instrumentation symbols. When combining symbols, you can preview the effect of variable radii before committing the results to the file. Both modules provide block functions, scrolling, and zoom-in and zoom-out features. The program runs on IBM PCs or compatible computers and on 80386-based machines. $1495.

Microcomputer Graphics Inc, 13468 Washington Blvd, Marina Del Rey, CA 90292. Phone (213) 822-5258.

Circle No 407

PC AUTOROUTER

- Rip-up and reroute algorithm achieves 100% routing
- Optimizing algorithm spreads traces evenly over area

PADS-SuperRouter is a 3-stage PCB board routing package that runs on 80286- or 80386-based computers. A math coprocessor is desirable but not essential. The initial routing phase uses a series of passes in attempting to find a route for all the connections on the board. When this phase has completed as many connections as it can, the rip-up and reroute phase completes the remaining connections, if necessary ripping out and rerouting connections completed by the initial phase. However, you can tag critical traces for no rip-up. The final phase reroutes all traces except tagged critical paths; it takes out many bends put in by the obstacle-hugging algorithm, spreads the traces evenly over the available area, and removes unnecessary vias. The package can route as many as 12 layers simultaneously, can route different traces of different widths simultaneously, and allows routing to pads with 1-mil resolution. The amount of memory required by the program varies with the complexity of the layout; typical requirements are 2M bytes for a 2-layer, 100-IC board, and 4M bytes for a 4-layer, 200-IC board. $5000.

CAD Software Inc, 119 Russell St, Littleton, MA 01460. Phone (800) 255-7814; in MA, (617) 486-9521.

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The role of histograms in A/D converter testing

The 4-pg application note AN/L-18, Histograms Simplify A/D Converter Testing, explains that testing a 12-bit A/D converter for missing output codes and differential linearity error requires examining codes from 4096 data points. After reviewing the old way of testing, the note describes how histograms make testing simpler and more accurate.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 410

STD µCs and IEEE-488 interfaces categorized

The 200-pg Technical Data Book details the vendor's complete line of STD-8088 industrial computer systems and IEEE-488 interfaces of microcomputers. The new products section focuses on industrial-networking products, IBM-compatible STD DOS systems, interfaces for the IBM PS/2, single-board computers, STD and IEEE-488 drive packages, and bubble-memory systems. The catalog provides application examples, a system designer's guide to 8088-based STD Bus systems, and the complete STD-8088 Bus specification. It also includes specifications, configuration guidelines, and ordering information.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401.

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Testability treated with a sense of humor

The 12-pg brochure Tales of Testability provides a light-hearted look at the trials and tribulations that occur when a manufacturer ignores testability features during the product-design cycle. The booklet deals with testability at three levels: device, pc board, and system. It defines the three primary testability techniques and sets forth the benefits, including shorter prototype debut time and shorter test-pattern-generation times, when testability features are part of the design cycle.

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Catalog of thermocouples and RTDs

The 28-pg *Thermocouples and RTDs* (resistance temperature detectors) describes two thermocouple classes: Super-Temp with hard-pack mineral insulation and glass-braid-insulation models. The selection of thermocouples includes 10-wire calibrations, 13 sheath materials, and 14 standard sheath diameters. The RTD selection lists five resistance values and three diameters. Also included are thermocouple and RTD assemblies, hardware, and accessories.

Software catalog available with videotape

The vendor’s SmartModel catalog lists the latest models for system simulation. A complete listing of distributors and representatives appears on the back cover. To help you evaluate the use of simulation for design verification, a videotape that provides a simulation of the design for an 80386 PC mother board is available.

*Logic Automation*, Box 310, Beaverton, OR 97075.

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CIRCLE NO 64
Engineering jobs in rehabilitation: Highly prized and hard to get

In 1965, Barry Romich was a junior engineering student at the Case Institute of Technology in Cleveland, OH. In need of a part-time job, he applied for a position in a medical-engineering research program. The program's director hired him, and Romich went to work designing instrumentation that would allow quadriplegics to turn on their lamps, radios, and televisions.

Romich's introduction to what's now called rehabilitation engineering occurred by chance, but his subsequent activities in the field have been anything but unintentional. While employed full time as a designer of machine-control systems and then research instrumentation, Romich devoted his evenings and weekends to refining the control systems he'd worked on in college. In 1975, he and his partner, Ed Prentke, developed a system that allowed a quadriplegic to answer or dial a telephone by blowing and sucking on a tube. After the Veterans Administration included the system in a demonstration of home equipment for the physically disabled, the two men put their new contacts to use by launching the Prentke Romich Co (Wooster, OH); the company specializes in communication devices for the disabled.

The appeal of solving difficult engineering problems together with the knowledge that he was helping people kept Romich focused on his goal. "It was an exciting thing to be doing," he remembers. "It was a technical challenge, and it was also satisfying to know that there was someone who needed what I was working on."

The growing number of engineers designing rehabilitative devices for...
the more than 35 million disabled Americans apparently agree with Romich's sentiments. Though the opportunities for engineers to work directly with patients in clinical settings are few—there are only 15 federally funded rehabilitation centers—the jobs are among the most sought after in the engineering profession.

Two important factors contributed to the development of rehabilitation engineering. In 1973, Congress approved legislation that established the Rehabilitation Services Administration and funneled federal money into handicapped services. Disability activists credit the 1973 act and its amendments with restoring civil rights to the handicapped. Equally important, the legislation forced rehabilitation technology out of the research and development laboratories and into clinical settings where it could be applied.

Materials development, for example, produced synthetics for lighter, more comfortable prosthetic devices and wheelchairs. But the most dramatic improvement resulted from the incorporation of electronics into aids for the handicapped.

Not only do electronics systems drive wheelchairs, they also free people from disabilities that hinder their speech and communication. By donning a headset and speaking into an attached microphone, a Massachusetts man, whose hands shake from Parkinson's disease, can dictate memos and other documents. The computer in front of him transforms his speech first into digitally encoded signals and then into text that appears on a screen in front of him.

People who have lost the use of their voices but can still turn or nod their heads can use special pointing devices to operate a computer. Others with limited head motion can control cursors by blowing into or sucking on tubes or mouthpieces. Romich's company produces control devices that operate when the user blinks an eye or raises an eyebrow.

Rehabilitation technology, which generally refers to the design of devices that work outside the body, has a sister science in the field of bioengineering. Specialists in bioengineering work not on rehabilitative devices, but on replacement limbs and functions. In carefully controlled experiments, researchers have successfully automated the movement of artificial arms and legs. Pushing that technology a step further, they've attached electrodes to the legs of paraplegics and through electronic signals have stimulated their limbs into motion.

A professional melting pot

Putting technology to work for the handicapped requires the pooling of experts from the scientific, engineering, and health-care sectors. A common denominator among some members of the richly diverse rehabilitation profession is an engineering background. Twenty percent of professionals in the field possess engineering degrees, estimates Patricia Horner, executive director of the Rehabilitation Engineering Society of North America (RESNA).

Successful rehabilitation of people with severe disabilities is by definition a team effort. Wheelchair clients who visit the Stanford Uni-

Designers in other sectors can help, too

Although expensive custom equipment is necessary to help profoundly disabled individuals, slight modifications in other electronic devices are all that's necessary to benefit many other people with disabilities of varying degrees.

"In many cases, high-tech solutions are not necessary for many people," says George Markowsky, chairman of the computer science department at the University of Maine. Markowsky points out that in the case of computers, small design adjustments would open use of the computer to people with a variety of disabilities. For example, volume control of the beeps that computer programs elicit when an error is made would allow use by the hard-of-hearing. Moreover, visual error signals such as an LED on the front panel of a computer monitor would allow deaf users to operate it.

Simple program commands also often block users of special adaptive devices from running a program. "Imagine a person who has a mouth-stick and wants to run Wordstar," says Markowsky, a 10-year veteran of IBM's Thomas Watson Research Center (Yorktown Heights, NY). "They only have one stick to use, so they can't utilize commands that call for using the control key in conjunction with another key." Yet writing a program that acts as if the control key is pressed would be an easy task, Markowsky says, adding that software makers should consider the inclusion of such programs in standard packages.

Markowsky and other disability activists hope that a new law scheduled to go into effect later this year will spawn improvements. That law requires all office products procured by government offices to be accessible to handicapped users.
versity Rehabilitation Engineering Center (Stanford, CA), for example, meet with a specialist in seating problems, an occupational therapist, and a communications engineer. Sometimes the client's own therapist attends the meeting also. The group assesses the individual's degree of disability and the level of assistance required.

This mandatory teamwork holds strong appeal for engineers, for whom more conventional work settings often lead to isolation and a sense of detachment. Engineers often complain that typical design positions don't tap the range of their skills and relegate them to doing piecework. They also say that they're often omitted from the decision-making process. "We have a lot of input in seeing projects through, and that's something not really found in industry," says Mike Burrow, a research engineer at the Georgia Institute of Technology's state-funded Center for Rehabilitation Technology.

A team effort

As technology becomes more complex, the need for rehabilitation specialists to work well together becomes more acute. "For a long time, technological issues were the primary issues in this field," says Ro­mich. "But more recently, the issues have become more applications- and linguistics-oriented." Designing a keyboard with a multimeaning icon system, he says, requires many months of work by a linguistic specialist as well as a design engineer.

RESNA attempts to provide a central hub for this assortment of specialists. Rehabilitation specialists formed RESNA in 1980, and it has grown quickly ever since. (RESNA has since changed its name to the Association for the Advance­ment of Rehabilitation Technology, but plans to retain its former acro­nym through a transition period.)

Last year was "a record year for RESNA in every sense," says Hor­ner. Membership now tops 1000. The organization's 1987 conference in San Jose, CA, ran for three days and attracted 950 attendees from 20 countries. RESNA's conventions have become the premier event in the field. Horner expects 2000 at­­tendees at this year's meeting in Montreal, Canada.

Engineers who have managed to get into this active field say their former jobs pale by comparison. Tony Bradshaw worked for three years as an industrial designer before he joined Georgia Tech's Center for Rehabilitation Technology in 1983. As an industrial designer, he designed "all sorts of gear" from coffeepots to vacuum cleaners. Last year, he directed the design and assembly of a prototype workstation that can act as a mechanical assistant to quadriplegics. The workstation incorporates a mechanical arm to retrieve files and notebooks, place them on a reading tray, turn pages, and replace the materials when the user is done.

His job as a product designer was to create something aesthetically pleasing. His work at the center requires him to take "whatever ca­pabilities the person has left and stretch them to the point where he or she can do something that's normal for an able-bodied person."

Interest in the field is greater than opportunities. After an article about the Stanford center appears in print, "we get more calls from engineers inquiring about jobs than from patients inquiring about services," says director of research Maurice LeBlanc. Finding engi­neers who already have the important clinical background is difficult, and LeBlanc adds, not always necessary. "A rehabilitation engineer should be first a good engineer, then follow with clinical experience."

Despite the profession's successes and the enthusiasm of its members, problems remain to be solved. Among the most critical issues is the question of who pays for the expensive custom equipment and training that the severely disabled need. For example, Bradshaw estimates that the manufacture of additional workstations will cost more than $20,000 each. Most clinical centers obtain the project money from a variety of third-party sources such as foundations, private insurance companies, and Medicare or Medi­caid.

"Reimbursement issues fuel and fund the technology," says Tom Rie­ger, director of the Stanford Rehabilitation Engineering Center. "Standard health care has standard reimbursement methods, and billing is easily reconciled. But recognition of the disabled is just starting to come to light, so the reimbursement issues aren't standardized. It's changing rapidly, but it's still a problem."

The high cost of custom devices and the complicated funding procedures limit the involvement of private-sector companies. But some businesses remain undaunted, de­vising new uses of technology for the handicapped. Prentke Romich Co, for example, continues to spe­cialize in keyboard and control de­­vices that help disabled people communicate. In Colorado, Johnson Engineering Co licensed the technology that NASA used in the Lunar Rover and adapted it for use by paraplegics in driving automo­biles and vans. Kurzweil Artificial
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CIRCLE NO 49

Intelligence (Cambridge, MA) markets a voice-activated word-processing system and has sold 30 of those systems to handicapped people.

The diversity of rehabilitation professionals, usually a positive aspect of the field, sometimes becomes a hindrance as well. “One of the problems in the field is that people are highly parochial,” Romich says. Indeed, heated conversation ensued at a recent RESNA meeting, when engineers said they felt that the organization should make a greater effort to meet their needs, as opposed to those of occupational therapists, physical therapists, or orthopedic surgeons. Associations already exist to represent the interests of these professionals, the engineers argued, but engineers in the rehabilitation field need a home of their own.

Still, the field’s generally low turnover—at Stanford, 50% of the staff members have been there longer than five years—indicates the high level of personal satisfaction that members derive from their work. Says Romich: “It’s hard to be down on life when you’re working in this field.”

“A rehabilitation engineer should be first a good engineer, then follow with clinical experience.”

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We need experienced individuals interested in working on file system implementation. You'll need experience in one or more of the following:
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For the above positions, you should also have programming experience in high-level languages (in addition to C), a BS or MS in Computer Science, and 5+ years of experience (or equivalent combination of degree and experience). Knowledge of VMS internals is a plus.

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You'll participate in the design and development of windows software and interact at a detailed technical level with other engineering groups within Digital. Ideally, you'll have the following experience:
• 5+ years' experience in operating systems
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• Data communications and/or distributed applications
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• User experience with VAX/VMS®, VAX/ULTRIX®, or UNIX

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You'll be responsible for technology issues relating to current and future programs.
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• SPICE modeling
• Developing test cases

Requires a BSEE and 5+ years of experience in VLSI design and/or applications. Background should include at least 2 years of design experience with gate arrays, ASICs, and full design or involvement in the selection, specification and process of these devices.

For consideration or more information about the above positions, please send your resume to: L. Taylor, Manager, Dept. 0303-8820, DECwest Engineering Group, Digital Equipment Corporation, 14475 NE 24th, Bellevue, WA 98007. Proof of legal right to work in the U.S. is required.

We are an affirmative action employer.

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Don Rothwell
Office Manager
Tactical Secure Communications Office

The professionals of Motorola's Government Electronics Group (GEG) have much to say about their company because GEG is a place where innovative ideas are put into action. The result is leadership in the research, development and manufacture of electronic hardware for our country's defense, national security and space programs. If you have the imagination and skill required to extend our technical frontiers, consider the opportunities now available.

Communication Systems Engineers
Must have experience in design and implementation of voice and data communication systems. Experience with frequency hopping and spread spectrum techniques also required. Knowledge of networking technology and packet switching concepts highly desirable. Prefer a BSEE and 7 years experience. Contact Kim Hertzmann.

LSI Design Engineers — Participate in very high speed LSI design in next generation encryption system. Detailed Bipolar LSI design and test experience desirable. Contact Kim Hertzmann.

RF Design Engineers — Various positions in the design of HF, VHF and UHF communications systems. Seeking experience in the design of multi-loop fast, settling frequency synthesizers; high dynamic range, low noise receiver front end; or broadband low loss, power combiners/dividers. Prefer BSEE with 7 years design experience. Contact Kim Hertzmann.

Radar System Engineers — Senior engineer with 10 years experience preferred. Will perform hardware design/development, new business pursuit; including proposal preparation and management. Must be able to translate broad Radar Systems requirements to specific hardware and sub-assembly designs. Contact Jerry Chadwick.

Software Design Assurance Engineers — Responsible for defining and implementing S/W QA programs. Requires thorough knowledge of engineering and QA procedures, as well as related government regulations (DOD-STD-2167, MIL-S-52779A, NSAM 81-2, NSAM 81-3). Familiarity with C, FORTRAN, Assembly, PASCAL languages as well as IBM PC's, HP computers and mini VAX computers. Prefer BSEE or BSCS with 3+ years software development experience. Familiarity with Yourdon Methodology helpful. Contact Kim Hertzmann.

CADCAM Database Project Leaders
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Gimbal Systems Design Engineers
BS/MS Mechanical Engineer with 7 years experience in the design, development, fabrication and testing of Gimbal Systems for Tactical Missiles and/or their components. Requires conceptualization of solutions for mechanical (or mechanism) design and development problems with an awareness of producibility requirements. Exposure to thermal management, component limitations, electronics packaging, radar systems and missile grade hardware requirements desirable. Contact Jerry Chadwick.


The Mind to Imagine
THE SKILL TO DO

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Requires BSEE and 4 years experience in digital logic circuit design. You should have extensive experience in: Motorola micros (68000/20), Intel micros (8085, 8086/186), MOS, CMOS, TTL, ECL, PLD's, ASIC's. Working knowledge of modems; RF and Physical Layer interfaces desired.

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Requires MSSEE/CS and 5 years hardware and software experience with extensive knowledge of data communications protocols. Working knowledge of network design is a plus.

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- Real-Time Software Systems Design
- Guidance and Control Design
- Test Systems Design
- Radar Systems
- Reliability/Quality Assurance
- Electro-Optics Design
- Missile Guidance Design

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Where quality starts with fundamentals.
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Unix in Europe will move full speed ahead

Within the next few years, Unix will experience a boom in Europe, according to Dataquest Inc (San Jose, CA). Unix is growing faster in Europe than it is even in the US, where the market doubled in 1986. The principal factors behind this more rapid growth are the X/Open group, European governments and international agencies, and European universities. Dataquest forecasts 183,140 unit shipments in Western Europe in 1991, and an installed base of 806,980 units.

X/Open, an industry group that advocates and adopts standards for application-specific systems, has contributed to the development of compatible applications programs that users can move among various computer systems simply by re-compiling them. X/Open has also focused its efforts on the development of "international" features that facilitate systems, which, although differing in language and character set, are identical in function.

Though Europe comprises many markets bound to the diverse customs, laws, and languages within each country, companies in the various European countries have united in their support of system integrations, international standards based on Unix technology. This strategy strengthens their position vis-a-vis the larger US manufacturers. Vendors offering only Unix technology can provide a superior list of features and products—for example, multiprocessors and parallel processors, multiple databases, and a variety of software and office-automation systems.

European governments and international agencies, then, have played an important part in the rise of Unix. With the intention of adopting X/Open as soon as possible, the Netherlands, Sweden, and the EEC (European Economic Community) have all accepted standards related to Unix. Some German agencies, as well as the British Ministry of Defense, have also adopted standards linked to Unix.

Although the European academic community was initially slow in recognizing Unix, it's now teaching the system to students on a wide scale. This development is significant because it guarantees a steady supply of workers trained in Unix and C. Furthermore, the universities themselves will demand a substantial number of unit shipments.

Europe should emerge as a principal consumer of Unix products by 1990. European manufacturers will exploit the X/Open base and their local organizations and distribution networks in order to combat the technological and manufacturing advantages enjoyed by US and Pacific Rim companies.

The next major development in Unix's European ascent will be the market-wide availability of applications using the X/Open system's international features and supported by various manufacturers and VARs (value-added retailers). However, because European VARs are traditionally local, the manufacturers of X/Open systems will have to resort to extraordinary measures to help the VARs distribute their software across national borders.

To terminal users, green still means go

Though long hailed for being designed to meet the needs of the human body—that is, for ergonomic reasons—amber and white display screens have yet to achieve the popularity of the traditional green screen. According to a national survey of computer-terminal users conducted by Applied Digital Data Systems Inc, 73% of those who use or are responsible for purchasing computer terminals work with and prefer the green screen. Only 21.5% of the survey's respondents expressed a preference for amber screens, and a mere 5.5% said they preferred white screens.

The future seems to hold little promise of change. When terminal users were asked what color screen they would choose to replace their present screens, 87% opted to keep their current color.

Although users remain loyal to their green screens, less than onethird of those surveyed felt screen color was important. Sixty-five percent indicated that color is not at all important to them, whereas 1% found color very important, 3% rated it important, and 31% deemed it somewhat important. Of the 35% who ascribed some degree of importance to color, 85% used or had chosen to purchase amber-colored screens. Thus, among those for whom color is a significant factor, amber gains markedly, and white remains a distant third.
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