Advanced features elevate 32-bit μPs to new heights
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CIRCLE NO 114
From the Company That Wrote the Book on STD DOS...

The Industrial Strength Computer Family

STD DOS is Ziatech’s implementation of IBM PC DOS on the rugged, low-cost STD Bus, giving industrial control applications access to the huge library of IBM PC software. In other words, a PC tough enough for industrial applications. Ziatech offers a complete family of STD DOS target systems and development tools designed to meet your application’s specific requirements.

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Ziatech’s STD DOS V50 delivers IBM AT performance and software compatibility.

Low Cost DOS, Under $600

STD Mini-DOS runs PC DOS on a single 8088-based STD Bus computer for applications with physical size constraints requiring less than 62K application program memory, instruments, data-collection terminals, and machine control applications can be equipped for under $600 in single quantities.

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Ziatech’s original two-board set includes an 8088-based single board computer and a DRAM memory board for applications with large memory needs. Both Mini-DOS and the original STD DOS feature two parallel ports, five counter/timers, a serial port, interrupt controller and provisions to add an Intel 8087 math co-processor.

Video Options, New Driver Support, and More

System developers wanting to see more of the STD DOS family can choose from a growing list of options, including an EGA video/keyboard controller, disk subsystems, multiprocessing, solid-state disks, a device driver library called STD DDP, and a soon-to-be-released CMOS STD DOS system.

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FREEZE VIDEO SIGNALS WITH A SAMPLE & HOLD AMP LIKE THIS.

Introducing the VA730 High-Speed Sample & Hold Amplifier... the only monolithic IC of its kind that operates in the 50MHz range. The only one that's available in surface-mount packaging, and in both commercial and military grades.

And the only one that's designed specifically to operate with 8-bit flash converters.

Best of all, not only is it less costly than expensive hybrids, it's priced well below competing Japanese monolithics.

The VA730 has an A/D converter reference power supply, a sample & hold function, and an ECL clock output section operating to a frequency of 50MHz.

It's available in a 14-pin cerdip package, a 20-pin ceramic leadless chip carrier (LCC), and in die form.

The VA730 Sample & Hold Amp is just part of VTC's broad line of Linear Signal Processing (LSP) ICs, which includes Op Amps to 500MHz gain bandwidth, precision, high-speed, and fast settling, plus dual and quad... with no sacrifice in performance.

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A family of ECL and TTL High-Speed Comparators to 1.5GHz.
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And Operational Transconductance Amplifiers to 50V/µsec, 75MHz.

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For samples and data sheets on the VA730, or any of our LSP products, call toll-free or write us today: VTC Incorporated, 2401 East 86th Street, Bloomington, MN 55420. (In Minnesota: 612/851-5200.)

CALL 1-800-VTC-VLSI
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CIRCLE NO 113
When perusing this year’s µP/µC Chip Directory, you may be surprised to find that software is becoming as important as the microprocessor in the design of a µP-based system. See pg 100.

(Photograph courtesy National Semiconductor; design by Petretto/Cook Design Group; photography by Lindstrohm Photographers)

DESIGN FEATURES

EDN's 14th Annual µP/µC Chip Directory 100

Choosing the µP is no longer the most important decision an OEM must make in designing a µP-based system. VLSI progress and software momentum have relegated the µP to the role of a team player.—Robert H Cushman, Special Features Editor

Designer's Guide to Switching Power Supplies—Part 2 191

Part 1 of this 2-part series dealt with simple switching power supplies and described a “cut and try” approach for stabilizing a supply’s feedback loop. The conclusion offers advice on designing more complicated switching supplies, ones with isolated outputs.—Jim Williams, Linear Technology Corp

Use of transimpedance amplifiers minimizes design tradeoffs 205

Transimpedance amplifiers, unlike standard voltage-input designs, maintain constant bandwidth regardless of the gain setting. You can use these amplifiers in video-speed and RF circuitry without having to decrease the gain at high frequencies, while maintaining good dc performance and low power consumption.—Alan Hansford, Analog Devices Inc

Eliminate the guesswork in analog-switch error analysis 219

As the accuracy and speed of data-acquisition systems increase, analog-switch errors can consume increasing portions of the error budget. However, you can employ several circuit-design techniques to minimize the effects of device limitations.—Stephen Moore, Siliconix Inc

Use op amps to design optical position-sensing circuitry 229

You can design a variety of op-amp circuits to condition optical position-sensing signals. Depending upon the special requirements, S/N ratio, input-signal strength, and cost constraints of your application, you can use one or more of the configurations presented here to implement your position-sensing circuitry.—Jerald Grinme, Burr-Brown Corp

Continued on page 7
Introducing perfect 32-bit balance

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A no-compromise solution for true 32-bit systems integration. At a price that won't weigh you down.

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CIRCLE NO 112

EDN November 26, 1987
TECHNOLOGY UPDATE

Motor-control ICs extend performance levels of stepper and brushless dc motors

Stepper motors and brushless dc motors find use in applications ranging from copiers and robotics to computer peripherals, and such applications demand monolithic ICs dedicated to the task of providing speed and position control.—Dave Price, Associate Editor

Silicon microstructures let manufacturers implement a variety of sensors on chip

Silicon, an element synonymous with low-cost digital electronics, is now the basis for inexpensive, IC-size analog sensors. Manufacturers have been selling silicon pressure sensors since 1985, but in the past six months they've branched out to offer other kinds of sensors that are chemically etched from a silicon substrate.—JD Mosley, Regional Editor

PRODUCT UPDATE

Synchronized 5¼-in. Winchester drives

DESIGN IDEAS

Open-loop servo adjusts shaft position
Simultaneous-addition algorithm saves time
PLD functions involve enabling outputs
Fast algorithm computes square root
Circuit measures op-amp settling time

Continued on page 9
Now see what your hardware and software are really doing, in real time, without waiting for problems to repeat. Nothing else comes close to tools like these in Tek's DAS9200 Digital Analysis System:

- **Register deduction.** Acquire and disassemble up to 32K samples of processor activity. The DAS9200 can show you the contents of the register before the problem occurred!

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In Oregon, 231-1220.
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EDN November 26, 1987

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Articke-writing programs load perks—and pressure—on engineers.
—Deborah Asbrand, Associate Editor

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Beware of the hidden costs of foreign sourcing.

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**Single supply MC33171 uses one-eighth the power.**

Operating from a single, ±3 to ±4 V supply, or dual ±1.5 to ±22 V supplies and with a common mode input which includes ground, the MC33171 family provides superior performance to industry standard bipolar single supply op amps. While consuming one-third the drain current of the LM324 and one-seventh the drain current of the MC3403 quad op amps, the MC33174 offers nearly double the bandwidth and slew rate of the popular devices.
The MC33171 provides 1.8 MHz bandwidth (nearly twice that of ordinary JFETs), and a 2.1 V/µs slew rate. This bipolar family has performance comparable to low-power JFET input op amps such as the TL061 and LF444 series but it provides a much better output voltage swing: 28.4 V p-p with ±15 V supplies.

**High performance MC34181 JFET sizzles at 4 MHz.**

That's four times more bandwidth than the LF444 and TL064.
What's more, this new family provides extremely fast settling times, 1.1 µs to 0.1% and 1.5 µs to .01%, ideal for A/D sample-and-hold circuits. Its 10 V/µs slew rate is three times greater than the TL061's and ten times more than the LF444's. Combine these parameters with the MC34181's low, 2 mV Vp-p, very high input impedance for low input bias and offset currents of 3 and 1 pA, respectively, and you have the answer to precise performance in instrument amplifiers.
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50-µW VOLTAGE COMPARATORS SPEC 2.5-µSEC RESPONSE TIME

The TLC393, TLC3702, TLC339, and TLC3704 voltage comparators from Texas Instruments (Dallas, TX, (800) 232-3200) are fabricated in polysilicon-gate LinCMOS technology, which allows them to draw only 1/20 the current used by similar bipolar devices. They typically provide a 2.5-µsec response time, but dissipate only 50 µW of power. Although these devices combine low power and high performance, the manufacturer asserts that their worst-case input offset voltage drift is typically 0.23 µV/month. Operating from a single 5V supply, the TLC393 and TLC3702 contain two independent differential-voltage comparators, and the TLC339 and TLC3704 contain four. The TLC393 and TLC339 both have open-drain TTL-compatible outputs, while the TLC3702 and TLC3704 have push-pull outputs that eliminate any need for external pullup resistors for driving capacitive loads. The TLC393 costs $0.52, the TLC339 is $0.65, the TLC3702 is $0.58, and the TLC3704 sells for $0.73 (100).—J D Mosley

PARALLEL-PROCESSOR DEVELOPMENT SYSTEM RUNS ON A PC

Coupled with an IBM PC/AT or equivalent computer, the SIMD (single-instruction, multiple-data) Processor Development System (SPDS) provides a complete software-development environment for NCR Corp's (Fort Collins, CO, (800) 334-5454) Geometric Array Parallel Processor (GAPP). The $50 (10,000) GAPP, which targets image-processing and pattern-recognition applications, incorporates a 6x12-element array of 1-bit processors. Although the company has previously offered software-development tools for the GAPP, its $28,500 SPDS is the first to offer full-speed GAPP program execution. SPDS performs this feat through hardware installed in a separate card cage. The card cage contains a controller card that communicates with a corresponding host-interface card in the PC over a 16-bit interface. The card cage also includes one array card containing 40 GAPPs (a 60x48-element array). You can install as many as four GAPP array cards in the SPDS cage, thereby creating arrays containing processor arrays as large as 108x96. The package also includes a compiler, linker, and debugger for developing software with the company's proprietary GAPP Algorithm Language.—Steven H Leibson

INTERFACE CARD PROVIDES DATA ACQUISITION FOR IBM PS/2

An interface card from Keithley Instruments (Cleveland, OH, (800) 552-1115) lets you use your IBM PS/2 Model 50, 60, or 80 computer for data-acquisition and control applications. The card plugs into your computer and provides a link to 10 slots in Keithley's external Series 500 card cage. To customize the system to fit your applications, you can select from 30 different data-acquisition modules that plug into the Series 500. For $770 you get the interface card and an upgraded version of Soft500 data-acquisition software on both 5¼- and 3½-in. floppy disks.—J D Mosley

POWER-SUPPLY OPTION REDUCES LINE-CURRENT NEEDS

An active power-factor-correction (PFC) option available in selected off-line converter products from Pioneer Magnetics Inc (Santa Monica, CA, (800) 233-1745) reduces the power supply's rms line-current needs. For example, a typical 115V ac, 15A circuit using a standard UL wall plug can support a 1000W output supply with correction; without correction it could support only a 700W supply. The PFC option converts the high-current pulses normally drawn by a switching power supply into a sinusoidal
waveform that's in phase with the ac line voltage. When the current waveform exactly matches the voltage waveform, the power factor becomes almost unity (0.99). As a side benefit, the PFC option also significantly reduces line harmonics between 10 and 150 kHz. The option is currently available on the company's PM2900 and PM2501B Series supplies. $200 (OEM qty).—Tom Ormond

TWO HIGH-DENSITY ASIC ARRAY FAMILIES EXCEED 100,000 CELLS

Using 1-µm drawn gate lengths, 1.2-µm design rules, and three metal layers to route signals and power, the Max HD100 Series CMOS macrocell arrays from Motorola Inc (Phoenix, AZ, (602) 821-4426) encompass more than 100,000 cells. In addition, the ASICs feature internal gate speeds of 400 psec (with a fan-out of 2) and offer as many as 512 configurable I/O cells. You can use the vendor's $7500 Modular Design System software package and $500 HDC macrocell library to develop designs for the Max family on a Mentor Graphics workstation.

Initially, the company plans to offer three members of the Max family: the HDC016, HDC031, and HDC100, which have 16,416, 31,290, and 104,832 cells, respectively. Nonrecurring engineering (NRE) charges for these arrays range from $35,000 to $250,000. The company estimates that you'll be able to use approximately 75% of the available gates on the devices in a typical design. Part costs range from about $37 for a 16k-cell array packaged in a plastic, quad flat pack to approximately $624 for a 100k-cell array packaged in a multilayer, ceramic pin-grid array.

Another CMOS ASIC array family, LSI Logic's (Milpitas, CA, (408) 433-8000) LCA100K Compacted Array Plus Series, realizes 100,000 usable gates on one die. To do so, the ASICs employ three layers of metal; a 0.7-µm channel length; and a 236,880-gate master slice that measures 590 mils per side. The family also includes devices with 139,104 and 187,748 gates, which the company estimates will yield 60,000 and 80,000 usable gates, respectively. The arrays exhibit an internal gate delay of 460 psec with a fan-out of 2.

The LCA100K family also offers as many as 344 I/O cells per device. You can configure the I/O cells as inputs, outputs, bidirectional pins, or 3-state nodes, and you can use these cells to drive internal as well as external signals. Each I/O cell can source and sink as much as 12 mA, and you can parallel two cells for a 24-mA driver. The parts come in either ceramic pin-grid arrays having 155 to 299 pins or ceramic leaded chip carriers having 144 to 300 leads. The company offers the Modular Design Environment (MDE) software package, which lets you develop designs for the LCA100K ASIC family on Sun Microsystems workstations. Depending on configuration, the MDE software costs from $50,000 to $300,000. NRE charges for the LCA100K family start at $150,000, and parts cost $200 and up, depending on the array and package you select.—Steven H Leibson

PROTOCOL ANALYZER FOR ARCNET LAN MAKES ITS DEBUT

Arcnet LAN users can now employ the Model PA-404 Arcnet Sniffer from Network General (Sunnyvale, CA, (408) 734-0464) to locate network problems. The $19,000 protocol analyzer captures frames from the network and can save this information on its integral disk for later evaluation. In addition, the instrument can stress the network by generating traffic to test the LAN's ruggedness and performance under load. For an additional $5000, you can acquire a dual-LAN Sniffer with diagnostic capabilities for Arcnet LANs and either Ethernet or token-ring LANs.—Steven H Leibson

EDN November 26, 1987
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SLIC IC PROVIDES TYPICAL LONGITUDINAL BALANCE OF 60 dB

The SL373 telephone subscriber-line interface circuit (SLIC) IC from Plessey Semiconductors (Swindon, UK, TLX 449637; in the US, Irvine, CA, (714) 472-0303) provides a power feed to the line, controls relays for ring injection and line testing, detects ground-key and off-hook conditions, and performs 2- to 4-wire conversion. You can program these functions to suit a variety of telephone standards, and you can also program the thresholds of the ring-trip and loop detectors. The device's common-mode rejection allows it to achieve a 60-dB longitudinal balance for the line. Power fed to the line is controlled by an on-chip switch-mode regulator that limits device dissipation to 1W—eliminating any requirement for a heat sink. The IC also has a low-power standby mode, and it can supply both the normal and reversed telephone line polarities often required for the transmission of billing information. The SL373 is packaged in a 28-pin ceramic DIP or J-lead surface-mount package. The DIP version sells for £10.93 (1000).—Peter Harold

MITI WILL ALLOW AN 80% INCREASE IN 1M-BIT DYNAMIC RAMs

The Japanese Ministry of International Trade and Industry (MITI) has relaxed certain semiconductor-production limits for the fourth quarter of 1987. The ministry has raised the production ceiling for 1M-bit RAMs by 80%, which will permit Japanese semiconductor manufacturers to turn out 21.5 million 1M-bit dynamic RAMs in the fourth quarter. At the same time, MITI will allow manufacturers to produce 152 million 256k-bit dynamic RAMs, which represents a 4.5% increase in production. MITI projects that Japan will export about 14.7 million of the 1M-bit dynamic RAMs and 89 million of the 256k-bit units. US computer firms are expected to buy 70% of the exported 1M-bit parts.—Joanne Clay

256k-BIT ECL RAM OFFERS 15-NSEC ACCESS TIME

Hitachi has produced an ECL RAM that offers a 15-nsec access time. The CMOS-bipolar device consumes 400 mW. Its I/O circuits and sensor amplifier are implemented in bipolar technology, and its memory cell in high-resistance, polysilicon-load, 4-transistor NMOS technology. The decoder is implemented in CMOS-bipolar circuitry. Samples will be available in March 1988; they'll sell for ¥24,000 (or $165.50) each.—Joanne Clay

SEMICONDUCTOR DISKS HAVE <1-MSEC ACCESS TIMES

Designed for use with Hewlett-Packard's minicomputers, these three semiconductor disks from disk-drive maker ISA (Tokyo, Japan) offer <1-msec access times and come in 32M-, 64M-, and 128M-byte versions. The disks specifically target the HP computers used on US military ships and aircraft. The company's US distributor, IEM, will market the parts in the US. The disks cost from $24,966 to $67,310.—Joanne Clay
The New 4180 Plug-In

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  SAT (SMA) $14.95
  TAT (TNC) $12.95
  NAT (N) $15.95

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EDN November 26, 1987
CIRCLE NO 106
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Need a tidier single chip than the DIP? Ask us about the new SOJ package that provides the megabit DRAM in J-lead surface mount. Or, get still more compactness with the OKI ZIP package’s very narrow profile.

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EDN November 26, 1987

TERADYNE
We measure quality.
Hardware/software for Macintosh deserves mention

I found your report on PC-based GPIB control and data-acquisition products (EDN, August 6, pg 94) very informative. However, I would like to suggest a future improvement for articles of this type.

Mainly because of its innovative user interface, the Apple Macintosh is currently finding its way into more and more corporate and engineering assignments. In many categories, the best software available runs on the Macintosh, and the open-architecture Macintosh SE and Macintosh II allow much more flexibility in hardware interfacing than do earlier models.

Your GPIB article included information on software and hardware only for IBM PCs and compatibles. Not mentioned were three similar products for the Macintosh: Reed College’s Benchtop Instrument, GW Instrument’s MacAdios, and National Instrument’s Labview. A review of Labview appeared in the May 1987 issue of MacWorld magazine. The program has an impressive graphical interface that does not require programming experience, yet it’s also very powerful—it’s able to control almost any IEEE-488- or RS-232C-based equipment.

In the future, please include the Macintosh in your reports on microcomputer-based software and hardware.

John Bartleson
Spokane, WA

Design Idea author swamped by EPROMs

In order to operate, the circuit in the Design Idea “Talking meter gives de-voltage readings” (EDN, August 6, 1987, pg 224) requires some tedious programming of an EPROM. The author, Ricardo Jimenez-G, had graciously offered to send readers a photocopy of the data program or to return a programmed EPROM to anyone who sent him a blank device.

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CIRCLE NO 29
As of October 5, Mr. Jimenez-G has received more than 50 requests and 25 blank EPROMs. What’s more, his EPROM programmer has broken down. Therefore, he is withdrawing the programming offer but will continue to send a photocopy of the program to any interested reader who requests one. (Include a self-addressed envelope with two $0.22 stamps.) His address is: Ricardo Jimenez-G, 96 Carmen Rivera Ave, Mexicali, Baja California, 21280 Mexico.

Emulators available
EDN’s July 23 report on 16- and 32-bit emulators (pg 252) failed to mention our products. We offer emulators for both the 8088 and the 8086. The Icebox includes 64k bytes of overlay RAM and 65,536 full-speed hardware breakpoints, and sells for $1395. An optional hardware performance analyzer is available. Our emulators come with a money-back guarantee.

DoD-STD-2167 document generator
We read with interest the article “CASE tool kits tailor DoD-STD-2167 requirements for software documentation” (EDN, August 20, pg 81). We were dismayed to see that ModaLogic’s Necessity tool set was not included in the article.

Necessity is a true DoD-STD-2167 tool set that produces accurate DoD-STD-2167 documents in the formats required by the appropriate Data Item Descriptors (DID). The Necessity tool set uses a menu format to solicit information from the system analyst or designer. The user needs to make only the minimal number of keystrokes to create a document. The output of Necessity is a finished document ready for review. Necessity is not an aid to the DoD-STD-2167 effort; it is a fully automated document generator.

By using the Necessity tool set, we have been able to provide DoD-STD-2167 documentation for commercial and industrial projects that don’t contractually require the standard.

A J Horning
Chief Engineer
ModaLogic Inc
Richfield, OH

WRITE IN
Send you letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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TASCO has complemented its unique line of MIL-STD-1750A In-Circuit Emulators with a low cost line of off-the-shelf VME bus compatible single board computers. The line includes computers based on the:
- MDC281 CPU TVME/1750AD SBC
- PACE1750A CPU TVME/1750ASP SBC
- F9450 CPU TVME/1750ASF SBC

Support tools include TASCO’s emulators, Hewlett-Packard’s HP 64000 and others.

For additional information, please contact M. Blasberg.

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CIRCLE NO 4

CIRCLE NO 5

EDN November 26, 1987
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The entire state of New Jersey on a chip.
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It's no wonder people expect big things from LSI Logic. We're the largest HCMOS ASIC company there is.

But that doesn't mean you have to be the largest in your field to come to us.

You just need to be doing ASIC. No matter if it's a few hundred gates or a complete system on a chip. Or even a multi-ASIC system.

It's plain and simple, really: We understand your ASIC might not need 100,000 gates today. But it's good to know it's here when you need it.

To simplify your ASIC design task, we have the largest library available of SSI and MSI building blocks. And more than 400 industry-standard LSI and VLSI building blocks for Channeled and Channel-Free™ Arrays, and Cell-Based designs.

So whether you need an array or cell-based product, you're covered.

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So don't worry about how big or small your ASIC need is. We're the right size for you.
WE HAVE SEEN THE FUTURE.

Mini on a chip.

AND IT IS VERY TINY.
Saying our new Modular Design Environment (MDE)™ is the most advanced ASIC design software anywhere isn’t small talk.

Using MDE, we’ve already accurately designed and simulated systems with more than two million gates of logic. And that’s just for starters.

Our software easily migrates into the latest technology. So your design will always have the highest performance and densities.

MDE is actually comprised of three modules.

The Logic Integrator™ is an entry-level module containing the design and simulation tools for building single ASIC chip designs.

The Silicon Integrator™ module handles the design and simulation of complex ASICs ranging from a few hundred to 100,000 usable gates. Its Silicon Compilers allow you to automatically develop logic and memory. Your compiled designs, of course, all have complete simulation and test vectors.

You can also effortlessly convert PALs to arrays with our Logic Synthesizer.

Our System Integrator™ module has mixed-mode behavioral and gate-level simulation capabilities. Use it to design your entire system, including multiple ASICs and standard components.

All with surprising ease and economy. So you can “electronically breadboard” your complete system before going to prototype.

And you can design your ASICs on more platforms than anywhere else. Like all the popular workstation and mainframe environments. Or commercial CAE systems through our CAD Connection Program. Or at one of our 24 Design Resource Centers—the world’s largest ASIC support network.

MDE is also tightly coupled to our worldwide manufacturing facilities. Which is why LSI Logic delivers working parts 100% of the time. Guaranteed.

And why you’ll see your future a lot sooner with us.
With more than 4,000 working designs under our belt, one clear fact emerges.
Our system works.
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MDE can be tailored to your specific situation. Just select the appropriate design modules.
We have all the performance you’ll need. Such as ECL-like speed in 1 or 1.5-micron HCMOS technology with gate delays of 460 picoseconds. And even more coming soon.

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That’s our system.
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Circle 120
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The low profile and small footprint of this remarkable new sensor enable you to create more compact equipment designs for remote switching applications such as occupancy monitoring, intrusion alarm, light switching, counting, level monitoring, speed indication and many other safety and security operations.

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1 1 GHz. The 11402 Digitizing Oscilloscope features a full 1 GHz bandwidth right on the probe tip to help you make the most demanding voltage and timing measurements.

2 10-14 BIT VERTICAL/10 ps HORIZONTAL RESOLUTION. 10-bit vertical resolution is averageable to 14 bits. Self-calibration decreases error to less than 1% DC.

3 AUTOMATIC MEASUREMENTS. Up to six measurements can be made at the push of a button, with results simultaneously displayed and continuously updated.

4 PUSH-BUTTON HARD COPY. Plug in a Tek or compatible Epson dot matrix printer using the scopes standard Centronics port.

5 AUTOSET. Push a button on the front panel or on the probe to automatically set up the scope based on the signal characteristics of the selected trace.

6 TOUCH SCREEN. Select a trace, a trigger, a measurement or other function by touching the appropriate area of the screen or by selecting from pop-up menus: the closest, most natural link yet between user and scope.

Tektronix introduces the 11000 Series: the new standard in digitizing and analog oscilloscopes.

These new fully programmable scopes display more traces (up to 8) at higher bandwidths (up to 1 GHz), with greater accuracy (up to 0.6% vertical), and include more new functions for expediting the capture and processing of data than can ever be listed here. Two new digitizing scopes exert the power of three 16-bit processors, long records, the most powerful triggering and the highest throughput ever. Use their built-in dual timebases to easily acquire pre- or post-trigger details of a trace, and view both the whole trace and the details on screen at once.

Two analog scopes feature an integrated 500 MHz universal counter/timer for unequaled resolution, accuracy, and scope versatility — for the

THE NEW ERA IN DIGITIZING AND ANALOG OSCILLOSCOPES.
price of a scope alone. A unique counter view trace lets you see exactly what you are triggering on, for a sense of confidence no conventional counter/timer can offer.

Perhaps most startling is the simplification and automation of the whole measurement and analysis process. Larger displays, pop-up and touch-screen menus, plus automated setup and measurement capabilities help unclutter the front panel and keep eyes focused on the display. For the first time, users need know nothing about a scope's technology to get the most out of it.

The 11000 Series continues the plug-in versatility of the Tek 7000 Series. Five new plug-ins and three new probes tailor the new scopes to a full range of applications, from design and debug to production test. New single-ended amplifier and differential amplifier plug-ins combine high bandwidth with low noise and fast overdrive recovery.

Demonstrations are now in progress. For more information or a personal demonstration, get in touch with your local Tek sales engineer. Or call Tektronix at 1-800-547-1512.

EDN November 26, 1987

Tektronix
COMMITTED TO EXCELLENCE
Motorola announces one of the smallest advances in the history of VME.
Motorola puts awesome multiprocessing performance on two new single-board computers.

As computer applications get more complex, OEMs are turning more to multiprocessing designs. To handle things like CAD/CAM, robotics, signal processing, simulation and large-scale data acquisition, a single processor simply can’t keep up.

Adding several CPUs to a system off-loads the main processor, but what happens to the system bus? It frequently reaches saturation, slowing down the entire system.

Motorola introduces a single chip solution to this problem. The VME Subsystem Bus, a fast, 32-bit secondary bus, has been implemented on a gate array at Motorola.

The end of the multiprocessor traffic jams.

The VSB sub-bus removes traffic from the VMEbus, increasing total system throughput. And by saving space on the VSB—and other components—Motorola has been able to pack an impressive array of multiprocessor functions onto two standard VME boards: the MVME135 and MVME136. These highly integrated microcomputers include all the functions usually required for high-performance multiprocessing. In addition to the VSB, they feature the MC68020 with floating-point coprocessor, both running at either 16.67 or 20.0MHz.

For virtual memory environments, a demand-paged memory management unit can also be added. Plus 1 Megabyte of shared local dynamic RAM is included—with optional parity—designed to operate with zero wait states.

Included in the 135/136 modules are many special hardware features that facilitate multiprocessing. Things like MP control and status registers. An expanded interrupt-handling mechanism. And master/slave control bit settings.

Hardware alone is hardly enough.

Complete multiprocessing hardware on a single board saves you design time and system space. But to get your application up and running on a tight schedule, it takes software and support tools too. Like those available from Motorola.

If you’re building a multi-user/multi-tasking system, you can use our version of AT&T’s UNIX® System V Release 3, with Remote File Sharing. For real-time tasks, there’s our full-featured VERSAdos® operating system, as well as debugging firmware with on-board diagnostics. Then too, you have access to third-party software such as OS-9®, MTOS®, PDOS®, pSOS®, RTUX®, and VRTX.

Add to that Motorola’s in-depth technical support. We have more experience in building reliable, high-performance VME system components than any other vendor. Plus a specialized systems and support staff available at over 100 field offices worldwide.

To see how good multiprocessors can come in small packages, call us toll-free today: 1-800-556-1234 Ext. 230 (in California, 1-800-441-2345 Ext. 230). Or write; Motorola Microcomputer Division, 2900 South Diablo Way, Tempe, AZ 85282.

MVME135/136 Highlights

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MVME135</td>
<td>VMEbus 32-bit SBC; 16.67-MHz MC68020 CPU; MC68881 FPU; 1Mb on-board DRAM; up to 512 Kbp EPROM; two RS-232-C serial ports; two 16-bit timers; master/slave interface; MP control and status registers; system controller</td>
</tr>
<tr>
<td>MVME135-1</td>
<td>Same as MVME135, but with 20-MHz MC68020 CPU</td>
</tr>
<tr>
<td>MVME136</td>
<td>Same as MVME135, but with MC68851 PMMU</td>
</tr>
</tbody>
</table>

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MOTOROLA Microcomputer Division
Approaching our technology from your point of view.

CIRCLE NO 65


Lasers '87, Lake Tahoe, NV. Society for Optical and Quantum Electronics, Box 245, Mclean, VA 22101. (703) 642-5835. December 7 to 11.


Third Annual Battery Conference on Applications and Advances, Long Beach, CA. Cecile Duong, Department of Electrical Engineering, California State University at Long Beach, 1250 Bellflower Blvd, Long Beach, CA 90840. (213) 498-4605. January 12 to 14.

Modern Electronic Packaging (seminar), Orlando, FL. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. February 9 to 11.

Unix Technical Conference, Dallas, TX. Usenix Conference Office, Box 385, Sunset Beach, CA 90742. (213) 592-1381. February 9 to 12.
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EDN November 26, 1987
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- Low power requirement
- Low noise

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In 1984, we introduced the 68020. Now, three years later, it has the largest installed and broadest application base of any 32-bit MPU on the market. Having set that standard in the first place, we feel qualified to raise it. Which is why the only microprocessor that really surpasses the 68020 is our second generation 68030.

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The '030 is twice the microprocessor its predecessor is. It's the first to sport an instruction cache, data cache and MMU on-chip. Combined with a Harvard-style parallel bus architecture that allows simultaneous, multiple fetches of instructions and data, processor throughput is pushed to unmatched levels.

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With its burst fill mode for the dual caches, you'll be able to squeeze SRAM performance from low-cost DRAMs. It gives you graphics capability without the need for a graphics co-processor. And there's true object-code compatibility between the '030 and the '020. All this adds up to economies you can count on.

An architecture you can build on.
And count on.

Application software that runs on any 68000 family MPU runs on the 68030. There's also a full array of development tools, and a new 68882 floating point co-processor, with up to 4x the performance of its predecessor. All of which gives your product plans an enormous amount of continuity. And that's not going to change. Since the 68030 supports both MS-DOS™ and UNIX® V.3, you can have your pick of over $12 billion worth of applications—and the broadest possible market.

With Motorola, you can see forever.
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For more information about the new 68030, call us toll-free at 800-521-6274 or write, Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

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EDITORIAL

Base telephone-access fees on actual use

The Federal Communications Commission (FCC) may make you pay extra for the privilege of using professional and consumer databases, electronic-mail services, computer bulletin boards, and other enhanced services. According to the FCC, people who use enhanced services are getting bargain rates at the expense of regular long-distance telephone customers. When long-distance phone carriers access local phone lines, they must pay local phone companies a fee. Under FCC regulations, enhanced-service providers (ESPs) such as Compuserve, Telenet, and the Source have avoided such fees—at least so far. Now, the FCC says that the ESPs must start paying for access to local phones such as yours and mine.

The enhanced-service providers argue that the FCC’s fixed access fee is unfair. Because there are fewer ESP calls than long-distance calls, the cost of a call to a database would increase by as much as $4.50 per hour, but long-distance charges would decrease only slightly. Further, the ESPs see the new arrangement as discriminatory. Thousands of corporations and government agencies have interstate networks, and none of them pay extra fees to connect to local phone systems.

It’s difficult to find anyone who will benefit from the FCC’s proposal to redistribute access charges among long-distance phone carriers and ESPs. In fact, there will be many losers. Because the enhanced-service providers will simply pass their costs through to their users, many students, libraries, and small businesses will balk at paying the higher rates. Thus, the database and data-communications industries may die an early death.

But before you rail at the FCC, remember that the long-distance carriers are in fact subsidizing the data services as well as others. Perhaps giving the new data services a subsidized start was worthwhile, but it’s time to wean them from the long-distance subsidies. On the other hand, the FCC’s proposal seems to force unreasonable fees on the infant data-service companies and their subscribers. Perhaps there’s a compromise position: The FCC could base telephone-access fees on actual equipment use rather than on its availability. Such a scheme requires extra accounting, but it seems to be a fair and realistic way to distribute costs.

Jon Titus
Editor

EDN November 26, 1987
The time and space saving Signetics PLHS501.

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An "instant gate array" with no "gate-a-risk." The high-speed ($t_{	ext{typ}} = 22\text{ns}$) Signetics PHS501 Programmable Random Logic unit blows away your gate array development time. And with it your NRE, inventory problems and quality concerns. It's programmable or reprogrammable within hours—not weeks. And delivered on schedule, fully tested.

**No interconnect restrictions.** The unique single NAND array architecture of the PHS501 eliminates the design constraints of AND/OR gates by delivering more utilization of on-chip resources. There are no interconnect restrictions because any NAND gate connects with any other NAND gate.

**Single-chip space saver.** The PHS501 provides 1300 effective gates—a complete solution on a single 52-pin PLCC package.

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CIRCLE NO 63
Digital has it now.
“Our Dracula™ layout design verification software was developed and based on Digital systems, and for very good reason,” states ECAD President Jim Hill. “Our customers in Integrated Circuit design regard Digital’s VAX™ systems as the standard. Recognizing that, we’ve developed a line of software products that have made us the standard of our industry.”

According to Mr. Hill, Digital’s unmatched software compatibility offers real benefits in creating customer acceptance. “We know that whatever Digital system the customer has purchased, our software will run on it successfully. That kind of confidence is rare in the IC design industry. And Digital’s hardware and software consistency helps us deliver a better product, faster and at a lower cost.”

“We're aggressively pursuing a worldwide market,” Mr. Hill adds. “And Digital has the worldwide presence to help us sell each market with strong local support. Our software and Digital’s systems sell each other. ECAD and Digital have evolved a strategic partnership, one that gives us a proven competitive advantage in the marketplace.”

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ITT CANNON
We're making progress. Not excuses.
Motor-control ICs extend performance levels of stepper and brushless dc motors

Dave Pryce, Associate Editor

Stepper motors and brushless dc motors find use in applications ranging from copiers and robotics to computer peripherals—especially computer peripherals, where disk drives, tape drives, and printers account for the lion's share of the total volume. Such applications demand monolithic ICs dedicated to the task of providing speed and position control.

This demand is sure to continue. Both floppy- and Winchester-disk drives depend on brushless dc motors for spindle-speed control and stepper motors for read/write head positioning. A printer requires one stepper motor for each function, so even a printer with only three functions (ribbon feed, paper feed, and carriage drive, for example) requires three motors.

One of the most successful of the stepper-motor control and driver circuits is the PBL3717, which has found wide acceptance in disk-drive and printer applications, and which Rifa introduced in 1982. The original PBL3717 (and its upgrades and derivatives) drives a bipolar constant current through one winding of a 2-phase stepper motor (Fig. 1). Each motor requires two devices.

The original 3717's drive-current rating is 0.8A continuous, 1.0A peak. Upgraded versions are available that can handle as much as 1.2A, including Rifa's PBL3717/2, Cherry Semiconductor's CS3717A, Unitrode's UC3717A, and SGS's PBL3717A. All of these derivatives come in 16-pin power DIPs. Thomson-Mostek sells a similar device enclosed in a power package that is capable of supplying a maximum drive current of 1.5A. (The device is also available in a DIP.) All of these ICs sell in the $1.80 to $2.10 range (1000).

Recently, Rifa introduced the PBL3770A, a 1.5A continuous (1.8A peak) high-performance version that sells for $3.87 (1000). This circuit requires external-protection diodes; the other devices include them on chip. Apart from this difference, however, they all have identical architectures and pin connections.

The 3717-type devices use switch-mode regulation to achieve current control and use the input logic terminals to provide a preset function that differentiates between three current levels. The phase input determines the direction of the current in the motor winding. A Schmitt trigger at the phase-input pin provides noise immunity, and a delay circuit minimizes the risk of cross conduction in the output stage during a phase shift.

A current-sensor circuit contains...
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a reference-voltage divider and three comparators for measuring each of the selectable current levels. The circuit senses the motor current as the voltage drop that occurs across the current-sensing resistor $R_s$ and compares it with one of the voltage references from the divider. When these voltages are equal, the comparator triggers the single-pulse generator, which switches off the power feeding to the motor winding. The output stage contains four Darlington transistors and four diodes in an H-bridge configuration that drives the motor winding.

For circuits like the PBL3770A that don't include on-chip protection diodes, you can use auxiliary ICs to perform this function. The CS-299D from Cherry (Fig 2) and the UC3610 from Unitrode are two such devices. The devices are identical: Both contain eight Schottky diodes in a dual-bridge arrangement that can handle the protection requirements of two PBL3770As. (You can also use the CS-299D and the UC3610 for other driver circuits such as SGS's L298, which requires external diodes and which is also shown in Fig 2.)

Extra ICs take up less space

The CS-299D and the UC3610 are enclosed in 8-pin plastic DIPs and are relatively low in cost. They actually cost about the same as would eight diodes but, because the diodes are included in the ICs' packages, you save space. The CS-299D sells for $1.07 (1000).

The 3717-type devices have proved very successful for the applications for which they were originally intended. Nonetheless, higher-density hard-disk drives and wafer-handling and robotics applications need higher step resolution than is possible with standard stepper motors using full- or half-step modes of operation. Recent offerings from Rifa and SGS can optimize the microstepping performance of many standard stepper motors, thus allowing the use of small 2-phase stepper motors in applications where precise positioning and smooth operation are required.

Rifa's 2-chip set, consisting of the PBL3771 and the PBM3960, is intended for precision microstepping systems. The PBL3771 is a constant-current, switch-mode (chopper) dual driver for bipolar stepper motors. It is similar to two PBL3717s but has a current capability of only 600 mA per phase. The PBM3960 contains a dual 7-bit D/A converter that provides most of the intelligence and an easy interface to such microprocessors as the Motoro-
Fig 3 shows the interconnections between the PBL3771 and the PBM3960.

**Dual driver for microstepping**

In contrast to the PBL3771's single channel, each of the PBL3771's channels has added features to enhance its performance in microstepping applications. Its CD input terminals, for example, select either a fast or slow current-decay rate during the turn-off portion of the switching cycle. Each rate has its own advantages.

In the slow current-decay mode, only one of the lower transistors in the H bridge is switched on and off while one of the upper transistors is held on. During turn off, the current recirculates through one of the upper transistors (depending on the current direction) and the corresponding free-wheeling diode connected to $V_{MM}$.

In the fast current-decay mode, the circuit switches both the upper and the lower transistors. During the off time, the supply opposes the free-wheeling current, causing a rapid discharge of the energy in the motor winding. Fast current-decay rates may be necessary in half-step and microstepping applications to facilitate rapid changes in motor current. A slow current-decay rate, however, produces less ripple and minimizes core losses and switching noise.

The PBM3960 generates a maximum of 128 voltage levels plus a sign bit that controls the current level and polarity in the windings of a 2-phase stepper motor via the PBL3771. Two 3-bit registers preset a voltage level that automatically selects a slow or fast current-decay rate, thus relieving the µP of this task. This feature is especially useful in high-speed microstepping systems. The PBL3771 costs $4.64; the PBM3960 sells for $3.97 (1000). Both devices are housed in 22-pin power DIPs.

Two ICs from SGS, the L6217 and L6217A, are each functionally similar to the Rifa 2-chip set and are designed for full-step, half-step, or microstepping applications. Each circuit is capable of driving both phases of a bipolar stepper motor with pulse-width modulation (PWM) control of the phase current (400 mA per phase).

The devices are identical except for different built-in D/A converters. The L6217 has a 6-bit converter; the L6217A has a 7-bit one. Obviously, the one you choose depends on the resolution required for your particular application. The D/A converter programs the output current of each phase. Latching the D/A converter inputs and the phase inputs that select the direction of current flow minimizes the interface requirements to an external memory bus or a microcontroller.

The devices' power section is similar to other dual H-bridge drivers and includes internal clamp diodes for current recirculation. To maintain the degree of accuracy required...
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for microstepping, the circuit internally senses and compares the motor current to the output of the D/A converter. A monostable multivibrator, programmed via an RC network, sets the motor current decay time.

**Package offers advantage**

One practical advantage of the L6217 and L6217A devices involves their packaging. Both come in 44-pin plastic LCCs suitable for surface mounting. The 11 pins on one side of the package connect internally to ground to aid in heat sinking. The L6217 costs $4.25, and the L6217A costs $4.75 (1000).

All of the stepper-motor control circuits discussed thus far work with bipolar-wound motors in which the stator flux is reversed by reversing the current in the windings. Bipolar motors use only one winding per phase, but require a push-pull drive that uses four transistors for each winding. Careful circuit design is necessary to ensure that the series transistors don’t come on at the same time and short the power supply. When properly operated, a bipolar-wound motor gives optimum results at low to medium step rates.

A unipolar-wound motor has two coils per winding. The stator flux is reversed by energizing one coil or the other. Because it uses only two transistors per winding, such a winding simplifies drive circuitry and eliminates the critical-timing problem during switching. However, because of the extra coils, the wire diameter must be smaller (for the same number of turns), which results in an increase in winding resistance. Thus, a unipolar motor typically has 30% less torque at low step rates. At high step rates, however, the torque output of bipolar and unipolar motors is nearly equal.

**Unipolar drivers are improved**

A recently introduced translator and driver circuit from Sprague Electric’s semiconductor group is specifically designed for 4-phase unipolar stepper motors. The UCN-5804B (Fig 4) combines low-power CMOS with high-current (1.25A) and high-voltage (35V) bipolar output stages. The CMOS logic section provides the sequencing logic, direction control, output-enable control, and power-on reset function. The UCN5804B sells for $2.65 (100) and comes in a 16-pin power DIP. It is a direct replacement for Sprague’s earlier FL versions, the UCN-4204B and the UCN-4205B-2.

Three user-selectable drive formats provide versatility. The 1-phase (wave-drive) mode energizes one phase at a time for reduced power consumption and greatest positional accuracy. The 2-phase mode energizes two adjacent phases simultaneously to provide the highest detent-torque and immunity to motor resonance. The half-step mode alternates between the 1- and 2-phase modes to provide an 8-step drive sequence.

**When it comes to speed control**

Whereas stepper motors have established a niche in position-control applications, brushless dc motors largely dominate speed-control applications, particularly in disk drives where reduced space mandates the smallest possible spindle motor. In its basic form, a motor-control IC must detect and decode rotor position, usually through Hall cells, and provide a correctly phased drive for the motor windings. It also has to have some means of regulating the motor drive to control the speed. Other important system functions include current sensing, overcurrent protection, and start/stop and forward/reverse operation.

To accomplish speed control in a brushless dc motor, the IC must control the current in the motor winding. You should be aware that achieving speed control by varying the dc voltage to the motor (chopping the dc supply) or by pulse-width modulation of the drive transistors can produce current spikes, which may cause noise problems in certain applications. In many of today’s compact disk-drive systems, for example, such current spikes can show up as additional bits of recorded information because of the magnetic disk’s proximity to the motor.

The LM621 from National Semiconductor performs the necessary phasing of the drive signals and supports 30° and 60° shaft-position sensor placement for 3-phase motors and 90° placement for 4-phase motors. It can directly drive the power-switching devices (either bi-
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polar or MOSFET) that drive the motor. In addition, the IC provides either bipolar drive to delta- or Y-wound motors or unipolar drive to center-tapped Y-wound motors.

To eliminate current spikes in the power-switching circuitry, the LM621 includes an adjustable dead-time circuit. The IC operates from a 5V supply, but its output circuit can accommodate voltage swings to 40V from the motor's supply source. It comes in an 18-pin DIP and costs $2.15 (1000).

Another circuit that provides control and drive for 3- and 4-phase brushless motors is the $4.90 (100) MC33034 from Motorola (Ref 1). The circuit provides a rotor-position decoder for commutation sequencing, a temperature-compensated reference that can supply power to the sensor, a frequency-programmable sawtooth oscillator, an accessible error amplifier, and a PWM comparator. It also has three open-collector top drivers and three high-current totem-pole bottom drivers, which are suitable for driving power MOSFETs.

Silicon Systems offers three single ICs for speed control of brushless dc motors for driving the spindle of Winchester-disk drives. The SSI-590 works with 2-phase motors, and the SSI-591 and SSI-593 are intended for 3-phase types; all three cost less than $3 each in production volumes.

The SSI-590 (Fig 5) provides all the timing and control functions necessary to start, drive, and brake a 2-phase, 4-pole, brushless dc spindle motor. The IC uses two external power transistors, three external resistors, and an external frequency reference. Optimized for a 3600-rpm disk-drive motor with a 2-MHz clock, it directly drives and decodes the Hall sensor in the motor.

Protection features of the SSI-590 include stuck-rotor shutdown, coil-overcurrent control, and supply-fault detection. The IC's linear control loop activates the power drivers using pulse-amplitude modulation.

A somewhat different control IC for 2-phase brushless dc motors is available from Unitrode. The UC3634 is a phase-locked frequency controller and provides precision control of the out-of-phase commutation signals required for driving 2-phase brushless motors (Fig 6). For a complete drive and control system, you need only add an external power-booster stage.

The two commutation outputs are open-collector devices that can sink more than 16 mA to the external booster. A disable-input pin allows you to force both of the commutation outputs to an active-low state. Double-edge logic, following the sense amplifier, doubles the reference frequency at the phase detector by responding to both edges of the input signal at the sense-ampli-
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fier input (pin 7). The UC3634 is housed in a 16-pin DIP and is priced at $2.10 (1000).

Integrated Power Semiconductors (IPS) uses linear-drive techniques with its motor-control ICs to reduce the probability of noise problems. Linear-drive techniques are compatible with either voltage- or current-mode control. Voltage-mode control uses the drive transistors as linear voltage regulators to vary the drive to the motor windings. Current-mode control uses the drive transistors as either linear current regulators or as variable current sources, which allows direct control of motor current. The IP3M05 uses the linear current-mode technique to control the motor current, and it works with 3-phase brushless motors.

Fig 7 shows one phase of the 3-phase output drive stage of the IP3M05. The current-source transistor (upper device) is fully on while linear operation of the sink transistor (lower device) controls the current to the motor windings. The output driver stage is rated at 15V and 2.5A continuous. A mask-programmable option with the output driver stage splits the collectors of the source transistors and the cathodes of the clamp diodes from the supply and brings these connections out to a separate pin for external control purposes.

The device offers other options as well, including an undervoltage lockout feature, open-collector or differential Hall sensor inputs, and stop/start and power-up/down sequences. A variety of power packages are also available. Because many of the IC's functions are optionally metal-mask programmable during fabrication, the IP3M05 provides a great deal of flexibility in adapting to different system-control methods. But, because of its mask-programmable nature, the IC must be customized according to customer requirements, and IPS only considers large volume orders. In quantities of 50,000, a unit cost of under $5 is typical.

This article covers only a small sample of some of the more significant types of motor-control circuits; you have a wide variety from which to choose. Most of the manufacturers whose products are discussed here also offer many other types of motor-control or driver circuits. Many of these vendors can also provide custom designs for applications where size, performance, and economic constraints are paramount.

Reference

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517

For more information . . .

For more information on the motor-control ICs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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<td>2000 S County Trail East Greenwich, RI 02818</td>
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<td>Integrated Power Semiconductors</td>
<td>2727 Walsh Ave, Suite 201 Santa Clara, CA 95051</td>
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<td>Motorola Semiconductor Products</td>
<td>3010 N 50th St Phoenix, AZ 85018</td>
<td>703</td>
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<td>National Semiconductor</td>
<td>Box 5869 Santa Clara, CA 95052</td>
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<td>14551 Myford Rd Tustin, CA 92680</td>
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<td>1310 Electronics Dr Carrollton, TX 75006</td>
<td>710</td>
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Silicon microstructures let manufacturers implement a variety of sensors on chip

J D Mosley, Regional Editor

Silicon, an element synonymous with low-cost digital electronics, is now the basis for inexpensive, IC-size analog sensors. Manufacturers have been selling silicon pressure sensors since 1985, but in the past six months they’ve branched out to offer other kinds of sensors that are chemically etched from a silicon substrate. By taking advantage of techniques developed and refined by semiconductor makers over the past two decades, manufacturers of a variety of sensors—such as chemical-sensitive devices, airflow sensors, and thermometers—are mass-producing silicon microstructures that mimic the functions of conventional sensors, yet are inexpensive to the point of being disposable. The bargain-basement pricing of these sensors will let you incorporate sensing capabilities in applications that previously wouldn’t have justified the added expense.

To the companies that are pioneering the development of these solid-state sensors, silicon micromachining is an art. Although silicon can easily be chemically sculpted with standard semiconductor processes to create cavities, walls, diaphragms, beams, and cantilevers—it is the degree to which a manufacturer can refine the etching technique that dictates how sensitive and accurate the devices can be, how many functions they can perform, and how many different types of sensors manufacturers can create with the silicon.

Manufacturers use additive processes such as epitaxial growth, doping, thin-film deposition, lamination, and thermal bonding to build up the surface of the silicon wafer, forming islands and additional layers where needed. Mechanical grinding, laser cutting, and ultrasonic drilling provide additional methods for creating unique shapes. Two types of chemical etchants— isotropic and anisotropic—cut gently rounded or sharply defined shapes into a silicon crystal (see box, “Fabricating silicon microstructures”).

In addition, silicon is a brittle substance: Located directly below carbon in the periodic table, silicon forms a crystalline structure similar to a diamond’s. The crystalline orientation is a significant consideration in micromachining, because etchants attack the planes within the crystal at different rates. So, just as a diamond cutter must combine technique with a knowledge of crystals to create the desired facets without pummeling the stone into dust, a silicon micromachinist must consider a variety of planar orientations and multiple processes to create a sensor composed of fragile structures ¼ the thickness of a human hair.

Fortunately, silicon is highly resistant to mechanical stress. It exhibits the strength of steel, but presents a higher elastic limit when under compression and tension, and it exhibits no weakening or hysteresis under repeated applications of tension and compression. Manufacturers can create an array of sensors in a single device to give the unit more functions. And because microsensors are carved from silicon, it’s a relatively simple matter to add on-chip microprocessors and electronic capabilities for intelligent measurement and control. After all, micromachining and semiconductor fabrication both expose silicon wa-
Fabricating silicon microstructures

To fabricate silicon microstructures, manufacturers combine standard IC-processing steps with chemical etching procedures to form micromechanical structures. The following list shows the preliminary steps manufacturers take to produce an IC-size silicon sensor.

Starting material

As in IC processing, the starting material for a silicon sensor is a silicon wafer. For micromechanical devices, the wafer is typically thinner than that used for standard ICs and is polished on both sides.

Oxidation and photolithography

The oxidation, photolithography, and oxide-etching processes for silicon micromechanical devices are similar to those of standard IC processing. For microstructures, manufacturers often perform these procedures on both sides of the wafer, and they pattern such alternate thin-film materials as nitrides and metals to form conductors or other physical features. The figure below shows a cross-section of a single chip on a silicon wafer.

Etching

Etching, or removing silicon chemically, is a key process in fabricating a micromechanical device. In addition to etching the wafer from both sides, manufacturers often use multiple etch steps to realize complex geometries. Single-side undercut etching, for instance, results in suspended microbeam and diving-board-like structures (a, below). Isotropic etchants produce a gently rounded hole (b). Using anisotropic etchants along various planar orientations.

Diffusion, epitaxy, and ion implantation

In a conventional IC, dopant regions are defined solely by their electrical characteristics. In microstructures, these regions also provide etch stops (see below). In many etch processes, the etching halts at the P-N junction: This procedure controls dimensions very accurately. The dopant regions are also useful for incorporating circuits on the same mechanical structure and for realizing piezoresistive sensing elements.

One of the original developers of silicon-sensor technology, IC Sensors, has introduced an accelerometer, a device that monitors acceleration, vibration, and shock. By focusing on low cost, small size, and light weight when designing the Model 3021, the company produced a solid-state 7.9×7.3-mm IC that weighs a fraction of a gram and offers a tenfold price reduction in comparison with a corresponding hand-assembled accelerometer. The IC currently comes mounted in a 1.5-cm² ceramic package; by December you'll be able to order the unmounted IC. Its unique 3-layer silicon structure lets the device act as its own housing. To mount the IC you just glue it down.

The 3021 operates over the range from ±5 to ±100G with a 20× over-range. It requires a supply of 5V or 1.5 mA and achieves full-scale sensitivities in excess of 50 mV. The sensor has built-in overforce stops and a damping factor of 0.707 to provide critical damping. And unlike piezoelectric devices, the bridge in the 3021 provides true dc response. Prices start at $87 each in sample quantities; the company expects to sell the parts for less than $10 in large quantities.

Sensors monitor to 300°C

The KTY line of silicon temperature sensors from Amperex includes models that can monitor heat ranging from 0 to 300°C, −55 to 175°C, and −55 to 150°C. Taking advantage of silicon's nearly linear temperature-dependent resistivity, these KTY sensors respond in as little as one second. They are accurate to within 0.7%/°C. You can order the...
TECHNOLOGY UPDATE

Totions of the crystalline silicon structure produces either a pyramidal hole (c) or perpendicular walls (d).

(a)

(b)

(c)

(d)

Lamination
Manufacturers often laminate together multiple micromechanical wafers of silicon or glass to form complex mechanical parts (below). These caps are attached at the wafer level before sawing. They provide protection for small internal moving parts, as well as mechanical stops and additional surfaces for etched features.

(The information on microstructure processing technologies was provided courtesy of IC Sensors.)

KTY sensor with standard tolerances of ±1%, ±2%, and ±5%.

The KTY sensor itself is a relatively simple device consisting of two resistive silicon devices of opposing polarity, sandwiched between a metalized bottom plane and a phosphor-glass passivating layer. Gold contacts conduct heat to the silicon devices. The 175°C and 300°C models use a single resistor and don't allow bipolar operation. Instead, when you positively bias the gold contact, you deplete the hole concentration in the upper N+ diffusion layer to boost the temperature response beyond the device's normal 150°C limit. Pricing for the KTY series ranges from $0.45 to $0.95 (10,000).

Another Amperex microsensor is the KMZ10 line of magnetoresistive devices, which detect variations in magnetic fields. The sensing material is a polycrystalline ferromagnetic alloy called "permalloy." The KMZ10 chip uses four permalloy strips arranged to form the four arms of a Wheatstone bridge. Gold stripes, laid down at 45° slopes on the permalloy surface in barber-pole fashion, rotate current through the device. This arrangement serves to maintain a linear magnetic field for increased device sensitivity. Capable of sensing both linear- and angular-displacement magnetic-field ranges of ±0.5, ±2.0, and ±7.5 kA/m, these components range in price from $1.25 to $1.75 (10,000).

Mass airflow sensors
The latest silicon microsensor from Honeywell's Micro Switch Div

EDN November 26, 1987
This die shot of a mass-airflow sensor exemplifies the intricate structures that silicon micromachining can produce. By applying semiconductor mass-production techniques to these micromechanical devices, Honeywell's Micro Switch Div can sell this device at a fraction of the cost of a conventional, handmade sensor.

is a mass-airflow sensor that uses a thin-film, thermally isolated bridge structure. Dual sensing elements flank a central heating element in the bridge and measure the thermal transfer that occurs when air flows across the surface of the sensing elements. The unit specs a response time of under 5 msec for airflow ranging from 0 to 200 standard cubic centimeters per minute (scm). Laser-trimmed resistors give the devices consistent sensitivity. The parts start at $26.50 (5000).

Other devices in the Micro Switch line of solid-state sensors include a series of miniature digital current sensors that operate with a 4.5 to 24V dc power supply and provide an open-collector output that changes—within 60 µsec—from the supply voltage to 0.4V when the sensed current exceeds a predetermined operating level. The sensors cost $11.30 (5000).

The MPX2000 sensors can detect pressure over the 0 to 30 psi range, and their full-scale output spans 0 to 40 mV. The company also offers the MPX3100, which uses on-chip voltage-amplification techniques to produce a 2.5V output from a 5V supply. This part, however, is expensive—it costs $75. Company representatives refer to it as a learning tool in their quest for a sensor with a 5V output.

Another company, NovaSensor, produces a pressure transducer that the company claims is the world's smallest. Housed in a package that's nearly identical to a standard 6-pin miniature DIP, the sensor can be mounted on a pc board with either through-hole or surface-mount assembly techniques. Two pressure ports accommodate standard ⅛-in. ID plastic tubing. You can choose from four versions ranging from 0 to 5 psi to 0 to 100 psi. The devices cost as little as $3 each (OEM qty).

ASIC sensors pave the way

Besides offering a variety of off-the-shelf silicon sensors, microsensor manufacturers can fabricate sensors to your specifications. If you have a unique kind of sensor in mind, and need at least 10,000 of them, you can have NovaSensor's engineers provide computer-generated designs for the parts that are based on a library of silicon mechanical structures. For example, within eight to 16 weeks, the company can deliver a custom-designed piezoresistive pressure sensor, with laser-trimmed resistors, that's accurate to ±0.1% of full-scale output. The company offers such devices in chip form, thus permitting you to develop your own application-specific packaging. The firm also offers such support services as an in-house prototype machine shop, an engineering-design facility, automated test and assembly, and quality-assurance programs designed to meet military requirements.

Devices tell chemicals apart

One of the most exotic types of microsensor available today is the silicon chemical sensor, a device that is sensitive to specific ions, gases, enzymes, or proteins. Incorporating a chemical microsensor in your circuit lets you differentiate among chemicals for such applications as hazardous-material warning systems and biomedical monitors.
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<td>Analog QuickChip family:</td>
</tr>
<tr>
<td>□ 150—524 NPN Transistors</td>
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<tr>
<td>□ $f_T$ typical to 6.5 GHz at 15V or 2.5 GHz at 65V.</td>
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<tr>
<td>Analog/Digital QuickChips:</td>
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<tr>
<td>□ Gate propagation delay: 400 ps</td>
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<td>□ Digital function library</td>
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By exposing the bare silicon-based gate insulator of a metal-insulator FET and adding a reference electrode, Chemfet Corp developed a sensor that can detect and differentiate among chemicals.

To aid in such tasks, Chemfet Corp manufactures chemically sensitive field-effect transistors (chemFETs). These devices are basically MOSFETs that the company renders ion sensitive by removing the metal-gate electrode to expose the silicon-based gate insulator. An external reference electrode functions as the device's gate terminal, as Fig 1 illustrates. By varying the chemical composition of the gate insulator, the company can alter the electrochemical potential of the surface field effect that occurs when the test solution contacts the gate insulator.

These devices differentiate among chemicals, as chemFETs do, but Molecular Devices claims they're more useful than chemFETs in biochemical applications. The firm explains that the exposed silicon-gate insulator of a chemFET corrodes and becomes unstable after repeated exposure to sodium ions. Water with dissolved salts is the basis of all biochemical reactions.

Molecular Devices makes these sensors by sealing a standard silicon wafer with a proprietary, monolithic insulating layer. The insulated silicon surface and an electrolytic test solution act as a capacitor. The manufacturer attaches a lead from the back of the silicon to a reference electrode that touches the test solution. Along the lead is an ammeter and a potentiometer, and across the back of the silicon is an array of LEDs. Each LED provides a discrete test site for measuring multiple substances in a single sample.

When one of the LEDs turns on, a photoresponse occurs in the silicon and a transient current flows in the lead. Modulating the light from the LEDs at high frequencies generates a majority-logic signal-processing technique to take an average pH reading from the 10 channels and to identify any deviant readings from individual channels.

A 10-oz handheld Model 100 pH/mV/temperature meter costs $595. The desktop Model 200 sells for $895. Sensor probes for both models cost $225.

For more information on the silicon microsensors discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

- Amperex Electronic Corp
  George Washington Hwy
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  TWX 710-381-8808
  Circle No 712

- Chemfet Corp
  777 108th Ave NE
  Suite 1200
  Bellevue, WA 98004
  (206) 462-1001
  Circle No 713

- Honeywell
  Micro Switch Div
  11 W Spring St
  Freeport, IL 61032
  (815) 235-5731
  Circle No 714

- IC Sensors Inc
  1701 McCarthy Blvd
  Milpitas, CA 95035
  (408) 435-1800
  TLX 350066
  Circle No 715

- Molecular Devices Corp
  3180 Porter Dr
  Palo Alto, CA 94304
  (415) 493-0166
  Circle No 716

- Motorola Inc
  Box 52073
  3102 N 56th St
  Phoenix, AZ 85072
  (602) 244-4566
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an alternating current in the lead as the ammeter indicates. A chemical reaction on the sensor changes its surface potential, creating a field effect that results in a measurable current. The biosensor, therefore, acts as a transducer, translating a chemical reaction into an electronic signal.

The company claims to have probed test sites as small as the diameter of a single red blood cell. Each test site occupies only one or two square millimeters of the sensor's surface. Within 10 minutes, a biosensor can detect low-concentration substances in blood, even when the concentration is as small as one part per 50 billion.

At least one company, Honeywell Inc, has announced its intention to add artificial intelligence (AI) to sensors that detect temperature, light, position, and magnetic change. This combination could give machines the ability to evaluate such intangible characteristics as flavor, odor, and softness. Of course, to perform such evaluations, you'd have to do extensive data analysis to determine specific criteria for the test parameters. Once you'd defined the precise combination of chemical attributes, however, you'd be able to automate control over even the subjective qualities found in a given product. Ultimately, the advent of such subjective sensing devices depends on continuing refinements in both AI and sensor technology.

References


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Synchronized 5\(\frac{1}{4}\)-in. Winchester drives operate in parallel and store 1.5G bytes

An industry first, the Parallel Disk 1800 family of drive subsystems uses multiple 5\(\frac{1}{4}\)-in. Winchester drives to emulate the operation of a single larger-capacity drive. The first available member of the family, Model 1804, stores 1.5G bytes of data (unformatted capacity) on five 380M-byte drives. The drive subsystem includes a power supply and a SCSI (Small Computer System Interface) controller. Its cost per megabyte and performance specifications make it comparable to 8-, 9-, and 14-in. disk drives.

Earlier 5\(\frac{1}{4}\)-in. drives weren't fast enough or reliable enough to replace larger drives. Newer 5\(\frac{1}{4}\)-in. Winchester drives such as those in the 1804, however, feature seek times equal to those of larger drives. The 1804 drive subsystem and drives, for example, feature a typical seek time of 16.5 msec. Manufacturers of newer 5\(\frac{1}{4}\)-in. drives have also steadily improved the products' reliability (their MTBF spec is typically 30,000 hours) and have lowered the drives' cost per megabyte.

Drives use SCSI controller

Mainstream drives larger than the 5\(\frac{1}{4}\)-in. form factor use the SMD (Storage Module Device) interface and transfer data at a maximum of 3M bytes/sec. Drives that transfer data faster than 3M bytes/sec use the IPI (Intelligent Peripheral Interface) or a proprietary interface. The Model 1804 drive, however, uses a synchronous-SCSI controller to achieve a transfer rate of 4M bytes/sec. The individual 5\(\frac{1}{4}\)-in. drives operate with 10-MHz read channels. Four of the drives store data, and the remaining drive stores parity information. Together, therefore, the drives have a raw data rate of 5M bytes/sec (4 drives\(\times\)10M bps).

When writing or reading data, the drive subsystem's master controller stores or retrieves one of four consecutive bytes of data on each of the four data drives. Automatically, the controller uses the fifth drive to generate or check parity. Motor-control circuits synchronize the drives' spindle motors and therefore closely match the drives' data rates. A local buffer on each drive ensures byte-wide data synchronization.

The Model 1804 also matches or exceeds SMD drives in the areas of data integrity and reliability. Error correction code (ECC) circuitry detects read errors on each individual drive. The master controller uses the parity drive to correct the errors on the fly. An error does not require immediate retries, therefore, and the data transfer occurs with no delay. The master controller handles retries and manages hard and soft errors during periods of inactivity in the drive. The ECC and parity-drive combination reduces the chance of reading corrupted data to virtually zero.

The vendor specifies the drive subsystem's MTBF as 65,000 hours. Note, however, that this spec doesn't have the same meaning as a 65,000-hour MTBF spec for a single drive. Manufacturers typically spec an SMD drive's MTBF at 50,000 hours or more, and the spec takes into consideration a single drive module and sometimes a power supply and controller. MTBF is typically calculated by adding together the reciprocals of each individual component's MTBF; the result is the reciprocal of the system MTBF.

To calculate MTBF for the 1804, however, you must consider five drive modules (each having a 30,000-hour MTBF), a master controller, and a power supply. Further, because the 1804 includes a parity drive, it can read correct data.
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when any one drive is not operating. Therefore, subsystem failures occur only when the power supply or master controller fails, or when two drive modules fail. When you consider the 1804's 5-drive matrix, then, you obtain a 65,000-hour MTBF.

When one of the 1804's drive modules fails, you can replace it without taking the subsystem out of use. In fact, nontechnical office personnel can make the change. The master controller regenerates the correct data on the new drive module. The regeneration requires 30 minutes on an unloaded system, or as much as three hours when performed in conjunction with heavy subsystem operation.

Subsystem emulates one drive
The drive subsystem operates in the same way that a single 5¼-in. drive with a SCSI controller does. If you have a SCSI software driver that handles any of the vendor's SCSI drives, you can plug the 1804 into your system; in this case, you also get the benefit of field-replaceable modules and improved reliability. In fact, when used with a redundant power supply, the product may have applications in fault-tolerant systems.

The subsystem is 7 in. high, 17¾ in. wide, and 22 in. deep, and it mounts in a standard 19-in. rack. Evaluation units will be available in the first quarter of 1988. The subsystem costs $8/megabyte (1000). You can expect the company to offer several more products that use the multiple-drive approach. For example, the vendor plans to replace the 380M-byte drives with 760M-byte models, yielding a 3G-byte subsystem in the same package. The company will also offer products with faster raw data rates (using 15M-bps drives) and faster interfaces (IPI or SCSI 2).—Maury Wright

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Of all the new products covered in EDN's September 17, 1987, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our September 17, 1987, issue.

**A PROTOCOLIC**
The AIC-6250 SCSI protocol IC targets high-performance applications by combining 5M-byte/sec synchronous SCSI transfers with 20M-byte/sec host transfers (pg 112).
Adaptec Inc.
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**IBM PC SCOPE**
The R2000 2-channel, 20M-sample/sec digital oscilloscope uses an IBM PC for display and storage (pg 314).
Rapid Systems Inc.
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**VOICE RECOGNITION**
The IntroVoice VI is an add-in board for the IBM PC/XT, PC/AT, and compatibles that combines voice recognition of 400 words with unlimited text-to-speech synthesis (pg 295).
The Voice Connection.
Circle No 602

**LOGIC-DESIGN TOOL**
The Scratchpad software package combines a schematic-capture editor and an interactive logic simulator (pg 304).
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The Model 410 is a general-purpose piezoresistive pressure sensor that is housed in a DIP for mounting on a pc board (pg 278).
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EDN November 26, 1987

CIRCLE NO 86
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ZIF and LIF PGA sockets, plus our minimal profile spring sockets in PGA footprint.

AMP is a trademark of AMP Incorporated.
AMP makes sure you have the socketing options you need to make it pay off.

Our high pressure tin sockets for plastic leaded packages come with an exclusive Positive Lock retention system that keeps chips secure during handling and shipping. Ceramic chip carrier sockets feature duplex plated contacts and snap-on covers that accommodate heat sinks. Both are available in standard and surface-mount versions.

AMP offers you more: high-speed, surface-mount sockets on .020" centers. Gold-plated plastic carriers and sockets. For pin grid arrays, sockets in ZIF and LIF styles, plus custom VHSIC capability.

Choose your technology. AMP makes it easy to implement, with full socketing support.

Call 1-800-522-6752 for more information on AMP sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

Low-height sockets in all standard sizes (JEDEC A, B, D), with duplex-plated contacts for sure performance. High-speed, surface-mount sockets feature 0.5pF, 1.4nH contact characteristics.
LEADTIME INDEX
Percentage of respondents

ITEM

ITEM

TRANSFORMERS
Toroidal
Pot-Core
Laminate (power)

RELAYS
0
0
0

12
14

63
43

12
29

13
14

0
0

10.5
12.0

8.6
9.7

27

47

26

0

0

8.7

9.2

CONNECTORS
0
19
20

0

100

0

25
20

50
40

6
20

0
20

40
54

50
13

10
13

Socket
Terminal blocks

27
11

50
61
62

18
22
31

5
6

50
33
12

38
34
75

6
33
13

47

41
60

6
8

D-Subminiature
Rack & panel
Power

0
6
0
0

7

6
4

Multi-layer

0

28
18

0

77

65
23

17

Prototype

22
13

0

50

45

31
32

7
12

32
43

9
7

44

Metal film
Metal oxide

27
7

32
43

0

Wirewound

19

25

25

25

Potentiometers

13

33

37

17

7.5

Diode

30

17

27

23

3

0

7.1

4.8

31
25

19
50

4

0
0

7.1
10.5

5.4
8.0

6.8

5.8

0
0
0
0
0
0
0

4.7
3.7

5.6
4.1

23
0
20
13

23
25

0

Zener
Thyristor
Small signal transistor

20
31

15
25

45
31

0
0

8.8
7.8

7.5
7.9

0

40

20

40

0

9.0

8.4

4.5
5.5

4.3
7.0

5.5

6.4

8.8
8.3

8.9
5.7

0
0
0
0

0
0

9.5
7.5

8.4
6.4

0
0

6.7
7.0

6.0
6.1

0
0
0
0

0
0
0
0

5.6

5.3

6.9

7.0

8.2

9.3
4.1

0
0
0

8.0

8.4
4.2

0
0
0

6.8
5.9

7.9
5.8

0
0
0
0
6
0
0

0
0
0
0
0
0
0

4.1
4.8

3.7
3.3

0
7
0

7.7
8.6
10.3

7.7
7.1
8.7

0
0

14.1 10.0
8.6
7.1

MOSFET
Power, bipolar

0
0
0
0

INTEGRATED CIRCUITS, DIGITAL
Advanced CMOS
CMOS

10
13

15
23

35
41

40
23

TIL
LS

12
19

44
33

19
19

25
29

INTEGRATED CIRCUITS, LINEAR
Communication/Circuit
OP amplifier
Voltage regulator

9

27

35

27

14

33

33

12

41

35

20
12

18

29

35

18

4.9

4.1

5.8
8.2

6.0
7.2

6.6
6.4

4.5
6.3
4.2

RAM 16k
RAM 64k

10
13

20
27
34

50
33
25

20
20
33

0
0

RAM 256k
RAM 1M-bit

9

27

46

18

27
33

33
13

33
40

0
7

0

10.0

7.7

0

0

8.8

0

9.1
10.8

0
0

8.8
9.1

8.5
8.0

6.6

9.9

0
0
7

ROM/PROM
EPROM 64k
EPROM 256k

25
11

31
44

38
45

33

34

11

11

44

33
34

0
0
0

Panel meters
Fluorescent

25
0

25

25

25

0

0

14

57

Incandescent
LED

0
27

33
27

11 .6 12.5
8.8 8.6
6.0 7.5

0

0

0
0
0
12

0
0
0

Liquid crystal

29
34
27
50

0

13.0

9.7

8-bit

6
8
0

22
23

39
46

33
23

0

16-bit
32-bit

0

0
0

8.9
8.0

6.8
8.3

15

23

54

8

0

10

20

30

40

0

0

9.2

9.4

O

37

27

36

0

O

45

22

33

0

0
0

8.9
8.3

9.3
8.6

43

29

14

14

0

9.4

7.9

29
35

38
15

8

35

15

6.8
7.0

4.7
5.0

19
19

27
19

0
0
0
0
0

4.8

20

4
4
5
4
4

6.2

23

7.5

5.5

6.7

5.6

34

8

0

8

8.0

6.3

EPROM 1M-bit
EEPROM 16k
EEPROM 64k

0

2.6

20
5

35
48

40
42

5
5

0
0

0

5.0

6.4

7
12

50
29

36
41

7
18

0
0

5.6
5.5

6.2
6.4

Thumbwheel
Snap action
Momentary
Dual in-line

18
13
0

27
40
33

37
40
50

18
7
17

0
0
0

0
0
0
0
0
0

6.9
6.5

9.3
7.0

5.4
7.6

7.1
6.9

Coaxial
Flat ribbon

17

44

28

11

0

11

56

33

0

0

0
0

5.3
4.3

4.3
5.1

Multiconductor

13
30

47
44

33
22

7
4

0
0

5.1

6.2

FUNCTION PACKAGES

54

23

8

0

3.7
4.7

2.8
2.3

Amplifier

15
33

29

29

9

0

0
0
0
0

4.5

6.0

0
0

0
39

55
22

36
39

9
0

0
0

12.3
9.0

6.2
6.7

Ceramic monolithic

21

29

14

36

14

7

0

7.3

5.6

Ceramic disc
Film

23
25

19

33

43

5

0

0

5.2

4.8

Aluminum electrolytic

23

Tantalum

19

27
39

0

50

SWITCHES

WIRE AND CABLE

8

7
6
0
0

0

8.3

DISPLAYS

33
19

38

MICROPROCESSOR ICs

Converter, analog to digital
Converter, digital to analog

12.6 12.5

LINE FILTERS

POWER SUPPLIES

CIRCUIT BREAKERS
HEAT SINKS
RELAYS
PC board

7.0

5.0
6.6

9

General purpose

0

9.9

5

Switcher
Linear

8.0
7.5

8.0

27

Power cords

6.8
9.2

5.7
6.9

59

Hookup
Wire wrap

0
0

0
0

FUSES

Rotary
Rocker

20

0
0
0

MEMORY CIRCUITS
17
12

Pushbutton

11
37

56
37
30

0

RESISTORS
Carbon film
Carbon composition

Networks

13

0
0
0
0
0
0
0
0
0
0
0

PRINTED CIRCUIT BOARDS
Single-sided
Double-sided

11

Mercury
Solid state

DISCRETE SEMICONDUCTORS

Military panel
Flat/Cable
Multi-pin circular
PC (2-piece)
RF/Coaxial

Edge card

Dry reed

9
6

48
30

38
30

5
34

0
0

0
0

5.2
8.7

4.4
7.7

CAPACITORS

INDUCTORS
Source : Electronics Purchasing magazine's survey of buyers

96

EDN November 26, 1987


JUST BECAUSE YOU'VE MADE IT...
...DOESN'T MEAN YOU'VE GOT IT MADE.

With a lot of ASIC vendors, your first prototype is just the beginning of a long journey into design revisions. And after the arduous task of making the thing work, you're still not sure the device can be mass produced.

Unless you're working with Fujitsu.

Because when we produce your prototypes, you can bet they'll meet your performance specs. And you can be absolutely certain you'll be able to produce the device in quantity. And on schedule.

Here's why. We've taken over 8,000 designs from concept through mass-production. And over 99% of them have worked the first time. That's right. Prototype number one worked as specified.
You see, we've been refining our design tools for the past fifteen years. And because they verify your input to worst case specs, as well as scrutinize every detail from spike analysis to bus contention, all the guesswork is eliminated. Our simulations are closely correlated to silicon (with a 99% hit rate). Plus, all prototypes and wafers are tested exactly like production units. So you know what you'll get. Before you get it.

**Mass production. Guaranteed.**

Once you've accepted a prototype from Fujitsu, you can put all your production worries aside. Our design system drives devices to match the production process. That's guaranteed by 100% AC testing at frequency, in addition to the standard DC and functional testing. What's more, all wafer fabrication, assembly and testing are done in-house. All this means that you can count on production units that work uniformly.

Combine these failsafe methodologies with our unprecedented quality assurance record, and you've got mass production with the highest quality available. Anywhere.

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Finally, consider our experience. We can deliver the precise technology you need to fit your application. Leading edge technology from CMOS to ECL. With more packaging options than you can imagine.

So don't listen to promises. The proof is in our performance. Simulations that match silicon 99.9% of the time. Prototypes that perform to spec the first time. And devices that work uniformly when they're mass produced.

Call our Custom Products Group today at (800) 556-1234, ext. 82; in California (800) 441-2345. Because when your devices are made by Fujitsu, you've really got it made.
Competition is strong in the high-stakes µP/µC game. Manufacturers are competing to produce CISC and RISC chips that run Unix as efficiently as possible. Each new high-performance device knocks previous chips out of the game. (Photo courtesy Intergraph Corp)
Choosing the μP is no longer the most important decision an OEM must make in designing a μP-based system. VLSI progress and software momentum have relegated the μP to the role of a team player.

Robert H Cushman, Special Features Editor

When EDN’s first annual μP/μC chip directory was published 14 years ago, the microprocessor was the star. The selection of a μP was often the sole starting point of a design. Memory and I/O were things to be tacked on as the need arose. Software was necessary merely to flesh out the application. As you can see from this year’s directory, however, the μP is now just another component. To be successful, it had better be a good team player.

Low-end μPs shouldn’t hog silicon

At the low end of the μP scale (the entries at the beginning of the directory), it’s just as important for a μP to be small in silicon area as it is for the chip to offer good performance. One of the designers of National Semiconductor’s COP800 says that given the limited size of any practical and economical 1-chip (300×300-mil) μC, OEMs could get more end-product appeal per dollar from a small, simple (60×60-mil) μP than they could from a more-complex μP. A small μP leaves more room for subsystems—ROM, RAM, EEPROM memories, serial I/O ports, timers, liquid-crystal-display (LCD) drivers, A/D converters, and so on. The same situation exists for ASIC design, in which small μP cores are perhaps even more desirable, because some of the subsystems are made with less-compact gate arrays.

At the high end (the chips listed toward the end of the directory), you can see that whatever else a μP does, it’s now absolutely vital for the chip to run the application software well. At the high end, software has become the star.

It’s patently obvious that software is king in the IBM PC domain. Industry analysts generally agree that the 80386 is headed for the same dominant share of the 32-bit world that the 80286 now enjoys in the 16-bit world. In a sense, the μP-selection process for the PC world has been taken over by end users and third-party software houses.

Some third-party specialists are currently trying to break the monopoly of the 8086/286/386 family. Phoenix Technologies (Norwood, MA), and Insignia (London, UK, but the company has an answering service in San Francisco, CA) offer 8086-family software emulators for other μPs, such as Motorola’s 68000 and National’s 32000 families. The emulators allow these non-8086-family μPs to run MS-DOS programs, though they do exact a speed penalty. Hunter Systems (Mountain View, CA) is working on a binary translation program that will convert MS-DOS programs to 68020/30 and Clipper binary code, a technique that’s expected to allow those μPs to run the software faster.

But so far no one has suggested that any of these software programs will allow other μPs to displace the 8086/286/386 μPs in the mainstream IBM PC markets. They will, however, allow systems using the Motorola and National μPs to share in the $10 billion worth of software available for 8086-based systems. For example, they will allow a 68020/30-based Unix workstation to run dBASE or a 32532-based, real-time factory controller to apply Lotus 1-2-3 after hours for performance analysis.
For systems that run Unix—both reprogrammable and embedded (dedicated) systems—the µP’s task is to be a “good Unix engine.” Among other things, this task requires that the µP architecture mate well with an accompanying optimizing C compiler. The Motorola 68020 has the lead in this area, and presumably the 68030 will help Motorola retain that lead. But the Unix market is an open field; Motorola’s 68000 family now has

### Manufacturers of µP/µC chips

For more information on µP/µC chips as those included in this directory, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. The abbreviations in parentheses after some companies are those used in the directory. Information about recent mergers and acquisitions also appears in parentheses.

<table>
<thead>
<tr>
<th>Company Name</th>
<th>Address</th>
<th>Phone Number</th>
<th>Circle No</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Micro. Devices (AMD)</td>
<td>901 Thomson Pl</td>
<td>(408) 732-2400</td>
<td>643</td>
</tr>
<tr>
<td>Analog Devices Inc</td>
<td>Digital Signal Processing Div</td>
<td></td>
<td>641</td>
</tr>
<tr>
<td>AT&amp;T Technologies Inc</td>
<td>Dept LT</td>
<td></td>
<td>615</td>
</tr>
<tr>
<td>Bipolar Integrated Technology (BIT)</td>
<td>Box 4740</td>
<td></td>
<td>616</td>
</tr>
<tr>
<td>California Micro Devices</td>
<td>2000 W 14th St</td>
<td></td>
<td>617</td>
</tr>
<tr>
<td>Calamos Semiconductor</td>
<td>20 Edgewater St</td>
<td></td>
<td>618</td>
</tr>
<tr>
<td>Cypress Semiconductor</td>
<td>3001 N First St</td>
<td></td>
<td>619</td>
</tr>
<tr>
<td>Fujitsu Microelectronics Inc</td>
<td>3220 Scott Blvd</td>
<td></td>
<td>620</td>
</tr>
<tr>
<td>General Instrument Corp (GI)</td>
<td>Microelectronics Div</td>
<td></td>
<td>621</td>
</tr>
<tr>
<td>Gould Semiconductor (AM1)</td>
<td>3000 Homestead Rd</td>
<td></td>
<td>622</td>
</tr>
<tr>
<td>Harris Semiconductor Products Div</td>
<td>2401 Palm Bay Rd</td>
<td></td>
<td>623</td>
</tr>
<tr>
<td>Hitachi America Ltd</td>
<td>2210 One plate Ave</td>
<td></td>
<td>624</td>
</tr>
<tr>
<td>Hitachi Ltd</td>
<td>Semiconductor &amp; Integrated Circuits Div</td>
<td></td>
<td>625</td>
</tr>
<tr>
<td>Inmos Corp</td>
<td>Box 10600</td>
<td></td>
<td>626</td>
</tr>
<tr>
<td>Inmos Ltd</td>
<td>1000 Aztec W</td>
<td></td>
<td>627</td>
</tr>
<tr>
<td>Integrated Device Technology (IDT)</td>
<td>3220 Scott Blvd</td>
<td></td>
<td>628</td>
</tr>
<tr>
<td>Intel Corp</td>
<td>3065 Bowers Ave</td>
<td></td>
<td>629</td>
</tr>
<tr>
<td>Intergraph Corp</td>
<td>Advanced Processor Div</td>
<td></td>
<td>630</td>
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<tr>
<td>Intermetall GmbH (ITT)</td>
<td>Box 840</td>
<td></td>
<td>631</td>
</tr>
<tr>
<td>LSI Logic Corp</td>
<td>1531 McCarthy Blvd</td>
<td></td>
<td>632</td>
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<tr>
<td>Mitsubishi Electronics America Inc</td>
<td>1050 Arques Ave</td>
<td></td>
<td>633</td>
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<tr>
<td>National Semiconductor Corp</td>
<td>2900 Semiconductor Dr</td>
<td></td>
<td>634</td>
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<tr>
<td>Motorola Integrated Circuits Div</td>
<td>3501 Ed Bluestein Blvd</td>
<td></td>
<td>635</td>
</tr>
<tr>
<td>Motorola Microprocessor Products Group</td>
<td>6501 William Cannon Dr W</td>
<td></td>
<td>636</td>
</tr>
<tr>
<td>National Semiconductor Corp</td>
<td>2900 Semiconductor Dr</td>
<td></td>
<td>637</td>
</tr>
</tbody>
</table>
many competitors—including even the 80386.

Other CISC-type (complex-instruction-set computer) 32-bit µPs exist: the AT&T WE32, the Zilog Z80000, and the National 32532. Each of these has its strong points. For example, National offers a 32532-based microcomputer board (the VME532) running at 20 MHz that delivers 10.9k Dhrystones; the company claims it will deliver 16.3k Dhrystones when it runs at 30 MHz.
That benchmark compares favorably with those published for the 80386 and 68030. There are also new RISC (reduced-instruction-set computer) µP chips: the Clipper, which has changed ownership recently but now may have found an appropriate home with workstation maker Intergraph; the SPARC chip, which is the basis of Sun’s open hardware/software SPARC system; and AMD’s 29000. The latter two are new additions to the directory this year.

Manufacturers are racing to make their CISC and RISC µPs chips suitable for use in Unix systems, but the CISC and RISC µPs are just part of that competition: The real race may be between their C-language compilers. These days, it’s the efficiency of the compiler that really determines how well a µP will be able to run Unix. Besides, the hardware benchmarks that count most may not be the speed at which the µPs can run standard test programs, but the amount of access time the µPs allow memories, the speed with which the µPs respond to interrupts, and the time the µPs take to perform context switches. To be successful, a Unix µP must also satisfy requirements at the operating-system level. An important benchmark, for instance, will be the µP’s ability to handle Unix multiprocessing and dual-mode operating systems (for instance, when Unix is combined with a real-time executive).

Requirements overlap for mid-range µPs

For the chips listed in the middle of the directory, the trends found at the high and low ends of the µP market overlap. Manufacturers have tried to optimize these chips for both low hardware cost and software efficiency. The desire for low hardware cost is manifesting itself in the almost complete conversion of all 8-bit µPs to 1-chip µCs. The desire for software efficiency is manifesting itself in the prolonged popularity of 8-bit µPs with known instruction sets and broad software support.

The current 40-million-per-year unit volume of the 6502 core µP (in the form of the one-chip Mitsubishi 50740 µC) illustrates this overlapping. The 50740 has the ideal combination of the 6502’s small µP-core area and the familiar 6502 software.

Probably the best example of a mid-range chip in which the trends toward low hardware cost and software efficiency overlap is the Z80 µP and its new higher-integration versions, the Hitachi 64180 and the Zilog Z280. The 64180 appears to be a solid success both in terms of statistics (from Dataquest, a San Jose, CA, market-research firm) and in terms of enthusiastic third-party support.

The Zilog Z280 super-enhancement of the Z80, which is even more enhanced than Hitachi’s 64180, reinforces the point, though it’s too early to predict the chip’s success. We think Zilog learned a lesson here. For five years, on the assumption that the Z80’s product life would soon be over, Zilog put the Z280 on a back burner, while spending a great deal of money and effort...
Introducing UniLab 8620 analyzer-emulator with InSight.

- There's nothing like InSight.™ A feature of the new 8620 that lets you actually watch your program go through its paces. So you can debug faster. And speed up microprocessor development. For demanding applications like the automotive controller shown.

- An exciting industry first, InSight blends analyzer/emulator techniques to give you continuous, real time monitoring of key processor functions. See changing register contents, I/O lines, ports, user-defined memory windows with your own labels. And all at once. Interactively. Without stopping your program.

- InSight is made possible by the 8620's advanced bus state analyzer, its 2730-bus-cycle trace buffer, and a new high-speed parallel interface that eliminates RS-232 bottlenecks.

- The fast interface also speeds data throughput. From your hard drive, you can load a 64K program into emulation memory in five seconds.

- On top of that, you get a new, crystal-controlled 1 µsec clock for super precise event timing.

- Computer integrated instruments from Orion prove debugging needn't be costly or tedious. For more than 150 processors. Like all our analyzer-emulators, the 8620 debugs by symptom. Via advanced truth table triggering. Always included is enough breakpointing and single stepping (now faster than ever) to assure optimum efficiency. We even provide a stimulus generator and built-in EPROM programmer to help finish the job.

- Get serious about price/performance. Save big on design, test, and support costs. UniLab 8620 analyzer-emulator.

- Look into it.


ORION
INSTRUMENTS

Computer Integrated Instrumentation
702 Marshall Street, Redwood City, CA 94063
Telex: 530942

*InSight is a trademark of Orion Instruments, Inc.
in trying to make the Z8 family a winner (which has not
yet happened). But now the company is finding that the
12-year-old Z80, far from being at the end of its life,
may just be reaching mid-life. Just because the hard-
ware side of a µP is outdated doesn't mean that its
software side is dying.

Intel appears to realize the great appetite that users
have for mid-range µPs and µCs that run existing
software and can use existing development tools. The
company says it is "repositioning" the 80186 for embed-
ded applications that are more data-oriented than
control oriented. If the 80C186 outdoes the 8096, which
Intel has aimed at embedded applications (albeit mostly
real-time-controller applications) for some time, its
success might be construed as still more proof that
users desire chips that will run widely known software.

**Breaking away from de facto software standards**

Throughout the directory, we make some observa-
tions (based on unit-volume figures from Dataquest)
regarding the actual popularity of µCs and µPs. This
data shows that you must temper your enthusiasm for
the technical features of a particular processor with the
sobering realization that you do encounter risks as you
move away from the established architectures, such as
the Z80 and 8086 families. The reason for the risk is the
software momentum that those families enjoy. Their
software momentum ensures that those µPs—and de-
sign tools for them—will continue to be available.
Designers who choose those chips won't be stuck with a
choice like the Thomson-Mostek 68200 µC, which we
had to remove from the directory again this year
because the company put it on "hold" after the Thom-
son-SGS merger.

Several trends may help users break away from the
entrenched de facto software standards. The steadily
increasing use of the high-level language C (which now
extends to all levels of µPs except the 4-bit level),
abetted by continuous improvements in optimizing com-
pilers, is definitely a healthy sign. The associated
increase in the use of Unix is also healthy. The in-
creased availability of generalized real-time-executives
is a step in the right direction, though none of these
proprietary executives has achieved the stature of
Unix.

Because these software tools aren't tied solely into
any particular µP family, they allow you to approach
your design from the top down. You can do your design
at a high, generalized level and then see which µP runs
your code best. Later, if the product needs a higher-
performance (or lower-cost) µP in order to remain
competitive, you can switch µPs without totally redo-
ing your software. A case in point is Sun Microsystems'
switch from the Motorola 68020 µP in its Sun-3 work-
station to the new Spare RISC in its Sun-4 upgrade.

A future trend that could further free the designer
from entrenched software standards is the use of an
all-encompassing high-level model for defining an open
standard for µP systems. An example of such a model is
the Japanese TRON (The Real-time Operating-system
Nucleus) [Ref 1], which is patterned after the ISO
standard model for data-communication systems.
TRON's architect, Professor Ken Sakamura of the
University of Tokyo, has explained that his goal was to
free µP progress from the chains of downward compati-
bility with older, successful µP families. In creating
TRON, Sakamura was thinking of the day—which will
arrive sooner than we think—when it will be practical
to put several million transistors on a chip, not just ¼
million, as it is today.

**Acknowledgments**

*EDN* would like to thank Patricia A Galligan of Dataquest
(San Jose, CA) for her help with statistical data on unit-
volume use of µPs and µCs. We also thank Andrew
Allison, consultant (Los Altos Hills, CA), for his views on
the relative importance of RISCs (though the views ex-
pressed in this directory are *EDN*'s).

**References**

1. Sakamura, Ken, "Looking into the Future with
TRON," *IEEE Micro*, April 1987, pg 4. This article, the
first of several in the issue, explains the Japanese TRON
definition for a family of µP architectures that balance the
need for standardization with the need for future growth.
2. Cushman, Robert H, "EDN's Thirteenth Annual
3. Cushman, Robert H, "Support chips give designers a
performance edge," *EDN*, June 11, 1987, pg 131. This 10th
annual report on support chips provides a basic list of the
subsystems that would be incorporated around a core µP
for a standard 1-chip µC (such as those listed in the first
part of this µP/µC directory or their ASIC equivalents).
4. Cushman, Robert H, "µP-like DSP chips," *EDN*, Sep-
tember 3, 1987, pg 155. This directory lists the DSP-type
µPs that were included in last year's µP/µC directory.

*Article Interest Quotient (Circle One)*

High 485 Medium 486 Low 487

EDN November 26, 1987
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Additional features include:
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- Supports unaligned transfers (UAT).
- (1) 16-bit and (1) 24-bit timer/counter.
- (7) prioritized interrupts.
- IEEE 1014 (Rev. C1) compatible.
- 4 level VME BUS arbiter (optional).
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Today your choice of OMNIMODULE's include:
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- (2) async RS422 serial ports.
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EDN November 26, 1987
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CIRCLE NO 128
COP400

**AVAILABILITY:** Now.

**COST:** Under $0.50 for NMOS 413L and under $1 for CMOS 413C in very high volume (1M/yr).

**SECOND SOURCE:** Thomson (over 6M units in ’86).

**CORE:** Core µP concept has been used all along for this single-chip family, though on an internal basis.

**Description:** NMOS and CMOS minimum-cost single-chip family. COP chips are microcontrollers intended to make low-cost, intelligent products feasible, and contain the complete µC system—µP, memory and I/O—necessary to implement dedicated control functions. Typical application would be as lone chip in a low-cost toy for mass consumer market, where it would provide the intelligence to interface to a human. An OEM customer might order COP chips at the rate of several million annually, paying just $0.60 apiece.

![Diagram of COP400 family](image)

**HARDWARE CHARACTERISTICS SOFTWARE**

**Description:** 4-BIT NMOS AND CMOS

**National Semiconductor Corp**

2900 Semiconductor Dr, MS 16-174

Santa Clara, CA 95051

Phone (408) 721-4345

**Status:** Dataquest figures for ’86 show COP continues to hold 2nd place in the mostly Asian-dominated 4-bit µC market. COP had 141½% of 4-bit market vs NEC’s 1st-place 75XX, which had 16%. Total COPS unit shipments were 37½M units; 31M were from prime source National. Note that National’s COP800 (next directory entry) is similar to COP400 in name only; it has a different architecture and instruction set.

**Notes:**

1. ROMless 402 and 404 are available for development and low-volume production, as well as piggyback CPUs that carry standard EPROMs. Some COP400 models and peripherals are configured with National Microbus serial I/O for easy exchange of data with low pin count.

2. CMOS chips have optional multi-input wake-up feature, improved timer, including interrupt-on-overflow; designed for increased ESD and latch-up margin.

3. 24- and 28-pin surface-mount packaging available for space-sensitive applications such as consumer goods.

**Specification summary:** Single-chip µC with split-memory architecture; 8-bit-wide instruction side (1k for 420 part) and 4-bit-wide data side (64 for 420 part). Considerable on-chip I/O despite small package size (28 pins for 420) including clocked serial/event-counter port. Family includes 30 devices with different memory and I/O options and fabricated in several device technologies, including basic metal-gate NMOS and CMOS. Power for CMOS will vary from 3 mA at 14-µsec cycle to 120 µA at 64-µsec cycle (using 32-kHz watch crystal) and 2.4V supply. "Asleep" drain will be 6 µA max. Extended-temperature-range devices (–40 to +85°C and –55 to +125°C) available, as well as extended-voltage-range devices.

**HARDWARE SUPPORT**

Mole (microcomputer on-line emulator) consists of two hardware components and software for a host computer. The two hardware components are a general-purpose Brain board common to all National microcontroller µCs and a personality board specific to the particular National µC being supported (which plugs into the Brain board). COP is supported by one of the personality boards.

The general-purpose Brain board works in conjunction with a terminal or host computer such as the IBM PC. With the personality board plugged in, it provides platform for both hardware and software development.

Application hot line: (408) 721-5582

EDN November 26, 1987
COP800

**AVAILABILITY:** Now for 1k ROM and 2k EEPROM. 1st qtr '88 for 4k ROM and 3rd qtr '88 for 4k ROM with UART.

**COST:** $2 to $5 for standard parts, 10k qty

**SECOND SOURCE:** Sierra Semiconductor

**CORE:** Sierra is using COP800 core for custom designs for portable medical monitors and home security, etc. Successful silicon has been achieved, Sierra says.

**Description:** 8-bit CMOS 1-chip family in which a purposely simple core µP is surrounded by varying amounts of memory, peripheral functions, and I/O. Some 20 parts exist or are in the works and many more are forecast for future. Initial core has provision for addressing 32k-byte program memory and 256-byte data memory, but that can be expanded in future. The program and data memory are treated separately so, like the 4-bit COP400, the COP800 has a Harvard architecture. Otherwise it seems quite like von Neumann common-memory machines such as Motorola’s 6805 or National’s 15-bit 1-chip device, the HPC 6040.

**HARDWARE**

- **8-BIT CMOS**

**SOFTWARE**

**I—DATA-MANIPULATION INSTRUCTIONS**

Add, add with carry, subtract and carry

- Logics include rotates, shift compares and conditionals
- Decimal correct
- Increment and decrement
- Bit manipulation: set, reset, and test individual bits in data memory, which includes those in data registers and I/O ports

**II—DATA-MOVEMENT INSTRUCTIONS**

- Load and exchange instructions with optional automatic post increment or decrement of the associated pointer. Most allow the use of either the B or X pointer.
- Decrement register and skip if zero

**III—PROGRAM-MANIPULATION INSTR**

- Jump instructions: relative, absolute, absolute long, indirect
- Subroutine, subroutine long, return and skip (Subroutine levels are limited only by the amount of available RAM)
- Push and pop

**IV—POWER-SAVING INSTRUCTIONS**

- Halt mode, entered by setting data bit and exited by resetting bit

**Notes:**

- 1. Program-branch decisions are implemented in skip-the-next-instruction manner.

**Specification summary:** 8-bit Harvard (split-memory) architecture µC in CMOS. 15-bit program counter (PC) can address 32-byte program memory, which can include data and data tables. Initial on-chip memory selections will be 1k, 2k, and 4k bytes. 8-bit data-address register can address 256-byte data. All data, control, and I/O registers are mapped into data-side memory space. Two bidirectional 8-bit and two unidirectional 4-bit I/O ports max. Each I/O pin has software-selectable options to adapt the chip to specific applications. Part may be operated in ROMless mode to provide for emulation and for applications requiring external program memory, in which case external memory is accessed serially via the two 4-bit ports. On-chip peripheral functions include software-selectable use assignment of 36 I/O pins, 3-wire serial I/O, 16-bit timer/counter with capture register and auto reload, and a multisource (8) interrupt. Each part has an EEPROM equivalent for full "form-fit" function emulation. Maximum speed is 1-µsec instruction cycle (most instructions take one cycle), and because part is static CMOS, it will run down to dc and won’t lose data in memory. Clock for 1-µsec cycle is 20 MHz. Fabricated in double-metal 2-µm (112 µm on way) silicon-gate CMOS. Operates over 2.5 to 6V range and draws 9 mA running full speed at 1-µsec cycles, but less than 1 µA when halted. Enclosed in 20, 24, 28 and 40-pin DIPs and surface-mount packages.

**Notes:**

- 1. Diagram shows basic COP800 family architecture. Over 10 basic parts planned for the family. Each has an emulator part created by replacing standard masked-ROM with EEPROM.
- 2. The basic core, including CPU and some peripherals, is only 66 ms per side (4330 ms sq area), thus only taking up 1/4th of reasonable-sized chip (200 ms per side or 40k sq ms area) and leaving adequate room for not only basic memory and I/O but also for UARTS, A/D converters, additional timers, LCD display drivers, and custom features for specific applications. Sierra says cost of ASIC design can be as low as $40k up front (16 weeks’ time), meaning it can be cost competitive for 100k quantities.
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For details, contact Sales and Marketing, International CMOS Technology, Inc., 2125 Lundy Avenue, San Jose, CA 95131. (408) 434-0678.

ICT CMOS Erasable PROM Selection Guide

<table>
<thead>
<tr>
<th>Device</th>
<th>Pins</th>
<th>Pkg.</th>
<th>Organization</th>
<th>Speed</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>27CX641C-40</td>
<td>24</td>
<td>600 mil</td>
<td>8Kx8</td>
<td>40 ns</td>
<td>80mA max.</td>
</tr>
<tr>
<td>27CX641C-45</td>
<td>24</td>
<td>600 mil</td>
<td>8Kx8</td>
<td>45 ns</td>
<td>80mA max.</td>
</tr>
<tr>
<td>27CX641C-55</td>
<td>24</td>
<td>600 mil</td>
<td>8Kx8</td>
<td>55 ns</td>
<td>80mA max.</td>
</tr>
<tr>
<td>27CX642C-40</td>
<td>24</td>
<td>300 mil</td>
<td>8Kx8</td>
<td>40 ns</td>
<td>80mA max.</td>
</tr>
<tr>
<td>27CX642C-45</td>
<td>24</td>
<td>300 mil</td>
<td>8Kx8</td>
<td>45 ns</td>
<td>80mA max.</td>
</tr>
<tr>
<td>27CX642C-55</td>
<td>24</td>
<td>300 mil</td>
<td>8Kx8</td>
<td>55 ns</td>
<td>80mA max.</td>
</tr>
</tbody>
</table>

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CIRCLE NO 126

EDN November 26, 1987
PIC1600 FAMILY

AVAILABILITY: First silicon for new silicon-gate CMOS expected 4th qtr '87.
COST: Projected at less than $2 to $5 in 25k qty, depending on speed and temperature specs and size of EPROM.
SECOND SOURCE: None.

Description: Family of small 1-chip static CMOS µCs that will use EPROM technology for both low-volume and high-volume production. Supplier says efficient 12-bit instruction word allows use of small EPROMs. Compact architecture also allows small die (100 x 105 mils for smallest part).

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Add and subtract
Logicals
Rotate right and left, decimal adjust
Swap halves
Bit set and clear
II—DATA-MOVEMENT INSTRUCTIONS
All RAM (general- and special-purpose registers) accessible by direct or indirect addressing
Page addressing
Move file
III—PROGRAM-MANIPULATION INSTR
Skip if zero (for comparisons and bit tests)
Move literal to W
Call subroutine
Go to routine
IV—PROGRAM-STATUS-MANIP INSTR
Can bit test on status-register carry, decimal carry, and zero
V—POWER-SAVING AND CONTROL INSTRUCTIONS
Sleep stops oscillator. CLRWDT clears watchdog timer. Tris instructs 3-state ports. Option loads option register.

Notes:
1. Diagram applies to original NMOS 1655A. See table for new CMOS parts.
2. 12-bit-wide instruction word allows all instructions to be single word, which produces compact code; supplier claims benchmarks show almost double the code efficiency of 8-bit instruction word.
3. All current devices are silicon-gate CMOS with 8-bit real-time clock counter, watchdog timer, and 2-level PC-save stack for subroutine nesting. No interrupts.

Specification summary: Split-memory Harvard architecture with 12-bit-wide program EPROM and 8-bit-wide data registers (RAM). See table for EPROM and RAM sizes. Not expandable in memory because intended for self-contained, stand-alone applications. Instructions executed from dc to 200 nsec (20-MHz clock). Devices are fabricated in silicon-gate CMOS. Power consumption ranges from less than 1 µA with clock stopped to 30 mA at 20 MHz. In 18- and 28-pin DIPs and surface mount.

HARDWARE SUPPORT SOFTWARE

Supplier will resell a new PC-based development system that Audix (Bohemia, NY) is readying for both the PIC and the Tl 320 DSP that General Instrument second sources. This development system will have user-friendly features such as extensive use of Microsoft Windows. Its price has been targeted at $3500 to $5000. It is scheduled for mid '88.

Software will be bundled with the new Audix hardware development system. (Actually because the instruction set has not changed—just 6 added instructions—considerable software has existed for some time, including many application programs, such as for motor control.)
8048 FAMILY

**AVAILABILITY:** Now for NMOS and CMOS (12 MHz).

**COST:** Masked-ROM parts less than $2 in high volume (100k qty). EPROM parts cost $18 in 100 qty. CMOS parts cost as low as $3 in 100k qty. Windowless-PROM parts cost $8 in 5k qty.

**SECOND SOURCE:** Toshiba, NEC, Signetics/Philips, National, Oki, Siemens, Fujitsu, GE-Intersil, UMC (Taiwan), with volume being spread out among suppliers.

**CORE:** Zymos has been using 80C49 as core for semicustom for a number of years. Others are following as 8048/49 combines widespread popularity with reasonably small core size.

**DESCRIPTION:** Broad family of 1-chip controller-type μC's, including version that can function as slave (8041). Basic models don't have serial communication ports (some versions from Philips do), but they can use 8080/85 peripherals for I/O expansion. See 8051 listing for enhanced version.

**HARDWARE**

<table>
<thead>
<tr>
<th>PART</th>
<th>MEMORY (BYTES)</th>
<th>PACKAGE PINS</th>
</tr>
</thead>
<tbody>
<tr>
<td>8035</td>
<td>0 0 64</td>
<td>3x8 40</td>
</tr>
<tr>
<td>8048</td>
<td>1k 0 64</td>
<td>3x8 40</td>
</tr>
<tr>
<td>8748</td>
<td>0 1k 64</td>
<td>3x8 40</td>
</tr>
<tr>
<td>8039</td>
<td>0 128 3x8 40</td>
<td></td>
</tr>
<tr>
<td>8049</td>
<td>2k 0 128 3x8 40</td>
<td></td>
</tr>
<tr>
<td>8749</td>
<td>0 2k 128 3x8 40</td>
<td></td>
</tr>
<tr>
<td>8040</td>
<td>0 0 128 3x8 40</td>
<td></td>
</tr>
<tr>
<td>8050</td>
<td>4k 0 256 3x8 40</td>
<td></td>
</tr>
</tbody>
</table>

**SOFTWARE**

**8-BIT NMOS AND CMOS**

**Intel Corp**<br>Embedded Controller Operation<br>5000 W Chandler Blvd<br>Chandler, AZ 85226<br>Phone (602) 961-8051

**STATUS:** This is still the leading 8-bit 1-chip family, based on Dataquest unit volume figures for '86 (43 million units). However, the Dataquest figures also showed a continuing drop in share of market—from a high of 41% in '84 to just 20% in '86. Intel is still bullish about its 8048, saying total family shipments are projected to be 110 million in '87, or 33% of the market. However, we note that Intel choose the 8051 over the 8048 as the kick-off core for ASIC, and Intel says it has no definite plans to ever use the 8048 as an ASIC core.

**HARDWARE CHARACTERISTICS**

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<td>II</td>
<td>Bit set and reset</td>
<td>II—DATA-MOVEMENT INSTRUCTIONS</td>
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<tr>
<td>III</td>
<td>Two working banks of 8-bit registers</td>
<td>III—DATA-MANIPULATION INSTR</td>
</tr>
<tr>
<td>IV</td>
<td>Indirect and direct data fetches</td>
<td>IV—DATA-MOVEMENT INSTR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note: Described are the 90 basic instructions for the 8048/8748.</td>
</tr>
</tbody>
</table>

**Notes:**

1. Diagram is for basic 8048. Table indicates some of other basic parts, most of which exist in both NMOS and CMOS.
2. CMOS parts are designated 80C48, 80C49, 80C50, etc.
3. There are many other variations on basic 8048 among the many suppliers. For example, Intel's 8041/42 chips are software compatible but can be configured as slaves to host μPs for interface applications. The National NS 405/455 uses the 8048 core as basis of a terminal controller. Siemens has telecomm-oriented 80C382/482. A number of semicustom houses use the 8048 as a core processor in their libraries.

**Notes:**

From Intel: Intel now plays down 8048 support, saying that there are now numerous third-party OEM suppliers of PC-hosted emulators for the 8048 family.

From NEC: Ekakit 84C-1 stand-alone emulator (less than $2000).
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Yet it’s performance you can use. Because the NS32532 was created for real-world designers working on real-world systems to meet real-world needs.

**PERFORMANCE YOU CAN COUNT ON**

The NS32532 is capable of delivering 15 MIPS peak performance, 8-10 MIPS sustained, at 30 MHz.

Not “no-ops” MIPS. Not benchmarking MIPS. Not RISC MIPS. But genuine VAX® 11/780 MIPS.

You’re looking at 16,600 Dhrystones per second.

Not to mention high integer performance and high floating-point performance. With a range of FPU solutions that deliver up to 8 million double-precision Whetstones per second.

Below: NS32532 chip
Left: VME532 evaluation board; NS32532 block diagram; competitive performance comparison

**The NS32532**

- 8-10 MIPS sustained, 15 MIPS peak
- 20-, 25-, and 30-MHz devices
- On-chip 1024-byte 2-way set associative physical data cache
- On-chip 512-byte direct mapped physical instruction cache
- Hardware cache invalidate for high-performance cache coherency
- On-chip demand-paged memory management including 64-entry fully associative Translation Lookaside Buffer
- 4-stage instruction pipeline including instruction prefetch and branch prediction
- 2-clock basic READ/WRITE cycle
- 1-clock burst-mode transfers
- Unique bit-manipulation and string-handling instructions
- Highly symmetrical and orthogonal instruction set producing compact code
- Extremely fast context switch (3.6 µs) and interrupt service (1.3 µs)
- Fabricated in NMOS
- 370,000 transistor sites
- SAMPLES AVAILABLE NOW

**SUPER-MINI PERFORMANCE ON A CHIP**

The NS32532 achieves its superior performance because it integrates key systems functions on a single piece of silicon.

Only the NS32532 incorporates on-chip data and instruction caches, demand-paged virtual memory management, and a 4-stage instruction pipeline. With instruction prefetches and branch prediction. Plus a hardware cache invalidate mechanism that ensures cache coherency.

**SCALABLE PERFORMANCE**

The NS32532 is one of seven CPUs based on the same 32-bit architecture. With the same orthogonal, highly symmetrical instruction set.

Which means you can migrate your design throughout the entire performance range without having to re-engineer your software at any level. And you can build consistently competitive systems without resorting to some “more innovative” architecture that leaves you and your software investment in the lurch.

**PERFORMANCE THAT’S READY FOR YOU TODAY**

We’ve already begun sampling silicon. We’ve already ported UNIX® System V.3 and VRTX®. And we’ve already produced a board-level implementation — a fully integrated, fully populated, plug-and-go VME-compatible native environment . . . available now for evaluation. So are nearly 150 other members of the Series 32000® family, including coprocessors, peripherals, development tools and optimizing compilers.

To talk about putting our performance into practice in your application, call our Application Engineers toll free: 800/538-1866, ext. 532 or 800/672-1811, ext. 532 (within California).
**8051/8052 FAMILY**

**AVAILABILITY:** Now for 8051, 80C51, 8031, 80C31, 8751, 87C51, 8032, and 8052, as well as special versions from second sources (see notes).

**COST:** $4.50 in 1000 qty for 8051; $8.50 in 100 qty for 80C51; $5.35 in 100k qty for 8052; $44 for 87C51; $70 for EEPROM UPI-452 slave version, 1k qty.

**SECOND SOURCE:** Siemens, Signetics/Philips, AMD, Fujitsu, Oki, and Harris-Matra (France) licensed.

**CORE:** Intel's new ASIC Components Group (Santa Clara, CA) considers the 8051 as its starting µP core. RCA and Fujitsu also using it as ASIC core.

**Description:** Expandable single-chip "controller," an enhanced version of the same supplier's widely used 8048 family. Architecturally, it features the more "regular" nonpaged form of addressing for easier programming, more interrupts with extra RAM register banks to service them, increased stack depth, and new instructions such as multiply, divide, and compare. In peripheral support, it adds a full-duplex hardware UART and enlarged timer/counter capability.

**HARDWARE CHARACTERISTICS SOFTWARE**

**I—DATA-MANIPULATION INSTRUCTIONS**

- Arithmetic, including add, subtract, multiply, and divide
- Bit manipulation, including complex tests on bits (and branching on results)

**II—DATA-MOVEMENT INSTRUCTIONS**

- Register addressing for the eight working registers in the four register banks
- Direct, immediate, and indirect data addressing for more general data accessing
- Table look-up in ROM via data pointer

**III—PROGRAM-MANIPULATION INSTR**

- Depth of subroutining limited only by available space in 128- or 256-byte on-chip RAM
- Conditional jumps on status-register flags
- Conditional jumps on comparisons
- Vectored interrupts to service two external interrupts, timers, and UART

**IV—PROGRAM-STATUS-MANIP INSTR**

- CPU's program-status word fully accessible via software. Status bits in timer and UART also software accessible

**Notes:**

1. The 8051 family have between 128 and 256 bytes of RAM and differ mainly in their amount and form of on-chip memory. The 8051 incorporates 4k bytes of masked ROM. The 8751 and 87C51 have 4k bytes of EPROM. The 8031 and 80C31 have 64k bytes of on-chip ROM. Hence, because it must use ports to access external memory, only port 1 is available for I/O. The 8052 has 8k bytes of masked ROM. The 8032 has no on-chip ROM.

2. The 8051's so-called Boolean-processor capabilities refer to the way instructions can single out bits in RAM, accumulators, I/O registers, etc, and perform complex bit tests and comparisons, then execute relative jumps based on results.

3. The slave version of the 8C51, the UPI-452, is counterpart of UPI-42 (8041/42) for 8048 family. It is intended for software-customizable interfaces.

4. Intel has one model of 8052 preprogrammed with a full Basic interpreter.

5. Siemens has developed proprietary enhancements called 80515/535. They feature 16k ROM, with additional I/O ports, 12-µsec 8-bit A/D with eight input channels, 12 interrupts with four programmable priority levels. They are 12-MHz (1-µsec cycle) NMOS, packaged in TAB/Micropack.

**From Intel:**

- ICE-5100/252 in-circuit emulator ($6995) supports the entire MCS-51 family including 8051, 8051, and 80C52. Comes with macrossembler and editor. The emulator is hosted on an IBM PC/AT/XT running DOS 3.1 or later, as well as Inteltec Series III/IV development systems. ICE-51 in-circuit emulator ($6000) hosted on Series III/IV Inteltec supports 8051 at 12 MHz.
- SDK-51 System Design Kit ($950) is a single-board computer for low-cost development of 8051 applications.

**From Siemens:**

- Meta-ICE-80515 in-circuit emulator for 80515, hosted on IBM PC.

**From Others:**

- A number of third-party software suppliers have developed C compilers for 8051 that have special features suited to microcontroller applications. Among these are Micro Computer Control (HopeWell, NJ) for $1495 and Archemides Software (San Francisco, CA) for $851. Both are hosted on IBM PC.
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CIRCLE NO 123
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DT2841 Series data acquisition boards connect directly to a processor board for 750kHz throughput, and signal processing, on the IBM PC AT!

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DT-Connect is an open interface specification which permits the direct connection of stand-alone data acquisition and frame grabber boards to processor boards for greatly accelerated signal (DSP) and image processing.

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1897: Alexander Graham Bell's telephone allows for the transfer of words as they're spoken. Fred Molinari, President, is inspired to develop similar real-time connections in data acquisition.

<table>
<thead>
<tr>
<th>Model</th>
<th>Channels</th>
<th>Resolution (Bits)</th>
<th>Gain</th>
<th>Throughput (kHz)</th>
<th>Model</th>
<th>Channels</th>
<th>Resolution (Bits)</th>
<th>Gain</th>
<th>Throughput (kHz)</th>
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</thead>
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<tr>
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<td>16SE/8DI</td>
<td>12</td>
<td>1,2,4,8</td>
<td>40</td>
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<td>1,2,4,8</td>
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<td>16SE/8DI</td>
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</tbody>
</table>

Notes: (1) Throughput shown is per D/A channel. Aggregate throughput is 260kHz. (2) Simultaneous Sample and Hold A/D

CIRCLE NO 122

EDN November 26, 1987
6804/6805

AVAILABILITY: Now for most models.
COST: $0.49 to $40. The $0.49 is 1M qty of 6804/1 (500x minimum order). CMOS parts remain more expensive than NMOS.
SECOND SOURCE: Hitachi, RCA, and Thomson; RCA for CMOS parts only.
CORE: Motorola and NCR have joint ASIC pact that will use CMOS 6805 as core along with NCR's similar 6502 µP core. (SGS has 56 core, which has somewhat similar architecture to 6800.)

Description: Family of 1-chip µCs based loosely on 6800 architecture, and software security. The 6804s are meant to be lowest end. They use amounts of I/O, RAM, and ROM. Internal bus frequencies span dc to 2 MHz. Some parts contain on chip a 28-pin interface, EEROM, serial I/O, and software security. The 6804s are meant to be lowest end. They use some serial data paths internally to reduce chip size to as small as 113x98 mils.

Hardware Notes:
1. Diagram is for nonexpandable Model P2 in 28-pin package.
2. Comparison of 6805 with 6800: Stack pointer has only five working register bits, so stack is only 32 bytes deep. Only one accumulator. Index register only 8 bits wide, so it can only span 256 memory locations. Only one external interrupt.
3. Note additional 116 bytes in ROM for built-in self-check program that tests I/O, ROM pattern, RAM, and interrupts. Program is initiated by special pin. 4. RCA has emulator versions (68EM05/C4.D2) for prototyping and low-volume production. These are ROM/µE devices with all ROM access buses brought out for direct interfacing to industry-standard EPROMs. Come in 40-pin piggyback (for 2764). RCA will have 7.7k ROM 6805 this year and 16k ROM 6805 in '88.

8-BIT NMOS AND CMOS

Motorola Microprocessor Products Group
6501 Wm Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

Status: Supplier's steady commitment to this family over past seven years has apparently paid off; Dataquest '86 figures show the 6805 has grown to nearly 15% of the 8-bit-µC market, attaining a volume of nearly 31½ million units/y. It traits only the 8046/49 family (which has 20% of 8-bit-µC market) and the 50740 (which has 16%). RCA is concentrating its efforts on the CMOS side of family and is bringing out its own enhancements. For some reason, the 6805's little sister, the 6804, has not caught on. Dataquest showed it's '86 volume at 1½ million units.

Hardware Notes:
1. Diagram is for nonexpandable Model P2 in 28-pin package.
2. Comparison of 6805 with 6800: Stack pointer has only five working register bits, so stack is only 32 bytes deep. Only one accumulator. Index register only 8 bits wide, so it can only span 256 memory locations. Only one external interrupt.
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Hardware

From Motorola: HDS-200 hardware/software development station; operates stand-alone or interfaced to virtually any host with an RS-232C line (including Motorola's Exor-trademarked stations). The less-costly 68705ESVM (HMOS) or 1468705EM (CMOS) boards, which have ports to a terminal and host computer, provide target-system emulation.

From RCA: Single-board evaluation kit that will interface to IBM PC via RS232.

From others: A number of third-party companies provide hardware emulators for the 6805 family: Sophia Systems (Santa Clara, CA), American Automation (Tustin, CA), etc. Most of these interface to IBM PCs.

Support

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733.

From others: Many cross macroassemblers and linking loaders, some relocatable. RELMS (San Jose, CA) has cross support for Intel development systems. Avocet Systems Inc (Rockport, ME) has crossassemblers for 6805 and 6804 that run on IBM PC, etc.

I—DATA-MANIPULATION INSTRUCTIONS

All 6800 arithmetic, logic, and shift instructions. Bit set, clear, and branch on bit test (bit tests can be made quite generally on all I/O and memory bits). 68HC05 has 8×8 multiply

II—DATA-MOVEMENT INSTRUCTIONS

Relative addressing allows data relocation

III—PROGRAM-MANIPULATION INSTR

18 conditional branches, including branch of interrupt line test

IV—PROGRAM-STATUS-MANIP INSTR

Instructions for manipulating bits in status register (and in timer)

V—POWER-SAVING INSTRUCTIONS

CMOS 6804s and 6805s have Stop and Wait instructions and will safely reset themselves when the clock is applied again

Specification summary: Common-memory architecture, in which instructions, data, I/O, and timers all share the same memory space. This allows I/O to be bit rotated, bit manipulated, etc. Dedicated bit manipulation includes bit set/clear and branch on bit set/clear. A 4-MHz oscillator provides a 1-MHz internal cycle on most '85 versions. New 68HC05s have a 2.1-MHz internal bus speed. Included are parts with program security, on-chip EEROM, A/D converter, serial peripheral interface (SPI), and PLL frequency synthesizer. Family consists of NMOS and CMOS parts in 20-, 28-, and 40-pin DIPs (also chip carriers, etc). NMOS requires 5V supply, while CMOS will operate over 3 to 6V.

I-DATA-MANIPULATION INSTRUCTIONS

III-PROGRAM-MANIP INSTR

IV-PROGRAM-STATUS-MANIP INSTR

V-POWER-SAVING INSTRUCTIONS

SOFTWARE

8-BIT NMOS AND CMOS
6801/6301/68HC11/68HC811

**AVAILABILITY:** Now for 6801, 6301, and 68HC11.

**COST:** In 1k qty, from less than $3 to $40.

**SECOND SOURCE:** Hitachi, Thomson. Hitachi is prime source on the 63XX CMOS versions.

**Description:** 6801 is large, expandable 1-chip version of the 6800, with enhancements that include 10 more instructions, serial I/O, 8x8 multiplication, and a multifunction 16-bit timer. 6301 is slightly enhanced with enhancements that include 10 more instructions, serial I/O, 8x8 multiplier. 68HC11 is further enhanced in static CMOS. 68HC11 has a second 16-bit-wide register, an 8-function timer, a 2-function pulse counter, and a multifunction 16-bit timer. 6301 is slightly enhanced with enhancements that include 10 more instructions, serial I/O, 8x8 multiplier.

**Availability:** Now for 6801, 6301, and 68HC11.

**Description:** 6801 is large, expandable 1-chip version of the 6800, with accumulator, an enhanced UART (SCI), a high-speed (1-MHz) serial shifter (SPI), an 8-channel, 8-bit A/D converter, and an EEROM.

**Description:** 68HC11 has additional active bits related to “stop” mode and Motorola 68HC11 fabricated in static CMOS (to allow dormant, data registers share the same memory space. This allows I/O, etc, to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and, beyond that, 91 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 2.1 MHz for 68HC11. The 6801 fabricated in NMOS, 6301 fabricated in CMOS, and Motorola 68HC11 fabricated in static CMOS (to allow dormant, micropower “asleep” state). 6801 in 40-pin DIP, 6301 in 64-pin DIP and flat pack, and 68HC11 in 48-pin DIP and 52-pin quad.

**Hardware Notes:**
1. 6801 has all 6800 µP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set, with 88 additional op codes.

**Specification Summary:** Expandable single-chip µC with common-memory architecture, in which all instructions, data, I/O, control, and data registers share the same memory space. This allows I/O, etc, to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and, beyond that, 91 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 2.1 MHz for 68HC11. The 6801 fabricated in NMOS, 6301 fabricated in CMOS, and Motorola 68HC11 fabricated in static CMOS (to allow dormant, micropower “asleep” state). 6801 in 40-pin DIP, 6301 in 64-pin DIP and flat pack, and 68HC11 in 48-pin DIP and 52-pin quad.

**Hardware Notes:**
1. Diagram is for 6801. See table for others.
2. Hitachi has developed some slightly enhanced CMOS versions, the 63XX Series, that Motorola has second sourced. “2TA” versions, such as the 63701VOP, have EEPROM program memories in inexpensive windowless packages for 1-time programming in moderate-volume production (to 10k).
3. Motorola 68HC11 is very much enhanced 6801. New 68HC11A8 has 512 bytes EEPROM. 68HC811A2 has 2k bytes EEPROM. EEPROM said to be handy for storing field and factory calibrations.

**From Motorola:** For 6801 family, M68701EVM is evaluation module that has port for terminal and port for any RS-232C host and will program 6801 EPROM parts. For 68HC11, the similar M68HC11EVM. Also M68HC11EVB boards ($168.11) for evaluating EEPROM versions. For both 6801 and 68HC11, HDS-300 software-development station operates stand-alone or interfaced to most any host with RS-232C.

**From others:** Third-party hardware development systems. For example CT68HC11 ($5000 to $6000) from Ashling Microsystems Ltd (Limerick, Ireland).

**8-BIT NMOS AND CMOS**

**Motorola Microprocessor Products Group**
6501 Wm Cannon Dr W
Austin, TX 78735
Phone (512) 440-2000

**Status:** This has been a well-received family with more than 14½ million units in '86, according to Dataquest (7% share of market). Motorola is now following migration of customers to more powerful 1-chip devices and is concentrating on the new 68HC11 enhancement of the 6801, such as increased on-chip EEPROM. The 68HC11 is still in early growth phase—Dataquest showed only 0.7 million units for '86.

**Hardware CHARACTERISTICS**

**Software**

1—DATA-MANIPULATION INSTRUCTIONS

Arithmetic and logic instructions to take advantage of two accumulators, including 8x8 multiply. 68HC11 has additional 16-bit operations, integer and fractional divide, and bit manipulation.

2—DATA-MOVEMENT INSTRUCTIONS

Can reach the first 256 locations of memory with short instructions. Can list-process efficiently with the index register (two on 68HC11) and can add accumulator to index register, within a 512-byte range. Relative addressing allows data relocation. Has 16-bit load and store.

3—PROGRAM-MANIPULATION INSTR

Has PDP-11 branches and conditional branches. Has unlimited subroutine nesting via stack pointer, addressing LIFO stacks in RAM. Eight levels of prioritized, vectored interrupts (21 on 68HC11).

IV—POWER-SAVING INSTRUCTIONS

6301 has sleep instruction. 68HC11 has Stop and Wait instructions similar to 146805 but with disabling provision via a bit in status register.

**Hardware Notes:**
1. 6801 has all 6800 µP instructions plus 10 new ones to handle additional resources such as advanced serial I/O ports and timers.
2. 68HC11 has enhanced 6801 instruction set, with 88 additional op codes.

**Specification Summary:** Expandable single-chip µC with common-memory architecture, in which all instructions, data, I/O, control, and data registers share the same memory space. This allows I/O, etc, to be handled like memory with all instructions applying. Instruction set is upwardly compatible with 6800, with 10 additional instructions for 6801 and, beyond that, 91 new op codes for 68HC11. The ROM, RAM, and I/O resources for 6801 and 68HC11 families are detailed in table. Internal bus speed to 2 MHz for 6801 and from dc (asleep) to 2.1 MHz for 68HC11. The 6801 fabricated in NMOS, 6301 fabricated in CMOS, and Motorola 68HC11 fabricated in static CMOS (to allow dormant, micropower “asleep” state). 6801 in 40-pin DIP, 6301 in 64-pin DIP and flat pack, and 68HC11 in 48-pin DIP and 52-pin quad.

**Hardware Notes:**
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**From others:** Third-party hardware development systems. For example CT68HC11 ($5000 to $6000) from Ashling Microsystems Ltd (Limerick, Ireland).

**From Motorola:** Software can be obtained free for downloading over phone lines by calling(512) 440-3733. C compiler to run on Unix System V for 68HC11. For least expensive approach, you can use 6801 parts with LLBug monitor on on-chip ROM (MC6801L1).

**From others:** Cross macroassemblers and linking loaders, some relocatable, to run on popular minis and personal computers. For example, C compiler from Archimedes (San Francisco, CA) to run on IBM PC ($995) and DEC VAX ($3995 to $5995).
PRESENTING THE WINNING ADVERTISERS FROM THE EDN AUGUST 6, 1987 ISSUE

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COMPANY: Control Data
AGENCY: MacManus Advertising Company

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Senior Staff Engineer, Spar Aerospace Limited

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Engineer, Controlled Power Corp.

COMPANY: Harris Semiconductor
AGENCY: The Downs Group Inc., Advertising

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Hardware... software... beachware! Nothing wears better in your islands of automation than our 80C86 circuits.
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"Good display examples."
Design Engineer, Rockwell International

COMPANY:
Advanced Micro Devices

AGENCY:
skeye/donna/pearlstein

"Peels your attention to it. Catchy."
Design Engineer, Sun Electric

"Hopeful, positive tone expressed in the graphics."
Engineer, Teledyne

"Good description of product data and price."
Engineer, Dravo Corp.
COMPANY: S-MOS Systems  
AGENCY: Van Bronkhorst Group  
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Design Engineer, Microwest Terminal Systems  
“Big, colorful and informative.”  
Staff Engineer, TRW

COMPANY: Precision Monolithics Inc.  
AGENCY: PMI Advertising  
“Concise and colorful. I got the info at a glance.”  
Design Engineer, Sun Electric

COMPANY: NCR Corporation  
AGENCY: NW Ayer  
“Eye catching, with useful information.”  
Development Engineer, Honeywell, Inc.

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Senior Test Engineer, Sanders Associates  
“Attractive layout, pleasant colorization, interesting headline.”  
Senior Engineer, Lockheed Space Operations
COMPANY: LTX
AGENCY: Kelley & Wallwork

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COMPANY: Hewlett-Packard
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Design Engineer, General Electric

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AGENCY: Austin Associates

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Design Engineer, Ziatech Corporation

COMPANY: Force Computers, Inc.
AGENCY: Royal Media

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Design Engineer, Industry Consultants

COMPANY: AT&T
AGENCY: Foote Cone & Belding/Leber Katz Partners

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EDN November 26, 1987
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Manufacturer of Gould AMI Semiconductors.
6500/1, 65C124, 50740, 37700

**AVAILABILITY:** Now for all NMOS and most 8-bit CMOS parts. 1988 for Mitsubishi 37700 16-bit internal parts.
**COST:** Prices range from $2 to $20 according to complexity of part and volume, whether in NMOS or CMOS. Volume leader Mitsubishi says its prices range from $2.25 to $8.

**SECOND SOURCE:** NCR (licensed) and California Micro Devices for Rockwell NMOS parts. WDC says it has licensed a number of suppliers worldwide for its CMOS designs.
**CORE:** Standard megacell in libraries of NCR, Mitsubishi, WDC, SMC, etc. (widely used because of compact 6502 die size).

**Description:** There are three different sources for 1-chip versions of 6502 µP: the original 6501/0 NMOS family from Rockwell, the new 65C124 CMOS family from WDC, and the very successful 50740 CMOS family from Mitsubishi. Most parts are 100% software compatible with 6502, though in some cases enhanced instructions such as bit manipulation have been added. Because of small die size of 6502 core, many of these parts are being designed according to standard-cell ASIC approach. Vendors claim these 1-chip sets have a speed advantage over competing 1-chip devices, because of 6502's 2-cycle bus and pipelining.

**HARDWARE**

**CHARACTERISTICS**

**SOFTWARE**

1. **DATA-MANIPULATION INSTRUCTIONS**
   - Arithmetic and logical. Decimal mode via control bit in status register.
   - Can operate on locations in memory space (which can be either RAM or I/O ports)
   - Bit-manipulation enhancement on some models allows bit set and reset and branching on bit set or reset

2. **DATA-MOVEMENT INSTRUCTIONS**
   - True indexed addressing, though index offset limited to eight bits in two CPU registers—X and Y. Short-form addressing to zero page. Has two sophisticated indirect-indexed and indexed-indirect instructions for handling tables

3. **PROGRAM-MANIPULATION INSTR**
   - Conditional branches with signed relative addresses
   - Nonmaskable and/or maskable interrupts, depending on model

4. **PROGRAM-STATUS-MANIP INSTR**
   - Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits

**Notes:**
1. 6500/1 instruction set is 100% identical to that of previous 650X family devices such as 6502, with exception of bit-manipulation instructions for some devices. (No new instructions added to handle new on-chip features like timers and I/O because they are all handled as if in external memory space.)
2. Mitsubishi chips have some added instructions.

**Specification summary:** 1-chip nonexpandable and expandable versions of 650X family. Have 2k- to 16k-byte ROM, 64- to 512-byte RAM, 8-bit A/D converters, LCD drivers, or high-speed parallel interfaces. Many models have special functions such as UARTs, 8-bit I/O devices, RS-232C ports, etc. Full MIL-spec temperature range devices from WDC.

**FROM ROCKWELL:** Emulator part, the 64-pin 6500/1E ($75), can be used in R6500/1 personality card ($995), which plugs into LCE System ($1250). Backpack part will be ROMless 40-pin 6500/1EA ($75), into which industry-standard EPROMs can be plugged.

**FROM MITSUBISHI:** Debugging machine PC4000E ($1000) with ICE cards for each device model ($750 to $1100).

**FROM WDC:** Toolbox design system that runs in conjunction with Apple lie & IIGS and includes ASC/ design capability (to $5,000).
Z8, SUPER8

AVAILABILITY: Now for 2k-byte, 4k-byte, and ROMless parts at 8 and 12 MHz and Super8. Sharp and Zilog have CMOS now. SGS has 4k EPROM and 8k ROM and will have S9 1 Qtr '88.

COST: Less than $3.50 for Z8 in volume, $6.50 for Super8 in volume. (28-pin version for $1)

SECONC SOURCE: SGS (licensed); Sharp for both NMOS and CMOS; Catalyst for EPROM version, VLSI Technology for CMOS.

CORE: From Zilog & VLSI Technology. (SGS’s S9 core is based on Catalyst for EPROM version, VLSI Technology for CMOS.

Description: Z8 is a "maxi" single-chip µC that is a composite of many machines. It has powerful features that can't necessarily be used simultaneously, a common problem with single-chip units—particularly the expandable ones. Not really compatible with supplier's Z80 or Z8000 because architecture is so different; closest to Z8000. However, slave Z8 versions interface to Z80 and Z8000 buses. New "Super8" version has more of everything: more data and program memory, more on-chip peripherals, more instructions.

SOFTWARE

I.—DATA-MANIPULATION INSTRUCTIONS
Add, add with carry, decimal adjust, increment byte and word, decrement byte and word, subtract, subtract with carry

Multiply and divide added to Super8 version

Logicals: AND, compare, complement, OR, and exclusive OR

Rotates and swaps

Bit manipulation: test under mask, test complement under mask, and logical tests of bits

II.—DATA-MOVEMENT INSTR
Address modes: immediate, register, register pair, indirect register, indirect register pair, direct, indexed, and relative

Block transfer: load constant autoincrement, load external autoincrement

Load: clear, load, load constant, load external, pop and push

III.—PROGRAM-MANIP INSTR
Call, decrement-and-jump on nonzero, interrupt return, jump conditional, and jump relative conditional, return

IV.—PROGRAM-STATUS-MANIP INSTR
Set, reset, and complement of carry flag

Note: Ability to set, reset, and test any bit or combinations of as many as eight bits allows any byte to function as a user flag register.

Specification summary: Unique architecture with three memory spaces: program memory (0, 2k, 4k, or 8k bytes in internal masked ROM; rest to 64k bytes can be external), data memory (to 64k bytes external), and CPU register file (256-byte space that includes 124 truly general-purpose working register/accumulators). Executes 129 instructions at 0.6 to 3.0 µsec at 8-MHz internal clock (16-MHz oscillator). Has built-in duplex UART (96k bps) and two 8-bit timers, each with 6-bit prescaler. Housed in 40-pin DIP, with 28-pin economy versions planned. New enhanced Super8 has 352 bytes of on-chip data and control registers (256 of which are general purpose). Initially it will be a ROMless part, but as much as 16k bytes of on-chip program ROM are expected. New multiply and divide instructions. On-chip peripheral functions include DMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has fast (600 nsec) interrupt response, with 37 interrupt sources. Comes in 48- and 44-pin packages.

Zilog Inc
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

Status: Last year, supplier predicted Z8 would reach 12-million-unit level in '87 because of increasing demand for $1 28-pin Z8, which is directed at appliance applications. Dataquest showed a volume of 4.3 million for '86, however, and Zilog admits build-up of Z8 has been somewhat disappointing. Zilog points out that Z8 volume is still growing, though, and that Z8 has had several-hundred design wins (many in Far East), and some of these are now going into production. Meanwhile SGS has turned its CMOS efforts to its S9, a proprietary enhancement of the Super8, which SGS will use for an ASIC building block.

HARDWARE — CHARACTERISTICS — SOFTWARE

Notes:
1. Diagram applies to basic 2k-byte version. Many other versions exist.
2. The 124 working registers (272 on Super8) are truly general purpose.
3. The register pointer singles out a "workspace" of 16 working registers (256 of which are general purpose) . Initially it will

     include OMA, two 16-bit timer/counters, maximum of 40 I/O lines, full-duplex UART, and optional synchronous/asynchronous serial channel. Has fast (600 nsec) interrupt response, with 37 interrupt sources. Comes in 48- and 44-pin packages.

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     From J-K Engineering (Singapore): Zilog-designed full-feature emulators ($600).

     From SGS: Emulator (TE-Z8) for software/firmware developed on SGS UX-8/22 development system ($2200). Interface for IBM PC ($3000).

     From Microtek (through New Micro, Gardenia, CA): Mice-II ($4,800 to $5,600), real-time emulation system for Super8.

     From Creative Technology (Atlanta, GA): Super8 emulator ($1195) low-cost system for use with IBM PC. Documents extra ($50).

     From others: Hardware development tools for Super8 from Orion Instruments and Sophia Systems.

     From Zilog (and SGS): A version of Z8 with Tiny Basic in ROM (Z8671) that allows stand-alone self-programming of chip. Super8 with Forth.

     From SGS: Emulator package, including debugger, disassembler, and trace function. Crossassembler for use with IBM PC.

     From others: Software (crossassemblers, etc) is also available from HP, Tektronix, 2500 AD, Western Ware, and Avocet; for Super8, Allen Ashley, 2500 AD, Creative Technology, and Microtek. C compiler from Micro Computer Corp. (Contact supplier for addresses).

HARDWARE — SUPPORT — SOFTWARE

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EDN November 26, 1987
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- France Tel: 01-3946-9612. Telex: 990499 NEC EF.
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- UK Tel: 020-691133. Telex: 826791 NECUK G.
- Asia Hong Kong Tel: 3-755-8900. Telex: 5461 HNHEK HK.
- Taiwan Tel: 02-252-4192. Telex: 22372 HNHEK TP.
- Singapore Tel: 4019888. Telex: 39726 NECES RS.
- Oceania Australia Tel: 03-287-6355. Telex: RAC8343 NECBCD.
7000 FAMILY

AVAILABILITY: Now for NMOS, CMOS, and EEPROM NMOS from Seeq, 8k CMOS 77C82 from TI by 4 qtr '87.

COST: TI pricing: $2.90 for 70C20 (100 qty) and $0.99 for 70C10 (1k qty). Seeq pricing: $48 for 16-MHz 72720 (100 qty) (projected to drop to $15 to $20 or less in volume).

SECOND SOURCE: General Instrument and Seeq (72720). Note that each supplier is taking a different direction so direct second sourcing is limited.

CORE: See note on Scat architecture.

Description: Software-compatible family of NMOS and CMOS 8-bit, expandable 1-chip µCs. Architecture laid out on chip so that new product variations in memory size, I/O, etc. are easier to accomplish. A full-duplex UART, enhanced timers, and interrupts are incorporated in high-end family members (70CXX2). Instructions typically perform combined load, operation, and store functions, thereby increasing overall system performance and code efficiency.

--- HARDWARE --- CHARACTERISTICS --- SOFTWARE ---

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, 8x8 multiply, BCD
Logicals, increment, decrement (single and double)
Rotates right and left. Bit test

II—DATA-MOVEMENT INSTRUCTIONS
Dual-operand moves avoid time wasted going through accumulator.
Apply to many instructions

INDEXING VIA B REGISTER
16-bit moves

III—PROGRAM-MANIPULATION INSTR
Call and return Bit test and jump on both I/O and memory Conditional jumps using PC-relative addressing

IV—PROGRAM-STATUS-MANIP INSTR
Status register contains carry, sign, zero, and interrupt enable. Instructions to change carry and interrupt enable

Specification summary: Unified-memory architecture in which application program ROM (EPROM), working registers, I/O registers, and some control registers all share common memory space of 64k bytes (except TI CT models). Low-end family members have an 8-bit timer with capture latch and 5-bit prescale; interrupt; 64, 128, and 256 bytes of RAM; and 2x or 4x bytes of ROM (to 12x-byte ROM for NMOS GI parts). High-end 70C42 includes two 16-bit timers (one with capture latch), which are cascadable to 26 bits; a UART with an 8-bit timer for baud-rate generation (or usable as a third timer); programmable interrupts; 256 bytes of RAM; and 4x bytes of ROM. High-performance model operates to 8 MHz with basic microconstruction cycle taking 250 nsec. Most instructions take 5 to 9 cycles. Minimum instruction time is 1.25 µsec, which includes load, logic or arithmetic operations, and store. The 8x8 unsigned multiply takes 10.75 µsec at 8 MHz. I/O to 32 pins with some models, including special functions such as UARTs and ADCs. NMOS and NMOS-EPROM devices require 5V supplies; CMOS operates over 2.5 to 6V VCC, and includes power-down modes. Available in 28- and 40-pin DIPs, and 28- and 44-pin PLCCs.

HARDWARE SUPPORT SOFTWARE

From TI: Crossassembler and linker to run on IBM PC that may serve as host for XDS (also on DEC VAX).
From Cybernetic Micro Systems (San Gregorio, CA): Assembler, simulator, and debugger to run on IBM PC.

From Allen Ashley (Pasadena, CA): Crossassemblers and emulators to run on IBM PC.

Literature: TI 7000 family data manual with applications.

--- TABLE ---

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8080A/8085AH/80C85

**AVAILABILITY:** Now for both in NMOS and for CMOS versions of 8085 (80C85).

**COST:** Prices for these older multisourced parts have dropped to $1 and below, with prices as low as $0.65 for volume purchases. CMOS parts, especially faster ones, are more expensive. Radiation-hardened CMOS parts are very expensive ($300 to $800).

**SECOND SOURCE:** 8080A: AMD. 8085: NEC and Toshiba (and Intel) had most of market between them in '86 but Mitsubishi, Siemens, and AMD also shipped parts. 80C85: Oki active with Harris and Calmos (Canada) supplying nuclear-radiation-hardened CMOS to military and aerospace customers.

**Description:** Has proven a good general-purpose, midrange µP, though not the most efficient one for small programs. 8085 executes 8080 instructions, but with simpler hardware. Z80 (see elsewhere in this directory) is an enhanced 8080 but has different package pinouts and bus operation. New 8086 (see elsewhere in this directory) is only vaguely software compatible, but 8-bit-bus 8088 version of 8086 can interface to 8080 and 8085 peripherals.

**Status:** The venerable 8080—the µP that gave legitimacy to the µP revolution—is pretty much obsolete. It has less than 0.28% of the 8-bit-µP market in '86, according to Dataquest. The 8085 is also starting to fall off, according to Dataquest figures: Its market share dropped from 28% in '85 to 17% in '86. Still, it was in second place behind the Z80.

**HARDWARE CHARACTERISTICS SOFTWARE**

### I—DATA-MANIPULATION INSTRUCTIONS
- Arithmetic and logic
- BCD arithmetic
- Double-precision operations (instructions string two data bytes together as 16-bit word)

### II—DATA-MOVEMENT INSTRUCTIONS
- Uses three pairs of so-called GP registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can perform multiple indexing with these, but takes additional steps compared with classical index-register concept. 8085 has two additional instructions—RIM and SIM—that interface with new serial-I/O pins (as well as interrupt system)

### III—PROGRAM-MANIPULATION INSTR
- Uses stack pointer (SP) to create LI F0 stacks in external RAM for unlimited subroutine nesting
- All GP registers can be incremented and decremented
- Multiple-interrupt capability
- Bus Controls allow addition of DMA

### IV—PROGRAM-STATUS-MANIP INSTR
- Software access to status register

**Specification summary:** Common instruction and data architecture (64k bytes) with optionally separate I/O space (256 bytes). Three 16-bit pointer registers allow efficient addressing of 64k-byte main-memory space. 78 basic instructions with 2-µsec typ add-register-to-accumulator execute time. NMOS technology: 8080A requires 2-phase external clock and ±5V and 12V; 8085A has on-chip clock and needs only 5V. High-speed versions—3-MHz 8080A, 5-MHz 8085A—and CMOS versions also available.

**HARDWARE SUPPORT SOFTWARE**

Most of the vendors of 3rd-party µP development systems have included 8080 development components as a routine part of their catalog. Typically, they use IBM PCs as hosts.

Most of the many companies that supply 8080 development systems also supply the software. Also, many software houses have 8080 software in every conceivable category.

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FAX 415-967-1590

<table>
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<td>TSC430</td>
<td>DUAL, HIGH SPEED ADVANCE DIFFERENTIAL INPUT NOTICE</td>
<td>3.0 A</td>
<td>3 mA</td>
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</table>
It's just a fact of life. Somewhere in the depths of even the simplest embedded microprocessor system design is the risk of a timing-dependent bug. Or two. And not even a million years of conventional testing can catch them all.

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CIRCLE NO 124
Z80

**AVAILABILITY:** Now for 6- and 8-MHz NMOS and CMOS versions.

**COST:** Because of the many aggressive second sources for this most-widely-used part, NMOS prices have dropped to $1 (6 MHz) and less (4 MHz); CMOS volume prices have dropped to $1.70 (6 MHz) and $1.30 (4 MHz), both in high volume.

**SECOND SOURCE:** Sharp, SGS, NEC, Toshiba, and Thomson-Mostek. Toshiba, Sharp, and SGS as well as Zilog have CMOS versions. Additional sources mentioned by Zilog are Gold Star, VLSI Technology, and Rohm.

**Core:** Both Zilog and Hitachi are considering the Z80 µP as an ASIC core in their enhanced versions, the 64180 and the Z280.

**Description:** Superset of widely used 8080/85; adds hardware and software features. Not pin-for-pin compatible with 8080 or 8085, but can use 8080 software and peripherals—though to do so would not take full advantage of Z80 and its peripherals, and might require additional TTL for interfacing.

---

**HARDWARE CHARACTERISTICS SOFTWARE**

![Diagram of Z80 CPU and peripherals](image)

**Notes:**
1. Support chips include peripheral interface (PIO), timer (CTC), serial communications (SIO), and DMA. All provide daisy-chained vectored interrupt for CPU and are being converted to CMOS.
2. Several enhancements of Z80 exist or are imminent. All are in CMOS. The first was the National NSC 800, which we dropped from the market in '86. The second is the Hitachi 64180, to which many Z80 designers are converting. The third is the supplier's Z280, which boosts NMOS prices have dropped to $1.70 (6 MHz) and less (4 MHz); CMOS volume prices have dropped to $1.30 (4 MHz), both in high volume. The Hitachi 64180 seems to be the most popular, but the Zilog Z820 represents the greatest Z80 enhancement. Whatever happens, one thing is certain: The Z80's momentum will probably last for the rest of this century, especially in ASIC core form.

**Specification summary:** Upwardly compatible with 8080A software, but adds 50 instructions, some of which are advance block-move and block-search macros. Instructions executed in 1.6 to 8.8 µsec (3 µsec avg) for 2.5-MHz Z80 and 1.0 to 5.5 µsec (2 µsec avg) for 4-MHz Z80A. 6- and 8-MHz versions also available. User can switch between two identical banks of CPU registers for fast response to interrupts. NMOS circuitry requires single-phase clock and one 5V supply at 60 mA for Z80; 90 mA for Z80A. TTL-compatible I/O and built-in automatic-refresh signals for dynamic RAMs. MIL temperature parts available. CMOS version consumes only 15 mA at 4 MHz and less than 10 µA when in power-down (clock-stopped) mode. Housed in 40-pin DIP. CMOS versions available also in flat pack and PLCC.

**From Zilog:** Zilog has stopped making its PDS and ZDS development systems because there are so many less-expensive third-party support systems for the popular Z80. Instead, it supplies "Z-Scan" emulator boxes that can be used alone or with host computers. Z-Scan-80 that will provide emulation for the 280H ($8695).

**From SGS:** UX-8/22 development system based on CP/M and two 8-in. floppy disks. Package for full-speed in-circuit emulation.

**From others:** Some of the many third parties that supply Z8080 hardware support are Applied Micro, Boston Systems, Emulogic, Hewlett-Packard, Huntsville Microsystems, Nicolet, Orion, Schaia Systems, Tektronix, and Zax. Contact Zilog for addresses.

**From Zilog:** Software for the various development systems. Macroassembler with relocatable assembler, linking loader, file-maintenance programs, and resident Basic, Cobol, C, Fortran, and PLZ (Zilog-created language that comes in "lower" level that mixes assembly- and system-language statements with a "higher" C language). Z800 has cross-software package (assembler, etc) that runs on DEC VAX or Zilog S8000 under Unix.

**From SGS:** Software package for UX-8/22, including debugger, disassembler, and tracer.

**From others:** A lot of software of all sorts, including the popular CP/M operating system (Digital Research) and the MS/X operating system (from Microsoft), which is popular in Japan. Contact Zilog for names and addresses of several dozen others.
**HD64180, Z180**

**AVAILABILITY:** Now for 6- and 8-MHz parts; early '88 for 10-MHz parts.

**COST:** $10 to $13 in 100 qty; $6 to $11 in 1000 qty. $17 for samples of 180-ZTAT.

**SECOND SOURCE:** Zilog is relabeling Hitachi parts as Z180 while it readiness production.

**CORE:** Hitachi considers basic 64180 a standard cell for building high-integration µPs and µCs.

**DESCRIPTION:** Enhancement of Z80 with various peripheral functions such as memory management (to reach larger, 1M-byte, memory space), DMAs, serial ports, modem control signals, etc, added on CPU chip and realized in CMOS. R-suffix versions will have “total” compatibility with Z80-family peripherals chips. Hitachi 641790 with on-chip EPROM represents first 1-chip Z80 µC.

**HARDWARE CHARACTERISTICS**

**HARDWARE**

- **Circuit diagram:** Shows the block diagram of the HD64180, Z180.

- **FUNCTIONS:**
  - **Z80 CPU:** Pipelined and with additional instructions.
  - **DMAC (1,2):** Direct memory access controller.
  - **ASYNC SERIAL PORT:** Allows communication with other devices.
  - **SERIAL PORT:** Data transmission and reception.
  - **MMU:** Memory management unit.
  - **CONTROL BUS:** Interface for controlling other circuits.
  - **ADDRESS BUS:** Path for addressing memory locations.
  - **DATA BUS:** Path for data transfer.

**SOFTWARE**

**SOFTWARE**

- **1—DATA-MANIPULATION INSTRUCTIONS**
  - Unsigned 8×8—16 multiply
  - Nondestructive ANDs for comparing I/O ports, immediate data, and memory to accumulator.

- **II—DATA-MOVEMENT INSTRUCTIONS**
  - Immediately addressed locations
  - Block output to I/O. (Must set up MMU bank registers to translate between 64k of Z80 and 512k external)

- **III—POWER-SAVING INSTRUCTIONS**
  - Sleep command disconnects processor from clock. (Interrupt or reset will reconnect.)

**SPECIFICATION SUMMARY**

- Object-code compatible with Z80 (and 8080, 8085). Pipelined CPU. On-chip MMU generates 19 bits (512k to 1M bytes) external physical address space. 2-channel DMAC (direct-memory-access controller), 2-channel asynchronous serial port, synchronous (clocked) serial port. Can interface to 8080 or 6800/6500 buses (R-suffix versions are matched to Z80-family peripherals). 8-MHz CPU performance now, 10-MHz projected. CMOS 50 mW at 4 MHz with lower power in sleep and halt modes. Packaged in 64-pin DIP and 68-pin PLCC.

**ADDITIONAL INSTRUCTIONS**

- Trap interrupt can be used both for catching undefined op codes and for allowing users to extend instruction set.

**SOFTWARE**

- Microtec Research (Santa Clara, CA) is supplying macroassembler, utilities, Pascal, and C compilers (to run on IBM PC and DEC VAX hosts).
- Also, Avocet (Rockport, ME) and Allen Ashley (Pasadena, CA) have announced IBM PC-based assembler and debugger.
- Hitachi America Ltd (San Jose, CA, 95131) has cross software to go with development hardware (assembler, C compiler, and debugger).

**CONTACT:**

- **American Automation AA 572-64180 real-time in-circuit emulator for use with company's E2-PRO development host.
- **Hewlett-Packard and Tektronix offer support on their development systems and logic analyzers.**
- **Contact suppliers for the many other third parties.**

**SOFTWARE NOTES:**

- Additional 64180 instructions can be treated as macros on a Z80 project for Japanese market.
- American Automation has cross-software to go with development hardware (assembler, C compiler, and debugger). Archimedes (San Francisco, CA) has C compiler ($995 for IBM PC, $3995 for MicroVAX and $5995 for VAX).

**EDN November 26, 1987**
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Hardcover. 200 Pages. 1987. $60.00

Solid-State Microwave Devices offers clear explanations of the materials, theories, and applications of the full range of solid-state devices. Examples involving microwave amplifiers, oscillators, mixers, phase shifters, and more, give you a hands-on feel for effective component design.

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Microwave Integrated Circuit Design Handbook
by Reinmut K. Hoffmann
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Preparing and Delivering Effective Technical Presentations
by David L. Adamy
Hardcover. 165 Pages. 1987. $50.00

Not just another public speaking book, this text focuses on practical ways to help the technical professional prepare easy-to-understand, interesting technical briefings. David L. Adamy, technical, management, and marketing consultant to the military electronics industry, provides practical "inside information" on how to keep your audience awake while making them understand the technical content.

Circle 45 for free 15-day exam

Principles of Electromagnetic Compatibility, 3rd Edition
by Bernhard F. Keiser
Hardcover. 345 Pages. 1987. $60.00

Written for design, test and manufacturing engineers and project managers, this thorough guide gives you step-by-step instruction for eliminating electromagnetic interference (EMI). You’ll discover every aspect of EMI control, including how emission, transmission and susceptibility occur and how to perform the computations needed to solve interference problems. Clear illustrations show you actual interference problems and their solutions without the extensive use of mathematics.

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Filters with Helical and Folded Helical Resonators
by Peter Vizmuller
Hardcover. 115 Pages. 1987. $49.00

Finally, a complete monograph explores the "black art" of helical resonators for radio frequency applications. Filters with Helical and Folded Helical Resonators gives RF engineers, technicians and students hard to find information on these low cost, high efficiency filters. Several proposals show you how to design and build mechanically stable filters that have the right frequency response, don’t drift with temperature, avoid resonance problems and have the lowest insertion loss for a given filter volume.

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Over-the-Horizon Radar
A.A. Kolosov, Editor
Translated by William F. Barton
Hardcover. 332 Pages. 1987. $60.00

This thorough analysis of specific Soviet and U.S. OTH radar systems gives you insight into state-of-the-art, over-the-horizon radar technology and design. The authors’ rigorous treatment of the propagation, path loss, cross section capability, and interference characteristics of OTH radar makes this book indispensable for engineers new to conventional radar or the OTH field.

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High Resolution Radar
by Donald R. Wehner
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With the depth and span of Donald Wehner’s short course, High Resolution Radar offers a unified treatment of the design and analysis of radar systems that depend on spatial resolution. Learn to apply this crucial information with a broad review of basic radar theory, over 200 figures, numerous design examples and problems ending each section.

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The Design of Automatic Control Systems
by Olis Rubin
Hardcover. 450 Pages. 1986. $60.00

Now, one reference helps you develop practical skills for designing quality control systems. Olis Rubin draws illustrative examples from such varied disciplines as radar, mechanics and astrophysics to show you how to translate user requirements into design specifications.

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Lossy Transmission Lines
by Fred E. Gardiol
Hardcover. 475 Pages. 1987. $60.00

Lossy Transmission Lines gives you first-time documentation of the calculator codes for determining transmission on lossy lines. Design engineers—with this book and a programmable calculator, you’ll learn to calculate: the input impedance of a section of lossy line, the corresponding reflection factor and its VSWR, the power absorbed by a linear load, the propagation factor, the characteristic admittance of a line, and more.

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Optimization of Digital Transmission Systems
by K. Trondle and G. Soder
Hardcover. 300 Pages. 1987. $60.00

Digital Transmission Systems describes the most effective criteria for the optimization of digital transmission methods. This career-long reference for design engineers, physicists and students provides detailed explanations of transmitters, transmission media, and receivers, as well as distortion and noise.
Z280

Description: Enhanced Z80 µP, upgraded to the point that it has most of the features of larger 16/32-bit machines. It has “privileged” system-control hardware and associated software for multiuser, multitasking operating systems. It has memory management for virtual memory and incorporates cache to achieve high throughput with moderate-speed external memories.

**HARDWARE CHARACTERISTICS**

**SOFTWARE**

I—DATA-MANIPULATION INSTRUCTIONS
16 x 16 = 256 multiply and 32/16 = 16 divide
Extended block mode manipulates data in blocks. (Can be used with supplier’s Z8070 IEEE floating-point coprocessor)

II—DATA-MOVEMENT INSTRUCTIONS
New addressing modes for more general 16-bit use of Z80’s 16-bit registers (HL, DE, BC pairs)
Instructions to communicate with coprocessors

III—PROGRAM-MANIPULATION INSTR
Jump on auxiliary accumulator/flag
Jump on auxiliary register file in use
System call

IV—PROGRAM-STATUS-MANIP INSTR
New master status register; see category V instructions

V—SYSTEM CONTROL INSTRUCTIONS
New instructions for added system-control registers. These are privileged instructions to permit operating system to define the system configuration upon start-up, to use the new system stack pointer, master status register, and set up the cache’s mode of operation

Software Note: Only those instructions that are enhancements of basic Z80 set are covered. Otherwise, the Z280 is object-code compatible with Z80 (and 8080).

Specification summary: The Z280 upwardly enhanced toward a general-register 16-bit minicomputer. On-chip memory management to address as much as 16M bytes of external memory. CPU is 3-stage pipelined with on-chip 256-byte program and data cache to automatically keep recently used instruction on chip for fast—to 2 MIPS—execution at 10-MHz internal bus clock. Planned mask shrink from initial 2-µm geometry to 1.5 µm is expected to allow 25-MHz clock. Future mask improvements are expected to allow speeds to 50 MHz. The I/O is pin programmable to match either 8-bit Z80 bus or 16-bit “universal” bus. Also included on chip are four 16-bit timer/counters, four DMA channel controllers, dynamic memory refresh control, and a serial UART port. Fabricated in static CMOS and housed in 68-pin PCC package; other options planned for future as requested by customers.

Hardware Notes:
1. Diagram indicates how basic Z80 CPU has been enhanced by adding other functions to the chip. Not so apparent are other enhancements to the Z80 CPU, such as more powerful, generalized 16-bit data and addressing operations.
2. Zilog says the integration not only lowers system cost but provides a speed advantage. When all subsystems are on chip, the system speed automatically increases.

Software Note: Source code for target resident Z280 debug monitor may be purchased for minimal charge. Otherwise Zilog is not planning software support.

From Zilog: Source code for target resident Z280 debug monitor may be purchased for minimal charge. Otherwise Zilog is not planning software support.

From others: 2500AD ((303) 369-5001) is shipping a crossassembler and is working on a C compiler. Rastek is considering a PC-based C compiler.

Note: It’s possible that software houses such as Digital Research and Microsoft—both of whom have been associated with Z80 software—have had Z280 projects on hold: Digital through its well-known CP/M operating system for 8080s and 286s, and Microsoft through its work in developing MSX, the multiuser enhancement of CP/M for some Japanese companies.

EDN November 26, 1987
8-BIT NMOS AND CMOS

Motorola Microprocessor Products Group
6501 W Wynn Canyon Dr
Austin, TX 78735-8598
Phone (512) 440-2000

Status: Introduced in 1974, the 6800 has been the foundation of one of the longest lived and broadest µP families of all. Among its progeny must be included the 6800 but its covered here and the following Motorola µPs and µCs, which are described elsewhere in this directory: the 6804, 6805, 6801, and 68HC11. The 6800 itself is now way past its prime and is not recommended; we retain it in the directory for reference. But the new 6802 and 6809 continue to be shipped in volume. Dataquest showed nearly 4 million units for the 6802 and nearly 3 million units for the 6809 in '86. That gave the family 3rd place (12% share of market) behind the Z80 and 8080 families, but just barely ahead of the 8088. For new designs, Motorola steers designers either upwards to 32-bit 68000 family (68008 has 8-bit bus) or downwards to 1-chip 68HC11.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS Arithmetic and logic
Instructions to take advantage of two accumulators
6809 has unsigned 8 x 8 multiply with 16-bit product
II—DATA-MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions
6809 can use four index registers for merging three source blocks into one destination block
Can autoncrement and autodecrement by one or two directly and indirectly. (Page zero can be software relocated during program execution, effectively increasing its size)
Indexing uses the "true indexing" relationship between base and offset (0, 5, 8, 16 bits) rather than the 6800 relationship
Can utilize the user stack for Polish-notation operations or interpretive language
III—PROGRAM-MANIPULATION INSTR
Has PDP-11-type branches and conditional branches. Unlimited subroutine nesting via stack pointer addressing LIPO stacks in RAM
Does not have vectored interrupt, but can achieve function with software (or with 6828 priority interrupt controller)
6809 has extensive relative addressing with wide reach, which allows creation of position-independent code and opens door to use of off-the-shelf, mass-produced standard firmware in ROMs
IV—PROGRAM-STATUS-MANIP INSTR
6809 has instructions for manipulating the status register (condition-code register). It may be transferred or exchanged with any 8-bit register, or pushed or pulled on either stack; any number of flag bits may be set or cleared in one instruction
IV—POWER-SAVING INSTRUCTIONS
6309 has SYNC and CWAI to put CMOS CPU in sleep mode. Sync instruction stops µP until it gets go-ahead signal from interrupt line

Specification summary for 6800: Common-memory architecture with 16-bit (64K-byte) memory space for instructions, data, and I/O; all data 8 bits wide. Instruction set patterned after the PDP-11 mini as closely as possible in shorter word machine with limited CPU registers. Execution times from 2 to 5 µsec. NMOS silicon-gate depletion-mode circuitry requires one 5V supply, 500 mA, housed in 40-pin DIP. Versions with -55 to +125°C range also available.

Specification summary for 6809: An 8-bit machine with extensive 16-bit addressing capability. Has two 16-bit index registers and a 16-bit user stack pointer that can also be software-specified as a third index register. Upwardly compatible with 6800, but only at source-code level. Bus operates at 2 MHz, so basic speed is similar to that of 6800, but greater efficiency of 16-bit addressing significantly increases throughput. Instruction set has 59 mnemonic and seven addressing selections for a total of 1464 instruction-addressing options. Instructions vary in length from 1 to 5 bytes, with register-inherent operations executing in 1 µsec at 2-MHz bus speed (320-nsec memory access). Longest instruction takes 20 cycles. The 6800 direct or page zero register is retained but can be software relocated anywhere in memory via programmable register. Motorola "HMOS" depletion-mode load circuitry with one 5V supply. Two versions, each in 40-pin DIP.

SOFTWARE

From Motorola: Software can be obtained free for downloading over phone lines by calling (512) 440-3733. The basic assemblers and other tools are for IBM PC.

From others: Tektronix, GenRad/FutureData, and Hewlett-Packard development systems support the 6800. Micro Industries (Westerville, OH) says it has acquired an exclusive license to Motorola "Micromodule" 8-bit boards.
Now you have three low-cost choices in Tek digital storage oscilloscopes. All featuring powerful 20 MS/s digitizing along with familiar, full-bandwidth analog operation. It's the best of both worlds in one easy-to-use, portable package.

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### 650X, 65COX

**AVAILABILITY:** Now for NMOS and CMOS, 4 to 6 MHz.

**COST:** The prices for both NMOS and CMOS were said to have dropped to less than $1. However “legitimate” US price said to be $2 to $3 for NMOS and twice that for CMOS.

**SECOND SOURCE:** Rockwell, California Micro Devices, NCR, and WDC. WDC (Western Design Center) has been creator of some of the CMOS designs, which have licensed widely around world (UMC in Taiwan, TIT-Intermetall in West Germany, etc), which is one explanation why second sources have proliferated.

**CORE:** NCR has pioneered the use of 6502 as semicustom core. Many of above sources also specify it as part of their cell libraries, as does SMC (Hauppauge, NY).

**Description:** Original design team’s goal was to achieve as much PDP-11-style addressing capability as would fit in an economical 138 x 151-mil chip. Because of the μP’s short 8-bit index register, it is optimally suited only to applications requiring access of smaller blocks of memory (although it benchmarks ahead of most other 8-bit μPs with respect to its speed of execution of high-level languages such as Basic and Pascal). New CMOS parts also have small economical die (70 x 52 mil) that gets still smaller with today’s finer geometries. See 6500/1 for 1-chip versions and 65SCB16/802 for 16-bit internal version.

**Notes on CMOS versions:**
1. CMOS 65CCX family members are slight enhancements of NMOS counterparts and can serve as plug-in replacements.
2. Among hardware enhancements are new 4-phase clock that gives decreased memory access time and a memory-lock (ML) output and bus-enable (BE) input that simplify multiprocessor designs. Also RDY in write as well as read and 5-state buses.
3. Among the software enhancements are the treating of all unused op codes as NOPs and removing the page-boundary restrictions on JMP indirect.
4. Decimal mode is automatically set off upon reset or interrupt, and the N, V, and Z flags are made active during decimal mode.
5. A BRK followed by interrupt is executed.
6. See instruction set for comments on new instructions.

### HARDWARE CHARACTERISTICS

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### 8-BIT NMOS AND CMOS

**Status:** The falling share of market for this μP (about 5% or between 2M and 3M units in ’86), according to Dataquest, would appear to indicate that it has reached the end of its lifecycle. However the architecture lives on in the form of 1-chip versions (see 6500/1 and especially the 50740) and ASIC versions. Some of these have very large unit volumes, so the 6502 architecture may remain, if only in-in-the world. The small die size of the 6502 core has lead one supplier, WDC, to explore GaAs versions for greatly increased speed.

### SOFTWARE

**SPECIFICATION SUMMARY:** Common-memory architecture with instructions, data, and I/O in same 64k-byte space; 57 instructions (68 for CMOS) execute in 3 µsec typ at 1 MHz, 1.5 µsec typ at 2 MHz. Many instructions provide choice of 13 PDP-11-type addressing modes (15 for CMOS). Advanced indexed-indirect addressing mode. NMOS and CMOS silicon-gate, depletion-mode circuitry requires one 5V, 250-mV supply. Some CMOS parts can run at 4-MHz clock (250 nsec/cycle). CMOS parts require 4 mA/MHz for operating and 10 µW standby (0 Hz).

**FROM ROCKWELL:** Cross software for Intel ISIS-II and personal development system. ($250). Support (in firmware) for assembly ($35), monitor ($65), Basic ($165), PLI/65 ($85), Fortran ($65), Pascal—“instant” ($100), math package ($35), and disk operating system ($50).

**FROM WESTERN DESIGN CENTER:** Emulation and test software is part of Tool Box.

**FROM CALIFORNIA MICRO DEVICES:** 65SC00 macroassembler for Apple Computer ($100), assembler for Intel ISIS ($1800), and Fortran assembler ($1800).

**FROM NCR:** Monitor for use in conjunction with emulator. Supports breakpoint, change memory and registers, software trace and real-time execution, etc.

**FROM OTHERS:** Because the 6500 has been so widely used, there are innumerable sources of software at different language levels; for example, the ORCA Series of macroassemblers and utilities from Byte Works (Albuquerque, NM, (505) 898-8183).
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EDN November 26, 1987

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65C816/65C802

**AVAILABILITY:** Now for 2-, 4-, 6-, and 8-MHz parts.

**COST:** In 100 qty, plastic, $20 for 816 and 802.

**SECOND SOURCE:** VLSI and California Micro Devices said to be main sources, but WDC says it has licensed others in US and abroad. (Mitsubishi says it will be doing a version of its 50740 6502-based 1-chip device that will also have a 16-bit internal architecture.)

**CORE:** All suppliers are considering this as µP megacell in their libraries, but WDC has most commitment to its ASIC use.

**802** is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The 816 has a different pinout but expands the addressing range of the 6502 from 64K to 16M bytes. Additional hardware enhancements on the 816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

**Description:** CMOS 8/16-bit µPs featuring software compatibility with 8-bit 6502 (both original NMOS 6502 and enhanced CMOS 65C02). The 802 is pin-for-pin compatible with the 6502, so it can be plugged into existing sockets. The 816 has a different pinout but expands the addressing range of the 6502 from 64K to 16M bytes. Additional hardware enhancements on the 816 allow it to be used for multiprocessor systems and in systems that have data and program caches.

**Hardware Notes:**
1. Compare diagram with previous 6502/65SC02 (elsewhere in directory) to see nature of architectural enhancements. The 8-bit registers have been widened to 16 bits and the 16-bit registers widened to 24 bits.
2. The new control-bus outputs on the 816 facilitate multiprocessing, caching, and virtual memory.
3. The new control-bus outputs on the 816 allow you to abort instructions for virtual memory and to control bus access.
4. Apple is said to have had to resort to special semicustom chips to allow the Apple IIGS to operate efficiently and at full system-level speed.

**SOFTWARE**

**Status:** Apple's use of the 65C816 in the IIGS upgrade of the widely used Apple computer provides a firm basis for hardware and software availability. The volume of devices shipped in Q4 was about 70,000 (according to VLSI), with some 80% going to Apple and only a disappointingly small amount to other users. EDN estimates that, depending on Apple's year-end IIGS sales, the volume in Q1 might reach 100,000. The software support is growing as third-party houses that have supported the Apple 6502-based Apples convert software to take advantage of the expanded memory and other capabilities of the 65C816. One indication of breadth of software support is Byte Works's claim that it has delivered several hundred of its ORCA/M tools for software development.

**Software Notes:**
1. Upon reset, 802 and 816 are in 6502 emulation mode. To go to native (enhanced) mode, the E bit must be reset to 0 via an exchange with previously reset carry bit in status register.
2. Full-sized 16-bit registers reported to facilitate high-level-language compiler writing as compared with 6502. The 16-bit index registers and the 16-bit stack pointer with no page-1 confinement help. Further, the more sophisticated stack-pointer addressing modes directly serve needs of compiler writers.
3. Tendency of new native (enhanced) mode coding to become trickier than 6502, because of tightly packed architecture (all 256 op codes used) and opportunity to flip back and forth dynamically between modes and between register and data widths.

**Specification summary:** Enhanced 6502 with 16-bit internal data option and 24-bit addressing option, software selectable. Data I/O off chip remains 8 bits, however. The 802 version is hardware compatible with 6502 (or 65SC02) and can be plug-in replacement. It will reset into 6502 emulation mode but can be software switched into varying degrees of 16-bit operation. The 816 version is almost identical internally to 802, but it has different pinouts because it brings the additional bits for 24-bit addressing space out of the multiplexed 8-bit data bus, and it has special control lines to facilitate virtual memory, coprocessors, and data and program caching. Performance is mostly identical to 6502 of same clock speed, except that extended addressing and data modes take additional cycles. Clock to 8 MHz. Fabricated in 2.4-µm and 1.5-µm CMOS and specs 5-mA/MHz power consumption with 1 µA standby.

---

**From Western Design Center:** The Tool Box in-system emulator for real-time emulation of 802/816 parts. WDC bases its development systems on the Apple computers, now favoring the new Apple IIGS computer. It is also extending its range of tools to include actual ASIC design capability so that users can use 6502 65C816 cores and apply their own custom I/O combinations around core. WDC's prices range from $3000 to $5000.

**From California Micro Devices:** Prototyping board for 816. 

**From Microtek Lab Inc (Gardena, CA):** In-circuit emulation.

**From Dynatemp (Irvine, CA):** RME-1600 board with 65C816.

**From Apple (Cupertino, CA):** The Apple IIGS personal computer ($700 to $1300) for use as development platform because it uses 65C816.

---

**From Byte Works (Albuquerque, NM, (505) 898-8183):** The ORCA/M crossassemblies and utility package ($99.95 on Apple ile under ProDOS, $69.95 on Apple IIGS under ProDOS-16). Also ORCA/Pascal compiler ($125), Basic interpreter and compiler (1st qtr '86).

**From Apple (Cupertino, CA):** Assembler and debugger ($100) and C compiler.

**From others:** Some 50 programs are said to have been written for Apple IIGS, although in many instances, as much emphasis is placed on using the new graphics of the IIGS as on the expanded memory and other features of the 65C816.
8096 FAMILY

AVAILABILITY: NMOS 8x9x in production with both an 8- and 16-bit bus option. The EPROM version is also available. The higher-performance CMOS version 80C196 is now in production.

COST: Less than $8 in 10k qty.

SECOND SOURCE: Signetics/Philips.

Description: Highly integrated 16-bit microcontroller combining 16-bit CPU with extensive I/O handling. On-chip memory includes 8k bytes of ROM and 232 bytes of register-file RAM. I/O capabilities include an 8-channel, 10-bit ADC, full-duplex UART, 8-level priority interrupt, pulse-width-modulated output, high-speed pulsed I/O, four 16-bit software timers, five 8-bit I/O ports, and a watchdog timer.

Hardware Notes:
1. The initial NMOS 8096 family consists of three parts—8096 through 8097—that come with or without A/D converters (and S/H circuits) and onboard ROM, and with either 48 I/O lines (68-pin package) or 32 I/O lines (40-pin package). They have option of either 8- or 16-bit system bus. The 8k-byte EPROM version has onboard programming capability and read/write selectivity.
2. New CMOS version 80C196 has 2 x NMOS performance.
3. Four high-speed trigger inputs record times at which external events occur. Storage in 8-deep FIFO.
4. Six high-speed pulse outputs can trigger external events at preset times. Commands are stored in 8-deep content-addressable memory. Output section can concurrently run as many as four software timers simultaneously.
5. 16-bit watchdog timer allows recovery from hardware or software error.

16-BIT NMOS AND CMOS

Intel Corp
Embedded Controller Operation (ECO) Marketing
5000 W Chandler Blvd
Chandler, AZ 85226
Phone (602) 961-8051

Status: According to Dataquest figures, this earliest of the 16-bit µCs continues to have top share of 16-bit µC (microcontroller) market in '86 with 269,000 units. However, because that market is still young, it's too early to tell whether this will be another case of Intel dominance. The only other 16-bit µC shown with any volume was the Thomson-Mostek 68020, but it has again dropped out of the picture (following the Thomson-SGS merger). Meanwhile, the National 16040 HPC and NEC 783XX (78312), which are newer designs, are being aggressively marketed and could pose threats. Actually, with the advent of the ASIC approach, the definition of this market is blurring; for now, any µC that is in common form in an ASIC library could have memory added and become a "µC," even Intel's own 80188/80186s.

† — DATA-MANIPULATION INSTRUCTIONS
8- and 16-bit signed and unsigned arithmetic in binary, including multiply and divide
Logicals
Bit, byte, word, and double-word operations
II — DATA-MOVEMENT INSTRUCTIONS
Addressing modes include Direct, Immediate, Indirect, Indexed, and Indirect with Autocrement
Load and store, push and pop
III—PROGRAM-MANIPULATION INSTR
Has calls, jumps, and returns
Conditional jumps upon Boolean functions of flags within
±128 bytes of instruction
Iteration control of loops
IV—PROGRAM-STATUS-MANIP INSTR
Zero, sign, overflow, carry, overflow trap, interrupt enable, sticky bit
(records previous value of carry during right shifts)
Can set and clear some bits

Specification summary: 16-bit µC with split-memory architecture and 8k-byte ROM and 232 bytes of register-file RAM on chip. External memory expandable to 64k bytes, with data bus dynamically programmable as 8 or 16 bits. Register-to-register architecture with ALU operating directly on register file. Has 8-channel, 10-bit A/D converter, four 16-bit software timers, PWM output, five 8-bit I/O ports, full-duplex serial port and high-speed pulse I/O ports. At 12-MHz clock, 16-bit addition takes 1 µsec, 16 x 16 multiply or 32/16 divide takes 6.5 µsec. Average instruction-execution time equals 1 to 2 µsec. New CMOS parts have 2 x performance of NMOS. In 48-pin DIP, 68-pin PLCC or 68-pin pin-grid array.

HARDWARE CHARACTERISTICS SOFTWARE

From Intel: Low-cost development kit ($2695) includes ISBE-96 emulator board and ASM-96 macroassembler and runs on IBM PC host as well as Intellec Series III and IV. Real-time emulation to 12 MHz. VLSICE-96 advanced emulator provides real-time emulation to 12 MHz and is hosted on IBM PC as well as Intellec Series III and IV. Programming support for EPROM versions supplied through Intel's line of universal PROM programmers.

From Intel: Macroassembler (ASM-96) and software simulator available along with PL/M-96 and C-96 compilers. Each software package includes relocation/linkage utility, library creation utility, and FPAL-96, a 32-bit floating-point utility. Software runs on IBM PC and Intellec Series III/IV and is priced at $750 for single-user license.

From Archimedes (San Francisco, CA): ANSI C-8096 compiler with additional features like control of interrupt. Hosted on IBM PC ($995), MicroVAX ($3995), and VAX ($5995).

From Cybernetic Micro Systems (San Gregorio, CA): Graphic programming and simulation aids that run on IBM PC ($295 and $995).
HPC 16040/83

**AVAILABILITY:** Now for 17- and 30-MHz parts.

**COST:** Less than $10 in volume.

**SECOND SOURCE:** To be announced.

**CORE:** Will be standard cell in supplier's ASIC library.

Description: 16-bit CMOS microcontroller family with basic version having 8k bytes of onboard ROM, 256 bytes of RAM, extensive I/O, and onboard peripherals. Original 16040 has 16.8-MHz clock with 240-nsec register instruction execution. Due to shrinking, new 16083 samples achieve 30-MHz clock rates, with shortest instructions just 134 nsec, over −55 to +125°C. Supplier says HPC stands for "high-performance microcontroller."

**HARDWARE CHARACTERISTICS SOFTWARE**

I—DATA-MANIPULATION INSTRUCTIONS

8- and 16-bit arithmetic in binary, including multiply and divide with 32-bit results

Logical AND, OR, XOR, and compares

Bit manipulation of all registers and through all 64k address space

II—MOVEMENT INSTRUCTIONS

10 addressing modes: register B indirect, register X indirect, direct, indirect, indexed, immediate, register indirect with autoincrement/decrement, register indirect with autoincrement, and skip

Instructions include load, store, push, pop, and exchange

III—PROGRAM-MANIPULATION INSTRUCTIONS

Calls, jumps, returns, and conditional jumps implementing high-level-type constructs

IV PROGRAM-STATUS-MANIPULATION INSTRUCTIONS

There is a carry bit and several status registers. These may be manipulated as all bits in register space, and in 64k address space may be set, reset, and tested

Specification summary: 16-bit CMOS µC and µP with memory-mapped architecture and 8k-byte ROM and 256-byte RAM on chip. External memory expandable to 64k bytes. 16-bit-wide architecture includes data bus, ALU, and registers. Has eight programmable 16-bit timers, eight vectored interrupts, full-duplex UART with programmable baud rate, PWM outputs, 10 timer-synchronous outputs, four input capture registers, 52 general-purpose I/O lines. Performance of 1640 at 16.8-MHz clock is 240 nsec for register operations and 7 µsec for 16 x 16 multiply and 32/16 divide. Performance of 16083 at 30 MHz is 134 nsec. Supplier says its "microCMOS" process will provide low 20-mA power consumption. Idle instruction is expected to reduce this to 2 mA, and halt instruction will drop it to 20 µA. Supply range is 3 to 5.5V. Available in industrial (−40 to +85°C) and extended (−55 to +125°C) temperature ranges (MIL-STD-883 in 1 qtr '88). In 68-pin PCC, LCC, and 68-pin PGA.

Notes:

1. Family is designed around common µP core for instruction-set consistency, with various models having various assortments of on-chip peripheral functions. Onboard peripheral functions planned are ADCs, gate arrays for customization, dual-port RAMs for efficient interprocessor communication (download/uploading), and EEPRoms. Also planned are HDLC, CRT, DMA, SCSI, and Ethernet controllers.

2. Microwire/Plus is used for synchronous serial data communications with supplier's Microwire peripherals (ADCs, display drivers, EEPRoms), COPs 4-bit µCs, 8050 8-bit µCs, and other HPCs for multiprocessing.

3. Watchdog logic monitors operations and signals upon the occurrence of any illegal activity such as infinite loops.

4. Halt and idle modes provide additional power savings by stopping clock or disconnecting it.

5. Emulator parts for 16040/B3 and port-expansion-and-recreation logic (Pearl) available.

6. UPI (Universal Peripheral Interface) port for connecting to µPs such as National's 32000 family.

HARDWARE SUPPORT SOFTWARE

Supplier's Mole (microcomputer on-line emulator) is a low-cost ($4590) development system for the HPC family. Mole consists of brain board and HPC personality board and optional software. The brain board is common to all National µCs. The personality boards tailor the system to emulate particular µCs. Moles can be used in conjunction with various hosts like IBM PC/XT/ATs or VAXs (Unix/VMS).

Crossassembler and C compiler to run on IBM PC. VAX (Unix/VMS) support will be available 1 qtr '88. Symbol debugger will also be available at that time. Floating-point math and general math packages are currently available.

Dial-A-Helper is a 24-hr on-line computer bulletin board serviced by National. It provides latest information on all National µCs chips (including development systems) and also specific application support. Phone (408) 739-1162.
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CIRCLE NO 145

EDN November 26, 1987
783XX

AVAILABILITY: Now for ROMless, masked ROM, and EPROM versions of 78312 (see also note 3).

COST: 10k qty, $12.50; expected to go under $10.

SECOND SOURCE: None yet.

CORE: As with many of the one-chip sets, supplier has been using cell-library concepts in house all along.

Description: Intended for high-end controller-type applications, 783XX combines a fairly fast, powerful, 16-bit ALU with many peripheral functions on single chip. Although there’s some architectural resemblance to supplier’s existing 7811 (see Note 3) and new V Series (especially V25), this is said to be an original design with its own unique instruction set.

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HARDWARE

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CHARACTERISTICS

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SOFTWARE

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I—DATA-MANIPULATION INSTRUCTIONS

Most operations 8 and 16 bit, including adds and subtracts, shifts and rotates, decimal adjust, and increment and decrement

Multiply 8 x 8 in 3.0μsec and 16 x 16 in 3.167 μsec

Divide 16/8 in 3.0μsec and 32/16 in 8.333 μsec

II—DATA-MOVEMENT INSTRUCTIONS

Addressing modes include immediate, register-register, indirect (including base and base-index), and direct (including direct-indexed). Direct addressing of internal RAM can accommodate 8 or 16 bits. (Although external data is restricted to 8 bits, internal RAM can be addressed on an 8- or 16-bit basis)

III—PROGRAM-MANIPULATION INSTR

Call, call table (1-byte call), branch, branch relative, branch register, branch register indirect, branch on condition, branch on bit, software break, return, return from interrupt

IV—PROGRAM-STATUS-MANIP INSTR

Enable and disable interrupts, break with context switch, select register bank, increment/decrement stack pointer. Software control of standby modes, watchdog timer, and on-chip peripherals

Specification summary: A new high-performance, single-chip architecture that features eight switchable register banks to handle demands of real-time control. This CMOS processor uses IEEE standard mnemonics. The 12-MHz (max frequency) oscillator is divided by 2 to create a 6.0-nsec system clock. Min instruction time is 500 nsec. A 3-byte instruction prefetch queue further speeds processing. Chip can access 64k bytes of memory, including 8k bytes of on-chip ROM, 256 bytes of on-chip RAM, and a 256-byte special-function register area that communicates with on-chip and off-chip peripherals. On-chip peripherals include a 4-channel 8-bit A/D converter, a full-duplex UART, and an extensive timer/counter system. There are two 16-bit up/down counters, two PWM outputs, a 16-bit timebase counter, and a free-running counter with two 16-bit capture registers. The 48 I/O lines include two, 4-bit, real-time output ports. There are four external interrupt lines and 11 internal interrupt sources. Eight macroservice channels can perform DMA in response to various interrupt sources. The CMOS device is housed in 64-pin flat pack, shrink DIP, and PLCC.

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HARDWARE

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SUPPORT

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SOFTWARE

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From NEC: Supported on the NEC MD-086 CP/M-86-based development system. An emulation board, the IE-78310-R, hooks up to IBM PC and other popular computers. Evaluation package consisting of board with monitor, relocatable assembler, and software examples ($150).

From Orion (Redwood City, CA): Emulator.

From third-parties: C compiler from Lattice. Forth interpreter under development.
V SERIES

DESCRIPTION:
Parts with numbers to 50 are stretched versions of Intel 8086 family. They obtain increased performance via such enhancements as dual internal 16-bit data buses, dedicated hardware for address generation, loop counters for block transfers, 16/32-bit temporary registers/shiflers for fast multiplication and division, and a prefetch register. Some parts can even do 8-bit 8080 instructions in an emulation mode. The 32-bit V60 and V70 are not really continuations of the same family as they aren't patterned after 8086 family. They are said to be derivatives of a 36-bit mainframe computer NEC has been doing for some time.

COST: In 100 qty, $6 for V20, $8 for V30, $17 for V40, $13 for V50, and $400 for V60 (16 MHz). V70 expected to be $500 to $600. Samples 4 qtr '87 with production 1 qtr '88.

AVAILABILITY: V20, V25, V30, V50, and V60 now. V70, engineering derivatives of a 32-bit mainframe computer NEC has been doing for the family for they aren't patterned after 8086 family. They are said to be

HARDWARE CHARACTERISTICS SOFTWARE

---HARDWARE---CHARACTERISTICS---SOFTWARE---

Notes:
1. Diagram shows V20 and V30, which have enhanced 8086/8088 architectures.
2. V25 is a controller-type µC with some on-chip memory.
3. V40 V60 and V70 are 32-bit µPs. Three of them can run same code redundantly with majority-vote scheme for systems that demand greater reliability.

SPECIFICATION SUMMARY: 16-bit CPU with dual-bus internal architecture and dedicated addressing hardware can reach 1M-byte memory locations. Multiplication and division take 6 to 8 µsec at 5-MHz clock rate. Data-block transfer rate to 625k bytes/sec at 5-MHz clock rate. Implemented in 2-µm CMOS, devices dissipate 500 mW max at 5 MHz, 50 mW in standby, and operate over -40 to +85°C. Housed in 40-pin DIP, which is pin-for-pin compatible with 8088 (V20) and 8086 (V30). The V25, V40, and V50 chips are in 1.6-µm CMOS, initially with 8-MHz clocks. They are available in 68-pin PGA, 68-pin PLCC, and 80-pin miniflat pack. The V60 and V70 are from a different 32-bit architectural origin. They have a more general-register orientation, but they can also run 8086 code, by emulation (via on-chip hardware). The V60 at 16 MHz performs 3 MIPS max, ½ MIPS sustained; 20-MHz V70 performs ½ MIPS max, ½ sustained. Table see synopsis of family features.

HARDWARE SUPPORT

IE 70000 Series family of in-circuit emulators for whole family ($7000 to $14,000). Can be hosted by PC/AT or VAX. Third-party hardware available from 2ax and Sophia Systems.

SOFTWARE

COMPATIBLE CROSS SOFTWARE FOR IBM PC, Intel Intellec; Series III development systems, VAX minicomputers for both VMS and Unix. NEC is working to make family compatible with Japanese Tron real-time operating systems. Third-party software from Intermetrics (Cambridge, MA), Digital Research (Monterey, CA), Microtec Research (Santa Clara, CA), and Systems & Software (San Diego, CA).
New Airpax Series 6600 thermostats are specially designed to be compatible with all automated production techniques common to PC board manufacturing. They can be installed with DIP auto-insertion equipment. They are sealed to withstand wave soldering and washing operations. And they provide both sensing and switching in a single space-saving device. Best of all, the Series 6600 combines production expediency with proven accuracy and reliability. Bimetallic snap-acting thermostats, the Series 6600 feature fast, positive response and excellent repeatability with 1 amp switching capability over a temperature range of 40°C (104°F) to 120°C (248°F). To ensure performance, the temperature is factory pre-set, and cannot be altered in the field. Add automated thermostat installation to your PC board production line. Call us today for configuration availability and further details. Airpax Corporation, Frederick Division, Husky Park, Frederick, MD 21701. (301) 663-5141.
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EDN November 26, 1987
8086/8088, 80186/80188

**AVAILABILITY:** Now for both NMOS and CMOS 8086/88. Now for 8-, 10-, and 12.5-MHz 80186. Now for 6-, 8-, and 10-MHz 80188. Now for 12.5-MHz 80C186 (16 MHz 1st qty '88).

**COST:** At 100 qty, under $5 for 8086/88; under $10 for 80186/188 in PLCC; $18 for 80C186 in 1k qty.

**SECOND SOURCE:** For 8086/8088: AMD, Harris, Matra-Harris, Fujitsu, Siemens, OKI. For 80186/8188: AMD, Fujitsu, Siemens.

**CORE:** Intel's ASIC group says it will be incorporating 80C186 in its cell library in mid-'88.

**Description:** Supplier's objective when 8086 was introduced back in '78 was to offer machine that matched performance of latest mid-range minis but retained some upward compatibility with widely used 8080/85. 8086 is intended as highest performance 8-bit µP. Floating-point math functions added on CPU chip, somewhat in anticipation of ASIC standard-cell trend (and Intel plans to add 8086 family members to its ASIC cell library in mid-'88 to give customers chance to design their own higher-integration combinations). The 80286 and 80386 (see separate directory entries) are more advanced members of family.

**8/16-BIT, 16-BIT NMOS AND CMOS**

**Status:** Next to the 8080/280 family group, the 8086 family has been the most successful µP family. Based on Dataquest '86 figures, the devices on this page had 60% of the market. If you also include the NEC V Series lookalikes and the 80286 enhancements and the new 80386 32-bit version, the 8086 architecture has gained 80% of the 16-bit-and-above µP market. The most visible application for the family has been in the IBM PC and its many clones. The 80186/88 high-integration versions covered here were intended for PC applications, but the 80186/88 never caught on with PC makers. Now that new designs for the PC market have switched to the 80286 and 80386, Intel is redirecting the 80186/88 at embedded applications, and is claiming success—2000 design wins for 80186 and 50 design wins for new 80C186.

**Notes:**

1. Enhanced CPU in 80186/188 includes new instructions: Pusha, Popa, Pendrel, instruction prefetch, the program counter can be ahead of BIU's instruction prefetch, the program counter can be ahead of itself

2. Enhanced CPU in 80186/188 includes new instructions: Pusha, Popa, Pendrel, instruction prefetch, the program counter can be ahead of BIU's instruction prefetch, the program counter can be ahead of itself

**Specifications**

| Specification summary for 8086/88: | 16-bit CPU that can reach 1M byte using "segment" address-extension registers. Register-to-register operations execute at 0.6 µsec with 5-MHz clock (0.37 µsec with 8-MHz clock). HMOS ion-implanted, depletion-load, silicon-gate circuitry requires 5V at 340 mA (substrate bias generated on chip). In 40-pin DIP, device is pin programmed to switch 8 pins from minimum to maximum external system mode. Harris CMOS 8066 dissipates only 10 mA/MHz when running, and clock can be reduced to 500 µA standby. |
| Specification summary for 80186/188: | Highly integrated µPs that combine functions of most common APX 6 system components onto one chip. Have same memory reach as 8086/88 but with improved execution times on some instructions. HMOS II ion-implanted, depletion-load, silicon-gate circuitry requires 5V at 300 mA (90 mA and less for CMOS). Housed in 68-pin JEDEC Type A ceramic leaderless chip carrier and a ceramic pin-grid array. Plastic leaded chip carrier also. |

**Hardware**

8086/8088, 80186/80188

- **AVAILABILITY:** Now for both NMOS and CMOS 8086/88. Now for 8-, 10-, and 12.5-MHz 80186. Now for 6-, 8-, and 10-MHz 80188. Now for 12.5-MHz 80C186 (16 MHz 1st qty '88).

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- **Hardware**

From Intel: ICE in-circuit emulator ($7995) supports 8086/8088 and 80186/8188 to 10 MHz. Emulators are hosted on IBM PC and Intelteck Series III/IV development systems. ICE186 in-circuit emulator ($995) supports 80C186 at 12.5 MHz.

From others: Because of popularity, family is widely supported by 3rd-party universal development systems, such as those from American Microsystems (Beaverton, OR).
**80286**

**AVAILABILITY:** In production with 6, 8, 10, 12.5 and 16 MHz (AMD for 16 MHz). CMOS 80C286 12.5 MHz in production and 20 MHz sampling.

**COST:** In 100 qty: $30 for 8 MHz, $40 for 10 MHz, $100 for 12.5 MHz, and $150 for 16 MHz in LCCs (PGAs more). For 80C286: $125 for 10 MHz and to $170 for 16 MHz, also in 100 qty.

**SECOND SOURCE:** AMD, Siemens, and Fujitsu. Harris for CMOS 80C286.

**Description:** An evolutionary extension of the 8086 with special capabilities for multitasking systems. Has on-chip memory-management and protection functions that support intertask isolation, program and data security, and 4 levels of privilege within a task. Memory management supports as much as 1G bytes of virtual-address space per task, mapped into a 16M-byte physical memory. Device is upward compatible with 8086/88 software.

**HARDWARE CHARACTERISTICS**

**SOFTWARE**

---

**DATA-MANIPULATION INSTRUCTIONS**

8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.

**DATA-MOVEMENT INSTRUCTIONS**

Addressing modes include literal, relative (to register and to segment), register, base plus index, base relative indexed, and register indirect.

Programmers can manipulate 16,383 segments in memory by means of memory-base descriptor tables and 4 segment registers. These segments can be between 1k and 64k bytes in length.

**PROGRAM-MANIPULATION INSTR**

Has calls, jumps, and returns within the same protection level, across protection boundaries, and between tasks.

Intrasegment calls and jumps use self-relative displacement for position-independent code.

Intersegment calls and jumps use the memory-based descriptor tables to provide position-independence of code.

Conditional jumps upon Boolean functions of flags within ±128 bytes of instruction.

Iteration control of loops.

String instructions, including repeat, for rapid iteration.

**PROGRAM-STATUS-MANIP INSTR**

8086 flags (carry, auxiliary carry, parity, zero, and sign) plus overflow, interrupt enable, direction (strings), trap (single-step), I/O privilege level, and nested task. Flag register is software accessible.

**Notes:**

1. Has high-level-language support instructions.
2. Virtual-address translation, memory management, and protection performed by CPU for faster execution.
3. Trusted instructions can only be executed at highest protection levels.

**Specification summary:** 16-bit CPU with 1G-byte virtual-address space per user, mapped onto 16M-byte physical-address space. Bus cycles execute in 250 nsec at 8-MHz clock (200 nsec at 10 MHz), requiring 0.25 μsec for register-to-register moves at 8-MHz clock, with 8-byte/sec bus bandwidth. HMOS ion-implanted, silicon-gate circuitry in a large chip (335×339 mils, approximately 134,000 transistors). Requires 5V at 600 mA. Has two operating modes: Real-address mode emulates 8086; protected virtual-address mode native to 286. House in a 68-pin JEDEC Type A leadless chip carrier, PLCC, and PGA.

**HARDWARE SUPPORT**

From Intel: ICE in-circuit emulator ($9995) supports 80286 at 8 and 10 MHz. It is hosted on IBM PC/AT/XT and Inteltec Series III/IV development systems. ICE286 ($12,495) supports 80286 at 12.5 MHz. iPAT Performance Analysis Tool, consisting of a hardware base unit, an interface to ICE, and host software for the PC/AT/XT, as well as Inteltec Series III/IV. iPAT provides high-level access to target-system performance analysis and test-case code-coverage analysis for the 80286.

From others: Number of 3rd parties support 286 on their universal development systems; for example, American Microsystems Corp (Beaverton, OR).

---

**SOFTWARE**

From Intel: Macroassembler (ASM 286) that includes systems builder, binder, mapper, and librarian. Compilers for C, Pascal, PL/M, Fortran, and Ada. For applications running in virtual 8086 mode, any of Intel’s 8086 software tools can be used. Hosts include PC-DOS, VAX/VMS, and Intel development systems. Prices are $750 for DOS. Real-time operating systems (Intel’s iRMX 286) available.

From others: Other operating systems and compilers being developed by 3rd-party software houses include MP/M-286 (Digital Research), Xenix-286 (Microsoft), Concurrent 286 (Mark Williams), Concurrent DOS (Digital Research), Unix System V (Digital Research), and of course OS/2 by Microsoft (Redmond, WA).
TEXAS INSTRUMENTS REPORTS ON DSP IN THE ERA OF MegaChip TECHNOLOGIES
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“The TMS320 helps us with one of our toughest tasks — designing toys with exciting features at prices that will sell.” Dave Small, VP Engineering, Worlds of Wonder, Inc.

Worlds of Wonder is a pioneer in developing interactive toys and now has an innovative new doll named Julie™. Using a single TMS320 chip, Julie’s designers are able to give her voice-recognition ability, coupled with synthesized speech and coordinated facial movement.

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<td>AREA CODE</td>
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TEXAS INSTRUMENTS
**80386**

**AVAILABILITY:** 16 and 20 MHz in production (at 2 geographically separate locations).

**COST:** In 100 qty, $299 for 16-MHz 80386, $575 for 20-MHz 80386. $500 and $855 for 16- and 20-MHz 80387.

**SECOND SOURCE:** None announced or planned in immediate future (although AMD is suing Intel for right to continue its second sourcing agreement on to 8386).

**Description:** The 32-bit member of the 8086 family, suitable for both multiprocessor and multitasking. Contains a full 32-bit, largely uncharacterized register set (some competitors debate this) and an on-chip MMU containing selectable segmentation and paging support with a 32-entry TLB. Has slower emulation mode in which it is 100% binary compatible with the 8086 and 80286, allowing 8086 and 80286 and 80386 applications to run concurrently. It's fabricated in 1.5-µm CMOS and has over 275k transistors.

**Hardware Characteristics**

**Software**

I—DATA MANIPULATION INSTRUCTIONS

Bit manipulation and bit-string manipulation (aided by 64-bit barrel shifter).

Conversion between bytes, words, and double words.

Arithmetic, including 16-bit and 32-bit operands and 32-bit signed and unsigned multiply and divide.

(80387 math coprocessor has full IEEE 754 instructions, including all transcedentals)

II—DATA MOVEMENT INSTRUCTIONS

String moves and gang push and gang pop of all registers.

Instructions to insert and extract bit strings (additional addressing modes for existing instructions allow more flexibility in assignment of registers)

III—PROGRAM-MANIPULATION INSTR

Repeat instructions based on flags.

Enter and leave procedure instructions, conditional or unconditional branch to anywhere in 4-byte memory space.

IV—PROGRAM-STATUS-MANIP INSTR

Flag instructions mostly similar to 8086 (contains 4 debug registers, allowing breakpoints on data or code accesses, even when in ROM).

V—HLL AND O S INSTRUCTIONS

Instructions for checking array bounds.

Segment assignment instructions.

Load and store descriptor tables for protection (processor context switch via 1 instruction)

Notes:
1. Only those instructions beyond basic 8086 instructions described.
2. 80386 said to be object-code compatible with previous members of 8086 family and can run their operating systems. There is a "virtual 8086" mode in which 8086 (and 8086) code can be run within the protected 386 environment.

**Specification summary:** A more or less standard, "classical" 32-bit minicomputer architecture that has a basic register set similar to the previous 16-bit members of 8086 family so that it can directly run their machine code. It has added features that make sense in a larger 32-bit environments: data-manipulation instructions that can be applied to almost any register, high-level-language-oriented instructions, operating-system-oriented instructions, and on-chip MMU. Performance can be 9k Drystones when operating at 16 MHz and with sufficiently fast (45 nsec) memory. Fabricated in 1.5-µm CMOS (supplier calls it CHMOS-III), it's expected to consume no more than 400 mA at 32-MHz external clock (16 MHz internal). Packaged in 132-lead ceramic PGA.

**Hardware**

**Support**

**Software**

**From Intel:** ASM-386 macroassembler ($600) and PMON-386 ($3500), DOS-hosted software debugger (DMON-386, $2500) is unhosted version. Also IC-386 and PL/M-386 high-level languages, RLL-386 set of relocation linkage and library utilities ($600).

**From others:** Rapidly growing 3rd-party support, of which most important are MS-DOS and forthcoming OS/2 from Microsoft, (Bellevue, WA). (There are variations in DOS such as Concurrent DOS by Digital Research (Monterey, CA)). Next is Unix V from AT&T (Morristown, NJ) and Xenix from Microsoft. Also real-time executives from Ready Systems (Palo Alto, CA), JMI Software (Spring House, PA), and others. In addition there are dual combinations of operating systems such as Unix-DOS from Phoenix (Norwood, MA), Locus (Santa Monica, CA), and Interactive Systems (Santa Monica, CA); CTOS-DOS from Convergent Technologies (San Jose, CA); and DOS-DOS from Intelligent Graphics (Santa Clara, CA).

**Notes:** Some software depends on 386 mode.
34010 GRAPHICS µP

Description: 32-bit CMOS µP optimized for graphics-display systems, but with true general-purpose Von Neumann architecture so it can be used for other applications that need the same bit manipulations as are required of pixel manipulations of CRT-type raster graphics. Features built-in instruction cache and ability to simultaneously access memory and registers. In addition to regular µP instructions, it has specialized instructions for pixel manipulation. 1G-byte address space is bit addressable on bit boundaries using variable-width data fields (1 to 32 bits).

HARDWARE

CONTROL

I/O

INSTR

DECODE

INSTR

GENERAL

256 BYTES

INTERRUPT

REGISTERS

INTERRUPTS

RESET

HOST INTERFACE

REGS (16 BITS)

VIDEO INTERFACE

REGS (SYNCH & BLANK)

LOCAL MEMORY

CONTROL REGS

STACK PTR

REGS

GP REGS

ALU

PROG COUNTER

STATUS

也知道

160 NSEC

INSTR CYCLE

LOCAL MEMORY

CONTROL & BUFFERS

32-BITS

Notes:
1. Architecture has some similarity to TI 99000 family µP, as Karl Guttag, who was involved in design of 99000, led design team.
2. Added graphics features are embodied in the second 16×(32) register file and among 28 16-bit I/O control registers. They allow programmable pixel and pixel-array processing for both monochrome and color systems of variable pixel sizes. Hardware incorporates 2-operand raster operations with Boolean and arithmetic operations, x-y addressing, window clipping, window "pick" operations, 1-to-n bits/pixel transforms, transparency, and plane masking.
3. A 2nd-generation version in development will have a full 32-bit (nonmultiplexed) bus for greater bandwidth.

SUPPORT

From TI: TMS34010 software development board ($2495), which plugs into IBM PC or compatible. Used for evaluation, familiarization, and software development, and comes with user interface and debugger software. TMS34010 XDS (22 emulator box ($14,995) operates as a stand-alone unit with dumb terminal or with IBM PC or compatible as host.

From others: Board-level and other hardware support now available from numerous sources. See TI’s TMS 34010 3rd-Party Guide (call 800-232-3200 ext 701 and ask for literature No SPVB066A).

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

General-purpose µP instructions: add and subtract, multiply and divide, rotate and shift, compare and logicals

Special graphics instructions: add, subtract, and comparisons relating to coordinates

II—DATA-MOVEMENT INSTRUCTIONS

General-purpose: Move byte, move field, move register

Special graphics instructions: Move x half of register, move y half of register, pixel transfer, pixel binary operations

III—PROGRAM-MANIPULATION INSTR

Call subroutine, conditional decrement and skip, push/pop, software interrupt, return from interrupt

IV—STATUS-MANIPULATION INSTR

Has 32-bit status register (not all bits used) that can be accessed and used for program-manipulation decisions

SPECIFICATION SUMMARY:

32-bit general-purpose CMOS processor with added hardware and software features to support CRT raster graphics. Chip contains two 16×(32) register files, hardware stack pointer, and 256-byte instruction cache. One of the 16-bit register files contains stack pointer and 15 general-purpose registers (the equivalent of the GP registers found in regular non-specialized µPs). Addressing modes of these registers is tuned to support high-level languages. Other register file is dedicated to CRT control as described in hardware note. ALU provides single-cycle, 160-nsec execution of common integer arithmetic and Boolean operations from 256-byte instruction cache (using LRU updating algorithm). More-complex instructions take multiple cycles, with signed multiply taking 20 and divide taking 40. Has 32-bit-wide barrel shifter that provides a single-cycle bidirectional shift and rotate function for one to 32 bits. Has 32-bit-wide address-data bus to support a gigabyte of off-chip “local” memory space. Interfaces directly to dynamic RAMs and video RAMs (including dual-port RAMs). A micro-coded local memory controller supports pipelined memory write operations of variable-size fields that may be executed in parallel with ALU operations. Has separate 16-bit-wide data bus and associated control pins to interface with host µP. Fabricated in 5V CMOS and packaged in 68-pin PLCC.

Texas Instruments Inc
MMP Graphics Dept
Box 1443, M/S 736
Houston, TX 77001
Phone (713) 274-3297

Status: This µP is included in directory despite its obviously specialized slant toward CRT graphics because it happens to have general-purpose Von Neumann architecture and instruction set and some of its attributes can be easily applied to other, nongraphics applications. In particular, its ability to do rapid bit manipulation of a large local address field. From the number of IBM PC-based board-level products announced that incorporate this part, it can be concluded that it is a success. TI says it will ship 100k units in ’87, mostly for graphics and similar laser-printer applications. One nongraphics area being explored by users is for industrial control where bit manipulation and low cost relative to other 32-bit µPs is found attractive, according to TI (even for consumer-oriented uses such as arcade games). In some cases designers in nongraphics areas are making clever use of some of special graphics features.

From TI: TMS34010 assembler package ($500) for IBM PC and compatibles using MS-DOS 2.11 or higher and for VAX ($1000) using VMS, Unix Berkeley 4.2, or Unix System V. Includes macroassembler/linker, source/object code archiver, and ROM utility. MS-DOS version also has a 34010 simulator.

A C compiler supporting full Kernighan & Ritchie C with extensions for in-line assembly code and enumerated data types. $1000 for PC and $3000 for VAX.

A graphics/math function library ($5000 for source code) provides graphics primitives, transcendental functions using double-precision floating point, matrix operations, 3-D transformations, text generation, etc. (TI says it has sold about 100 of these, mostly to smaller companies that want a head start).

From others: Software now available from numerous 3rd-party sources such as JMI (Spring House, PA) who has done a real-time executive. See the TI TMS 34010 3rd-Party Guide mentioned under Hardware Support.
WE TAUGHT THE WORLD TO DRIVE WITH OUR FULL-SIZE MODELS.
VL 86C0X0 ARM

AVAILABILITY: Now for production volumes of 86C010. 4th qtr '87 for announcement of enhanced version, 86C020 (tentative number).

CORE: $99 for samples. $20 for 86C010 in volume.

SECOND SOURCE: None announced.

CORE: Part of VLSI's cell library. (Was designed by customer Acorn Computers using VLSI's semicustom tools.)

Description: ARM stands for Acorn-RISC machine (RISC stands for reduced-instruction-set computer). According to RISC-architecture philosophy, leaving out seldom-used instructions, a designer can make chip smaller and faster. Then, when complex instructions are needed, they can be generated by compiler, which in turn is supposed to be more efficient and easier to write because of simpler instructions. It is one of first µPs designed by customer using supplier's ASIC tools. It took 2 systems engineers and 4 circuit designers at Acorn 18 months to design initial 86C010 chip, but announcing subsequent upgrades such as the 86C020 (tentative number) are that much easier and quicker because the µP is now part of the VLSI ASIC library and the Acorn designers are familiar with the design tools.

Notes:
1. In addition to 86C010 µP, VLSI has associated set of chips for memory (86C110), video (86C310), and I/O (86V410). For floating-point math, VLSI suggests using one of the commercially available coprocessors such as AT&T's WES2206.
2. Note the 25 registers. This is less than on some RISC machines, but they do overlap as is common in RISC to speed interrupt service (overlapping gives automatic saving of data). This means programmer only sees 16 registers at most, and of these, only 15 are general purpose.
3. Some provisions for memory management, including cache and virtual memory through abort signal, move control bits.

VLSI says that much of the hardware support comes from Acorn. There is a PC-form-factor board ($2500) for software development. (Note: It can be expected that VLSI will bias its support toward the ASIC approach in which the Arm µP will be considered a core around which the customer will be encouraged to apply "application-specific" I/O, memory, etc; thus, VLSI's ASIC design tools might be considered part of the hardware support.)

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, logics and comparisons. Bit clear. Shifts (barrel shifter with ALU)

II—DATA-MOVEMENT INSTRUCTIONS
Most data movements are by register-to-register instructions with option for multiple-register addressing. Only load and store operations to memory (typical of RISC)

III—PROGRAM-MANIPULATION INSTR
Skip-type decision instructions (though old-fashioned, this simple approach can give fastest response in some cases). Branch instruction has option where combined PC and status register are copied in R14 data register for quick, simple return.

IV—PROGRAM-STATUS-MANIP INSTR
Usual status bits are combined with PC and mode-control bits in a 32-bit-long register. This allows all three elements to be saved in one fell swoop.

Notes:
1. Only 44 instructions, in keeping with RISC concept.
2. Simple RISC instructions are said to ease the task of writing efficient high-level-language compilers.
3. User and supervisory modes with supervisory mode being entered by software interrupt.

Specification summary: 32-bit CMOS Von Neumann (common memory) µP with RISC-style architecture. Has simple ALU with associated barrel shifter and set of 32 registers on CPU µP chip, 16 of which are accessible to programmer. Has some features expected in a large-memory-space machine: instructions and controls to handle virtual memory and caching. 32-bit external data bus and 26-bit external address bus allow linear addressing for external 64M-byte external memory space (can be addressed on 8-bit-byte or 32-bit-word basis). Only simple load and store instructions for external memory. 10-12 MHz, 2-phase clock gives 4-5 MIPS sustained performance with 10 to 12 MIPS max. Interrupt latency is 2.75-μsec max. No provisions for separate I/O addressing so I/O must be memory mapped. Fabricated in 2-µm CMOS with chip 230 mils on side. To 70°C temperature range. Packaged in 88-pin JEDEC Type-B leadless ceramic chip carrier and plastic leadless chip carrier. Forthcoming 86C020 (tentative number) will be in 1.5-μm CMOS and have 2 x performance.

EDN November 26, 1987
OUR COMPACTS HAVE SOLD MILLIONS.
IMS T212, T414, T800 TRANSPUTER

AVAILABILITY: Now for production quantities of T414 (15 and 20 MHz), T212 (17 and 20 MHz). T800 in samples quantities with production 4th qtr 87.

COST: In 100 qty, T414 (15 MHz, PLCC) $163, T212 (17 MHz, PGA) $108, T800 (17 MHz, PGA) $406.50, T800 (20 MHz, PGA) $487.50.

SECOND SOURCE: Negotiations said to be still in progress.

Description: RISC-like machine, though it uses microcode and has multiple-cycle instructions. Most interesting feature is incorporation of interprocessor communication links to simplify construction of multiple-Transputer systems. As many as 100 Transputers have been linked in parallel, and supplier claims that the performance increase has been linear. To make such multiple-μPs systems feasible from standpoint of cost and board space, supplier has incorporated dynamic-RAM controller and timers, as well as communication links, on chips. Software support for multiprocessing is in form of multitasking-real-time kernel in instruction set and supplier's Occam language.

HARDWARE

T800, T414, and T212 are available as discrete components as well as on evaluation boards, including boards for IBM PC and VME systems. Modules are also available, ranging from a T800 with 8M bytes to a T212 with 64K bytes, and include graphics facilities. Multiple modules can be mounted on a mother board, and the interconnections can be varied under program control using a C004 link switch on mother board. For designers wishing to explore parallel systems, there is a 10-slot card cage configured with 40 transputers, each with 256K bytes of RAM. These systems have a top performance of 400 MIPS and 60M flops (some 60 of these $35k to $50k R&D systems have been sold). The new T800 version will sell for $70k. Also available are the C011 and C012 link adapters.

SOFTWARE

From Inmos: C, Pascal, and Fortran compilers for all family members. Ada promised for 88. Development tools allow multilanguage programming. For distributed systems and parallel computing, Inmos also offers Occam, a concurrent language with explicit facilities for Transputer interrupt handling, multitasking, and message passing. Compilers are available either as integrated suite—the Transputer Development System—with editor, compiler, syntax checker, and multiprocessor linker/loader, or as separate components for use with customer's own editors, etc.

From others: Inmos says there is a growing body of software tools from third parties, including some C compilers with Occam-like features for multiprocessing and parallel computing.

16/32-BIT CMOS

Inmos Corp
Box 16000
Colorado Springs, CO 80935
Phone (303) 630-4000
(Designed, processed, Bristol, UK)

Status: Volume buildup has been slow—EDN estimates that amounts have been only at 10k level so far. One possible explanation is that most of the applications have been for multiprocessor configurations (typically 4 to 10 transputers), so designers have been engrossed by the challenge of developing practical parallelism. Supplier expects some of its 50 or so "design wins" will move into production during '87 and '88. One of these may be the workstation that Atari is introducing. The new T800 that Atari is using has on-chip floating point. Parent company Thorn EMI continues to try to sell part or all of Inmos; meanwhile Inmos says it's reaching profitability.

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

Integer arithmetic, including multiply and divide. Logicals, shifts, and comparisons. T800 has on-chip IEEE FP add & subtract, multiply & divide, and square root, both 32 and 64 bits.

II—DATA-MOVEMENT INSTRUCTIONS

Memory-bandwidth block moves, 2-dimensional block moves for graphics BitBit. Load/store of local variables done relative to workspace pointer. Indexed load/stores available from address in A register. Immediate loads done 4 bits at a time. Large immediate values loadable from tables, from instruction stream, or from a sequence of special instructions.

III—PROGRAM-MANIPULATION INSTR

Conditional and unconditional jumps. Procedure call and return. Subroutine call and return. Computed jumps. Process (task) creation and deletion. 2-level priority and time-sliced scheduling with message passing and time events, using built-in hardware. One level of interrupt

IV—PROGRAM-STATUS-MANIP INSTR

Error flag detects overflow. Test, set, clear, stop-on-error instructions. One error flag per task priority level. Instructions for checking array bounds.

Notes:

1. Frugal 4-bit operation code allows only 16 basic instructions. Most of these are movement types (category II) involving one workspace-pointer-relative 4-bit address and used to push and pop data on and off evaluation stack. Two op codes support building data fields bigger than the basic 4 bits. One op code causes data field to be interpreted as stack operation (eg, add, subtract, etc).

2. Two priority-ordered process queues are each supported by front and back registers, indicating a linked list of processes ready to run. Event-based multitasking is fully supported by a real-time kernel in microcode.

3. Supplier’s Occam language said to facilitate programming multiple Transputer systems. But programmer must still study how best to partition task. Third parties have announced extensions to C to accomplish same ends.

Specification summary: Family of 16- and 32-bit μPs oriented toward multiprocessing. Unique in that they have the hardware and software links that allow them to be hooked to each other for parallel processing. The newest family member, the T800, has 4K-byte on-chip RAM, which occupies the bottom 4K bytes of a full 4G-byte address space. Four, full-duplex, 20M-bps serial links driven by on-chip, 8-channel DMA provide basic multiprocessor communication links as well as I/O. T800 has on-chip dynamic-RAM controller and a pair of timers. One 5-MHz external clock is multiplied by on-chip PLL to generate 20-MHz chip clocks, giving 50-nsec instruction cycle. Submicrosecond interrupt latency, procedure call, and task switch. Most instructions take 1 or 2 cycles. Integer multiply takes 38 cycles, and divide takes 39 cycles (under 2 μsec). Single-precision floating-point add takes 7 cycles (350 nsec). FP multiply takes just 11 to 18 cycles (550 to 900 nsec), and FP divide takes 16 to 28 cycles (800 to 1400 nsec).
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ONE T800 TRANSPUTER GIVES 2.5 DOUBLE PRECISION MEGAWHETSTONES...

When it comes to processing power, seven InMOS T800 chips could give the mighty CRAY 1S, rated at 16.1 MEGAWHETSTONES, a real run for its money!
MORE
MULTIPROCESSOR
MUSCLE.
MORE RAW
PERFORMANCE.

When you're out in the trenches fighting it out with ordinary microprocessors, running out of muscle is all too easy. That's why you should look to the new T800 Transputer from INMOS.

The T800 is the fastest 32-bit, single chip, floating-point microprocessor available today. A quick glance at its statistics will show why nothing else is in its league...

- 32-bit enhanced RISC processor...64-bit on-chip IEEE Floating-point processor...4K Bytes on-chip 50ns static RAM...Four 20 MBit/sec interprocessor communication links...Eight independent DMA engines, All on a single chip capable of sustained 1.5 MFLOPS...and 4.6M Whetstones!

And, if that's not enough raw power, the T800's links allow multiprocessor systems to be constructed quickly and easily - giving you 6 MFLOPS with four T800's...30 MFLOPS with 20...150 MFLOPS with 100...In fact, there's no limit to the number of Transputers you can use!

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Want to turbocharge your current system? No problem. Our exclusive Link Adapter IC's allow Transputers to be connected to other microprocessors or peripherals.

Other team members include the pin compatible T414 Transputer, offering lower cost, 10 MIPS performance and 0.75M Whetstones.

Lined-up to provide all the I/O processing you need, the T212 16-bit Transputer is the ideal high performance controller and the M212 Disk Processor combines disk controller hardware and a Transputer on a single chip, supporting both Winchester and floppy disks. And the C004 Link Switch makes the design of software reconfigurable multiprocessor systems as easy as kicking an extra point.

Whatever field you're in - from real-time distributed systems to high-performance graphics, from fault-tolerant systems to robotics, Transputer technology can give you scalable performance at a cost you can afford.

Transputers are manufactured using an advanced 1.5 micron CMOS process which keeps the power consumption under one watt.

Tranputers to MIL-STD 883C will be available in the first half of 1988.

If this all sounds like your kind of game, put the ball in play by contacting your local INMOS sales office today. And get ready to score.
Z8000/Z80000

**AVAILABILITY:** Now for NMOS Z8000 at 4, 6, 10, and 12 MHz. Now for NMOS Z80000 at 8 and 10 MHz. CMOS versions for Z8000 and Z80000, '88 and '89, respectively.

**COST:** $6 to $12 for Z8000 in 1k qty, and down to $3.50 in PLCC (Z8005) in high volume. MIL-spec versions typically run in hundreds of dollars. Under $100 for Z8000 in ceramic PGA at 250 qty. As low as $25 in 25k volume projected for 68-pin PLCC (Z80320).

**SECOND SOURCE:** AMD (licensed), SGS (Italy and Arizona), and Sharp for Z8000. NEC for Z80000, by mask exchange.

**Core:** Zilog is incorporating both Z8000 and Z80000 as cores in its "in-house" ASIC library, planning to use Zbus for their systems on silicon. Says that 150x 160-mil Z8000 core is small enough to leave room for other functions on practical 400x400-mil ASIC chip.

**Description:** One of first µPs to have architectural features of a modern minicomputer. Original 16-bit Z8000 comes in 40-pin package for addressing 64k-byte memory or in 48-pin package for addressing 8M-byte memory. Said by many industry observers to be architecturally more powerful than 8086 but less powerful than 68000. Supplier says military has found it to be highest performance 16-bit µP, offering best CPU speed, interrupt-handling, and character-string search. New 32-bit version, Z80000, is superminicomputer-like enhancement that remains object-code compatible with the Z8000. Has cache for data and instructions and an MMU.

**Notes:** Supplier has companion peripherals suitable for both processors:
For Z8000, a range of DMA, FIFO, data ciphering (NBS), communica-
tions and counter/timer parts.
For Z80000, two 32-bit parts: a Z32104 CMOS DMA controller, 32-bit address and data buses with 8-bit peripheral bus; and a Z32106 CMOS floating-point coprocessor that implements IEEE P754 format.

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**16/32-BIT NMOS AND CMOS**

**Zilog Inc**
210 Hacienda Ave
Campbell, CA 95008
Phone (408) 370-8000

**Status:** The Z8000 has, according to Zilog, found most acceptance in real-time control applications, particularly military. Dataquest figures for '88 show the Z8000 reached a unit volume of 523k units, holding its 41% share of 16-bit µP market. This was greater than National's 32016's unit volume, though much less than either the 8086 or 68000 families. Supplier says it has been shipping samples of the much-delayed Z80000 for 6 months and some customers have found it will run at over 16 MHz in their systems. Zilog will be pushing the Z80320 "32-bits-for-32-bucks" derivative of the Z80000. Supplier has again slipped its schedule for CMOS versions and now says it will be '88 for Z8000 and '89 for Z80000.

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**PRELIMINARY SPECIFICATIONS**

- **CLOCK:** 10 MHz
- **IO:**
- **ADDRESS BUS (24):**
- **INSTR REG**
- **ALU**
- **1 RFC; rf REFRESH**
- **Refreshing**
- **GEN**
- **16 BIT ALU**
- **32 BIT ALU**
- **7 SEGMENT POINTERS**
- **V SYSTEM - CONTROL INSTRUCTIONS**
- **I - DATA - MANIPULATION INSTRUCTIONS**
  - Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed)
  - Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n)

**Notes:**
- Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulators.
- The Z32106 floating-point processor will do IEEE 754 operations.

**Software**

**I - SOFTWARE**
- **Software**
  - Arithmetic, including add, subtract, decimal adjust, increment, decrement, multiply (signed), divide (signed)
  - Logicals, including AND, OR, exclusive OR, compare, test, complement, rotate, and shift (by n)

**Notes:**
- Operations can be on bit, BCD nibble, byte, 16-bit word, or 32-bit double word, and can use any of the 16 general-purpose registers as accumulators.
- The Z32106 floating-point processor will do IEEE 754 operations.

**II - DATA - MOVEMENT INSTRUCTIONS**
- Eight addressing modes using general-purpose registers as indexers and stack pointers.
- Comprehensive set of block-transfer and string-manipulation macro-equivalents, including many dedicated to I/O space.

**III - PROGRAM - MANIPULATION INSTR**
- Call and call relative (±4096 bytes)
- System call using special system stack pointer
- Jump conditionals

**IV - PROGRAM - STATUS - MANIP INSTR**
- Set and reset flags, complement flags.
- Set-multiple-interrupt modes.
- Tests for the micro in and micro out lines for multiple-microprocessor configurations.

**V - SYSTEM - CONTROL INSTRUCTIONS**
- The 8000 has privileged instruction for exclusive use by an operating system.
- Specification summary: Common-memory architecture with optional separate I/O space and separate "systems" stack.
- Z8000 is 16-bit µP that has directly addressable memory space of 8M bytes (8001, 8003) using segment pointers, expandable to 48M bytes using the six available memory spaces and an MMU. Executes 110 basic instructions with 410 combinations at speeds ranging from 0.30 µsec through 1 or 2 µsec to 7 µsec for 16-bit multiply, all at 10-MHz system clock (4 and 6 MHz also available). Eight large-computer-style addressing modes. NMOS, requiring one +5V supply (plus substrate-decoupling capacitor) in either 40- or 48-pin package. Z80000 is a 32-bit upward-compatible version of Z8000 and can run same software. 6-stage pipelining of instruction fetch/execute cycle and 256-byte on-chip associative cache for instructions and data for improved performance (and use of 100- to 150-nsec memories). Also on-chip MMU for virtual memory with address bus a full 32 bits for 4G-byte memory space. At 25-MHz clock has 12.5-MHz (80-nsec) instruction cycles, that gives 12.5-MIPS burst rate (when doing loops out of cache), and 5 MIPS continuously (4 MIPS with MMU virtual-memory translation). 16 x 16 multiply in 1.2 µsec and 9 x 32 in 1.9 µsec, 2-µm NMOS dissipating 3 to 4W with 1½-µm CMOS promised for 88 (Z8000) and 89 (Z80000). Initial samples have been packaged in ceramic PGAs but lower-cost Z80320 will have mixed address and data buses and be in 68-pin PLCC.

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**SUPPORT**

**From Zilog:** Z-Scan 8000 in-circuit emulator ($5500), 500-page Z8000 technical manual.
**From others:** Applied Micro, Boston Systems, Hewlett-Packard, Kontron, Orion, Single Board Sol, Sweet Micro System, and Tektronix. Contact supplier for addresses.
68000 FAMILY

AVAILABILITY: Now for production quantities of all models to 25-MHz 68020. Samples of 68030.

COST: In 100 qty, from $10 for low-end 68008 and 68000 to $135 for 12.5-MHz 68020 and $530 for 25-MHz 68020. 68881 math coprocessor is $107 for 12.5 MHz and $347 for 25 MHz. Production pricing for 68030 not available.

SECOND SOURCE: Rockwell, Hitachi, Mostek, Signetics/Philips, and Thompson SGS, all licensed with mask interchange for 16-bit parts. Thompson was to be second source for 32-bit 68020, but Motorola says it plans to keep 68020 and 68030 to itself for time being (it needs the revenue to justify the $20 million or so development cost).

Description: Family based on a modern minicomputer architecture using a basic group of 16 fairly general, 32-bit registers. Family members have various addresses and data-bus widths and different ALU widths. The bottom of the line, the 68008, has a narrow 8-bit data bus. The middle member, the 68000, has a mid-sized 16-bit data bus and ALU and 24-bit addressing. Current top of the line, the 68030, is full 32 bits throughout with instruction and data caches and MMU on board.

HARDWARE

68000

ADDRESS (22)

CLOCK

PROGRAM COUNTER (22)

USER STACK REGISTER

ADDRESS REGISTERS

DATA REGISTER

6800 PROGRAM COUNTER

TRAP

BAD ADDRESS

0

16 BITS

ALU

REGISTERS

Note: Diagram favors the basic 68000, which although it has 32-bit-wide registers, has 16-bit-wide ALU and data buses and only 23-bit-wide address bus. It comes in 48-pin DIP and 68-pin grid array.

3. Upper-range 68010 and 68012 are similar to 68000 but support virtual memory. 68010 has 24-bit address bus and comes in a 64-pin DIP or 68-pin grid array. 68012 has full 32 bits of address and comes in 84-pin grid array.

4. Top-of-the-line 68020 and 68030 are full 32 bits throughout, including ALU and address and data paths. Both have instruction caches and the 68030 also has a data cache and an MMU.

5. Two important support chips, not shown, are the 68881/2 floating-point coprocessor and the 68651 MMU. Both are in CMOS.

6. The 68070 by Philips/Signetics includes various support functions on chip.

SUPPORT

VersaDOS real-time operating system, system V/68 operating system, CP/M-68K operating system, concurrent DOS-68K operating system, and VRTX real-time operating system ($6775 from Hunter Systems). Unix support from Motorola includes direct ports of Unix V, AT&T. From 3rd parties: Supplier has catalog listing the considerable outside support for family. New type of support is software to allow 68000 to run MS-DOS (8086) programs: by Phoenix (Norwood, MA) and by Insignia (London, UK, but with offices in San Francisco); and by binary translation from Hunter Systems (Palo Alto, CA). The latter's package, XDOS ($600), uses a binary compilation approach to generate disks that will run at competitive speeds on 68000 µPs.
SERIES 32000

AVAILABILITY: Now for all older NMOS and some CMOS replacements for NMOS parts. The new CMOS 32352 is sampling (see table).

COST: In 100 qty, from $8.75 ($5 or $6 in volume) to $1000 (see table).

SECOND SOURCE: Texas Instruments for some NMOS parts only.

Description: A 32-bit µP family in which various models bring out different-sized address and data buses. The fully 32-bit core processor has acquired reputation even among competitors for being “elegant” in its symmetry: that is, its instructions and addressing apply regularly to all registers, which supplier claims makes high-level-language compilers easier to write. It also has reputation for needing less memory space for programs. These software virtues should apply to all family members as strict code compatibility across line. Family is intended to match the needs of operating systems like Unix and to have big-computer features expected of 32-bit systems, such as demand-paged virtual memory, protection of operating system from users, and protection of one user from another user.

HARDWARE CHARACTERISTICS SOFTWARE

Hardware Notes:
1. Shown are four original members of basic 5-chip set (32202 interrupt control missing). 8- and 32-bit external data bus also available. Note that low 16 bits of address coming off CPU are multiplexed with data.

2. Floating-point chip (NS32081) is example of slave-type processors National is using to extend CPU. These processors will be integrated on chip when VLSI technology permits; they are transparent to CPU hardware (Mod register) and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions expected of 32-bit systems, such as demand-paged virtual memory, protection of operating system from users, and protection of one user from another user.

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 721-5000

Status: National is in 3rd place in 32-bit shipments. This year National estimates its full 32-bit devices (32-bit external buses) will reach a volume of 500,000, up from the 104,000 unit volume Dataquest listed for '86. National says that because all its 32XXX family members are full 32-bit internally, those members with 8- and 32-bit external data buses should also be included which would bring the total up to 700,000 units or roughly on par with what Motorola and Intel are claiming for their 68020 and 80386. What seems critical now is how well the new 32532 is received. It appears to be the ultimate CISC machine (for now), and if it can run at the promised 30 MHz and deliver the promised 10-MIPS sustained performance, it should be attractive for multiprocessor Unix systems (whether in reprogrammable or embedded applications).

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

All instructions operate on either 8-, 16-, or 32-bit data and can be accessed by any appropriate addressing mode. Multiply and divide, BCD arithmetic, logicals and bit manipulation throughout memory space and CPU registers.

II—DATA-MOVEMENT INSTRUCTIONS

Intelligent string operations and bit-field handling allow efficient movements.

III—PROGRAM-MANIPULATION INSTRUCTIONS

Stack- and frame-pointer instructions suitable for high-level languages (including Polish notation). Modular software support via special CPU hardware (Mod register), and tables automatically implemented for indirect addressing of position-independent ROMs, etc. Array instructions.

IV—PROGRAM-STATUS-MANIP INSTRUCTIONS

Status registers in slave processors and MMU as well as in CPU, with both privileged and user access.

Specification summary: 32-bit “maxi-mini”-type pipelined architecture implemented in multichip NMOS VLSI. Uniform addressing of up to 4G memory locations. Instruction set chosen to match operations needed by high-level-language compilers. All instructions can symmetrically apply to all data types (8, 16, and 32 bits, etc) and all register and memory locations. Performance of family ranges from 4 MIPS to 10 MIPS (sustained). The top-of-line model 32532, when running at maximum 30-MHz clock, has a peak performance of 15 MIPS and a Dhryper benchmark of 16.3k. It has 4-stage overlapping execution pipeline that includes instruction prefetch and branch prediction. It has parallel address and data units, each with own buses and 32-bit ALU. Separate caches for instruction and data: the instruction cache is 1k bytes (direct mapped); the data cache is 1k bytes, 2-way set associative. On-chip demand-paged virtual MMU with 64-entry associative translation look-aside buffer. Fabricated in 1.5-µm double-metal CMOS. Packages range from 48-pin DIP for 32008 to 175-pin pin-grid array for 532. LCC and PLCC packages available for some models.

From National: SY3232/20 that converts IBM PC XT/AT into a Series 32000 development tool (from $3500). Splice in-system emulation covers family µPs up to 32332 with support for 32532 on way. Development/evaluation boards based on 32016, 32032, and 32332 are also available from National and from other suppliers (contact National for list) with prices from $965 to $9900.

From others: PC plug-in board with 32016 or 32032 and memory ($2000 to $3000) that allows running Unix from Opus Systems (Cupertino, CA). PC-based logic-analysis workstation by Northwest Instrument Systems (Beaverton, OR).

SOFTWARE

From National: Series 3200 Software Catalog is guide to available software. It lists compilers for C, Pascal, Fortran, Cobol, Modula-2, Ada, etc. Supplier says its new CT compiler technology optimizing compilers can increase performance and code density as much as 2×. Operating systems include supplier’s Genix V 3.2 based on AT&T System V, release 3.0 and Genix 4.2 based on Berkeley 4.3.

From others: Software-analysis workstation from Northwest Instrument Systems (Beaverton, OR). Software coprocessor from Phoenix Technology (Worcester, MA) that allows family to run VRTX real-time multitasking operating system from Ready Systems (Palo Alto, CA).
WE32 FAMILY

AVAILABILITY: Now for both WE32100 and WE32200 (see table for speeds)

COST: $110 for 10-MHz 32100 CPU, 1k qty (see table for others)

SECOND SOURCE: Zilog for 32100. To be announced for WE32200.

Description: CMOS chip sets for building top-of-the-line, minicomputer-like computing systems. Provided with depth of Unix operating system support, so suited to multuser/multitasking applications. New 32200 has better performance but at a price increase (see table). (Note that AT&T has separately developed a RISC-type 32-bit µP called Crisp. So far no schedule for commercialization has been announced.)

WE32100

CPU 32-BIT MICROPROCESSOR

WE32101

MMU MEMORY-MANAGEMENT UNIT

WE32102

CLOCK 2-PHASE CLOCK

WE32103

DRAM DYNAMIC-RAM CONTROLLER

WE32104

DMAC DIRECT-MEMORY-ACCESS CONTROLLER

WE32106

MAC MATH-ACCCELERATION UNIT

WE32200

CPU 32-BIT MICROPROCESSOR

WE32201

MMU MEMORY-MANAGEMENT UNIT

WE32204

DMAC DIRECT-MEMORY-ACCESS CONTROLLER

WE32206

MAC MATH-ACCCELERATION UNIT

WE32100

CPU 32-BIT MICROPROCESSOR

WE32101

MMU MEMORY-MANAGEMENT UNIT

WE32102

CLOCK 2-PHASE CLOCK

WE32103

DRAM DYNAMIC-RAM CONTROLLER

WE32104

DMAC DIRECT-MEMORY-ACCESS CONTROLLER

WE32106

MAC MATH-ACCCELERATION UNIT

WE32200

CPU 32-BIT MICROPROCESSOR

WE32201

MMU MEMORY-MANAGEMENT UNIT

WE32204

DMAC DIRECT-MEMORY-ACCESS CONTROLLER

WE32206

MAC MATH-ACCCELERATION UNIT

32-BIT CMOS

AT&T Technologies Inc

Dept LT

555 Union Blvd

Allentown, PA 18103

Phone (800) 372-2447

Status: These chip sets have an advantage: AT&T is developing its newest versions of Unix on them. But so far there has been no indication that they have any marked acceptance for Unix applications compared with any of the many other 32-bit µPs. Meanwhile, AT&T's internal use of the chips for its 3B computers (in the "tens of thousands") plus other uses where the chips are embedded in AT&T telecomm equipment and in commercial applications have given the family the start down the production learning curve that is so important for all large 32-bit chips.

I—DATA-MANIPULATION INSTRUCTIONS

Fairy complete arithmetic, logical, and bit-manipulation instructions (including 2- and 3-operand instructions)

II—DATA-MOVEMENT INSTRUCTIONS

Wide variety of addressing modes that support high-level language constructs (eg, arrays, structures) and allow manipulation of byte, half-word, word (32-bit), floating-point, BCD, and string data types. Also supports bit field manipulation. All instructions can be used in any addressing mode with any data type, allowing programming and compiler design flexibility.

III—PROGRAM-MANIPULATION INSTR

Large selection of conditional branches. Conditional returns from subroutines. Call and return from procedures which automatically update execution stack, providing efficient procedure linkage.

IV—PROGRAM-STATUS-MANIP INSTR

The 32-bit status register contains 26 bits of status information that covers not only the ALU condition codes of smaller µPs but information that relates to exceptions, interrupt mask level, execution level, cache control, etc.

V—SYSTEM-CONTROL INSTRUCTIONS

Operating system instructions that allow efficient process switching and system calls (privileged and nonprivileged). Breakpoint, trap, and cache flush instructions

Notes:

1. Software compatible with AT&T's previous 32-bit µP, the WE 32000.
2. There are four levels of execution privilege: kernel, executive, supervisory, and user.

Specification summary: Upwardly compatible chip sets (see table) intended for large-memory, minicomputer-like 32-bit systems. The 32100 CPU features separate addressing and data execution sections each with 32-bit-wide bus. A 64-word instruction cache followed by an 8-byte instruction queue control a 3-deep pipelined execution unit. Performance can be maintained at 3 to 4 MIPS. The 32100 CPU is augmented by four VLSI support chips (see table): The 32101 MMU provides support for 4G bytes of virtual memory and incorporates both demand-paged and demand-segmented approaches. The 32103 DRAM addresses 16M bytes of dynamic RAM, supporting the newest 1M-bit devices and incorporates refresh control, etc. The 32104 DMAC handles 32-bit address generation for rapid memory-to-memory data transfers (14.5M bytes/sec) and has additional 8-bit-wide bus for efficient transfers to slower peripherals. The 32106 MAC coprocessor executes IEEE floating-point math, allowing the 32100 system to achieve 1.4M Whetstones/sec. Chip set is fabricated in 1.5-µm twin-tub CMOS (32100 CPU consumes 0.6W) and are in ceramic grid array packages (see table).

The 32200 enhanced chip set delivers up to 8 MIPS when operating in the 20- to 30-MHz range. CPU has 32 registers and 256-byte instruction cache. MMU has 4K-byte data cache plus bus watcher. MAU provides up to 3.9M Whetstones.

WE3210S development system that includes WE321AP analysis pod ($22,500 for 10-MHz) in-circuit emulation of 32100 and 32101. 14 MHz also available. WE321/22 device monitors provide signal observation of high-speed systems.

WE321EB evaluation board ($5500 at 10 MHz, $6500 at 14 MHz) with 32101 MMU and 32106 math accelerator.

WE321SB single-board computer with VME Bus that is compatible with AT&T 3B computers, giving users access to one of the largest off-the-shelf collections of Unix software.

WE321SG software-generation programs run on host Unix systems. Includes C compiler, assembler, linking editor, and optimizer. Prices range from $750 to $1250. Also compilers for Fortran, Cobol, Lisp, Basic, and Ada. Over 1000 end-user programs, including Informix, Crystal Writer, and Multiplan have been developed for the chip set, according to AT&T.

AT&T provides a range of Unix licensing arrangements from $60 for binary sublicense for a 1- or 2-user situation to $72,000 for an initial license for source code (substantial discounts for educational institutions).
Description: CMOS chip set intended to run Unix-based software at state-of-the-art speeds (5 to 50 MIPS). CPU has a RISC flavor with streamlined instruction set and a large number of registers. But the basic RISC frugality is augmented with on-chip floating point and two cache/MMU chips: one for instructions and one for data. Because the dual caches are large (for µPs), the Clipper is said to achieve 90% hit rates and sustain 5-MIPS average performance at 33-MHz clock for C100 (2 to 3 times more at 50-MHz clock for C300). With 100% cache hits, bursts of 33 MIPS can be achieved with C100 (50 MIPS for C300).

Hardware Notes:
1. Clipper consists of three CMOS chips. The original chip set, C100, with its 33-MHz clock, is shown in diagram. The forthcoming C300 is a plug-in upgrade that runs at 50-MHz clock.
2. The CPU chip has RISC-like ALU plus a CISC-like macrocode ROM and floating-point unit. The other two chips are identical pin-programmable cache/MMU chips, so one can be used for instruction caching and the other for data caching. The instruction cache carries the CPU's PC (instruction program counter). The 4096-byte capacity of each cache (large for µPs) plus the sophisticated caching control (2-way set associative) gives the Clipper a high hit ratio (over 90%), a key factor for sustained execution speed.
3. Each cache supports virtual memory via the on-chip MMU. The caches (especially the data cache) operate on a physical memory basis, so less flushing is needed. The C100 requires 136-nsec memory devices, and the C300 requires 90-nsec memory devices.
4. Sophisticated pipelining is used on CPU, but with provision for bypassing so that an instruction can obtain the result of a preceding instruction without delay.

Software Notes:
1. Clipper's 168 instructions are a balance between 1-cyle RISC and multicycle CISC commands. The RISC takes care of the simpler, most frequently used instructions. The CISC macrocode takes care of complex instructions such as floating/integer conversion, character-string manipulation, save and restore registers, and trap/interrupt entry and return sequences.
2. C100 and C300 instruction sets are compatible.

Specification summary: Modified RISC-type architecture in which the basic frugal RISC instruction set is supplemented with boost from macrocode ROM. The bus-bandwidth bottleneck is solved by having separate buses for instruction and data and putting a cache/MMU chip on each bus. Putting the caches on separate chips allows them to be large enough to generate hit rates over 90%. Partitioning also allows IEEE 64-bit floating point to be incorporated on CPU chip so there is no off-chip delay (as when going to an external coprocessor). There is no need for CPU to have a separate multiply divide hardware because these operations can be done in the floating-point unit. Performance is 5 MIPS average for C100 and projected to be 2 to 3 times that for C300. The three chips are fabricated in double-metal CMOS with 2-µm geometry for C100 and 1.5-µm for C300. For user convenience, they are sold mounted with clock on a 3.5 x 4.5-in. multilayer C card with 96-pin DIN connector.
You've seen the advantages offered by the A100 Digital Signal Processor. The single-chip DSP solution that features 32 multiply-accumulators, executes up to 320 MOPs, and easily attaches to microprocessors.

Now INMOS speeds A100 system development with the new D704, the complete DSP Development System. The D704 overcomes the clutter normally encountered in developing DSP systems such as hand-crafted assemblers, interleaved busses and power-hungry glue. And since it is tailored for the A100, your end product is first to market and second-to-none in performance.

The D704 combines a comprehensive set of software tools, PC plug-in card and extensive documentation, providing a powerful yet easy-to-use DSP environment. You can experiment with the technology, simulate DSP algorithms in software and run them in real time on the A100's provided on the board.

The A100 is quickly becoming the number one choice in everything from avionics to ultrasonics. And with MIL-STD 883C devices available soon, it will be a natural for military DSP programs of all types. With the D704 Development System, creating DSP solutions has never been easier.

So if you'd like to cut through the clutter, start by clipping the coupon.
SPARC RISC

Availability: From Fujitsu: now for 10 MIPS, 2 qtr '88 for 20 MIPS via gate array. From Cypress: 2 qtr '88 for 20-MIPS full-custom CMOS. From BIT: '89 for bipolar ECL.

Cost: For Fujitsu: $420 (single qty), $200 (OEM qty) for present versions. Prices for other Fujitsu, Cypress, and BIT parts not yet determined.

Second source: Hardware-wise, Fujitsu, Cypress, and BIT SPARC's will be different and probably not compatible. Software-wise, they must all run the Sun-defined SPARC software.

Core: Fujitsu has made a start in this direction with a gate array.

Description: Goal is to set a high-performance RISC-type software standard while allowing maximum hardware flexibility so that multiple vendors can vie for present and future maximum performance. Sun Microsystems defined SPARC at instruction-set and programmer's model level and then entered into entirely separate joint agreements with silicon vendors with the intent of reaching 100-MIPS performance by 1990. Meanwhile Sun provides development hardware and software support via its workstations (with the most recent model, Sun-4, using Fujitsu's 86900 SPARC).

HARDWARE

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<tr>
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<tr>
<td>External memory</td>
<td>Coprocessor</td>
</tr>
<tr>
<td>Data</td>
<td>Control</td>
</tr>
</tbody>
</table>

Notes:
1. Diagram is for Fujitsu 86900. This existing version is most likely the simplest for it uses Fujitsu 1.5-µm CMOS gate array that has only 20k transistors. Fujitsu also supplies gate-array companion chip 86910 that provides interface to Weitek 1164/65 floating-point chip set.
2. Cypress will implement its SPARC in full-custom CMOS using Cypress's 0.8-µm, 2-layer-metal process. The chip set will include integer, floating point, and cache "solutions.
3. BIT will implement its SPARC in bipolar ECL.
4. SPARC stands for scalable processor architecture.

Software

1. Data-manipulation instructions
   - Add, subtract, multiply (step).
   - Logicals and shifts. (Floating point operations via Weitek 1164 and 1165)
2. Data-movement instructions
   - Load and store to memory (in RISCs only simple loads and stores used to external memory).
   - Load and store to CPU registers. Load and store to floating-point registers. Load and store to coprocessor registers.
3. Program-manipulation instr
   - Call subroutine, branch conditional, save and restore, jump and link.
   - (There are 128 hardware and 128 software traps, mostly user definable.)
4. System-level instructions
   - Instruction-cache flush. Can set up system and user modes and associated protection. (Note that address pins define user and system instruction and data spaces.)

Notes:
1. There are four stages of pipelining and it is up to optimizing compiler to prevent pipeline breaks by inserting a delay instruction before branch instructions.
2. Overlapped CPU register file windows are said to allow faster context switching than if usual stack were used.

Specification summary: 32-bit µP family that is standardized at software level but open at hardware level for whatever implementation gives a competitive performance/price ratio. Architecturally it follows the RISC philosophy of minimum instructions (Fujitsu shows about 107) that executes mostly in single cycles (1.3 to 1.7 clocks per instruction). It has a fairly large number of on-chip registers (120) to hold data being processed for rapid access, which also permits the fixed-length instructions to carry the two source and one destination addresses needed for single-cycle operations (register file has 3-port structure). The on-chip registers are partitioned into seven 24-register groups that are overlapped at edges so that parameters can be easily passed between them. There are also eight global registers. Can address 4G bytes of direct address space and 256 pages of 4G-byte indirect space. Addressing supports various user-defined cache configurations. Fujitsu 86900 has separate coprocessor port that couples tightly to Weitek 1164/65 FP chips. Performance ranges from 10 MIPS sustained for Fujitsu 86900 at 16.67 MHz, to 20 MIPS expected of Cypress chip set, to projections of 50 to 100 MIPS by 1990. Floating-point performance for 86900 is 1.2M to 1.5M flops; for Cypress's it will be 5M to 7M flops. Present and planned implementations include CMOS and bipolar and possibly gallium arsenide. Both semicustom (gate arrays) and full-custom design approaches are being used. Strategy is to aggressively upgrade performance by frequent redesign in newer technologies as they emerge. Packages will vary with implementations. Present Fujitsu 86900 gate array has about 256 pins, of which about 190 are shown used.

HARDWARE

<table>
<thead>
<tr>
<th>Support</th>
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<tbody>
<tr>
<td>Silicon vendors refer customers to Sun workstations, indicating that even the older models that use Motorola 68000-family µPs are adequate as Sun maintains software compatibility (obviously the newer models, from Sun-4 onward, which use SPARC, would be ideal). Evaluation board from Fujitsu.</td>
</tr>
</tbody>
</table>

Software

Silicon vendors say they'll pass along Sun's optimizing compilers for C, Pascal, and Fortran as well as Sun's Unix operating system. (Note that in case of RISC machines, the quality of compiler becomes especially important.) Vendors also say that ADA and AI languages ( Lisp) will be available. Fujitsu says it plans to port SPARC software to other Unix environments such as VAXs and PCs (with Unix).
29000 RISC

AVAILABILITY: 4th qtr '87 for 29000 CPU, 1st qtr '88 for 29027 arithmetic accelerator.

COST: Under $500, possibly in the several hundred dollar range initially, but dropping to under $100 with maturity.

SECOND SOURCE: Some discussions but will probably not be decided until after formal introduction.

Description: State-of-the-art implementation of RISC µP concepts with expected stress on obtaining as close to single-cycle operation as possible (even with branching) and a special emphasis on keeping user's system costs down by bus timing, etc, which allows lower-cost external memories. Note that though first two digits of this µP's designation—"29"—are the same as supplier's previous building-block families (see elsewhere in directory), this 29000 family is the opposite architecturally. The other building-block families are intended for user-defined (microcoded) complex instruction sets, whereas this µP has a regular, fixed and purposely simple instruction set; moreover, it is decoded by logic. Companion compilers are an essential part of family.

Notes:
1. Burst-mode addressing allows use of lower-cost video RAMs to replace more-expensive, high-speed, static CMOS RAMs, with only moderate loss in performance (14 MIPS sustained vs 17 MIPS).
2. There is a coprocessor interface to companion 29027 floating-point chip. The 29027 uses combinatorial logic, so operations take only five 29000 cycles.

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HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Add, subtract, multiply (step), divide (step)
Logicals, compare, convert floating point (floating point is not currently implemented in hardware but companion floating-point chip 29027 is available)

II—DATA-MOVEMENT INSTRUCTIONS
Register-to-register moves
load & store to external memory & I/O

III—PROGRAM-MANIPULATION INSTR
Jump, call subroutine, and returns
Branches (with decisions based on Boolean data in general-purpose registers rather than ALU condition codes)

IV—PROGRAM-STATUS-MANIP INSTR
Status register has usual bits to indicate ALU condition

V—SYSTEM-LEVEL INSTRUCTIONS
Some of the 23 special-purpose registers are for system control and are protected and can be set up via software (some also are affected by execution)

Notes:
1. Total of 115 instructions, not all of which are yet implemented in hardware, and only cause traps.
2. Multiply and divide only do a step. RISC has neither microcode for all steps nor space on chip for hardware multiply (as with DSP chips). Possibly the compiler will put in all the steps in software.

Specification summary: 32-bit CPU fashioned after RISC concepts, designed to perform most frequently used, simple instructions in one cycle. Offered with companion compilers intended to take advantage of architectural simplicity and produce code optimized for performance. Also offered with companion floating-point chip, 29027, which in more CISC fashion makes up for crudeness of math instructions (only partial multiplication and division instructions). Features that ensure uninterrupted flow in 29000's 4-stage execution pipeline are single-cycle branching with branch delays and a 512-byte branch-target cache. Main 192-register file has a 3-port configuration so that instruction fields can specify sources for both operands and the destination for the result. 128 of the registers are addressed by a stack pointer that (in conjunction with the compiler) provides a type of "caching" that speeds procedure calling. External memory space is reached by 4G-byte virtual addressing with demand paging. An on-chip 256-entry MMU performs address translation in a single cycle and is flexible so users can choose memory strategy. 25-MHz operating frequency (40-nsec clock period) gives 25-MIPS peak and 17-MIPS sustained performance. Fabricated in 1.2-µm (effective) CMOS with 1.5W power dissipation. Housed in 169-pin PGA.

---

HARDWARE SUPPORT SOFTWARE

Debugging and chip-test aids incorporated in 29000 hardware, some of which are equivalent to having an in-circuit emulator. Can halt and single-step through pipeline. Can jam instructions into instruction register, execute them, and then return to regular code.

Notes:
1. Total of 115 instructions, not all of which are yet implemented in hardware, and only cause traps.
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### Hardware

**Specifications summary:** TTL bus-compatible building blocks for creating moderately high-performance computers and controllers. Slices were originally 4 bits wide but now can be as much as 32 bits wide. Parts include sufficient features for emulating most computer architectures. User defines and product's macroinstruction set by microprogramming μROM. RALUs (2901, 2903, and 29203) respond to 8 and 16 basic instructions (2903 and 29203 include multiply and divide instructions) within one cycle of 50 to 125 nsec (2901C performs 16-bit add in 83 nsec). Original family parts were fabricated entirely from Schottky TTL, but higher-speed ECL has been used for internal parts.

### Software

**User defines macroinstructions set by microprogramming μROM.** Parts respond to the following instructions:

1. **Data-Manipulation Instructions**
   - 2901 performs three arithmetic functions on two operands, as well as five logic functions.
   - 2903A performs seven arithmetic functions and nine logic operations, as well as multiply and divide. Simultaneous add (or subtract) and shift possible.
   - 29203 has floating-point-normalize instruction.

2. **Data-Movement Instructions**
   - 16 working registers in RALU ram can be addressed two at a time for supplying two operands to the ALU simultaneously.

3. **Program-Manipulation Instruction**
   - Defined by user in microcode.

From 3rd parties: Step Engineering (Sunnyvale, CA) offers new lower-cost PC XT/AT-based Microstep microcode development station ($3695). It consists of plug-in card for PC containing 25-ns RAMs to simulate a 128×4k-bit microcode ROM plus debug/control software. It would be used in conjunction with Step's Metastep Microprogram language ($3000, or $6195 bundled with Microstep). Step's full-fledged Step-40 is expensive ($25 to $30), but it has 10-ns, 512×64k-bit microcode ROM. Hardware tools also available from HiLevel Technology (Tustin, CA) and others.

For ASIC: Silicon compilers for members of 2900 family (2901, 2910, 2913 and 2940) are in VLSI Technology's compiler library ($25,000).
**29300/400, 29C300**

**AVAILABILITY:** Most are available but some have been delayed till '88 (see table).

**COST:** As can be seen from table, cost initially in the hundreds of dollars per part, even at 100 qty.

**SECOND SOURCE:** None directly but, especially for CMOS parts, there are now quite a few suppliers who make functionally similar devices, such as TI, Weitek, Wafer Scale Integration, Analog Devices, Cypress, IDT, etc.

**Description:** 32-bit bipolar and CMOS building-block chip set that follows concepts established by 2900 bit-slice family, but with two major differences. First, family members all have a fixed, 32-bit data width. Second, the architecture and resulting microinstruction set are optimized for easy compiler writing. State-of-the-art performance has been achieved, as indicated by 80- to 90-nsec microinstruction cycle times, and a DSP-quality 32×32-bit multiplier that completes within this cycle time. Supplier says it has followed customer advice and left final differences. First, family members all have a fixed, 32-bit data width.

**Description:**

**PART NO** | **DESCRIPTION** | **PERFORMANCE** | **AVAILABILITY** | **COST ($100 QTY)**
---|---|---|---|---
29331 | 18-BIT SEQUENCER | 90 nsec | NOW | $99
29325 | 32-BIT PROCESSOR | 90 nsec | NOW | $239
29332 | 32-BIT ALU | 90 nsec | NOW | $299
29334 | 64x18 REG FILE | 24 nsec | NOW | $89
29340 | BOUNDS CHECKER | 20 nsec | NOW | $66
29338 | BYTE QUE | 35 nsec | IQ = 88 | NA
29C331 | 16-BIT SEQUENCER | 100 nsec | NOW | $180
29C325 | 32-BIT PROCESSOR | 125 nsec | IQ = 88 | NA
29C332 | 32-BIT ALU | 100 nsec | IQ = 88 | NA
29C334 | 64x18 REG FILE | 24 nsec | NOW | $105

Notes:
1. Many different architectures possible because of flexibility of parts.
2. Possibility of sharing dual-ported registers between two ALUs so that address calculation and data manipulation occur simultaneously within cycle. (Each ALU would have its operands and result read and written into a common multiported register file.)
3. Deep pipelining avoided so there can be fast response to decisions.

**SUPPORT**

**From 3rd parties:** Step Engineering (Sunnyvale, CA) offers new lower-cost PC XT/AT-based Microstep microcode development station ($3695). It consists of plug-in card for PC containing 25-nsec RAMs to simulate a 128×4-bit microcode ROM plus debug/control software. It would be used in conjunction with Step's Metastep Microprogram language ($3000, or $6195 bundled with Microstep). Step's full-fledged Step-40 is expensive ($25 to $30) but it has 10-nsec, 512×64-bit microcode ROM. Hardware tools also available from HiLevel Technology (Tustin, CA) and others.

**32-BIT BIPOLAR AND CMOS**

**Advanced Micro Devices**

901 Thompson Pl
Sunnyvale, CA 94086
Phone (408) 732-2400

**Status:** Supplier now has two very different architectures targeted at high-performance 32-bit applications. AMD's new 29000 µP (also in directory) may have the same first two digits as this 29300, but it is entirely different. The 29000 is RISC, rather than CISC like this 29300. RISC chips use combinational logic to get instructions down to single-cycle execution. The 29300 family described here is just the opposite; the 29300's instructions are made up of multiple cycles executed out of a microcode ROM. From the viewpoint of the microcode system design, it could be said that this 29300 architecture favors wide horizontal microcode whereas the 29000 RISC favors narrow vertical instructions; thus AMD is now involved in both extremes of the CISC-vs-RISC controversy (both with similar performance).

**I—DATA-MANIPULATION INSTRUCTIONS**

For 332 ALU: includes 64-bit n-bit shift-up/down funnel shifter that can be combined with logic functions. Multiply and divide (one bit at a time). Priority encoding to support floating-point operations and graphics. For 325 floating point: efficient execution of Newton-Raphson division and Horner's method of polynomial evaluation. Both IEEE and DEC formats (addition, subtraction, multiplication) with conversion between two modes.

For 323 32×32-bit multiplier: single- or double-precision multiply in one or four cycles, respectively.

**II—DATA-MOVEMENT INSTRUCTIONS**

For 334 64×18-bit register file (cascaded for full word width and desired length and used in conjunction with ALU): individual write for byte, 16-bit half word, or 32-bit full word.

**III—PROGRAM-MANIPULATION INSTR**

For 331 microprogram sequencer: instructions designed to support high-level-language constructs

The 33-level stack supports interrupts, loops, subroutine nesting, and multitasking at microlevel

Microtrapping for reuse of prior microinstruction

No support for relative addressing, as designers wanted to avoid performance penalty of adder, but decisions and interrupts handled on chip for fastest response.

**IV—PROGRAM-STATUS-MANIP INSTR**

Status registers in ALU, floating point, etc.

Notes:
1. Designers say they endeavored to keep instructions orthogonal and symmetrical to ease task of compiler writing and facilitate structured microprogramming.
2. Self-checking implemented by parity bits in register file and by parity in off-chip data paths and ability to parallel units and compare results.

**Specification summary:** Building blocks for 32-bit-wide microprogrammable computer systems. Core set includes five parts (see table) that can stand alone or be used in mixed systems. Architecture supports features needed on advanced minicomputers, like parity checking and master/slave functional comparisons. Also suited for direct, very-fast execution of high-level languages via compiled microcode. Triple databus architecture, with unidirectional buses for minimum speed loss caused by bus turnaround. Parts have 20- to 30-nsec throughputs so that 70- to 80-nsec microinstruction cycles can be accomplished. Architecture sufficiently open to allow inclusion of performance accelerator, and family includes floating-point unit (125 nsec) and 1-cycle fixed-point multiplier (80 nsec). Bipolar technology with off-chip TTL interfaces. Packages incorporate three low-profile horizontal fins to handle 4 to 7W heat dissipation. Fins are horizontally oriented so that cooling airflow can be in any direction and package height will be low enough (0.4 in.) to allow normal board spacing. Required cooling airflow (300 cfm) is said to be within allowable limits for office environments. CMOS versions will dissipate in the 1W range and will not require heat sinks or cooling airflow.
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least hassle. Which means you can spend more time perfecting the rest of your application.

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Our low cost ICE™ 196 PC development tool gives you more for less, too. Together with high-level languages like PL/M and C, it delivers the easiest, lowest-cost design support you can get.

Further support is available from the world's largest network of field applications engineers. Plus customer workshops to get you up to speed fast.

So you see, there's really no easier or more powerful answer to embedded real-time control than Intel's 80C196. For complete technical information, call toll-free (800) 548-4725 and ask for Literature Department W398.

Do it now. And relax. Because we're ready to meet your demands.
74AS8XX/74AS88XX

AVAILABILITY: Now for 8XX parts and first 88XX parts, though many are nearly 6 months behind promised schedule (see table).

COST: See table for prices.

SECOND SOURCE: None, but see AMD 29300/400 and Analog Devices

Word Slice for similar families (typically designers mix and match between families)

Description: 8- and 32-bit custom CPU building-block chip sets done in high-performance bipolar and CMOS processes. Cycle times of 50 to 75 nsec worst case said to be accomplished at relatively low power-dissipation levels even for bipolar members, so no heat sinking is required. Family architecture facilitates byte operation, allowing for flexibility in data-word manipulation and resulting in system throughput in the 10-MIPS range.

HARDWARE

<table>
<thead>
<tr>
<th>PART NO</th>
<th>DESCRIPTION</th>
<th>PERFORMANCE (nsec)</th>
<th>NO OF PINS</th>
<th>AVAILABILITY</th>
<th>COST (100 QTY)</th>
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</thead>
<tbody>
<tr>
<td>74AS890</td>
<td>8-BIT REGISTER ALU</td>
<td>46</td>
<td>68</td>
<td>NOW</td>
<td>$30</td>
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<tr>
<td>74AS900</td>
<td>14-BIT MICRO-CONTROLLER</td>
<td>1</td>
<td>68</td>
<td>NOW</td>
<td>$40</td>
</tr>
<tr>
<td>74AS97</td>
<td>74ACT3232</td>
<td>50</td>
<td>68</td>
<td>NOW</td>
<td>$40</td>
</tr>
<tr>
<td>74AS970</td>
<td>DUAL 16-W/32-BIT REGISTER</td>
<td>22</td>
<td>24</td>
<td>NOW</td>
<td>$6/4</td>
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<tr>
<td>74AC832</td>
<td>32-BIT REGISTER ALU</td>
<td>50-75</td>
<td>28</td>
<td>NOW (SAMPLES)</td>
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<td>74AC835</td>
<td>16-BIT MICRO-SEQUENCER</td>
<td>20-35</td>
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<td>NOW (SAMPLES)</td>
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<tr>
<td>74AS834</td>
<td>64-W/320-BIT REGISTER FILE</td>
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<td>NOW (SAMPLES)</td>
<td>NA</td>
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<td>74AS833</td>
<td>BARREL/FUNNEL SHIFTER</td>
<td>10</td>
<td>15</td>
<td>NOW (SAMPLES)</td>
<td>NA</td>
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<tr>
<td>74AC831</td>
<td>32/16-BIT榕</td>
<td>25</td>
<td>15</td>
<td>NOW</td>
<td>$40</td>
</tr>
<tr>
<td>74ACT836</td>
<td>32X2-BIT MULTIPLIER</td>
<td>80</td>
<td>NA</td>
<td>NOW (SAMPLES)</td>
<td>NA</td>
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<tr>
<td>74AC7832</td>
<td>FLOATING-POINT PROCESSOR</td>
<td>100</td>
<td>NA</td>
<td>NOW (SAMPLES)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Notes:
1. Family architecture facilitates the high degree of system parallelism possible with "wide" microcoding, allowing designer to operate devices simultaneously for greater throughput.
2. ALU and microcontroller support master/slave operation for tandem processing.
3. All members are 2-μm bipolar except for 8836 and 8837, which will start out in 1-μm CMOS. The bipolar will achieve low (4W) power dissipation because of special Schottky transistor logic that operates at 2V internal supply. Because of large die size (in order of 100k sq mils) and complex structure (two Schottky barrier metals are used), these circuits are likely to start off with low yields.

8- AND 32-BIT BIPOLAR AND CMOS

Texas Instruments Inc
15356 N Central Expressway
Dallas, TX 75265
Phone (214) 995-6611

Status: Supplier expects to compete with similar AMD bipolar 29300/400 for applications in high-end workstations, graphic engines, and performance-driven superminis. Supplier's chips may also receive competition from new CMOS RISC μPs such as Clipper, SPARC, and AMD 29000 (all in directory) as well as Weitek Accel (not in directory). These CMOS devices have MIPS rates similar to those of the bipolar chips, though the RISC chips don't allow designers the architectural flexibility to achieve higher levels of parallelism. With respect to bipolar-vs-CMOS controversy, TI engineers tell us they have found it expedient to convert some bipolar parts to CMOS (even after bipolar samples were put out) because CMOS has been better at meeting desired specs.

SOFTWARE

Notes:
1. Family architecture facilitates the high degree of system parallelism possible with "wide" microcoding, allowing designer to operate devices simultaneously for greater throughput.
2. ALU and microcontroller support master/slave operation for tandem processing.
3. All members are 2-μm bipolar except for 8836 and 8837, which will start out in 1-μm CMOS. The bipolar will achieve low (4W) power dissipation because of special Schottky transistor logic that operates at 2V internal supply. Because of large die size (in order of 100k sq mils) and complex structure (two Schottky barrier metals are used), these circuits are likely to start off with low yields.

Supplier recommends same approach for development systems as that used with other microwaved building-block chip sets such as the 2900.

Third-party support available from Hewlett-Packard, HiLevel Technology (Tustin, CA), and Step Engineering (Sunnyvale, CA). High-speed microcode ROM emulators from above companies cost $13,000 to $30,000. Supplier's evaluation module (EVM) board incorporates a full Basic interpreter and monitor program that can be accessed through an RS-232C port using a nonintelligent terminal or terminal emulator (personal computer with appropriate software).
**WORD-SLICE GP NUMERIC PROCESSOR**

**AVAILABILITY:** Now for most parts; see table.

**SECOND SOURCE:** No direct source, except for industry-standard multipliers. Similar functions are available from AMD, Cypress Semicon­ductor (San Jose, CA), Integrated Device Technology (Santa Clara, CA), Wafer Scale Integration (Fremont, CA), Weitek (Sunnyvale, CA), and many others.

**Description:** Follows trend established with 2900 bit-slice family of many others.

**multipliers. Similar functions are availab­le from AMO, Cypress Semicon­ductor (San Jose, CA), Integrated Device Techno­logy (Santa Clara, CA), generators that could be used with supplier's floating- and fixed-point suppliers' floating- and fixed-point systems. This family has been found suitable for general multipliers to design complete systems.

**COST:** $27 to $300; see table.

**Suitable ROM-simulation systems are available from Step Engineer­ing and HiLevel Technology (Tustin, CA). Similar aids are offered by Tektronix and Hewlett-Packard.**

**Notes:**

1. Architecture shown is only one of many possibilities.
2. Microcode memory can be 64k deep. It can be as wide as designer needs for simultaneous control of one or more data pipes (typically approximately 100 bits).
3. Microcode memory can be RAM for downloading of algorithms from host.

**16-BIT CMOS μP BUILDING BLOCKS**

**Analog Devices Inc**

**Digital Signal Processing Div**

**Norwood, MA 02062**

**Phone (617) 461-3881**

**Status:** Supplier originally thought of this chip set (or building blocks) for DSP applications but then found that parts (especially double-precision floating point) were more likely to be used for general-purpose high-end bit-slice-type μPs intended for math-intensive applications.

**I—DATA-MANIPULATION INSTRUCTIONS**

For ADSP-1101 16-bit integer arithmetic unit:

- Add and subtract, multiply, multiply and accumulate (MAC)
- Dual 40-bit accumulator control and internal feedback
- Logicals and shifts
- Block floating-point shifters and control

For ADSP-321X/2X floating-point multipliers and ALUs:

- Multiply single-precision floating point, double-precision floating point, and 32-bit fixed point
- Complete arithmetic and logical ALU operations
- Complete format-conversion operations

**II—DATA-MOVEMENT INSTRUCTIONS**

For ADSP-1410 16-bit address generator:

- Preupdate and postupdate mode conditional looping (zero overhead)
- Add or subtract increments or offsets to pointers
- Register transfers
- Logicals and shifts
- Bit-reverse output (for FFT)

**Specification summary:** Microprogrammable chips set for numerical processing, permitting increased throughput by user-developed parallelism. Consists of various multipliers and multiplier accumulators (see table) and microcode program sequencers and address generators (see table), and, in this clocked, can be driven by a 10-MHz clock, and within resulting 100-nsec cycle can perform complete instructions (obtain data from memory and process it). Most recent versions support 50-nsec cycle. Sequencer helps host computer download code into a RAM microprogram store (for accelerator applications). Fabricated in CMOS.

**PART | DESCRIPTION | AVAILABILITY | COST (100 QTY)**

| 3201 | MULT , SINGLE PRECISION , FP | NOW | $97 |
| 3202 | ALU , SINGLE PRECISION , FP | NOW | $97 |
| 3210 | MULT , FP | NOW | $300 |
| 3211 | ADD , 8-BIT | NOW | $300 |
| 3212 | MULT, FP (IEEE) | 4Q ‘87 | $297 |
| 3213 | MULT , FP (DEC) | 4Q ‘87 | $297 |
| 3220 | ALU , FP | NOW | $300 |
| 3221 | ALU , FP | NOW | $300 |
| 3222 | ALU , FP (IEEE) | NOW | $297 |
| 3223 | ALU , FP (DEC) | 4Q ‘87 | $297 |

**III & IV—PROGRAM-MANIPULATION AND -STATUS INSTR**

For ADSP-1401 16-bit program sequencer:

- Jump and branch-absolute, relative and indirect
- Push, pop data, counters and pointers to subroutine stacks
- Modify subroutine stack and register stack pointers
- Interrupt masking and control
- Writable control store (for downloading)

Mnemonics with microcode fields are available from the supplier for use with a meta-assembler. These programs can be used by a designer to create a design-dependent assembly-level language. Step Engineering, HiLevel Technology, and Microtek Research meta-assemblers support parts via definition files for Wordslice mnemonics.
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Going beyond even A+ screening, P+ involves a dynamic self-heating accelerated burn-in that tests a device at thermal shutdown. This approach has been proven more effective than standard 125°C burn-in as an early screen for infant mortality defects in power devices, such as regulators.

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---

National's Low Dropout Regulator Family

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2925</td>
<td>Low dropout, 5 V, 750 mA with delayed reset</td>
</tr>
<tr>
<td>LM2930</td>
<td>Low dropout, 3-terminal, 5 V or 8 V, 150 mA</td>
</tr>
<tr>
<td>LM2931</td>
<td>Low dropout, low quiescent current, 5 V or adjustable, 100 mA</td>
</tr>
<tr>
<td>LM2935</td>
<td>Low dropout, dual 5 V for memory keep-alive, 750 mA or 10 mA</td>
</tr>
<tr>
<td>LM2940C</td>
<td>Low dropout, 5 V, 12 V, or 15 V, 1 A</td>
</tr>
<tr>
<td>LP2950/2951</td>
<td>Low dropout, micropower, 5 V or adjustable, 100 mA</td>
</tr>
<tr>
<td>LM2984</td>
<td>Low dropout, 3 tracking 5 V outputs with watchdog</td>
</tr>
</tbody>
</table>

National Semiconductor
Linear Solutions
P.O. Box 58090
Santa Clara, CA 95052-8090
PMI's newest high speed op amp guarantees slew rate of 50V/µs and settling time of 1µs to 0.01%. With its 10MHz gain bandwidth and 850kHz full power BW, the OP-42 combines high speed with accurate DC performance.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>OP-42</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>750µV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A_VOL</td>
<td>500,000</td>
<td>Min</td>
<td></td>
</tr>
<tr>
<td>CMR</td>
<td>88dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCVOS</td>
<td>10µV/°C</td>
<td>Max</td>
<td></td>
</tr>
</tbody>
</table>

Guaranteed unity gain stability, capacitive load tolerance, and clean transient response make the OP-42 easy to use . . .

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Designer’s Guide to Switching Power Supplies

Part 2

Galvanically isolated switching supplies provide high power

Part 1 of this 2-part series dealt with simple switching power supplies and described a “cut and try” approach for stabilizing a supply’s feedback loop. The conclusion offers advice on designing more complicated switching supplies, ones with isolated outputs.

Jim Williams, Linear Technology Corp

The fundamental difference between the switching supply in Fig 1 and the circuits presented in Part 1 (Ref 1) is that Fig 1’s output is galvanically isolated from its input—often a requirement for telecommunications equipment. Such isolation necessitates a transformer rather than a simple 2-terminal inductor, and also requires that feedback passes to the regulator across a nonconducting path. The requirement for a transformer complicates the circuit’s start-up and switching characteristics, and the need for isolated feedback complicates frequency compensation.

In this circuit, the VIN pin receives power from a transformer winding. Obviously, the winding can’t supply power at start-up because the circuit isn’t functioning. Q1-Q4 solves this power-up problem. When you apply power to the supply, Q3 can’t conduct because the LT1071 doesn’t have any power going to it. Q1, Q2 (which functions as a zener diode in this circuit), and Q3 are off. Under these conditions, Q1 is on, pulling the VC pin down and strobing off the LT1071. (The circuits in this article use the lower-current, lower-cost LT1071, rather than the LT1070 used in Part 1.)

The potential at Q1’s emitter slowly rises as the 10-kΩ/100-µF combination charges. When Q1’s emitter rises high enough, Q1 turns on. Zener-connected Q3 conducts when the voltage across it is about 7V, biasing Q3 on. Q1 then sees regenerative feedback, which turns on Q3 harder. As Q1 turns on, it cuts off Q2, allowing the VC pin to rise and turning on the LT1071.

Soft-start characteristic helps

The 10-µF/diode combination limits the rate of rise at the VC pin and forces the VC pin to come up slowly, providing a soft-start characteristic. This delay prevents start-up at starved or unstable VIN voltages, which could cause erratic or destructive modes of operation. The 100Ω/diode string discharges the 10-µF capacitor on removal of circuit input power.

When start-up does occur, the transformer feeds the VIN pin with dc via the 50Ω resistor and the MUR120 rectifier diode. The 50Ω resistor combines with the 100-µF capacitor to provide good ripple and transient filtering. This voltage is ample to run the LT1071 and reduces the current through the 10-kΩ resistor, saving power. Q1, Q2, and Q3 remain on, biasing Q4 to permit operation of the LT1071.
With transformers, unlike inductors, all of the flyback energy doesn’t end up in the output capacitor.

In the flyback circuits described in the first part of this article, the \( V_{SW} \) pin drove the inductor directly. The output capacitor clamped the output voltage and dumped the flyback energy directly into the output capacitor; excessive voltages did not occur. In Fig 1, however, a transformer takes the place of the inductor, and its flyback characteristics are different from a simple 2-terminal inductor.

In the case of the transformer, all the flyback energy doesn’t end up in the output capacitor. Substantial flyback-voltage spikes (>100V) appear across the transformer’s primary.

Certain measures prevent these spikes from destroying the circuit. The 0.47-µF/2-kΩ/diode combination across the transformer’s primary (a damper network) conducts during the flyback action, which loads the transformer’s primary and minimizes flyback amplitude. You have to select the damper network’s values empirically, and you have to weigh the damping effectiveness vs the power dissipation in the damper network. Very low resistance values markedly reduce flyback potential, but cause excessive dissipation. High damping-resistor values limit dissipation, but allow excessive flyback voltages. You should select the damp-
er values under fully loaded conditions because flyback energy is proportional to transformer power levels.

Even with the damper network, however, the flyback voltage is too high for the LT1071's output transistor. Qs, in series with the LT1071's output transistor, prevents the LT1071 from seeing the high voltage. In this configuration, sometimes called a cascode, Qs's high standoff rating blocks the high voltage and lets the LT1071 operate well within its breakdown limits.

Parasitics pass spikes

Qs confers mixed blessings, though. Large parasitic capacitances are associated with all its terminals and during switching, these capacitances can allow excessive transient voltages to appear in unexpected places. The 18V zener diode guarantees against gate-source breakdown (VGS max = 20V), and the MUR120 diode clamps the VSW pin to the VIN potential.

The transformer's secondary gets rectified and filtered to produce the 5V output. This output is galvanically isolated from the circuit's input. To preserve isolation, the feedback path must also be galvanically isolated. IC1, the optoisolator (4N28), and associated components serve this purpose. IC1, powered by the 5V output, compares a resistively sampled portion of the output with the LT1004 1.2V reference. Operating at a gain of 200, it drives the optoisolator's LED.

The optoisolator's output transistor, in turn, biases the LT1071's VC pin, closing the regulation loop. The IC1/optoisolator combination essentially bypasses the feedback amplifier inside the LT1071. Normally, the drift of the optoisolator's transmission characteristics over time and temperature would result in unstable feedback. Here, IC1's gain comes ahead of the optoisolator, which attenuates the uncertainties and provides a stable loop. The ground return for the optoisolator goes through a zener diode having the same voltage as VREF instead of directly to ground. This routing forces the op amp to bias well above ground, minimizing saturation effects during output transients.

Compensation is more complex

As stated earlier, frequency compensation is somewhat involved. The 0.1-µF capacitor rolls off IC1's gain. This roll-off keeps the gain low at high frequencies, preventing amplified ripple and noise from feeding back to the LT1071. The 36-kΩ/0.47-µF combination gives significant gain reduction under transient conditions. Local compensation at the LT1071's VC pin stabilizes the loop. The 100Ω resistor at the 5V output, a deliberate path for sinking current, ensures loop stability for a light load or for no load. The 50Ω resistor at Qs combines with the gate's capacitance to slightly slow FET switching, reducing high-frequency harmonics.

Circuit waveforms appear in Fig 2. Trace A in Fig 2a is Qs's drain voltage, and trace B shows the drain current. Trace A indicates that, due to flyback effects, the MOSFET sees about 100V. The ringing upon turn-off is normal. Trace B shows that the current is fast, clean, and controlled. In b, trace B is Fig 1's transient response for a 1A step added to a 2.5A output. When trace A goes high, the step occurs. Trace B indicates that output sag is corrected in about 8 msec.

Fig 2—In a, trace A shows Fig 1's Qs drain voltage and trace B shows the drain current. Trace A indicates that, due to flyback effects, the MOSFET sees about 100V. The ringing upon turn-off is normal. Trace B shows that the current is fast, clean, and controlled. In b, trace B is Fig 1's transient response for a 1A step added to a 2.5A output. When trace A goes high, the step occurs. Trace B indicates that output sag is corrected in about 8 msec.
You have to weigh the damping effectiveness vs the power dissipation in the damper network.

When trace A returns low, the 1A load is removed and recovery is similar to the positive step. The optional output filter (Pulse Engineering part #52901, San Diego, CA) in Fig 1 will reduce broadband output noise to about 75 mV p-p.

One of the most desirable switching-supply circuits is also one of the most difficult to design. Fig 3's circuit exhibits many similarities to Fig 1, but derives its power directly from the 115V ac line. Off-line operation is preferable because it eliminates large, heavy, and inefficient 60-Hz magnetic components and filter capacitors. This particular circuit provides an isolated 5V,

### Choosing a diode can be surprisingly tough

“Simple” diodes furnish a good example of how carefully you must consider a switching supply’s operating conditions while designing. Switching diodes have two important transient characteristics: reverse-recovery time and forward turn-on time.

Reverse-recovery time occurs because the diode stores charge during its forward-conducting cycle. This stored charge causes the diode to act as a low-impedance conductive element for a short period of time after reverse drive gets applied. You measure reverse-recovery time by forward-biasing the diode with a specified current, then forcing a second, specified current backwards through the diode. The time required for the diode to change from a reverse-conducting state to its normal reverse-nonconducting state is the reverse-recovery time.

Hard turn-off diodes switch abruptly from one state to the other following reverse-recovery time. They therefore dissipate very little power even with only moderately short reverse-recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable power dissipation in a diode during its turn-off interval.

Fig Aa shows typical current and voltage waveforms for three common diode types (fast, ultra-fast, and Schottky) used in fly-back converters and when \( V_{\text{IN}}=10\text{V} \) and \( V_{\text{OUT}}=20\text{V} \), 2A. Long reverse-recovery times can cause significant extra heating in the diode or the power switch. The total power dissipation during the reverse-recovery time is

\[
P_{\text{RR}} = V \times f \times t_{\text{RR}} \times I_F,
\]

where \( V \) = diode reverse voltage, \( f \) = switching frequency, \( t_{\text{RR}} \) = reverse-recovery time, and \( I_F \) = diode forward current just prior to turn-off.

For a boost-configuration switching supply where \( I_F = 4\text{A} \), \( V = 20\text{V} \), and \( f = 40\text{ kHz} \), for example, the diode’s on current is twice the output current. A diode with \( t_{\text{RR}} = 300 \text{ nsec} \) creates a power loss of

\[
P_{\text{RR}} = 20(40 \times 10^3)(300 \times 10^{-8}) = 0.96\text{W}.
\]

If this same diode has a forward voltage of 0.8V at 4A, its forward loss will be 1.6W. Reverse-recovery losses in this example are nearly as large as forward losses. You must realize, however, that reverse losses don’t necessarily result in significant increases in diode dissipation. A hard turn-off diode will shift much of the power dissipation to the power switch, which will see high current and high voltage during the reverse-recovery time. This stress need not be harmful to a properly selected power switch, though the power loss remains.

The effects associated with diode turn-on time can potentially be more harmful than reverse turn-off effects. Consider that the output diode clamps the inductor’s or transformer’s output connection and prevents it from rising higher than the output voltage. A diode that turns on slowly can have a very high forward voltage impressed across it for the duration of the turn-on time.

The problem is that this increased voltage appears across the power switch. The graphs in Fig Ab show diode turn-on spikes for the three types. The actual height of the spike will depend on the rate of the current rise and the initial current value; nonetheless, the graphs emphasize the need for fast turn-on characteristics in applications that strain the limits of the switch-voltage ratings.

Fast diodes can prove useless if your circuit has excessive stray inductance in the diode, output capacitor, or regulator.
20A output as well as isolated ±12V, 1A outputs. It operates over a 90 to 140V ac input range, includes ac line-surge suppression and soft-start capability, and promises loop stability under all conditions. Efficiency exceeds 75%.

Before describing this circuit's construction, it's vital that you're aware of the need for extreme caution during testing or use: AC line-connected, high-voltage potentials are present.

The diode-bridge/470-µF-capacitor combination rectifies and filters the ac-line power. The metal-oxide varistor (MOV) device provides surge suppression, and loop. For instance, 20-gauge hook-up wire has 30 nH/in. of inductance. The current-fall rate of the LT1070 switching-regulator IC's (Linear Technology Corp, Milpitas, CA) power switch is 10³A/sec. This rate generates a voltage of

\[ (10^3)(30\times10^{-9}) = 3 \text{V/in.} \]

in the stray wiring. Keep the diode, capacitor, and ground and switch lead lengths short.

**Fig A**—Shown here are typical current and voltage waveforms for three common diode types (a) \((V_{IN}=10V, V_{OL}=20V, 2A)\). Long reverse-recovery times can cause significant additional heating in the diode or the power switch. The graphs of the diodes' turn-on spikes (b) emphasize the need for fast turn-on characteristics in applications that push the limits of switch-voltage ratings.
Power-switching parasitics can allow excessive transient voltages to appear in unexpected places.

the thermistor limits turn-on in-rush current. Start-up and soft-start circuitry are similar to that of Fig 1's, with some changes necessitated by the higher input voltage. The 220-kΩ/1.24-kΩ divider prevents erratic operation at extremely low ac-line voltages (70V ac); at such levels, the divider forces the LT1071's feedback pin to a low state, shutting down the circuit.

The high input voltage, typically 160V dc, means that the LT1071's internal current limit is set too high to protect the regulator if the circuit's output gets shorted. Q6 and associated components provide about 2 amps of current limiting. The LT1071's ground-pin current doesn't go directly to ground; instead, it flows through the 0.3Ω resistor, turning on Q6 if current is too high. The 22-kΩ/50-pF RC network filters noise, preventing erratic Q6 operation.

Qo, a power MOSFET, is in a cascode configuration with the LT1071 to withstand the necessary high-voltage switching. Qo has a 500V voltage-breakdown rating. The switch circuit is similar to that of the one in Fig 1. The 50Ω resistor in the gate circuit combines with the gate capacitance to slow Qo’s transitions slightly, thus reducing high-frequency harmonics. Reducing the harmonics eases layout considerations. The transformer's damper network is borrowed from Fig 1; only the component values are reshuffled.

The IC/optoisolator feedback loop preserves the transformer's galvanic isolation and is also similar to

Fig 3—This switching supply operates directly from the 115V ac line. Off-line operation is desirable because it obviates the need for large, inefficient 60-Hz magnetic components and filter capacitors.
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Off-line operation is desirable because it eliminates large, heavy, and inefficient 60-Hz magnetic components and filter capacitors.

that of the one in Fig 1. Compensation values for IC₁ and the LT1071 are different, reflecting this circuit’s different gain-phase characteristics.

Checklist will help

In conclusion, no matter whether you need to design a simple switching supply like those delineated in Part 1 or an isolated one like the supplies described here, your design will proceed more smoothly if you remember the following advice.

• Always consider inductive flyback effects. Are semiconductor-breakdown ratings adequate to withstand them? Will you need a snubber (dampener) network? Consider all possible voltages and current paths, including the transient ones via semiconductor-junction capacitances.

• Account for all of the capacitors’ operating conditions. Voltage ratings are the most obvious consideration, but remember to plan for the effects of ESR and inductance. These specifications can have a significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult.

• Keep in mind that layout is vital. Don’t mix signal, frequency compensation, and feedback returns with high-current returns. Arrange the grounding scheme to achieve the best compromise between ac and dc performance. In many cases, a ground plane may help. Account for the possible effects of stray inductor-generated flux on other components, and plan your layout accordingly.

• Analyze the semiconductor-breakdown ratings thoroughly, and allow for all conditions. Transient events usually cause the most trouble because they introduce stresses that are often hard to predict. Watch for the effects of feedthrough via semiconductor-junction capacitances. Such capacitances can permit excessive voltages for brief intervals at what is nominally a low-voltage node. Carefully study the breakdown, current-capacity, and switching-speed ratings on the data sheets. Ask yourself if the test conditions match your application; if you have any doubts, consult the manufacturer.

• Don’t forget that the most common problem area with switching-supply designs is the inductor or transformer and that the most common difficulty involves saturation. Saturation can often result in destructive failures. An inductor or transformer becomes saturated when it can’t hold any more
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Layout is vital. Don’t mix signal, frequency-compensation, and feedback returns with high-current returns.

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<thead>
<tr>
<th>TRACE</th>
<th>VERTICAL</th>
<th>HORIZONTAL</th>
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<tr>
<td>A</td>
<td>20V/DIV</td>
<td>50 μSEC/DIV</td>
</tr>
<tr>
<td>B</td>
<td>50V/DIV</td>
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</tr>
<tr>
<td>C</td>
<td>500 mA/DIV</td>
<td>50 μSEC/DIV</td>
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**Fig 6**—Compared with Fig 5, this scope photo shows a longer drive pulse, allowing more inductor current buildup. The current ramp waveform is clean and controlled, meaning that the inductor has enough capacity.

Taking a look at the test circuit in **Fig 4** will help to illustrate the importance of the previous advice. The pulse generator drives Q1, forcing current into the inductor. The diode/RC combination forms a typical load. In **Fig 5**, the voltage at Q1’s collector falls when it turns on (trace A is the pulse-generator output, and trace B is Q1’s collector). Trace C, the inductor current, ramps up in a controlled fashion. When Q1 goes off, the current falls and the inductor rings off.

In **Fig 6**, the drive pulse is longer, allowing more inductor-current buildup. This buildup requires that the inductor store more magnetic flux, but the ramp waveform is clean and controlled, indicating that the inductor has the necessary capacity.

**Fig 7** shows some unpleasant surprises. The drive pulse is longer still, and the inductor current departs from its linear ramp shape and changes to a nonlinear slope. The nonlinear behavior starts between the third and fourth vertical divisions, and the curve shows rapidly increasing current. The inductor is becoming saturated. If the pulse width increases much more, the current will rise to a destructive level. You should be aware that some inductors saturate much more abruptly than this one.

**Reference**


**Author’s biography**

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at MIT. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

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Use of transimpedance amplifiers minimizes design tradeoffs

Transimpedance amplifiers, unlike standard voltage-input designs, maintain constant bandwidth regardless of the gain setting. You can use these amplifiers in video-speed and RF circuitry without having to decrease the gain at high frequencies, while maintaining good dc performance and low power consumption.

Alan Hansford, Analog Devices Inc

In video-speed and RF applications ranging from buffers for flash A/D converters to ultrahigh-speed sample/hold amplifiers, you can use the transimpedance amplifier—a special type of operational amplifier—to enhance circuit performance. Transimpedance amplifiers offer several performance benefits over standard voltage-input amplifiers (see box, "Compare amplifier configurations").

The transimpedance amplifier's primary benefit is that its bandwidth is relatively independent of gain. For example, a hybrid transimpedance amplifier with a unity-gain bandwidth of 100 MHz will have a 95-MHz bandwidth at a gain of 10 and a 75-MHz bandwidth at a gain of 20. A monolithic transimpedance amplifier can deliver a 40-MHz unity-gain bandwidth and still maintain a 30-MHz bandwidth at a gain as high as 30.

Small-signal bandwidths in excess of 40 MHz usually exact great dc-performance sacrifices in an amplifier. Many high-speed applications, however, still require low offset voltages, drift, and low power consumption. Such applications are made to order for transimpedance amplifiers: The AD9610 hybrid transimpedance amplifier, for example, specs a ±0.3-mV offset voltage, 5 µV/°C offset voltage drift, and 630-mW typ power dissipation (see box, "Inside a transimpedance amplifier").

Improving pulse-repeater performance

You can take advantage of transimpedance amplifiers in some specific circuit designs, such as pulse repeaters, fast flash converters, ultrafast S/H amplifiers, and subranging A/D converters. Fig 1 shows how you can use a transimpedance amplifier in a pulse-repeater design.

Large values of distributed capacitance develop signal losses in long cable runs inside systems. By placing a pulse repeater at appropriate intervals along the cable, you can recover a distorted signal and retransmit it at near-original quality. In contrast, simple analog amplification would amplify the cumulative distortion effects along with the original signal.

In the pulse-repeater circuit illustrated in Fig 1a, the noninverting stage of the transimpedance amplifier (IC2) makes use of high gain and output limiting to create a square-wave output pulse, regardless of the shape of the input signal. When you configure IC2 for a gain of 10, you'd normally expect low-level input signals...
The transimpedance amplifier's primary benefit is that its bandwidth is relatively independent of gain.

to drive the output to full scale (either plus or minus). In this circuit, however, the output never reaches full scale, because two parallel diode strings are connected between ground and the output of IC₂. The diode strings limit feedback current when the transimpedance amplifier's output exceeds the forward-conduction voltage.

The 66Ω feedforward resistor also limits feedback current and prevents oscillation. The 1700-pF capacitor helps to stabilize the output waveform at the threshold's clipping level. The polarity of the input signal determines which of the two suggested divider networks you should use. The positive feedback through R₁ and R provides a small amount of hysteresis to

---

**Fig 1**—This pulse repeater recovers and retransmits a distorted signal at nearly its original quality. You can configure the pulse repeater for noninverting (a) or inverting (b) operation.
improve noise immunity and eliminate false switching.

The output of IC₁ determines precise switching levels by providing IC₂ with a low-impedance reference-voltage source. You should adjust the switching levels so that the pulse duration equals that of the original transmitted pulse.

You can also configure this circuit to operate in an inverting mode (Fig 1b). This pulse repeater operates as the noninverting circuit does, except for one difference—the positive and negative clipping points equal the forward bias voltage of the diode strings. As in Fig 1a's circuit, in Fig 1b the clipping levels are still related to stage gain, and the hysteresis and switch-point settings are the same as before.

Transimpedance amplifiers can also benefit high-speed, flash A/D-converter designs, which require input-buffer amplifiers that have high bandwidths and can drive large capacitances. Most monolithic amplifiers, in contrast, run out of usable bandwidth at about 50 MHz and can supply output currents of only 10 mA.

The overall performance of a high-speed conversion circuit depends on how well you match the input signal level to the input range of the A/D converter. Most flash converters operate over the 0 to 2V analog input range. Normally, you can use a standard gain stage for low-level input signals. However, when the input signal is greater than the A/D converter's input range, you should use the circuit shown in Fig 2. In that circuit, the transimpedance amplifier (IC₁) provides attenuation and sufficient output current to drive a 150-MHz flash

**Fig 2—The overall performance of high-speed conversion circuitry, such as the flash A/D converter shown here, depends on how well you match the input signal level to the input range of the A/D converter. A hybrid transimpedance amplifier can readily provide the fast slew rates and high current required by a flash converter's capacitive input.**
By using a 2-stage approach, you can build an S/H amplifier that has a fast acquisition time and long-term stability.

A/D converter (IC2) that has an input capacitance of 17 pF. Although IC2 has a 150-MHz encode rate, its small-signal analog bandwidth is 115 MHz, which is well within the speed range of the AD9610 transimpedance amplifier.

You select the value of the components in the voltage-reduction network (Ry, Rv, and R1) to match the input signal level (which may be as high as ±10V) to the 0 to 2V input level of the flash A/D converter. This component matching is a simple process because the AD9610 is unity-gain stable.

You'll also need to consider some other factors when designing this circuit. For example, you'll need a substantial ground plane under IC2, and you must pay extra attention to the three reference inputs (+VREF, REFMID, and -VREF). The +VREF and -VREF inputs require a low-impedance driving source. You can improve the converter's 1-LSB integral nonlinearity by adjusting the ladder midpoint, REFMID. The reference circuit consists of a low-cost amplifier (IC3), transistor Q1, and a few resistors.

The flash A/D converter (IC2) has a differential encode signal that requires a drive signal for both the Encode and the Encode pins. IC4 is a high-speed ECL comparator with differential inputs and complementary outputs. The Data and Overflow outputs can supply

---

**Compare amplifier configurations**

The primary difference between standard voltage-input amplifiers and transimpedance amplifiers is that voltage-input amplifiers experience voltage feedback and transimpedance amplifiers have current feedback. In voltage-input amplifiers, internal parasitics limit the amplifiers' upper performance level at high frequencies, and you can do little to overcome these effects. The voltage feedback also limits voltage-input amplifiers' bandwidth.

You can see the voltage-input amplifier's bandwidth-limitation problem by looking at a voltage-feedback amplifier configured for noninverting operation (Fig Aa). The circuit's operation is described by an equation that sums the currents at the inverting input and defines the relationship between the input voltages and output voltage:

\[
V_{OUT} = A(V_A - V_B); \quad \frac{V_B}{R_1} + \frac{V_B - V_{OUT}}{R_F} = 0,
\]

where \(V_{IN} = V_A = V_B\). After some rearranging and manipulation, these equations reduce to

\[
\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A \frac{R_1}{R_F + R_1}} = \frac{R_F + R_1}{R_1} \cdot A + 1.
\]

When you remember that \((R_F + R_1)/R_1\) equals the closed-loop gain \((A_{VCL})\), and the open-loop gain,

\[
A(W) = \frac{A_o}{1 + \frac{W}{W_o}}.
\]

is actually the frequency-dependent term, the equation expands to

\[
\frac{V_{OUT}}{V_{IN}} = \frac{A_{VCL}}{A_{VCL} \left(1 + \frac{W}{W_o}\right) + 1}.
\]
output currents ranging to 20 mA. All the output levels are ECL compatible, and you should use proper ECL terminations (100Ω resistors tied to -2V) to avoid ringing and reflection.

This circuit has one other unusual feature—IC2 has two AIN pins. You must drive these two pins symmetrically with connections of equal length. Otherwise, aperture-delay errors may degrade the converter's performance at high frequencies.

Optimize an S/H amplifier for speed

You can use a 2-stage approach (Fig 3) to build an S/H amplifier that has both a fast acquisition time and long-term stability. The first stage accepts the signal quickly and allows the system to move on to the next channel. When you optimize the S/H amplifier for speed, however, you'll degrade voltage-drift performance over time. To keep the circuit from drifting, you can place a second S/H amplifier after the high-speed circuitry. The combined circuit will have both long-term output stability and an extremely short (10-nsec) acquisition time.

The performance of Fig 3's circuit depends on the Schottky-diode ring, which is controlled by the switching network's forward or reverse biases. The circuit provides forward and reverse biasing by using the pulse

If Ao (the dc open-loop gain) is large in comparison with A_VCL (the closed-loop gain), the closed-loop gain dominates the response of the gain stage. As the frequency (ω) approaches the closed-loop gain-break frequency (ω0), the denominator begins to increase, causing a proportional decrease in gain (Fig Ab).

The key point here is that, in Eq 1, the frequency-dependent term is multiplied in the denominator by the closed-loop gain. As the closed-loop gain increases, so does the frequency-dependent error. This gain-bandwidth product implies that for a single-pole roll-off (20 dB/decade), you obtain a constant when you multiply the closed-loop gain by the bandwidth.

In contrast, the output voltage of a transimpedance amplifier (Fig Ba) is a function of the current entering the inverting input—a low-impedance point. The relationships shown in Fig B are summarized by the equation

$$ I + \frac{V_B - V_{OUT}}{R_F} + \frac{V_B - 0}{R_I} = 0; \ V_{OUT} = -AI, $$

where $V_{IN} = V_A = V_B$.

When you assume that the transimpedance open-loop gain is frequency dependent and note that $R_F + R_I/R_I$ is the closed-loop gain, you obtain

$$ \frac{V_{OUT}}{V_{IN}} = \frac{A_{VCL}}{R_F \left(1 + \frac{W}{W_0}\right) + 1}. $$

Although this result closely parallels that obtained with the voltage-input amplifier, the frequency-dependent term has one important difference—you multiply the transimpedance roll-off by the value of the feedback resistor rather than by the closed-loop gain. Therefore, a transimpedance amplifier's bandwidth is constant for a constant feedback resistor—you can vary gain with little or no degradation in bandwidth (Fig Bb). Once you optimize the design for a given feedback resistor, the bandwidth will remain essentially unchanged.
The overall performance of a high-speed conversion circuit depends on how well you match the input signal level to the input range of the A/D converter.

transformer to overcome the static voltage potential of the two voltage sources. When the ring is forward biased, the circuit is in the track mode, and the input signal will charge the hold capacitor. When the ring is reverse biased and the diodes are off, the circuit switches to the hold mode and disconnects the input signals from the capacitor.

Amplifier IC1 provides high-speed buffering to drive

Inside a transimpedance amplifier

The AD9610 is a transimpedance amplifier that has both inverting and noninverting input terminals as well as a low-impedance output stage. The current flowing in or out of the inverting input controls the output voltage. Split power-supply feeds power the input section and the output stage separately. In addition to the usual amplifier connections, the AD9610 package provides two external bias points to accommodate external decoupling needs. Two grounding pins, internally connected via the case, provide some inherent shielding.

The block diagram in Fig A is a conceptual model of the AD9610. Among the amplifier's key features are the buffered, high-impedance, noninverting terminal and the low-impedance (20Ω) inverting input terminal. Any signal current in the inverting terminal leg will flow through the 20Ω impedance. The voltage created across the input impedance drives the ideal-amplifier stage that follows, resulting in a current-to-voltage output conversion.

As is the case with any real amplifier, the AD9610 does not have ideal input characteristics. Its offset-voltage and offset-current specs are ±0.3 mV and 5 µA, respectively, and its noninverting bias-current drift is ±30 µA. The voltage and current sources shown in Fig A account for the offset voltage and current. The offset error is an output error in the noninverting-input-terminal buffer. The current source attached to the inverting terminal models the input bias current (bias currents flow in both input terminals, but the bias current in the inverting input is the most important).

The AD9610 also has an integral 1500Ω feedback resistor. This resistor partly controls the effects of any parasitic-body capacitance and lead inductance associated with discrete feedback components. In contrast, the 1-pF parasitic-body capacitance of an external 1500Ω feedback resistor would limit an amplifier's bandwidth to 100 MHz max.

The AD9610's power-supply feeds are split, so the output transistors have separate connections. This scheme allows you to use external resistors to limit output swing and current (the amplifier has a ±50-mA typ drive capability).

The noninverting input provides a voltage reference for the input stage. Unlike the inverting input, the noninverting terminal is a high-impedance node; therefore, you should drive it from a low-impedance source to minimize any unbalancing effects it might have on the inverting side. (A ground connection is an excellent low-impedance reference point.) Typically, inverting-gain configurations have less overshoot than do noninverting configurations.

Fig A—The buffered, high-impedance, noninverting terminal and the low-impedance, inverting input terminal are key features of this transimpedance amplifier.
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Parasitic capacitances within a voltage-input amplifier limit the performance level at high frequencies no matter what you do.

A traditional S/H amplifier (IC₂). Because it has a low value, the hold capacitor preserves the acquisition speed. However, the hold voltage does drift somewhat because of the effects of leakage current. You can minimize the leakage current by using a FET buffering stage to isolate the hold capacitor from the rest of the circuit. The high bandwidth and input impedance of the circuit make it ideal for ultrahigh-speed sampling applications.

A 2-stage approach can also improve the performance of an A/D converter. By using a high-speed, flash A/D converter and subranging architecture, you can design a 12-bit A/D converter with submicrosecond conversion speeds (Fig 4). The circuit in Fig 4 converts an analog input in two steps. First, a 7-bit flash A/D converter directly converts the input signal. This 7-bit signal is then loaded into a high-speed, 7-bit, 12-bit-accurate D/A converter. Next, a difference amplifier (IC₁) subtracts the D/A converter's output from the analog input. For the second conversion, the resulting error

**Fig 3—Fast acquisition time and low droop are key features of this sample/hold-amplifier circuit. The circuit uses a 2-stage approach, employing a transimpedance amplifier for the input stage.**

**Fig 4—To build a 12-bit A/D converter with submicrosecond conversion speeds, you'll have to use a 2-stage approach that employs a high-speed flash A/D converter and a subranging architecture.**
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<table>
<thead>
<tr>
<th>WATTS</th>
<th>MAIN</th>
<th>CH 2</th>
<th>CH 3</th>
<th>CH 4</th>
<th>MODEL No.</th>
<th>TYPE</th>
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<tr>
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<td>+5V/2.5A</td>
<td>+12V/2.0A</td>
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<td>PCB</td>
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<td>U CHANNEL</td>
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<td>+24V/3.0A</td>
<td>RBO 223</td>
<td></td>
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</tbody>
</table>

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<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Technology</th>
<th>Operating Current at 4MHz</th>
<th>Power-Down Current</th>
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<tbody>
<tr>
<td>TMPZ84C00</td>
<td>4MHz Z80A CPU</td>
<td>CMOS</td>
<td>15mA</td>
<td>&lt;10µA</td>
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<tr>
<td>TMPZ84C30</td>
<td>CTC: Counter/Timer Circuit</td>
<td>CMOS</td>
<td>3mA</td>
<td>&lt;10µA</td>
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<tr>
<td>TMPZ84C20</td>
<td>PIO: Parallel Input/Output</td>
<td>CMOS</td>
<td>2mA</td>
<td>&lt;10µA</td>
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<tr>
<td>TS4807</td>
<td>Clock Generator/Controller</td>
<td>CMOS</td>
<td>2mA</td>
<td>&lt;10µA</td>
</tr>
<tr>
<td>TMPZ84C40</td>
<td>SIO: Serial Input/Output</td>
<td>CMOS</td>
<td>25mA</td>
<td>&lt;10µA</td>
</tr>
<tr>
<td>TPMZ84C10</td>
<td>DMA: Direct Memory Access</td>
<td>CMOS</td>
<td>25mA</td>
<td>&lt;10µA</td>
</tr>
</tbody>
</table>

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Eliminate the guesswork in analog-switch error analysis

As the accuracy and speed of data-acquisition systems increase, analog-switch errors can consume increasing portions of the error budget. However, you can employ several circuit-design techniques to minimize the effects of device limitations.

Stephen Moore, Siliconix Inc

When you employ solid-state analog switches in high-resolution, high-accuracy data-acquisition systems, you'll need to predict the effect of several types of switch imperfections: leakage current, for example, as well as on-resistance variations induced by signal voltage. Moreover, when designing fast systems, you'll have to take into account the throughput limits engendered by the switches' speed, injected charge, and break-before-make time; similarly, you'll need to determine the amount of high-frequency current that will flow through an open switch because of the switch's off-state capacitance.

Fortunately, you can do more than simply determine the detrimental effects of the analog switches. You can follow a few practical guidelines that will help minimize the effects of the switch limitations on system performance.

Regardless of its speed, a data-acquisition system must first meet its specified dc accuracy. Unless you can make the analog switches drive a high-impedance load, like the noninverting input of a follower, achieving the required dc accuracy will require you to account for the voltage drop caused by current flowing through switch on-resistance. Further, you will have to consider the variations in on-resistance caused by changes in input voltage, in power-supply voltage, and in temperature. If a diligent search fails to turn up a switch whose on-resistance is low enough under the worst combination of conditions, you will probably have to limit the analog signal swing.

Keep in mind, though, that you don't want to limit the swing unnecessarily; doing so would require additional gain following the switches. That extra gain could in turn introduce drift, noise, and nonlinearity. Many switch data sheets don't make it easy for you to determine the largest acceptable signal swing. You need to know the maximum and minimum values of on-resistance you will encounter for any range of input voltages you specify, yet the device data sheet may obscure that information or fail to provide it at all. In particular, for switches optimized for speed, and for which the typical on-resistance is low, you are likely to find the variation large compared with the typical value—a fact that may only become apparent if you take the trouble to add up numbers extracted from several curves (Fig 1).
Changes in input voltage, in power supply voltage, and in temperature can cause variations in on-resistance.

Illustrating on-resistance's effects, Fig 2a shows a programmable-gain amplifier (PGA) in which the analog switches are in series with the gain-determining resistors. In this circuit, a front end for a 4½-digit or 15-bit ADC, not only must you trim each gain resistor to compensate for the 0V-input on-resistance of the switches, you also must know the maximum and minimum values of switch resistance to predict gain change with temperature and signal level. (Gain change with signal level is called nonlinearity.)

The switches you select for such applications should have closely controlled on-resistance, as, for example, Siliconix's DGP Series CMOS analog switches do. At 25°C and with a ±15V power supply, DGP devices' total on-resistance variation over the ±5V analog signal range is less than 5% of the maximum 0V-input on-resistance. In the circuit of Fig 2a, if you use gain-determining resistors larger than 200 kΩ, (that is, 20,000 times the DGP201A's 10Ω max on-resistance variation), nonlinearity introduced by the switches will be less than ±1 count out of the ±20,000-count full-scale range of the 4½-digit ADC.

Fig 2b shows another version of the PGA. At the expense of using a larger number of precision resistors — albeit of lower values — than the circuit in Fig 2a, this configuration provides better linearity and gain stability by placing the switches where all that flows through them is the op amp's input bias current and the leakage of the off switches. This total current is so small that the effects of switch on-resistance variation may safely be ignored. The circuit of Fig 2c combines low parts count with insensitivity to switch on-resistance, but the price is steep; adjusting any one of the four programmable gains affects the other three.

Several semiconductor manufacturing processes are used to produce analog switches. Each process yields devices with a different combination of characteristics. Fig 1 compares typical analog-signal-induced on-resistance variation of switches produced by three different process technologies. Table 1 lists performance areas in which devices fabricated by several technologies excel, and it lists the sacrifices in performance that had to be made to optimize specific characteristics.

Unless your system has a large number of channels, at room temperature leakage of off switches is unlikely to affect accuracy very much. But as temperature increases, leakage effects can become significant — especially if you are making high-resolution or high-impedance measurements. Remember that except for surface effects, leakage of silicon doubles for every 10°C temperature rise.
In a conventional multiplexer, like the one shown in Fig 3a, the leakage of all off switches flows through the one on switch and its signal source. At 25°C, even with a 5-kΩ piezoelectric motion transducer connected to the multiplexer's input, the circuit's few nanoamperes of leakage would barely affect the 15-bit-resolution, ±1.6V-full-scale measurement. Raise the temperature by 60°C—not an unreasonable rise in many process-control applications—and it's a different story; leakage may cause an offset of close to 10 counts. You can control this offset if you use a switch whose leakage is specified over the operating temperature range. For the DGP508A, Siliconix guarantees maximum leakage over the -40 to +85°C industrial temperature range; in this example, the device's 20-nA maximum leakage limits offset to less than one count.

When a multiplexer must handle a large number of channels and operate over a wide temperature range, it is sometimes appropriate to submultiplex, as shown in Fig 3b. By breaking up the multiplexer into smaller units whose outputs are themselves multiplexed, submultiplexing reduces the number of off channels that contribute leakage currents to the selected channel. Submultiplexing also breaks up the capacitance on the multiplexer's output bus, which improves settling time.

Whenever you make an analog switch part of a feedback network, you must consider how the switch's on-resistance affects the performance of the closed-loop system. In Fig 2a, a single-ended PGA illustrates the point. Fig 4 pictures a differential-input, single-ended-output audio amplifier with three programmable gains—approximately 0, 10, and 20 dB. The amplifier's input is derived from a 600Ω balanced line on which capacitively coupled line-frequency-related hum appears superimposed on the desired signal. The amplifier's common-mode rejection (CMR) reduces the hum at the output. Because gain accuracy is loosely specified, switch on-resistance itself is not especially important,

---

**TABLE 1—SWITCH-TECHNOLOGY PERFORMANCE TRADEOFFS**

<table>
<thead>
<tr>
<th>TECHNOLOGY</th>
<th>EXAMPLE</th>
<th>PERFORMANCE FEATURE</th>
<th>DYNAMIC- PERFORMANCE TRADEOFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-CHANNEL JFET MULTICHIP</td>
<td>DG181</td>
<td>LOW CROSS-TALK (-70 dB AT 10 MHz)</td>
<td>LIMITED SIGNAL RANGE (-75 TO +15V)</td>
</tr>
<tr>
<td>P-CHANNEL JFET BIFET</td>
<td>SW-01</td>
<td>LOW CROSS-TALK (-50 dB AT 10 MHz)</td>
<td>SLOW SWITCHING (600 nSEC t&lt;sub&gt;flip&lt;/sub&gt;)</td>
</tr>
<tr>
<td>CMOS (44V)</td>
<td>DG201A</td>
<td>LOW CHARGE INJECTION (20 pC)</td>
<td>SLOW SWITCHING (600 nSEC t&lt;sub&gt;flip&lt;/sub&gt;)</td>
</tr>
<tr>
<td>CMOS (SILICON GATE)</td>
<td>DG271</td>
<td>HIGH SWITCHING SPEED (50 nSEC t&lt;sub&gt;on&lt;/sub&gt;)</td>
<td>LIMITED BANDWIDTH</td>
</tr>
<tr>
<td>D/C MOS (MONOLITHIC)</td>
<td>DG536</td>
<td>WIDE BANDWIDTH; LOW CROSS-TALK (-70 dB AT 40 MHz)</td>
<td>LIMITED SIGNAL RANGE (0 to 7.5V)</td>
</tr>
</tbody>
</table>

---

**Fig 2**—One of three programmable-gain-amplifier variations (a) places analog-switch on-resistance in series with gain-determining resistors. A second version (b) has greater parts cost, but linearity is unaffected by switch on-resistance variation. Although seeming to combine the virtues of the first two circuits, a third (c) is not recommended, because adjustment of any of the programmable gains affects all of the others.

---

EDN November 26, 1987
Switches optimized for high speed are likely to exhibit large variations in on-resistance.

but the on-resistance match is critical because it partially determines the CMR.

If the resistors are perfectly matched and the op-amp has infinite CMR, when the gain is set to 10 dB, the DGP201A's 10Ω max mismatch yields a CMR of 48.6 dB. To minimize the signal swing they experience, the switches in the feedback path are connected on the summing-junction side of the feedback resistors, thus minimizing the switches' signal-induced on-resistance variation—and, in turn, the distortion they introduce in the amplifier's output. The alternate location, near the amplifier output, should be used if it is important to limit the audible pop created by the switches' charge injection (that is, coupling of a portion of the switches' gate drive into the signal path via gate-to-channel capacitance) when you change gain. With one side of the switches connected directly to the output, most of the injected charge flows into the amplifier's output stage; very little of it produces an IR drop in a feedback resistor, so the pop is minimized.

Injected charge is just one of the factors you have to evaluate when considering the dynamic performance of data-acquisition systems. Switching time, break-before-make time, settling time, channel-to-channel crosstalk, and off-state isolation are some of the others. None of these is solely a function of switch properties; all are strongly influenced by the surrounding circuits and the layout.

Data-acquisition systems that acquire time-varying analog signals usually contain sample/hold amplifiers. These circuits place many demands on analog switches. Obtaining fast acquisition, low aperture uncertainty, low offset and pedestal errors, and low droop is a challenge to circuit designers. (For a definition of these terms, see box, “Sample/hold terminology needn't cause confusion.”)

Fig 5 shows a sample/hold circuit that uses low-charge-injection switches and charge-injection compensation to minimize pedestal error. The pedestal error, also known as the hold step, is caused by transfer of charge onto the hold capacitor at switch turn-on and
Because \( V = \frac{Q}{C} \), if injected charge is 20 pC and the hold capacitor is 1000 pF, the pedestal is 20 mV.

By using the 50-pF variable capacitor to inject an equal charge, derived from a signal that swings in a sense opposite than that of the analog-switch gate drive, you can achieve a first-order cancellation of the step. However, the switch's gate-to-channel capacitance, through which the charge is transferred, is affected by the analog-signal level, so the cancellation

---

**Sample/hold terminology needn't cause confusion**

Fig A illustrates most of the terms used to describe the performance of sample/hold amplifiers, also referred to as track/hold amplifiers. Although difficult to illustrate, the terms aperture delay and aperture jitter—the two components of aperture time—deserve clarification, because they are widely misunderstood. Aperture delay and jitter are important if the input signal is changing at the instant the amplifier switches from track to hold, a situation common when rapidly varying signals are digitized.

As indicated in Fig A, aperture time begins when the hold command crosses the nominal threshold of the logic element that receives it in the amplifier and ends when the amplifier switches from track to hold. Aperture delay is aperture time averaged over a large number of track/hold cycles during which the input signal repeatedly makes its maximum specified excursion—asynchronously from the track/hold command.

Aperture uncertainty is the peak-to-peak variability in the aperture delay. Because, normally, no direct indication is available, the instant at which the track/hold transition occurs must be calculated from the voltage that appears at the track/hold output just after the hold-mode settling time. Uncertainty can be affected by input-signal characteristics (for example, voltage level and slew rate) and may be specified for signals whose rate of change does not exceed some maximum value. Aperture uncertainty is a key specification of track/hold amplifiers used to capture rapidly changing analog signals. It is the track/hold characteristic most likely to limit the maximum frequency of the signals that can be accurately digitized and reconstructed.

In many sample/hold circuits, aperture uncertainty is related to properties of the analog switch used for sampling. For example, if the circuit topology is such that the voltage on a FET's source terminal—at the instant when the FET effectively ceases to conduct—depends on the analog-input-signal level, then the point on the track/hold control-logic waveform where analog-switch conduction ceases also depends on the input-signal level. Because the slew rate of the sample/hold control signal is finite, the exact point at which the switch ceases to conduct depends on the analog-signal level. Examples of switch properties that can affect aperture uncertainty are capacitance at the control input and the magnitude of the required logic-signal voltage swing.
Several semiconductor manufacturing processes are used to produce analog switches; each process yields a different combination of characteristics.

Fig 5—This high-performance sample/hold circuit uses injected-charge cancelation to minimize pedestal error.

can be perfect only at one value of the signal voltage. The amount of charge a switch injects when you turn it on or off depends on the product of its gate-to-channel capacitance and the voltage swing at its gate. When you apply no more than the specified gate drive, Siliconix's DGP201A holds this product to a maximum of 50 pC.

In Fig 5, the circuit is in sample mode when the logic input is low (when S1 and S3 are on and S2 and S4 are off). An overall feedback loop is closed around the amplifier, so the hold capacitor, C2, charges to the input voltage through S3. When the logic input goes high, the circuit enters hold mode (S1 and S3 open while S2 and S4 close). Although the overall feedback loop is now open, after transients settle, the sample/hold output voltage equals the voltage on the hold capacitor. When S2 conducts, it closes a local feedback loop around the input op amp, keeping its gain at 1. Closing S1 injects a charge onto C2 to null the pedestal. Because you can't control the swing at S1's gate, you adjust C1 to make the compensating charge exactly cancel that injected when S2 opens.

Turn-on and turn-off times of the DGP201A limit the acquisition and aperture times of this circuit and restrict throughput to a maximum of approximately 500k samples/sec. Substituting a faster switch (for instance, the DG271, which has 52 nsec turn-on and turn-off times) makes the circuit capable of 5M-sample/sec performance, but accuracy is reduced because of the faster switch's higher leakage; droop rate on the hold capacitor rises by a factor of four.

If you are acquiring signals whose frequency is greater than approximately 100 kHz, crosstalk can result from interchannel capacitance of multichannel switches and from input-to-output capacitance of switches in the off state. Your first line of defense is to understand which device fabrication technologies minimize this capacitance and select your switches accordingly. (If that approach doesn't yield adequate performance, it's time to investigate different circuit approaches.)

CMOS switches parallel n- and p-channel devices to achieve relatively constant on-resistance over the analog signal range. The capacitance across the parallel switches is higher than the capacitance across a single switch. DMOS (double-diffused MOS) FETs are better

Fig 6—NMOS and DMOS channel lengths differ substantially. In an NMOS device (a), photolithographic definition determines channel length (L). In an n-channel DMOS device, channel length is determined by the depth of subsequent diffusions (b).

Fig 7—The T switch configuration is useful at high frequencies. When series switches S1 and S2 are open, the shunt switch S3 grounds out signals fed through the capacitance of S2.
high-frequency switches, not only because they use a single device, but because their channel length is determined by the difference in the depth of successive diffusions and not by photolithographic definition.

Compared with NMOS or CMOS, DMOS results in a shorter channel with less capacitance for a given on-resistance (Fig 6).

Placing the switches in a T configuration minimizes crosstalk in high-frequency applications. Fig 7 shows three switches connected this way. When the composite T switch is on, the two series switches conduct and the shunt switch is open; when the composite switch is off, the series switches are open and the shunt switch conducts. When the input series switch is open, signals that feed through its off-state capacitance flow to ground through the shunt switch. In this way, the output series switch is called upon to block only a very small feedthrough signal. Careful use of this circuit technique permits design of multiplexers that handle 100-MHz signals.

A new fabrication process, called D/CMOS, allows one chip to combine DMOS analog switches with CMOS control logic. The DG5636 16-channel multiplexer shown in Fig 8a combines 16 DMOS T switches and control logic in a single device. Configuring the switches into two 8-channel banks and submultiplexing their outputs—the technique shown in Fig 3b—halves the output capacitance that any switch must drive. When several multiplexer outputs connect to a common point, the device’s internal output switching even further reduces the capacitive load presented to the T switches. When all channels are off, you can use the switch labeled DIS to discharge the multiplexer’s output bus capacitance, thereby minimizing the effect of the previously selected channel’s voltage on your measurement of the currently selected channel’s voltage. Fig 8b shows the low crosstalk produced by the T switches.

**Author’s biography**

Steve Moore is staff marketing engineer at Siliconix’s IC Div in Santa Clara, CA. He has been at Siliconix for three years; prior to that he worked in both design and marketing at Precision Monolithics. Steve is interested in the performing arts: He is a member of the Society of Motion Picture and Television Engineers, and he composes, performs, and records rock music. His other leisure activities include backpacking and handball.

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You can design a variety of op-amp circuits to condition optical position-sensing signals. Depending upon the special requirements, S/N ratio, input-signal strength, and cost constraints of your application, you can use one or more of the configurations presented here to implement your position-sensing circuitry.

Jerald Graeme, Burr-Brown Corp

Now that low-cost photodiodes and lasers are widely available, the task of designing light-tracking and position-sensing circuits is greatly simplified. You can design a variety of op-amp circuits to condition the output of these light-source/sensor pairs. The circuits' differential capabilities define position in terms of signal differences.

In the simplest case, you can tell the relative distances of two photodiodes from a light source of known intensity by examining the diodes' output-current levels. This distance-measurement facility is often used in aligning machine tools and surveying as well as in other distance-measurement applications. The output signals from these photodetectors are often low-level common-mode signals that you must translate to differential, high-level signals for proper measurement.

Added complications arise for applications in which the signal strength of the light source is unknown: Surveying applications, for example, encounter environments in which the light source is distorted and, consequently, the signal level from the photodetector reflects not only the distance of the detector from the source, but also the disturbances in the intervening medium. To compensate for these variations, you can normalize the difference signals obtained from the photodetectors against the mean of the photodetectors' output signals, you can compress the signals, or you can use a linear array of detectors monitored by a maximum-signal detector. These three basic approaches to photodiode signal conditioning are referred to as differential monitoring, signal compression, and maximum-level detection.

Differential monitoring

An instrumentation-amplifier configuration such as the one shown in Fig 1 effects a common-mode-rejection...
To monitor more than one axis of position displacement, you need two or more photosensors for each axis being monitored.

ratio of greater than 10,000:1—a figure much better than the signal-level error caused by the responsivity mismatches of the photodiodes. This circuit obtains a distance measurement in the form of a voltage output whose value can be expressed as

\[ e_v = (I_{P1} - I_{P2})R_1. \]

The diode currents are first converted to voltages by the current-to-voltage converters constructed with op amps IC\(_1\) and IC\(_2\). The output of the current-to-voltage converters is in common-mode form. All the light impinging upon each of the detectors is converted to a voltage. The difference in distance from the light source to the two detectors is the desired measurement; therefore, the difference in current between the two detectors is the signal of interest. The differential amplifier, IC\(_3\), provides this differential voltage function.

Errors caused by mismatches between the photodiodes will occur in the circuit's common-mode and differential signals. You can remove these error voltages by adding resistance in series with the differential amplifier's inputs. In effect, the added series resistance adjusts the common-mode rejection and relative signal gains in such a way as to counteract the effects of the diode mismatch. In addition, because the circuit has a grounded-cathode configuration, it can use monolithic dual photodiodes, which will, in turn, reduce the initial photodiode mismatch.

In a current-to-voltage converter, the dominant dc error generally results from the flow of the op amp's input bias current through the feedback resistance. You can normally compensate for that error by adding matching resistance in series with the op amp's noninverting input. In Fig 1's circuit, however, you don't need to compensate for the current-to-voltage converters, because the matched dual op amps act as current-to-voltage converters at the input. The dc errors they produce follow the matching of the input bias currents and the high-value resistors.

The resulting equal output offsets from the amplifiers constitute a common-mode signal at the INA105 differential amplifier's input; the differential amplifier, naturally, rejects the signal. Matching accuracy for the components of Fig 1's circuit limits the output offset of the op amps to 100 µV, which is comparable to the input offset errors of the op amps.

A noise assessment of the circuit requires a complex analysis, which has been carried out in detail for current-to-voltage converters (Refs 1 and 2). Increasing the feedback resistance of these converters to the maximum practical level optimizes the S/N ratio, because the signal gain increases along with the resistance while the noise increases only by the square root of the resistance. Note, however, that the large feedback resistances also act in combination with the high photodiode capacitances to produce elevated amplifier-noise gains. An alternative would be to capacitively bypass the large feedback resistors; however, that procedure would place noise optimization in direct conflict with signal bandwidth.

Fig 2 illustrates the interplay of the effects of the variation in feedback resistance upon the various gains: open loop, current-to-voltage, and noise gain. Fig 2a shows a model of a single current-to-voltage converter; it includes the photodiode capacitance (C\(_D\)) and the stray capacitance (C\(_S\)) that shunts the R\(_1\) resistor. The model includes the voltage noise of the op amp; the current noise of this circuit, as of other circuits that use FET op amps, is negligible.

The signal gain is actually transimpedance rather...
than voltage gain; nevertheless, it is shown on the same plot (Fig 2b) so that you can compare the bandwidths. The transimpedance gain falls off at 3.2 kHz for a 0.5-pF stray shunt across a 100-MΩ R₁, which is far short of the op amp’s unity-gain crossover frequency, f_c. To extend the signal bandwidth to f_c in this circuit, you’d need to use a feedback resistor of less than 160 kΩ—a resistor value that would degrade the S/N ratio. Unless the bandwidth is your overriding concern, therefore, you won’t want to use such a low-value resistor.

If you use the high-value resistor, as recommended, to improve the S/N ratio in Fig 2’s circuit, only the op-amp noise enjoys the gain benefit over the entire bandwidth of the op amp. The amplifier noise begins to climb at the break frequency of R₁ and C₁, and climbs to a level defined by the ratio of C₁ to C₂, which is 100 in this case. The logarithmic compression of the graph may hide the extent to which noise dominates this circuit. The fact is, the major part of the amplifier bandwidth is in the upper frequency region, dominated by noise.

The preferred means of counteracting the noise’s gain advantage in this circuit is to use post-filtering. Post-filtering preserves the S/N ratio that you get from the high resistance values, and it limits the bandwidth of the op amp, thereby restricting the noise-gain bandwidth. The bypass capacitor would reduce the signal and noise bandwidths by the same amount. Another way to achieve the desired filtering is to bypass the last two resistors on the right in Fig 1 (to do so, of course, you must build your own difference amplifier). This approach requires you to match the circuit’s net impedances precisely; otherwise, the circuit’s common-mode-rejection ratio will be severely degraded.

**Post-filtering reduces noise**

The total output noise for the components shown in Fig 1 is 209 µV rms: 128 µV from the feedback resistors and 165 µV rms from the op amps. Post-filtering with a single pole at 3.2 kHz reduces the noise to 140 µV rms—nearly that of the resistors alone.

The differential circuit configuration of Fig 1 provides some immunity to such external noise sources as electrostatic discharge, electromagnetic interference, and radio-frequency interference. These noise sources are readily received by the high-impedance inputs of the photodiodes and their associated circuitry. At lower frequencies, the differential arrangement of the circuit rejects the common-mode signals injected by these noise sources.

The differential connection of Fig 1’s circuit lies in the amplifiers, but you can also connect the photodiodes themselves in a differential manner (Fig 3a). This configuration offers much simpler circuitry, but it does cause some performance degradation in comparison with Fig 1’s circuit. When the diodes are connected back to back across the amplifier’s input, they deliver to the amplifier a signal equal to their difference current. Because the diode’s voltage is held to zero by the op amp’s inputs, the photodiodes are simply 2-terminal current sources that are responsive to incident light. Fig 3a’s circuit simplification is useful only in situations in which diode mismatches and rejection of externally induced noise aren’t critical. You can’t use the well-matched monolithic dual photodiodes in this circuit.

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**Fig 3—When you connect two photodiodes back to back, as in a, you obtain a differential input; b’s circuit provides both differential-input and reduced-resistance levels.**
The extension of photosensor circuitry from a 1-dimensional system to a multidimensional system is generally straightforward.

because of their common cathodes. Neither can you compensate for the diodes' responsivity mismatch by adjusting amplifier gains. However, you can provide dc compensation for the error by offsetting the normally grounded end of $R_2$.

By making a minor modification to Fig 3a's circuit, you can obtain differential-amplifier benefits, as long as you're willing to accept a reduced bandwidth. If you place the photodiodes directly across the inputs of the op amp, as in Fig 3b, the diode difference current will flow in $R_2$. Although $R_2$ normally provides only dc error compensation, in this configuration it develops a signal voltage that doubles the circuit gain, allowing you to use half the resistance level that would normally be required to reduce the dc error due to amplifier input currents. This circuit further reduces noise because the voltage on $R_2$ is no longer impressed upon the diodes; the diodes' leakage currents are largely eliminated. The balanced impedances presented to the op amp's inputs lead to the rejection of coupled noise. Because $R_2$ is now a gain element, Fig 3b doesn't require the noise-removing 0.01-$\mu$F bypass capacitor that Fig 3a uses.

A close analysis of Fig 3b, which is modeled in Fig 4a and illustrated in Fig 4b, reveals that the op amp's common-mode input capacitance causes a drop in the circuit's bandwidth. The common-mode input capacitance, $C_{CM}$, shunts $R_2$ and is six times the stray capacitance, $C_s$ (which is the bandwidth limit for Fig 3a's circuit). The lower resistance level of Fig 3b's circuit, however, reduces the effect of the increased capacitance—the net effect is that the bandwidth is reduced by a factor of 3.

The frequency response of Fig 3b's circuit exhibits two plateaus instead of one. As the frequency increases, the gain of the circuit makes a transition from the transimpedance ($R_1+R_2$) to $R_1$ because, with increasing frequency, $C_{CM}$ shunts $R_2$. The next level of response is caused by the shunting action of $C_s$, which shunts $R_1$ for the second roll-off.

Because Fig 3's circuits each contain only one current-to-voltage converter, not two, they exhibit better noise performance than does Fig 1's circuit: In Fig 3's circuits, the noise due to op amps and resistors is reduced by a factor of $\sqrt{2}$. The total resistance used in Fig 3's circuits is reduced to one-half that of Fig 1's, because the individual diode currents are not processed by separate resistors in Fig 3's circuits. Note, however, that in Fig 3's circuits, twice the diode capacitance is presented to the op amp's input, increasing noise gain peaking. The total output noise caused by the circuit is 184 $\mu$V rms. You can reduce this figure to 120 $\mu$V rms by using a single-pole filter set at the signal bandwidth.

A noise analysis of Fig 3b's circuit reveals that it's a good approximation to consider $R_1+R_2$ as shunted by the series combination of $C_{CM}$ and $C_s$. A noise analysis of Fig 3b's circuit reveals that it's a good approximation to consider $R_1+R_2$ as shunted by the series combination of $C_{CM}$ and $C_s$. The noise output of the circuit is 192 $\mu$V rms, which you can reduce to 125 $\mu$V by using a single-pole, 3.2-kHz filter.

Two-axis monitoring

To monitor more than one axis of position displacement, you need two or more photosensors for each axis being monitored. As you can see from the circuit shown in Fig 5, the extension of photosensor circuitry from a 1-dimensional system to a multidimensional system is generally straightforward. However, you need to be aware of a few special considerations. Not only must the diodes within each diode pair be well matched, but the pairs must also be well matched, because the ratio of x and y signals yields the direction angle in a system that
uses polar representation of position. This angle information is of predominant importance in tracking applications. Although signal magnitudes depend on the highly variable diode responsivity, interpair matching compensates for the ratio (of the two axes' signals) or angle information. The best way to achieve this interpair matching is to use monolithic photodiode arrays.

The placement of the diodes injects a further requirement: The diodes must be thermally and spatially matched. Wider spacing of the diodes expands the diodes' detectable range, but also increases the probability of thermal mismatches among the diodes. Photodiodes typically have a response temperature coefficient of 1000 ppm/°C. You can use a thermally conductive mounting to provide an isothermal base for the diodes, but a better alternative would be to use a monolithic array of diodes built on a common substrate and housed in a common package. Such arrays are ideal for laser-positioning applications, because the required spatial detection range is compatible with monolithic construction spacings.

**Normalized outputs**

In all the preceding circuits, the generated signals indicate only the relative position of the light source with respect to the sensors. Absolute-displacement measurements require a light source of calibrated intensity. Errors in the calibration of the light source can be partially removed by tracking adjustments, but these errors provide the ultimate limit to distance-measurement resolution.

To compensate for variations in intensity in both position-sensing and optical-tracking applications, you can normalize the difference signal you receive from the diode circuit. The simplest and most accurate approach to normalization is to use an analog divider, as Fig 6a illustrates. The divider, which is adapted for the monitor circuit in Fig 1, receives the difference signal directly from the normal monitor output. To derive the
Absolute-displacement measurements require a light source of calibrated intensity.

Summation signal, you add a voltage divider between the outputs of the current-to-voltage converters of IC₁ and IC₂. This signal sum drives the denominator input of the divider, providing the desired normalization. The output signal is proportional to the difference signal divided by the sum of the diode currents.

This circuit's dominant noise source is output noise introduced by the divider. Divider noise is a function of the magnitude of the divider's denominator signal. The noise is worst for this circuit at low signal levels; it reaches a maximum of 1 mV rms at the divider's minimum denominator level. The total output noise is 1.02 mV rms. You can reduce the noise figure to 580 µV rms by using a filter with a cutoff frequency greater than 3.2 kHz.

The dynamic range of the detector circuit is limited by a combination of noise and the minimum input requirement of the divider. The minimum input signal required by the DIV100 divider shown in Fig 6a is 250 mV. The maximum input level that the divider can accept is 10V, yielding a 40:1 dynamic range for the denominator signal. Above 10V, the divider output saturates; below 250 mV, divider errors dominate. These restrictions apply directly to the sum of the two photodiode currents; therefore, the maximum detectable variation in light intensity is also 40:1. The circuit has an overall gain of 4, the analog divider has a gain factor of 10, the voltage divider has a gain of ½, and the DIV100's input resistance loads the voltage divider by a factor of 0.8, yielding an overall gain of 4.

**Use analog multiplier instead of divider**

Another way to effect normalization of the circuit is to insert an analog multiplier in the feedback loop, as shown in Fig 6b. Multipliers are more readily available and cost less than dividers. Because the multiplier in Fig 6b is located in the feedback loop, its function is inverted: It acts as a divider (Ref 3). The divider's numerator produces a current in R₁ that can't be accepted by the op amp's input. As a result, the amplifier drives the multiplier's Y input, forcing the multiplier to supply the current through R₂ and thereby creating a voltage, at the multiplier's output, that's equal to R₂/R₁ times the original input signal. The multiplier feeds back signal D(e⁻/10) to R₂; this expression demonstrates the control that the denominator, or D signal, exerts over the circuit's transfer function.

When you use this multiplier-feedback method to obtain the division function, the bandwidth of the op amp and that of the multiplier will interact. The combination of the op-amp and multiplier roll-offs can contribute enough feedback phase shift to the circuit to make it oscillate. To avoid oscillation, make sure that one of the devices, either the op amp or the multiplier, has a much higher bandwidth than the other. Fig 6b uses a MPY634 multiplier, whose 6-MHz bandwidth is well beyond that of the OPA111 op amp. The op amp creates a dominant feedback pole for all the levels of feedback gain provided by the multiplier. In the worst-case condition, when the signal at the multiplier's X input is at its 10V full-scale level, the net phase shift through the feedback loop is merely the sum of phase shifts for the op amp and the multiplier; before the loop unity-gain crossover frequency, it's not enough to cause oscillation.

You can reduce the complexity of the normalization circuit from the 5-device circuit of Fig 6 to the 3-device circuit shown in Fig 7. This configuration doesn't allow you to use common-cathode photodiodes, however, so you can't use well-matched, monolithic dual photodiodes.

An additional drawback to this configuration is that it
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The simplest and most accurate approach to normalization is to use an analog divider; a less-expensive method is to use an analog multiplier instead.

allows for the possibility of a latch condition. If, in a power-up sequence, for instance, the voltage presented to the amplifier's -X input is positive, the polarity of IC2's feedback will be reversed. This change in polarity creates a positive-feedback situation, which allows the circuit to latch. To avert this latch condition, you should capacitively couple the negative supply to the -X input.

The circuits discussed thus far derive differential, relative input signals from an optical signal source and provide normalization for those signals. The normalization offers a direct correction for variations in light intensity. However, you can also use two other signal-conditioning techniques—signal compression and maximum-level detection—to adjust to the variation in light intensity.

**Signal-compression techniques**

You can use the voltage-mode output of the photodiodes (Fig 8) to achieve inherent signal compression. The voltage-mode output is characterized by a logarithmic response to light input. This response extends the dynamic range of the circuitry without requiring normalization techniques. The high resistance of the photodiodes limits the bandwidth of the circuit, because the signal swings must be impressed upon the large diode capacitance through the diode resistance. For the circuit shown, the diode capacitance is 50 pF and the resistance is 100 MΩ, yielding a 32-Hz bandwidth for the circuit.

Besides its limited bandwidth, another limitation of this circuit is that its offset error can amount to many millivolts at the op amp's input. These offset voltages dominate the dc error performance of the circuit. You can compensate for the offset errors by offsetting D2 with the potentiometer and voltage divider shown in the circuit. The differential operation of the circuit eliminates most coupled noise.

Another method of adjusting to the wide dynamic range of optical signals is to use linear arrays to select the maximum signal level from among the receiving photodiodes (Fig 9). From this information, you can obtain the position of the signal source relative to the array.

In Fig 9's circuit, each amplifier is connected to a photodiode segment, and each of their inverting inputs

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*Fig 8—To provide an output that adjusts to a wide range of input signal levels, this circuit takes advantage of the inherent signal compression afforded by the voltage-output mode of the photodiodes.*

*Fig 9—A linear array of photodiodes configured as in this illustration gives a TTL-high-level output signal for the photodiode with the highest incident light intensity.*
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is connected to the same feedback/sensing point. Each amplifier attempts to control the voltage at this common point; however, only one amplifier is able to do so, because of the blocking action of the signal diodes that are in series with the amplifier outputs. The amplifier with the highest input voltage (the greatest input signal from the light source) drives the sense point to a level above the level needed to maintain a satisfactory feedback condition for the other, lower-output-level amplifiers.

Because the feedback is no longer satisfactory for these amplifiers, their outputs are driven even lower, and the voltage divider converts all the outputs to TTL levels. The amplifier with the highest input level has a high TTL level, and all others present a TTL-low state.

References

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Jerald G Graeme is manager of instrumentation-components design at Burr-Brown Corp (Tucson, AZ); he directs a linear-IC development group. He holds a BSEE from the University of Arizona and an MSEE from Stanford University. Jerry has eight patents to his credit, and he has authored many articles and books on op amps. His leisure pursuits include photography, woodworking, and scuba diving.
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New Developments in RS232 Interfaces

Robert Dobkin

New RS232 interface chips have been developed that offer significant advantages over older devices such as the 1488 and 1489. The new RS232 interface ICs improve speed, power, voltage supply requirements, and protection over older devices. Further, the new chips are easier to use, requiring fewer external components and may be turned off to a "zero" power supply current condition for use in battery powered systems.

The new RS232 drivers are implemented in a monolithic bipolar technology. A unique output stage was designed that provides large output swings, minimizing power supply voltage requirements, while retaining outstanding overload protection features. The outputs can be driven beyond the power supply voltage without drawing excessive current or forcing current back into the power supplies. Of course, current limiting is included to protect against short circuit conditions.

Initial consideration of technologies for implementing RS232 interfacing might include CMOS as a possible technology for this type of application. Power supply requirements are low, output voltage swing is high, and higher voltage CMOS technologies are available to allow operation up to ±15V. Consideration of some of the problems associated with CMOS decreases its attractiveness for RS232 drivers.

Inherent in the CMOS structure, are diodes between the drain and source of the CMOS devices and the power supplies as is shown in Figure 1. A requirement of RS232 interfaces is the ability to withstand voltage applied to the output pins. With a CMOS output stage this is achieved with the inclusion of a 3000 resistor in series with the output. (The resistor is similar to the resistors included in older drivers.) It protects the interface chip, but still allows damage to other devices powered by the same supply.

A problem occurs when the output of a driver which is powered from the 5V logic supply is connected to an external 12V or 15V source as is allowed by the RS232 specification. External current flows through the 3000 limiting resistor, through the diodes, which are a part of the CMOS structure, and into the power supply. This forces the power supply to 12V or 15V damaging the 5V logic that is connected to the supplies. This problem can even cause latchup if the logic supply is off when external RS232 signals feed voltage into the supply. This problem did not usually exist in the past, because the RS232 interfaces were powered by separate ±12V supplies.

ESD damage is probably the most frequent cause of failure of interface chips. Bipolar devices are relatively rugged but still can be damaged by ESD. System requirements for ESD may be as high as 20kV. No IC can withstand that much voltage without external protection.

A requirement of the RS232 specification is the ability to withstand ±25V input signals. The CMOS LTC1045 which is used as an RS232 receiver has been designed to operate with external resistors in series with the input. These resistors allow very large voltage swings at the input pins and provide ESD protection to the IC. Using on-chip resistors precludes the use of the optimum ESD protection structures, so CMOS devices may be more sensitive to ESD destruction at their inputs.

Figure 1. CMOS Line Driver Showing Parasitic Diodes to the Power Supplies
The output stage of the bipolar drivers is shown in Figure 2. Opposed collector NPN and PNP transistors give the widest possible output swings. The PNP transistor will swing to within 200mV of the positive supply while the NPN transistor with its associated Schottky diode will swing within about 900mV of the negative supply. If the output voltage is forced above the positive supply the emitter base junction of the PNP transistor reverse biases, and no current flows into the supply. The device is unaffected by external voltage up to the breakdown voltage of the transistor. If the output is forced below the negative supply, the Schottky diode reverse biases and prevents external current flow into the chip. Capacitor C1 is used to control the output slew rate so that no frequency compensation components are required to meet the RS232 specification of 4V/µs to 30V/µs.

![Figure 2. New Bipolar Driver Output Stage](image)

A recent advance in the drivers and receivers is on-chip power supply generation. Devices like the LT1080 and LT1081 include an oscillator, capacitive voltage doubler, and capacitive inverter to generate ±9V from the 5V power supply. The charge-pump power supply generator requires only four 1µF capacitors to generate RS232 communication levels from a 5V logic supply. Figure 3 shows a typical hook-up for the LT1080. The on-chip power supply generators generate excess power over the LT1080 requirements, so another RS232 communication device such as the LT1039 can be powered from the same power supply generator. Table 1 gives typical performance of all Linear Technology driver/receiver devices for RS232 communication.

![Figure 3. 5V Powered RS232 Driver/Receiver](image)

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>DRIVERS</th>
<th>RECEIVERS</th>
<th>SHUTDOWN</th>
<th>SUPPLY GENERATOR</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1030</td>
<td>4</td>
<td></td>
<td>X</td>
<td></td>
<td>Low Cost</td>
</tr>
<tr>
<td>LT1032</td>
<td>4</td>
<td></td>
<td>X</td>
<td></td>
<td>RS423 Compatible</td>
</tr>
<tr>
<td>LT1039</td>
<td>3</td>
<td>3</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LT1039N16</td>
<td>3</td>
<td>3</td>
<td>X</td>
<td></td>
<td>MC145406 Compatible</td>
</tr>
<tr>
<td>LTC1045</td>
<td>6</td>
<td></td>
<td>X</td>
<td></td>
<td>Micropower</td>
</tr>
<tr>
<td>LT1080</td>
<td>2</td>
<td>2</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>LT1081</td>
<td>2</td>
<td>2</td>
<td>X</td>
<td></td>
<td>MAX232 Compatible</td>
</tr>
</tbody>
</table>

Linear Technology Corporation
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FAX: (408) 434-0507 • TELEX: 499-3977
Open-loop servo adjusts shaft position

James C Smith
NASA, Greenbelt, MD

By using digital techniques to control a stepper motor, Fig 1a's circuit lets you manually adjust the position of a remote shaft. (Fig 1b shows one possible application for the system. Others include the remote positioning of flow valves and leveling devices.)

The ICs and the stepper motor require a 12V supply, which also drives a regulator chip (IC2) that supplies 5V to a digital potentiometer (not shown). This potentiometer generates 256 pulses for each revolution of its adjustment knob, producing the channel A and B quadrature square waves. These two signals enable flip-flop IC3 to decode the potentiometer’s direction of rotation.

IC4 generates control signals for the stepper motor, and transistors Q1-Q4 supply the necessary drive current to the motor's windings. (IC4 alone can supply 350 mA/phase to the motor. If your motor requires more current, use the IC’s data sheet to select an R3 value that provides base drive appropriate to the external transistors you’re using.)

Components R1 and C1 filter the supply voltage, Rs limits the motor current, and the 5V zener diodes (D1-D4) reduce voltage transients by providing a flyback path for motor current when a transistor turns off. Because the motor steps at the pulse rate of channel B, the motor rotation is proportional to the rotation of the potentiometer knob—for knob rotation below about 1 rev/sec.

Unlike analog servo circuits, this system’s positioning capability isn’t affected by temperature or long-term component drift. Precision and resolution are limited primarily by the mechanical linkage between the motor and its load.

To Vote For This Design, Circle No 748

Fig 1—This shaft positioner converts the output of a digital potentiometer to signals suitable for driving a stepper motor.
Simultaneous-addition algorithm saves time

S Murugesan
ISRO Satellite Centre, Bangalore, India

An algorithm that performs computations in parallel is faster than one that uses a conventional counting method. For example, if you want to count the number of 16 single-bit inputs that are high (logic ones), you first compose a 16-bit word in which each bit position corresponds to an input. In the conventional counting method, you then set a register to zero and left-shift the 16-bit word 16 times, incrementing the register each time an overflow occurs. Although simple, this sequential process requires the µP to execute many time-consuming instructions.

The algorithm of Listing 1 computes in parallel. The trick is to arrange the data bits in segments so you can apply the 16-bit add instruction without generating an overflow (carry bit). Sixteen-bit data, for instance, requires four steps.

Step 1 pairs off the data bits \(a_0\) to \(a_{15}\) with zeros so you can perform eight sums simultaneously. These are \(a_0 + a_1, a_2 + a_3 \ldots a_{14} + a_{15}\), which yields the eight 2-bit results \(S_1, R_1, S_2, R_2 \ldots S_8, R_8\).

Step 2 performs the four additions \(S_1, R_1 + S_2, R_2 \ldots S_8, R_8\) yielding the four 3-bit sums \(V_1, U_1, T_1 \ldots V_4, U_4, T_4\). Finally, steps 3 and 4 execute sums that combine these 3-bit numbers into the final 5-bit number \(E\), whose value is the number of inputs \((a_i)\) that are high.

To Vote For This Design, Circle No 749

---

**LISTING 1—SIMULTANEOUS-ADDITION ALGORITHM**

<table>
<thead>
<tr>
<th>READ INPUT (A=a_{15}a_{14}\ldots a_1a_0)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>STEP 1</strong></td>
</tr>
<tr>
<td>(A_1=\text{AND } A, 5555H)</td>
</tr>
<tr>
<td>(A_2=\text{SHR } A)</td>
</tr>
<tr>
<td>(A_3=\text{AND } A_2, 5555H)</td>
</tr>
<tr>
<td>(B=\text{ADD } A_3, A_1)</td>
</tr>
<tr>
<td><strong>RESULT</strong></td>
</tr>
</tbody>
</table>
| \(\begin{array}{c}
    0 \ a_{14} \\
    0 \ a_{15} \\
    S_8 \ R_8 \\
\end{array}\) |
| \(\begin{array}{c}
    0 \ a_{12} \\
    0 \ a_{13} \\
    S_7 \ R_7 \\
\end{array}\) |
| \(\begin{array}{c}
    0 \ a_0 \\
    0 \ a_1 \\
    S_1 \ R_1 \\
\end{array}\) |

| **STEP 2**                                  |
| \(B_1=\text{AND } B, 3333H\)               |
| \(B_2=\text{SHR } B, 2 \text{ BITS}\)      |
| \(B_3=\text{AND } B_2, 3333H\)            |
| \(C=\text{ADD } B_3, B_1\)                |
| **RESULT**                                  |
| \(\begin{array}{c}
    0 \ 0 \ S_7 \\
    0 \ 0 \ S_8 \\
    0 \ 0 \ S_1 \\
\end{array}\) |
| \(\begin{array}{c}
    R_7 \\
    R_8 \\
    R_1 \\
\end{array}\) |
| \(\begin{array}{c}
    0 \ 0 \ 0 \\
    0 \ 0 \ 0 \\
    0 \ 0 \ 0 \\
\end{array}\) |
| \(\begin{array}{c}
    V_4 \ U_4 \ T_4 \\
    V_4 \ U_4 \ T_4 \\
    V_4 \ U_4 \ T_4 \\
\end{array}\) |
| \(\begin{array}{c}
    0 \ 0 \ 0 \\
    0 \ 0 \ 0 \\
    0 \ 0 \ 0 \\
\end{array}\) |
| \(\begin{array}{c}
    Z_2 \ Y_2 \ W_2 \\
    Z_1 \ Y_1 \ X_1 \ W_1 \\
\end{array}\) |

| **STEP 3**                                  |
| \(C_1=\text{C}_{L} \) (LOWER BYTE OF C)    |
| \(C_2=\text{C}_{H} \) (HIGHER BYTE OF C)    |
| \(D=\text{ADD } C_2, C_1\)                |
| **RESULT**                                  |
| \(\begin{array}{c}
    0 \ V_2 \ U_2 \ T_2 \\
    0 \ V_4 \ U_4 \ T_4 \\
    Z_2 \ Y_2 \ X_2 \ W_2 \\
\end{array}\) |
| \(\begin{array}{c}
    0 \ V_1 \ U_1 \ T_1 \\
    0 \ V_3 \ U_3 \ T_3 \\
    Z_1 \ Y_1 \ X_1 \ W_1 \\
\end{array}\) |

| **STEP 4**                                  |
| \(D_1=\text{AND } D, 0\text{F}_H\)        |
| \(D_2=\text{SHR } D, 4 \text{ BITS}\)      |
| \(E=\text{ADD } D_2, D_1\)                |
| **RESULT**                                  |
| \(\begin{array}{c}
    0 \ 0 \ 0 \ 0 \\
    0 \ 0 \ 0 \ 0 \\
    0 \ 0 \ 0 \ 0 \\
\end{array}\) |
| \(\begin{array}{c}
    Z_1 \ Y_1 \ X_1 \ W_1 \\
    Z_2 \ Y_2 \ X_2 \ W_2 \\
    e_4 \ e_3 \ e_2 \ e_1 \ e_0 \\
\end{array}\) |
PLD functions involve enabling outputs

Michael Robinson
KLA Instruments Corp, San Jose, CA

Programmable-logic devices (PLDs) are useful for implementing complex logic functions, but their sum-of-products form limits the number of OR terms available. The popular 16L8, for instance, provides only seven. You can implement a more complex function, (one containing eight or more OR terms), if the PLD has unused output pins.

One way is to break the function into two levels and feedback the first level's output as an input to the second level. Consider the "checkerboard function" of four variables (Fig 1) and its associated Karnaugh map, for example. You can split this function in two (Fig 2a). Because neither part contains more than seven OR terms, you can now implement the function in a 16L8 as long as it has an unused output pin.

This approach restricts your output-pin assignments, though, because not all of the 16L8's output pins feed back to the input array. What's more, the two logic levels double the propagation delay. You can avoid both disadvantages by using the 3-state output-enable inputs to implement a function in parallel, on a single level.

Partitioning the function as shown in Fig 2b yields two sections with only four OR terms each. You externally connect the two outputs together; the variable A selects the appropriate output and disables the other (contention will not occur because the output-enable controls are complementary). This technique doesn't carry any delay penalty because the time it takes for a 16L8 (and similar PLDs) to enable or disable an output is the same as the propagation delay through the device. Your choice of output pins isn't restricted because there isn't any feedback involved.

You can generalize this technique by realizing that each variable in the output-enable equations corresponds to a binary partitioning of the Karnaugh map. Variable A divides the Karnaugh map for Fig 2b's logic equations into two halves, for example, and you therefore connect two outputs together.

For more complex functions, you can use two variables to divide the Karnaugh map into quarters, therefore tying together four of the outputs. The most complex function you can implement with a 16L8 requires the tying together of all eight outputs. Such a function can contain as many as 56 OR terms.

Fig 2—You can implement the Fig 1 function (a) on a 16L8 PLD by partitioning the function differently (b) and using the output-enable controls.

To Vote For This Design, Circle No 750
Fast algorithm computes square root

Bruce Komusin
Fortune Systems International, Monte Carlo, Monaco

Listing 1 computes the “floor” of the square root of an unsigned 32-bit number—that is, the largest integer whose square is equal to or smaller than the given number. Floating-point coprocessors can perform this operation, but 32-bit processors may require too much time or memory space for the range of numbers in your application. The algorithm in Listing 1 makes this computation faster than other methods for the 68000 µP.

(Jim Cathey compared test results in *Dr Dobb’s Journal*, #118, August 1986. His test loop, executed on an Atari 520ST computer, calls the subroutine under test and then provides a sequence of values for computation. Each of his tests starts with N=0 and then increments by ((N/2^16)+1) until N exceeds its 32-bit range. The comparative results are as follows: Cathey’s Newton subroutine, 439 sec; Cathey’s bit-shift subroutine, 417 sec; Listing 1, 228 sec.)

---

LISTING 1—SQUARE-ROOT ALGORITHM

*************************************************************************
* Motorola 68000 -- Unsigned 32-bit Integer Square Root routine.
* *
* Enter: d0 = N = unsigned 32-bit number
* Exit: d0 = 32-bit square root of N. The high word is always 0000. 
* d0 is the floor of the root; i.e. d0 squared is never > N.
* No registers are affected except d0.
*************************************************************************

SQRT:

move.l dl,-(a7) save dl
move.l d2,-(a7) save d2

*****
* Compute the "first guess". Strategy:
*
* 1. Find the most significant non-zero bit pair in N.
* (A bit pair is bits \( b, b-1 \) with \( b \) even.)
* 2. Define \( i = b/2 \).
* 3. Create two numbers:
* \( N \) divided by \( 2^i \) (\( N \) shifted right \( i \) times), and
* \( 1 \) multiplied by \( 2^i \) (1 shifted left \( i \) times).
* 4. Average them to get guess1, the first guess.

move.l d0,d1 d1 = N from now on
bmi.b Nbit32b31 bit pair "32",31 is non-zero
beq.b return if N = 0, root is 0 too
add.l d0,d0 move bit b-1 to bit b
or.l d1,d0 "non-zero-ness" of pair b,b-1 now in b only
moveq #15,d2 d2lo = b/2 = i for b=30 d2hi = 0
guess:

lsr.l #2,d0 test next bit pair \( b, b-1 \) (b=30..0, even)
dbs d2,guess until a non-zero pair is found

move.l d1,d0 d0 = N again
lsr.l d2,d0 d0 = N/2^i
add.w #16,d2 d2lo = i+16 d2hi = 0
LISTING 1—SQUARE-ROOT ALGORITHM (Continued)

bset.l d2,d2
d2hi = 2^i

swap d2
d2lo = 2^i

add.w d2,d0
extend,d0lo = N/2^i + 2^i (17 bits)

roxr.w #1,d0
d0 = 1/2 [ N/2^i + 2^i ] = guess1

*****
* Apply Newton’s Method. Strategy:
*
* 1. Given guess1, apply twice the Newton iteration formula:
*    guess(K+1) = 1/2 [ N/guess(K) + guess(K) ]
*    generating in turn guess2 and guess3.
*    Guess3 will then be either the correct root, or one higher.
* 2. Square guess3.
* 3. Compare this with N. If higher, the root is (guess3)-1.
*    Otherwise the root is guess3.

newton:
move.l d1,d2
d2 = N
d2lo = N/guess1 d2hi = junk

divu d0,d2
d2lo = N/guess2 d2hi = junk

add.w d2,d0
extend,d0lo = N/guess1 + guess1 (17 bits)

roxr.w #1,d0
d0 = 1/2 [N/guess1 + guess1] = guess2

move.l d1,d2
d2 = N
d2lo = N/guess2 d2hi = junk

cmp.w d0,d2
is N/guess2 < guess2? (i.e. guess3<guess2)

bhs.b return
no, so guess2 is the root

add.w d2,d0
extend,d0lo = N/guess2 + guess2 (17 bits)

roxr.w #1,d0
d0 = 1/2 [N/guess2 + guess2] = guess3

move.w d0,d2
d2lo = possible root

mulu d2,d2
d2 = square of the possible root

cmp.l d1,d2
is this > N?

bls.b return
no, so guess3 is the root

dec_it:
subq.w #1,d0
yes, so (guess3)-1 is the root

return:
move.l (a7)+,d2
restore d2

move.l (a7)+,d1
restore d1

rts

*****
* For the case N > or = $80000000, compute guess1 specially & faster.

Nbit3231:
clr.w d0
d0 = N/2^16 (d0=$8000..FFFF)

* See if N is FFFEO001 or greater; if so, return FFFF.
* (We know that FFFF squared is FFFEO001.)
* This prevents overflow that would occur in the divide.

move.w d0,d2
d2lo = N/2^16

neg.w d2
if N < FFFEO000 then d2lo > or = 3

* Note: Also, extend flag is set since d2lo is not 0.

roxr.w #1,d0
d0 = 1/2 (N/2^16 + 2^16) = guess1

subq.w #2,d2
is N < FFFEO000? (d2lo > 2?)
The subroutine is based on a variation of the well-known Newton method, in which you feed a first estimate \((K=1)\) to the Newton equation

\[
GUESS(K+1)=\frac{1}{2}\left[\frac{GUESS(K)}{N} + GUESS(K)\right].
\]

\(N\) is the given 32-bit number. \(GUESS1\) generates a better guess \((GUESS2)\), with which you generate a better guess, and so on. This procedure converges on the exact root when you use pencil and paper or floating-point arithmetic.

For integer-only arithmetic, however, the procedure produces guesses that eventually bounce between two integers on either side of the desired root, unless \(N\) is a perfect square. Older algorithms use this behavior as an exit condition from the iteration loop: Deliberately choosing the first guess too large causes the subsequent guesses to be smaller, and the first guess in the sequence equal to or larger than the one before stops the iteration. You then throw away the last guess; the previous one is the desired floor root. Newton’s method requires one to four iterations to obtain the correct floor root for 32-bit numbers.

**Listing 1**, though, recognizes that \(GUESS3\) is either always correct or is one integer greater than the correct root. No conditional loops are necessary; the routine simply applies the Newton equation twice. To determine if \(GUESS3\) is correct, the routine squares it—a faster operation than the Newton iteration—and checks whether the result is greater than \(N\). If it isn’t, \(GUESS3\) is the answer; if it is, the answer is one integer less than \(GUESS3\).

**Listing 1** also includes a first-guess loop that saves time by performing special handling of numbers with values of \(80000000H\) or larger (numbers for which the most significant bit is set). The routine computes \(GUESS1\) faster as a result and is also able to detect values of \(FFFFFF00H\) or greater (numbers that cause divide overflow if handled normally). For these large values, the routine then returns the root immediately without having to use Newton’s equation.

---

**Circuit measures op-amp settling time**

James Butler and Peter S Henry
*Precision Monolithics Inc, Santa Clara, CA*

The Fig 1 test circuit is suitable for measuring the settling time of op amps and is simpler than other methods currently in use (Refs 1, 2, and 3). *(Ed Note: The authors developed the idea of using batteries as a floating supply for the device under test (DUT) on their own, but Bob Pease and Ed Maddox also presented the idea in a 1971 article, in Teledyne-Philbrick’s New Lightning Empiricist.)*

The DUT is connected in a unity-gain configuration. Nine-volt batteries supply \(\pm 18V\) power to the DUT, and a pulse generator drives the virtual (false) ground formed by the junction of these supply voltages. You should connect decoupling capacitors \((C_1\text{ and }C_2)\) across the DUT and the supplies as in normal practice. (Fast-settling DUTs may require capacitor values larger than those shown.)

Schottky diodes \(D_1\) and \(D_2\) clamp the DUT’s output within 300 mV of ground, and the JFET buffer transistor \((Q_1)\) minimizes capacitive loading. \(IC_1\), a fast hybrid
improve circuit performance...$12.95 (6-49 qty)

Now available for the first time...IF bandpass filters that maintain constant 50-ohm impedance over their passband and stopband. What are the significant advantages over conventional bandpass filters whose impedance and VSWR change drastically outside the bandpass region? For receivers, improved intermod performance. For wideband amplifiers, greater stability. For mixers, less spurious reflections and improved flatness of response. For oscillators, considerably better noise characteristics.

Housed in a hermetically-sealed package, only 0.4 by 0.8 by 0.4 in., the PIF-series IF bandpass filters meet MIL-STD-202 requirements, have a VSWR of 1.3 (typ), and are offered at IF center frequencies shown in the chart. For your design convenience, performance specs are provided at 20dB, 10dB, 1dB rejection points within and outside the bandpass region.

Available for immediate delivery, the constant-impedance IF bandpass filters are priced at only $12.95 (6-49 qty) and carry Mini-Circuits’ one-year guarantee.

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<tr>
<td>Center Frequency (MHz)</td>
<td>30</td>
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<td>Bandpass (MHz) 1dB max.</td>
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<td>35-49</td>
<td>41-58</td>
<td>50-70</td>
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<td>Stopband (MHz) 10dB min.</td>
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<td>12-200</td>
<td>14-240</td>
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<tr>
<td>Stopband (MHz) 20dB min.</td>
<td>2-210</td>
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<td>3-350</td>
<td>4-400</td>
<td>5-490</td>
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setting higher standards
op amp, amplifies the buffer's output with a gain of \((1+R_F/R_e)\). Two more Schottky diodes, \(D_3\) and \(D_4\), clamp the circuit's output voltage to minimize the effect of saturation in the scope's input amplifier.

The resistor values shown produce an output that is 10x that of the DUT. This gain allows measurement of 1-mV error signals (0.01% of a 10V step), which in turn lets you use a digitizing oscilloscope—the HP54100A, for example, which has a maximum resolution of 10 mV/div.

The remaining components form an autozero circuit that reduces the relatively large \(V_{os}\) of IC1. By offsetting the bias voltage for \(Q_1\), the components force the average output offset to less than 500 \(\mu\)V (the input offset voltage of IC2).

During testing, the DUT's output produces a 10V step in response to each 10V transition of the pulse-generator signal and immediately slews back and settles at about the 0V level (Fig 2). The DUT output supplies load current through \(R_L\) (via the pulse generator) as the waveform begins slewing. The load current then drops nearly to zero as the DUT's output voltage enters the ±300-mV clamp band set by \(D_1\) and \(D_2\). By observing this voltage on an oscilloscope, you can measure op-amp settling times of less than 400 nsec, to within ±0.01%.

Note that \(R_L\) doesn't load the DUT during its settling phase. To simulate a load in a real application, you may want to connect a resistor or RC network between the DUT's output and its virtual ground (connected to the noninverting input). Note also that ringing and long-

---

**Fig 1**—By driving the op amp's supply voltages with a pulse generator, this circuit refers the op-amp output's settling waveform to ground for 10V as well as -10V output steps.

**Fig 2**—In this scope photo, the upper waveform is the pulse-generator signal from Fig 1, and the lower waveform is the resulting output response of an OP-42 op amp.
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CMOS GATE ARRAYS

- 1.3-µm, double-level-metal CMOS technology
- Toggle rates to 175 MHz

The M6002X and M6003X Series 1.3-µm CMOS gate arrays offer D-flip-flop toggle rates to 175 MHz. Their patented gate-isolation structure achieves a 47,000-gate density on a die area that is 15 to 25% smaller than designs using oxide isolation. The gate-array family includes both conventional channel and variable-track master-slice architectures. The company’s gate-array CAD system allows for on-chip configurable RAM and ROM. The typical access time for the memory cells is 15 to 25 nsec. Your design-interface options include Mentor Graphics, Daisy, Valid Logic, and FutureNet development systems; you use the company’s cell library. The library offers more than 80 TTL-equivalent macro functions, and more than 180 macro cells, such as gates, flip-flops, and buffers. The arrays are available in small-outline and plastic flat packages; in plastic leaded chip carriers for surface-mount applications; and in plastic DIPs, plastic shrink DIPs, and ceramic pin-grid arrays. They cost from $0.003 to $0.01 per gate, depending on production quantities, density and package.

Mitsubishi Electronics America Inc, Semiconductor Div, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 351

A/D CONVERTERS

- Provide 8- or 10-bit, 15-µsec A/D conversion
- Include an 8-channel analog input multiplexer

The 8-bit SDA0808 and the 10-bit SDA0810 are CMOS monolithic A/D converters that incorporate an 8-channel analog input multiplexer. Pin compatible with ADC-0808/0809 A/D converters, each converter operates from one 5V supply and has an 8-bit, TTL-compatible, latched 3-state output port. The SDA0810 provides its 10-bit output in two sequential output bytes. The channel-address inputs for the multiplexer are also latched. Operating on the successive-approximation principle, the converters have a 15-µsec conversion period and feature a temperature-stabilized differential comparator and sample/hold circuitry. They require an external 5V reference voltage. The analog inputs accept signals in the 0 to 5V range, and the total conversion error is ±0.5 LSB, without any offset or gain adjustment required. Both devices are housed in 28-pin DIPs and are available in versions that operate over either -40 to +85°C or -40 to +125°C. They dissipate a maximum of 15 mW. The SDA0808, $3; the SDA0810, $5 (1000).

Siemens AG, Zentralstelle fur Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 352

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500.

Circle No 379

NETWORK CIRCUITS

- Octal line driver features 3-state output
- Octal line receiver is TTL/MOS compatible

The UC5170 octal-line-driver and UC5180 receiver ICs are designed for LAN applications where you need maximum densities and high levels of integration. The UC5170 features 3-state outputs, low power consumption, and TTL/MOS-compatible inputs. Its slew rate is programmable. The UC5180 can with-
INTEGRATED CIRCUITS

stand differential inputs of ±25V. It’s TTL/MOS compatible, and it features a reduced supply current of 25 mA. Both devices are available in either a 28-pin DIP or a 28-pin plastic leadless chip carrier. UC5170, $3.05; UC5180, $3.12 (OEM qty). Delivery, stock to eight weeks.

Unitrode Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

Circle No 353

DC/DC CONVERTER

- Operates directly from rectified 115/230V ac lines
- Provides 15V, 500-mA dc output

The IR2100 dc/dc converter needs only three external components to form a complete 15V dc, 500-mA dc/dc converter power supply that works directly from 115/230V ac lines. The device is especially suited for bias-supply applications in switch-mode power supplies where only unregulated dc power is available—an application that formerly required a bulky 60-Hz transformer. Its other applications include instrumentation, motor control, office machines, and battery chargers for portable tools. The converter’s internal frequency is set at 150 kHz in order to reduce the size of the magnet. The recommended external components comprise a 4.7-mH inductor, a 1-µF capacitor, and a fast-recovery flyback diode. The IR2100A in a 5-pin T0-220 package, $9 (1000). Production quantities are scheduled for the first quarter of 1988.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (800) 223-7018; in CA, (213) 607-8969.

Circle No 355

SIGNAL TRANSMITTER

- Drives a 4- to 20-mA, 2-wire current loop
- Measures signals from RTDs and strain gauges

The AD693 provides a low-cost method of taking remote sensor-based measurements. It provides excitation for and measures signals from sensors such as RTDs (resistance temperature detectors) and strain gauges. You can power the device from the loop current or from a local supply whose output is set for a 4- to 20-mA, 0- to 20-mA, or 12±8-mA signal transmission. The device includes an instrumentation amplifier, a voltage-to-current converter, a voltage reference, an auxiliary amplifier, and application resistors. The stable 6.2V voltage reference can supply 3.5 mA for sensor excitation, and the application resistors simplify sensor hook-up by providing six pin-strappable ranges for 100Ω RTDs. The IC also provides pin-programmable, current-span, and zero adjustments. In a 20-pin ceramic DIP, $9.00 (100). Delivery, 26 weeks ARO.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577. TLX 174059.

Circle No 354

NPC

(Division of Seiko Watch Group)

NPC is the technical pioneer and leader of IC manufacture of digital filters for CD players.

DIGITAL SIGNAL PROCESSING

- SM5831F
  - Digital Video Filter
  - 4 to 8 tap variable FIR
  - f clk = 15 MHz
  - Package: 64PIN FPP

- SM5828
  - Video Shift Register
  - 8 bit word, 1 to 128 variable step
  - f clk = 20 MHz
  - Package: 24PIN DIP

- SM5805
  - PCM Audio Digital Filter
  - 12th order filter x 2 ch.
  - Package: 28PIN DIP

- SM5808
  - 8 x 8 bit Multiplier
  - f mac = 45 ns
  - Package: 48PIN DIP

- SM5810
  - 16 x 16 bit Multiplier
  - f mac = 65 ns
  - Package: 64PIN DIP/68PIN PGA

SPECIAL FUNCTION

- SM6100
  - 8 Bit A/D Converter
  - Conversion time 2.1 µs
  - No S/H required
  - µP-bus compatible
  - Package: 20PIN DIP

- PLL2001
  - PLL Frequency Synthesizer
  - f In = up to 200 MHz
  - Package: 16PIN DIP

- SC6433
  - B/W TV Camera Sync. Generator
  - NTSC or CCIR
  - Package: 22PIN DIP

- SM8530B
  - IEBC Bus Interface Controller
  - Meets IEEE-488 (GP-IB)
  - Package: 40PIN DIP

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2151 O'Toole Ave, Suite L
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TEL: (408) 922-0133
TOLL FREE: 1-800-237-4590
FAX: (408) 922-0137
TLX: 9102405802/SEPONIX USA

EDN November 26, 1987

CIRCLE NO 17
**ANALOG SWITCHES**

- **Low on-resistance**
- **Fast switching**

The DG400 Series analog switches are built with the company's high-voltage silicon-gate CMOS process. The DG411 contains four independently operated, normally closed (logical zero is on) switches and is pin compatible with the DG211. The DG412 has four normally open switches; the DG413 contains two switches in each logic configuration. The series is designed for use in precision S/H circuits. Each of the quad spst analog switches features 35Ω of on-resistance, a 250-pA leakage current, and a 175-nsec switching speed. The switches are suitable for application in disk drives, industrial controls, instrumentation, and automatic test equipment. They cost $3.15 in plastic DIPs, $3.85 in small-outline packages, and $7.25 in ceramic DIPs; MIL-STD-883 versions are $8.98 (100). Delivery, four to eight weeks ARO.

**Motor-Control IC**

- For universal ac motors
- Uses a minimum of external components

The ZN410 motor controller performs all the functions necessary to control the speed of universal ac motors. The IC needs only six resistors, eight capacitors, and one diode as external components. It controls speed by comparing a potentiometer voltage with a voltage derived from an F/V converter that's proportional to the actual motor speed. It then amplifies the difference, or error voltage, and uses it to define the conduction angle of a triac, which is connected in series with the motor's supply voltage. The device is powered from the ac line through a limiting resistor or from a dc source. The ZN410 operates over 0 to 70 °C. It's available in a 16-pin plastic DIP or a 16-pin small-outline, surface-mount package. $1.32 (1000). Delivery, stock to six weeks.

**GaAs Static RAM**

- Achieves cycle times of 2.5 and 3.5 nsec
- Includes registers and a write-pulse generator

The 12G014 256×4-bit static RAM has reduced its 3.0- and 5.0-nsec cycle times to 2.5 and 3.5 nsec, respectively, resulting in a 400-MHz cycle rate. Because of the chip's architecture, which includes on-chip registers and a write-pulse generator, the device is suitable for applications that store and process information in real time. The two versions are available in either leadless or leaded chip-carrier packages. 2.5-nsec 12G014-25, $124.70; 3.5-nsec 12G014-35, $99.50 (500).

**Pressure Sensors Provide Amplified Output**

140PC pressure sensors are individually calibrated and temperature compensated, then amplified so they can directly interface to control circuitry or A/D converters. They're ready to use, off-the-shelf.

These sensors provide a higher degree of accuracy than low level output products, and are interchangeable. PCB terminals exit on the opposite side of the ports. Optional 12-inch, 24 guage colored leadwires are also available.

For more information or a FREE catalog covering our full line of pressure sensors, write MICRO SWITCH, The Sensor Consultants, Freeport, IL 61032. Or call 815-235-6600.

**Up to 500 psi Pressure Sensor**

The 240PC Series offers pressure sensing options ranging from -15 to 500 psi. A rugged aluminum housing makes these sensors suitable for applications where durable packaging is required. Several types of internal O-ring seals are available for wide media compatibility with non-caustic fluids.

Accuracy comes from temperature compensating circuitry, computer-consistent calibration of null and full scale output, plus excellent repeatability. These sensors are amplified and fully signal conditioned.

For more information or a FREE catalog covering our full line of pressure sensors, write MICRO SWITCH, The Sensor Consultants, Freeport, IL 61032. Or call 815-235-6600.

**Advertisement**

EDN November 26, 1987
At about $15 a sensor, the 16PC is the lowest cost method of sensing the differential pressure of liquids and high-humidity gases.

And while our new miniature sensor is economical, it's also very reliable. Thanks to the unique new chip mounting technique we use. It seals the sensing element so that moist media can be applied to both sides of the sensor chip.

Temperature compensation and on-chip laser trimming add to reliability as well, ensuring high stability over 0-5, 0-15 and 0-30 pressure sensing ranges.

The 16PC Series is compatible with high volume circuit board assembly processes and is available in differential, gage and modular versions.

Applying technology innovatively is just one of the ways we can help you save money. To find out more, call us at 815-235-6600. Or write MICRO SWITCH, Freeport, IL 61032.

Together, we can find the answers.

MICRO SWITCH
a Honeywell Division
**INTEGRATED CIRCUITS**

**VOICEBAND INVERTER**
- Operates in the 300- to 3000-Hz voiceband range
- Fixed-frequency inversion

The MX004 is a half-duplex, audio-filter array and frequency-inversion scrambler IC for mobile radio applications. It exchanges high and low frequencies in the 300- to 3000-Hz voiceband and renders transmitted messages unintelligible to listeners using other systems. You can switch the single voiceband channel to either transmit or receive. Its high-order filtering permits the IC to operate with a continuous-tone controlled-squelch-system scheme and other subaudio-signaling schemes, and provides high-quality recovered audio. An on-chip clock generator controls the carrier and filter cutoff frequencies. For ease of interface with a µP, you can address the logic inputs either serially or in parallel.

In a plastic DIP, $10.46 (1000).

MX-COM Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (800) 638-5577; in NC, (919) 744-5050.

Circle No 359

**MULTIPLYING DAC**
- ±0.5-LSB max differential nonlinearity
- 125-nsec settling time

The VC512 12-bit multiplying DAC maintains a settling time of 125 nsec while providing what is essentially 13-bit accuracy with its ±0.5-LSB max differential nonlinearity. The settling-time specification includes the propagation delay through the device. The multiplying feature, combined with D/A-conversion capabilities, allows you to use fewer components in such complex data-acquisition and display applications as graphics displays and other high-speed A/D data-conversion tasks. The device delivers an 8-mA output, and you can modulate the multiplying reference current at 8 mA/µsec. From $38.70 for plastic leaded chip carriers to $125 for surface-mount military packages (100).

VTI Inc, 2401 E 86th St, Bloomington, MN 55420. Phone (612) 851-5200.

Circle No 361
NEW PRODUCTS

COMPUTERS & PERIPHERALS

TIME SOURCE

• Synchronizes the calendar clocks of networked VAX computers
• Generates signal from Coordinated Universal Time

The VAX Time Source synchronizes the calendar clocks of networked VAX computers. The timing device is synchronized to the world time standard, Coordinated Universal Time (UTC), as transmitted by the National Bureau of Standards (NBS). It generates a signal within 10 msec of the UTC standard, and will run on any VAX computer using DEC's VMS operating system. Its hardware consists of an analog AM receiver and a µP-based signal-processing section. It has a crystal-controlled dual-conversion receiver, which monitors the five NBS frequencies. The device interfaces with the computer through an RS-232C port and a TTL-level output. It includes turnkey VMS software that sets the system calendar clock at power-up, accounting for the time zone and the computer's location. If the computer clock drifts, the software maintains a log of the variance between the source and the VAX system clock; the software triggers an alert for the system manager upon achieving a selectable limit. The device makes adjustments for daylight-saving time and automatically resets itself after a power outage. The unit runs from 115V ac at 10W and weighs 3½ lbs. $1495.

Precision Standard Time Inc, 105 Fourier Ave, Fremont, CA 94539. Phone (415) 656-4447.

Circle No 362

GRAPHICS BOARD

• Provides VME Bus systems with 1280×1024-pixel color displays
• Displays as many as 256 colors from a palette of 16.8 million

Featuring two AMD QPDM quad pixel data-flow manager ICs and a frame buffer with 2M bytes of dual-ported video RAM, the double-Eurocard OPAC graphics board provides you with a high-resolution graphics subsystem for VME Bus systems. The board allows you to simultaneously display as many as 256 colors from a palette of 16.8 million on a 1280×1024-pixel resolution display with a refresh rate of 60 Hz. By cascading three OPAC boards together, you can operate with 24 bits/pixel, theoretically allowing you to simultaneously display all 16.8 million colors. By using VME Bus broadcast data transfers, you can program all the QPDMs in parallel; therefore, increasing the color resolution does not slow down the board's graphics operations. Graphics commands to the board are queued in a 1k-byte onboard FIFO buffer, relieving the host processor of waiting while the board becomes available for the next graphics command. Software support for the

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The 197 Microvolt DMM detects the small change—one part in 220,000—for small change: 5620. And you can automate with its IEEE-488 option. Find out how to get a big change in your measurement capabilities. Call the Keithley Product Information Center: (216) 248-0400.

The Model 197 Microvolt DMM

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Circle No 21
board includes the company's QPAC software development tools, and high-level graphics packages (for example, GKS). Less than DM 6000 for a version with one QPDM and 1M-byte of RAM; less than DM 10,000 for a version with two QPDMs and 2M bytes of RAM.

Eltec Elektronik GmbH, Galileo-Galilei-Strasse 11, 6500 Mainz 42, West Germany. Phone (06131) 50630. TLX 04187273.

Circle No 363

VOICE MODULE
- Produces voice-quality communications at 9600 bps
- PC board contains µ-law codec

The low-bit-rate voice digitizer LBRV Codec Module produces voice-quality communications. The PC board contains a µ-law codec that digitizes an analog voice input. A compression algorithm, based on a combination of TDHS (time domain harmonic scaling) and APC-DBA (adaptive predictive coding/dynamic bit allocation), achieves a selectable 9600- or 12,000-bps bit rate. It allows you to send 12 real-time voice channels or a mix of voice and asynchronous or synchronous data over a 56k-bps DDS (digital data service) circuit or over a DS-0 channel in a T1 circuit. The unit contains a signal processor, pre-emphasis and de-emphasis filters, and a dual-port USART. A 4-wire voice I/O interface with 150-msec 1-way throughput delay provides full-duplex operation. Other features include remote command diagnostics and SDLC bit-oriented protocol compatibility with frame error detection. The device enables a 1200-bps asynchronous data channel and two real-time voice channels to transmit signals over one 19,200-bps modem. $400 (1000).

Advanced Compression Technology, 31368 Via Colinas, Suite 104, Westlake Village, CA 91362. Phone (818) 889-3618.

Circle No 364

PRINTERS
- 9-pin dot-matrix printer has 180-cps draft mode
- Handles 1-step loading of single sheets

The 182 Plus 9-pin dot-matrix printer offers bidirectional print speeds of 180 cps in high-speed draft mode, 120 cps in utility mode, and 30 cps in near-letter-quality mode. Front-panel buttons select print mode as well as 10, 12, or 17 characters/in. A paper-handling feature allows 1-step loading of single sheets of paper. You can pin feed labels and continuous forms from the rear or bottom of the printer, and an optional tractor handles forms with as many as four parts. Print-style options include enhanced, superscript, subscript, and double-width characters, as well as underlining. The 9.9-lb printer can produce bit-image graphics and charts having resolutions as high as 288×72 dpi. It is available with a parallel or serial interface with IBM or Microline emulation. $319.

OkiData, 532 Fellowship Rd, Mount Laurel, NJ 08054. Phone (609) 235-2600. TWX 710-897-0792.

Circle No 366

OPTICAL DATA ENTRY
- Data-entry system recognizes variable typestyles
- Consists of a handheld scanner and an expansion board

The TransImage 1000 optical data-entry system for the IBM PC/XT, PC/AT, or 100%-compatible computers can recognize typeset and text. The system reads characters from fixed-pitch, proportionally spaced, typeset, typewritten, near-letter-quality, and laser-generated documents. It can recognize variable character sizes and typestyles. It consists of a handheld scanner with user-definable function buttons and a single-slot PC expansion board with menu-driven software. A recognition engine in the expansion board has a 10-MHz 68000 µP and custom gate-array chips to achieve a 40-cps recognition rate. $2595.

TransImage Corp, 910 Benicia Ave, Sunnyvale, CA 94086. Phone (800) 227-1817; in CA, (408) 733-4111.

Circle No 365

PEN PLOTTERS
- Feature axial pen speeds to 32 ips on 16 sizes of media
- Have 0.0005-in. mechanical resolution

Designed for the PC-based CAD market, DMP-60 Series pen plotters draw on paper, vellum, and polyester film using fiber-tip pens, dispos-
COMPUTERS & PERIPHERALS

able technical pens, refillable liquid-ink pens, and roller-ball pens. The DMP-61 produces drawings on 16 sizes of media, from 8½ × 11 in. to 24 × 36 in.; it has 32-ips max axial pen speed and 4g max axial acceleration. The DMP-62 accommodates 23 sizes of media, from 8½ × 11 in. to 36 × 48 in.; it features 24-ips max axial pen speed and 2g max axial acceleration. Both models have 0.0005-in. mechanical resolution and ±0.002-in. same-pen repeatability. They each have a 68000 µP, which allows them to do closed-figure-area fills and arc-based fonts with fills. Both plotters feature RS-232C interfaces and ten character sets; a Kanji character set is optional. The single-pen plotters also have a 6-pen changer option. DMP-61, $4695; DMP-62, $6495.

Houston Instrument, 8500 Cameron Rd, Austin, TX 78753. Phone (512) 835-0900.

Circle No 367

TRANSPUTER CARD

- Provides a T414 or T800 Transputer in VME Bus systems
- Uses as CPU or gateway to multiple Transputer systems

The BBK-V2 double-Eurocard CPU board for VME Bus systems is based on a 20-MHz T414 or T800 Transputer. The board has 2M bytes of RAM, which is dual ported to both the Transputer and the VME Bus. The Transputer also has direct access to the VME Bus for 8-, 16-, or 32-bit VME Bus data transfers using 24- or 32-bit addressing. You can program the board’s address modifier decoding via software. You can also install as much as 1M byte of onboard EPROM-resident firmware. Four serial Transputer links, operating via RS-422 drivers at a data rate of 20M bps, allow you to link the BBK-V2’s Transputer to other Transputer systems or subsystems via as much as 10m of cabling. To transmit over longer Transputer links, you can jumper-select the links to operate at 10M or 5M bps. The VME Bus interface has a VME Bus interrupt handler and interrupt generator, and includes support for DMA operations and multiprocessor VME Bus environments. Software development for the board is supported by the Occam parallel programming language and by C, Pascal, and Fortran-77 compilers. DM 8900.

Parsytec GmbH, Juelficher Strasse 338, 5100 Aachen, West Germany. Phone (0241) 1822275. TLX 8329659.

Circle No 368

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| 18.347 | 16.154 | 1.5737 | 18.745 | 195.86 |
| 17.961 | 1.8497 | 15.876 | 191.60 | 17.949 |
| 16.975 | 186.67 | 179.87 | 15.134 | 145.87 |
| 15.783 | 1.1654 | 136.56 | 11.387 | 1.6781 |
| 15.786 | 118.75 | 158.70 | 114.36 | 17.169 |
| 11.080 | 1.1342 | 178.67 | 10.287 | 1.6085 |
| 1.2136 | 1.8514 | 10.562 | 1.2905 | 191.70 |

The 175 Autoranging DMM can—up to a hundred readings, and it determines minimum and maximum values. Five functions and a lot more—for 449. IEEE-488 and battery options, too.

QUICK—Call the Keithley Product Information Center: (216) 248-0400.

The Model 175 Autoranging DMM

CIRCLE NO 22

EDN November 26, 1987
COMPUTERS & PERIPHERALS

endar clock. The external interfaces include two RS-232C ports, a keypad port, a display port, and an expansion port. A resident ROM contains 20k bytes of a multitasking Basic language called CAMBasic. Using a 5V power supply and a CRT terminal, or an IBM PC/XT or PC/AT with the vendor's SmartLink, you can develop, debug, and store programs on the board. The CAMBasic command set contains multitasking and interrupt-handling features for real-time environments such as the AutoLog command, which can acquire and store 5000 analog samples/sec. 28k-byte version, $396 (100).

Octagon Systems Corp, 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 426-8540. TLX 4931919. Circle No 369

PROJECT SYSTEM

- Locks onto horizontal scan rates of 15 to 50 kHz
- 650-lm peak light output for large screens

The ECP 3000 3-lens video projection system is suitable for video and low-end CAD environments. It provides a high brightness level (650-lm peak light output) for large screens (from 5 to 25 ft). It has circuitry that automatically locks onto horizontal scan rates of 15 to 50 kHz. A linear nondifferential video amplifier accommodates digital clock rates of 130 MHz and has a 3-dB bandwidth of 60 MHz. The horizontal retrace time is 4 µsec, and vertical retrace time is 300 µsec. Hybrid optics provide an optical resolution of 1200 pixels. F1.0 hybrid lenses are color-corrected and have a separate adjustment for corner focusing of either flat or curved screens. The system has a battery-backed µP and memory to store setups for 28 input sources. An IR remote-control system handles full-zone digital convergence and on-screen display. The system comes with one RGB input module and operates with data or graphics terminals. $14,995. Delivery, 60 days ARO.

Electrohome Lim, 809 Wellington St N, Kitchener, Ontario, Canada N2G 4J6. Phone (617) 894-3100. Circle No 370

19-IN. MONITOR

- 1280x960-pixel resolution for the Macintosh SE
- Seven times larger than the standard Macintosh screen

The Viking 1 large-screen monochrome monitor is suitable for desktop publishing on the Macintosh SE computer. The 19-in. monitor features 1280x960-pixel resolution with a noninterlaced 66-Hz refresh rate. Images are seven times larger than those on the standard Macintosh screen and display one full page or two facing pages. Three desktop-publishing modes include an Extend mode, which extends the image to the Macintosh SE, allowing a larger image to be displayed and to be vertically scrolled; a Magnify mode, which magnifies whatever the cursor is pointing to on the large screen; and a WYSIWYG (what-you-see-is-what-you-get) mode, which lets the Macintosh SE display the document at exact print size. A hardware screen saver turns off the screen after a selected interval. Monitor with a plug-in controller card, software, a manual, and a 6-ft cable, $1995.

Monitorm Corp, 5740 Green Circle Dr, Minnetonka, MN 55343. Phone (612) 935-4151. TLX 753626. Circle No 371

DIGITIZERS

- Available with 0.005- or 0.010-in. positional accuracy
- Allow you to connect a menu tablet and terminal

The HR46T-Worktop digitizing panels are suitable for incorporation into CAD workstations or existing desktop systems. They come in two versions with positional accuracies of 0.005 and 0.010 in. (0.127 and 0.25 mm). You can have the color and surface texture matched to your individual requirements. The digitizers have an active digitizing area of 46x26 in., which is suitable for continuous digitizing of A1 or larger documents. The units connect to a host via an RS-232C, IEEE-488, or parallel interface, and they are compatible with most CAD software packages. The devices are supplied with a control unit that allows you to connect a dedicated menu tablet and a video display unit or PC to the digitizer, while still using only one host computer port. £4800 for the 0.005-in.-accuracy version; £3600 for the 0.010-in.-accuracy version.

Terminal Display Systems Ltd, Lower Philips Rd, Whitebirck Industrial Estate, Blackburn, Lancashire BB1 5TH, UK. Phone (0254) 676921. TLX 635693. Circle No 372
I/O CARD

- Provides analog and digital I/O for the Apple II, II+, and Il e
- Features 2.5-µsec A/D-conversion time for 8-bit resolution

The Data I/O 8 analog and digital interface card for the Apple II, II+, and Il e computers has eight analog input channels with frequency bandwidths from dc to 10 kHz. Its ADC facilitates digital conversion of analog voltages from 0 to 5.10V into 8-bit data in 2.5 µsec, whereas its 8-bit DAC converter drives eight analog output channels in the range of 0 to 5.10V. Three 8-bit digital input ports comprise the 24 TTL digital inputs. Similarly, three 8-bit output data latches comprise the 24 TTL digital outputs. The digital outputs can drive 10 LSTTL loads. You can use Basic commands to read from or write to the card. Its analog inputs are dc protected to ±30V and are protected against transients to ±150V. The card comes with four cables and a 40-pg manual. $295.

Naylor Industries, Box 33187, Indianapolis, IN 46203. Phone (317) 783-6049.

Circle No 373

COMMUNICATIONS CARD

- Provides VME Bus systems with a variety of protocol emulations
- Has driver and spool software available for Unix System V

The SICC-BSC double-Eurocard communications card for VME Bus systems handles a variety of bisynchronous communications protocols. The board allows you to access vari-

ous emulations including IBM-2780, -3780 and -3270, and Siemens-8315/8418 and 8160/9750. The board handles, as much as possible, all the communications protocol requirements, including data-link control, insertion and deletion of control characters, assembly and disassembly of data blocks, data-block transmission and reception, and error handling. High-level commands, issued from a VME Bus host CPU, allow you to control the data-link and transfer-data function, as well as perform initialization, diagnostic, and statistical-evaluation functions. The board supports serial communications at data rates as high as 19,200 bps via an X.21 interface that is routed through its P2 connector. All the necessary control firmware is ROM resident on the board. A software driver and an RJE (remote-job-entry) spool administration software package are available for the board in a Unix System V operating-system environment. The company will undertake integration into other operating systems. The SICC-BSC board costs approximately DM 6800; the RJE spool system with 3780 emulation costs approximately DM 9600.

Stollmann GmbH, Max-Brauer-Allee 81, 2000 Hamburg 50, West Germany. Phone (040) 3890030. Teletex (17) 403226.

Circle No 374

SCSI ADAPTER

- Contains a message-passing co-processor
- Provides asynchronous SCSI transfer rates to 1.5M bytes/sec

The Rimfire 2500 Multibus II SCSI host-bus adapter board occupies one slot and conforms to the double-height Eurocard form factor. It can support as many as seven SCSI devices compatible with the ANSI...
X3.131-1986 specification. Its Western Digital WD33C92 SCSI controller chip provides asynchronous and synchronous transfer rates of 1.5M and 4M bytes/sec, respectively. The device’s floppy-disk-drive interface supports four single- or double-sided, single-, dual-, or quad-density disk drives. A message-passing coprocessor facilitates unsolicited and solicited message passing over the system bus. Solicited data transfer across the Multibus II bus can be burst at 32M bytes/sec. A 256k-byte buffer decouples the SCSI and message-passing activity. The board also supports the Multibus II Built-In-Self-Test (BIST). You can order drivers for iRMX 286 and the Unix System V operating system. $2495.

Ciprico Inc, 2955 Xenium Lane, Plymouth, MN 55441. Phone (612) 559-2034.

Circle No 375

LASER PRINTER

- 12 pages/minute with 300×300-dot/in. resolution
- Printer life is 600,000 pages, extendable to 1.2 million

The PageLaser12 laser printer has a print speed of 12 pages/minute. Long-lasting consumables such as toner, developer, and drum contribute to a product life of 600,000 pages; an optional service kit can extend the product life to 1.2 million pages. The company manufactures all accessories; these include as many as three trays for paper, a standard 250-sheet bin, an optional 500-sheet bin, and an optional envelope feeder. Other accessories include an output collator for sorting and universal trays that are adjustable for statement-, letter-, or legal-sized sheets. The standard onboard memory is 512k bytes; 1.5M bytes of memory is optional. The printer produces text and graphics with 300×300-dot/in. resolution. Prestige Elite, Courier 10, and Line Printer fonts are resident; HP LaserJet-compatible fonts can be downloaded from disk. $3699.

Toshiba America Inc, Information Systems Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (800) 457-7777; in CA, (714) 380-3000.

Circle No 376

COMPUTER

- Runs 32-bit Unix System V release 3.1
- Based on 80386 µP chip

The 6386 WGS 32-bit personal computer is based on the Intel 80386 µP chip and runs 32-bit Unix System V release 3.1 applications concurrently with MS-DOS applications. A feature called DOS Supervisor runs as many as eight MS-DOS applications simultaneously. It will also run OS/2 applications when they become available. A 16-MHz desktop model accommodates as many as 20 simultaneous users, and a 20-MHz floor-standing model, called the 6386E (Extended) WGS, serves a network of as many as 32 users. The desktop model is available in four configurations: a single floppy-disk-drive unit and units with hard disks of 40M, 68M, and 135M bytes, respectively. Each desktop unit has 1M byte of RAM, expandable to 48M bytes. The floor model features a 135M-byte hard disk and 2M bytes of RAM, expandable to 64M bytes. The computer supports CGA (color graphics adapter), EGA (enhanced graphics adapter), VGA (video graphics adapter), and AT&T graphics and has a 101-key PC/AT-compatible keyboard. An RS-232C serial port and a Centronics compatible parallel port are standard. From $4899 to $10,395.

AT&T, 1 Speedwell Ave, Morris-town, NJ 07960. Phone (800) 247-1212.

Circle No 377

GRAPHICS CARDS

- Allow PCs to drive 800×560-pixel display monitors
- Are compatible with EGA and CGA monitors

The TT786-B5 and TT786-B20 are graphics cards for IBM PC, PC/XT, PC/AT, and compatible computers that support the 800×560-pixel display resolution of NEC MultiSynch and similar monitors. Both boards are fully compatible with CGA monitors, and, with the capability to display 16 colors from a palette of 64 colors, are also compatible with EGA monitors. The boards are based on the Intel 82786 graphics processor, which provides hardware windows, and a high-level graphics instruction set that includes BitBlt and CharacterBlt commands. The TT786-B5 has a 512k-byte display memory; the TT786-B20 has a 2M-byte display memory. Software support for the boards includes drivers for AutoCAD, Microsoft Windows, and Digital Research’s GEM, and a port of Turbo Pascal Graphix. TT786-B5, £450; TT786-B20, £750.

Tektrite Ltd, 9 Coolhurst Rd, London N8 8EP, UK. Phone 01-341 2468. TLX 269441.

Circle No 378
NEW PRODUCTS
COMPONENTS & POWER SUPPLIES

SEALED SWITCHES

- Handle loads ranging to 10A
- Offer -25-mΩ max contact resistance

P3 Series rectangular-shaped push-button switches are completely sealed at both the front and back of the panel. The devices handle loads ranging from computer level to 10A. Contact resistance is <25 mΩ. The switches feature a contact-wipe design that helps break contact welds and maintain low contact resistance. They have a 0.25-in. front-panel projection and a 1.125-in. rear-panel projection, including the 0.25-in. quick-connect terminals. These snap-in mounted switches are available in NO, NC, and dpdt configurations. $4.59 (100). Delivery, four to six weeks ARO.

Otto Controls, 2 E Main St, Carpentersville, IL 60110. Phone (312) 428-7171. TLX 722426.
Circle No 381

DISPLAY

- Includes drive electronics and controller
- Character generator can store two 128-character sets

The APD-256M026-1 is a 256-character dot-matrix plasma display that comes with drive electronics and a controller. The unit operates in a serial or parallel mode and provides eight lines of 32 characters each. Each 0.26-in., 5×7 dot-matrix character has a 5-dot underbar that you can use as a visible cursor or lower-case descender. The display features a 100-fl brightness level and a 150° viewing angle. The integral 4k×8-bit EPROM character generator can store two 128-character sets including 128 ASCII characters and an alternate set of 128 programmable characters. The display is also available in a version that interfaces with CRT controllers. $730 (100).

Dale Electronics Inc, 2064 12th Ave, Columbus, NE 68601. Phone (402) 564-3131.
Circle No 382

SOLID-STATE RELAY

- Rated for 0.5A at 600V
- Requires only 5-mA control current

The Power Mini Series relay is rated for 0.5A at 600V. The device can handle 12A surge currents and features a back-to-back SCR design that meets NEMA ICS 2-230 noise-immunity specifications. Precision zero-cross switching provides gains in EMI and RFI elimination while controlling loads over the frequency range of 20 to 500 Hz. The input control levels are TTL and CMOS compatible. The GaAlAs IR LED input circuitry requires only 5 mA of drive current. Optical isolation ranges from 2500 to 3750V rms. In a 6-pin DIP, $3 (1000).

Theta-J Corp, 107 Audubon Rd, Wakefield, MA 01880. Phone (617) 246-4000.
Circle No 383

OPTICAL SWITCHES

- Available with transistor or Darlington-type outputs
- Come in a variety of package styles

Slotted optical switches are available with transistor (Series MOC70) and Darlington-type (Series MOC71) outputs. The MOC70 units come in six different packages; the MOC71 units are available in five package versions. Three current
transfer ratio (CTR) ratings are available for each series: The MOC70 Series has CTRs ranging from 0.15 to 0.6 mA, and the MOC71 Series offers a range from 2.5 to 8 mA min. Turn-on/turn-off times for the devices spec at 20/80 µsec and 120/500 µsec, respectively. $1.35 to $1.75 (1000). Delivery, stock to 10 weeks ARO.

Motorola Inc., Semiconductor Products Sector, Box 52073, Phoenix, AZ 85072. Phone (602) 244-3818. Circle No 384

POWER SUPPLIES
- Are UL recognized and CSA certified
- Feature input EMI filters

Mustang Series power supplies comprise 34 models and offer power levels to 150W. The enclosed supplies have UL recognition and CSA certification. All models have a typical efficiency of 70 to 75% and feature an input EMI filter, inrush-current limiting, output-voltage adjustment, and built-in overload protection. Their line regulation, from low to high line, equals 0.4%, and no-load to full-load regulation equals 0.8%. All models provide a holdup time of 20 msec min. $59.50 (1000).

Computer Products Inc., 2900 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-5500. TWX 510-956-3098. Circle No 386

HEAT SINKS
- Designed to cool TO-3 devices
- Handle 25W in forced-air applications

Designed to cool TO-3 power semiconductors, Series 5021-24 heat sinks can handle as much as 25W in forced-air applications. Because the fins are staggered, heat dissipates directly into the atmosphere instead of being transferred to an adjacent fin. Air circulates freely from all sides for maximum cooling. The devices are available in four heights ranging from 0.5 to 1.25 in. With an input of 6W, the 1.25-in. unit has a 10°C/W thermal resistance under natural convection. Made of aluminum alloy, the devices are available in gold chromate and black, red,
COMPONENTS & POWER SUPPLIES

bronze, or blue anodized finish. 1-in. model, $0.34 (100).

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400.

Circle No 388

DISPLAY

- 100-ft readability
- Horizontally or vertically stackable

The SP-432 gas-discharge display features six 2-in.-high, 7-segment characters. It includes decimal points and commas in each position, with colons following the second and fourth positions, and a plus or minus sign included with the most significant digit. A 150° viewing angle and a 90-FL brightness level make this neon-orange display readable at distances ranging to 100 ft. The display is vertically or horizontally stackable and comes with single-in-line flexible leads. $51.55 (100).

Babcock Display Products Inc, 1051 S East St, Anaheim, CA 92805. Phone (714) 491-5121. TLX 249646.

Circle No 389

POWER SWITCHES

- Designed for use in harsh environments
- UL, CSA, VDE, and SEV approved

Designed for use in harsh environments, Series 22 shock-proof power switches meet IP 65 standards; their chemical-resistive case meets IP 20 standards. Insulated rear connections prevent inadvertent contact. The self-cleaning, double-break, snap-action contacts are available in four configurations. The devices are rated for 12V ac/50 mA min or 380V ac/10 mA max, and have a dielectric strength rating of 2000V ac between all terminals and ground. A variety of illumination options are available: midget grooved T-1½ lamps ranging from 6 to 60V, or T-1¼-type LEDs in 6, 12, 24, or 48V ratings with a choice of red, yellow, or green colors. You can choose between translucent or transparent lenses. All switches are UL, CSA, VDE, and SEV approved. From $6.25. Delivery, four to six weeks ARO.

EAO Switch Corp, 198 Pepe's Farm Rd, Milford, CT 06460. Phone (203) 877-4577.

Circle No 390

FIBER TRANSCEIVER

- Operates at data rates of 20M to 50M bps
- Includes data encoder and decoder circuitry

The P35-8858 is a fully integrated fiber-optic transceiver module operating at data rates of 20M to 50M bps. It is suitable for use with fiber-optic links as long as 600m in LANs, digital telephone exchanges, and PABX equipment. The module interfaces to the optical fiber via twin expanded-beam fiber-optic connectors incorporated into standard DIN-41612 edge connectors. The module includes Manchester bi-phase data encoders and decoders in its transmitter and receiver sections, respectively, and it drives the...
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COMPONENTS & POWER SUPPLIES

fiber with a high-radiance, 850-nm LED. It is available for through-hole or surface-mounting to a PCB. From $350 (100). Delivery for volume quantities, 60 days ARO.

Plessey Optoelectronics Ltd,
Wood Bureote Way, Towcester,
Northants NN12 7JS, UK. Phone
(0327) 51871. TLX 312428.

Circle No 391

Plessey Three-Five Group, 9630
Ridgehaven Ct, San Diego, CA
92123. Phone (619) 571-7724. TWX
910-322-1347.

Circle No 392

ENCLOSURES
- Available in desktop or rack-mount versions
- Accommodate power supplies and disk drives

Offered in desktop or 19-in. rack-mount versions, these VME Bus enclosures are available in 3U, 4U, 6U, and 9U sizes. The 3U unit will accept as many as 5 VME boards; the 6U enclosures can accommodate as many as 21 boards. The systems come in three depths—13, 16.25, and 21 in. You can mount a power supply and your choice of drive mechanism at the front of the enclosure; fans mounted on the rear panel have standard cutouts for various connectors. From $350.

Elma Electronic Inc, 41440
Christy St, Fremont, CA 94538.
Phone (415) 656-3400.

Circle No 394

RECTIFIERS
- Deliver 44A in TO-3P package
- Come in a center-tapped configuration

40CPQ050 and 40CPQ060 dual-die center-tapped, Schottky diode rectifiers deliver 44A at the center tap in versions rated for repetitive peak reverse voltages of 50 or 60V. The devices are configured with two
anode input pins and a single cathode center-tapped output pin that is connected to the base plate. The rectifiers have a 525A nonrepetitive surge-current rating, a 25-mA peak reverse-current rating (at $T_J=25^\circ C$), 0.6°C/W per junction junction-to-case thermal resistance, and a −40 to +125°C operating range. The forward voltage drop measures only 0.63V per junction at 25°C. 40CPQ050, $6.41; 40CPQ060, $6.58 (100). Delivery, eight weeks ARO.

*International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8837.*

### POWER SUPPLY

- **Designed for small analog systems**
- **Operates to 50°C without derating**

Designed for small analog systems, the Model 22-100 power supply has a dual-tracking ±15V/±100-mA output. The pc-board-mountable unit has ±0.02% line and load regulation and 2-mV max output noise. The output is factory set to within ±0.5% of nominal output and uses foldback current limiting for short-circuit protection. The unit can operate with case temperatures of 50°C without derating. Two mounting kits are available: Model MK015 features an edge connector, and Model MK08B has a barrier strip. Model 22-100, $83; MK015, $30; MK08B, $23.

*Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 269888.*

---

**Relays**

- **Handle 20A loads**
- **Have 100,000-operation lifetime**

OZF Series relays incorporate pc-board coil terminals and 0.187-in. quick-connect load terminals to facilitate field wiring in automotive, appliance, and process-control applications. UL recognized, the spst miniature relays can switch 20A at 120V ac or 28V dc and have a 100,000-operation lifetime at full load. Coil voltage ratings range from 3 to 48V dc, and the relays are available in standard and sensitive versions. Wide insulation spacing provides 5-kV ac dielectric and 10-kV surge-resistance ratings. The contact material is silver cadmium oxide. $2.15 (1000). Delivery, eight to 12 weeks ARO.

*Original Electric Manufacturing Co Inc, 123B Lincoln Blvd, Middlesex, NJ 08846. Phone (201) 271-5770.*

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**CIRCLE NO 26**

EDN November 26, 1987
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

DSP SOFTWARE
• Provides progressive instruction on DSP functions
• Runs on IBM PCs and compatibles

ILS Starter is a subset of the full ILS (Interactive Laboratory System) DSP package. The software runs on an IBM PC/XT or compatible with 640k bytes of RAM, a math coprocessor, a hard disk, and a Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), or a Hercules graphics card. The menu interface provides a structured environment that helps you select specific DSP operations, specify operation options and parameters, and store, in data sets, the data requested by the menu interface. A primer manual, *Getting Started with ILS*, guides you through a variety of DSP operations. A command user interface provides more processing options than the menu interface and lets you use standard ILS commands to specify DSP operation. You can employ the package with IBM's DACA boards or with high-speed data-acquisition hardware from Data Translation. $495.

**Signal Technology Inc**, 5951 Encina Rd, Goleta, CA 93117. Phone (800) 235-5787; in CA, (805) 683-3771. TWX 910-334-3471. Circle No 398

SIMULATION MODEL
• Lets you simulate the Am29000 32-bit µP
• Provides advanced troubleshooting aids

The Am29000 SmartModel is a simulation model of the Am29000 32-bit µP from Advanced Micro Devices (Sunnyvale, CA). The model lets you perform simulations that verify both hardware and software designs. It also lets you check for violations of timing requirements (such as setup and hold times or minimum pulse widths) and analyzes usage conditions such as I/O protocols and initialization parameters. Whenever the model detects an error condition, it emits a detailed error message that allows you to pinpoint the time, location, and nature of the problem. It is currently available for use on Mentor Graphics systems; versions for other systems are in development. $6900.

**Logic Automation Inc**, Box 310, Beaverton, OR 97005. Phone (503) 690-6900. Circle No 399

FILTER-DESIGN PROGRAM
• Lets you design and analyze passive filters
• Handles any filter type with as many as 21 poles

The LCFIL stand-alone, menu-driven filter-design program runs on IBM PCs and compatibles or on the Apple Macintosh. You can design highpass, lowpass, and bandpass filters that have as many as 21 poles, and you can specify Butterworth, Cauer, Chebyshev, and Bessel response characteristics. The program computes filter magnitude, phase, and delay characteristics, and provides both normalized and actual component values. An optional signal-processing module that works with LCFIL analyzes and plots the transient response of your filter design. The vendor provides optional drivers for CGA-, EGA-, and Hercules-compatible graphics adapter boards, and for as many as 30 different plotters. $95.

**BV Engineering**, 2200 Business Way, Suite 207, Riverside, CA 92501. Phone (714) 781-0252. Circle No 400

PARTS LISTER
• Builds simple or customized parts lists
• Lets you load output files into a Dash schematic

The Enhanced Part List Utility software package lets you build either a simple parts list, showing quantity, part name, and location...
designator of each part, or a customized list with additional information supplied by the operator. The area-translator utility can format the parts-list output files (or any ASCII file) into a FutureNet area file that you can load directly into a FutureNet Dash schematic. The $95 program runs on IBM PCs and compatibles; registered users can upgrade their earlier versions to the Enhanced version for $45.

CAE Utilities, 14819 Sherman Way, Suite 8, Van Nuys, CA 91405. Phone (818) 989-3308.

Circle No 401

SCHEMATIC CAPTURE
• Provides schematic capture and logic simulation
• Lets you generate artwork on a printer

EE Designer version 1.7 is a PC-based software package for schematic capture, logic simulation, pcb-board design, and artwork generation. This version is enhanced by a graphics kernel that lets you define trace widths, pad sizes, and D-code settings for Gerber photoplotting. The router now offers orthogonal-snap and double-snap modes for improved schematic routing. The package contains a symbol library with corresponding cross-reference files; the plot-file feature lets you write your own device drivers so that you can generate prototype-quality artwork on an Epson-compatible, dot-matrix printer. You can direct output to pen plotters, photoplotters, numerical-control drill tapes, and laser printers that can use the HPGL graphics language. $995; upgrade to version 1.7 for current users, $200.

Visionics Corp, 343 Gibraltar Dr, Sunnyvale, CA 94089. Phone (408) 745-1551.

Circle No 402

ANIMATION SOFTWARE
• Controls lighting and motion path
• Provides real-time wireframe preview of animation sequences

The Topas (3-D object processing and animation) Animator is a professional keyframe animation program that lets you animate model attributes including position, orientation, size, warp, color, transparency, camera position, and zoom factor, as well as light position, color, and intensity. It lets you define and edit keyframes and time

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controls, and provides script file management. You can obtain a wire-frame preview of your animation script on your microcomputer display. The package includes the Topas Pro-Modeler and 3-D image builder and editor that let you create images on your microcomputer or capture them from standard videotape equipment. You can add as many as nine light sources and render the image to obtain 512×512-, 1024×1024-, or 2048×2048-pixel resolution; you can store the resulting image in the TGA format used by the AT&T Targa display board with which the software operates. You'll need an AT&T PC6300+ or an IBM PC/AT or compatible equipped with 640k bytes of RAM, a 10M-byte or larger hard disk, and DOS 2.0 or a later version. You must also have 8M bytes of RAM on a memory board that is compatible with the Lotus-Intel-Microsoft EMS extended-memory specification, an AT&T Targa or Vista display board, and a mouse or digital input pad. $11,995.

AT&T, Graphics Software Labs, 10291 N Meridian, Suite 275, Indianapolis, IN 46290. Phone (317) 844-4364.

Circle No 403

SCANNER UTILITY
- Allows you to display and store images captured by a scanner
- Lets you edit individual pixels or complete images

The GEM Scan utility package controls image scanners from Canon, Princeton, Hewlett-Packard, and other vendors. The program runs on an IBM PC or compatible with at least 512k bytes of RAM and a hard disk. The package lets you bring an image into memory via the scanner, after which you can manipulate individual pixels or transform the image in various ways without diminishing the 300-dot/in. resolution. When finished, you can send the customized image directly to an output device, save it on disk, or import it into a document that you're processing. You can execute GEM Scan directly from DOS or from graphical interfaces such as the vendor's GEM Desktop or Microsoft's Windows. $95.

Digital Research Inc, Box DRI, Monterey, CA 93942. Phone (408) 649-3896.

Circle No 404

UNIX FOR 80386
- Makes full use of the extended 80386 instruction set
- Based on Unix System V Release 3 for the 80386

The System V/386 multitasking, multiuser version of Unix System V Release 3 is designed specifically for use on 80386-based personal com-

**ATE For Manufacturing: Just In Time**

Reilly's the name. Dogboard Reilly. All-around good Joe. Test engineer. Companies with big test problems look to me and an outfit called Support Technologies for help. Take Steinwood's Stellar Systems. I was sawing logs when the phone rang at 2:00 AM. It was Eddie Starr, Steinwood's VP of Manufacturing:

"Reilly, I'm in big trouble. Steinwood's implementing a Just In Time line and I have to be ready to test those boards in a couple of weeks!"

"Keep your shirt on, Eddie. 'JIT' is Support Technologies' middle name." I gave Eddie the facts about Support's 3100 Performance Test System and his JIT line.

- Able to test today's and tomorrow's state-of-the-art boards
- High-speed driver/sensors
- Small footprint
- Growth path through versatile open architecture
- Low capital investment for fast payback

"Well, Reilly, you're a hero in my book."
"You're referring to your checkbook I hope, Eddie. My fee's still twenty-five bucks a day—and expenses."
"Go easy on the expenses this time, Reilly."

Let Support 'JIT' Technologies show you how their 3000-Series test systems can solve your functional test mysteries. Call or write for your free copy of Dead Men Don't Fix Boards.
It provides 80286 compatibility, dynamic buffer allocation, shared libraries, a link kit that allows user-installable device drivers, and demand-paged virtual-memory management. The kernel provides record and file locking; it can make full use of an 80387 math coprocessor and includes an emulator for systems without an 80387. System administration features are menu-driven, and the system has an extensive on-line help facility. An optional DOS-Merge module allows you to execute DOS programs under Unix while running Unix application programs. For computation-intensive jobs, an 80386-based machine running System V/386 can accommodate as many as eight users; in less-demanding applications, as many as 33 users can share the same computer. Two versions are available: run-time system, $199; full software-development and text-processing system, $799; DOS-Merge module, $395.

Microport Systems Inc, 10 Victor Square, Scotts Valley, CA 95066. Phone (800) 722-8649; in CA, (800) 822-8649. TLX 249554.

Circle No 405

ACTIVE FILTER

- Lets you combine different filters for analysis
- Provides manual or automatic pole/zero pairing

The enhanced Active Filter Design version 3.0 lets you design all-pass active filters and calculate component values for designs that use National MF-10 switched-capacitor filter ICs, as well as the Reticon ICs handled by previous versions of the program. Version 3.0 also allows you to examine the phase delay of a filter design. The interactive graphics feature lets you analyze both the impulse and the step response of your design, and you can see the effect of cascading several filters (which may be of different types). You can select Butterworth, elliptic, Chebyshev, or Bessel response characteristics for designs that use voltage-controlled voltage-source, multiple-feedback, biquadratic, state-variable, or switched-capacitor techniques. A Spice file-conversion utility converts output files to the Berkeley 2G.6 format that is directly usable by most versions of the Spice simulator. To run Active Filter Design, you'll need an IBM PC, PC/XT, PC/AT, or compatible computer equipped with at least one floppy-disk drive, at least 350k bytes of RAM, and DOS 2.0 or later. Active Filter Design 3.0, $525; Spice file-conversion utility, $125.

RLM Research, Box 3630, Boulder, CO 80307. Phone (303) 499-7566.

Circle No 406

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- Has repetition rate variable from 0 to 25 MHz
- Features 0.3- to 2-nsec rise times

You can vary the output of the AVMM-2-C pulse generator from 0 to 5V and use it to trigger TTL, or you can switch on an internal adjustable dc offset and use the unit to trigger ECL circuits. You can get units with positive, negative, or dual (positive and negative) output. You can adjust the repetition rate from 0 to 25 MHz, the pulse width from 0.5 to 10 nsec, and the rise time from 0.3 to 2 nsec. A synchronous output with a variable delay aids in scope triggering. As an option, you can get units with inputs to which you can apply dc voltages for remote control of output amplitude, pulse width, and offset voltage. The 4x8x12-in. units operate from 110/220V at 50 or 60 Hz. $2238 to $3148. Delivery, 60 days ARO.

Avtech Electrosystems Ltd, Box 5120 Station F, Ottawa, Ontario, Canada K2C 3H4. Phone (613) 226-5772. TLX 0534591.

Circle No 407

DISTURBANCE ANALYZER

- Measures environmental and power conditions
- Accepts five plug-in modules simultaneously

Along with making many ac-line related measurements, the 626A disturbance analyzer can monitor humidity, dc voltages, radiated RF, temperature at multiple points, and sequences of events on as many as eight channels. You can install as many as five plug-in modules that enable the unit to monitor single-phase and polyphase ac voltage, current, and power; the harmonic distortion of ac current; the magnitude and duration of ac-voltage sags and surges; and the magnitude, direction, and duration of ac-current impulses. Because the unit records the time of occurrence of all the phenomena that it detects, you can use its output to correlate malfunctions in the unit under test (UUT) with power and environmental disturbances. A 3-phase graphics module stores "pictures" of power-line disturbances to simplify determination of the cause of and remedy for malfunctions in the UUT. You can print the pictures on an optional graphics printer or on an external dot-matrix printer. Mainframe, $4200; plug-ins, from $550.

Dranetz Technologies Inc, 1000 New Durham Rd, Edison, NJ 08818. Phone (201) 287-3680.

Circle No 408

CALIBRATORS

- Provide dc and ac voltage, current, and resistance
- Use your PC as system controller

3000K Series precision calibrators use your IBM PC or compatible as an IEEE-488 controller. Their output ranges from 100 nV to 1200V dc; 100 nV to 1000V ac, 0.001 Hz to 100 kHz; 100 µΩ to 2000 MΩ; and 100 nA to 20A. Their resolution is 0.5 ppm of range; they have a basic accuracy of 10 ppm for a year following calibration by a standards lab. You can set their output at zero or reverse polarity with a single keystroke. When you program a voltage of 200V or more, the units automatically switch their output to a set of high-voltage terminals and illuminate a lightning-bolt warning symbol on their front panels. Software included with the units allows you to store calibration procedures for all of your instruments. From $9700.

California Instruments Corp, 5125 Convoy St, San Diego, CA 92111. Phone (800) 356-2244; in CA, (800) 821-1634.

Circle No 409
**60-MHz SCOPE**

- Digitally displays measured quantities on screen
- Also displays control settings

The LB0-2060 displays two channels, each of which has a 60-MHz bandwidth and sensitivity adjustable from 0.5 mV/div to 5V/div. It can also display the sum of or difference between the inputs. By positioning a pair of cursors on one or two waveforms, you can obtain an on-screen digital display of the difference in voltage or the elapsed time between the two points, the frequency of a signal, or the phase difference between a pair of signals. On-screen digital displays also indicate the settings of the front-panel controls, including the trigger conditions. The unit has dual timebases and allows alternate triggering. $1490.

**Leader Instruments Corp.** 380 Oser Ave, Hauppauge, NY 11788. Phone (516) 231-6900. TWX 510-227-9669.

Circle No 410

**ANALYZER**

- Displays voltage and impedance magnitude vs frequency
- Has built-in tracking generator

The Model FSAP Spectnet displays voltage vs frequency, impedance magnitude vs frequency, and transfer-function magnitude vs frequency, thus combining the functions of a spectrum analyzer and a scalar network analyzer in a single instrument. It covers frequencies from 50 kHz to 1.8 GHz and includes a built-in tracking generator. You can use it to display the frequency response of passive and active networks. The 3-color display is annotated with voltage, impedance, and frequency scales appropriate to the measurement you are making. When you are setting up a test, menus appear on screen to define soft-key functions. You can store seven complete test...
setups in internal memory, program the instrument via a built-in IEEE-488 interface, and produce hard copies of screen displays on an external printer. Model FSAP, $17,900; Model FSAL, which lacks network analysis capability, $14,900. Delivery, 90 days ARO.

Rohde & Schwarz-Polarad Inc, 5 Delaware Dr, Lake Success, NY 11042. Phone (516) 328-1100. TWX 5 10-22 3-04 14.

Circle No 411

IC DIAGNOSTIC SYSTEM

- Includes scanning electron microscope
- Compares internal voltages with predicted values

The IDS 5000 integrated diagnostic system permits designers of ICs and hybrid circuits to investigate circuit performance and debug devices at the individual circuit-element level, something that designers of board-level products have always been able to do. A scanning electron microscope (SEM) provides a micrograph of the chip under test on the workstation monitor. The contrast of conductors displayed in the picture responds to voltage changes within the chip. The system can be linked to the computer containing the design database, and a split-screen display can simultaneously show, in addition to the SEM picture, the logic equations that serve as the design input, the output waveforms produced by a logic simulator, and the layout produced by a CAE router. $495,000. Delivery, 60 days ARO.

Schlumberger/ATE, Advanced Products Group, 1601 Technology Dr, San Jose, CA 95110. Phone (408) 437-5000. TWX 910-338-0558.

Circle No 412

IEEE-488 EXTENDER

- Links two buses via as much as 4000 ft of fiber-optic cable
- Allows 14 local and 14 remote devices

The Extender-488/F transmits and receives at 115k bps. A fiber-optic link provides electrical isolation between the local and remote devices. With the exception of parallel polling, operation is transparent to the IEEE controller. Speed requirements of parallel polling preclude this mode from operating transparently; in parallel poll mode, the controller performs two polls and discards the data from the first. $995.

IOtech Inc, 23400 Aurora Rd, Cleveland, OH 44146. Phone (216) 439-4091. TWX 650-282-0864.

Circle No 413

ANALYZER/EMULATOR

- Displays register contents, I/O line, and port data
- Includes stimulus generator and EPROM programmer

While you are debugging your program, the Unilab 8600 presents a continuously updated display of register contents, as well as 48 channels
TEST & MEASUREMENT INSTRUMENTS

max of data on I/O lines and ports. It will also display the contents of a range of memory that you define. It communicates with the host computer—an IBM PC or compatible—via a parallel bus and provides a 2730-cycle-deep trace buffer. The unit includes a stimulus generator and an EPROM programmer. You can obtain a program performance analyzer as an option. $2990.

Orion Instruments, 702 Marshall St, Redwood City, CA 94063. Phone (800) 245-8500; in CA, (415) 361-8883.

Circle No 414

VIDEO GENERATORS

• Deliver pixels at 1.6 GHz
• Modular design allows user configuration

You can configure the 8700 Series modular video generators as stand-alone instruments, to work under the control of an ATE system, or to be controlled by your IBM PC or compatible computer. You can select from nine video interface modules, four of which provide analog and digital output, four of which provide analog output only (both 50 and 75Ω), and one of which provides a 1-bit digital output that can handle rates as high as 1.6 GHz. In the stand-alone and ATE versions, the mainframe incorporates a 68000-based µC with a 640k-byte disk drive, as much as 2M bytes of video RAM, and as much as 1M byte of program memory. The vendor now furnishes on disk all information that might be subject to change during the life of the instrument, so you no longer have to program EPROMs to customize the software.

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Quantum Data, 2111 Big Timber Rd, Elgin, IL 60123. Phone (312) 888-0450. TLX 206725.

Circle No 415

PROGRAMMER

• Programs multiple EPROMs with the same or different data
• Works with terminal or integral 25-key pad and LCD display

You can use the S125-EG as a set EPROM programmer or as a gang duplicator. It programs 16- or 32-bit-word sets. It will duplicate eight (16 optional) devices from internal RAM or from a master. You can download 512k bytes of data (1M byte optional) into internal RAM via the device's RS-232C port. The unit's built-in 25-key keyboard and 32-character LCD display allow you to operate it in a stand-alone mode. Its RS-232C port lets you connect it to an external terminal or to an IBM PC or compatible running either Promsoft or Promlink software. A second RS-232C port is optional. The unit performs self-test routines; it detects empty or failing sockets and devices inserted upside-down. It saves default parameters in 2k bytes of nonvolatile RAM. As an option, it can support 40-pin µPs and 3-voltage EPROMs. $995.


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Rental instruments cataloged
This 1987-88 catalog lists test equipment available for rental from major instrumentation companies such as Hewlett-Packard, Tektronix, and Intel. The 30-pg booklet comprises an equipment listing and an index of manufacturers. Among the product types included are analyzers, meters, generators, oscilloscopes, desktop computers, and telecommunications instruments. Rental terms and conditions and toll-free numbers of the nearest distributors are given.

Genstar Rental Electronics Inc, 6307 DeSoto Ave, Suite J, Woodland Hills, CA 91367. Circle No 420

Listing of test and measuring instruments
In its 1987 short-form catalog of test and measuring instruments, the manufacturer presents spectrum and modulation analyzers; scalar analyzer systems; microwave sweepers, microwave signal sources, and microwave counters; and power sensors and power meters. The 4-color publication also describes white-noise test sets; mobile/cellular radio test sets; transceiver test systems; TV test systems; and GPIB adapters.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401. Circle No 421

Help for configuring automatic test systems
Covering relay switching from dry circuit to approximately 100W configurations, *A Guide to Signal Switching in Automated Test Systems* is designed to help personal-computer users automate testing and provide faster data acquisition than was previously possible with manual systems. It discusses how switches affect overall measurement, how to control noise, how to make connections, and how to analyze errors. Sample applications and system models complement the information.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Circle No 422

Reference book covers nickel alloys
The 140-pg publication entitled *Nickel Alloys for Electronics* is useful in evaluating and designing nickel alloys. Numerous graphs and tables supplement explanations of physical and mechanical properties; a special section is devoted to nickel electroplating. Other sections cover semiconductor packaging, leadframe and glass-sealing alloys, reference data on nonmetallic materials, nickel, copper-base connector and spring alloys, and stainless steel alloys.

Nickel Development Institute, 7 King St E, Toronto, Ontario, Canada. Circle No 423

Voltage references for A/D converters detailed
*Application Note DS15AN1* explains the use of voltage references with the manufacturer's CS501X Series A/D converters and CSZ511X Series S-to-Z converters. Included are reference design considerations, suggested reference circuits, and a design example. Graphs and tables highlight the text.

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Circle No 424

Custom MMICs and digital ICs presented
This 6-pg brochure, *Gallium Arsenide Custom and Semicustom Integrated Circuits*, describes how custom MMICs (monolithic microwave ICs) and digital ICs are designed. The pamphlet summarizes the company's various program services and the 1- and 0.50-µm fabrication processes. It also provides examples of custom circuits.

Harris Microwave Semiconductor, 1530 McCarthy Blvd, Milpitas, CA 95035. Circle No 425

Catalog summarizes Z-System software
The 20-pg *Z-Catalog* lists various configurations of the Z-System (an operating system for Z80-, Z280-, and HD64180-based microcomput-
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TM of Dg. Equip. Corp.
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VENIX: TM of VentexCorp

**LITERATURE**

Guide details optoelectronics products

The 45-pg, 4-color *Optoelectronics Product Guide* is a combination data book-selector guide that provides electrical and optical characteristics, package outlines, and pinout specifications. It also describes product features and applications. It’s divided into sections covering visible lamps; single- and multiple-digit displays; integrated displays; custom capabilities; infrared emitters and detectors; and optocouplers.

Three-Five Semiconductor Inc, Box 111, Tempe AZ 85282.

Circle No 427

Disk speeds selection of power transistors

*Spectsc in Secs* is a catalog on a disk that contains information on more than 1600 bipolar power transistors and power MOSFETs plus more than 3500 cross-references. It requires an IBM PC or compatible with a 384k-byte RAM. The disk communicates with you in any of five user-selectable languages. In the bipolar-transistor category, you can specify characteristics for breakdown voltage, collector current, power dissipation, polarity, package, price, and 10 other parameters. The TMOS (T-configuration MOS) power-MOSFET category contains breakdown voltage, drain current, power dissipation, package, price, and seven other parameters. The disk is available for $2 by requesting DK101/D.

Motorola Semiconductors Products, Literature Distribution Center, Box 20924, Phoenix, AZ 85063.

INQUIRE DIRECT

Catalog of linear ICs and hybrid circuits

The company's 20-pg catalog sums up its range of linear ICs and custom and standard hybrid circuits for the military and industrial markets. It includes specifications and diagrams of the company's power interface.
products for computer peripheral equipment, as well as switch-mode power-supply circuits, linear voltage regulators, power interface circuits, and Darlington transistor arrays. In addition, it features a parts list cross-referenced by product type and package type, and includes representative and distributor listings.

Silicon General, 11861 Western Ave, Garden Grove, CA 92641.

Circle No 429

Memory and μPak products featured
This short-form catalog provides information about the company's line of static RAMs and μPak products. It includes military monolithic static RAMs as well as high-density and high-performance memory modules. Besides specifications and package information, the 20-pg brochure contains descriptions of the vendor's part-numbering system and military manufacturing processes.

Electronic Designs Inc, 42 South St, Hopkinton, MA 01748.

Circle No 432

Catalog features test equipment
The company's 52-pg, 4-color catalog describes digital multimeters, oscilloscopes, telecommunications test equipment, function generators, and frequency counters. Along with specifications and color photographs of each product, it includes a section that illustrates the company's digital temperature-measuring instruments.

Beckman Industrial Corp, 3883 Ruffin Rd, San Diego, CA 92123.

Circle No 433

Rental catalog
The 48-pg Electronic Instruments Rental Catalog, Vol 25, lists a broad selection of general-purpose test equipment that you can rent, lease, or buy. The book also contains a manufacturer/model index.

Continental Resources Inc, 175 Middlesex Tpk, Bedford, MA 01730.

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EDN November 26, 1987

This book covers the principles of signal processing including signal analysis, probability, random signals and systems, and filtering and detection theory. It features examples geared toward computer implementation of various algorithms for physical problems encountered in electronic information processing. Individual chapters cover linear, analog, and digital transforms; matrix theory; and estimation and filtering methods. The book also contains extensive coverage on detection theory and sequential and nonparametric detection methods.


This text presents both a conceptual overview and a detailed analysis of microwave circuits. It features precise formulas for the design of passive elements, giving quantitative specifications for many semiconductor microwave circuits. The book also includes the general principles of detection, mixing, amplification, and oscillation, as well as a discussion on noise and the limitations of power.


Along with descriptions of switching devices and methods that meet the requirements of high-energy pulsed systems, this book explains the design and performance of switches capable of handling more than a billion watts of pulsed energy. Included is physical and design information on gas-insulated spark gaps, solid dielectric switches, liquid dielectric switches, exploding wires or fuses, explosively assisted circuit breakers, and vacuum and low-pressure closing switches.


This reference book compares monomode/multimode technologies and describes applications from...
both a systems and a component viewpoint. It presents several state-of-the-art applications: monomode sensor operation; monomode-cable plant design, using various components; circuit-design techniques for transmitters and receivers; integrated fiber-optic design and fabrication; and angular division multiplexing.


This reference discusses three categories of adaptive filters: adaptive finite-impulse-response (FIR) filters, adaptive infinite-impulse-response (IIR) filters, and adaptive property-restoral filters. For the use of FIR filters, the authors present the most popular analytical tools and a collection of design guidelines; for the use of adaptive property-restoral and the IIR filters, they focus on theoretical foundations and suggested applications. The text includes a detailed description of the purpose and motivation of adaptive filtering in three practical signal-processing problems.

**The Viewport Technician**, by Michael Brian Bentley. 496 pgs; $24.95; Scott, Foresman and Co, Glenview, IL, 1987. Phone (312) 729-3000.

This reference is useful for designing, developing, and coding software that you can port from one system to another. The book covers data structures, utility routines, program language, graphics interfaces, and source-code organization. It gives a technical comparison of the following computers: Amiga with Intuition; Atari ST with GEM; IBM with GEM or Windows; Macintosh; and Apple II GS. The author includes numerous charts, graphs, and tables.


This book emphasizes the practical aspects of the use of both analog and digital electronic devices in measuring systems. Approximately 100 applications are discussed, including some specialized measurement and control systems.
Article-writing programs load perks—and pressure—on engineers

Once considered the also-rans of a company's publicity efforts, trade-press articles have recently been recognized as a cost-effective means of publicity. The successful publication of articles has become an important and much-pursued goal of public-relations teams. But much of the responsibility for preparing technical articles falls squarely on a company's engineers, who provide the technical expertise. And, although more companies are using cash awards, prizes, commemorative plaques, and recognition ceremonies to entice their engineers into writing articles, it is still not clear when engineers are supposed to find the time to write.

Formerly, a company trying to promote its product and image looked on its engineers' magazine bylines and conference participation as freebies. Most efforts to boost product recognition and corporate visibility took the form of advertising campaigns. But as competition in the electronics industry came to a head in the late 1970s and early 1980s, companies sought more creative, less obvious ways of promoting themselves.

Now, technical articles, because of their potentially large audiences, have become firmly entrenched features of most public-relations and corporate self-promotion strategies. "It's an important part of building image in the minds of our customers and others in the industry," says Nancy Teater, press-relations manager for Hewlett-Packard's Electronics Instrument Group in Palo Alto, CA. And, what's more important, she adds, "it's a lot cheaper than advertising."

Cost-effective benefits

Indeed, the cost advantages of article publication versus advertising have motivated many companies to refocus their publishing goals in recent years. "We took a hard look at where we wanted to spend our money," says John Hamburger, manager of product public relations for Advanced Micro Devices (Sunnyvale, CA). Whereas his company once paid engineers for articles published in any journal or magazine, it now pays only for those articles published in a dozen trade magazines selected for their large circulation and breadth of coverage.

Magazine bylines also offer something that money can't buy: credibility. "Reading an article about one of our products means much more to a design engineer than seeing our ads does," says Laura Maguire of United Technologies Microelectronics Center (UTMC), a Colorado maker of military components. Debra Seifert, marketing communications manager of Tektronix's Laboratory Instruments Div (Beaverton, OR), says that research done by her department confirms this belief. "Technical articles always come out high on the list of places engineers turn to when they're looking for information on new products."

The opportunity to reach existing and potential customers is another factor that has led an increasing number of companies to add weight to their technical-article programs.
Analog Devices' technical publicity manager, Al Haun, says that technical articles disseminate application tips for his company's component products. What's more, he says, the articles keep the company's name in the limelight.

**Cash benefits for engineers**

Despite the involvement of public relations and marketing personnel, a company's publishing activity, of necessity, centers on its engineers. To encourage engineers to squeeze time out of their already busy schedules, nearly all large companies offer their employees a variety of honoraria and other incentives. Consumer-product companies, for example, offer their engineers merchandise from various product lines. Financial incentives include matching the magazine's payment or making a cash award calculated on a per-page basis.

Some companies lavish attention on their engineers-cum-writers in the hopes of attracting more of them. At Tektronix's Laboratory Instruments Div, for example, engineers receive cash awards for each article that they publish with a $500 cap per article. During quarterly division meetings, the general manager awards each published engineer a check and a polished pewter stein engraved with the engineer's name, the article's title, and its publication date. The company also inscribes each author's name on a plaque that hangs in the facility's conference room.

**Publishing pays**

Some corporations establish honorary organizations for published authors. Signetics, of Sunnyvale, CA, grants its published authors membership in the Signet Society—in addition to the $100 to $300 per page that it pays in cash awards. Motorola Semiconductor (Phoenix, AZ) began its Silver Quill program in 1979; under the program, published engineers qualify for cash payments, honorary plaques, mention in the corporate newsletter, and attendance at recognition banquets. Among the most generous programs are those sponsored by National Semiconductor (Santa Clara, CA) and by components-manufacturer Burr-Brown (Tucson, AZ). National Semiconductor pays $250 per published page, with a $3000 cap. Burr-Brown's Golden Quill program pays $500 to $650 per published page to authors of articles that appear in any of 100 approved journals.

Before initiating the Golden Quill program in 1984, Burr-Brown wasn't "getting the output" it wanted, says Fran Bria, marketing-services manager. Bria won't divulge how much money Burr-Brown has paid out through the program, but he credits the financial incentive with helping the company get two dozen articles published each year—a success rate that he believes renders the program economical. "We feel that a page of published editorial is roughly equivalent to one page of advertising," he says.

**Red-carpet treatment**

For prolific writers who can turn out several articles per year, companies are more than willing to pull out the stops. "If you find someone who's ready to roll—who's a good engineer and a good writer—you need to throw some sort of mantle over them and treat them like gold," says Bill Sharpe, a PR specialist at Hewlett-Packard's Ft Collins, CO, Technical Systems Sector.

The companies most able to offer such treatment and, generally, to support publishing efforts are large companies. Therefore it isn't surprising that many of the bylines that appear in trade magazines belong to engineers who work for such companies. Smaller companies, though, are also beginning to fund author-incentive programs. UTMC, a 7-year-old company with 500 employees, recently increased its per-page cash awards from $100 to $300 and added a $1000 bonus for engineers who write or coauthor five technical articles in one year. Even start-up companies, for whom time is precious, find the stamp of legitimacy that accompanies a published article well worth their efforts. "When something you write is published, it's in the same size type as an article by a large company," says Larry Manieri, vice president of sales and marketing for Sequence, a 3-year-old, San Jose, CA, maker of waveform digitizers. "It makes a small company seem larger than it is. It bolsters your image and makes you credible."

**Publish or perish**

Before engineers can receive any perquisites, however, they must somehow find the time to write. And the increasing pressure on en-
engineers to do so is causing some to ask if engineering has become a publish-or-perish profession.

Some companies consider writing an optional, after-hours project. Bria says that Burr-Brown requires its author-engineers not to let their writing interfere with their engineering assignments. "We ask them to do the writing on their own time," says Bria. "We feel it's a voluntary effort for which we reward them amply."

Other companies, however, consider writing part of an engineer's job and a condition for advancement. "If you're going to go to the rank of division fellow—which is equivalent to a vice president—one criterion is that you become a published author, a spokesperson for the company and the industry," says Analog Devices' Haun. Haun concedes that such a requirement poses a challenge, because "engineers are already working 10 to 12 hours a day."

Tektronix, too, requires that its top-ranking engineers be published. "To get to the highest level of engineering, you have to become an expert in your field," says Seifert. "To prove that [you've done so], you have to assemble all of the work that you've published."

Balancing assignments

Even at those companies that require their engineers to write, however, engineering managers prefer to see engineers expend their creative energies on design problems rather than writing tablets. Although Tektronix requires that engineering managers approve any writing assignments that engineers take on, Seifert says the continuing time tug-of-war "can be very tricky."

Changing industry conditions are tempering writing policies at some companies. Hewlett-Packard, for example, is in the midst of some corporate soul searching over its publishing procedures. Historically, the company has taken a dim view of competitors' author-incentive programs; its divisions offered some form of remuneration, but the rewards were meager compared with the liberal offerings of other employers.

Financial incentives for writing are "controversial to an old-line engineering company" like Hewlett-Packard, where writing has been considered part of an engineer's job, rather than an optional activity, says Sharpe.

Yet Sharpe says the company is now considering changing its policies in response to new developments in the engineering environment. "The research and development lab a few years ago was much more academic, not quite as tightly tied to return-on-investment as it is now," he says. "We've seen a tightening of the reins on an engineer's time." And as a result, Sharpe says, there's been "an erosion of some of the more creative efforts" such as writing.

To shore up publishing activity at one Hewlett-Packard sector, Sharpe is conducting a pilot program that provides leadership for the writing projects and offers cash awards, plaques, and letters of recommendation to engineers who participate.

For all their efforts, though, some companies see a dark side to the high visibility that engineers receive from articles that carry their byline. Says Scott of Signetics: "You get someone who's very good, and the first thing you know, someone's looking [to hire] him, so there is a liability to this."
## CAREER OPPORTUNITIES

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<th>Parent Company</th>
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| PRESENT OR MOST RECENT EMPLOYER | 
| Name | Parent Company |
| Home Address | Your division or subsidiary: |
| City | State | Zip |
| Home Phone (include area code): | Business Phone if O.K. to use: |

| POSITION DESIRED | 
| Present or Most Recent Position | From | To | Title |
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| EXPERIENCE | 
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| Job Title: | 
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| Years Experience | Base Salary | Commission | Bonus | Total Compensation | Asking Compensation | Min. Compensation |
| Date Available | I Will Travel | Light | Moderate | Heavy | I own my home. How long? | Rent my home/apt. |
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<th>Non-U.S. Citizen</th>
<th>My identity may be released to:</th>
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<th>WILL RELOCATE</th>
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Beware of the hidden costs of foreign sourcing

As American companies face further competition from foreign companies that seem to offer lower quotes for comparable products, US purchasing managers need to be aware of the hidden costs of sourcing abroad, according to a study by the economic-consulting firm of Quick, Finan, & Associates (QF&A) (Washington, DC). Although this report was compiled for the National Tooling and Machining Association (NTMA), similar purchasing cautions apply to the electronics industry as well. The consultants found that disregarding hidden costs can be especially significant with foreign sources. In some instances, the difference in cost between domestic and foreign sources vanishes when hidden costs and complications are considered.

In a hypothetical 2-stage buying decision, purchasing managers first rate their sources according to the quality and responsiveness of the likely suppliers. But these characteristics are difficult to quantify, so once a supplier passes this test, quoted price dominates the second stage of the decision.

Because of the fierce competition between domestic and overseas companies for contracts with US-based customers, the NTMA will fight foreign sourcing by educating potential customers about hidden costs. NTMA President Matthew Coffey believes the association’s forging of this “self-help” program is a more appropriate and constructive response than turning to Washington for protection. QFA believes the approach could critically modify purchasing patterns as well as reinforce the position of US shops involved.

Professional books and journals have long recognized and discussed the problems that hidden costs pose for purchasing decisions. Experts have defined geographic location, the distance between supplier and purchaser, as a critical consideration during periods of rapidly shifting production priorities. Important, too, are transportation alternatives, inventory costs and controls, and the supplier’s quality controls. A given supplier’s reserve capacity should not be ignored, and its general flexibility, or ability to respond to emergency and rush shipments, should not be forgotten.

Foreign sourcing intensifies some of these problems and adds others. As geographic distances increase, a supplier’s flexibility and general responsiveness to special situations is likely to lessen. Transportation alternatives also become more complicated. The turnaround time for repairs and modifications can lengthen as well. If purchasing agents and engineers want to visit sites abroad to evaluate them, hidden costs include their time and transportation. And, obviously, communications costs rise in foreign-sourcing situations.

There are other hidden costs peculiar to foreign sourcing. Quoted prices, for example, don’t include customs duties. Financing may require international processes involving extra fees and paperwork. If a supplier cites a price in a foreign currency, the purchasing agent should consider possible fluctuations in the foreign-exchange rate. In terms of the contracts themselves, QFA points out that some European and Asian suppliers demand annual contracts with specific monthly shipments, whereas US suppliers are more flexible.

Different interpretations of technical, industrial, and business terms can defy the talents of the best translator. In the US, for example, “first shot” means ready to sample and inspect; in other countries, the term often refers to a stage at which many critical features are uncompleted.

Quantifying all these hidden costs is a tricky problem. Some US companies have successively monitored the hidden costs for domestic sourcing; the principles they’ve employed can be useful in evaluating foreign suppliers as well. Three possible techniques involve evaluating the performance of suppliers according to the varied importance of their characteristics, evaluating by linear averaging, and evaluating by cost-ratio methods.
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<thead>
<tr>
<th>Model</th>
<th>Freq Range (MHz)</th>
<th>Gain Max (dB)</th>
<th>NF (dB)</th>
<th>DC Power (mA)</th>
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