Technology improvements yield high-speed op amps
integrated into a networked environment? No problem. We'll even take it a step further. With our Ethernet-based LAN, your PL 386 becomes part of a truly distributed environment—including PC/ATs, high performance accelerators, layout workstations and the Digital Microvax II. All sharing the same operating system, the same database, the same proven software.

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Circle 41 for demonstration

![Waveform Generator](image)

1. Place “thumbtack” markers.

2. Insert standard waveform.

3. Reset “thumbtack” marker positions.

4. Stretch “rubberband” with edit cursor.

5. Move “thumbtacks” and complete waveform editing.

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PMI's newest high speed op amp guarantees slew rate of 50V/µs and settling time of 1µs to 0.01%. With its 10MHz gain bandwidth and 850kHz full power BW, the OP-42 combines high speed with accurate DC performance.

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DESIGN FEATURES

Special Report: Monolithic op amps

Monolithic op amps continue to evolve within the traditional performance categories, but many of this year's models bridge those familiar classifications by combining speed with precision, with low noise, and even with low supply current.—Tarlton Fleming, Associate Editor

EDN's DSP Project—Part 3

We present a hands-on account of how we used some of the tools (described in part 2 of this series) to create a transponder.—David Shear, Regional Editor

EDN's DSP Chip Directory

In EDN's first DSP Chip Directory, an offshoot of our traditional annual µP/µC Chip Directory, we concentrate on µP-like DSP devices.—Robert H Cushman, Special Features Editor

Check list helps you choose a pc-board autorouter

This article explains the functions of eight types of autorouters and provides a check list of 26 key features that will help you compare and select routers.—John Roth, Aptos Systems Corp

High-speed video DACs drive CRTs to new performance heights

New high-speed video DACs with bandwidths to 400 MHz and color CRTs with 2048 x 2048-pixel resolution have set the stage for dramatic improvements in the quality and cost effectiveness of high-resolution graphic displays.—Paul M Brown, Honeywell Inc

Low-cost quad op amps boost circuit performance

By exploiting the spare op amps available in a quad op amp, you can boost the performance of your circuits. You can also use high-performance monolithic quad op amps to design unique circuit configurations.—Jerald G Gavenas, Burr-Brown Corp

Solid-state devices ease task of designing brushless dc motors

The solid-state devices available today make motor drive control circuitry less complex, more efficient, and more compact. With such devices, brushless dc motor drives appear more attractive as systems solution.—Daniel Artusi and Warren Schultz, Motorola Inc

Continued on page 7
The Fluke 2280B Data Logger.
Set it down,
and you've set it up.

It's designed for fast and easy set up.
The more you depend on test measurements, the more you need a Fluke 2280B Data Logger. It saves you time because it's easy to set up. You never need to write and maintain software programs. Simply enter your applications at the front panel in response to step-by-step prompts.

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The 2280B Data Logger conditions over two dozen signal types and automatically converts measurements to engineering units. You have the flexibility to run a variety of tests. All with Fluke's legendary accuracy and reliability.

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To set up a 2280B in your application, contact your local Fluke Sales Engineer. Or call 1-800-426-0361.
Your selection of a simple or complex CAE-documentation package depends on what you're going to do with it (pg 81).

**TECHNOLOGY UPDATE**

2,7 RLL controller boards and ICs extend the life of the ST506 hard-disk interface

Disk-controller board and chip manufacturers are using 2,7 RLL (run-length limited) coding to boost the capacity of small hard-disk drives that incorporate the ST506/412 disk interface.—*Steven H Leibson, Regional Editor*

μP cores let you develop customized ICs that are dedicated to your application

By employing core μPs, you can develop a processor chip that’s customized to your own requirements.—*Jim Wiegand, Associate Editor*

Electronic documentation tools blend text and graphics for CAE

Varying in sophistication from simple editing tools to complex desktop publishing systems, the latest CAE-documentation tools let you annotate your computer-generated drawings, designs, and schematics right from your CAE system.—*J D Mosley, Regional Editor*

**PRODUCT UPDATE**

CMOS DSP IC

Single-board μcontroller family

160-MIPS imaging system

**DESIGN IDEAS**

LED driver displays 8-character segments

D/A converter generates ramp waveforms

Flip-flop debounces mechanical switch

Frequency divider generates 50% duty cycle

Program converts binary to BCD code

Continued on page 9
Only Nature Routes It Better.

P-CAD'S NEW VERSION 2.0
More capacity. Lower prices.

Face it. Nobody routes as well as Mother Nature. But if you want something that comes close, you want the power and performance of P-CAD's Version 2.0 PCB Design System.

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Consider even better placement with automatic gate and component swapping. And better routing capabilities made possible by new routing algorithms; beveling for 45°; and control of routing density across layered pairs.

Naturally, there's more to our story, such as support of surface mount devices. Including components on both sides of the board and buried vias.

And there's still more big news. Like the performance to handle PCB designs of higher densities and non-standard sizes.

P-CAD's big capabilities also include improved graphics, drawing speed and text editing—all in a new system environment that's so easy to use even Mother Nature could appreciate it.

Which is why it's no surprise we're the market leader in PC-based PCB CAD. Nobody gives you this kind of performance at our prices!

So call (408) 971-1300 ext 7048 for information on the P-CAD dealers nearest you.

Once you install Version 2.0, the most complex PCB designs become second nature.
EDN September 3, 1987

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The US may be unwilling to defend Japanese interests unless Japan sheds its isolationism.

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Mentoring: A subculture success some engineering companies would like to duplicate.—Deborah Asbrand, Associate Editor

LOOKING AHEAD 315

Machine-vision market held back by myopia.

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Cahners Publishing Company.
Specialized Business and Consumer Magazines for Building & Construction
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Only Mentor Graphics has brought a billion gates to light.

In just 5 years, over a billion gates have flowed through our IDEA Series™ design automation systems. And that's a very conservative estimate.

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And so did hundreds of other companies.

Before millions of people picked Macintosh, Apple picked Motorola's M68000 Family—the brains behind one of the most successful computer products ever launched.

Now Apple has tapped the brainpower of the Motorola MC68020 microprocessor for the Macintosh II, bringing the high performance of a graphics workstation to business desktops everywhere.

72% of all 32-bit systems ever shipped included at least one MC68020. That's more than half a million high-performance systems.

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The MC68020 is not just the overwhelming choice in workstations—it is now setting new performance standards in the office—where it is essential to the computation, graphics and communication necessary for interconnected systems.

While Apple's choice of the MC68020 was a smart move, there's no license on genius: the '020 is the microprocessor of choice in advanced business system designs by such industry leaders as Altos, Alpha Micro, Casio, C.Itoh, Fujitsu, Honeywell Bull, NEC, NCR, Olivetti, Plexus, Ricoh, Sanyo, Sharp, TI, Toshiba and UNISYS.

The graphics solution.

The M68000 family helped Apple implement the visionary "point and click" graphic workstyle that has driven productivity up while driving training costs way down. Businesses of all sizes are discovering dramatic productivity increases in office computing through innovations such as desktop publishing.

The software solution.

Among programmers and designers dedicated to creating the best, most innovative applications, the M68000 architecture has been the leading choice by far—with over seven million M68000 systems installed since 1979.

Meanwhile, the MC68020, on the market now for three years, is already backed by two billion dollars worth of 32-bit software. This is more 32-bit software than all competitive products combined!

The Brain Trust: Where M68000 microprocessors predominate.

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Join the Brain Trust.

Challenge us to persuade you of the sound business and technical reasons to join the MC68020 Brain Trust. Write to us at Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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NEWS BREAKS
EDITED BY JOAN MORROW

MODULAR 1500W POWER SUPPLY OFFERS USER CONFIGURABILITY

A completely modular design concept gives designers maximum flexibility when choosing Powertec Inc's (Chatsworth, CA, (818) 882-0004) Model-6D Multimod power-supply configurations. The 1500W supply will accommodate six separate output modules, and any module may include multiple outputs. Designed with 100-kHz MOSFET switching technology, the supply meets international safety and emission standards, such as VDE, CSA, and UL. Because of the modular approach, designers can essentially choose from many off-the-shelf configurations. The company will deliver supplies in two days to four weeks if the configuration uses modules with standard output voltages. Initially, you can choose from 300W single-output modules ranging from 2 to 48V dc. The company also plans to offer multiple-output modules and modules that occupy more than one of the six plug-in spaces. All of the output modules use current-mode control techniques. A supply equipped with six single-wide output modules costs $1500.—Maury Wright

SCSI IC's HOST INTERFACE SUPPORTS 20M-BYTE/SEC DATA RATE

A 16-bit system-bus port allows the AIC-6250 SCSI controller chip from Adaptec Inc (Milpitas, CA, (408) 432-8600) to transfer data over a host µP bus at a 20M-byte/sec rate. Though this speed cannot be reflected on the SCSI side, the IC still achieves SCSI data rates of 5M bytes/sec for synchronous and 3M bytes/sec for asynchronous transfers. The extra speed on the host side of the chip prevents high-speed transfers between the system bus and the SCSI bus from soaking up a large portion of the system-bus bandwidth. The company claims that this feature allows the system bus to be free as much as 93% of the time during a SCSI transfer. The device also incorporates a separate bus that provides access to the SCSI controller's internal registers, allowing the host µP to queue up additional commands while the previous command transfers data over the system's main data bus. Packaged in a 68-lead PLCC, the part costs $20 (1000).—Steven H Leibson

LOW-COST µCs LETS YOU UPGRADE 4- AND 8-BIT APPLICATIONS

Featuring a 16-bit free-running timer, the MC68HC05C2 and MC68HC05C3 µCs from Motorola (Austin, TX, (512) 440-2035) include 2k bytes of ROM, 176 bytes of RAM, and 32 I/O lines. Suitable as direct replacements for the manufacturer's M146805 MCU, the MC68HC05C2 and -C3 come in 40-pin DIPs and feature an 8x8-bit multiply instruction. The -C3 version has a synchronous Serial Peripheral Interface and an asynchronous Serial Communication Interface. Both devices operate at 2 MHz, and you can order a 4-MHz high-speed option. They cost $3 (OEM qty).—J D Mosley

COMPANIES RUSH TO ANNOUNCE VGA-COMPATIBLE GRAPHICS ICS

Six months after IBM's announcement of the PS/2, three companies are introducing chips that emulate the PS/2 graphics hardware, the video graphics array (VGA). Paradise Systems' (South San Fransisco, CA, (415) 588-6000) PVGAI is a single-chip implementation that the company claims is fully hardware compatible with the VGA, allowing you to bypass the VGA BIOS and program the graphics register directly. The chip also offers 16 colors and an 800x600-pixel resolution (which is greater than the VGA's); monochrome mode provides a 1280x1024-pixel resolution. The PVGAI comes in a 100-pin PLCC and is priced at $60 (100).

Chips and Technologies Inc (Milpitas, CA, (408) 434-0600) has a 2-chip set comprising the 82C441 graphics controller and the bipolar 82A442 bus interface. Both are available in 100-pin PLCCs; the 2-chip set costs $40.50 (1000). The company is not
claiming hardware compatibility to the register level: you can program the hardware
directly for pixel update functions (such as moving the cursor). For other graphics
functions, such as mode initialization, you must program the hardware via the BIOS.

Finally, Tseng Laboratories (Newtown, PA, (215) 968-0502) offers the 1-chip ET3000,
which the company claims provides hardware-level compatibility with the VGA as well
as with IBM’s older graphics standard, the enhanced graphics adapter (EGA). The chip
comes in an 84-pin PLCC and costs less than $500 (OEM). All three companies say
samples are available now.—Margery S Conner

PC-BASED INSTRUMENT PROVIDES LOW-COST STIMULUS AND RESPONSE

Using the technology it developed for its microprogramming development systems,
Step Engineering (Los Gatos, CA, (408) 356-6248) created the Step Design Analyzer
(SDA), a stimulus/response instrument controlled by an IBM PC/AT or compatible com­
puter. A multioslot chassis accepts cards containing as many as 384 pattern-generation
(stimulus) outputs and 256 response inputs. The system generates test vectors and
samples responses at frequencies to 45 MHz with a 500-psec timing resolution. The
included SDA Monitor software executes on the IBM PC/AT and controls the SDA’s
operation. System prices range from $29,950 to $46,000.—Steven H Leibson

EXPERT SYSTEM REVIEWS AND IMPROVES ASIC DESIGNS

If you use the standard-cell and gate-array design environment called ViSys, you can
now obtain an option called Design Advisor from NCR Corp (Dayton, OH, (513)
445-3467), which analyzes your ASIC design and suggests improvements relating to
logic design, testability, timing analysis, cost effectiveness, and logic minimization.
Design Advisor is a menu-driven expert system with a knowledge database that encom­
passes such factors as chip timing, synchronicity, testability, performance, and I/O.
Features include a menu-driven interface, help and explanation facilities, a truth­
maintenance inference engine, and “what-if” analysis. You can analyze segments of
your circuit and retain the results to speed your analysis of the final design. Available
this fall as a dial-up service, the Design Advisor should handle most hierarchical
module analyses in a few minutes and cost from $4000. NCR also plans to offer Design
Advisor as a software option to the ViSys environment in early 1988.—J D Mosley

VENDORS ANNOUNCE BUS STANDARD FOR MODULAR TEST INSTRUMENTS

Five major instrumentation companies have jointly announced the VME Bus Exten­sion
for Instrumentation (VXIbus). The VXIbus is aimed at both the commercial and
military need for modular instrumentation with an open bus architecture. A VXIbus
system may have as many as 256 devices, including one or more VXIbus subsystems.
A VXIbus subsystem consists of a central timing module and 12 additional instrument
modules. The bus standard specifies as many as three connectors, with the P1 connec­
tor identical to the VME Bus P1. The P2 connector provides the standard 32-bit exten­sion
to the VME Bus plus a 10-MHz clock, ECL and TTL triggering, an analog summing
bus, a flexible local bus, and module identification. The P3 connector adds a 100-MHz
clock, precision module independent triggers, and an additional local bus.

The VXIbus is being submitted to the IEEE P1155 for consideration as a commercial
standard and is also being submitted to the Modular Automated Test Equipment
(MATE) Instrument-on-a-Card (IAC) subcommittee for consideration as an Air Force
standard. The VXIbus was developed by Colorado Data Systems Inc (Englewood, CO),
Hewlett-Packard Co (Palo Alto, CA), Racal Dana Instruments Inc (Irvine, CA), Tektronix
Inc (Beaverton, OR), and Wavetek Corp (San Diego, CA).—Doug Conner
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HIGH-SIDE DRIVER LIMITS INRUSH CURRENT WITHOUT GENERATING EMI

Aimed at automotive applications, the L9801 high-side driver from SGS (Agrate Brianza, Italy, TLX 330131; in the US, Phoenix, AZ, (602) 867-6100) suits 12V/6A load switching applications. Manufactured using the company's Multipower-BCD technology, the device integrates a DMOS power transistor with an R_on of 0.08Ω, and control, diagnostic, and protection circuitry on a single chip. For lamp switching, the driver limits the inrush current to 25A using a linear technique that doesn't generate EMI. The device has a TTL/CMOS-compatible control input and an open-drain diagnostic output that is activated when output short circuits, open circuits, or over-voltage conditions occur, or when the device goes into thermal shutdown. The L9801 costs approximately $1 in high volumes.—Peter Harold

RISC-BASED COLOR-GRAPHICS WORKSTATIONS SUSTAIN 10 MIPS

Whitechapel Workstations (London, UK, TLX 885300) is launching a range of Unix-based color-graphics workstations priced at less than £20,000. Incorporating MIPS Computer Systems' R2000 RISC chip set, the workstations are capable of a sustained throughput of 10 MIPS and provide 1280x1024-pixel color displays. They are supplied with the Unix 4.3bsd or Unix System V operating system and either the X-Windows or NeWS window management system. The company's Oriel window system is emulated under NeWS. Optimizing compilers are available for C, Pascal, and Fortran. Networking facilities include Ethernet/Cheapernet operating with TCP/IP and NFS protocols. An IBM PC/AT bus allows you to add expansion boards. The workstations feature 8M bytes of RAM (expandable to 40M bytes), an MS-DOS-compatible floppy-disk drive, a 95M-, 170M-, or 320M-byte hard-disk drive, and an optional 60M-byte tape cartridge.—Peter Harold

MITSUBISHI TO PRODUCE ASICs, 1M-BIT DRAMs IN US

Mitsubishi Electric Corp is pouring about ¥5 billion ($34.5 million) into its US subsidiary in North Carolina to construct a facility for the production of application-specific ICs and 1M-bit dynamic RAMs. The plant is scheduled to begin operation in April 1989 and will give Mitsubishi the distinction of being the only Japanese semiconductor manufacturer to produce an ASIC line in the US.

The company plans to manufacture 8- and 16-bit microprocessors, gate arrays, standard cells, and full custom ICs at the facility, which will have a 5600-sq-meter wafer plant, a class-10 clean room, and manufacturing equipment capable of handling devices with a 1.5-µm design rule. The ASIC operation is expected to have about 170 employees to support anticipated 1990 annual sales of approximately $50 million.—Joan Morrow

SEIKO-EPSON TO PRODUCE PERSONAL COMPUTERS IN US

Seiko-Epson has announced plans to produce its EquityIII+ 16-bit personal computer at its printer facility in Portland, OR. Production is scheduled for 4000 units per month. The company planned this move to avoid the 100% tax imposed on Japanese products by the US government. The lower-end Models II+ and I+ are made in South Korea.—Joan Morrow
Stimulate experiments with real-time analog waveforms reproduced from your actual captured data!

Connected via the GPIB interface, the Nicolet Model 4094 digital oscilloscope teamed up with the Nicolet Model 42 arbitrary function generator provides instantaneous waveform storage and generation.

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Incoming signals digitized by Nicolet’s high accuracy 12-bit, 10 MHz digitizers or high speed 8-bit digitizers allow you to see things you’ve never seen before. Zoom expansion to X256 allows you to see the details in waveforms composed of up to 16k points. Cursor readout of measurement values, continuously variable pretrigger positioning, and built-in disk drives all contribute to Nicolet’s tradition of measurement power and ease of use.

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3 KHz - 800 MHz
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from $2.95

Choose impedance ratios from 1:1 up to 36:1, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55631 requirements*). Fast risetime and low droop for pulse applications; up to 1000 M ohms (insulation resistance) and up to 1000V (dielectric withstanding voltage). Available for immediate delivery with one-year guarantee.

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*units are not CRPL listed

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  SAT (SMA) $14.95
  TAT (TNC) $12.95
  NAT (N) $15.95

Model Availability
- SAT (SMA)  CAT (BNC)  NAT (N)  TAT (TNC)
  Model no. = a series suffix and dash number of attenuation.
  Example: CAT-3 is CAT series, 3 dB attenuation

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EDN September 3, 1987
Chopper-stabilized op amps have taken a whole new direction.
Chop Amps™ from Teledyne Semiconductor keep the voltage high, the noise low and the capacitors on-chip—in singles, duals and quads.

They give you performance like you’ve never seen...because they're like no operational amplifiers you've ever seen. Completely monolithic. Linear CMOS. Chopper stabilized—with design so advanced they don't need external chopper capacitors.

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They're all backed by Teledyne's impeccable reputation for quality, service and support, earned over more than a quarter century in the semiconductor business.

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*Available in surface mount package.

The TSC915 combines high voltage (±15 V) operation with low-noise performance.
You wouldn't do this with your Analog VLSI devices.

You'll have to if you go to most ATE companies for a solution to today's sophisticated "system silicon" testing problems. Because all you'll get is a make-shift tester. And that means resigning yourself to man-months of custom hardware work integrating analog and digital instrumentation. And putting up with the long hours of low-level software development that go with custom solutions. Worse, you can expect these delays to cut your chances of getting your product to market on time.

Teradyne now has a simple answer to this complex testing problem. The A500 Analog VLSI Test System. It's the first of a new generation of systems specifically for AVLSI "system silicon" devices. A test system that can help you cut critical product development time by months or even years.

**One Test System, Once and for All**
With AVLSI devices you won't get fast design feedback, unless you test individual components—the "building blocks" of system silicon. And you won't comply with customer and industry requirements if you don't do complete "system" functional testing. With conventional test systems it means two of everything. Two testers, two test programs, two insertions, two data bases. And more than twice the time to get to market.

The A500 allows you to do it all with one system. So there's only one system to program. One insertion to make for both component and functional testing. And only one data base to work with. Which means significantly less time to market.

**Vector Bus II**: the Great Integrator
The heart of the A500 is Teradyne's unique Vector Bus II architecture. It integrates analog and digital VLSI test capability at the system level. Which means you won't have to build special applications hardware for every new device you design. Vector Bus II eliminates that costly custom-work bottleneck.
Why accept it in an Analog VLSI Test System?

with such features as TimeMaster™ Synchronization, Mixed-Signal Event Control, and MultiSource Data Mixing.

A Picture's Worth a Thousand Keystrokes
The A500 also revolutionizes program development. Our IMAGE™ (Interactive Menu-Assisted Graphics Environment) software gives you graphics programming as powerful as device designers' CAD/CAE tools. Using a mouse to control multiple windows, pop-up menus and software "power tools," you move ideas rapidly from mind to screen. And much faster to market.

Teradyne's new A500 is the only test system with the features you need to win the race for Analog VLSI market opportunities. To find out more, call Beth Sulak at (617) 482-2700, ext. 2746. Or call your nearest Teradyne sales office or write: Teradyne, Inc., 321 Harrison Avenue, Boston, MA 02118.

EDN September 3, 1987
Space exploration yields more than rocks

I respect Jon Titus's right to have the opinions expressed in EDN's June 11 editorial. But denigrating our early space-exploration results as "a pile of expensive rocks" is, in my opinion, lamentably disturbing.

A quick analogy is that we are today only in the Christopher Columbus era of space exploration. Nearly 300 years after the first Columbus sea voyage, James Cook returned from his first Pacific Ocean expedition with only a bunch of new plants and a few trinkets.

Today we have barely begun to explore the cosmos. If we lose the desire to continue, we humans will have lost the will to live. We should crawl back into the caves.

Responding to the challenges of space exploration has already stimulated discoveries and applications of science that have incalculably improved our living on earth.

We know that missile and space projects in the 1960/1970 era did not by themselves produce all semiconductor and related discoveries and applications. But missile and space projects were the essential stimulus, because immaculate guidance and control were impossible without those technologies.

So we must continue to challenge ourselves with projects whose requirements are beyond our scientific knowledge—in fact, beyond our present imaginations of the potentials of scientific discovery.

In the context of history, Columbus, Cook, et al had no vision whatsoever of America today. I predict that in 1992, 500 years after Columbus discovered America and less than 25 years after Neil Armstrong and Buzz Aldrin walked on the moon, we will have discovered space solutions for on-Earth problems such as energy generation that avoids the use of coal, oil, and nuclear materials; the disposal of garbage; and the manufacture of products based on hazardous materials.

I agree that education deserves full support. But please do not deny this nation the motivation to exist and the stimulus to discover.

Scotty Maxwell
San Pedro, CA

Mars sample return is next on space agenda

Mr Titus's editorial "Nix the Mars trip" (EDN, June 11, pg 51) raises the valid question of the cost of a Mars sample return: Is $10 billion (I think about half that is a better estimate) worth five kilograms of Mars rocks? The National Academy of Sciences says yes. It isn't just rocks, of course, but fundamental...
Sprague is the only company that makes all of the electronics for brushless DC motors. Sprague makes a wide range of brushless motor drivers: unipolar, half-bridge, full-bridge, dual full-bridge, 3-phase: some with commutation logic.

Sprague also makes Hall Effect IC sensors for use as brushless DC motor commutators. These solid state devices not only have long life but operate accurately over extended temperature ranges and survive in punishing environments. You can count on Sprague to give you the right match of power ICs and Hall Effect sensors for sensible driving of brushless DC motors. May we tell you more? Sprague Electric Company, Lexington, MA. For applications assistance, call 800/247-2077 (in Mass., 800/247-2076). For Motor Driver Brochure WR-202, Hall Effect Application Guide CN-207, and Data Sheet 29318.20 write to Technical Literature Service, Sprague Electric Company, P.O. Box 9102, Mansfield, MA 02048-9102.
Design tips to simplify actuation

Heat sink bracket improves solenoid actuator performance. See below.

These tips make solenoids more attractive than ever for designing high quality, reliable, long life actuators:

1 Specialized types. For example, Ledex offers rotary solenoids with or without axial movement, with standard life from millions to hundreds of millions cycles. Extremely high speed/high force models extend yesterday’s limits. Soft Shift™ solenoids allow precise variable speed control.

2 Controllable characteristics. Virtually every parameter can be optimized, either by selection of the right model, or by solenoid design optimization. Low cost digital controls are easily applied. For example, to maximize quiet operation a digital current ramp generator makes a Soft Shift solenoid practically noiseless.

3 Versatility unlimited. Any rotary, linear, or combination motion can be achieved using a solenoid and linkages to change stroke length or direction. For example, here are two locking mechanisms, of many. Ledex can suggest approaches, or furnish the whole package.

4 Design actuators faster. Want to develop breadboards and prototypes faster? Choose solenoids because you can get working hardware fast, by phone if you’re in a rush. Ledex stocks hundreds of types and models, and our applications staff can help you select. Compared with some actuators, solenoids are relatively low in cost.

5 Mounting cools solenoid. Solenoids can concentrate a lot of electrical energy in a small package. Plan to mount the solenoid on a heat sink, such as an aluminum plate or bracket for best performance.

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information that is to be returned. A Mars sample return has for 10 years been the recommended next major objective in US planetary exploration, because of its importance in providing the samples that will permit detailed Earth-based analysis of Mars’s history. This history is part of understanding the origin, evolution, and behavior of terrestrial planets—and in particular of our own Earth.

But exploration can never be proved valuable before it occurs. Science and exploration together advance a nation and a society. Remember when the US had a space-exploration program of which we were proud. Remember how space motivated teachers, students, educators, and writers. A hidebound outlook about exploring, while spending money on facilities and training programs without a goal, is no way to rejuvenate our society. That is why the Soviets are spending money on space exploration. If we join them, we get that benefit and two more: international cooperation and shared costs. Not bad—considering on what else government spends its money.

Louis Friedman
Executive Director
The Planetary Society
Pasadena, CA

“NASA’s $10 billion” is really ours
Although some may label Jon Titus “antiscience” for opposing a Martian exploration, none will accuse him of being antistate.

It’s not “NASA’s extra $10 billion” we’re talking about; it’s ours. In principle, it’s not inevitable that NASA would have to spend it at all. It’s only inevitable because Mr Titus and the rest of us are fully conditioned to automatically sanction the state’s spending 44% of the GNP.

But since we are thus conditioned, and since some of us think rocks at $1,000,000,000 per pound...
Hewlett-Packard's new logic analyzer family offers you something not found in other logic analyzers...
HP's new logic analyzer family gives you more of what you want in logic analyzers. For less.

So now measurements are easier to make. And high-quality HP logic analyzers are easier to buy!

You get the performance that best suits you: from 32 to 400 channels of 100 MHz transitional timing/25 MHz state, and up to 80 channels of 1 GHz timing analysis.

Our new family also offers you easy operation, powerful triggering, a CAE link, an oscilloscope, pattern generation, portability, built-in mass storage, simple probing, optional 3-year protection, and much more.

The small secret behind the big value.

To give you more for your money, HP developed a Logic-Analyzer-on-a-Chip containing a complete state analyzer, timing analyzer, and acquisition memory. This proprietary HP IC makes exceptional value possible...80 channels of 100 MHz transitional timing for only $7,800*.

You can assign state or timing in 16-channel increments. Get fully independent state, timing, state/timing, or state/state setups. Even time-correlate measurements on complex multiprocessor systems.

Operational simplicity runs in the family.

We've made our controls even easier than before, without sacrificing performance.

You can make timing or state measurements using just three menus, so you never get lost. Triggering setups, from the simple to the complex, are a snap. And autoscale gives you one-button setup for timing analysis.

You even get a color touchscreen and knob, or optional mouse with the new HP 16500A. Color lets you quickly distinguish between menu choices, measurements, and results...and find glitches more easily.

Probing made easy.

HP's new passive probes are lightweight and flexible...specially designed to grip easily and securely to your device under test. Plus, our preprocessors give you quick setups with most popular 8, 16, and 32-bit µPs, including the Motorola 68020 and Intel 80386. And if you've already invested in HP preprocessors, we offer you an easy upgrade path.

**HP 1651A: full-featured logic analyzer for only $3,900.***

With 32 channels of 100 MHz transitional timing for just $3,900*, the HP 1651A gives the hardware engineer a highly economical, yet powerful debugging tool.

It's a full-featured logic analyzer with no compromises in state and timing capabilities (25 MHz state/100 MHz transitional timing on all channels), memory depth, triggering, or I/O features. It supports most popular 8-bit µPs with full inverse assembly. Plus it's compact, weighs just 22 lbs., and has an optional carrying case for easy transport.

**HP 1650A: the new standard in general-purpose logic analysis for just $7,800.***

The HP 1650A features time-correlated state/state or timing/state operation on 80 channels. Plus eight sequence levels to meet your toughest triggering tasks. Yet it's priced below $8,000!

You get 25 MHz state/100 MHz transitional timing on all 80 channels, and preprocessor support for 8, 16, and 32-bit µPs. And, the
More value.

HP 16500A is a modular system solution, priced your way. The HP 16500A is modular, with the flexibility to meet your debug, characterization, or pass/fail test application needs today and tomorrow. You get a combination of state, timing, oscilloscope, and stimulus-response capabilities through your choice of performance modules. You can have up to 400 channels of 25 MHz state/100 MHz transitional timing. 8 channels of full-featured, simultaneous scope analysis. 80 channels of 1 GHz timing. Or 204 channels of 50 Mbit/sec stimulus. Just $12,400* buys you a basic configuration with 80 channels of 25 MHz state/100 MHz transitional timing.

You can trigger one module with another. Time-correlate measurements between modules. 400 Ms/sec scope and 1 GHz timing, for example. Even view state, timing, and analog on the same screen! Fully programmable, the HP 16500A eliminates the need for separate data storage and printer control. HP-IB and RS-232 are standard.

Now, bring real-world measurements into the CAE environment.

The HP 16500A is part of HP DesignCenter...a product development environment that unites engineers from IC design/verification to PCB design and test. By linking the HP 16500A with HP CAE, you can compare measurement results and simulated data on your workstation, and use measurement results as your simulator patterns.

Mail the card today!

For more information, fill out and mail the postage-paid reply card today. Call us direct at 1-800-752-0900. Or contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.
Excellent reliability, service, and support.

When you purchase a logic analyzer from HP, you get high reliability. The support you need to be productive with your instrument quickly. And a worldwide sales and service network to ensure your continuing satisfaction for years to come.

HP 1651A $3,900 *

The HP 1651A is a general-purpose, low-cost 32 channel logic analyzer with many features normally found on more expensive analyzers.

- 100 MHz transitional timing on all 32 channels.
- 25 MHz state on all channels.
- Support for most popular 8-bit µPs.
- Fully programmable, with built-in disc drive and hardcopy output.
- Portable and compact — weighs just 22 lbs.
- Optional 3-year protection.

HP 16500A

The HP 16500A is a modular, configurable system solution that can meet a wide variety of logic analysis, oscilloscope, and stimulus-response measurement requirements.

- Configurable through your choice of performance modules:
  - 25 MHz state/100 MHz transitional timing (80 channels per module) $5,200 *
  - 400 Ms/sec 100 MHz bandwidth digitizing oscilloscope (2 channels per module) $5,500 *
  - 1 GHz timing (16 channel master) $7,800 *
  - 50 Mbits/sec pattern generation (12/48 channels per module) $3,700/$4,000 *
  - Mainframe $7,200 *
- Color touchscreen and knob, with optional mouse.
- Intermodule triggering.
- Two built-in disc drives.
- Fully programmable, with RS-232 and HP-IB interfaces.
- Optional 3-year protection.

* U.S. list price.

Motorola 68020 is a trademark of the Motorola Corporation.
Intel 80386 is a trademark of the Intel Corporation.
are a bargain, Mr Titus should have logically suggested instead that we just make it 44.4% and have NASA spend their extra $20 billion on his ideas and theirs, too.

George Barry
President
Seven Oaks Research
Saratoga, CA

Mars trip would motivate US industry
Collecting Martian soil is the last good argument for undertaking a Mars expedition. Challenging our free-enterprise industry and its engineering professionals is much higher on the list. I personally believe this country could use a stiff, nonmilitary competition to bind us together.

Throwing money at academic facilities, teachers, and illiterates (although a good political platform) has only perpetuated the real problem —lack of motivation. Alternatively, supporting scientific endeavors has always provided an excellent return on the investment. Even the argument “We can put a man on the moon, why can't we...” is an intangible extra steering us toward excellence.

Thomas P Becker
Kenosha, WI

YOUR TURN
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CIRCLE NO 46

CALENDAR

- Designing Signal Processors with DSP and Bit-Slice Chips (short course), Palo Alto, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 29 to October 2.
- Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-II), Palo Alto, CA. Martin Freeman, Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. (408) 991-3591. October 5 to 8.
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<th>Array</th>
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<td>2856</td>
<td>68pin-180pin</td>
<td>168</td>
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<table>
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**ONE TIME PROGRAMMABLE**

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<td>TCS31001P</td>
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EDITORIAL

Increase Japan's defense role

As industry and government officials debate how to open more Japanese markets to US goods, they say little about having Japan assume more responsibility for its own defense. Japan operates as a major economic power, but it does so bolstered by the US's strong defense presence in Asia. If Japan expands its military role or increases its defense budget, its neighbors will be alarmed. This alarm has a basis in history: Even before World War II, Japan was a major Asian power. In 1905, during the Russo-Japanese War, it destroyed Russia's naval presence in Asia.

Japan can calm its southern neighbors' fears by concentrating defense efforts in the north Pacific region. This area could involve complementary US, Japanese, and Canadian activities. Obviously, this area concerns the Soviet Union, too. The USSR's only major open-ocean naval base, Petropavlosk, is just 1300 miles northeast of Tokyo.

Opening markets for semiconductors and other electronic components in Japan is a worthy goal, but so is expanding Japan's defense role in the north Pacific so that it is commensurate with the economic clout of a $2.3 trillion GNP. Although Japan's Defense Agency budget recently rose above 1% of Japan's GNP—a ceiling set by its cabinet 10 years ago—recent increases have been small. Unfortunately, the Japanese are caught between budget deficits and constitutional prohibitions on collective defense as well as being constrained by offensive capabilities. The Japanese must reconsider these limitations if they wish to keep their place in the global economy.

A greater defense role should entail more than a buildup of arms. Recently, Toshiba surreptitiously sent state-of-the art milling machines to the Soviet Union—machines that can produce submarine propellers that run quietly. So, while Japan's Self-Defense Force tries to advance antisubmarine warfare techniques, a Japanese company is indirectly helping enemy submarines evade detection. As part of an expanded defense role, the Japanese must adopt and enforce export controls that prevent a repeat of the Toshiba affair. Without a commitment to its own defense and a willingness to share the burden of defending its global neighborhood, Japan may find the US less willing to use its power to support the Japanese economy. After all, very little oil from the Persian Gulf goes to the US.

Jon Titus
Editor
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EDN September 3, 1987

CIRCLE NO 37
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We'll show you what a little quick cache can do for your business.

2,7 RLL controller boards and ICs extend the life of the ST506 hard-disk interface

Steven H. Leibson, Regional Editor

Disk-controller board and chip manufacturers are using 2,7 RLL (run-length limited) coding to boost the capacity of small hard-disk drives that incorporate the ST506/412 disk interface.

That interface, which was introduced by Seagate Technology (Scotts Valley, CA) in 1980 and is now pervasive throughout the industry, has hampered attempts to pack hundreds of megabytes into small hard disks because of its traditional 5M-bps data-transfer rate and MFM (modified FM) coding.

Boost capacity 50%

The 2,7 RLL coding that manufacturers have now begun using, however, allows a disk controller to boost the capacity of these disk drives by 50%. That's because 2.7 RLL coding is more efficient than MFM coding at converting data bits into flux transitions. However, concerns about data reliability accompany the extra capacity.

Advances in magnetic head and media technology allowed drive vendors to greatly expand track densities in their products since the introduction of the original Seagate ST506 drive, but the number of bits per track stayed fixed because the ST506/412 disk interface prevented the disk controller from delivering bits to the drive at faster rates. Some disk-drive manufacturers solve this problem by building ESDI or SCSI ports into their products. Because these higher-performance (and higher-cost) interfaces force the data separator and endec (encoder/decoder) off the disk controller and onto the drive, many of these vendors use 2,7 RLL chips in their drives to take advantage of the coding scheme's benefits.

Not a new technology

IBM introduced 2,7 RLL encoding on its 3370 disk drive for its mainframe computers in 1979, so the basic technology is hardly new. However, disk-controller manufacturers didn't apply the coding scheme to small hard-disk drives until the mid 1980s for a variety of reasons: 2,7 RLL code requires a more complex endec than does MFM code; small disk drives did not need the added capacity in their early stages of development; and the first small disk drives didn't have the bandwidth or noise margins to support the encoding scheme. With improved heads and media, however, the drive vendors started to find that the fixed bit rate and MFM encoding scheme of the ST506/412 interface were becoming the limiting factors that were making increases in drive capacity difficult to achieve.

The 2,7 RLL code simply allows a disk controller to cram more bits onto a track. It accomplishes this feat by packing an average of 1.5 data bits into each magnetic flux transition. MFM, a 1,3 RLL code, packs each data bit into one flux transition (see box, "Coding schemes for the ST506/412 disk interface"). Thus, the 2,7 RLL coding scheme achieves a 50% improvement in data storage over MFM coding for the same number of flux changes per inch (fci).

A limited number of buses

Several companies now offer 2,7 RLL disk-controller boards. Significantly, every vendor listed in Table 1 manufactures, uses, and sells ICs to perform data separation and 2,7 RLL coding. Because of the complexity of the 2,7 RLL code, endec consolidation into an IC appears to
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CIRCLE NO 39

EDN September 3, 1987
Supporting 2,7 RLL coding on the ST506/412 interface plus the ESDI disk interface, this OMTI 8627 disk controller for the IBM PC/AT bus, from Scientific Micro Systems Inc, also controls two floppy-disk drives.

be the only cost-effective approach to building the coding circuits for small hard disks. In the table, you should note that the available 2,7 RLL controller boards plug into a very limited number of buses: The IBM PC, PC/XT, and PC/AT buses and the SCSI bus are the only buses that have attracted the controller manufacturers' attention.

The SCSI controllers work on a variety of computer buses, given the appropriate host-bus-to-SCSI adapter card. But the IBM PC and compatible computer market's cost sensitivity demands a dedicated

Coding schemes for the ST506/412 disk interface

As originally conceived by Seagate Technology and implemented by various disk and controller manufacturers, the ST506/412 disk interface supported only MFM data encoding. MFM's simple coding rules, shown in Table A, encode a single bit at a time. Because this coding scheme can produce as few as one and as many as three consecutive 0s in the encoded bit stream, MFM code is also called 1,3 RLL code. Run-length-limited simply means that the code limits the distance between flux transitions. In contrast, 2,7 RLL coding accepts 2- to 4-bit groups of data bits and encodes these groups into 4- to 8-bit codes, as shown in Table B. This coding scheme allows as few as two and as many as seven consecutive 0s.

For either coding scheme, a transition between a 0 and a 1 or a 1 and a 0 in the encoded bit stream writes a flux reversal on the disk medium. Because 2,7 RLL coding allows more consecutive 0s, a disk controller can use a higher bit-transfer rate than can MFM coding and still maintain the same number of flux changes per inch. This higher transfer rate results in greater disk capacity.

However, the higher transfer rate extracts a price. Although 2,7 RLL coding does not increase the number of flux changes per inch, it does reduce the amount of time allotted to each bit. This reduction shrinks a drive's window margin from the 100-nsec specification for MFM drives to 67 nsec. Early MFM drives were too noisy to work well with 2,7 RLL controllers. If a drive has a noisy read/write channel, the noise causes pulse jitter in the data stream coming from the disk drive, and jitter eats into the window margin. Newer drive designs, particularly drives designed for 2,7 RLL controllers, have improved S/N ratios and reduced pulse jitter.
second of error” that the part might contribute. In addition, the company uses a dual-mode locking scheme for the part’s clock-generation circuitry, first using a frequency lock to generate a clock from the incoming bit stream and then using a phase lock to stay in phase with the data bits. Western Digital claims that the 2,7 RLL disk drives can trick ordinary data separators and force them out of phase by delivering asymmetrical data—hence the need for the phase-locking circuitry.

Conversely, Data Technology Corp uses what it calls a simple data-separator circuit with one type of loop filter for the PLL. Based on window-margin tests it has conducted, the company feels that its data-separation approach is just as effective in recovering a clock from a 2,7 RLL-encoded bit stream as other types of data separators are; in addition, the approach requires simpler, less expensive circuitry. Because its ICs are closely coupled, Data Technology usually sells its 2,7 RLL controller chips to OEMs as a set. Along with the set, the company provides schematics, code listings, and engineering assistance for a price that’s negotiated on a contract basis.

Scientific Micro Systems (SMS) incorporates both the 2,7 RLL data separator and endec on its $13.50 (1000) 5027 IC. The device supports two levels of write precompensation, a feature the company believes is extremely important for the higher-performance disk drives with around 1000 tracks. SMS sells a kit including the 5027, its 5055 sequencer/SCSI controller chip, and its 5080 SCSI driver/receiver for $40 (100,000). The company will supply a package including these devices, schematics, software for either a Z8 or 8051 µC, and engineering assistance on a contract basis.

Controller board and chip vendors also disagree on the amount of error-correction circuitry that 2,7 RLL drives need. Table 1 shows some controller boards using 32-bit error-correction codes (as do most MFM controllers for small hard-disk drives), some that use 48-bit ECCs, and some that use 56-bit ECCs. The size of the ECC relates to the expected defect size on the media. Because 2,7 RLL code enlarges the effective media defect size by 50%, some controller manufacturers feel that larger ECC fields are necessary.

In particular, Western Digital holds that view and presents as evidence Table 2, which compares the

<table>
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<tr>
<th>TABLE 2—PERFORMANCE COMPARISON OF 32- AND 56-BIT ECC POLYNOMIALS</th>
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<td><strong>PERFORMANCE FACTOR</strong></td>
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<td>MAXIMUM SINGLE-BURST CORRECTION</td>
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<tr>
<td>MONTH TO READ PRIOR TO MISCORRECTION (NOTE 4)</td>
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</table>

**NOTES:**
1. AT OR BETTER THAN THE INDUSTRY-ACCEPTED MISCORRECTION PROBABILITY OF 10^-5.
2. AT THE TYPICAL SINGLE-BURST CORRECTION SPAN (FIVE BITS).
3. FOR SINGLE BURSTS, FIVE BITS LONG
4. AT 10M bps

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error-detection and -correction performance of 32- and 56-bit ECC polynomials. Table 2 clearly shows the advantage of the longer ECC.

However, Data Technology holds the opposing view, apparent in its use of 32-bit ECC fields for its 2,7 RLL controllers. The company believes that its surface-scanning technique will catch and lock out (by means of a defect map) bad sectors —those with hard errors—leaving mostly soft errors to correct during drive operation. Because re-reading a sector containing a soft error usually eliminates the problem and is faster and less costly than correcting bad data, a 32-bit ECC scheme is more than adequate, the company says. Meanwhile, Scientific Micro Systems takes a middle-of-the-road approach by using a 48-bit ECC field.

Clearly, 2,7 RLL controller vendors do not share unified philosophies for controller designs. Because each vendor targets its products for particular markets (for example, those that are cost sensitive or performance sensitive), you should decide what controller characteristics are most important for your application and select the controller or chip set that best matches your needs.

Once you have selected a 2,7 RLL controller, you face the selection of a drive and the task of integrating the two components. Even though 2,7 RLL coding does not increase the required bandwidth for a disk drive, not every hard disk with an ST506/412 interface will support the coding scheme.

Although the fei remain constant, 2,7 RLL controllers supply data to a drive at a 7.5M-bps data rate (2,7 RLL's bit rate is 50% higher than MFM's), so the drive's read/write channel must support higher-frequency signals. 2,7 RLL coding allows more consecutive 0's, so the drive's read/write channel must support lower-frequency signals as well. Because drive manufacturers tune a drive's read/write channel response for an expected signal, MFM drives generally aren't good candidates for 2,7 RLL subsystems, although some drives with extra bandwidth will work well. (Some advertisements for 2,7 RLL controllers don't make this point very clear.)

Bad matches give poor results

In fact, as drive vendors rode the learning curve and improved their products, controller manufacturers noticed that the newer disk drives had bandwidth to spare. This series of events led directly to the creation of 2,7 RLL controllers to take advantage of that extra bandwidth. Unfortunately, drive manufacturers still held manufacturing tolerances to MFM specifications, so 2,7 RLL compatibility for a particular disk drive could change from lot to lot.

The results of using 2,7 RLL coding on drives not certified for 2,7 RLL operation gave the technology a black eye. Sometimes, the mated controller and drive failed to work at all, while other times, the married couple decided to divorce a few months after the system went into operation, resulting in catastrophic data loss. According to Carter O'Brien, director of marketing at Seagate Technology, drive manufacturers now offer disk drives certified as 2,7 RLL compatible, and controller manufacturers have improved data separators to the point that you should not experience problems if you stay with newer products.

Priam took a different approach to solving the problem of system integration. The company offers matched sets of 2,7 RLL controllers...
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As one of the major proponents of an extended 2,7 RLL (ERLL) disk-interface specification, Maynard Electronics offers this ERLL controller board bundled with matched, internally mounted or external hard-disk drives.

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IBM PC/AT bus but do not support 16-bit bus transfers. The company claims that the PS180 works with MFM-rated drives and that the PS200 works with 2,7 RLL-rated drives. Although the company has approved several drive vendors’ products and sells some drives for operation with its controllers, it apparently does not offer matched sets, so you would have the responsibility for the subsystem integration.

All of these augmented 2,7 RLL schemes share a common problem: They are attempting to run disk drives and interfaces far beyond the products’ original design limits. That these companies have any success at all in integrating their products with standard disk drives is a tribute to the window margins in today’s small disk drives.

However, the drive and controller vendors may change that situation. At an ERLL symposium held on March 27, 1987, and sponsored by Maynard Electronics, drive and controller vendors met to discuss the future of a high-speed, 2,7-RLL interface specification. The only consensus reached at that meeting was for a 10M-bps ERLL data rate. However, if future meetings produce an ERLL specification, the interface could join ESDI and SCSI in a troika of high-performance interfaces for small hard-disk drives and controllers.

References

Article Interest Quotient (Circle One)
High 518 Medium 519 Low 520

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The L6114 is just one of a whole range of ICs based on SGS’ Multipower-BCD™ technology. This unique smart power technology is bringing you a whole new generation of devices with improved performance levels and application potential.

<table>
<thead>
<tr>
<th>Absolute Maximum Ratings</th>
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<tbody>
<tr>
<td>Vdss max</td>
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<tr>
<td>Iout max</td>
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<tr>
<td></td>
</tr>
<tr>
<td>Ron</td>
</tr>
<tr>
<td>Fswitch</td>
</tr>
<tr>
<td>Package</td>
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</table>
SGS' exclusive Multipower-BCD technology—that's integrated Bipolar, CMOS, DMOS—has a lot more to offer. What other smart power IC technology isolates the DMOS output power transistors to let you connect as many as you need on a chip in any way you like? None.

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### Video MUX/Amp Combos

<table>
<thead>
<tr>
<th>Model</th>
<th>Channels</th>
<th>Frequency</th>
<th>Voltage</th>
<th>Price</th>
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### Video Amplifiers/Buffers

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### Video Switches

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### Video Multiplexers

<table>
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<th>Channels</th>
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<td>MAX310</td>
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<td>76dB</td>
<td>$8.00</td>
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<td>MAX311</td>
<td>2 of 8, Differential</td>
<td>76dB</td>
<td>8.00</td>
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<tr>
<td>MAX312</td>
<td>Latched, 1 of 8, 84dB</td>
<td>10.00</td>
<td></td>
</tr>
<tr>
<td>MAX313</td>
<td>Latched, 2 of 8, 84dB</td>
<td>10.00</td>
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(Prices are for 100-up quantities)

Multiplex ±2V into a 75Ω load.

Buffering the output of a MAX310 with a MAX450 eliminates switch insertion loss. It also enables you to drive ±4V into a back-terminated 75 ohm load or signals up to ±8V with lower loads. All these applications feature low differential phase and gain error. This is only one example of how Maxim's video ICs can suit your needs.

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µP cores let you develop customized ICs that are dedicated to your application

Jim Wiegand, Associate Editor

By employing core µPs, you can develop a processor chip that’s customized to your own requirements. In contrast, a standard µP might provide more I/O than you need but not enough timers—a situation that would force you to include extra timer ICs in your board-level design. However, the core approach would let you substitute extra timers for the standard part’s superfluous I/O.

Production costs

When estimating the savings that core µPs can deliver, keep in mind that the true cost of production must include the cost of testing your products. Board-level tests now contribute as much as 50% to the cost of production of an electronics board, and even if you could populate your board with free samples, you wouldn’t escape the significant test costs.

By incorporating more functionality into a single IC you can reduce your total expenses, even if the single IC costs more than the combined prices of the standard parts it replaces. Not only are board fabrication costs lower, but test costs are as well: With the core-based design the test cost is included in the IC cost.

In addition to the reduced test costs associated with core-based design, the technique improves system reliability. The dominant mode of failure in electronic systems is in the interconnection of the electronic components, and when you eliminate interconnections, you improve reliability. A related factor favoring core-based designs is low cost of repair: A small improvement in reliability due to reduced interconnection will be reflected in significant maintenance-cost reduction. A single service call, even if it results in nothing more than a board swap, can easily cost $100 or more.

Another advantage to core-based design is performance improvement. If, for example, you can incorporate all the memory your design requires on a single chip, then you can eliminate all the wait states that interfacing to slower, off-chip memory would have made necessary.

Space savings is, of course, a significant advantage to the core-based approach. In military and automotive applications—and any applications requiring portability—space savings may be the primary consideration, and indeed, these applications have utilized cores to the greatest extent so far. The high volumes involved in automotive applications also make it easy to justify the NRE costs involved in the development of a core-based design.

Cores available from various manufacturers run the gamut of µP technology. They include conventional complex-instruction-set µPs, military processors, and RISC cores.

Typical of the conventional µP cores is the COP800 core, developed jointly by National Semiconductor and Sierra Semiconductor. Although the COP800 offers a streamlined instruction set—it has only 44 instructions in its repertoire—the core's architecture is not a reduced-instruction-set one. The load-and-store interface to memory and extensive use of registers characteristic of RISC operation are not found in this core.

Size is important

What you do find is the smallest 8-bit core cell in the industry—4000 mil², excluding optional on-core memory; as much as 8k bytes of optional ROM; as much as 192 bytes of RAM; a 16-bit timer; and as many as 160 I/O ports. The chip allows you to access as much as 32k bytes of off-chip RAM through the use of bank switching. The core also includes a Microwire interface. (Microwire is a synchronous serial communications system that can operate at rates to 1M bps.)

For applications that require nonvolatile storage of acquired data, you can add as much as 8k bytes of

<table>
<thead>
<tr>
<th>CORE µP AVAILABILITY</th>
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<tr>
<td></td>
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<tr>
<td>80C51</td>
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<tr>
<td>GE/RCA</td>
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<td>INTEL</td>
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<td>LSI LOGIC</td>
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<tr>
<td>VLSI TECHNOLOGY</td>
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<td>ZYMOS</td>
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Rockwell's R144HD, a V.33 half-duplex modem for the public telephone network, offers 14.4 Kbps operation in facsimile and other imaging equipment, and also communicates at 1200, 9600, 7200, 4800, 2400 and 300 bps. It can transmit a page in less than 10 seconds, significantly lowering transmission costs. It's optimized for use in Group 3 facsimile machines and is compatible with Group 2. It's small (13" square), low powered (2.5 W typical), and has a serial/parallel host interface and standard connector for a simple design in small spaces. It also has Automatic Adaptive Equalization algorithms, permitting virtually error-free transmission over poor phone lines.

Rockwell's R144DP is a V.33 and V.29 compatible modem that permits high-speed transmission over all types of telephone lines by modems, multiplexers and network control equipment. Production quantities will be available in October.

It's VLSI-based design permits all necessary circuitry to be contained in less than 19 square inches, with automatic speed recognition and Automatic Adaptive Equalization.

And both, like all Rockwell standard modems, feature a five-year warranty ensuring reliability.
TECHNOLOGY UPDATE

EEPROM on the chip. This on-chip EEPROM is especially useful in low-power applications. You can acquire data, store it in EEPROM, and power down until the information is required. You can include EEPROM control circuits and a high-voltage generator on the chip so that you can operate it from one 2.5 to 6.0V supply.

Other peripheral cells available include a 32-segment-LCD controller/driver, an LED display driver, a UART, a keyboard encoder, a watchdog timer, a 10-bit DAC, and a 10-bit ADC.

There are some differences between the ASIC core implementation of the part and the COP820C standard product from National Semiconductor with which it's compatible. The core makes 64 signals, including the internal data bus, available at the interface to your surrounding logic; the standard product makes only 28 signals available. The presence of the core's extra signals illustrates another of the strengths of core-based design: You can overcome pinout and packaging restrictions when you incorporate your design on a single IC.

In addition, the core doesn't include the standard part's ports L, D, and I. You can, however, use a port macrofunction to generate as many as 160 I/O ports. An extra interrupt pin has been added to the core, the Halt signal has been brought out so that you can power down your logic simultaneously with a µP Halt, and a bank-enable pin has been added to the RAM decoder to allow you to bank-switch RAM in case you need to use more than 192 bytes of RAM.

The proper tools

As with any µP project, you will be concerned with the availability of development tools for the core-based design. Sierra provides an interface board that you plug into the COP8 socket of National Semiconductor's Mole (microcontroller on-line emulator) development system. You can also obtain from Sierra a bonded-out version of the core itself. You can use this core on your own prototype board for development, or you can use it in conjunction with the Mole, which provides you with breakpoint and trace capabilities.

An application area where space savings is typically at a premium is the military area. MIL-STD-1750A delineates an instruction set architecture (ISA) that's implemented by LSI Logic's L64500 chip. This MIL-STD-1750A µP is available as a core that you can surround with as many as 18,000 gates. If you wish to use LSI Logic's Compacted Array—a channel-free, sea-of-transistors type of gate array—to surround the core, then you can pack in as many as 36,000 gates along with the core.

The L64500 is a 16-bit µP geared to military real-time-processing applications. The µP's ALU is expandable to 32-bit operation, and it operates at 25 MHz over the military temperature range. A and B timers are available as on-chip options.

The L64500 is available from LSI Logic's Gigacell library, and development of the chip is therefore supported on the LSI Logic's LDS (Logic Development System). The LDS has been expanded to include, among other features, floor planning, multichip simulation, fault grading, and timing analysis. Together, these functions constitute the MDE (Modular Design Environment). The MDE allows you to design and simulate the core and peripheral circuits simultaneously.

Besides the fact that you can integrate memory and peripheral logic with the 1750 core, you may be able to integrate a dual-redundant 1750 system—including voter circuitry, which makes certain that both cores agree—on a single chip. The motivation for this design approach is, of course, reliability, something of great interest to military designers.

As is often the case in ASIC de-
signs, however, pin count could be the restricting factor when you try to achieve this level of integration in an IC. You may have to multiplex data and address buses or other signals in order to reduce the pin count to a practical level. In addition to high integration levels, some designers are using the 1750 core to implement the basic requirements of the 1750 specification along with the circuitry to realize extra user-defined instructions.

A part that has found a great deal of popularity in the commercial area is Intel's 8051 microcontroller. The 8051's combination of hardware functionality has made it one of the most popular microcontrollers available. However, some of the features that make it a popular choice for microcontroller design might limit its flexibility in a core-based design. For this reason, Intel has brought some of the internal signals from the core's center to the edge. The company terms this collection of signals the special-function register (SFR). Fig 1 illustrates the SFR's effect on program execution.

Software compatibility

As you can see from Fig 1, the core implementation will not be identical to a standard-product implementation. You gain performance, but you lose 100% software compatibility. If you want to take an existing standard-product design and cast it into silicon using an 8051 core, you will have to modify your existing software to take into account changes in the instruction set, such as those illustrated in Fig 1.

Along with software compatibility, core size is an important consideration in the selection of a µP core. But core size is by no means the only criterion on which to judge a µP core. The availability of development tools, the number of support peripherals in the cell library, and the appropriateness of the core itself for your application are primary concerns. But core size will have an impact on your design, limiting the amount of circuitry that you can practically place around the core.

For example, Motorola has extracted from its 6805 standard-product line a 6805 core that measures 90 x 97 mils, one of the smaller cores available. A 4k x 8-bit ROM consumes 127 x 103 mils using the same 2-µm process, and a 256 x 8-bit RAM uses 75 x 40 mils. If you choose to use a chip which is 292 mils on a side, then you would have 31,185 mil² left over after you place the core and memory. This remaining area would allow you to include about 5000 gates of support logic in addition to the aforementioned components. Motorola offers (at greater cost, of course) chips with dimensions of 400 mils on a side in the company's 2-µm process. Fig 2 illustrates the difference between a standard product and a core-based 6805 implementation.

The priority that you should attach to compatibility between your core-based design and a standard-product design depends on your application. If you are merely consolidating an existing design, then you will assign a high priority to software compatibility. If, on the other hand, your design is from scratch, then you may want to deviate from the standard-product instruction set.

RISC core

RISC-based designs have received a lot of attention lately, and VLSI Technology Inc has devoted enough attention to the concept to provide you with a RISC-based core for ASIC development. The company's 32-bit RISC processor, the VL86C010, has a complement of 46 instructions. In keeping with the tenets of RISC methodology, the processor is implemented as a single-cycle execution unit and a load-and-store memory interface: an interface for which the only operations that the processor uses for memory reference are the load operation and store operation; all other manipulations are carried out on registers. There is one operation that requires more than one clock cycle to execute: the multiplication operation. The operation is a 32 x 32-bit multiply that yields a 32-bit result in, at worst, 16 clock cycles.

The processor also performs load and store-N operations. This capability allows you to transfer large blocks of memory and to rapidly save machine states to accommodate context switches. For instructions that transfer more than one register, the first register is transferred in four machine cycles, and subsequent registers require one machine cycle to complete the transfer.
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For development support, the VL86RDPC software development board is available from VLSI Technology Inc. This development-system module plugs into an IBM PC and supports C, Fortran 77, Prolog, Lisp, and Basic.

In the case of the VL86C010, backwards software compatibility is obviously not an issue. In fact, Jim Miller, VP of marketing and sales at VLSI Technology, says that the company is finding more customers who want to deviate from, rather than maintain strict compatibility with, standard µPs. He says that customers have their own unique set of demands and that core-based design is the way for them to produce an IC that best suits their needs.

The plethora of cores available today indicates a strong investment in this design methodology. More players are becoming involved all the time. Intel and Texas Instruments recently announced an agreement whereby Texas Instruments will obtain access to Intel's µPs for use in TI's ASIC designs and whereby Intel will have access to TI's ASIC cells.

In addition, Harris (Melbourne, FL) is developing a RISC processor core named the Fort plus optimized RISC Computing engine (Force). This Machine directly executes Fort, a high-level language optimized for real-time control applications. This core is scheduled for integration into Harris's cell library by the first quarter of 1988. At that time the Force may be with you.

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Electronic documentation tools blend text and graphics for CAE

J D Mosley, Regional Editor

Varying in sophistication from simple editing tools to complex desktop publishing systems, the latest CAE documentation tools let you annotate your computer-generated drawings, designs, and schematics right from your CAE system. These new packages run on CAE workstations or desktop computers. Their electronic cut-and-paste functions allow you to develop documents from CAE programs that you could previously use only for creating schematics.

How simple or complex a documentation package you require depends ultimately on what you're going to do with it. A simple package will usually suffice for documents that will be circulated internally, but to produce brochures, spec sheets, proposals, and manuals that need a professional appearance, you'll probably require a more sophisticated system.

You also need to consider the program's ease of use and its user interface. Some documentation programs require you to exit your CAE program before you can call up document functions. Other packages are easier to use—they let you pop up a documentation window without having to leave your drawing routine. Further, unless the user interface between your CAE program and your documentation program is simple to learn and use, you'll have to spend a lot of time learning to use the commands. You'll probably want a program whose commands are similar to those of other programs that you're already familiar with.

Some documentation programs include menus or icons that can shorten the time you spend learning to use them. Remember, however, that once you become proficient in the use of the program, the menus may become a hindrance by slowing your performance or by preventing you from developing customized functions.

Time can also be a consideration in your choice of a documentation package. If you share a CAE workstation with other engineers, you may not have the time to become familiar with the program and then use it to compose text. The recent price reductions in the workstation market may solve that problem, however—soon, the price of a workstation will no longer prohibit companies from purchasing one for each designer. For example, DEC dropped the price of its diskless VAXstation 2000 from $10,500 to $5400, and Sun's 3/50M workstation now sells for $4995. And the price/performance ratio of IBM PC/AT clones continues to improve, especially since the latest announcements of the 80386-based computers. It isn't uncommon to find PC/AT-compatible computers selling for $2000 or less.

Also consider whether you need color documentation. Although some CAE applications, such as a single-sided pc-board layout, don't necessarily require color, it's almost impossible to follow traces and vias in a complex chip design or a multilayer double-sided board design without the use of color output.

If you require color, you may also require a new printer—printers and plotters that are suitable for CAE can't always handle documentation. Color plotters and dot-matrix printers can't provide sufficiently fine resolution for professional-quality documentation, and color laser printers are still in

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The drawing shown below was produced on the HP DraftMaster with AutoCAD software.
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the development stage.

Color ink-jet printers such as the $1395 Paintjet from Hewlett-Packard, however, can handle documentation needs. Paintjet produces near-letter-quality text at speeds as fast as 167 cps and graphics at resolutions reaching 180 dpi. A color thermal printer, such as the 300-dpi model that QMS Corp recently demonstrated at Comdex/Spring in Atlanta, is also an option. The company plans to introduce the machine in the fourth quarter of 1987. The printer can produce 4-color output on 11 x 17-in. coated stock. Its price will probably fall between $15,000 and $25,000.

Integrated tools speed editing

If you want to annotate your work but are content to leave sophisticated page-layout tasks to a technical-publishing staff, consider Viewlogic’s Workview software. The package runs on the IBM PC/XT and compatible computers. It consists of integrated modules that provide a uniform user interface for a variety of engineering functions, including basic documentation functions.

The Workview modules include the Viewdraw schematic-entry and graphics-editing tool, a Spice simulation module, the Viewterm terminal-emulation tool, the Viewmail electronic-mail (Ethernet) module, the Viewmouse mouse interface, the Viewtext word-processing module, the Viewsys DOS system window, and a number of other modules and utilities. An entry-level Workview system starts at $5000 and ranges to $14,000, depending on the number of modules and features you choose.

Viewdoc, the document-processing module, lets you merge text and graphics in a straightforward manner. You first call up Viewdoc and type in some text. Then you open a window containing a drawing, put the drawing into the system’s Cut buffer, place the cursor at the bottom of the graphics area in the text (on the main screen), and execute the “area insert” command, which merges the drawing with the text. Viewdoc doesn’t let you mix text and graphics on a single line, and it doesn’t allow you to edit your drawings inserted in the text; you must edit drawings in a Viewdraw window before merging them with the text.

Viewdoc limits you to three fonts: Tiny, Small, and Medium. Only the Small and Medium fonts support bold and underline printing. You can’t format your text in columnar form, but by using Viewmail, you can port your cursory engineering documentation to your company’s technical-publishing staff.

Revision control

Mentor Graphics also incorporates a word processor and text formatter in every CAE package it sells. The text formatter, Doc, uses icons and pop-up menus to simplify the document-definition process. PicEd, the optional picture editor, lets you create graphics and charts. You can also import engineering graphics generated with any manufacturer’s CAE tools.

Doc also lets you physically partition a single document among multiple Apollo workstations so that multiple authors or editors can participate in the documentation process. To avoid a breakdown in communications among these editors, and to maintain consistency within the document, Doc and PicEd tap directly into the relational-database-management system (DBMS) that is the keystone of the Mentor Graphics CAE system. Every phase of the design cycle—from design capture and simulation to physical layout, testing, and document preparation—uses tools that share this common database.

As a result, Doc provides a means of managing the documentation procedure—a unique feature in a document-processing package. With the aid of the DBMS, Doc facilitates the communication and control of changes as they occur in a document and as they relate to changes in the design of the actual schematic.

Using Doc’s graphics-by-reference feature, one or more documents can call out a single drawing in one or more locations, and any changes relating to that drawing will be updated automatically in
TECHNOLOGY UPDATE

each of those documents. Because it eliminates the need for multiple copies of the same drawing, this technique also lets you store graphics efficiently on disk.

Doc's level of control lets you maintain what amounts to an audit trail for changes made to a given document. You can track insertions and deletions to the character level, chart the impact of a proposed design change, or freeze and archive a specific version of a document. You can even determine when and by whom each change was made, modified, or frozen. This level of control helps to streamline the review and approval cycle for changes made during the design cycle. Mentor Graphics' Design Station, including Doc, starts at $20,400.

**Doc control for a CAE system**

You can take advantage of Doc's capabilities even if you don't purchase a Mentor Graphics CAE workstation. The Doc software is available from Context Corp in a number of configurations. For $4900, you can purchase a software program called Engineering Writer, which gives you a version of Doc that's specifically suited to electrical-engineering uses. For $4000 more you can add PicEd to the software package. Alternatively, you can spend $8900 for Engineering Writer, a 32-bit Apollo DN3000 workstation with 4M bytes of RAM and a 15-in. monochrome monitor.

If you prefer a 19-in. color monitor and a full-featured version of Doc that can produce complex documents in a technical-publishing environment, consider the $28,900 Context Editor, which includes an Apollo workstation and PicEd. For an additional $3000, you can up-
Choosing the right PCB design solution can be a challenge. Especially when you consider that today's dense, multilayer designs combine digital and analog technologies with both through-hole and surface-mount packages.

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grade the Context Editor to run your C and Pascal programs. Each of the Context systems includes an electronic-mail facility.

In its Distributed Publishing (DP) System, Intergraph Corp uses an object-oriented software environment to create relationships among document components. The package lets you dynamically specify the ways that the various parts of a document relate to each other—for example, you can specify that section headings appear both in the text and in the table of contents. Because the software assumes some of the document-organization chores, it's fairly easy to use. The package runs on the company's electronic-design engineering workstations, which are based on Fairchild's 32-bit, 5-MIPS Clipper CPU chip and a VAX host processor.

The DP System comprises two products: DP/Publisher and DP/Presenter. DP/Publisher continuously displays an 8½×11-in. window, a structural-editor window, and an icon-driven menu panel. The program provides styling templates that you can use to fine-tune your document's appearance by specifying parameters such as word and letter spacing, fonts, headers and footers, the placement of captions under figures, text color, and justification. What's more, you don't need to remember programming codes or commands. The program provides graphics representations of sliding switches, buttons, and toggles; you make your selections with a mouse.

The 8½×11-in. window provides a WYSIWYG (what you see is what you get) display of each page. An alternative to using the WYSIWYG mode is to use the Structural Editor to edit and rearrange the components of your document. The Notes facility lets you make brief notations in your text for review on the screen.

DP/Publisher can emulate a number of popular word-processing programs, such as WordStar and DEC's MASS-11, so you can create text without leaving the DP System. It also gives you access to an on-line thesaurus, an interactive and a batch spelling checker, and a revision-tracking facility. By means of the Initial Graphics Exchange Specification (IGES), you can import graphics from CAE systems from Intergraph and other companies. DP/Publisher also lets you produce hard copy with any laser printer or typesetter that uses the PostScript page-description language.

The other member of the DP System, DP/Presenter, lets you produce business graphics from spreadsheet information. Thus, it lets you interactively generate an assortment of bar graphs, scattergrams, pie charts, and line graphs from data generated by programs such as Lotus 1-2-3.

The DP System links an individual author's personal document database to a shared collective database residing on a VAX or MicroVAX host. Such document sharing isn't an automatic feature; it occurs only at the author's option. However, this approach does provide a way of distributing and partitioning documentation among the members of a design or engineering-support group.

**Desktop publishing for PCs**

Stand-alone PC-based desktop publishing programs are suitable for generating documents that will circulate outside your company. As an EE, however, you may not be particularly concerned with fonts, columns, and interparagraph spacing, so unless you are personally responsible for generating documents for outside use, you may find these publishing packages too sophisticated for your needs.

Before you can use one of these dedicated desktop publishing packages, you need to spend a lot of time learning the system. What's more, such packages aren't primarily intended for generating text, so they usually have only rudimentary text editors. These programs, such as Ventura Publisher Edition from Xerox Corp, let you lay out a printed page by importing text and graphics previously generated with other programs.
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To use Ventura Publisher Edition to provide extensive documentation for an AutoCad design, for example, you would generate a text file by using a word-processing program such as WordStar or Microsoft Word; load Ventura Publisher; define the document’s format; import the AutoCad file containing the design; import the text file; and use Ventura Publisher to crop, resize, and relocate your design, and then to cut, copy, and paste the associated text. Ventura Publisher also lets you change character fonts and print attributes, and it is compatible with any of 20 different printers, including color ink-jet, dot-matrix, laser, and typesetting printers. The program runs on IBM PCs and compatible computers.

Ventura Publisher requires you to define the layout rules for your document; it automatically applies those rules to the text and graphics you combine on any given page. Thus, the system can retain company-wide standards for proposals and contracts, and can afford to pay $15,000 for a turnkey system from Interleaf that includes a VAX-station 2000 and an Interleaf Cx laser printer for $29,900.

Workstation programs ease task

If, instead of a PC, you have a DEC, Apollo, or Sun workstation and can afford to pay $15,000 for Interleaf’s Technical Publishing Software (TPS) version 3.0, you can become a proficient desktop publisher in a matter of hours. TPS features mouse-selectable icons and pull-down menus that make the program easy to use and don’t require extensive training. Thus, you can concentrate on your page layout rather than on which command to execute next. If you don’t happen to have a spare workstation at hand, you can purchase a turnkey system from Interleaf that includes a VAX-station 2000 and an Interleaf Cx laser printer for $29,900.

The TPS display, on a 19-in. monitor, provides a full-page view of a document on one side of the screen, an assortment of icons on the other side, and boxes along the top of the screen that identify pull-down menu trees. You can compose text while running TPS; the software continuously updates the display so that a printout at any instant exactly matches the image on the screen—in other words, it’s a WYSIWYG display.

TPS also lets you import ASCII files, text files generated by several popular word processors (including Wang and WordStar), graphics produced on Apple’s Macintosh PC, HPGL-format graphics, IGES-format graphics, Calcomp CAD-format files, and scanned images. You can also create sketches using the mouse, standard graphics primitives, and clip-art symbols. TPS comes with 10 standard typefaces in a variety of point sizes.
STEP UP IN PERFORMANCE, DOWN IN SIZE.

Motorola VCXO's Offer a Space Saving Dimension in System Design

Motorola VCXO's not only deliver the reliability and stability your applications demand...they also provide space saving dimensions for greater design flexibility! Hybrid and I.C. component technologies give the Motorola VCXO a space saving size of just 0.820" x 0.520" with a 0.355" seated height. Motorola's new VCXO occupies only .426 in.² of board space compared with some competitive offerings of 2.25 in.² or .714 in.².

Superior Deviation/Stability Performance

Motorola voltage controlled crystal oscillators are another example of Motorola high performance in a smaller, more efficient design. Motorola VCXO's offer a wide frequency range of 3 to 24 MHz featuring superior frequency stability and deviation sensitivity. Our VCXO's maintain a frequency stability of ±0.0025 percent throughout a wide range of conditions: operating temperatures of 0° to +70°C; varying input voltage and load changes; aging; shock; vibration and more. Deviation of ±100 ppm is achieved over a voltage range of 0.5 Vdc to 4.5 Vdc. Wider deviation is optionally available.

Inherent Reliability

Motorola's custom integrated circuit minimizes the number of components, resulting in a VCXO that offers outstanding reliability and consistency from unit to unit. The double hermetic seal with class 100 clean room processing enhances reliability.

Phase-Lock Loop Applications

VCXO's are predominantly used in all phase lock loop applications for communications equipment and analog/digital interface as well as in LAN's and other forms of computer-shared management systems. For phase lock loop applications, Motorola offers a wide variety of reference oscillators to fill your system needs.

Contact us for complete information and samples at the following address: Motorola Inc. - Components Division, 2553 North Edgington Street, Franklin Park, IL 60131. Phone: (312) 451-1000 EXT. 4835. TWX: (910) 255-4619, FAX: (312) 451-7585, TELEX 499-0104.
TECHNOLOGY UPDATE

WHAT'S NEW IN VME PACKAGING

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sub-rack. Plug in your cards and go.

First Vectorboard
Now VMEbus

document-processing features that
Interleaf's TPS provides, and it
adds a few nice touches such as an
on-line help facility and a programmable,
batch list-extraction program for generating indexes and
lists across multiple documents. In addition, Frame Maker's object-oriented core maintains the relationship among elements in your document, so you can add text to page 1
of a 100-page document without manually reformatting the entire
document. You can obtain a free
demonstration copy of the product
by sending a blank ½-in. cartridge
tape to the company.

The design as documentation
Although document processing
now seems to be the last word in
CAE documentation, at least one
company has begun a quiet revolu-
tion by advocating the use of a pic-
torial programming language called
Input/Output Requirements Lan-
guage (IORL). Teledyne Brown En-
gineering's Tags (Technology for
the Automated Generation of Sys-
tems) automates the entire process
of developing and documenting
hardware and software designs.
Tags uses IORL symbols to depict
components, interfaces, and pro-
cesses, thus providing a graphic de-
scription of all the input and output
requirements for a particular sys-
tem. In much the same way that a
flowchart illustrates the logical pro-
gression of processing functions, an
IORL-based design imparts the
functional organization of a system
of elements.

Unlike flowcharts, however, IORL symbols don't have to be
translated into machine-readable
form, because IORL is a design and
system-requirements language that
combines system specification, de-
sign, and documentation as a unified
process. In effect, the graphic de-
sign is also your engineering docu-
mentation. IORL defines all data
types and values, specifies timing
constraints, and illustrates parallel
and concurrent logic.

You can use a simulation compiler
to automatically produce an execut-
able discrete-event simulation of
your IORL design in Ada source
code. Then you can use an Ada
compiler to generate executable ma-
chine code. Teledyne Brown expects
to release an Ada code generator for
IORL late this year. The company
also offers a document processor
that generates standard-form engi-
neering documents from IORL that
meet DoD and NASA specifications.

Running on a $9900 Apollo Do-
main desktop workstation, Tags
sells for $28,750 per single-station
license. The company plans to offer
a Tags upgrade in 1988 that will
provide a VHDL hardware-design
language (VHDL) and an interface
from VHDL to a variety of CAD/
CAM tools.

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(Circle One)
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EDN September 3, 1987 CIRCLE NO 74
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- performance from 0.9ns

**GATE ARRAY PRODUCTS**

**TSGB SERIES** (2µ) **TSGC SERIES** (1.2µ/2µ) with 1K-10K densities

<table>
<thead>
<tr>
<th>TSGB/GC No.</th>
<th>No. Gates</th>
<th>No. I/O</th>
<th>PWR</th>
<th>DIP Package</th>
<th>Pin Grid Arrays</th>
<th>Chip Carriers</th>
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<tbody>
<tr>
<td>01000</td>
<td>1120</td>
<td>56</td>
<td>12</td>
<td>28, 40, 48 (C/P)</td>
<td>68 (C/P)</td>
<td>44, 52, 68 (C/P)</td>
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<tr>
<td>02000</td>
<td>2128</td>
<td>76</td>
<td>12</td>
<td>28, 40, 48 (C/P)</td>
<td>68, 84 (C/P)</td>
<td>44, 51, 68 (C/P) 84 (C)</td>
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<tr>
<td>03000</td>
<td>3264</td>
<td>96</td>
<td>12</td>
<td></td>
<td>68, 84, 100 (C/P)</td>
<td>68, 84 (C/P) 100 (C)</td>
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<tr>
<td>04000</td>
<td>4256</td>
<td>108</td>
<td>12</td>
<td></td>
<td>68, 84, 100, 120 (C/P)</td>
<td>68, 84, 100 (C/P) 100, 124 (C)</td>
</tr>
<tr>
<td>06000</td>
<td>5880</td>
<td>132</td>
<td>12</td>
<td></td>
<td>68, 84, 100, 120 (C/P)</td>
<td>68, 84 (C/P)</td>
</tr>
<tr>
<td>08000</td>
<td>7872</td>
<td>168</td>
<td>16</td>
<td></td>
<td>144 (C)</td>
<td>100, 124 (C)</td>
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<tr>
<td>10000</td>
<td>9776</td>
<td>192</td>
<td>16</td>
<td></td>
<td>84, 100, 120 (C/P)</td>
<td>84 (C/P)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>144, 160 (C)</td>
<td>100, 124 (C)</td>
</tr>
</tbody>
</table>

C = ceramic, P = plastic

**In addition to ASIC, Thomson-Mostek manufactures a broad selection of MOS and bipolar devices for both commercial and military applications: microcomponents, memories, telecommunication and linear circuits as well as Discrete, RF and microwave transistors and passive components.**

EDN September 3, 1987

CIRCLE NO 76

97
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CIRCLE NO 82
CMOS DSP IC offers 80-nsec cycle time; operates on IEEE floating-point numbers

Targeted at high-performance applications such as graphics, telecommunications, image processing, high-speed control, and speech processing, the Model WE DSP32C CMOS floating-point digital signal processor (DSP) features cycle times as low as 80 nsec. The processor is compatible with the IEEE standard floating-point format. You can purchase an optimized C compiler for software development. Three 512x32-bit banks of RAM on the IC ensure fast access to memory. A second version of the chip substitutes a 1k×32-bit array of ROM for one of the banks of RAM.

The chip also features 15 general-purpose registers, five increment registers, two external interrupts, eight vectored interrupts, and a 16M-byte address space. You can program the DSP chip for 8-, 16-, or 32-bit accesses to external memory. Furthermore, the chip automatically inserts as many as three wait states when used with slow main memory. A loop-control register controls execution through 0 to 255 iterations of code with no overhead. On-chip I/O resources consist of a 16-bit parallel port and a serial port capable of operating as fast as 22.5M bps.

The DSP32C can fetch two 32-bit numbers from memory, multiply and accumulate the result, and write it to memory in one 80-nsec instruction cycle (25M flops). It executes 6.6M Whetstone instructions per second, performs a 1024-point FFT in 4.4 msec (including bit reversal), executes a FIR-filter algorithm at 80 nsec/tap, and executes an adaptive-filter algorithm at 160 nsec/per tap. The company also plans to offer the DSP32C in a 100-nsec version.

Unlike most DSPs based on Harvard architecture, the DSP32C uses a single high-speed data/program bus that can support four memory accesses in a single instruction cycle. This bus allows the processor to fetch two operands from memory, perform a multiply/accumulate operation, and write the result to memory in a single instruction cycle.
PRODUCT UPDATE

Because the DSP32C is source- and object-code compatible with its predecessor, the NMOS WE DSP32, designers have direct access to a large library of applications code. Furthermore, you won’t have to wait for the DSP32C to become available to begin development. You can use the first-generation DSP32 now, and replace it with the higher-performance, lower-power DSP32C when it becomes available.

The new CMOS chip does include certain enhancements. The DSP32C internally uses a 24-bit mantissa and 8-bit exponent floating-point format. For access to IEEE databases, it includes logic that converts between the IEEE floating-point format and the IC’s internal format in a single cycle. The chip also provides single-cycle instructions to convert 8-bit µ-Law, 8-bit A-Law, and standard 8-, 16-, and 24-bit integer formats to and from the DSP32C’s internal 32-bit floating-point format.

After each floating-point multiplication or addition, the DSP32C automatically normalizes the accumulator result in hardware. This operation prevents a loss of precision when moving data from the accumulator to main memory, or before adding the accumulator result to another floating-point number.

To support access to external data, the DSP32C interfaces to codecs, other DSP32s and DSP32Cs, and TDMs (time-division multiplexed lines) without requiring glue logic. The on-chip serial port is double buffered and therefore can perform back-to-back transfers. An on-chip DMA controller supports simultaneous DMA transfers between the serial port and the parallel port without program intervention.

A full complement of development tools including a C-like assembler, a link editor, a simulator/debugger, and a C compiler support software development for the DSP IC. The software development package executes on the MS-DOS operating system and costs $995. The company also plans to offer a set of tools for Unix. A $1500 IBM PC-based hardware development system provides full-speed in-circuit emulation of the DSP32C, breakpoint capabilities, and analog/digital I/O. The same command language controls the in-circuit emulator and the simulator/debugger.

Expect samples of the DSP32C to be available around the end of the year, and production quantities will be shipped in the first quarter of 1988. The $70 (10,000) device will be packaged in a 133-pin PGA.

— Maury Wright
AT&T Technology Systems, 555 Union Blvd, Allentown, PA 18103.
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CIRCLE NO 11

EDN September 3, 1987
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EDN September 3, 1987
circle no 83
101
Single-board μcontroller family features tailored Basic language

This family of three single-board computers employs a custom, multitasking version of Basic, called CAMBasic by the manufacturer, to perform control tasks in real time. In addition to the CAMBasic language, the boards share other features, including Z80 μPs, 32-bit parallel I/O ports, two serial ports, a keyboard and a display port, and a battery-backed clock/calendar. Two members of the family also incorporate analog multiplexers and A/D converters.

CAMBasic devotes 37 of its 144 commands and functions to manipulating the onboard I/O resources on the single-board computer. For example, the Autolog command configures and starts the analog multiplexer and A/D converter on the SBS-1000 and SBS-1100 computers. On the SBS-1100, which has an 8-channel analog multiplexer and a 10-bit successive-approximation A/D converter, this command can acquire 5000 samples/sec. The SBS-1000 has a 4-channel analog multiplexer and a 12-bit integrating A/D converter that converts at a 200-sample/sec rate. The third board in the family, the SBS-1200, does not have an analog multiplexer or an A/D converter.

The 32 general-purpose, digital I/O lines include eight outputs with 500-mA, 50V drivers. In addition, one command in CAMBasic converts eight of the I/O lines into a dedicated port that can drive the company's DP-2×20 vacuum-fluorescent, alphanumeric display; another command configures another eight lines into a dedicated keyboard port. Special commands and functions in the language allow you to send characters to the display and read keystrokes from the keyboard without resorting to low-level I/O routines or directly addressing the hardware.

All three boards support program development with nothing more than a 5V power supply and an ASCII CRT terminal. The language ROM on the boards contains a program editor and debugging aids. The company also offers a $49 package called Smartlink for program development when using an IBM PC or compatible computer. With this software, you can upload and download programs from the PC's disks. Pop-up windows provide additional programming help by providing additional information about the single-board computers' error messages. Once a program has been debugged, the boards can store the program in EPROM, EEPROM, or battery-backed RAM. The boards incorporate a ROM programmer.

CAMBasic supports multitasking through an event-driven mechanism. At the end of each Basic instruction, a monitor routine checks for all interrupt conditions, as the program defines them. If any such conditions exist, the monitor makes a program branch to the appropriate line in the Basic program. The company claims the monitor routine checks for interrupt conditions at least 500 times/sec.

Although these three boards are designed to operate in stand-alone applications, an edge connector brings out an expansion port using the company's existing OEM bus pinout. Thus, you can use the company's full range of OEM bus expansion boards and its card cage to expand the capabilities of these single-board computers. In addition, the company offers an adapter card that allows a group of I/O pins on any of its single-board computers to directly drive Opto-22's I/O module racks. The SBS-1000 and SBS-1100 cost $495, and the SBS-1200 costs $445.—Steven H Leibson

Octagon Systems Corp, 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 426-8540.

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- CMOS technology for low power consumption
- Separate logic ground (78093-B) allows direct TTL connect without level shifting

Silicon Systems' SSI 78093 is a 12x8 matrix-array crosspoint-switching IC for telecom-switching and industrial-control applications. The new IC allows a large number of lines to be interconnected through one point. It is designed for use in key telephone systems, low-end PBX's, and datacom switching units. It could also have industrial applications in almost any kind of electronic control equipment.

Standard integrated features include microprocessor-control inputs, a line decoder, address latches, and a 6 Vpp analog-signal capability. Some of the advantages of SSi's new CMOS chip are: low power dissipation; supply voltages specified down to 4.5V; an option offering a separate logic ground for direct TTL logic level interface; very fast timing characteristics; and low nominal "ON" resistance.

For detailed specifications of the new part, send for a copy of the 8-page data sheet. Contact Silicon Systems, 14351 Myford Road, Tustin, CA 92680. Phone: (714) 731-7110, Ext. 575.

---

**PRODUCT UPDATE**

**160-MIPS imaging system sports open architecture**

Integrating text, graphics, and photographic-quality image processing at speeds reaching 160 MIPS, the $88,000 Model 120 image computing system uses standard software; the system employs an open architecture based on the VME Bus. The system combines a 68020 CPU with an image memory manager, an algorithm processor, and a parallel image processor to provide a plug-and-play imaging system in a single, integrated unit that fits beside a desk.

The Model 120 also simplifies software development by letting you use standard products such as Unix BBS 4.2, MIT's X-Windows, and the C programming language. You can use DEC and HP graphics software-development tools for the X-Windows environment. The Image Display List System (IDLS), which is similar to PHIGS (Programmers' Hierarchical Interactive Graphics Standard), provides a high-level software interface to further cut your application development time and is available now. The manufacturer plans to release a true PHIGS package for the Model 120 during the fourth quarter of this year.

A custom VLSI image-processing chip set endows the Model 120 with its 160-MIPS speed. The chip set contains four image DSPs that operate in parallel. Each IC includes an ALU, writable control store, control logic, a register file, and multipliers. The company plans further integration by developing VLSI circuits for image memory control, image algorithm processing, and floating-point operations.

The Model 120 comes with a 16.67-MHz 68020 CPU, 68881 floating-point coprocessor, 4M bytes of RAM, 140M-byte hard-disk drive, 60M-byte tape drive, six VME Bus slots, Ethernet interface, keyboard, mouse, and Unix license. The 120's 19-in. color monitor offers 1280x1024-pixel resolution. In addition, 10M bytes of image memory have three buffers with a capacity of 2.5M pixels per buffer (eight bits per pixel).

For $68,000, you can buy a Model 100. Including a 13-in. color monitor with 640x480-pixel resolution, the Model 100 operates at 122-MIPS image computing speeds. This version comes with 6M bytes of image memory with storage for 1.5M pixels per buffer.

An application development software package costs $4995 and includes X-Windows, IDLS, a primitive module of image/graphics algorithms, and a set of image-oriented window and menu tools.

—J D Mosley

Visual Information Technologies Inc, 3460 Lotus Dr, Plano, TX 75075. Phone (214) 596-5600.

Circle No 630
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“You told us you wanted a modem chip that connects directly to the computer bus with no additional IC’s—a chip compatible with popular bus standards but flexible in use. And you wanted it to run from a single +5 volt supply with the lowest possible operating power. So we developed the SSI K222U—the industry’s most highly integrated combination modem and UART. And here’s what our new chip does for you.

“It operates off the system microprocessor without the need for a separate controller chip. It frees up board space for other purposes by putting the modem, the UART, and system related functions all in one 40-pin DIP. It provides you with all the modem functions you need for world-wide operation at 300, 600, and 1200 bps rates for Bell and CCITT standards. And it gives you a UART interface that is completely compatible with the industry standard 8250A/16C450 devices used with IBM PC compatible products. Our unique design also allows you to use the UART independent of the modem function, giving you an additional serial port. All of this in a low-power CMOS device that operates from a single +5V supply.

In short, it’s a chip that we designed for your application.”

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For more information on the SSI K222U, or the complete K-Series family of compatible modem IC’s, contact: Silicon Systems, 14351 Myford Road, Tustin, California 92680.
Until now, if you wanted to put 50,000 gates on one chip, you usually had to put them in one at a time. You had to put in three months work. And you had to put your launch date into a holding pattern. Not anymore.

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READERS' CHOICE

Of all the new products covered in EDN's June 25, 1987, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our June 25, 1987, issue.

COMM TESTERS
The Interview 5, 5 Plus, 10 Plus, and 15 Plus are portable units that feature built-in keyboards and LCDs and combine the functions of several instruments (pg 324).
Atlantic Research Corp.
Circle No 605

DSP DEVELOPMENT
The 320/PC-20 daughter board, when used with the company's Algorithm Development Package (ADP), provides a full development system for the TI TMS32020 DSP microcomputer (pg 282).
Atlanta Signal Processors Inc.
Circle No 602

DISPLAYS
The Supernova system consists of stackable 4-character LCD modules and a serial-ASCII input controller card. The operating range is −30 to +85°C (pg 312).
IEE Inc.
Circle No 603

SWITCHING-REGULATOR ICs
The CS-320/321 current-mode control ICs connect in any of three configurations that sense peak inductor current (pg 114).
Cherry Semiconductor Corp.
Circle No 601

C FUNCTION LIBRARY
The BlackStar C function library provides 275 fully tested functions for use with versions 3.0 and 4.0 of the Microsoft compiler and version 3.0 of the Lattice compiler (pg 322).
Sterling Castle Software.
Circle No 604
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CIRCLE NO 96
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For more information worldwide, contact one of the Gates Regional Sales Offices listed below.
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Source: Electronics Purchasing magazine's survey of buyers
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Then we suggest you find a nice quiet place, clear your mind of all distractions, and think it over. Maybe a nice quiet place like Bora Bora.

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Program

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- Sensors
- Sample-and-hold devices

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- Power semiconductors
- Linear regulators (including low dropout regulators)
- Switching power supplies
- Power drivers and switches

LUNCH

Session III:
Special Functions
- Motion control devices
- Sensors for process control
- References
- Communications devices
- Video devices
- Local area network devices
- Modems
- Analog switches

BREAD Session IV:
Data Acquisition and Filters
- Switched capacitor filters
- Techniques for analog-to-digital and digital-to-analog conversion
- Application circuits

Dates and locations

Bellevue, WA Oct. 5 Phoenix, AZ Oct. 13
Santa Clara, CA Oct. 6 Denver, CO Oct. 14
Los Angeles, CA Oct. 7 Dallas, TX Oct. 15
Santa Ana, CA Oct. 8 Minneapolis, MN Oct. 19
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Cleveland, OH Oct. 21
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CIRCLE NO 132
Monolithic op amps continue to evolve within the traditional performance categories, but many of this year's models bridge those familiar classifications by combining speed with precision, with low noise, and even with low supply current.

*Video, avionics, and satellite communications demand a fast signal-processing amplifier. (Photo courtesy Elantec Inc)*
By offering improved electrical performance, this year's monolithic operational amplifiers let you design analog circuits with less compromise and fewer circuit tricks. Occasionally, one of these new monolithic devices can replace an expensive hybrid.

The demand for speed is one of the driving forces behind these recent improvements. Modern applications such as workstation video, fiber optics, and automatic test equipment can use all the bandwidth and slew rate that monolithic op amps can muster. In response to this demand, op-amp manufacturers have recently produced high-speed models that are based on CMOS and some that are based on bipolar processes in which the transistors are separated by means of junction isolation, oxide isolation, and dielectric isolation.

Manufacturers have also recently produced op amps distinguished not by speed but by precision, low noise, or low power consumption. Even these models, however, provide higher speed than ever before. The greater bandwidths and slew rates that these products exhibit result from ongoing refinements in the fabrication processes.

This year's crop of monolithic op amps also emphasizes special-purpose products, such as power devices, chopper-stabilized CMOS devices, and devices that fit readily into µP systems because their performance specs are guaranteed for 5V power supplies.

Upgrade your quad-741 sockets

Five-volt operation is one attribute of the bipolar VA4741/4742 from VTC—all of the product's guaranteed specs are based on ±5V supplies. This quad 741-type op amp comes close to fitting into the general-purpose category, yet it offers a typical 2.7V/µsec slew rate and a 5-MHz gain-bandwidth product, which represent a fourfold increase in speed over that of the standard 741. The device, which is available in two standard pinouts, lets you upgrade the ac performance of circuits based on conventional quad-741 op amps from Raytheon, Harris, and Micro Power Systems.

The bipolar LM604 from National Semiconductor is difficult to classify: It has little in common with a quad op amp, except that it has four differential inputs. Called a 4-channel mux-amp, the LM604 has one output and four digitally selectable inputs (a change of channel requires 5 µsec). By adding external components, you can configure the device as a multiplexer, a programmable filter, or a programmable-gain amplifier (PGA). What's more, the output has a digitally controlled high-impedance state that lets you create an 8-channel multiplexer, for instance, by connecting two device outputs in parallel.

Bipolar devices remain the best choice for applications that require precision op amps (except when you're developing low-frequency applications, for which chopper-stabilized CMOS amplifiers may be more suitable). The definition of a "precision" op amp varies, but one manufacturer suggests that such a device should have an input-offset voltage ($V_{os}$) of no more than 200 µV, a $V_{os}$ drift of 2 µV/°C, an input bias current of 20 nA, low noise, and an open-loop gain of at least 200,000 ($A_{ol}$). Most of the following precision products adequately meet these specs.

Raytheon's RC4207B, for example, replaces the generic 4558-type dual op amp, but each amplifier in the RC4207B resembles the industry-standard OP-07. The RC4207B differs significantly from the OP-07 in some
Bipolar processes remain the best choice for precision op amps, but a chopper-stabilized CMOS amp may be more suitable for low-frequency applications.

This low-power sample/hold circuit makes use of the low supply current, single-supply operation, and 0V signal-handling capability of Linear Technology's LT1006 precision op amp.

respects, however: The op amps in the RC4207B spec a 1.5-MHz bandwidth, 10-nA input bias current, and 100-dB CMR; the corresponding specs for the OP-07 are 0.6 MHz, 3 nA, and 110 dB. The RC4227B quad op amp is similar but offers more speed. It has a 1.5V/μsec min slew rate and a 5-MHz bandwidth, vs the OP-07’s 0.1V/μsec and 0.4 MHz. It also has a lower noise spec than that of the OP-07—the RC4227B specs 0.08 μV p-p, 0.1 to 10 Hz; the OP-07 specs 0.35 μV p-p.

The MAX401 from Maxim features a proprietary technique for trimming the offset voltage after package assembly. The result is a 15-μV max offset, according to the preliminary data sheet. This model offers excellent dc specs and better ac specs than those of most precision op amps: 0.4-μV/°C V OS drift, 10 6 A VOL, 0.08-μV p-p noise (0.1 to 10 Hz), a 1.7V/μsec slew rate, and a 5-MHz bandwidth.

National Semiconductor and Harris also offer precision bipolar op amps. National’s LM607AC offers a max V OS and V OS drift of 25 μV and 0.3 μV/°C (respectively), a min A VOL of 5×10 6 (when the load is 2 kΩ), and excellent common-mode rejection and power-supply rejection of 124 and 120 dB min. The Harris HA-5134A-5 offers decent specs for a precision quad: a 100-μV max V OS, 1.2-μV/°C max V OS drift, 4-MHz typ bandwidth, and 1.5×10 6 min gain.

Linear Technology Corp calls its LT1006 the industry’s first single-precision op amp that operates from a single supply. Although it operates with any supply voltage between 2.7 and 15V, its specs are optimum at 5V (the introductory data sheet lists 15V specs as well). The input common-mode range includes ground, which simplifies the amplification of low-level signals, such as those produced by strain gauges and thermocouples. The output swings within a few millivolts of ground, and the output also delivers ±20 mA while drawing only a 520-μA max supply current at 25°C.

The LT1006AC specs a 50-μV max V OS, 1.3-μV/°C max V OS drift, 0.25V/μsec min slew rate, and 10 6 min A VOL (10-kΩ load). It comes in an 8-pin DIP or metal can. By connecting a resistor to pin 8, you can program the internal operating current to achieve lower supply current (90 μA) or a higher slew rate (1V/μsec or more).

Finally, Precision Monolithics has three new precision op amps that are now available and three more that will be available soon. The PM1012A, for instance, is an alternate to the LT1012 from Linear Technology. Drawing only 400 μA, which is 1/4 the supply current of an OP-07, the PM1012A offers performance similar to that of the OP-07 but with lower V OS (35 vs 75 μV) and much lower input bias current (0.1 vs 3 nA). Another low-power device, the OP-97, will maintain OP-77 performance except for noise (17 vs 10.3 nV/√Hz at 10 Hz) while drawing only 0.4 mA of supply current (vs the OP-77’s 2 mA).
Because these chopper-stabilized op amps from Intersil operate on ±15V and have standard pinouts, they can replace conventional op amps in low-frequency, precision applications.

PMI’s OP-200E is a dual OP-77. Key specs for the part include a 50-µV $V_{os}$, 0.7-µV/°C $V_{os}$ drift, min $A_{Vin}$ of $5 \times 10^6$ (10-kΩ load), and only 725 µA of supply current per amplifier. The company notes that a monolithic dual op amp often yields a better pc-board layout than do two singles or half a quad. PMI will introduce the OP-270 in October (a dual OP-27) and the similar but faster OP-271 in November.

The OP-490 is a quad OP-90, and it’s available now. Like the single OP-90s, each amplifier of the quad draws less than 20 µA of supply current, operates on single or dual supplies, and has an input-signal range that includes ground (the output swings within 500 µV of ground when the load is 10 kΩ). As in the OP-90, the OP-490’s input signals can exceed either supply rail by 20V without causing damage. Again, PMI plans to introduce a dual OP-90 (the OP-290) in January 1988.

Chopper stabilization is another option for precision signal-processing applications. Although the current monolithic-CMOS chopper amplifiers are suitable only for frequencies below about 10 Hz, they suit a large number of interface applications that require amplification of the signals from strain gauges and thermocouples. The technique achieves very low values of $V_{os}$ and $V_{os}$ drift by nulling the amplifier’s input offset voltage repeatedly—200 to 600 times per second.

The chopping action not only reduces $V_{os}$ and its variation with time and temperature; it also removes 1/f noise and therefore contributes less noise than does a precision bipolar op amp in bandwidths below 1 Hz. And because the chopping is independent of output level and is equally effective for all values of supply voltage and input-signal level, the chopper amplifiers provide excellent CMR, PSR, and $A_{Vin}$.

Op amps chop the cost of signal processing

Despite the advantages of chopper amplifiers, the widespread use of these parts was inhibited by their complexity and cost until Intersil introduced all-CMOS versions several years ago. In these devices (the monolithic ICL7650 and the lower-noise ICL7652), CMOS analog switches replaced mechanical switches as signal choppers. This good idea created such demand that Linear Technology, Maxim, National, Siliconix, and Teledyne Semiconductor have since introduced pin-compatible versions of their own.

The original CMOS choppers required two external capacitors for storing error voltages. Maxim simplified the application of its MAX430 and MAX432 by including chip capacitors in the package, and Teledyne further simplified its versions by integrating the capacitors on chip, using electronic means to magnify the capacitors’ apparent size.

Intersil then responded with the ICL7650S and ICL7652S, which offer better ac and dc performance than the originals. Like the earlier monolithic choppers, these amplifiers are fabricated with a CMOS process that features low breakdown voltage, and, therefore, they can tolerate no more than 18V between the supply rails. This limitation can prevent the direct replacement of many bipolar op amps.

To solve that problem, Intersil next introduced the...
Although the current monolithic-CMOS chopper amplifiers are suitable only for frequencies below about 10 Hz, they suit various interface applications.

ICL420 and ICL421. Featuring the standard 8-pin op-amp pinout and characterized for ±15V supplies, the ICL420 plugs right into the socket of a conventional op amp such as the OP-07. (Note that you still have to connect two external capacitors between pins 1, 5, and 8.) The ICL421, on the other hand, comes in a 14-pin DIP that includes terminals for an external clock, an input-guard circuit, and an output-clamp connection that reduces the recovery time following saturation caused by excessive input voltage. Both devices offer an ESD-protection rating in excess of 2 kV (all pins), and both can operate on a single supply. For a single-supply voltage of 10V or more, the input common-mode ranges include ground.

Onboard capacitors simplify application

Teledyne Semiconductor has added models TSC901, TSC902 (dual), and TSC903 (quad) to its family of monolithic-CMOS, chopper-stabilized op amps. All these devices can operate with ±15V supplies or with a single 7 to 32V supply, and the input common-mode ranges include the negative supply rail. Each amplifier includes two integrated capacitors for storage of V_OS error voltages. The parts also feature a low supply current (0.6 mA max) as well as fast recovery at the output—20 msec following positive saturation, 5 msec following negative saturation—without the requirement for an external clamp circuit.

The non-chopper CMOS op amps pioneered by Intersil and TI offer an assortment of distinct advantages and drawbacks. Compared with bipolar op amps, the CMOS types are weak on CMR, PSR, slew rate, and AvoL, and they are relatively noisy. On the other hand, CMOS op amps give you 5V operation, low power consumption, and very low I_S, and they're continuing to improve.

The TLC279 from TI is a quad op amp that has the advantages of silicon-gate CMOS: low initial V_OS, good V_OS stability over time and temperature, and decent ac performance. The device comes in four V_OS grades (0.75, 2, 5, and 10 mV) for each of the commercial-, industrial-, and military-temperature ranges. The typical V_OS drift is 1.8 µV/°C. The typical ac specs for the part are a 3.6V/µsec slew rate, 1.7-MHz bandwidth, and 46° phase margin. The TLC279 comes in a DIP or surface-mount package and operates from a single 4 to 16V supply.

For applications that require an ultra-low I_S, you can hardly do better than the OP-80 from PMI. The preliminary data sheet lists a remarkable 15 pA max at 125°C. At room temperature, the company says, the typical I_S (10 fA) is 62 electrons/msec. The device comes in an 8-pin DIP or metal can with a standard pinout. It has a 2-mV max V_OS, an AvoL of 10^6 (for a 2-kΩ load), and a 200-µA max supply current.

The ALD1702 from Advanced Linear Devices is another CMOS op amp that offers something you can't
JFET inputs provide speed and fast settling for the OP-44, a fast, precision op amp from Precision Monolithics.

get anywhere else—an input-signal (common-mode) range that includes both supply rails. The input stage consists of a differential pair of p-channel transistors connected in parallel with an n-channel pair. As the signal level passes through a threshold 1.5V above the negative rail, the device switches from one pair to the other. The output, too, is guaranteed to swing within 150 mV of the rails, over the commercial temperature range, when operating with a 2-kΩ load. Fabricated in silicon-gate CMOS, the op amp operates with 5V or ±2.5V supplies.

RCA offers a variety of op amps that feature a combination of bipolar and MOS transistors. The BiMOS devices have better ac performance than that of CMOS op amps, and they have much in common with CMOS amps as well: 5V operation, low IB, low cost, and an input-signal range that includes the negative supply rail.

The company's CA5130, for instance, offers unity-gain stability (if you add an external 47-pF capacitor), 90-dB min A_voL (with a 10-kΩ load), a 10V/µsec slew rate, and a 4-MHz unity-gain bandwidth. The output stage is a CMOS inverter that swings the output voltage within 10 mV of either supply rail when operating with light loads. The CA5160 is a similar device that is internally compensated for unity-gain operation, but you can add further, external compensation if your application requires it. The dual version is a CA5260.

Two more BiMOS op amps from RCA, the CA5470 quad op amp and the CA5202 dual video op amp, are slated for introduction in September. Advance information on the CA5470 promises a 4V/µsec min slew rate and a 10-MHz unity-gain bandwidth, as well as the standard BiMOS attributes: very low IB, a common-mode range that includes the negative rail, and the ability to operate with supply voltages in the range from 3 to 16V (or ±1.5 to ±8V). The CA5202 dual video op amp will provide a 50-MHz bandwidth and a 100V/µsec slew rate while drawing only 6 mA of supply current per amplifier.

Low gain allows speed and stability

Another way that manufacturers achieve low IB in an op amp is to use junction FETs (JFETs) in the device's input stage. The JFETs have a more important effect, however: They allow the op amps to achieve speed without sacrificing stability. Because a JFET has lower transconductance (g_m) than an equivalent bipolar transistor does, the JFET can achieve a given slew rate with less destabilizing gain. (As a bonus, JFET construction is reasonably compatible with the bipolar-IC fabrication process.)

Therefore, JFET-input (BiFET) op amps can offer low-IB error, high slew rate, and fast settling time—an attractive combination for the output amplifier of a 12-bit D/A-converter, for example. Three recent BiFET op amps suit these and other applications that demand both speed and precision.

First, the unity-gain-stable OPA602 from Burr-Brown specs a 20V/µsec min slew rate, a 3.5-MHz min gain-bandwidth product, and 1.0-µsec typ settling to 0.01%. The company measures this op amp's dc and dynamic specs with an unusually heavy output load—1-
<table>
<thead>
<tr>
<th>MANUFACTURER AND MODEL</th>
<th>INPUT OFFSET VOLTAGE (mV MAX)</th>
<th>INPUT BIAS CURRENT (µA MAX)</th>
<th>LARGE-SIGNAL VOLTAGE GAIN (V/µSEC MIN)</th>
<th>INPUT NOISE-VOLTAGE DENSITY AT 10 Hz (nV/√Hz TYP)</th>
<th>SLEW RATE (V/µSEC MIN)</th>
<th>0-DB BANDWIDTH (MHz TYP)</th>
<th>SETTLING TIME TO 0.1% (µSEC TYP)</th>
<th>CMRR (dB TYP)</th>
<th>PSRR (dB TYP)</th>
<th>NOMINAL SUPPLY VOLTAGES (V TYP)</th>
<th>SUPPLY CURRENT (mA TYP)</th>
<th>PRICE (US$)</th>
<th>COMMENTS</th>
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<tr>
<td>ADVANCED LINEAR DEVICES ALD1702PA</td>
<td>0.9</td>
<td>30 pA</td>
<td>0.05</td>
<td>100 (AT 1 kHz)</td>
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<td>70/70</td>
<td>±2.5</td>
<td>1.1</td>
<td>$3.97</td>
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<td>0.15</td>
<td>45</td>
<td>45</td>
<td>13</td>
<td>0.5 (TO 0.01%)</td>
<td>70/89</td>
<td>±15</td>
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<td>90/90</td>
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<td>45</td>
<td>45</td>
<td>13</td>
<td>0.5 (TO 0.01%)</td>
<td>70/89</td>
<td>±15</td>
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<td>0.05</td>
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<td>2</td>
<td>2.5</td>
<td>4.0</td>
<td>80/80</td>
<td>±15</td>
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<td>LM675T</td>
<td>10</td>
<td>2.0</td>
<td>0.03</td>
<td>8</td>
<td>5.5 (GBW)</td>
<td>—</td>
<td>70/70</td>
<td>±15</td>
<td>18</td>
<td>$4.25</td>
<td>POWER OP AMP</td>
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<td></td>
</tr>
<tr>
<td>PLESSEY LS541B</td>
<td>10 (TYP)</td>
<td>20</td>
<td>45 dB</td>
<td>—</td>
<td>1400 (+) 900 (-)</td>
<td>800</td>
<td>0.04</td>
<td>47/40</td>
<td>121/5</td>
<td>25</td>
<td>$36.49</td>
<td>CURRENT-FB AMP</td>
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</tr>
<tr>
<td>PRECISION MONOLITHICS PM1012A</td>
<td>0.035</td>
<td>100 pA</td>
<td>0.3</td>
<td>17</td>
<td>0.1</td>
<td>—</td>
<td>—</td>
<td>114/114</td>
<td>±15</td>
<td>0.38</td>
<td>$6.50</td>
<td>LOW-POWER OP-07 (MIL VERSION)</td>
<td></td>
</tr>
<tr>
<td>OP-97E</td>
<td>0.025</td>
<td>0.002</td>
<td>5.0</td>
<td>17</td>
<td>0.1</td>
<td>0.4</td>
<td>—</td>
<td>120/110</td>
<td>±15</td>
<td>0.4</td>
<td>$5.20</td>
<td>LOW-POWER OP-77</td>
<td></td>
</tr>
<tr>
<td>OP-200E</td>
<td>0.005</td>
<td>0.003</td>
<td>5.0</td>
<td>11</td>
<td>0.1</td>
<td>0.5</td>
<td>—</td>
<td>120/115</td>
<td>±15</td>
<td>1.2</td>
<td>$5.90</td>
<td>DUAL OP-77</td>
<td></td>
</tr>
<tr>
<td>OP-80E</td>
<td>1.0</td>
<td>40 fA</td>
<td>0.1</td>
<td>—</td>
<td>0.2 (TYP)</td>
<td>0.3 (GBW)</td>
<td>—</td>
<td>72/63</td>
<td>±5</td>
<td>0.2</td>
<td>$14.00</td>
<td>CMOS</td>
<td></td>
</tr>
<tr>
<td>OP-44E</td>
<td>0.75</td>
<td>200 pA</td>
<td>0.5</td>
<td>—</td>
<td>100</td>
<td>20 (GBW)</td>
<td>—</td>
<td>88/66</td>
<td>±15</td>
<td>5.1</td>
<td>$9.50</td>
<td>FET INPUT</td>
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<tr>
<td>OP-490E</td>
<td>0.5</td>
<td>0.015</td>
<td>0.7</td>
<td>60</td>
<td>0.005</td>
<td>0.02</td>
<td>—</td>
<td>100/80</td>
<td>±15</td>
<td>0.6</td>
<td>$6.50</td>
<td>QUAD OP-90</td>
<td></td>
</tr>
<tr>
<td>RAYTHEON RC4207FNB</td>
<td>0.075</td>
<td>0.01</td>
<td>0.25</td>
<td>103</td>
<td>0.1</td>
<td>1.5</td>
<td>—</td>
<td>100/100</td>
<td>±15</td>
<td>5.7</td>
<td>$4.53</td>
<td>DUAL</td>
<td></td>
</tr>
<tr>
<td>RC4227FNB</td>
<td>0.075</td>
<td>0.055</td>
<td>0.25</td>
<td>3.8</td>
<td>1.5</td>
<td>10</td>
<td>—</td>
<td>100/100</td>
<td>±15</td>
<td>6</td>
<td>$4.07</td>
<td>DUAL</td>
<td></td>
</tr>
<tr>
<td>SIGNETICS NE5212</td>
<td>—</td>
<td>60 (MIN)</td>
<td>4.9 kΩ</td>
<td>—</td>
<td>—</td>
<td>120 (-3 dB TYP)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>24</td>
<td>$2.30</td>
<td>TRANSIMPEDEANCE AMP</td>
<td></td>
</tr>
</tbody>
</table>
The non-chopper CMOS op amps pioneered by Intersil and TI offer designers an assortment of distinct advantages and drawbacks.

### TABLE 1—MONOLITHIC OP AMPS

<table>
<thead>
<tr>
<th>MANUFACTURER AND MODEL</th>
<th>INPUT OFFSET VOLTAGE (mV MAX)</th>
<th>INPUT BIAS CURRENT (µA MAX)</th>
<th>LARGE-SIGNAL VOLTAGE GAIN (10^6 MIN)</th>
<th>INPUT NOISE VOLTAGE DENSITY AT 10 Hz (mV/√Hz TYP)</th>
<th>SLEW RATE (V/µSEC MIN)</th>
<th>CMR/PSR (dB TYP)</th>
<th>NOMINAL SUPPLY VOLTAGES (V TYP)</th>
<th>SUPPLY CURRENT (mA TYP)</th>
<th>PRICE ($/TYP)</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SILICON GENERAL</td>
<td>4.0</td>
<td>0.5</td>
<td>0.04</td>
<td>-</td>
<td>0.7</td>
<td>0.9</td>
<td>76/80</td>
<td>±24</td>
<td>10</td>
<td>$23.25</td>
</tr>
<tr>
<td>SPRAGUE</td>
<td>10</td>
<td>1.0</td>
<td>0.01</td>
<td>-</td>
<td>1.0</td>
<td>0.035</td>
<td>60/50</td>
<td>±6</td>
<td>40</td>
<td>$1.47</td>
</tr>
<tr>
<td>TELSYN SEMICONDUCTOR</td>
<td>0.015</td>
<td>50 pA</td>
<td>1.0</td>
<td>-</td>
<td>2 (TYP)</td>
<td>0.8</td>
<td>120/120</td>
<td>±15</td>
<td>0.45</td>
<td>$5.25</td>
</tr>
<tr>
<td>TSI903CpA</td>
<td>0.015</td>
<td>50 pA</td>
<td>1.0</td>
<td>-</td>
<td>2 (TYP)</td>
<td>0.8</td>
<td>120/120</td>
<td>±15</td>
<td>0.9</td>
<td>$9.45</td>
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<tr>
<td>TSI904CpA</td>
<td>0.015</td>
<td>50 pA</td>
<td>1.0</td>
<td>-</td>
<td>2 (TYP)</td>
<td>0.8</td>
<td>120/120</td>
<td>±15</td>
<td>1.8</td>
<td>$19.95</td>
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<tr>
<td>TEXAS INSTRUMENTS</td>
<td>0.075</td>
<td>0.6 pA (TYP)</td>
<td>0.005</td>
<td>130</td>
<td>3.6</td>
<td>(TYP)</td>
<td>70/85</td>
<td>5</td>
<td>2.7</td>
<td>$2.26</td>
</tr>
<tr>
<td>VTO</td>
<td>5</td>
<td>0.4</td>
<td>0.006</td>
<td>2.7 (TYP)</td>
<td>5</td>
<td>80/66</td>
<td>±5</td>
<td>14</td>
<td>$3.96</td>
<td>QUAD</td>
</tr>
<tr>
<td>VA701PK</td>
<td>0.025</td>
<td>0.04</td>
<td>1.0</td>
<td>5.5 (MAX)</td>
<td>3</td>
<td>8 (GBW)</td>
<td>10 (TO 0.01%)</td>
<td>±5</td>
<td>7</td>
<td>$3.93</td>
</tr>
<tr>
<td>VA711PK</td>
<td>0.025</td>
<td>0.04</td>
<td>1.0</td>
<td>5.5 (MAX)</td>
<td>25</td>
<td>8 (GBW)</td>
<td>10 (TO 0.01%)</td>
<td>±5</td>
<td>7</td>
<td>$5.98</td>
</tr>
</tbody>
</table>

**NOTES:**
1. EXCEPT WHERE INDICATED
2. OP-AMP MODELS ARE COMMERCIAL- OR INDUSTRIAL-GRADE PARTS UNLESS OTHERWISE NOTED.
3. GBW = GAIN-BANDWIDTH PRODUCT
4. FB = FEEDBACK
5. IA = 10^-3 A
6. DI = DIELECTRIC ISOLATION

kΩ in parallel with 500 pF—connected. The company states that the capacitance has little effect on settling time, so the OPA602 is a robust candidate for applications with low-impedance loads.

Second, Analog Devices' AD744 offers a settling time (to 0.01%) of 0.5 µsec typ, 0.9 µsec max. The part's internal compensation provides stable operation at minimum closed-loop gains of -1 or 2. You can add external compensation that extends the gain bandwidth to over 200 MHz or enables the amplifier to drive 1-nF capacitive loads. Preliminary specs for the device include a 45V/µsec min slew rate, a 13-MHz typ gain-bandwidth product, and 0.003% total harmonic distortion (THD), making the device suitable for high-fidelity audio applications.

**Low I_D allows a high source impedance**

Third, the wideband OP-44 from PMI offers ac performance similar to that of Harris's HA-2520. Like the HA-2520, the OP-44 is stable for closed-loop gains of 3 or more. It has a 100V/µsec min slew rate, a 20-MHz gain-bandwidth product, and a full-power bandwidth of 1.5 MHz min. Its settling time to 0.01% is less than 1.2 µsec.

Finally, Analog Devices' AD549 electrometer op amp makes full use of the FET input as a low-I_D device. Built with the company's proprietary Topgate BiFET process and offered in four electrical grades, this monolithic amplifier specs a max I_D as low as 60 fA at 25°C. The model also specs a 0.5-mV max V_os and a 10-µV max V_vs drift. The AD549 is suitable for use with photodiodes and other signal sources with a high (1 MΩ or more) source impedance.

**Fast-slewing, low-noise models**

For signal-processing applications such as audio, you can choose from a number of new fast-slewing, low-noise op amps. Motorola's MC33078 (dual) and MC33079 (quad) op amps, for example, have less than 5 nV/√Hz voltage noise above 20 Hz, and less than 4.5 nV/√Hz above 100 Hz. Their peak-to-peak noise from 0.1 to 10 Hz is about 0.2 µV. In addition, the op amps provide a 7V/µsec typ slew rate, a 9-MHz typ unity-gain bandwidth (open-loop measurement), and a typical THD of 0.002%. (Although the two devices are available now, these specs are preliminary ones, and are subject to
Chopper amplifiers not only reduce $V_{os}$ and its variation with time and temperature; they also remove $1/f$ noise.

Suitable for RF and video applications, Analog Devices' AD5539 offers spec improvements over existing versions of the device.

Latest DI-bipolars are fast and quiet

From Harris, the HA-5101-5 (which is unity-gain stable) and HA-5111-5 (which is uncompensated and requires an $A_{cl} \geq 5$) offer 7 and 3.5 nV/√Hz at 10 Hz and 1 kHz. Built with the Harris DI-bipolar (dielectrically isolated bipolar) process, the op amps share a 3-mV max $V_{os}$ and a 3-µV/°C max $V_{os}$ drift. The HA-5101-5 has a 6V/µsec min slew rate and a 10-MHz typ small-signal bandwidth. The uncompensated HA-5111-5 has a 40V/µsec min slew rate and a 60-MHz typ gain-bandwidth product (at a gain of 10).

Another DI-bipolar op amp from Harris, the HA-5147A, has a noteworthy combination of speed, precision, and low noise. Requiring a minimum closed-loop gain of 10, the device offers a 35V/µsec typ slew rate, a 120-MHz gain-bandwidth product (at 1 MHz), and a 500-kHz full-power bandwidth. Its $V_{os}$ is 25 µV max, and its $V_{os}$ drift is 0.6 µV/°C. The max noise density is 5.5 and 3.8 nV/√Hz at 10 Hz and 1 kHz.

A few manufacturers intent on making monolithic devices with the highest possible bandwidth and slew rate have developed some new very wideband bipolar processes. Others have adapted a current-feedback architecture for these purposes. First, several companies use (or are developing) processes that are complementary in terms of large and comparable bandwidth ($f_0$) for the pnp and npn transistors. Second, Elantec recently produced a current-mode-feedback amplifier (the EL2020) in monolithic form. (Comlinear Corp has long used this architecture in building high-speed hybrid amplifiers.) Comlinear will also introduce monolithic devices of this type in September (the CLC400 and CLC401), and Analog Devices will follow suit in October with its AD846. Plessey, too, offers a current-feedback device, the recently introduced SL2541B.

An op amp or not an op amp

You might argue that the current-feedback amplifier isn't an op amp, but you'd be correct only in that the device doesn't fit the textbook definition applicable to conventional voltage-feedback amplifiers. The current-feedback amplifier (also called a transimpedance amplifier) is at least as easy to use as conventional op amps are, and it provides greater bandwidth at a given gain than an equivalent voltage-feedback op amp does.

The major difference between the transimpedance amp and a conventional op amp lies in the input stage (Fig 1). An internal unity-gain buffer connects across the input terminals. The noninverting input has a high impedance and the inverting input has a low impedance, but in normal operating configurations, the inverting-input current is very small. Therefore, the input resembles that of an op amp in two respects: Voltage between the terminals is ideally zero, and
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### Flash Converters

<table>
<thead>
<tr>
<th>Model</th>
<th>Bits of Resolution</th>
<th>Conversion Rate</th>
<th>Sampling Rate</th>
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<tr>
<td>ADC-310</td>
<td>10</td>
<td>20 MHz</td>
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<td>ADC-300</td>
<td>20 kHz</td>
<td>20 MHz</td>
<td>16 MHz</td>
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<tr>
<td>ADC-301</td>
<td>30 kHz</td>
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<td>30 MHz</td>
</tr>
<tr>
<td>ADC-302</td>
<td>50 kHz</td>
<td>50 MHz</td>
<td>50 MHz</td>
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<td>ADC-303</td>
<td>100 MHz</td>
<td>100 MHz</td>
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<td>20 MHz</td>
</tr>
<tr>
<td>ADC-207</td>
<td>7</td>
<td>35 MHz</td>
<td>35 MHz</td>
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### Sampling Boards

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<th>Sampling Rate</th>
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<tr>
<td>ADC-B207</td>
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<td>35 MHz</td>
<td>ADC-B207</td>
</tr>
</tbody>
</table>

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**JFET-input (BiFET) op amps offer low-$I_B$ error, high slew rate, and fast settling time.**

![Current-feedback connection](image)

**Fig 1—This conceptual diagram (from a Comlinear application note) shows the basic architecture of a current-feedback amplifier.** The internal transimpedance gain block, $A(s)$, senses small changes in the inverting terminal's bias current ($I_{INV}$) and produces a large but proportional change in $V_{OUT}$.

current into the terminals is nearly zero.

For most applications, you use a feedback-resistor value ($R_F$) recommended by the manufacturer. (In fact, some designs provide this resistor internally, and you simply choose the desired gain-setting resistor, $R_C$.) $A(s)$ represents the amplifier's gain. A small change in $I_{INV}$ produces a large change in $V_{OUT}$, so $A(s)$ is a transimpedance function. If you let $A(s) = N(s)/D(s)$, then

$$\frac{V_{OUT}}{V_{IN}} = \frac{GN(s)}{N(s) + R_F D(s)},$$

where the closed-loop gain $G = 1 + R_F/R_C$.

To appreciate the advantage of current feedback, compare its transfer function with that of an op amp:

$$\frac{V_{OUT}}{V_{IN}} = \frac{GN(s)}{N(s) + GD(s)}.$$

You can see that the op-amp function's denominator (and therefore its pole locations) will change as you change $G$. But the current-feedback amplifier's poles remain fixed because you don't bother $R_F$ when changing gain. The result is a minimal change in bandwidth for different values of closed-loop gain, as well as improvements in the amplifier's settling time, rise time, and phase linearity.

To fabricate the monolithic CLC400 and CLC401 amplifiers, Comlinear uses a bipolar process featuring 2.5-GHz vertical pnp transistors and 4-GHz npn transistors. The devices come in 8-pin plastic DIPs, require ±5V supplies, and draw about 15 mA of no-load quiescent current. The CLC400's nominal 250Ω feedback resistor lets you set gain values in the range from ±1 to ±8. Typical specs for a gain of 2, for example, include a 3-dB bandwidth of 200 MHz, 1.6-nsec rise and fall times, an 8-nsec settling time (to within 0.1%), and an 800V/µsec slew rate.

For the higher-gain CLC401, a nominal 1.5-kΩ feedback resistor lets you set gains from ±7 to ±40. At a gain of 20, the device provides a 3-dB bandwidth of 150 MHz typ; 2.5-nsec rise and fall times; a 10-nsec settling time (to within 0.1%); and a 1200V/µsec slew rate.

Elantec uses a dielectrically isolated bipolar process to build its EL2020. The amplifier operates best with a 1-kΩ feedback resistor, and it provides closed-loop gains between 10 and −10. It comes in an 8-pin plastic or ceramic DIP and operates with single or split power supplies in the range from ±3 to ±18V. The quiescent supply current is 9 mA when the op amp is operating with ±15V supplies. At unity gain, the amplifier specs a 50-MHz (typ) bandwidth, a 500V/µsec slew rate, 6-nsec rise and fall times, and a 90-nsec settling time to 0.1%.

Analog Devices calls its entry a precision operational transimpedance amplifier. Scheduled for introduction in October, the AD846 comes in an 8-pin can or 14-pin DIP and draws 5 mA from ±15V supplies. According to preliminary data, at a gain of −1 it has a bandwidth of 40 MHz typ, a 600V/µsec slew rate, a 10-nsec rise time, and an 80-nsec settling time (to 0.1%). The input specs a $V_{OS}$ of 0.25 mV max and a $V_{OS}$ drift of 1 µV/°C max, and the output can deliver ±50 mA.

**Amplifier includes buffer and V reference**

The monolithic SL2541B from Plessey includes, for convenience, a bandgap voltage reference and a separate 60-MHz video buffer. The device draws 25 mA from 12V/−5V supplies. At a gain of 2, the main amplifier has an 800-MHz bandwidth and slew rates of 1400V/µsec (rising) and 900V/µsec (falling). The op amp's rise and fall times are 1.6 and 3.2 nsec, and its settling time to 0.01% is 40 nsec. It comes in a 16-pin DIP or a 20-pin LCC.

Analog Devices' AD5539 is a more conventional (but very high frequency) op amp that is suitable for video and RF applications. It must operate at a minimum gain of 5 unless you add external compensation. The
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EDN September 3, 1987
Fast-slewing, low-noise amplifiers are useful for general signal-processing applications such as audio.

part specs a 220-MHz typ bandwidth (at a compensated gain of 2), an 82-MHz full-power bandwidth, and a 600V/µsec slew rate.

VTC now offers monolithic dual and quad versions for each op amp in its 4-member VA705-VA708 family. These op amps provide slew rates from 25 to 105V/µsec and gain-bandwidth products from 25 to 300 MHz.

The monolithic NE5212 from Signetics is also an amplifier that's worthy of mention, even though it's not an op amp: It's called a transimpedance amplifier (but it's not a current-feedback device). The NE5212 produces a differential voltage output in response to a current input. Suitable for use in applications such as fiber-optic receivers and RF amplifiers, it features

### Manufacturers of monolithic op amps

For more information on monolithic operational amplifiers, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.
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Current-mode feedback produces a minimal change in bandwidth for different values of closed-loop gain.

14-kΩ typ transresistance and a 120-MHz bandwidth.

Last in the roundup of high-speed op amps is Maxim's MAX452 family. These parts demonstrate that CMOS video amplifiers are practical. The MAX452 is a low-gain (40), 50-MHz amplifier that's intended for driving low-impedance (75Ω) loads. It has a 150V/μsec min slew rate, operates with ±5V supplies, and consumes only 250 mW. The monolithic MAX453, MAX454, and MAX455 are versions of this amplifier that include video multiplexers of 2, 4, and 8 channels, respectively.

**Automatic shutoff protects power op amps**

The category of monolithic power op amps also includes a number of recent offerings. The ULN-3751Z from Sprague is unity-gain stable and operates with supply voltages from ±3 to ±13V, or with a single supply of 6 to 26V. It can deliver 3.5A pk and includes a self-resetting circuit that shuts down the device when the chip temperature reaches approximately 160°C. Because the modified 5-lead, TO-220 plastic package has a heat-sink tab that connects internally to the chip's substrate, you must insulate the tab from ground when using split power supplies.

Capable of operating with supplies of as much as ±24V, the SG1173 from Silicon General has input specs that are comparable to a conventional op amp's: a 4-mV max V_{os}, 150-nA max input offset current, and 92-dB min A_{voL}. It includes automatic thermal shutdown and automatic current limiting at 3.5A. You can choose from TO-66 and TO-220 packages, in which case and tab, respectively, connect internally to the negative supply terminal.

The data sheet for National Semiconductor's LM675 specifies ±25V power supplies, but you can operate the device with supply voltages as high as ±30V. The op amp must operate at a minimum closed-loop gain of 10. It has an 8V/μsec typ slew rate and delivers 3A pk. To prevent inductive-kickback damage when driving reactive loads, the chip includes clamp diodes from each supply rail to the amplifier's output.

For additional protection, the LM675 not only limits output current to about 4A but reduces this level when a high voltage appears across either output transistor. Moreover, a separate circuit shuts off the amplifier when the chip temperature reaches 170°C. The amplifier resumes operation when the temperature drops to 145°C, but if temperature soon rises again, a second shutdown occurs at 150°C. This scheme provides protection during sustained overloads yet prevents a complete shutdown during short-duration faults.

The rugged OPA602BM from Burr-Brown can deliver a continuous ±5A while operating with ±40V supplies. It has a 1-mV max V_{os}, 8V/μsec min slew rate, 90-dB min A_{voL}, and 45-kHz min full-power bandwidth. You can operate the device and set the internal (symmetrical) positive and negative current limits by connecting one external resistor. Because the 8-pin, TO-3 package is electrically isolated from the chip, you can obtain maximum heat transfer by mounting the package directly on a heat sink.

The coming year promises further improvements in op amp performance. Although most manufacturers are taking a conservative position on new-product announcements and introductions, some have hinted at the developments underway. You can expect these efforts to lead to better bipolar, FET-input, and CMOS op amps. Maxim, for instance, is working on an auto-zeroed CMOS device it modestly calls the “superamp.” The firm's design goals for the superamp include a sub-µV V_{os}, 5-nV/√Hz midband noise, a 100-dB A_{voL}, a 140-dB CMR and PSR, a 1-MHz bandwidth, and a 0.5V/μsec slew rate.

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Specifications

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<td>SNT Series</td>
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<td>–</td>
</tr>
<tr>
<td>DIP Noise Filter</td>
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<td>Feed-through</td>
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EDN’s DSP Project—Part 3

Design and build a transponder using DSP tools

In the second part of this 4-part series, we reviewed some representative DSP tools available to help you design and build digital signal processors. In this the third part, we present a hands-on account of how we used some of those tools to create a transponder. Although a highly detailed knowledge of DSP algorithms was unnecessary, we did need to know much about µP development in order to use those DSP tools fruitfully.

David Shear, Regional Editor

In the August 20th issue (pg 183), we described the tools that are available for the development of DSP-based projects. To demonstrate how these tools work, we used some of them to build an acoustic transponder based on the Texas Instruments TMS320E17 general-purpose digital signal processor.

We purposely chose to design a simple device in order to show how the tools work—not how the device itself operates. Our transponder simply responds to a 523-Hz signal with a 965-Hz signal (see box, “A glance at an acoustic transponder”). The project was so simple that at first it didn’t look like a viable candidate for DSP at all. As we got further into the project, however, we found that even such a simple device can benefit from DSP techniques.

Evaluating the analog approach

An analog solution would be adequate for such a project. The block diagram of an analog approach (Fig 1) shows a rather typical analog system: input amplifier, filter, detector, signal generator, and output amplifier. But this approach has some inherent difficulties—primarily concerning the filter and the signal generator. The filter requires precision components and tuning, is nearly impossible to reconfigure without rebuilding, and is difficult to make stable and accurate over time and temperature. In addition, the signal generator’s output signal must start and end at the 0° phase point to eliminate the noise that would otherwise occur, and such phase control is difficult to obtain.

The DSP approach follows the analog

In our solution, we used DSP versions of the analog blocks. A bandpass filter filters all incoming signals to allow detection of the trigger signal in the very stable digital environment. After detection, the transponder creates a response. Because the sine waves are generated digitally, we can start and end at any phase angle we wish, thereby eliminating the noise from any abrupt changes in the output.

Next, we evaluated the feasibility of the design. Most of the software we needed was simple to write. It’s easy to evaluate the programs for acquiring data, feeding data to the filter, monitoring the output of the filter, creating the delays, and creating the sine-wave pulse. The necessary software sections require very little memory and execution time. The big question is the time it takes to run the filter software and the amount of memory that the filter requires.

Is the DSP approach feasible?

We used the Digital Filter Design Package (DFDP) from Atlanta Signal Processors Inc (Atlanta, GA). It’s a menu-driven package that requires color-graphics
Looking into the feasibility of a filter design is greatly simplified by having the filter code generated for you.

(CGA or EGA) capability. We used the Paradise (South San Francisco, CA) Autoswitch EGA 480 card along with a Mitsubishi AUM1471A color monitor.

The first screen yields a choice of five options: Recursive (IIR) Filter Design, Kaiser-Window Nonrecursive (FIR) Filter Design, Parks-McClellan Equiripple (FIR) Filter Design, TMS32010 Code Generation, or Return to DOS. We started at the top of the menu—the IIR filter.

The program then asked a series of questions about parameters and options. For each type of filter, we were careful to select the option to quantize the filter coefficients so that the code generator would work. This quantization is necessary because of the limited precision of the TMS32010 family. Within the IIR filter group, we found that an eighth-order Butterworth, an eighth-order Chebyshev (I or II), or a sixth-order elliptic met our requirements.

After the filter coefficients were calculated, we selected the plot option from the next menu to check the magnitude response and the group delay (Fig 2). Satisfied with the results, we saved the coefficients to disk for later use by the code generator.

Many filters can be quickly evaluated

None of the other filter designs met our requirements. The Kaiser FIR filter had a length of 449 taps. The resulting filter was very close to spec, but the data RAM requirements exceeded what we had available. The Parks-McClellan FIR filter design recommended a length of 379 taps, but the program would only accept a length of up to 130. We tried a length of 130, but the

A glance at an acoustic transponder

We designed a transponder that could be used to measure distances under water. Unlike typical sonar systems, our transponder system wouldn't rely on a reflected signal. Instead, the transponder would receive a trigger signal from a remote device and, after a fixed delay, transmit a response that's a signal of a higher frequency. The remote device could then calculate distance based on the delay between its transmission of the trigger signal and reception of the transponder's higher-frequency output.

When our transponder receives a trigger signal, the transponder waits (to give the reflections from the trigger signal time to die down) and then responds with its own signal. After responding, it shuts down for a length of time known as the deadband—a delay that gives the transponder's receiver time to recover from the rather overpowering response signal.

The DSP approach not only offers inherent stability and accuracy of digital methods, but it also can perform very sophisticated signal processing on incoming signals and can create complex response signals. Even in our simple project, we were able to move very easily from a single-tone to a multitone trigger signal; the analog alternative would have made this change much more complicated.

![Fig 1—An analog approach to our transponder task would include some signal conditioning, a bandpass filter and detector to detect the presence of the trigger signal, a level comparator, some delay elements, a sine-wave generator, and a power amplifier.](image-url)
stopband attenuation of the resulting filter was well below our desired value of 40 dB.

The least-order filter, in this case the sixth-order elliptic, appeared to be the best choice. After the DFDP created the filter code, we assembled the filter and checked the execution time and memory requirements. We used an 8-kHz sample rate, so the time we have available to process each sample is 125 µsec. With a cycle time of 200 nsec, we can execute 625 instructions per sample. The sixth-order elliptic IIR filter requires 69 cycles, 98 words of program memory (including initialization and coefficients), and 22 words of data memory. The TMS320E17 can handle a filter with these characteristics.

When we originally used the DFDP, we did not have an Intel 80287 in our PC/AT. The response of the system was dismal. Many of the operations took 10 to 15 minutes. This long response period prevented any interactive experimenting with various approaches in software—at least within a reasonable period of time. After we installed an 80287, a rather frustrating piece of software became a very useful tool.

The hardware looks simple

The hardware design of the transponder is shown in the schematic in Fig 3. The hardware's physical simplicity misrepresents its complexity of function. The system input is amplified and then fed to the TLC32040 analog interface chip (AIC). The AIC contains an antialiasing filter, a 14-bit ADC, a 14-bit DAC, a

---

**Fig 2**—The Digital Filter Design Package provides a magnitude plot and filter specifications and coefficients.
The creation of software for a DSP project is very similar to that of any software project. Many of the same tools are at your disposal.

smoothing filter, and control and timing circuitry—in other words, all of the circuitry needed to properly acquire analog information and produce an analog output.

The AIC communicates with the TMS320E17 via two serial ports, one for transferring data each way. The AIC transfers 16-bit words as two 8-bit transmissions, the most significant first. The TMS320E17 receives both of these bytes and reconstructs the 16-bit word. The AIC transmits and receives data simultaneously. Because the AIC initiates all data transfers, the TMS320E17 must always be prepared with data in the serial interface prior to an AIC request.

It’s tempting to interrupt the TMS320E17 and have

---

Fig 3—The simplicity of the transponder hardware can be misleading. The TLC32040 contains all of the hardware for data acquisition and signal synthesis. Inside the chip is the antialiasing filter, a 14-bit ADC, a 14-bit DAC, an output smoothing filter, and all of the timing and control logic to generate the sample rate.
it initiate the acquisition, but this technique can result in time jitter between samples because of the asynchronous nature of interrupt response. The jitter increases the noise of the input and the distortion on the output, so it’s very important that the sampling time be constant.

The rest of the circuitry provides the amplification of

![Circuit Diagram]

the signal from an electret condenser microphone, the speaker driver amplifier, a power-on reset, and the drive for the LED.

**Software starts with states**

The development of the control software (Listing 1, which begins on pg 144) began with a state machine (Fig 4) representing the four states of the operation: filter, delay, pulse, and deadband. After initialization, the program waits for a sample to arrive from the AIC; processes the sample in a manner depending on the present state; and then, if certain conditions are met, moves to the next state. Finally, it returns to waiting for another sample to arrive.

The sine-wave generator for the pulse output (response) is a slight modification of the version presented in the TI DSP Application Report, “Precision Digital Sine-Wave Generation.” This wave-generation subroutine adds a phase increment to the existing phase and then converts the phase to amplitude via a sine-wave look-up table. Each time the subroutine runs, a new amplitude is generated for output to the AIC.

The filter and the sine-wave generator are separate modules that are linked to the control program. Although a linker is not always needed, it is convenient. When we used the DFDP to change the filter parameters, it generated new code that can then link to the control code or to other program sections. Thus, we could make the changes to the filter, assemble the filter code, relink it all together, and then see how the filter works.
The hardware available for DSP designs has greatly simplified the design process and reduced the board space required to accomplish very complex tasks.

Fig 5—The control file that we used with the linker links XPNDR, SINEGEN, and IIR1 together starting at location 0. The common segments are placed so that the variables for each module will use its own memory area.

We used the TI assembler and linker to convert the assembly-language programs into object files for the simulator, the emulator, or the PROM programmer. Like most assemblers, ours was very easy to use. The result was a listing and a relocatable object file.

Not all tools are first rate

The linker from Texas Instruments was another story. Someone must have tried real hard to make such a complex and difficult-to-use linker. This linker is not tuned to the TMS320 family. As a result, it has a lot of flexibility, but that flexibility comes at the cost of added complexity. To run the linker, we had to first create a control file that told the linker what to do. Fig 5 shows the control file we found that worked. This linker produces an object file (.LOD) and a map file (.MAP). When the linker was done, it told us it had completed the linking process. That was it. To see whether there were error messages, we had to look at the .MAP file. But the error messages were not very helpful. All in all, it wasn’t a very impressive tool.

After linking the program, we tried to run it. We chose to use a simulator first because of the sterile, predictable environment that a simulator provides. Also, this transponder program was so simple that the simulator allowed us to walk through the entire program and check out all of the logic.

The first simulator we tried was the TI simulator. It does the job but requires constant entry of commands that define what’s to be displayed. The results of each command then scroll onto the screen, and any other bits of information that were on the screen previously are lost.

The next simulator we used was the Avsim product from Avocet Systems. This simulator constantly provides all of the information on the screen at one time. At first it’s a bit overwhelming (Fig 6), but it quickly becomes extremely useful.

Avsim offers many options after it’s started and a program is loaded. We found that we could single-step our program or run it continuously at three different speeds. As the program runs, the code to be executed is highlighted in the program fragment window. Setting breakpoints is simple: We just moved a cursor to where we wanted to place the breakpoint in the window that contained the appropriate code. Changing data in memory or registers is just a matter of placing the cursor on the data to be changed and entering the new value. We could change the input and output as well as the external pins with the same technique.

In our program, we waited for the BIO line (Fig 3) to change state to learn of the availability of a sample. It’s an easy test to perform during simulation. We started the program with the cursor on the BIO line. When the program entered the loop, waiting for BIO to change state, we entered the new BIO value and watched the program operate.

The Avsim simulator also makes it very easy to check out a program even with hardware interaction. In our development, the simulator was much easier to use than the hardware emulator. When the program did not work, we always went back to the simulator to investigate the problem.

After walking through the software with the simulator and after building the prototype, we plugged the emulator into the TMS320E17 socket on the prototype
and began the system test.

At the beginning of any integration, it's usually important to check the power supplies and the clock. In our case the clock looked terrible: It was not stable and caused many problems with the AIC. Our caution resulted in a lot of wasted time and effort, however. It turns out that the XDS emulator provides a messy clock until communication with the controlling PC is established. We would have been better off had we not bothered checking the clock.

Once the clock improved, we found the output of the AIC was insufficient to drive the emulator load. The emulator manual said that the $I_{IH}$ (input high current) was 1350 µA, and the AIC can only drive 300 µA. Another call to the factory informed us that the manual was in error; as a result, our emulator was not correctly set up for the TMS320E17. By moving a few jumpers, we got everything up and running.

The XDS emulator can run from a host computer (when it's placed between the host and a terminal) or from a PC. Using this emulator is like traveling back in time to the dark ages of µP development, however. It's very complex and shows very little information at any one time.

**Test DSP systems by looking at signals**

To test our software, we used a technique right out of the scope and probe world. First, the acquired sample was sent directly to the output. The input and output were then displayed on two channels of a scope. When they looked the same, we concluded that the interface to the AIC was working properly.

The next step was to check the filter. The input was sent to the filter, and the output of the filter was then sent to the AIC. We then could let the DFDP design a filter for us and check its operation in the real world—without requiring that we make any code changes. All we had to do was execute a batch file that assembled the DFDP output and linked it to the control program.

The convenience of DSP really became evident when it's necessary to make substantial changes. We found we could reconfigure the filter with extreme ease and then quickly check the new design in real time.

We continued along with this approach until the entire system was tested. When we linked the sine-wave generation program, we ran into a rather severe problem when using the code generated by DFDP. During initialization, the LACK (load accumulator with a constant) instruction points to the filter coefficients that must be loaded into data memory. This instruction loads an 8-bit constant into the accumulator; it cannot load a number greater than 255. In the DFDP-generated programs, the coefficients are loaded from program memory via the TBLR (table read) instruction. If the coefficients are above location 255, the linker flags a warning message:

**ADDRESS SPACE OVERFLOW FOR TAG=%%.**

The DFDP is not to blame here. But the net result is that all of the coefficients must be moved to the first program in the link list so that they will be in low memory. When we were testing just the filters, we did not see this problem because the program was small. But the full system software was larger, and therefore the overflow occurred. We read the warning message but were not able to decode it. Eventually we discovered the problem that the linker had already found but failed to communicate to us. The rather meaningless message indicated that we had tried to stuff an address with more than eight bits into a LACK instruction.

Once the system worked with the emulator, we figured we were home free. Now all we needed to do was burn the EPROM in the TMS320E17. The program was loaded into an EPROM programmer that accepts TI object files. The TMS320E17 was placed into an
Pulling the entire system together revealed many problems with the tools and their interaction with each other.

adapter that reconfigures its pins to look just like those of a 27C64 (Fig 7).

The programming went without a hitch. But when we placed the TMS320E17 into the circuit and applied power, nothing happened. Naturally, we checked the power supply and the clock first. They looked fine. Our inclination at that point was to pull out the logic analyzer and see what the system was doing. But because of this chip’s configuration, we couldn’t have access to the address, data, and control signals, so a logic analyzer was useless.

Another call to the factory revealed the method that TI uses to program the TMS320E17. First, it loads the TI object file into the XDS emulator. Then, it loads the same file, without code modification, back up to the PC in Intel Hex format. The Intel Hex is then sent to a PROM programmer to program the device.

We followed that example and used the XDS emulator as a file translator. It worked, but during the operation we found that the reason our programmer did not work was that, in this instance, it couldn’t read the TI object file. We found a C program that converts TI object files to Intel Hex, but we didn’t have an opportunity to investigate it.

The final test of the system consisted of subjecting it to different frequencies and checking the response. We were not able to test the range-measurement function because we lacked the necessary interrogation equipment. But when we used the appropriate tone, it did respond as designed.

The beauty of the DSP approach is the ease with which the entire system can be changed. For example, we found the transponder could be confused when reacting to just a single tone. Therefore, we designed in three different filters, each of which must apply a tone to the detector before a response can occur. This modification was a very easy one to make with the DSP approach, especially with DFDP creating the coefficients and the filter code. With the analog approach, we would have had to restart from nothing, and the size of the design would have increased almost threefold.

The cost of the DSP approach based on the TMS320E17 ($100) and the TLC2040 (about $50) was about $200. If production costs were more important than the nonrecurring engineering costs, we would have had another option. We could have used the mask-programmable TMS32C017 at $32 (5000) and the TCM29C18 codec at about $4 for a system cost of about $50—a figure competitive with the analog solution.

We also found that it’s possible to use DSP tools to create a working device with little knowledge of DSP algorithms. In terms of the project as a whole, the DSP part of it produced only minor problems in the use of these tools. But remember, you must also be experienced in the development of µP systems to be able to use them.

LISTING 1

****************************************************************************************************************************
* XPNDR - Transponder
*
* This program performs the Transponder function. After initialization, it will
* wait for a trigger signal. After receiving
* the trigger signal, it will respond by first
* waiting the delay time, then it will create
* the response signal, and finally it will delay for a dead band time.
*
* The program for the transponder consists of
* this main module, the filter module and the
* sine wave generator module. The filter module
* is used exactly as created by DFDP with the
* modification to include the coefficients in
* this module. The sine wave generator module
* is a slightly modified version of the one

EDN September 3, 1987
### LISTING 1 (Continued)

* listed in the "Precision Digital Sine-Wave Generation" application report available * from Texas Instruments.

---

<table>
<thead>
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<tr>
<td>REF FIIIR1</td>
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<tr>
<td>REF IIR1</td>
</tr>
<tr>
<td>REF GSINE</td>
</tr>
<tr>
<td>REF ISINE</td>
</tr>
<tr>
<td>REF SINE</td>
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| DEF VIIR1  | filter 1 variable |
| DEF FTTT   | temp value for all filters |
| DEF DELTA  | gsine phase increment |
| DEF SINA   | gsine amplitude |
| DEF COEF   | coefficients for IIR1 |

*VARIABLES

| INPUT     | EQU >0000 | 16 bit input from AIC |
|           |           |                      |
| HIINP     | EQU >0001 | MS byte of input     |
| LOINP     | EQU >0002 | LS byte of input     |
| HIOUT     | EQU >0003 | MS byte of output    |
| LOOUT     | EQU >0004 | LS byte of output    |
| ONE       | EQU >0005 | integer 1 (for INC and DEC) |
| SET1      | EQU >0006 | LOCR point to HICR   |
| SET2      | EQU >0007 | HICR setup           |
| SET3      | EQU >0008 | LOCR setup           |
| FILTT     | EQU >0009 | temp value for filters |
| MASK      | EQU >000A | mask for value to AIC |
| OUTPUT    | EQU >000B | 16 bit output        |
| THRES     | EQU >000C | threshold            |
| STATE     | EQU >000D | state xpnrd is presently in |
| DCOUNT    | EQU >000E | countdown for delay  |
| PCOUNT    | EQU >000F | countdown for pulse  |
| BCOUNT    | EQU >0010 | countdown for deadband |
| LEDDN     | EQU >0011 | output to LOCR for LED on |
| LEDOFF    | EQU >0012 | output to LOCR for LED off |
| VIIR1     | EQU >0013 | filter 1 variable    |
| SINA      | EQU >0014 | sine amplitude       |
| DELTA     | EQU >0015 | Delta phase          |

*I/O PORTS

| LOCR      | EQU >0  | low command register |
| HICR      | EQU >1  | high command register |
| SERIAL    | EQU >1  | serial I/O port |

*CONSTANTS

| PAGE      | EQU >0  | data page |
| FILTRM    | EQU >0  | filter state |
| DELAYM    | EQU >1  | delay state  |
| PULSEM    | EQU >2  | pulse state  |
| DEADM     | EQU >3  | deadband state |

<table>
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<tr>
<th>PSEG</th>
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<tbody>
<tr>
<td>START B INIT *branch over data values to INIT</td>
</tr>
<tr>
<td>INT B INT *not using interrupt</td>
</tr>
</tbody>
</table>

*INIT DATA

| SET     | DATA >B300, >000F, >BA00 | command regs |
| SETM    | DATA >FFFC | mask |
| SETT    | DATA >400  | threshold |

Continued on pg 146
LISTING 1 (Continued)

SETLDN DATA >BE00 *ledon
SETLOF DATA >BA00 *ledoff
DSET DATA 4000 *delay count, .5 sec
FSET DATA 402 *pulse count, 50 cycles
BSET DATA 8000 *deadband count, 1 sec
SETDLT DATA >1000 *delta phase, 965 Hz

COEF
* COEFFICIENT INITIALIZATION STORAGE AREA
* from DFDP IIR1 program
* had to be here for LACK to work
* during initialization
* SECOND-ORDER SECTION # 01
*
DATA 17982 *B0
DATA -17982 *B2
DATA 29999 *A1
DATA -32238 *A2
*
SECOND-ORDER SECTION # 02
*
DATA 9223 *B0
DATA -16678 *B1
DATA 9223 *B2
DATA 29991 *A1
DATA -32512 *A2
*
SECOND-ORDER SECTION # 03
*
DATA 12714 *B0
DATA -23845 *B1
DATA 12714 *B2
DATA 30241 *A1
DATA -32523 *A2
*
************************************************************
* * *
INIT Initialization Routine
Set up the TMS320E17 for operation
************************************************************
INIT DINT *disable interrupts
LDPK PAGE *set DP to page
SOVM 01 *set overflow mode
LACK ONE *set to 1 for INC and DEC
LARP 00 *set ARP to 0
LACK SET *point to beginning of init data
TBLR SET1 *set SET1
ADD ONE, O *INC pointer
TBLR SET2 *set SET2
ADD ONE, O *INC pointer
TBLR SET3 *set SET3
ADD ONE, O *INC pointer
TBLR MASK *set MASK
ADD ONE, O *INC pointer
TBLR THRES *set THRES
ADD ONE, O *INC pointer
TBLR LEDON *set LEDON
ADD ONE, O *INC pointer
TBLR LEDOFF *set LEDOFF
ADD ONE, O *INC pointer
TBLR DCOUNT *set DCOUNT
ADD ONE, O *INC pointer
TBLR PCOUNT *set PCOUNT
ADD ONE, O *INC pointer
TBLR BCOUNT *set BCOUNT
ADD ONE, O *INC pointer

Continued on pg 148
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1-800-824-6706 (in CA.)
LISTING 1 (Continued)

TBLR DELTA  *set DELTA
LACK FILTRM  *start in filter state
SACL STATE  *load STATE
OUT SET1,LOCR  *point to upper control reg
OUT SET2,HICR  *set upper control reg
OUT SET3,LOCR  *set lower control reg
CALL IIIIR1  *init filter 1
CALL ISINE  *init sine wave gen
B XPNDR  *done initializing, now do it

**************************************************************
*  *
*XPNDR  -  Do the dirty deed.  *
*  *
**************************************************************

XPNDR BIOZ GETIT  *wait for next sample
B XPNDR
GETIT OUT LOOUT,SERIAL  *output lower half of last
IN HIINP,SERIAL  *input upper half of new
WAIT BIOZ WAIT  *wait for rest of sample
IN LOINP,SERIAL  *input lower half of new
LAC HIINP,8
ADD LOINP  *build new into 16 bit
SACL INPUT  *save it for filter input

*  LAC STATE  *determine present STATE
BZ FILTER  *case filter state =
SUB ONE  *0, then filter
BZ DELAY  *1, then delay
SUB ONE
BZ PULSE  *2, then pulse
B DEAD  *anything else, then dead

FILTER LAC INPUT  *get newest input
SACL VIIR1  *filter input
CALL FIIR1  *output of filter1
LAC VIIR1  *absolute value of filter1
ABS SUB THRES
BLZ FDONE  *IF abs filter1 < threshold
*THEN done
LACK DELAYM  *ELSE trigger detected
SACL STATE  *set STATE to delay
OUT LEDON,LOCR  *turn on LED
FDONE B SMPDON  *done with filter

DELAY LAC DCOUNT  *get Dcount
SUB ONE  *decrement Dcount
SACL DCOUNT
BGZ DDONE  *IF Dcount > 0
THEN done
*  LACK PULSEM  *ELSE set STATE to pulse
SACL STATE
LACK DSET  * reset Dcount to Dset
TBLR DCOUNT
DDONE B SMPDON  *done with delay

PULSE LAC PCOUNT  *get Pcount
SUB ONE  *decrement Pcount

Continued on pg 150
Dialight LED indicators. For a selection that makes a noticeable difference.

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LISTING 1 (Continued)

SACL  PCOUNT
BGZ  CSINE
*L
LACK  DEADM
SACL  STATE
LACK  PSET
TBLR  PCOUNT
B  PDONE
*  branch done
CSINE  CALL  GSINE
LAC  SINA
SACL  OUTPUT
*generate next sample
PDONE  B  OUTP
*done with pulse
DEAD  LAC  BCOUNT
SUB  ONE
SACL  BCOUNT
BGZ  BDONE
*reset Pcount to Pset
*branch done
*L
LACK  FILTRM
SACL  STATE
LACK  BSET
TBLR  BCOUNT
OUT  LEDOFF,LOCR
*turn LED off
do with sequence
*B  START
*START ALL OVER AGAIN
BDONE  B  SMPDON
*done with dead
SMPDON  ZAC
SACL  OUTPUT
*set output to 0

OUTP  LAC  OUTPUT
AND  MASK
SACL  LOOUT
LAC  OUTPUT,B
SACH  HIOUT
OUT  HIOUT,SERIAL
B  XPNDR
*go back for next sample
PEND
END
Marconi has been building Signal Generators for 50 years, so it's not surprising that we offer you 40 different models and versions with a full range of modulation capabilities configured with time saving digital control from the front panel and via GPIB ... we also include a non-volatile memory for your most used settings.

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(b) 32-pin PLCC (c) 44-pin PLCC (d) 20-pin SOIC
Space saving packages:
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<td>40MHz</td>
<td>16.5MHz</td>
<td>15MHz</td>
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<tr>
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<td>72402*</td>
<td>35MHz</td>
<td>40MHz</td>
<td>16.5MHz</td>
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<td>35MHz</td>
<td>40MHz</td>
<td>15MHz</td>
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<td>64x5 CY7C404</td>
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<td>35MHz</td>
<td>40MHz</td>
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<td></td>
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<tr>
<td>64x4 MM16A413</td>
<td>72405*</td>
<td>35MHz</td>
<td>40MHz</td>
<td>15MHz</td>
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*Now available in 300 mil space saving thin sidebraze for IDT7201/02
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μP-like DSP chips

DSP, or digital signal processing, chips are now cheap enough for talking toys, yet powerful enough to rival superminicomputers. In EDN's first DSP Chip Directory, an offshoot of our traditional annual μP/μC Chip Directory, we concentrate on μP-like DSP devices.

Robert H Cushman, Special Features Editor

After struggling for 10 years, DSP versions of μPs are seeing mainstream use. Prices are coming down, reaching the $10 level—even $5 is being quoted for very high volumes. Also, the chips' high-speed number-crunching abilities are exceeding the μPs' capabilities and even those of some superminicomputers.

What is a μP-like DSP chip?

The phrase μP-like (or μC-like) means that the chips fetch instructions from memory and execute those instructions just like any other computer; what makes a DSP μP different from ordinary microprocessors is that it can do the sum-of-products algorithms of digital signal processing at high speed. As you can see by referring to the directory listings (which begin on pg 159), DSP chips achieve this speed by single-cycle hardware multipliers and Harvard architectures where the instructions are fetched in parallel with the data.

As you study the directory entries, you'll also notice other DSP features, like the ability to simultaneously feed data to each side of the multiplier, that further help the chips to do sum-of-products algorithms. Some are also capable of bit-reversal addressing, which aids in performing the FFT computations often used in digital signal processing.

This year's directory doesn't include certain programmable DSP chips because they seem too narrowly specialized. Examples of these are the NEC 7281 Data Flow, the Zoran 34161 FFT, and the NCR GAPP. Chips such as these may fall into the μP-like category, but they are hardly flexible enough for general use—in contrast to the DSP chips we have included. In fact, some designers perceive some of the newer DSP chips as being so μP-like that they are using them in lieu of general-purpose μPs. For instance, they are suitable for use as controllers in servo systems where users want to be able to rapidly compute servo equalization (a form of filtering). The advantage here is that the chips possess the speed to handle and coordinate multiple servo loops and have the computational ability to do performance analysis for sophisticated adaptive-control schemes.

As far as the DSP chips that we have included, you'll find it quite important to know the relative market positions of the various suppliers, especially because a lot of companies have dropped out. Overall, the TI 320 family leads the pack. It is an acknowledged fact that TI has some two-thirds of the main 16-bit fixed-point market. NEC follows, thanks to its head start with the little 28-pin 7720. Then comes AT&T, which just might finally have a winner because of its early start in 32-bit floating-point arithmetic. Next is Motorola with its 24-bit fixed-point math chip; competitors ruefully acknowledge this product will do well "just because it's from Motorola."

After these large semiconductor suppliers comes Analog Devices (who believes it has made a good start in some niche markets). Then the market positions become more difficult to determine, though some of the overseas suppliers may have access to large consumer and entertainment markets.

National Semiconductor discontinued its plans for its 32900 DSP while we were preparing the directory (amid protestations that they weren't). A large number
of DSP pioneers have dropped by the wayside: Intel with its 2920, AMI with its 2811, ITT with its UDPI-01, and STC (England) with its DSP-128. Many of these early birds had hoped that OEM designers would adopt DSP chips as fast as OEMs picked up µPs back in the 70s. They became discouraged when they saw how long it would be before volume orders began to come in and how much support was needed by OEM designers.

Nevertheless, some of the past dropouts may be re-enlisting. A TI source tells us that Intel may come back in as a second source for the 320 family. Also, as you can see in the directory, ITT has come back with the UDPC version of its entertainment-oriented DSP chip.

Manufacturers of µP-like DSP chips
For more information on µP-like DSP chips such as those included in this directory, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. The abbreviations in parentheses after some companies are those used in the directory.

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<td>Analog Devices Inc</td>
<td>Digital Signal Processing Div</td>
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<td>AT&amp;T</td>
<td>555 Union Blvd</td>
<td>(215) 428-7317</td>
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<td>3800 Homestead Rd</td>
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<td>3055 Bowers Ave</td>
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References

1. Cushman, Robert H., "EDN's Thirteenth Annual µP/µC Chip Directory," EDN, November 27, 1986, pg 102. The pages on DSP chips that you’ll find at the end of this and previous µP/µC directories from now on will be part of EDN’s DSP directories.

2. “Systolic Arrays,” Computer, July 1987. This special issue of IEEE magazine is devoted to systolic arrays and wavefront computers. It includes eight articles, some of which discuss the use of the DSP chips covered in this directory as building blocks for systolic and wavefront computers.

Non-µP-like DSPs do exist

Although EDN’s DSP directory concentrates on µP-like DSP chips, you should be aware that there is a relatively new and growing class of “non-µP-like” DSPs. These chips perform the sum-of-products and other DSP algorithms in hardware.

Their advantage is that they can handle still higher signal bandwidths—even video. They gain their speed by parallelising the hardware. Instead of software using one multiplier sequentially, as in the case of µP-like DSP chips, a number of multipliers might be used simultaneously in parallel.

A FIR filter, for instance, could have a multiplier for each tap so that each signal sample could be completely operated on in just one clock time. This type of operation could allow perhaps a hundredfold increase in bandwidth. The drawback is that non-µP-like chips are limited in purpose, having none of the open-ended flexibility of a µP-like, software-programmable machine.

Examples of algorithms-in-hardware DSP chips that variously do FIR or IIR (infinite impulse response) filters include the Zoran 33XXX, Calmos/Intersil 29C128, NCR 45CF8, Fairchild FSP-100, Inmos A-100, RCA CDSP-100, Gould/AMI 614381, Motorola 56200, and Kurzweil KSC 2408.
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*ALSO INCLUDES DESCRIPTION OF THE UNNAMED 24-BIT FLOATING-POINT DEVICE FROM FUJITSU.
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16. BC, AB, SK, MB
    Interworld Electronics & Computer Industries, Ltd.
    604-984-4171
17. ON, PQ
    Electroalert
    416-475-6730
7720 FAMILY

AVAILABILITY: Original 7720 devices have been in production many years; production is now done in US. Samples for the new 77C25 are scheduled for the 3rd qtr of '87. EPROM version (also in CMOS) is promised for the 4th qtr of '87. ROM code acceptance will begin in the 3rd qtr of '87. 77C25 will also be produced in the US starting late in the 4th qtr of '87.

COST: The NMOS 7720A is around $12. The CMOS 77C20A costs approximately $15. The EPROM 77P20 sells for around $25. The 77C25 will be $20 in 1k qty and will drop to $15 in high volumes. The EPROM 77P25 will cost approximately $40.

SECOND SOURCE: Gould (RAM) for earlier 7720 (not 7720A); Oki for 77C20 (not 77C20A). Silicon Systems has license for Oki 77C20D. None announced for 77C25.

Description: The first successful DSP µC, the 7720 should also be the lowest cost because it comes in a much smaller package than the rest of the DSP chips in this directory—just 28-pins—and has the longest production history. The new member—the 77C25—operates at twice the speed (122-nsec instruction cycle) and has four times the instruction ROM (2k x 24) and twice the data RAM (256 x 16). It is drop-in compatible with previous members of 7720 family because it has same pinout and same 8-MHz clock.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

For ALU: add, logicals, decrement, shift, and complement. Multiplication done automatically in the separate multiplier every instruction cycle.

II—DATA-MOVEMENT INSTRUCTIONS

Source/destination addressing; load immediate; unique row/column RAM addressing scheme provides for efficient filter algorithms.

III—PROGRAM-MANIPULATION INSTR


IV—PROGRAM-STATUS-MANIP INSTR

Each of the two accumulators has a duplicate set of flags relating to ALU status.

Software Notes:

1. The 77C25 is software compatible with the 7720, but has enhancements such as two additional branch instructions, which can be taken care of by assembler directives (note that 77C25 instruction ROM is 1 bit wider, 24 vs 23 bits).
2. Multiple functions per each instruction (in the 7720 and nine in the 77C25).
3. Dual overflow and sign flags (in each status register for two accumulators) allow special hardware saturation register (SGN) to hold correct value for as many as three consecutive additions/subtractions for proper overflow correction in second-order filters (two additional instructions for testing and loading required).

Specification summary: Single-chip digital signal processor that can execute 16-bit sum-of-products computations in a 250-nsec instruction cycle. Split-memory architecture with instruction side fed from 512 x 23 masked ROM as addressed by program counter with 4-level subroutine/interrupt-save stack. Data side receives and delivers 8-bit digitally coded analog signals at 2-MHz shift rate and processes them in 16-bit parallel data paths and registers, storing intermediate results in 128 x 16 RAM and obtaining equation coefficients from 512 x 13 ROM. The CMOS 77C20 parts have a speed and power consumption advantage over the original NMOS parts, and the latest CMOS 77C25 parts have a speed advantage over the earlier 77C20A CMOS parts (see table). The 77C25 has four times the instruction ROM (2k x 24) and two times the data RAM and ROM (256 x 16) and 1k x (16)). 77C25 instruction cycle is twice as fast (122 vs 244 nsec). 77C25 power consumption is the same 40 mA max as the 77C20, and there is a 50% power-down mode. Both 77C20 and 77C25 are in CMOS, but 77C25 is in 1.6 µm and 77C20 is in 2.4 µm (see table). Package options include 28-pin DIP (plastic and ceramic) and 44-pin PLCC.

EDN September 3, 1987
UDPC 01

AVAILABILITY: Now, but only in high volume as masked-ROM part.
COST: About $10 in large volume.
SECOND SOURCE: None, but in addition to its West German factory, ITT has brought up a second semiconductor plant in the US in Shelton, CT.

Description: Real-time signal processor for the audio frequency range. Has a dual-bus structure and uses pipelined program execution. The basic multiply-and-add for signal processing is carried out in two cycles of 100 nsec each. The 16-bit data multiplied by 10-bit coefficient is added to 20-bit accumulator, using signed 2's-complement arithmetic.

16/10-BIT FIXED-POINT CMOS DSP

Intermetall GmbH
Box 840
D-7800 Freiburg
West Germany
Phone (0761) 5170

In USA:
ITT Semiconductors
55 Merrimack St
Lawrence, MA 01843
Phone (617) 688-1881

Status: A cut-down version of the UDPI that was in EDN's µP directory in 1984 and 1985. UDPC is a spinoff of a high-volume part developed for automotive customers to use in digitally implemented car radios. By reducing the architecture to a bare minimum—just 10 bits for coefficients—and by eliminating parallel data I/O and by shrinking the geometry to 1.5 µm, ITT says it has been able to get the volume price down to the $10 range. Intermetall, the West German division of ITT that developed part, has been a pioneer in applying DSP to consumer TV and audio.

HARDWARE CHARACTERISTICS SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS
Arithmetic, including multiply (signed fixed-point 2's-complement) and add (or subtract)
Also absolute value, complement, increment, shifts, negation, round off and logicals
II—DATA-MOVEMENT INSTRUCTIONS
Extensive data-movement instructions, individually covering almost every possible movement within architecture
Control of address and loop counters
I/O instructions for three different interfaces
III—PROGRAM-MANIPULATION INSTR
Jumps and conditional jumps (based on status bits and test pins)
Subroutine calls and return (3-level program-counter stack)
IV—PROGRAM-STATUS-MANIP INSTR
Seven status bits (three user defined) and instructions to set and reset each. Bits for selection of overflow and automatic rounding modes

Software Notes:
1. Instruction cycle is 100 nsec, but many instructions take two cycles.
2. DSP multiply-and-accumulate instructions are carried out in 200 nsec, including the data change of all registers involved, even for sequences of different multiply-and-add instructions.
3. Can move the accumulator into the 12-bit DCO (clock control register) for implementing PLLs (i.e., fine-tuning clock to synchronize to external process).

Specification summary: Harvard-architecture DSP µP with instructions executed in 100 nsec. Signed 2's-complement arithmetic. Booth’s algorithm, 16×10=20, multiply in two cycles or 200 nsec (including add, fetch, and move instructions). 20-bit accumulator. Two data buses and pipelining. 1k×15-bit program ROM. 160×16-bit data RAM. Two coefficient stores: 128×10-bit ROM and 72×10-bit RAM. Two separate serial I/Os: fast (to 5M bps) asynchronous 16 bit, and slow 10 bit (to slave peripherals). 1.5-µm CMOS, double metal, consuming 100 mW max at full speed. 5V supply. TTL I/O levels. Packaged in 44-pin plastic quad, J bend.

HARDWARE SUPPORT SOFTWARE

Evaluation board ($500). PC-based in-circuit emulation system ($1000). Consists of board-carrying UDPC emulation chip (along with fast PROMs that store a sample demonstration program) and an interface card that plugs into PC. There is also associated menu-driven software. General manual; only 30 pages, but it’s concise.

Cross assemblers: VAX-based ($200) and PC/AT-based ($100). Simulators: VAX-based ($200) and PC/AT-based ($100). These tools are written in Fortran-77. Software supplied with in-circuit-emulation board written in Turbo-Pascal.

EDN September 3, 1987
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Like proud parents, we love to talk about the family.

TELEDYNE RELAYS
Innovations In Switching Technology
320 DSP FAMILY

AVAILABILITY: Now for 1st- and 2nd-generation parts (see table) up to 320C25 at 40 MHz.

COST: In 100 qty: 1st-generation parts, $11 to $30; 2nd-generation parts, $75. In very high volume: 1st-generation parts going down to $5.

SECOND SOURCE: General Instrument for 1st-generation 32010 and 320C10, with TI also sole prime source on EEPROM 320EE12. TI is negotiating with a large US semiconductor manufacturer for 2nd- and 3rd-generation parts. (Meanwhile, TI says users are assured of a continuing supply because TI “front ends” parts in Europe and Japan as well as in the U.S.)

Description: This was the first DSP to combine the familiar µP architecture with a 1-cycle multiplier so it could do DSP-type sum-of-product algorithms fast enough to handle digitized audio-bandwidth analog signals in real time. The family has by now been expanded to include 16 variations, most of which are enhancements of the original 32010. Hardware and software compatibility has been maintained so that most models will, to some extent, drop into previous sockets and run previous software.

HARDWARE

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320C30 (T1) 50 24 8 UNLIM (BY SOFTWARE) 4x32/16 EXPANDABLE TO 16M 10x32/16 EXPANDABLE TO 16M 10µm CMOS 80-PIN FPP 1QTR 188 $40-800 HIGH VOL 188

320EE12 (T1) 195 16 0 4 | 25kx16 | 2.0µm CMOS 44-PIN PLCC | $100 |

320EE12 (T2) 195 16 0 4 | 25kx16 | 2.0µm CMOS 44-PIN PLCC | $100 |

16-BIT FIXED-POINT

NMOS AND CMOS DSP

Texas Instruments Inc

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Box 1443, M/S 737 Houston, TX 77001

Phone (713) 274-2320

For Military Version:

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Military Products

Box 6448, MS 3028

Midland, TX 79711

Phone (915) 561-7150

Status: The 320 family is by far the most successful of the µP-like DSPs: It is generally acknowledged to have approximately 70% of the market. TI got a head start when it introduced the 320 family in 1982, and TI has maintained its lead over the competition by backing the family with broad support and by the timely introduction of enhanced models. Most industry observers—including competitors—agree that, at least for the basic 16-bit fixed-point DSPs, the 320 leadership position is secure. See separate directory page for information on the 320C30, the 32-bit floating-point model that TI will be introducing in 1988.

CHARACTERISTICS

I—DATA-MANIPULATION INSTRUCTIONS

Add and subtract, with 0- to 15-bit simultaneous shift option. Multiply and conditional subtract (to assist divide), logicals. On 320C20: floating-point assist and “square-and-add” instructions.

On 320C25: carry bit with multiprecision arithmetic support and unsigned multiply instructions. Also adaptive filtering instructions.

II—DATA-MOVEMENT INSTRUCTIONS

Four basic addressing modes: Direct, Indirect from AR, Indirect from AR with autoincrement or autodecrement. Also Immediate operands (13 bits on original 32010, 16 bits on later models).

On 32020: more addressing modes, full 16-bit immediates, block moves, and 1-cycle multiply/accumulate by Repeat instruction.

On 320C25: bit-reversal addressing, 8-bit immediate add and subtract.

Conditional Branches upon status bits or contents of accumulator.

Branch on I/O pin.

Call and Return (for subroutines).

Vectored interrupts.

On 32020: repeat instructions allow single instruction to be performed up to 256 times; Push and Pop instructions to allow extended nesting of subroutines and interrupts in data memory.

On 320C25: Hold mode allows processor to continue operation with on-chip memory while external memories are read/modifed.

IV—PROGRAM-STATUS-MANIP INSTR

Enable and disable interrupt.

Load and Store status: overflow, overflow mode, interrupt mode, plus data-address pointers are saved in data RAM.

Additional flags and instructions on 32020 with still more on 320C25.

SOFTWARE

Specification summary: Space limitations prevent a summary of the different specifications of the 16 variations of this family. However, the accompanying table gives a useful overview of the three main generations, from the initial NMOS 32010 through the CMOS 320C25 and ending with the floating-point 320C30. The table doesn’t cover the range of I/O variations, which now range from codec-oriented-serial to µP-oriented parallel interfaces. On-chip DMA is included to allow transparent interchanges with external world.

SUPPORT

From Ti: EVM evaluation module ($1000 for 32010). XDS box with full-speed emulation capability, which can interface to host computer such as IBM PC ($8500 for 1st-generation 320C1X, $13,500 for 2nd-generation 32020/2C5). AIB Analog Interface Board ($750) for 12-bit A/D and D/A to interface to EVM and XDS. DSP familiarization kit ($320, $220) that includes sample 320 parts, codec, and four programmed PROMs along with application software library.

From others: GI says Audix Inc (Bohemia, NY) has “MicroWorkshop,” development system that covers 32010, 320C10, and 320EE12. In addition, there are more than 40 3rd-party vendors supporting the 320 family, according to TI. Their hardware support ranges from PC add-in boards to emulators and logic analyzers. Contact TI for names.

From Ti: Basic tools such as macro assemblers/linkers ($500) and simulators ($1500). DFDP Digital Filter Design Package ($995), a menu-driven software package intended to speed design of digital filters with floating-point accuracy or fixed-point economy. SWDS Software Development System ($3000) consists of PC card, assembler/linker, and applications software library. Full Kernighan and Ritchie C compiler for 320C25 that runs on IBM PC or VAX/VMS.

From others: GI says Audix Inc (Bohemia, NY) MicroWorkshop has editor/compiler/test software for 32010, 320C10, and 320EE12. In addition, TI says more than 40 3rd-party vendors have crossassemblers, simulators, high-level language compilers, etc for 320 family.
68930

**AVAILABILITY:** Now for ROMless 68931 and 12 to 16 weeks after receiving customer code for masked-ROM 68930.

**COST:** $49 for 68930 and $95 for 68931 in 1k qty.

**SECOND SOURCE:** None announced.

**Description:** Similar part to other 3rd-generation DSPs except that, so far, it's just in NMOS and has modes in which it can do complex and double precision numbers. It takes two instruction cycles for these special modes. In the complex modes, it follows a 16-bit real cycle with a 16-bit imaginary cycle. In double-word precision, it concatenates the two 16-bit cycles.

**HARDWARE CHARACTERISTICS SOFTWARE**

**I—DATA-MANIPULATION INSTRUCTIONS**
Instruction field that defines operations for 16 x 16 = 32 multiplier and the 16-bit ALU: add, complement, logicals, rotates, and shifts

**II—DATA-MOVEMENT INSTRUCTIONS**
Instruction fields that allow setting up and executing direct, indirect, and circular modes for addressing two data RAMs (selectively using eight pointer registers, etc)

**III—PROGRAM-MANIPULATION INSTR**
Instruction fields for setting up loop counter, etc, for addressing program ROM
Software means for expanding the 1-level hardware stack in RAM

**IV—PROGRAM-STATUS MANIP INSTR**
Instructions for 15 active bits of status register. Includes flags for device mode control and circular addressing for data RAMs. Also bits for multiplier and ALU overflow and saturation control plus special bits for complex mode.

**Software Notes:**
1. Specifications modestly say only 13 instructions, but the many fields of wide 32-bit instruction word broadens that out considerably. For example, the 5-bit ALU control field is used for 28 ALU instructions.
2. 32 branch conditions with computed “go to” on all.

**Specification summary:**
Usual Harvard architecture for DSP with mostly separate program and data sides. Program memory consists of 1250 x (32) on-chip ROM for 68930 and access to 64k x (32) off-chip space for 68931. Data memory consists of two 128 x (16) on-chip RAMs, each with its own address-generation unit. 4k external data access (with some restrictions). Also a 512 x (16) coefficient ROM (on-chip for 68930, but with equivalent external addressing for 68931). Multiplier and ALU can be programmed for three different operating modes: basic single 16-bit word, complex 16-bit real plus 16-bit imaginary words, or 16-bit plus 16-bit double-precision double words. A 160-nsec instruction cycle time for all 16-bit mode instructions except branches. The two 32-bit modes (complex numbers and double-word precision) take two instruction cycles. 1024-point FFT with looped code takes 9.65 msec. External world interface controls are based on parallel bus matched to 68800 µP and with mailbox control for synchronization. Provisions for master, slave, or DMA operation. No limit to cascading devices. Present devices fabricated in 2-µm NMOS with 1.5W power consumption. CMOS family members scheduled for '88 introduction. Packaged in 48-pin plastic DIP (68930) and 84-pin LCC (68931).

**HARDWARE SUPPORT SOFTWARE**

**SOFTWARE**

Macro crossassemblers and simulators for VAX, IBM PC, and HDS-PSI hosts. Library of DSP macro routines.

**DESCRIPTION**

**HARDWARE**

HDS-PSI development station.
EVA-PSI evaluation card with mini-assembler/debugger/monitor.
Associated modem-oriented I/O parts: 68950 receive ($20), 68951 transmit ($29), and 68952 clock generator ($11). These come in kit ($450) assembled on half-size IBM PC card with DSP and allow you to explore modems up to 9600 baud.
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Naturally, there's a lot more to know about our drives. So if you're interested, and you'd like more information, call or write today. It's a great way to go.

The original 8764 and its nonexternally expandable 87064 were joined by an enhanced floating-point device, which so closely resembled the first two that the supplier says they have a family resemblance, even though the first two are 16-bit fixed-point devices and the other two are 24-bit floating-point parts. (Note that the supplier has a full 32-bit floating-point DSP that is said to have no similarity to the 8764 family and is thus covered on a separate page in this directory.)

### HARDWARE

#### CHARACTERISTICS

1. **DATA-MANIPULATION INSTRUCTIONS**
   - Multiply and divide as well as add and subtract, etc.
   - Some logicals and some shifting ability

2. **DATA-MOVEMENT INSTRUCTIONS**
   - Each of two 128 x 16-bit on-chip RAMs has own independent address calculation arithmetic
   - Virtual shift to implement Z^-1 delay operator is helpful in doing DSP equations

3. **PROGRAM-MANIPULATION INSTR**
   - Conditional and unconditional jumps based on flags

4. **PROGRAM-STATUS-MANIP INSTR**
   - ROM can be used for coefficient table (crossover between separate sides of Harvard architecture)

5. **VIRTUAL-PRGRAM-STATUS-MANIP INSTR**
   - New software tools "up to US OEM standards" such as software simulators promised for floating-point enhanced versions. Although initial tools, such as assembler, will come from Japan, supplier will be contracting with US 3rd parties for additional tools such as a software simulator.

### SUPPORT

Assembler and simulator for IBM PC ($285) and VAX/Linux and VAX/VMS ($500). Programming manual (March '84) and instruction set manual (edition 1.1, March '84) and new approximately 50-page application manual.

Note: Original Software Development Tool Kit (MB87902) consisting of cross assembler (ASM64) to run on Fujitsu FM-16S personal computer (CP/M-86), the evaluation board mentioned under hardware support (FDSP kit 8764), and monitor program (MON64).

New software tools "up to US OEM standards" such as software simulators promised for floating-point enhanced versions. Although initial tools, such as assembler, will come from Japan, supplier will be contracting with US 3rd parties for additional tools such as a software simulator.
ADSP 2100

**Hardware Notes:**
1. Only main chip subsystem blocks and main buses are shown. Actual chip is much more complex than indicated.
2. Note that all buses for both program and data external memories come off chip. Supplier says this allows full-speed operation with 45-nsec static RAMs.

**Description:** A μP-like 16-bit DSP chip that is to be used with external memory. The supplier says it has patterned the architecture after configurations found popular in bit-slice approaches to DSP. As result, DSP experts will probably find that the subsystem sections—the program control, the data address generation, the data crunching—have familiar features. Supplier says device shows its advantage when larger memory spaces are required, because chip is able to run full speed even when accessing data off chip. Ideally the critical software loops should be running out of on-chip cache so that the two data operands can be accessed simultaneously, one from data memory and the other from program memory.

**Hardwar e Notes:**
- Cross-software tools for VAX (VMS and Unix) and IBM PC (MS-DOS). Includes system builder for defining target hardware details, assembler, linker, and software simulator. The simulator uses the same interactive and symbolic user interface as the hardware simulator (emulator). A multuser VAX is $2850; price of a single-user IBM PC is $450 for assembler, linker, and system builder and $975 for simulator. Unix version of cross software is scheduled for the 4th qtr '87.
- Stand-alone emulator ($6500) for real-time tests of software and hardware. Connects to host μP via RS-232C. Uses same interactive and symbolic user interface as software simulator. Evaluation board scheduled for the 4th qtr '87.

**Software**

I—DATA MANIPULATION INSTRUCTIONS

Three main groups of instructions that control the operations of the multiplier/accumulator, shifter, and ALU, respectively. Most of these can be made conditional.

II—DATA MOVEMENT INSTRUCTIONS

Data can be moved flexibly between the approximately two dozen register locations on chip and between these registers and external memories. Both direct and indirect addressing are available for many of these instructions.

III—PROGRAM-MANIPULATION INSTRUCTIONS

Jump, call, and return from subroutine, return from interrupt, do until, and trap. All can be made conditional.

IV—PROGRAM-STATUS-MANIPULATION INSTRUCTIONS

A large number of status registers are maintained: 8-bit ALU status, 8-bit stack status, five bits for interrupt (plus four bits for interrupt mask). Some of these are used for determining decisions in program-manipulation instructions.

V—PROGRAM MODE CONTROL INSTRUCTIONS

4-bit mode-control register allows software selection of desirable DSP options, such as bit reversal in addressing and saturation-mode arithmetic.

**Software notes:**
1. As is common in highly parallel DSP architectures, instructions can combine functions from groups I, II, and III. However, because instruction word is only moderately long (24 bits), only certain combinations are valid.
2. Supplier describes assembly language as “high level” because it is patterned after Fortran and C, using an algebraic-like notation, which is said to ease programming because it makes the functions being performed intuitively obvious.

**Specification summary:** Harvard-architecture μP with program and data memory off chip. There is, however, a 16 x 24-bit program-memory cache on chip that is said to be adequate for holding short routines (such as DSP inner loops). A 14-bit PC to address 16k instruction words off chip (optionally 32k) and 14-bit data address generators addressed 16k x 16 data words off chip. Access time for external memory: 45 nsec for program and 55 nsec for data. When a program loop is executing from cache both operands can be read in simultaneously—the signal data from data space and the coefficient from program space. Loop counters and special stacks are provided for “zero-overhead” execution of typical DSP recursive operations. Data-crunching section includes the three elements typical of DSP devices: a 16 x 16 x 40 multiplier, a 32-bit barrel shifter (facilitates block floating point), and a 16-bit ALU. All instructions, including compound data manipulation/data movements/program manipulation executed in 125 nsec. I/O is memory mapped, and control signals are available so a host μP can access the program memory via DMA. Fabricated in 1.5-μm CMOS with double-metal interconnect layers. Die size is 280 x 230 mils. Packaged in 100-pin ceramic PGA.
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Look at the Tek 2465A with a 17-bit Word Recognizer. It's an easy, economical scope option that makes the critical difference when you need to trigger on data to monitor digital system performance. Parallel bus information triggers your display, so you can view up to four channels of real-time information. Add standard features such as 350 MHz bandwidth, on-screen cursors, 500 ps/div time base and trigger level readout, and you have a scope made for solving tough problems in digital design!

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( ) Phone Ext

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Check Tek software development packages. They make it easy to generate automated and semiautomated test procedures, even without prior GPIB-programming experience. Use the simple, multi-

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<th>2465A</th>
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<tr>
<td>Probe Tip Bandwidth</td>
<td>350 MHz</td>
<td>350 MHz</td>
<td>350 MHz</td>
<td>350 MHz</td>
<td>150 MHz</td>
</tr>
<tr>
<td>No. of Channels</td>
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<td>4</td>
<td>4</td>
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<tr>
<td>Horizontal Accuracy</td>
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<td>2% (.001%*)</td>
<td>2% (.001%*)</td>
<td>2% (.001%*)</td>
<td>2% (.001%*)</td>
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<tr>
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<td>500 psec</td>
<td>500 psec</td>
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<tr>
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<td>2 mV/div</td>
<td>2 mV/div</td>
<td>2 mV/div</td>
<td>2 mV/div</td>
</tr>
<tr>
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<td>500 MHz</td>
<td>500 MHz</td>
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<tr>
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<td>Standard</td>
<td>Standard</td>
<td>Optional</td>
<td>Optional</td>
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<td>Counter/Timer/Trigger/Word Recognizer</td>
<td>Standard</td>
<td>Standard</td>
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<td>Optional</td>
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</tr>
<tr>
<td>Digital Multimeter</td>
<td>Standard</td>
<td>Standard</td>
<td>Not Available</td>
<td>Optional</td>
<td>Optional</td>
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<td>Video Trigger</td>
<td>Standard</td>
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<td>2</td>
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<td>Warranty</td>
<td>3 years on parts and labor, including CRT</td>
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</tbody>
</table>

*with Counter/Timer/Trigger

Get the full story! Return the reply card to Tek today. For a hands-on demonstration, call your Tek Sales Engineer.
Description: Another example of pushing DSP-oriented architecture to its logical limit. The design aim appears to be to keep the die and package size moderate (in DSP terms) for reasonable device cost. At the same time, designers wanted to achieve 3rd-generation performance (beyond 2nd-generation T1 32010), therefore, they used a very wide control word (40 bits) and dual 16-bit data paths.

Hardware Notes:
1. The 5010 is a 1-chip µC with limited 1k x 40 program ROM. Its data-side memory space can be expanded off chip.
2. The 5011 is a ROMless µP version of the 5011 that has a large 64k x 40 off-chip program memory space.

Software Notes:
1. The many fields of wide instruction word provide an orthogonal matrix of software options that are said to make OSP operation flexible and programming simple.
2. User can choose either pipelined or nonpipelined mode via software control.

Specification summary: Harvard architecture with entirely separate program and data sides. High degree of parallelism. Control side has 40-bit-wide control word that allows up to six operations to be performed simultaneously. Data side has dual 128 x 16 RAMs and dual 16-bit buses so that both operands can be presented simultaneously to 16 x 16 - 40 multiplier and 16-bit ALU. Each data RAM and an additional 512 x 16 data ROM has its own address-computation ALU. A 3-port 15 x 16 register file aids data movements and frees buses. The instruction cycle is 125 nsec (8 MIPS) for all instructions including multiply (although the one, two, or four optional levels of pipelining can mean a delay at the beginning of series of DSP instructions). Fabricated in 1.5-µm single-metal CMOS with die size approximately 312-mil sq. Packaged in 68-pin PLCC (5010) and 144-pin PGA (5011).

Software:
Crossassemblers (ASM) that run on VAX/VMS (from $1700) or IBM PC ($995). Standard macro library (LIB) covering single- and double-precision and complex arithmetic, logic, bit manipulation, initialization and I/O, and DSP functions such as FIR and IIR filters and FFTs. LIB is included in VAX ASM package but is extra for IBM PC ($995). Screen-oriented software simulators for VAX/VMS (from $1995) and IBM PC ($1995).
**PCB 5020/21 (SP-50 FAMILY)**

**AVAILABILITY:** 5021 samples, 1st qtr ‘88; 5020 production, 3rd qtr ‘88.
**COST:** $250 for 5021 samples; $25 for 5020 (1k qty).
**SECOND SOURCE:** None announced.

**Description:** This pair, new to the supplier’s SP-50 family, has been tailored for the hi-fi-audio market. It has a wide 24-bit main data path to achieve dynamic range, but a narrow 12-bit filter coefficient path to economize on-chip area. It has an unusual feature of access to an external dynamic RAM for implementing reverberation delays.

---

**24/12-BIT FIXED-POINT CMOS DSP**

**Philips**
Elcoma Corp Center  
Box 218  
5600 MD Eindhoven,  
The Netherlands  
Phone (31) 40 724223

**Signetics Corp**
Box 3409  
Sunnyvale, CA 94086  
Phone (408) 991-2000

**Status:** First announced at the June ‘87 Chicago Consumer Electronics Conference, these parts are an example of DSPs being targeted towards a specialized high-volume market. The initial customer was an automotive manufacturer who wanted a car stereo that could be programmed to have the delays of various concert halls (which is why the chips have access to delay dynamic RAMs). Philips has also been using digital techniques in its compact-disk (CD) players. Despite their tailoring, the devices are sufficiently general so they can be used in other applications—for example, quality speech processing.

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**HARDWARE CHARACTERISTICS SOFTWARE**

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<tr>
<th>PROGRAM SIDE</th>
<th>DATA SIDE</th>
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<tr>
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<tr>
<td><strong>ADDR</strong></td>
<td><strong>DATA</strong></td>
</tr>
<tr>
<td><strong>TO HOST µP/µC</strong></td>
<td><strong>TO REVERB RAM</strong></td>
</tr>
</tbody>
</table>

**Hardware Notes:**

1. 5020 is a 1-chip DSP with on-chip program ROM (512×32) and coefficient ROM (128×12).
2. 5021 is a ROMless version for prototyping.

**Specification summary:** Usual Harvard DSP architecture with separate program and data sides. Program words of 32 bits allow as many as six operations to be performed in parallel. 5020 has 512×(32) on-chip program ROM. On ROMless 5021, this is simulated by external memory through an “emulator interface.” Dual 128×(24) data RAMs, A and B, each with its own address-computation ALU. B has I/O link with µP host for coefficient update. Associated with this B RAM is a 128×(12) space ROM for storing permanent coefficients. On the ROMless 5021, this is emulated by an additional 128×(12) RAM page. The multiplier/accumulator is 12×24=40 bits, the bits being sized to required precision for hi-fi audio coefficients and data. Two separate data buses—24 and 24/12 bits—to allow full use of multiplier/accumulator. A 4-word register file stores intermediate results. Instruction cycle time is 88 nsec (11.3-MHz clock). Serial data interfaces and associated control bus are after supplier’s proprietary IIS and IIC standards, so are matched to companion audio-system support ICs (like A/D and D/A converters and host µP or µC). Also a parallel-I/O interface for access to external dynamic-RAM memory so user can implement audio delay effects like reverberation, compression, etc. Fabricated in 1.5-µm CMOS single metal.

**Real-time emulator (supplier says the SP-50 support tools will be adapted to include 5020/21. Supplier is introducing associated parts, which might be used in conjunction with 5020 in audio systems. These parts and their 10k-volume prices are: the 7220 digital filter, $5.50; the 7320 stereo D/A, $9.50; the 7250 preprogrammed DSP µP, $19.50; and the 5022/23 stereo A/D and quad D/A, $25/set.

**To be available:** crossassembler, simulator, and software application support, including standard audio algorithms.
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**WE DSP16**

**AVAILABILITY:** Samples now; production, 4th qtr '87.  
**COST:** $96 for 75 nsec and $113 for 55 nsec (100 qty); $60 for 75 nsec and $80 for 55 nsec in 10k volume. Volume prices in '88 may drop to the $30 to $40 level.  
**SECOND SOURCE:** Being actively pursued, supplier says.

**Description:** Achieves speed and economy through economical architecture and 1.0-µm feature size. The two sides of the 16×16=32 multiplier are fed in parallel from the data RAM (variables) and the program ROM (coefficients). The arithmetic section that follows the multiplier can accumulate data to 36 bits. Because of its fairly simple architecture and fine 1.0-µm feature size, the chip size is only 236×335 mils, which is economically small, as DSP chips go.

---

**16-BIT FIXED-POINT CMOS DSP**

**AT&T**  
555 Union Blvd  
Allentown, PA 18103  
Phone (215) 439-7317

**Status:** AT&T has used its historic head start in DSP to produce a very competitive 16-bit integer device. AT&T announced a similar device in 1978, but it has only been used internally. This device has also been designed into internal AT&T applications, which should assure it production volumes in the many tens of thousands in '88, according to the supplier. Supplier considers TI 320C25 the main competition. DSP16's strong point is its speed; its main drawback is lack of off-chip expansion for data memory.

---

**HARDWARE CHARACTERISTICS SOFTWARE**

I—DATA-MANIPULATION INSTRUCTIONS

Instructions for 16×16=32 multiplier and the 36-bit ALU. Logicals, bit test, and shifts. Software control of saturation. (Supplier says program has control of three stages of pipelining: data fetch, multiplication, and accumulation)

II—DATA-MOVEMENT INSTRUCTIONS

Commands for register indirect addressing of data RAM with post modification of registers using associated increment registers. Can implement circular buffers in RAM suitable for DSP via modulo addressing.

III—PROGRAM-MANIPULATION INSTRUCTIONS

Single “do” instruction can evolve 127-long loops in the 15 word on-chip cache. “Redo” instruction repeats do sequence. Standard gotos, conditional branches, and subroutine calls. Push and pop

IV—PROGRAM-STATUS MANIP INSTRUCTIONS

Processor status register has fields in which bits indicate conditions in data-manipulation section. These include flags for logical and mathematical overflow and state of sign bits in each of two accumulators.

**Software Notes:**

1. Instruction syntax patterned after C language, having equation-like form.
2. Nesting for subroutines and interrupts is one level by hardware with additional levels via software.

**Specification summary:** Usual Harvard architecture but with provisions for obtaining DSP coefficients from program ROM. Program memory is 2k×(16) on-chip ROM with direct full-speed is access to 64k×(16) off-chip expansion space. Data memory is 512×(16)-bit on-chip RAM with no direct high-speed access to off-chip expansion space. Both program ROM and data RAM have their own address-generation ALUs. Data manipulation by 16×16=32-bit multiplier and 36-bit ALU with two accumulators. Instruction cycle time is 55 or 75 nsec. Parallel interface to 16-bit-µP bus (can be used as two buses for full duplex to 8-bit bus). Supports 145M-bps data rate. Serial I/O transmits or receives 8- or 16-bit words at 10M bps. Can be used as multiprocessor interface for as many as eight DSP16s or as TDM interface to eight codecs. Fabricated in 1.0-µm static CMOS, double-metal. It has 500 mW max operating power consumption and is packaged in 84-pin PLCCs and CLCCs.

---

**HARDWARE SUPPORT SOFTWARE**

DSP16-DS development-system "box" for real-time applications evaluation with in-circuit emulation ($3000). The development system is compatible with software library. Up to 16 development systems can be cascaded for multiprocessor applications.

DSP16-SL software library contains an assembler and software simulator. Library is available to run on most popular development computers and their operating systems including MS-DOS ($500), Unix ($1000) and VMS ($1500).  
Assembler source is similar to C language, with usual features of labels, symbols, commands, etc. A C preprocessor can be used for conditional assembly and to improve program readability.

---

EDN September 3, 1987
DSP 56000 FAMILY

AVAILABILITY: RAM-based 56001 available now. ROM-based 56000 will follow in the 3rd qtr '87.

COST: $500 for RAM-based 56001 samples. There will be a nonrecurring mask charge for ROM-based 56000.

SECOND SOURCE: None announced.

Description: A 24-bit, fixed-point, arithmetic DSP family. First members of this CMOS, mostly single-chip family are a ROM-based model (56000) that requires factory programming and a RAM-based model (56001) that is unusual because the program-memory space is in on-chip RAM. This is first DSP device to have balanced 24-bit widths for both instruction and data words. The wide words are needed for parallel control and analog precision, respectively. An unusually large assortment of on-chip peripheral functions are included on chip, after the fashion of microcontroller μCs.

Hardware Notes:
1. Diagram is for 56001 program-in-ROM version.
2. The 56000 program-in-RAM is identical except for:
   a) Program memory = 0.5k RAM.
   b) X, Y data ROMs are preprogrammed.
   c) Bootstrap ROM on-chip to load program RAM.
3. There are 18 interrupt sources, which are serviced in 200 nsec.
4. No speed penalty for single external-memory accesses.

24-BIT FIXED-POINT CMOS DSP

Motorola DSP Operation
6501 William Cannon Dr W
Austin, TX 78735
Phone (512) 440-2030

Status: Supplier says now that RAM-based 56001s are in the hands of customers, announcements of products using the 56000 family will be forthcoming by end of '87. Professional audio designers are said to like the combination of high throughput and wide word for applications like music synthesizers and voice recognition. Supplier is using die shrinks to improve the throughput: a shrink from 1.5 to 1.2 μm has boosted speed from the device's 97.5-nsec instruction cycle time last year to 75 nsec. These shrinks may also be needed to reduce the current high cost.

Hardware Notes:
- Diagram is for 56001 program-in-ROM version.
- The 56000 program-in-RAM is identical except for:
  - Program memory = 0.5k RAM.
  - X, Y data ROMs are preprogrammed.
  - Bootstrap ROM on-chip to load program RAM.
- There are 18 interrupt sources, which are serviced in 200 nsec.
- No speed penalty for single external-memory accesses.

From Motorola: Application Development System (ADS), consisting of an interface board and evaluation board (ADM) with diskette ($3000), the host is an IBM PC in which the interface board occupies one slot. Because 3rd-party DSP applications software exists for the PC and the ADS user interface is the same as the simulator user interface, the PC-ADS combination offers an algorithm-development environment as opposed to just a hardware/software development environment. The ADS is logically based on the 56001 and is available now.

From third parties: Data-acquisition and hardware accelerator boards for IBM PC.

Software Notes:
- Filter design package for IBM PC.

From Motorola: User-friendly assembler and simulator which run on IBM PC under MS-DOS ($295), on VAX under VMS, and on Sun-3 workstation under UNIX 4.2. The 56000 assembler is a relocatable assembler that supports object-code linking and macros. The 56001 simulator simulates on a clock-cycle basis as opposed to only on an instruction-cycle basis. Each of the execution subsystems is simulated individually, as are each of the on-chip peripherals. Scheduled for the 3rd qtr of '87 are a K&R C compiler and a translator that turns 1120 code into 56000 code.


From third party: Filter design package for IBM PC.
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6992

AVAILABLE: Now for 8- and 10-MHz 6992; 1st qtr ’88 for 699210 samples.
COST: $250 for 8-MHz 6992; $325 for 10-MHz 6992. High-volume price
for 699210 is projected to be $25.
SECOND SOURCE: None announced.

Description: Follows the now-established architecture for 3rd-generation
µP-like DSPs, but has a data word size that falls midway between
the 16-bit fixed-point, integer machines and the full 32-bit floating-point
machines. Designers wanted a dynamic range that would be superior to
16-bit integer machines, but did not want a chip size as large and
expensive as a full 32-bit floating-point DSP.

22-BIT FLOATING-POINT CMOS DSP
Oki Semiconductor
650 N Mary Ave
Sunnyvale, CA 94086
Phone (408) 720-1900

Status: The initial 6992, based on 2.0-µm standard cells, is said to be
fully available in speeds up to 100 nsec per instruction cycle. The more
economical 699210 will be a 1.5-µm custom design and is scheduled for
the 1st qtr ‘88. Some industry observers wonder whether Oki will
provide a competitive level of support tools and application assistance
for this device. But while Oki’s full-time support staff for 6992 in US still
consists of just one marketing and one application engineer, Oki is said
to be investing in a considerable effort in Japan to develop the support
tools that will hopefully match those provided by US DSP suppliers such as
Tl, AT&T, and Analog Devices.

I—DATA-MANIPULATION INSTRUCTIONS
22-bit floating point, 16-bit fixed point and 22-bit logicals. Conversion
between fixed and floating point. Software control of rounding and
clipping

II—DATA-MOVEMENT INSTRUCTIONS
Instructions have two data source fields to allow simultaneous feeding
of two multiplier inputs and one data destination field for result.
Addressing is via indexed pointers with separate addressing registers
and address computation logic for both data memories

III—PROGRAM-MANIPULATION INSTR
Nested looping (8-level stack) with single-instruction hardware loops.
Conditional jumps

IV—PROGRAM-STATUS-MANIP INSTR
Instructions for 10 bits of status register

Specification summary: Harvard architecture with mostly separate
program and data sides. Program memory: 6992 has 1k × 32 on-chip
ROM and access to 64k × 32 off-chip space. 699210 will have 2k × 32
on-chip ROM but no off-chip space. Data memory: 6992 has two
128 × 22-bit on-chip RAMs plus I/O to access two 64k × 22 memory
spaces off chip. 699210 will have two 512 × 22-bit on-chip RAMs and
same 64k × 22-bit off-chip space. Each of the dual data memories has its
own address-generation logic. Multiplier and ALU can be programmed
to do either 22-bit floating-point or 16-bit integer operations. The
floating-point format is 16-bit mantissa and 6-bit exponent. Perfor-
mance: 20M flops for 10-MHz 6992. A radix 2, 1024-point FFT with
looped code takes 6.9 msec. External world interface controls are
sufficient to allow the chip to operate in master, slave, or DMA mode.
6992 is fabricated in 2.0-µm CMOS double metal and designed with
standard cells. Forthcoming 699210 is being designed in 1.5-µm CMOS
double metal full custom. 6992 has 400-mW power consumption and is
packaged in 132-pin PGA. 699210 will be packaged in 84-pin PLCC or
100-pin flat pack.

Hardware Notes:
1. Diagram shows the 6992. The 699210 to have double-sized internal
memories, but won’t have external program memory. It will be in a
smaller package.
2. The I/O controls allow the 6992-family devices to be hung on standard
16-bit µP buses.

IBM-PC evaluation card ($500) for familiarization. Has external memory
that can be downloaded by PC via an included software monitor. Full-up
emulator/development box, EMU-92 ($8750), which includes 8k words
of external program memory, 8k words of external data memory, and
two FIFOs for emulating application I/O. An in-circuit emulation cable is
also included. Lower-cost single-board version of EMU-92, the EMU-
92L ($3750) that has ICE cable but less external data memory, etc.

ASM-92 assembler comes with hardware development tools. Growing
library of DSP macros covering IIR and FIR filters, adaptive filters,
matrix arithmetic (including matrix multiplications), power-series calcu-
lation of transcendental functions (sine, cosine etc), FFTs, etc.
In works: software simulator (SIM-92) for algorithm debug, etc. Available
in 3rd qtr ‘87.

In planning: high-level-language support.

EDN September 3, 1987
DSP32, DSP32-C

AVAILABILITY: In full production (being used internally in high volume by AT&T). CMOS version, 1st qtr '88.

COST: 100 qty prices in '87 for 100-pin package will be $200 for 250-nsec part and $270 for 160-nsec part. High-volume prices will be $153 and $190, respectively. Supplier says it is contemplating "dramatic" price reductions to assure leading position.

SECOND SOURCE: Being actively pursued.

Description: 32-bit floating-point NMOS DSP μP/μC with transparent normalizan after operations. Has both on-chip and off-chip memory. Has parallel (8-bit) ports and serial ports, the latter being CODEC compatible. Floating point said to be especially desirable for graphics applications, speech recognition, and large FFTs where there is danger of overflow or loss of accuracy during computations. CMOS version will probably find applications beyond DSP.

---

32-BIT FLOATING-POINT
NMOS AND CMOS DSP

AT&T
555 Union Blvd
Allentown, PA 18103
Phone (215) 439-7317 or (800) 372-2447

Status: Originally disclosed at the February '85 ISSCC, this device was the first 32-bit floating-point DSP to become real, and supplier believes it has chance to be market leader. This shouldn't be surprising, because AT&T has long been the leader in both DSP theory and practice. The NMOS part is said to be in volume use inside AT&T because it is being used in electronic switching systems. An enhanced CMOS version is still scheduled for 1988, but the availability has slipped from the 1st qtr to the 2nd qtr. The CMOS version will have more features and increased speed, as detailed below.

---

HARDWARE

CHARACTERISTICS

SOFTWARE

I—DATA-MANIPULATION INSTRUCTIONS

Instructions for the DAU, which does the main DSP multiply/accumulate computations in floating point. (Transparent normalization after operations to maintain floating-point accuracy)

II—DATA-MOVEMENT INSTRUCTIONS

Instructions for the CAU for data-address computations

III—PROGRAM-MANIPULATION INSTR

Instructions for the CAU for program-address computations

IV—PROGRAM-STATUS-MANIP INSTR

Conditions monitored include status of DAU, CAU, and I/O

Software notes:
1. Assembly-language syntax intended to resemble high-level language like C to ease task of converting DSP algorithms to code.
2. The wide instruction word has separate fields for the various categories of instructions so that more than one category can be performed during an instruction cycle.

Specification summary: 32-bit Harvard architecture with separate sections that can operate in parallel for increased throughput. On-chip program memory is 2k bytes, arranged as 512x(32). On-chip data memory is 4k bytes, arranged in two 512x(32) RAMs. Off-chip memory space 56Kx(32). Has 32-bit multiplier that can simultaneously receive inputs from two data RAMs and deliver result for addition to four 40-bit accumulators (32 bits plus eight bits to guard against overflow) all in same cycle. In addition has 16-bit fixed-point ALU for usual integer operations plus computing addresses for both program and data side of Harvard architecture. Instruction cycle is 160 nsec with 25-MHz clock. This gives 6.25M instructions per sec and 12.5M floating-point operations per sec. Serial and parallel I/O ports. Both have provisions for user-implemented DMA. Serial port is compatible with codecs. Fabricated in 1.5-μm NMOS with single metal layer. Chip size 500×250 mils. Consumes 1.7W average, 2.6W worst case. Packaged in 40-pin DIP and 100-pin PGA (need 100-pin package for external memory). CMOS DSP32-C will have double the program ROM (1Kx(32)), an additional 512x(32) RAM, and it will be expandable off chip to 16M bytes. The memory addressing will include bit-reversal for radix=2 FFTs. The arithmetic section will have single-instruction IEEE floating-point formats and both 16- and 24-bit integer operations. It will come in two speeds: 80 and 100 nsec. with the 80 nsec delivering 12.5 MIPS and 25M flops. Its I/O will interface directly to 8- and 16-bit µPs.

---

HARDWARE

SUPPORT

Software Assembler with C-language-like syntax, linker, editor, and simulator. Latter is architectural simulator with appearance of high-level language. Software tools operate on Unix V ($1000) and MS-DOS ($500) with VMS version planned. Full C compilers for both NMOS and CMOS devices are under development.
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Dept. D-100  
2355 West Chandler Blvd.  
Chandler, AZ 85226-6199

Or call GIM at (602) 963-7373 and ask for our DSP Technology Center.
**77230 FAMILY**

**AVAILABILITY:** Masked-program-ROM 77230 is in volume production, and ROM codes are being accepted. EPROM 77P230 scheduled for 4th qtr '87, Fixed-point 77220 scheduled for sampling late in 4th qtr '87. 

**COST:** Volume pricing is $60 to $100 for masked-ROM 77230, around $150 for EPROM 77P230, and $50 to $60 for fixed-point 77220.

**SECOND SOURCE:** Actively being pursued. Zilog was considered one possibility, but a Zilog source says negotiations were broken off.

**Description:** 32-bit floating-point CMOS µP/µC intended for high-precision audio-bandwidth digital signal processing and other number-crunching applications. Features a 32-bit floating-point multiplier and a 55-bit-wide ALU. The 77P230 is an EPROM version, and the 77220 is a 24-bit fixed-point "cut down" version.

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**32-BIT FLOATING-POINT AND 24-BIT FIXED-POINT CMOS DSP**

<table>
<thead>
<tr>
<th>HARDWARE</th>
<th>CHARACTERISTICS</th>
<th>SOFTWARE</th>
</tr>
</thead>
</table>

**I—DATA-MANIPULATION INSTRUCTIONS**
Floating point and fixed point add and subtract. Logicals. N-bit shift (in 47-bit barrel shifter). Data rounding and normalization. Data conversions between floating and fixed point.

**II—DATA-MOVEMENT INSTRUCTIONS**
Source register to destination register transfers. External memory access.

**III—PROGRAM-MANIPULATION INSTR**
Branch and conditional branch, with conditions based on state of ALU-driven status bits, index registers, and serial and parallel ports. Subroutine call and return. Loop counter control (decrement).

**IV—PROGRAM-STATUS-MANIP INSTR**
Operations on PSW, which has extensive condition-indicating and control bits.

**Software Notes:**
1. Wide (32-bit) instruction word has a number of fields, each pertaining to a different class of operations. This allows software to make use of parallel Harvard architecture.
2. The 77220 has no floating-point instructions.

**Specification summary:** 32-bit floating-point DSP-oriented, Harvard split-memory architecture with both on-chip and off-chip program and data memories. Program memory is 2k x 32-bits on chip and 4k x 32-bits off chip. Data memory is composed of a 1k x 32 RAM and 1k x 32 ROM on chip and 8k x 32 bits off chip. The 32-bit program instruction word is divided into multiple fields for simultaneous control of data manipulation, data movement, and program manipulation. The 32-bit data word is divided into 24-bit mantissa and 8-bit exponent, but the option for 24-bit fixed-point operation is also provided. Both inputs of 32-bit floating-point multiplier can be fed simultaneously from dual data memories. The output can be directed to either main bus or to a 47-bit barrel shifter and then on to a 55-bit-wide ALU (8-bit exponent added), and eight 55-bit working registers. All instructions, including multiply, execute in one 150-nsec cycle. 32-bit parallel I/O and 4-MHz serial I/O. Fabricated in 1-µm CMOS, consuming 1.2W max power (1.0W typical). Packaged in 68-pin PGA. The 77220 is hardware and software compatible sub set, with just 24-bit fixed point and one-half amount of data RAM for lower cost.

---

**Evakit-77230 full-speed emulator ($8500), which connects to IBM PC or other host, available now. Has probe for connecting to user’s target system. Can also connect to PROM writer. Features include on-line assembly/disassembly of instructions, multiple breakpoints, look-back trace, etc. PC-based evaluation board ($900) containing preprogrammed 77230 with many callable DSP routines. Package includes assembler software.**

**Relocatable assembler, librarian, linker, object converter package for MS-DOS and CP/M-86 systems ($500), available now. VAX/VMS relocatable assembler ($1600) is available now; a VAX/Unix version is scheduled for 2nd qtr '87. Simulator that runs on VAX/VMS ($1800), with VAX/Unix version to follow in the 2nd qtr '87. Application library containing DSP modules is now available. Supplier says 3rd-party support is on way.**
320C30

**AVAILABILITY:** 1st half '87 for 320C30 (33 MHz); now for software tools; 1st qtr '88 for hardware tools.

**COST:** $40 to $60 in high volume. Supplier plans aggressive pricing compared to other floating-point DSPs.

**SECOND SOURCE:** None announced, but supplier says its policy is to obtain second sourcing for 320 family. Says current candidate for 2nd- and 3rd-generation family members is not GI, who is presently second source for 1st-generation, but “one of the major US semiconductor houses,” possibly Intel.

**Description:** The 3rd-generation member of 320 DSP family, the C30 provides significant improvements in features compared with previous 320 generations. The 320C20 has 32-bit floating-point math vs 16-bit fixed-point, 60-ns instruction cycle vs 160 to 200 nsec., a 16M x 32 total memory space vs 4k x 16 to 128k x 16. These computing enhancements are matched by equally significant jumps in I/O capability. The 320C30 has two 32-bit parallel and two 8M-bps serial ports, plus on-chip DMA to allow their concurrent use. Much of this will be possible because it is fabricated in finer-geometry 1.0-µm CMOS vs 1.8-µm CMOS or 2.4-µm NMOS. Still, chip size will be large—over 400 mils on a side being needed to hold its 700k transistors. (For overview of 320 family, see the table in directory entry for fixed-point 320 family members.)

---

**HARDWARE CHARACTERISTICS**

**PROGRAM SIDE**

- RAM 0 16k (32)
- ROM 0 4k (16)
- CACHE 64k (32)
- DP 32
- other reg 8 (32)
- ADDR (HEX 8-16)
- ALU
- BARREL
- SHIFT
- DMA
- TIMER 0,1
- INTERRUPTS
- CONTROL
- PARALLEL I/O
- SERIAL 0,1
- PERIPHERAL

---

**DATA SIDE**

- RAM 1 16k (32)
- ADDR (HEX 8-16)
- ALU
- BARREL
- SHIFT
- DMA
- TIMER 0,1
- INTERRUPTS
- CONTROL
- PARALLEL I/O
- SERIAL 0,1
- PERIPHERAL

**NOTES:**

- although device has harvard architecture prog. data and i/o are all in single logical 16m word space.

---

**SOFTWARE**

**DATA-MANIPULATION INSTRUCTIONS**

- 2- and 3-operand arithmetic and logical instructions

**DATA-MOVEMENT INSTRUCTIONS**

- Concurrent with data-manipulation instructions, using separate fields of wide program word (possible because of separate address-computation ALUs and large number of parallel buses on chip)

**PROGRAM-MANIPULATION INSTR**

- Repeat mode to implement zero-overhead loops: RPT single instruction and RPTB block with latter being interruptable.
- Standard branches (including calls and returns) taking four cycles and delayed branches taking one cycle.
- Multiple branch conditions can be programmed.
- Unlimited software stack (four external and a number of internal interrupts)

**PROGRAM-STATUS-MANIP INSTR**

- Details not yet available

**Software Notes:**

1. Integer and floating-point data formats:
   - a. 16-, 32-, and 40-bit integer
   - b. 16-, 32-, and 40-bit floating point
2. Interlocked instructions to synchronize multiple C30s, using external signals (such as semaphores)
3. Software upwardly compatible with existing 320 family (code-conversion software available)

**Specification summary:** Harvard architecture, yet its separate memory spaces can appear to the programmer as one large (16M x 32) linear space.

**Program memory:** A 4k x 32 on-chip ROM with access to off-chip spaces. On-chip 64 x 32 cache.

**Data memory:** Two 1k x 32-bit on-chip RAMs plus access to program ROM (for coefficients) and to off-chip spaces. Two address-generation ALUs with eight auxiliary (pointer) registers.

**CPU:** Multiplier and ALU can be programmed to do either 32-bit floating point (with 40-bit extended precision) or 24-bit integer operations. Barrel shifter can shift 32-bits left or right in single cycle.

**Performance:** 60-ns instruction cycle giving 33M-flops computation rate.

**External:** Two serial ports and associated timers/counters with I/O pins. Two parallel ports, both 32-bit data, but one with 24-bit address and other with 13-bit address. DMA is provided so transfers can be conducted concurrently with CPU operation. Fabricated in 1.0-µm CMOS. Typical power consumption expected to be 1W. Packaged in 144-pin (µP version with access to external memory) or 84-pin (self-contained µC version).

---

**32-BIT FIXED- AND FLOATING-POINT CMOS DSP**

**Texas Instruments Inc**

**Description:**

- The 3rd-generation member of 320 DSP family, the C30 provides significant improvements in features compared with previous 320 generations. The 320C20 has 32-bit floating-point math vs 16-bit fixed-point, 60-nsec instruction cycle vs 160 to 200 nsec, a 16M x 32 total memory space vs 4k x 16 to 128k x 16. These computing enhancements are matched by equally significant jumps in I/O capability: The 320C30 has two 32-bit parallel and two 8M-bps serial ports, plus on-chip DMA to allow their concurrent use. Much of this will be possible because it is fabricated in finer-geometry 1.0-µm CMOS vs 1.8-µm CMOS or 2.4-µm NMOS. Still, chip size will be large—over 400 mils on a side being needed to hold its 700k transistors. (For overview of 320 family, see the table in directory entry for fixed-point 320 family members.)

**HARDWARE**

- Fabricated in 1.0-µm CMOS. Typical power consumption expected to be hundreds of dollars being asked for other 32-bit floating-point DSPs, we are going to price our part well under $100. Because of the general 32-bit nature of this type of "DSP," with its large unified address space, it may find as much use in general number-crunching-type computing as in DSP, especially in conjunction with its promised full general-purpose K&R C compiler.

**SUPPORT**

- From TI: Macroassembler/linker, simulator and full Kernigan & Ritchie C compiler that runs on IBM PC and VAX/VMS. A software-development system package that is composed of a card for IBM PC, an assembler/linker, and applications software library. Provides real-time in-circuit emulation with environment to reassemble, relink, and reload code when debugging.

**SOFTWARE**

- From TI: Kernel version of K&R C compiler that runs on IBM PC and VAX/VMS. A software-development system package that is composed of a card for IBM PC, an assembler/linker, and applications software library. Provides real-time in-circuit emulation with environment to reassemble, relink, and reload code when debugging.

---

**NOTE:**

- Although device has harvard architecture prog. data and i/o are all in single logical 16m word space.

---

**AVAILABILITY:**

- 3rd-party vendors that have been supporting the fixed-point members of the 320 family are extending their efforts to include the 320C30.

**COST:**

- $40 to $60 in high volume. Supplier plans aggressive pricing compared to other floating-point DSPs.

**SECOND SOURCE:**

- None announced, but supplier says its policy is to obtain second sourcing for 320 family. Says current candidate for 2nd- and 3rd-generation family members is not GI, who is presently second source for 1st-generation, but "one of the major US semiconductor houses," possibly Intel.

---

**DESCRIPTION:**

- The 3rd-generation member of 320 DSP family, the C30 provides significant improvements in features compared with previous 320 generations. The 320C20 has 32-bit floating-point math vs 16-bit fixed-point, 60-nsec instruction cycle vs 160 to 200 nsec, a 16M x 32 total memory space vs 4k x 16 to 128k x 16. These computing enhancements are matched by equally significant jumps in I/O capability: The 320C30 has two 32-bit parallel and two 8M-bps serial ports, plus on-chip DMA to allow their concurrent use. Much of this will be possible because it is fabricated in finer-geometry 1.0-µm CMOS vs 1.8-µm CMOS or 2.4-µm NMOS. Still, chip size will be large—over 400 mils on a side being needed to hold its 700k transistors. (For overview of 320 family, see the table in directory entry for fixed-point 320 family members.)

---

**SOFTWARE NOTES:**

- 1. Integer and floating-point data formats:
   - a. 16-, 32-, and 40-bit integer
   - b. 16-, 32-, and 40-bit floating point
   - 16-, 24-, and 32-bit floating point.
   - 2. Interlocked instructions to synchronize multiple C30s, using external signals (such as semaphores)
   - 3. Software upwardly compatible with existing 320 family (code-conversion software available)

---

**SPECIFICATION SUMMARY:**

- Harvard architecture, yet its separate memory spaces can appear to the programmer as one large (16M x 32) linear space.

**PROGRAM MEMORY:**

- A 4k x 32 on-chip ROM with access to off-chip spaces. On-chip 64 x 32 cache.

**DATA MEMORY:**

- Two 1k x 32-bit on-chip RAMs plus access to program ROM (for coefficients) and to off-chip spaces. Two address-generation ALUs with eight auxiliary (pointer) registers.

**CPU:**

- Multiplier and ALU can be programmed to do either 32-bit floating point (with 40-bit extended precision) or 24-bit integer operations. Barrel shifter can shift 32-bits left or right in single cycle.

**PERFORMANCE:**

- 60-ns instruction cycle giving 33M-flops computation rate.

**EXTERNAL:**

- Two serial ports and associated timers/counters with I/O pins. Two parallel ports, both 32-bit data, but one with 24-bit address and other with 13-bit address. DMA is provided so transfers can be conducted concurrently with CPU operation.

**FABRICATED IN:**

- 1.0-µm CMOS. Typical power consumption expected to be 1W. Packaged in 144-pin (µP version with access to external memory) or 84-pin (self-contained µC version).
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86232

AVAILABILITY: Samples in the 4th qtr '87 with production following one to two months after in '88.
COST: In the "hundreds of dollars."
SECOND SOURCE: None announced.

Description: Another top-of-the-line 32-bit floating-point DSP μ.P. Among its features are a 3-port RAM approach to data memory, dual 32-bit buses on chip, and bit-reversing addressing (for FFTs). It has direct access to large off-chip program and data memory spaces.

Hardware Notes:
1. Chip constructed with supplier's 1.3-μ.m CMOS standard-cell technology. 450k transistors and 60k gates.
2. Large 208-pin package allows separate 32-bit I/O for off-chip parallel access to instruction and data memories plus the addressing and control for those memories. There are also pins left over for 16-bit parallel I/O and serial I/O plus a number of interrupts.

32-BIT FLOATING/FIXED-POINT CMOS DSP
Fujitsu Microelectronics Inc
3320 Scott Blvd
Santa Clara, CA 95054
Phone (408) 727-1700

Status: Supplier says that because the chip has been designed and built with supplier's 1.3-μ.m CMOS gate-array technology, it will be possible in future to give customers ASIC-type access to 86232 macro cells so customers will be able to create their own optimized versions. Supplier realizes its weakness in support, so for the US, it is turning to 3rd-party organizations. In addition, it is planning to emulate TI and work closely with US universities (University of New Mexico is being used as a Beta site).

Hardware Characteristics

Hardware - Support

Software Notes:
2. Program memory can be used for data table.

Specification summary: Harvard architecture with mostly separate program and data sides, supported by two 32-bit-wide buses. For program memory: a 1k×(32) on-chip ROM and access to 64k×(32) off-chip space. For data memory: a 512×(32) on-chip RAM with 3-port access so both multiplier operands can be read while result is written back in. Also I/O access to 1M×(32) off chip. Multiplier and ALU can be programmed to do either 32-bit floating-point or 24-bit integer or 32-bit integer operations. Sixteen 32-bit internal registers. 75-nsec instruction cycle that includes multiply/accumulate (2-stage pipeline in multiplier). Fabricated in 1.3-μ.m CMOS triple-metal (standard cell) and packaged in 208-pin PGA.

Software - Support

Basic assembler is being prepared in Japan. In addition, US arm of supplier says it will be contracting with US 3rd parties for software simulators, etc, "to bring support up to standards expected by US OEMs."
Supplier says it will be contracting for a high-level-language compiler with the candidate languages being C and Fortran.

186 EDN September 3, 1987
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3M has had a whole generation of experience in the development, manufacture and refinement of perfluorinated liquids. We first introduced these versatile liquids to electronics design, testing and production professionals in the fifties. Since then, Fluorinert Liquids have become the mainstays in electronic cooling, high reliability testing and vapor phase soldering.

Fluorinert Liquids, used as a direct contact heat transfer medium, offer a range of physical properties that make them particularly suitable for electronic uses. They are non-polar and exhibit no solvent action. They are colorless, low in toxicity, non-flammable and offer exceptionally high dielectric strength plus thermal and chemical stability. Most important, they have almost no chemical reactivity and they evaporate without leaving a residue on parts.

**Buy the numbers**

Our FC™ numbers — FC-40, FC-70, FC-77, etc. — are used to identify Fluorinert Liquids that offer certain physical characteristics to meet specific application needs. These FC numbers are solely 3M designations for various fluorochemical products.

Fluorinert Liquids are being used cost-effectively in cooling, high reliability testing and vapor phase soldering operations. When you are interested in applying these versatile liquids in your own production, 3M can provide an abundance of technical information and support.

**Technical assistance: the main benefit of Fluoronics Resources**

3M offers prompt assistance to help you solve many production and testing problems. We provide comprehensive technical recommendations for specific fluids. We consult with you on the proper application equipment and help you evaluate production methods and results. Our service bulletins bring you up to date on the most recent advances in vapor phase soldering and high reliability testing. Ask us about 3M’s audiovisual materials and on-site application training seminars.

**Discover Fluorinert™ Liquids’ heat transfer capability**

What are your needs? A precise degree of temperature control? Fast, uniform heat transfer? High dielectric strength? Fluorinert Liquids offer the broad range of physical characteristics required in most applications.

Fluorinert Liquids are an effective direct contact heat transfer medium whether used in a liquid or vapor state. Their unique properties enable you to use them in contact with sensitive components and substrates.

Major differences between the various products in the Fluorinert Liquids family can be seen in their boiling points. These can range from 56°C to 253°C. Should you need products with intermediate boiling temperatures, the 3M staff will work with you to fashion a product especially for your needs. It’s an example of how 3M’s Fluoronics Resources provide you with “customized” service to solve special problems.

**Fluorinert™ Liquids achieve accurate high reliability testing**

It’s a small world you work in. Where time ticks in nanoseconds and dimension is measured in Angstrom units. And as circuitry becomes more complex, a greater demand is placed on testing capability — not only in speed, but in higher reliability and accuracy.

Fluorinert Liquids meet those requirements by providing a controlled temperature environment and a high degree of electrical protection. They offer maximum compatibility between
the heat transfer medium and the device under test. Fluorinert Liquids reduce testing costs by reducing testing time substantially. They do this by rapidly reaching test temperature and providing precise and uniform temperature control. You'll minimize the number of faulty units by detecting defects before they become rejects.

These liquids provide cost-effective tests such as gross leak, thermal shock, liquid burn-in, ceramic crack detection, electrical environmental, temperature calibration and failure analysis/short detection. Fluorinert Liquids are specified in the MIL-STD's for thermal shock and gross leak testing.

**THERMAL SHOCK TEST CONDITIONS**

<table>
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<tr>
<th>Military Standard 883-1011</th>
<th>Military Approved Fluorinert Liquids</th>
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<td>Hot Test Step 1</td>
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<tr>
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<td>100°C - 0°C</td>
</tr>
<tr>
<td>B</td>
<td>125°C - 55°C</td>
</tr>
<tr>
<td>C</td>
<td>150°C - 65°C</td>
</tr>
<tr>
<td>D</td>
<td>200°C - 65°C</td>
</tr>
<tr>
<td>E</td>
<td>150°C - 190°C</td>
</tr>
<tr>
<td>F</td>
<td>200°C - 190°C</td>
</tr>
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</table>

**GROSS LEAK TEST CONDITIONS**

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<th>Indicated Fluids</th>
<th>Detector Fluids</th>
<th>Absorption Fluids</th>
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<tr>
<td>MIL-STD 883-1014</td>
<td>FC-40, FC-43</td>
<td>FC-72, FC-84</td>
<td>Do not apply</td>
</tr>
<tr>
<td>MIL-STD 702-1671</td>
<td>FC-40, FC-43</td>
<td>FC-72, FC-84</td>
<td>FC-43, FC-75, FC-77</td>
</tr>
<tr>
<td>MIL-STD 202-112</td>
<td>FC-40, FC-43</td>
<td>FC-72, FC-84</td>
<td>Do not apply</td>
</tr>
</tbody>
</table>

**Discover higher yields in vapor phase soldering**

Fluorinert Liquids have been the industry's fluid of choice since the vapor phase reflow soldering (VPS) process was introduced in 1975. There are a number of good reasons for this universal acceptance. VPS with Fluorinert Liquids produces highly reliable solder joints. The system reduces reject rates, increases production, and lowers production costs. With Fluorinert Liquids, you can be assured that your products will never be exposed to a temperature higher than the selected liquid's boiling point. (See above)

You'll avoid those problems usually associated with other systems — shadowing, uneven heating, and overheating. The liquids are non-flammable. Their low surface tension helps them evaporate quickly from the work pieces without leaving a residue.

VPS with Fluorinert Liquids is especially suited for boards with high mass or complex geometries. The liquid vapors completely surround the assembly and penetrate remote recesses to heat all surfaces evenly. The vapors are 15 to 20 times heavier than air so they can be contained easily within the work area. The system offers an oxygen-free, non-corrosive environment to minimize rejects from oxidation contamination.

Some typical applications using Fluorinert Liquids in VPS include surface mounted leaded or leadless components, through-hole leads and wire-wrap pins, lead frame attachment, reflow of electroplated solder or tin and miscellaneous metal joining.

**VPS SELECTION GUIDE**

<table>
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<tr>
<th>Fluorinert Liquid</th>
<th>Boiling Point</th>
<th>Typical Solders</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC-43</td>
<td>174°C/340°F</td>
<td>50 Sn/35 Ag</td>
</tr>
<tr>
<td>FC-70, FC-5311</td>
<td>215°C/419°F</td>
<td>63 Sn/37 Pb</td>
</tr>
<tr>
<td>FC-71</td>
<td>253°C/487°F</td>
<td>100 Sn</td>
</tr>
</tbody>
</table>

**Discover the unique cooling benefits of Fluorinert™ Liquids**

As the package size decreases, your need for more efficient heat dissipation increases in proportion. 3M Fluorinert Liquids are very efficient as a direct contact heat transfer medium, with the added advantage of having the high dielectric characteristics needed to meet stringent demands of the diversified electronics industry. We offer 11 liquids with boiling points that range from 56°C to 253°C. These liquids allow you to maximize power density and miniaturize your package. Yet they reduce failure rates and increase reliability.

Fluorinert Liquids are used in such demanding applications as:
- Radar transmitters • Power supplies
- High voltage transformers • Lasers
- Radar klystrons • Computer modules
- Computer memories • Fuel cells

Typical properties of Fluorinert Liquids used in cooling are:

<table>
<thead>
<tr>
<th>Fluorinert Liquid FC-77 (English Units)</th>
<th>Liquid</th>
<th>Boiling Point (207°F)</th>
<th>Vapor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density (lb/ft³)</td>
<td>1.11</td>
<td>0.96</td>
<td></td>
</tr>
<tr>
<td>Thermal Conductivity (Btu/ft²/hr°F)</td>
<td>0.030</td>
<td>0.030</td>
<td></td>
</tr>
<tr>
<td>Specific Heat (Btu/ft²°F)</td>
<td>0.25</td>
<td>0.28</td>
<td></td>
</tr>
<tr>
<td>Viscosity (cP)</td>
<td>1.42</td>
<td>0.46</td>
<td></td>
</tr>
<tr>
<td>Coefficient of Thermal Expansion (ppm/°F)</td>
<td>0.0006</td>
<td>0.0009</td>
<td></td>
</tr>
</tbody>
</table>

**Discover heating/curing with Fluorinert™ Liquids**

Because they maintain their vapor temperature with absolute precision, Fluorinert Liquids can be used in many heating and/or curing operations. They serve as heat transfer media in solder mask and polymer thick film applications and for polymer processing. The non-corrosive vapors will not support oxidation. Ideal where solvent flash-off is a problem.
Discover Fluoronics Resources

Three cassette tapes are available describing Fluoronics high reliability testing and chemical products: Direct Contact Cooling, Vapor Phase Soldering, and High Reliability Testing.

For technical information or assistance on High Reliability Testing, call 612-273-6626.

For more information, visit 3M's Chemical Products Division at 3M Center, St. Paul, MN 55144.
Check list helps you choose a pc-board autorouter

Before you can choose the right pc-board autorouter for your needs, you need to understand how these programs work and how their features affect your project's entire design cycle. This article explains the functions of eight types of autorouters and provides a check list of 26 key features that will help you compare and select routers.

John Roth, Aptos Systems Corp

An automatic pc-board-routing program can save you a lot of time, provided that you use it as a design aid and don't expect it to solve all your routing problems. Autorouters come in a wide variety. To select the router that best suits your needs, you should have a general idea of how the various types operate and of what functions they can and can't perform. In the following pages, you'll find brief descriptions of the eight major types of autorouters and a check list of 26 key features to consider when comparing products. The glossary on pg 195 defines some of the terms commonly used on autorouter data sheets.

Autorouters differ mainly in the number and type of constraints that they impose on the routing process. There are two basic types of autorouters: gridded and gridless. Most of today's routers are the gridded type; they center traces and pads on an imaginary grid. The interval between grid lines typically ranges from 1 to 50 mils. These routers also rely on a strict set of design rules that determine the dimensions of the rectangular routing cell.

Gridded routers work best with designs that consist mainly of SSI and MSI components: The higher the component density becomes, the slower the router runs, because it has to manipulate a larger number of coordinate vectors. Thus, the search and scan time for assessing each individual net increases as the component density increases. Another major weakness of gridded routers is that they can't use all the available space during the routing process. However, a great advantage of gridded routers is that they are relatively easy to set up and to understand.

Gridless routers also rely on design rules, but they are not constrained by fixed grid or cell dimensions. Instead, they assess trace width, conductor spacing, and via size for the net currently being routed, so they can vary the grid size on the fly. The resolution can be as fine as one millionth of an inch. This technique allows the router to make use of all the available space on the board and thus gives it a good chance of completing the intended net on the first pass.

The major weakness of the gridless router is that after routing is complete, the board may need extensive manual editing. These routers may produce poor conductor alignment and nonstandard connections that may be difficult or impossible to manufacture. The greatest advantage of gridless routers is that they...
The maze router, used by itself, may create erratic routes and large numbers of vias.

adapt easily to changes in topological and packaging technology (for example, the requirements of surface-mount devices).

Besides the two basic categories of gridded and gridless routers, autorouters come in a number of subcategories. The following paragraphs list some of the more common types of autorouters and discuss their principal advantages and disadvantages.

**Maze router**: C Y Lee originally developed the maze router as an aid to routing taxis through the streets of New York City. Others first applied Lee's algorithms to pc-board wiring in 1961, and almost all of today's routers make some use of them. The maze router starts at a source point and proceeds to a target point one net at a time. It does not remember the locations of previous targets, nor does it know in advance the location of the next source. Thus, it may create erratic routes with many unnecessary vias (Fig 1).

**Line-probe router**: The line-probe (or branch) router starts each net at both the source and the target point simultaneously; it searches every available path between the source and target points until it finds a path that allows the trace ends to meet. In every other respect, however, it's similar to Lee's original maze router. The line-probe router tends to be extremely slow when routing medium- and high-density boards.

**Pattern router**: The pattern (or memory-I/O) router recognizes repeated circuit configurations, such as the data and address connections of memory ICs. If you use the pattern router in conjunction with other routers and restrict it to routing the repeated patterns, it can save you much time. However, if you use it alone, it can create such a confusion of traces and vias that nonrepeating nets can't be completed, and you may then have to reroute the whole board.

**Bus router**: The bus router can also recognize repetitive circuit patterns, but it's much more limited than the pattern router. The bus router is known as a single-pass router, because it routes only the most direct nets between source and target points, does not produce vias, and does not iterate (a process of finding and rerouting any troublesome traces).

**Pair-wise router**: A pair-wise router can route two (but not more than two) layers at a time, so its use is limited to traditional topologies and circuit designs. It may employ more than one of the routing methods in this list.

**Multilayer router**: A multilayer router can route more than two consecutive layers at a time, can place buried vias in specified hidden layers, and can usually handle complex packages such as surface-mount devices. This type of router may also use more than one of the algorithms in this list.

**Rip-up router**: The rip-up (multipass) router attempts to complete 100% routing of a board by automatically performing many iterations of the routing process. At some critical point in the process, the rip-up router may defy some of the design rules in order to complete the routing; in that case, when routing is complete, the router performs another iteration in an attempt to clean up the areas where it broke the rules. Because this autorouter requires a large database, you should use it on a computer with a large memory (a mainframe or a workstation), in order to reduce the number of disk accesses. Further, because the rip-up router must perform a very great number of computations, it may be slow unless you run it on a large host or a workstation that's equipped with a hardware accelerator. The rip-up router also tends to create an excessive number of vias; during the later iterations, therefore, it expends most of the available CPU time on reviewing and removing vias.

**Smoothing router**: Unlike the rip-up router, which removes and completely replaces routes that block its
completion of the routing process, the smoothing router (or the push-and-shove router, or hugging router) attempts to make room for a new route by displacing existing traces. It tries to make full use of the available space in the expansion rectangle while still conforming to the existing grid pattern. However, when used by itself, this type of router may create unmanufacturable board designs; it may, for example, leave insufficient clearance between traces. For this reason, you must usually supplement the smoothing router with another type of router.

Consider routers' specific features

Routing is only a small part of the total pc-board design cycle (Table 1). The features present or lacking in a particular product may influence not only the routing process but also other parts of the design and manufacturing cycle.

After making an initial assessment of the general class of router that you'll need, you can consider the products' specific features. You can use the check list that follows to compare different routers and to assess their suitability for your purposes.

1. In what format does the autorouter's parts-library database construct, store, and use its devices? Some routers use formats that are compatible with design tools from other vendors; some use completely proprietary formats that may require you to use CAE tools only from a single vendor. The characteristics of the parts library have a considerable influence on a router's capabilities. You should find out what routing parameters (such as part sizes, pin characteristics, and electrical characteristics) are built into the parts-library database of the router you're considering.

2. Which library packages come with the router? Do they contain standard digital, surface-mount, analog, connector, and discrete parts? Surface-mount technology (SMT) is becoming more widely used in the design and manufacture of pc boards. Even if a particular router lets you build a library that includes SMT parts, some routing algorithms may not be able to process SMT parts. Some libraries allow you to add your own library parts and to copy or modify the parts supplied by the library vendor.

3. What are the router's facilities for packaging, placement, and manipulation of logic elements? These facilities determine how well the router will perform.

You have to package the elements in accordance with their function and place the components on the board according to their relative network connectivity and circuit structure. You should find out whether the router you're considering employs manual or automatic element packaging; whether the library contains pre-packaged elements; and whether the placement routine is manual, automatic in batch mode, or interactive. Further, an efficient router lets you swap pins, gates, and components to achieve the optimum placement for routing.

4. In what manner does the software display the rat's nest and allow you to manipulate the display? Automatic-placement routines and routers begin by merging the schematic net lists with the component list to create a rat's nest. The rat's nest has proved to be a valuable visual aid in the placement and routing of pc boards. Some routers let you delete, change, and add to the rat's nest either during the initial setup procedure or interactively at a later stage. You can also force some routers to route certain nets in a specified order.

<table>
<thead>
<tr>
<th>TABLE 1—THE STAGES OF PC-BOARD DESIGN</th>
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<td>2. SIGNAL BUSING NETWORK</td>
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<td>3. DATABASE HIERARCHY</td>
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<tr>
<td>CIRCUIT-DESIGN ANALYSIS</td>
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<td>1. ELECTRICAL-RULE CHECK/DESIGN-RULE CHECK</td>
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<td>2. LOGIC SIMULATION</td>
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<td>3. CIRCUIT SIMULATION</td>
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<td>4. TIMING ANALYSIS</td>
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<td>PC-BOARD DESIGN</td>
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<td>PC-BOARD-DESIGN ANALYSIS</td>
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</table>
The smoothing router can move traces and vias; it tries to use all available space in the expansion rectangle in order to accommodate a new route.

5. What is the routing program's user interface? Some routing programs are menu driven, and some accept multiple-command lines. To set up the router, you need to know how the routing algorithms operate, on what principles the board is laid out, and what router instructions will best route your design. Products that automate the task of setting up the router are helpful for inexperienced users, and they ultimately reduce routing times and increase the efficiency and accuracy of the router.

6. Can the system provide statistical analysis of the topology and predict the routing density before the routing starts? Some products include a very fast "preroute" program that can predict, for a given component placement, the percentage of routes that the program will be able to complete. If the predicted completion percentage is low, you can then change the placement before wasting routing time on a bad layout. Some products can also predict total wire length and problem nets, and some can warn you when they violate the routing limitations.

7. Is the router interactive or does it operate in batch mode? Some routers are completely processor-controlled; that is, once you've started the routing process, you can't make it pause—you can only abort and exit to the operating-system command level. Others allow you to suspend the operation and then re-enter it (though not at the point where you stopped it). Some routers are fully interactive; they allow you to stop, make modifications, and pick up where you left off. Still others provide some combination of these modes. Ideally, you should be able to stop the routing at any point and then have the choice of saving what has been done, backing up to a previous point and restarting, or quitting the program without saving the work.

8. How much RAM does the router need, and how much hard-disk space does the router itself occupy? How much hard-disk space does the router need?

9. What is the maximum board size (in inches) that the router can handle? It's also important to know how many grid points are available within the board area and how many components, pins, gates, nets, and connectors the program allows. The database characteristics can have a great (and sometimes unwelcome) influence on router performance. Some routers, for instance, allow you to design boards as large as 50x50 in. but limit the number of ICs that you can put on one board to 150, regardless of the board's size.

10. Is the router gridded or gridless? If you're considering a gridded router, check to see whether it lets you select different grid spacing for different layers of the pc board and for the x and y axes of the grid. Some routers work best at one particular grid spacing; others work equally well over the whole range of spacing. If you're considering a gridless router, check to make sure the program provides a smoothing operation.

11. How many levels or layers of design does the router address? The more layers in the pc board, the more flexible the routing can be. However, a router that can handle as many as 50 layers may not be able to route them all in one operation. Further, some routers make it difficult for you to add another layer in the middle of a routing operation. It's also important to know how many layers are available for traces and pads, how many layers are reserved for planes, and how many of the available layers you can define yourself.

12. How does the router handle multilayer boards? If your designs are likely to include boards of more than two signal layers, you need to know if the router will be considering all possible layers at once or routing the layers in pairs and going to additional layers when a given pair is full. On one hand, you don't want the router to make the expensive step of adding more layers unnecessarily; on the other hand, pair-wise layering algorithms can create complexity because of channel blocking that would not occur if more layers were being considered simultaneously. The pair-wise layering approach poses an additional problem: transmission effects. Say, for example, that during a route the router gets stuck on one pair of layers and has to go to another pair. Suppose also that the last trace routed on the first pair ran from lower right to upper right before it got stuck, and then ran all the way back on the new pair of layers. Such long, overlapping nets can create huge transmission effects, which are serious problems that are difficult to catch before you actually build and test the board.

13. On what basis does the router assign trace sizes? Trace width is critical to any design, and it must be user-definable. You need to know how many different trace sizes the router can use during one pass. Some
routers let you assign particular widths to specific nets before the routing starts. Some also allow you to protect traces that were placed either manually or by a previous routing operation, so that subsequent routing will not undo them. When you’re considering a particular router, find out whether it can place 45° traces or radial traces or both, and find out whether it lets you control and vary the cost factors.

14. Can you force the router to work through the nets from shortest to longest (or vice versa)? Can you prioritize the nets before the routing operation starts, so that the nets will be routed in the order you specify?

15. Does the program provide parameters or attributes that designate special handling of the traces carrying certain signals? Most routers can handle traditional TTL designs but have difficulty with high-speed designs that use RF, ECL, and HS-CMOS components. Such designs require specialized trace functions to avoid signal chaining, transmission-line effects, impedance mismatches, signal distortion and reflection, and high-frequency noise.

16. How much control do you have over the placement of vias? Most routers tend to be “via-happy,” because their mandate is to complete a net by any means possible. Therefore, they place many vias that would be unnecessary if they routed the net differently, and they place some of the vias inappropriately. Because ECL, HS-CMOS, RF, and SMT components may require special handling of vias, it’s essential that you be able to retain some control over the placement and length of vias.

Some routers place vias automatically, and some let you specify via sizes. Some routers optimize vias during the routing process; others optimize vias by means of a batch routine that runs when routing has been completed. Further, some can place buried or blind vias; if you’re considering one of these products, find out whether the router can use a buried or blind via as the source of a new net.

17. Does the router let you define “keepouts?” Keepouts are critical areas of the board—for example, under glass-body components, under heat sinks and other hardware, or close to edge connectors—where

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**Glossary of autorouting terms**

**Blocked edge:** Any edge of an expansion area or rectangle that becomes obstructed by a non-fixed trace or via.

**Cell:** The expansion rectangle within which the router works according to the design rules.

**Design rule:** Any user- or system-defined guideline that determines router behavior with respect to parameters such as trace width, conductor spacing, via pad size, or grid size.

**Edge:** A source or target pad, track, via, or free or blocked edge that can be expanded into an expansion area.

**Edge, fixed:** An obstructed edge of an expansion rectangle, as calculated by the design-rule constraints.

**Edge, free:** A continuous edge of an expansion rectangle that is free of obstructions.

**Enclosed rectangle:** A potential area, calculated according to the design rules, for placement of a via.

**Expansion rectangle:** An area, delimited by four fixed or free edges, that encloses a potential route path.

**Fixed obstacle:** Any preplaced constraint that the router can’t manipulate, such as board outline, trace- or via-restriction areas, component pads, free pads, connector fingers, traces, and vias.

**Net:** An entire string of connections, from first source point to last target point, including pads and vias.

**Nonfixed obstacle:** Traces and vias, previously placed by the router, which may be removed, replaced, altered, or deleted by subsequent passes.

**Orthogonal:** A trace segment is said to be orthogonal if it conforms to a given grid-design rule (such as a rule that allows 45° as well as 90° trace angles). A non-orthogonal trace is one that does not strictly conform to the specified grid-design rules.

**Subnet:** A single source and single target point, together with the associated vias, component pads, and preplaced items, that are completely connected by route segments within one net.

**Via-site rectangle:** Any edge of an expansion rectangle that can hold a via.
Gridless routers can adjust grid spacing on the fly, and they allow resolution as fine as one millionth of an inch. They adapt easily to surface-mount technology.

you must be able to prevent the router from placing traces and vias. Some routers let you define a keepout as an integral part of a library item; others let you define it in some other function of the pc-board design so that the router will automatically respect the keepout. If you can define keepouts, find out to how many layers of the board they apply. Keepouts can be global, affecting all layers of the board, or they can be local, layer-specific.

18. What kind of reports does the router produce? A router is of little use to you if it can’t report what it accomplished during the routing operation. It should be able to generate comprehensive reports that not only help you complete the current design but also provide information that will let you use the router more effectively and thus complete future designs more quickly.

For example, the router you choose should report the percentage of completed routes and the elapsed time. It should also tell you how many nets are incomplete after the routing, whether any conflicts were encountered, and what errors occurred. It’s also good to know how many layers were used and what vias were produced. Some routers display these reports on the screen during the routing operation, and some capture reports in a file for future investigation. It’s an advantage to be able to choose either or both of these methods.

19. How does the router provide for power and ground planes? Some routers automatically create power and ground planes. With some routers, you can extract power and ground nets from the full net list for special handling. On a multilayer board, you’ll often need to create internal planes dedicated to power and ground, as well as power and ground planes on the component and solder sides of the board. Many systems, however, will route power and ground connections as traces but won’t create power and ground planes.

20. Does the program provide back annotation? Often, when you pass a schematic to the board designer, the reference designators, gates, pin numbers, discrete component part numbers, and component values are not completely specified. A back-annotation feature can solve this problem by automatically updating the schematic to agree with the final board design. If the router you’re considering has a back-annotation feature, find out what data it can update and whether it can work both ways (that is, from pc board to schematic and from schematic to pc board).

21. Does the package provide a design-rule checker (DRC)? Design-rule checkers check for spacing and connection errors. A router follows a specific set of design rules and only rarely defies its own guidelines. However, a designer who is manually editing the output of the router may make mistakes; an automated DRC will find these errors much more quickly than you can by checking the output visually. In a router that provides a DRC, you’ll want to know what kinds of errors the DRC can detect and report (for instance, violations of the pad-to-pad, pad-to-trace, and trace-to-trace rules). It’s also a good idea to find out whether the DRC routine is a postprocessing task or a task that runs in real time during the manual editing process. Some routers with DRCs allow you to modify the DRC files, and some allow you to create design-specific DRC files.

22. What kinds of continuity errors does the router detect? A continuity check determines the validity of the routed traces on the board. Check to see whether the router can detect such errors as duplicate traces on the same net, pin-connection errors, and incomplete routes. Also find out whether the continuity check is executed during the routing process or as a postprocessing task.

23. Does the router provide a connectivity check? A connectivity check compares the net list of the pc board with the schematic net list. Find out what kinds of errors the checker can detect. Some connectivity checkers can find duplicate net names on the same trace, different nets tied to the same pin, and extra pin connections, for example. Again, you’ll want to know whether the connectivity check runs in real time during the routing process or is a postprocessing utility.

24. Is the manual editor easy to use? Because no router can route all board designs with 100% completion or produce a completely manufacturable board from all designs, the package must include a manual editor that lets you correct the errors and omissions of the automatic router. You’ll want a router whose manual editor is easy to use.

25. Will the routing system produce documents and files that are compatible with the manufacturing facility you’ve chosen? The requirements include reliable
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photplotting output and checking, pen or raster plots or both, and numeric-control files or tapes for drilling, automatic component insertion, and testing.

26. Does the router have any special hardware requirements? Hidden hardware costs can drive a seemingly low-cost system through your price ceiling. You need to consider not only the cost of the basic hardware, but also the cost of upgrades and maintenance.

Author's biography
John Roth is president and CEO of Aptos Systems Corp (Scotts Valley, CA) and has held this position for nearly two years. Before that, he was director of sales for Personal CAD Systems Inc. John has 15 years of technical sales and marketing experience. In his spare time he enjoys piloting hot-air balloons.

Article Interest Quotient (Circle One)
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High-speed video DACs drive CRTs to new performance heights

New high-speed video DACs with bandwidths to 400 MHz and color CRTs with 2048×2048-pixel resolution have set the stage for dramatic improvements in the quality and cost effectiveness of high-resolution graphic displays. However, don't undervalue a system's parameters when incorporating these DACs in your design.

Paul M Brown, Honeywell Inc

The graphics available on today's personal computers and workstations range from good to nearly breathtaking. At one end, the 320×200-pixel resolution of the IBM PC standard color display provides adequate resolution for text and simple graphics. At the other end of the spectrum, state-of-the-art workstations can achieve resolutions of over 2048×2048 pixels and palettes of nearly 17 million colors. The results rival 35-mm film for clarity. However, the solutions to several technical problems have remained expensive. The availability of high-speed monolithic video DACs is helping to pave the way toward lowering the cost while still increasing the performance of high-resolution displays.

Display requirements define the system

Although the individual components are different, the basic block diagram of today's raster-scan graphics system (Fig 1) remains much the same as it has for years. Previously, expensive laser-trimmed hybrid DACs, large amounts of discrete logic, and single-port RAMs were necessary to implement the various functions. Such requirements made high-resolution graphics systems bulky and power hungry as well as expensive. The possible uses of high-speed analog-digital ICs in the development of complex high-performance building blocks now allow the construction of small, efficient, reliable, and reasonably priced high-resolution graphics systems. Today's graphics-system design contains the CPU, a graphics controller, high-speed RAM, a logic array for glue logic, and either one or three video DACs (depending on whether the application is monochrome or color).

Graphics controllers range in function from relatively simple screen-refresh types, such as the Motorola 6845, to dedicated custom graphics processors. Screen-refresh controllers supply the sync and blank signals and control the flow of data between the CPU, the screen-buffer RAM, and the video DAC. Although limited in speed and resolution for some applications, they are frequently used in low-end workstations and PCs with resolutions ranging from 320×200 to 1024×512 pixels. Dedicated graphics-processors contain specialized instruction sets for graphics and require little CPU support. The latter architecture is found in the highest-performance graphics displays.

The graphics controller supplies the video DAC with a digital word that represents each pixel in the display. Typically, the electron beam in the CRT scans across the screen in noninterlaced lines from left to right and top to bottom under the control of the horizontal and vertical sync and blank signals (Fig 2). The electron beam scans one line for each pixel row in the vertical direction. As the beam scans from left to right across the face of the CRT, the video DAC receives one digital word for each pixel in the line. The refresh rate is the number of times per second that all of the pixels in the
Some of today's workstations can achieve resolutions to 2048 x 2048 pixels.

display are redisplayed. The rate at which the DAC must convert digital words to analog pixel intensities depends on the number of pixels per line (horizontal resolution), the number of lines (vertical resolution), the horizontal- and vertical-retrace (flyback) time, and the refresh rate.

DAC bandwidth and rise time are important

Benchmarks for DAC bandwidth are shown in Fig 3 for various common display resolutions. The calculation of these bandwidths assumes a 60-Hz refresh rate and that the horizontal and vertical retrace uses 30% of the time required for each frame time. (Frame time is 1/60 of a second, the time it takes to scan one complete screen.)

Another way to determine the required DAC performance is to evaluate the pixel time for various display resolutions. The pixel time is the period during which the DAC processes a received digital word and changes its output to the analog value of that word. Fig 4 illustrates the approximate pixel times for various screen resolutions. It is important to understand that a video DAC does not settle to its rated accuracy during a pixel time; rather it rings above and below the settling level at a very high frequency. The screen's phosphor and the human eye serve as a lowpass filter and average out these variations. The most critical concern, therefore, is the rise time of the DAC's output, not the settling time. A fast rise time maximizes the illumination of each pixel during the pixel time period.

Not only must the DAC be very fast, it must also drive a substantial signal into a hefty load. Typically, the load is a dual 50 or 75Ω load (actual impedance 25 or 37.5Ω). Fig 5 illustrates the composite video waveform defined in the EIA RS-343A specification. In some applications, the DAC does not process the sync and black levels. The standard waveform (not including the 10% overbright level) is 1Vpp, commonly expressed as 140 IRE (Institute of Radio Engineers) units. Thus, each IRE unit has a value of about 7.14 mV.

The important levels of the composite video waveform are sync, blank (the level applied during retrace, also called "blackest than black"), reference black (the darkest color), reference white (the lightest color), and 10% overbright (sometimes called "whiter than white"). Cursors use the 10% overbright level where a large contrast is necessary with any color, even white. The

Fig 1—The typical raster-scan graphics system includes the main processor (CPU); a screen-refresh graphics controller to supply the sync and blank signals and control the flow of data; screen buffer-RAM; and, for a color system, three video DACs.
portion of the waveform between reference black and reference white represents the gray scale for a monochrome system or the potential hues for a color one. The number of discrete levels in this region depends on the resolution of the DAC. Low-end systems need as few as four bits (16 levels) of resolution, but high-end systems intended for solids-modeling applications may need 10 bits (512 levels).

**Final resolution depends on the display**

No matter how many bits of resolution or what the data rate, the graphical representation of the data to the user in the end depends upon the display device. The cathode-ray tube (CRT) is currently the most commonly accepted means of displaying computer-derived text and graphics—especially for high-resolution monochrome or color displays. The CRT consists of an evacuated glass envelope that contains an electron gun, a shadow mask (for color), and a phosphor-coated glass surface (Fig 6).

A control yoke (deflection coil) is usually supplied as an integral part of the CRT assembly. The yoke controls the deflection of the electron beam as it travels from the electron gun to the phosphor-coated screen. The delta-gun configuration, popular in the past, requires deflection-control elements that need periodic alignment. The in-line gun does not require adjustment and is now the choice for nearly all applications.

At refresh rates above approximately 40 Hz, the yoke becomes a critical element because of the heat generated by the increased power necessary to drive the yoke, and because of the potential for arcing caused by the increase in back emf. A typical yoke has an inductance of 300 µH and requires about 6A of drive current. The back emf is on the order of 1200V. State-of-the-art yokes designed for higher-resolution applications feature inductance values of less than 100 µH but require between 10 and 20A of drive current. The skin effect, however, increases the effective series resistance (and therefore the power dissipation of the coil) at high scan rates.

You can minimize the heating of the coil at higher drive-rates by using litz wire in the design. The multiple strands of litz wire maximize the skin thickness, thus reducing the effective series resistance of the coil. The lower inductance minimizes the back emf, reducing

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**Fig 2—The raster display is made up of pixels on the screen.** As the electron beam scans across the face of the CRT, a graphics controller supplies the DAC with a digital word for each pixel in the display.

EDN September 3, 1987 203
The availability of high-speed monolithic video DACs is helping to pave the way toward lowering the cost and increasing the performance of high-resolution displays.

![Graph showing total pixels versus DAC converter bandwidth](image)

**Fig 3**—Plotted above is the DAC bandwidth required for common display resolutions, along with the relevant technology. The bandwidth calculations shown assume a 60-Hz refresh rate and that the horizontal and vertical retrace take 30% of each frame time.

The flyback or retrace time becomes increasingly critical with higher-resolution displays because of the increase in the number of retrace periods resulting from the additional lines of vertical resolution. The total time needed for horizontal and vertical retrace is reduced, which in turn decreases the data-writing time available for writing data to memory. Thus, the DAC must process more pixels in a shorter time.

Color displays need a shadow mask

The most crucial elements in determining CRT resolution are the beam spot size and the shadow mask. For very high-resolution displays, the shadow mask requires a dot pitch of less than 0.22 mm. The construction of the CRT arranges the phosphors on the screen in groups of red, green, and blue (RGB). The electron guns focus the electron beams through the shadow mask to strike the appropriately colored phosphor. The

![Graph showing pixel time versus number of pixels](image)

**Fig 4**—The pixel time required for various display resolutions is one way to evaluate the required DAC performance. The pixel time is the period during which the DAC processes a received digital word and changes its output to the analog value of that word.
shadow mask ensures that, as the beam traces across the screen, the beam from each gun strikes only the correctly colored phosphor.

As resolution increases, the spot size gets smaller. The smaller spot size requires more power to focus the beam and a stronger beam to maintain the same intensity. This increased power results in greater power dissipation and heat. The smaller spot size also requires a reduction in the spacings between the openings on the shadow mask, thus making the mask more fragile. Only 10 to 20% of the beam energy strikes the phosphor. The balance of the beam heats the shadow mask, which can cause it to bow out.

This mechanical deformation of the shadow mask changes the focus and blurs the image (it's most apparent in the larger screen sizes). Keeping the gossamer-like shadow mask stable in spite of localized heating from the electron beam, changes in ambient temperature, and the effects of shock and vibration is a difficult task. The only practical solution is to reduce the size of the display, thereby increasing the mechanical strength of the shadow mask.

**Fig 5**—The standard composite video waveform (excluding the 10% overbright level) is \( V_{pp} \), a value equivalent to 140 IRE units. Each IRE unit has a value of about 7.14 mV. Reference black is the darkest color and reference white is the lightest color. The 10% overbright level (sometimes called “whiter than white”) is for cursor use or for where a large contrast is necessary. The blank level (sometimes called “blacker than black”) occurs during retrace.

**Fig 6**—The CRT is an evacuated glass envelope containing an electron-gun, a shadow mask (for color), and a glass surface coated with phosphors. A control (deflection) yoke is an integral part of the CRT assembly. Most of today's CRT's use the in-line gun, which does not need periodic adjustments. For high-resolution displays, the shadow mask must have a dot pitch of less than 0.22 mm.
No matter how many bits of resolution or what the data rate, the graphical representation of the data depends on the display device—in most cases a CRT.

The available monolithic video DACs combine ultra-high-speed process technologies and advanced architectures to make high-resolution graphics displays. The fabrication process of choice for video DACs is either oxide-isolated bipolar ECL or small-geometry CMOS. Both processes are optimized for minimum device size. Small on-chip components reduce such parasitic elements as stray capacitance and thereby allow high-speed performance at reduced current while also permitting the integration of more circuitry on the chip, both in terms of die size and power dissipation.

Bipolar and CMOS are in continual competition for the dominant technological position. A bipolar DAC waves new performance standards, which are later matched by a CMOS device that uses 75% less power. Next comes the announcement of an even faster bipolar DAC with features such as more resolution, a fast color look-up table, and data latches. Bipolar technology usually leads the performance parade by satisfying the most demanding state-of-the-art applications. As the performance level increases, the development of CMOS devices permits a reduction in both size and cost of the previous state-of-the-art design by reducing the power requirements and increasing the level of integration.

Many of the new video DACs, such as the Bt451 and the HDAM51100, have on-chip color palettes that include address and data registers. Other architectures include on-chip data multiplexers that can interleave several banks of relatively slow memory into a very fast DAC to achieve the desired throughput. Having the faster circuitry such as the color palette or the multiplexer on-chip eliminates the stray capacitance caused by interchip connections. Manufacturing the additional circuitry in the same fast process as the DAC also allows the matching of all logic voltage swings and logic timing for highest performance. But this higher level of integration does curb your architectural freedom at the system level. Also, it's difficult to upgrade that system without a major component revision.

In raster-graphics applications, the DAC bandwidth (or update rate) corresponds directly to low, medium, and high resolutions. Within those categories, you can sort DACs according to their bit accuracy. Either a 4-bit or an 8-bit DAC operating at a given million-words/see update rate in a particular application produces the same display (pixel) resolution. The 8-bit converter will, however, offer more shades of gray or more possible colors. Table 1 lists the available monolithic video DACs and their speed, accuracy, process, special features, and manufacturer.

Select DACs according to performance

In terms of speed, the DAC you select must be able to comfortably handle the required data rate with varia-

<table>
<thead>
<tr>
<th>RESOLUTION</th>
<th>SPEED MWPS</th>
<th>PROCESS</th>
<th>LOGIC</th>
<th>PART #</th>
<th>VENDOR</th>
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<td>ECL/TT</td>
<td>TDC1016-10</td>
<td>TRW</td>
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Table 1—Monolithic Video DACs
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Beam spot-size and shadow-mask construction are critical to CRT resolution. High-resolution displays require a shadow mask dot-pitch of less than 0.22 mm.

Operations in power-supply voltage and in the logic voltage swing over the ambient temperature range in which it must operate.

When you consider rise time, the output of the DAC must be able to reach the intended analog value in a fraction of the pixel time. It's unimportant that the output settles to its final value. The DAC must illuminate the pixel at full intensity for the largest possible fraction of the pixel time.

The glitches, or output spikes, are undesirable in any DAC, and especially so in high-resolution video applications. Glitches generally occur at major carries (¼, ½, and full-scale) and appear as intensity variations on the screen. A parameter called "glitch energy" usually specifies the magnitude of any glitches. This parameter is a measure of both the amplitude and duration of the spike. A great deal of effort has gone into designing glitch-free DACs. Some DAC architectures use special circuitry or adjustments to reduce or eliminate glitches, while other architectures are inherently glitch free.

High power-dissipation means a higher die temperature for the DAC, which can in turn lead to performance degradation at higher temperatures and can increase the load on the system power supply as well. Many times, however, the only way to achieve the desired performance is to bite the power-dissipation bullet. This is the arena in which bipolar and CMOS technologies continue to do battle.

The resolution of the DAC determines the number of intensity levels in monochrome displays or the number of possible colors in color displays. In the past, four bits were considered adequate for some applications. Today, most new designs employ at least eight bits. Solids-modeling applications generally require eight to 10 bits. A greater resolution requires a correspondingly larger amount of high-speed memory for support.

In terms of logic compatibility, the fastest DACs require ECL to drive them at their rated speed and have ECL-compatible logic inputs and consequently require ECL power supplies. In these very high-speed applications, you must make all logic interconnections using controlled-impedance techniques such as microstrips or striplines to avoid the undesirable reflections known as ringing. Ringing, caused by impedance mismatches, can easily result in the sensing of erroneous logic states and can wreak havoc on high-resolution displays.

Most monolithic video DACs can directly drive doubly-terminated 50 or 75Ω loads. As speed increases, the improved bandwidth of the 50Ω system becomes more attractive, mandating the use of a DAC capable of driving an actual load of 25Ω.

The future of high-resolution displays is bright and colorful. Color monitors capable of 2048×2048-pixel resolution and 60-Hz noninterlaced refresh are here, and 400-MHz video DACs (HDAC51400) with the bandwidth and signal swing necessary to drive these displays are commercially available. High-speed bipolar memories with access times under 5 nsec are also available. What's more, prices are coming down. Gallium arsenide (GaAs) is getting into the act with offerings of very high-speed logic, useful for control functions and for multiplexing low-speed memory to improve throughput. There are also some lower-resolution video DACs now available in GaAs technology. All of the parts have been cast, the stage is set, and the curtain is rising on a new era of ultrahigh-resolution video displays.

Author's biography

Paul M Brown is applications manager of the Signal Processing Technologies Group of Honeywell Inc in Colorado Springs, CO. Paul's experience includes circuit design and applications engineering at National Semiconductor, manager of custom products at Exar, manager of new product development at PMI, and director of applications at Micro Linear. He holds two patents and presented a paper on one of his designs at ISSCC 1979. Paul has written over a dozen technical articles for journals and trade magazines, and a 350-pg book on custom linear-IC design. Paul has a BSEE from San Jose State and is a member of Tau Beta Pi, Eta Kappa Nu, and the IEEE; he's also a licensed professional engineer. Paul's hobbies include woodworking, hiking, and writing.

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<tr>
<th>Device</th>
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<th>Package</th>
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<tbody>
<tr>
<td>µPD27C1024D-15/-20/-25</td>
<td>64K x 16 bits</td>
<td>150/200/250</td>
<td>40-pin DIP JEDEC standard pinout</td>
</tr>
<tr>
<td>µPD27C1000D-15/-20/-25</td>
<td>128K x 8 bits</td>
<td>150/200/250</td>
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<td>128K x 8 bits</td>
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* Patent pending
Low-cost quad op amps boost circuit performance

By exploiting the spare op amps available in a quad op amp, you can boost the performance of your circuits. You can also use high-performance monolithic quad op amps to design unique circuit configurations.

Jerald G Graeme, Burr-Brown Corp

By using monolithic quad op amps instead of single op amps in your circuits, you can remove a number of errors that occur in single-amplifier implementations. Programmable gain amplifiers (PGAs) and instrumentation amplifiers (IAs), for example, can make use of all four of the amplifiers in a quad op amp. The four amplifiers can remove switching and gain errors associated with PGAs. In IAs, quad op amps permit easier trimming and provide differential outputs for greater output swing. In your circuits that require fewer than four op amps, you can use the spare amplifiers of a quad to enhance circuit performance.

Programmable gain control

The single-amplifier configuration of a PGA traditionally places FET switches in the feedback path to implement programmable gain (Fig 1). However, switch errors usually force you to make a switch-position compromise: You must choose between a low-impedance node and a path with low signal current. In circuits that use common MOSFET switches, errors can be produced by the switches' series resistances, capacitances, leakage currents, and noise.

When you place the switches at the amplifier's output, the switches are driven from a low-impedance, large-signal point (Fig 1a). In this setup, the FET substrate's leakage currents and capacitances, along with their noise, introduce little error. The low-impedance output supplies the currents for leakages and parasitic capacitances; switch noise is introduced only after the signal has been amplified. However, because feedback-signal current flows through the switches' series resistance, a serious error source is produced. Also, this gain-switching configuration always has unconnected resistors at the op amp's summing junction; these resistors can electrostatically couple noise to the amplifier.

One way to avoid these error-producing effects would be to move the switches from the op amp's output to its input, as in the circuit shown in Fig 1b. Ideally, in this configuration, zero signal current would be present to create error caused by switch resistances, and no open resistors would result. However, this solution would pose new problems, because leakage currents (along with currents that charge switch capacitances) would be conducted through the feedback resistors. In addition, the switching noise would be introduced right at the sensitive amplifier input, and the switches' parasitic capacitances would affect the loop stability, because the switches would be coupled from the amplifier's inverting input to ac ground.

An ideal PGA configuration doesn't have switches in series with either the amplifier's input or its output.
You can use the spare op amps of a quad op amp to improve the performance of a programmable gain amplifier.

You can effect such a configuration by using a quad op amp, as in the circuit in Fig 2. In this circuit, the switches are internal to the overall amplifier, where they are both isolated from the combined amplifier input and buffered from its output. Yet the switches are both driven from the low-impedance output of an op amp, and they conduct only the low input current of another amplifier. The op-amp outputs supply all switch-leakage and capacitor-charging currents, and the switch resistances carry no signal currents. Further, any switch noise is preceded by the high gain of an op amp. Thus, by using a quad op amp, you combine the desired attributes of both Fig 1a’s circuit and Fig 1b’s circuit.

To achieve gain selection in Fig 2’s circuit, you connect one of the outputs of three preamplifiers to an output buffer. The preamps sense different taps on a common feedback network, so only one of those amplifiers will control the loop at any given time. The other two preamps remain in an open-loop configuration and have no influence on the feedback path as long as they draw no input current under input overload. The quad op amp in this circuit is the OPA404, which doesn’t draw excessive input current for signal levels as large as the supply voltages. The circuit’s gain, then, is simply that of a positive-gain op amp; the input and output components of the feedback network are formed by various combinations of the resistors. For example, when IC1b is connected to the loop, the gain is 1 + (R3 + R4) / (R1 + R2). This common feedback network leaves no resistors unused.

The performance of Fig 2’s PGA is very much like that of the single-amplifier PGA implementation, except that it doesn’t exhibit switch errors. The gain accuracy is set by the ratio matching of the feedback resistors and the loop gain of the controlling amplifier. Gain transitions occur with minimum switching transients in the feedback network; the settling times of the op amps control the switching time. For the OPA404, the switching time varies from 3.5 µsec (at a gain setting of 10) to 300 µsec (at a gain setting of 1000).

In Fig 2’s PGA configuration, offsets caused by leakage currents from the switch are absent, but a new offset phenomenon occurs. The input offset voltage of the overall amplifier changes in accordance with the gain switching as a different op amp controls the input at each gain setting. It’s still the input offset voltage of one op amp that detracts from the input signal, but that offset changes with the choice of gain, and would require more frequent autozero routines than a PGA circuit would normally need.

The frequency-response characteristics of Fig 2’s circuit are the same as those of the single-amplifier versions, except that Fig 2’s circuit includes additional consideration for the output buffer. The bandwidth for a given gain is still the gain-bandwidth product of the individual op amp divided by the closed-loop gain. That bandwidth ranges from 640 to 6.4 kHz for respective

---

Fig 1—Two conventional methods of obtaining programmable gain control are to connect the switches in series with the op amp’s output (a) and to connect the switches in series with the op amp’s input (b).
gain settings from 10 to 1000 for the OPA404. However, for gain settings of less than 10, the output buffer in the feedback loop contributes to the frequency response. In practice, the overall closed-loop gains remain much greater than the unity gain of the buffer, so the buffer's bandwidth remains far above that of the completed loop. This condition preserves frequency stability by avoiding phase shift from two op amps.

A circuit's slew rate can also be affected by the series connection of two op amps, because the buffer slews only in response to the rate of change of the preamp's output. At high gains, that rate of change is bandwidth limited, and it does not reach the slew-rate limit. However, as the circuit gains get closer to unity, the two op amps will exhibit a combined slew rate. This slew rate will asymptotically approach \( \sqrt{2} \) times the slew rate of each stage. For the OPA404, the slew rate would be \( 25 \text{V/\mu sec} \) (\( \sqrt{2} \times 35 \text{V/\mu sec} \)).

### Build an absolute-value detector

You can also use the four op amps of a quad as a differential-input absolute-value detector (Fig 3). This circuit consists of an input section, comprising amplifiers IC\(_{1A}\) and IC\(_{1B}\), followed by an IA, comprising IC\(_{1C}\) and IC\(_{1D}\). You can rectify the input signal by switching the signal between the IA inputs in accordance with the signal polarity.

In Fig 3's circuit, the differential-input signal \( (E_1 - E_2) \) is first impressed across \( R_0 \), which defines the current-feedback path around IC\(_{1B}\). When the differential-input signal is positive, a current is created that forward-

---

**Fig 2**—In this PGA configuration, the switches are internal to the overall amplifier, where they are both isolated from the combined amplifier's input and buffered from its output. Yet the switches are both driven from the low-impedance output of an op amp, and they conduct only the low input current of another amplifier.

**Fig 3**—This differential-input absolute-value detector consists of an input section (amplifiers IC\(_{1A}\) and IC\(_{1B}\)) and an instrumentation amplifier (IC\(_{1C}\) and IC\(_{1D}\)). You can rectify the input signal by switching the signal between the IA inputs in accordance with the signal polarity.
Ideally, a PGA configuration doesn’t have switches in series with either the amplifier’s input or its output.

biases D₁ and reverse-biases D₂, resulting in a configuration like the one shown in Fig 4a. In this setup, the amplified signal is connected to the inverting input of the IA. This circuit state yields positive gain, because the signal is inverted twice (first by IC₁₁B, and then by the IA). Negative differential inputs reverse the diode states, causing the signal to be applied to the non-inverting input of the IA (Fig 4b). This circuit state yields negative gain, because the signal is inverted only by IC₁₁B.

In both of the circuit states, the amplified signal reaches only one input of the IA. Note, however, that another signal component is present. The signal E₂ resides at the summing junction of IC₁₁B, where it is added to the differential signal. At the same time, E₂ is also coupled to the other IA input through the idle feedback resistor, so E₂ is a common-mode signal.

The IA (IC₁₁C and IC₁₁D of the circuit in Fig 3) employs a common feedback network for the differential inputs. As the figure shows, the feedback interconnection establishes IC₁₁D as an inverting amplifier in the feedback path of IC₁₁C. Each amplifier presents a signal input with high impedance to eliminate loading of the rectifier circuitry.

Some degree of common-mode signal coupling to the output will be present, depending on the common-mode rejection (CMR) of the op amps and the matching of their feedback resistors. Because the op amps of the OPA404 have CMRs of 100 dB (or CMRRs of 100,000:1), they are not generally the limiting factor. To make the op amps the controlling factor in CMR, you’d need resistor matching of better than 0.001%. Generally, the CMRR is the reciprocal of the net fractional resistor mismatch; that is, the CMRR is 10,000:1, which corresponds to 80 dB for a 0.01% mismatch.

Besides considering offset and switching time, you need to pay attention to resistor matching. Matching the two feedback resistors of IC₁₁B ensures equal circuit gains for the two signal polarities. The offset voltages shift the point of polarity reversal. In this circuit, the important offset is the difference between the input offset voltages for IC₁₁A and IC₁₁B; this offset is typically 350 µV for the OPA404. The input-bias-current offset is insignificant in the OPA404, however, because the OPA404 requires only 1 pA of input bias current.

Because of the time required to switch the diodes, Fig 3’s circuit isn’t an ideal absolute-value detector. That switching time is a function not of the diodes themselves, but of the speed with which the op amp can drive one diode off and the other on. You can’t entirely avoid error during this transition—to do that, you’d need instantaneous switching. However, the slew-rate limit and gain-bandwidth product of IC₁₁B impose a nonzero switching time, while the amplifier output swings two diode voltage drops (approximately 1.2V). For large signals, the amplifier is driven to its slew-rate limit (35V/µsec), and it makes the transition in 34 nsec.

Use quad in instrumentation amp
Quad op amps can increase the speed and accuracy of instrumentation-amplifier designs, because they exhibit better characteristics than do single op amps. The OPA404, for instance, offers 1-pA input bias current, 12-nV/√Hz noise, and 1.5-µsec settling time (unity gain). In IA applications in which various input signals are multiplexed to the IA, settling time is critical. The op amp’s settling time often dominates the time required for signal acquisition. A 3-op-amp IA using the OPA404 settles to 0.01% of its final value in 2 µsec.

Traditionally, to achieve a high degree of precision in IAs, you need to perform resistor trimming or software correction. You can do less trimming when you configure the fourth op amp of the quad as a bipolar offset potentiometer (Fig 5).
The conventional differential-input structure, formed by IC_{IA} and IC_{IB}, forces the signal on the gain-setting resistor (R_g) to be the difference between the input signals (E_1 and E_2). The outputs of IC_{IA} and IC_{IB} are then sent, with unity gain, to IC_{IC}, where common-mode signals must be separated from the differential component. The difference amplifier formed by IC_{IC} and its feedback network performs this separation. Accurate separation of these signals depends on the ratio matching of the four resistors connected to this amplifier. In this circuit, in which the resistors have equal values, the CMRR of the output stage is twice the reciprocal of the fractional mismatch. The IA's overall CMRR is the product of the CMRR of the output stage times the differential gain of the input stage.

One way to adjust the CMRR would be to use a potentiometer in the feedback path and connect the wiper to an input of IC_{IC}. However, this configuration would add capacitance at the input, especially if the potentiometer were remotely mounted at the edge of a pc board. Capacitance at the input is deadly to the OPA404's high-speed performance. An alternative would be to use two potentiometers, one for each output of the differential-input stage (IC_{IA} and IC_{IB}), but this

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**Fig 5**—When you use a quad op amp to configure a 3-op-amp instrumentation amplifier, you can use the fourth op amp to provide bipolar-CMR and offset adjustment.

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**Fig 6**—This instrumentation amplifier, with a differential output, doubles the output voltage swing while minimizing differential phase error.

EDN September 3, 1987
You can use the four op amps of a quad as a differential-input absolute-value detector.

**Fig 7—Among the applications for the fourth op amp in a quad-op-amp IA implementation are a guard-drive amplifier (a), a circuit that provides current output (b), and a circuit that performs output filtering (c).**

setup would complicate the adjustment procedure.

The circuitry surrounding IC10 in Fig 5 avoids these compromises—it creates variable resistance that can be either positive or negative, so it can handle either direction of resistor mismatch in the IA. You can adjust the CMRR by varying the amount of positive and negative feedback around IC10.

The circuit creates negative resistance in the following manner. Current in the reference arm of the IA impresses a voltage across R3 that is amplified and inverted by IC11. This voltage is fed back to the op amp's noninverting input. The inverting input must follow the noninverting input, so the voltage presented to the IA is in opposite sense to the direction of the current, and the circuit simulates negative resistance. The polarity of this resistance and its magnitude are determined by the two feedback paths of the amplifier and are balanced by potentiometer Rv1.

To overcome the lack of offset-adjustment pins on the op amps, you sum a dc signal into this CMR-adjustment circuit by using Rv2 and the 150-kΩ resistor. Because the adjustment alters the circuit resistance, degrading CMR balance, you should perform the offset trim first.

**Quad improves IA performance**

You can also use the fourth amplifier in a 3-op-amp IA to obtain the higher swing of a differential output with improved frequency response. You create a differential output by paralleling the difference amplifier with a second identical stage, as in Fig 6. The input connections to this second stage are reversed so that they generate an opposite-phase output signal.

This configuration takes advantage of the matching characteristics of quad op amps. Because the amplifiers are on the same chip, they have well-matched gain and bandwidth characteristics. Therefore, the phase differences and time delays associated with the output stages are closely matched. Unacceptable deviation errors occur at a considerably higher frequency in a circuit that uses a quad op amp than in a single-op-amp implementation. (For circuits that use the OPA404, this frequency can be as great as 100 times higher than that for single-op-amp implementations.)

This differential configuration doubles the output voltage swing without your having to resort to specialized amplifiers and power supplies. One single-ended op amp of the OPA404 is capable of delivering 26V p-p with ±15V supplies; the differential output boosts that figure to 52V p-p.

Of course, doubling the output voltage swing quadruples the output power requirements for a given load. However, when you're using the OPA404, you can only double (at best) the maximum available output power, because the amplifiers have output current limits. It is the quad amplifier package's dissipation capabilities that dictate maximum power output. For resistive loads, the package's internal dissipation equals the quiescent current, plus the average load current, times the power-supply voltage, minus the average load voltage. The OPA404's internal dissipation can be as high as 1W.

**Differential mode yields greater bandwidth**

An additional benefit of converting the IA output to differential mode is that you obtain greater bandwidth. Doubling the output swing also doubles the voltage gain without increasing demands on the gain-bandwidth products of the input amplifiers. Therefore, for a given gain requirement, the input amplifiers need only supply one half of the closed-loop gain, which doubles the bandwidth. However, the gain doubling restricts
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EDN September 3, 1987
An instrumentation amplifier with a differential output doubles the output voltage swing while minimizing differential phase error.

the minimum IA gain to 2 instead of 1.

Fig 7 illustrates the use of a fourth op amp in some other IA applications. Fig 7a shows a guard-drive-amplifier design, a circuit that’s often used to drive the shields of the input cables with the common-mode signal. This scheme uses the cable capacitances to neutralize the common-mode signal, improving CMR.

You derive current (rather than voltage) output from an IA by bootstrapping that amplifier with a voltage follower, as Fig 7b shows. This configuration floats the IA and resistor $R_s$ on top of the voltage developed at the load.

An inverting amplifier following the IA can provide filtering without your having to add capacitors to the IA, and thus without degrading CMR (Fig 7c). That added amplifier also gives you the opportunity to add gain, thus reducing the gain demands on the IA and improving the overall bandwidth.

Applications for the spare op amp

Besides improving IA applications, the spare op amp of a quad can also benefit a number of other types of circuit segments. Chances are you already use quad op amps for many circuits that require only three op amps, because the purchase and installation costs for a quad are lower than those of multiple-package alternatives that provide just three op amps. Unless you can stretch that fourth amplifier into some adjacent circuitry, you probably tend to leave it idle. By adding only a few more resistors, however, you can turn that idle amplifier into a performance booster for the other three op amps. The amplifier can remove dc input errors, boost output-signal level, or increase bandwidth.

An amplifier’s bandwidth expands in a straightforward manner when you split the high gain of a given stage into two stages. To obtain maximum bandwidth, you must make the gains of these two stages equal to the square root of the original gain ($\sqrt{A}$). The net gain, $A$, is unchanged, but the bandwidth increases by approximately $0.64\sqrt{A}$. For a gain setting of 1000, the bandwidth will increase by a factor of 20.

You can improve the amplifier’s slew rate by converting the amplifier’s output to the differential mode, as in the design in Fig 8a. $IC_{1A}$, $R_1$, and the upper $R_2$ resistor form a noninverting amplifier. Instead of returning $R_1$ to ground, you connect $R_1$ to the current-to-voltage converter formed by the spare amplifier ($IC_{1B}$) and $R_F$, where $R_F$ equals $R_2$. This connection causes the feedback current of the original amplifier to develop a second, out-of-phase signal at the new amplifier output. The differential output now slews twice as fast as a single-ended stage does, because the signal level has been doubled. Because the gain has also been doubled, you can expand the bandwidth by a factor of two by readjusting this parameter. The one restriction on this differential output is that the load must float between the two amplifier outputs instead of being referred to ground.

![Diagram](image_url)

**Fig 8**—By putting a spare op amp to work, you can boost output voltage by means of a differential output (a) or boost output current by means of a current amplifier (b).
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Chances are you already use quad op amps for many circuits that require only three op amps, because of the quad's lower price and installation cost.

Another application of the spare fourth op amp doubles the output current (Fig 8b). Again, the amplifier stage comprising IC_{1A}, R_1, and R_2 is altered by the inclusion of a second amplifier, IC_{1B}. Connecting the latter as a current amplifier with sense and feedback elements R_3 and R_4 boosts the current available to the load. Current I_1, supplied by IC_{1A}, develops a voltage on R_3 that is sensed by IC_{1B}. IC_{1B} delivers an additional current, I_2, which develops a matching voltage on R_4, doubling the available load current when R_3 and R_4 are equal. Note that the elements of the added amplifier are inside the feedback loop of the original circuit, so IC_{1A}'s open-loop gain diminishes the importance of the added dc errors. This use of an additional amplifier in the feedback loop might make you concerned about the frequency stability, but the low-impedance feedforward voltage of R_3 bypasses the effect of the cascaded amplifiers.

Compensate for dc errors

In general, you can also use the spare op amps of a quad to compensate for dc errors. Signals generated by those amplifiers compensate for the effects of both offset voltages and input bias currents (Fig 9). Quad-op-amp packages have a limited number of pins, and they lack the usual provision for offset-voltage adjustment. These limitations are not major ones for inverting amplifiers, because you can simply sum in an offset-correcting signal. Noninverting connections lack this convenience, however, because the gain becomes a function of the adjustment of the offset-correction circuitry.

To avoid that interaction, you can apply an offsetting dc correction voltage to the normal feedback network of a noninverting amplifier (Fig 9). IC_{1A} represents the typical noninverting amplifier connection, and IC_{1B} provides the offsetting voltage via a variable input bias voltage. The signal does not reach the adjustment resistors, because they are isolated by IC_{1B}. However, the noise and offset-voltage drift of the added stage are not isolated; in the quad-op-amp implementation, these errors will increase by a factor of √2.

Author's biography

Jerald G Graeme is manager of instrumentation-components design at Burr-Brown Corp (Tucson, AZ), where he directs a linear-IC development group. During his 21-year tenure at the company, Jerry has been granted eight patents. He has authored numerous articles and books on op amps. Jerry holds a BSEE from the University of Arizona and an MSEE from Stanford University. In his spare time, he enjoys photography, scuba diving, and woodworking.
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Solid-state devices ease task of designing brushless dc motors

The solid-state devices available today—linear driver ICs, sense-cell MOSFETs, and fourth-generation power MOSFETs—make motor-drive control circuitry less complex, more efficient, and more compact. With such devices, brushless dc motor drives appear more attractive as a systems solution.

Daniel Artusi and Warren Schultz, Motorola Inc

Brushless, fractional-horsepower dc motors are gaining in popularity. They boast characteristics similar to brush-type dc motors, but they don’t have the drawbacks associated with the brushes needed to apply power to the rotor through the commutator. Nor do they suffer from the speed-control problems typically associated with ac induction motors. Rather, they have a broad speed range, linear speed/torque curves, high starting torque, and high efficiency.

Historically, the prevailing tradeoffs involved the cost, complexity, and efficiency of the commutation and control electronics required to drive the motors. Today’s dedicated control ICs significantly reduce the drive complexity and are capable of exploiting the potential of today’s power MOSFET output devices. In addition, current-sensing power MOSFETs offer a more efficient and cost-effective way of detecting overload conditions in brushless-motor drives.

The drive-circuit design example presented here takes advantage of the capabilities of these solid-state devices. The circuit includes commutation logic, speed control, the brake function, current limiting, output drivers, and self-protection networks.

Fig 1 shows the motor-control circuit. The MC33034 IC’s integrated logic decodes the rotor position input signals from the motor’s three position sensors into the sequence required to drive six external power transistors connected in a push-pull configuration. Three IC outputs (AT, BT, and Cn) control the top supply-rail side, and three other signals (AB, BB, and Cn) control the bottom supply-rail side.

The three top-side outputs sink an output current of 50 mA max, have a 50V min breakdown voltage rating, and drive either bipolar power transistors or p-channel power MOSFETs. The three totem-pole bottom drive outputs sink and source 100 mA max and drive external npn bipolar power transistors or n-channel power MOSFETs. To minimize internal dissipation during pulse modulation, the bottom-side outputs have typical rise and fall times of 150 nsec.

The bottom drive outputs have a separate powersupply input (Vc) to provide more system-design flexibility. Suppose, for example, that the motor operates at 24V while the specified gate-drive voltage for the power MOSFETs is 12V. You can still apply the 24V to the motor and the IC’s main sections, and power the output stage with a simple regulator implemented with a zener diode and resistor at pin 18 (Fig 1). The undervoltage lockout circuit monitors this input and disables circuit operation if the gate-drive voltage drops below 9.1V,
Brushless dc motors have a broad speed range, linear speed/torque curves, high starting torque, and high efficiency.

Eliminating the possibility of underdriving the power MOSFETs.

If you want to use the bottom-side outputs to drive the base of bipolar power transistors, connect \( V_c \) to the MC33034's main supply input pin. The separate drive ground (pin 16) reduces the effects of switching noise on the current-sense input, which is important when you're driving MOSFETs with current-sense outputs. Most of the MC33034's inputs and outputs are TTL compatible, and many of the inputs include pull-up resistors to minimize external component requirements.

You can use optoelectronic or Hall-effect devices for the position sensors. The three sensors' output signals indicate six possible rotor positions, which the internal position decoder uses to properly sequence the top and bottom drive outputs. The sensor inputs are TTL compatible with typical thresholds of 1.4V. The sensors themselves can generate eight possible codes, but two are invalid. If the MC33034 receives one of these invalid codes, the on-chip diagnostic circuit will generate a fault signal (indicating a short or open in the sensor array) that disables the drive outputs. With six valid input codes, the decoder can resolve rotor position to within 60 electrical degrees.

The forward/reverse input changes the motor-rotation direction by reversing the voltage across the stator winding. When this input changes from high to low because of a given sensor input code (100, for example), on-chip circuitry exchanges the enabled top and bottom drive circuits with the same alpha designations (A_T to B_T, C_B to C_T), effectively reversing the commutation sequence.

The output-enable pin provides motor on/off control. When the pin's open, an internal 20-µA current source brings this input to a high state, and the logic can sequence the top and bottom drive outputs. When the pin's grounded, the top outputs turn off and the bottom outputs are forced low. This action causes the motor to coast and activates the fault signal.

---

![Diagram](image)

**Fig 1**—In this control circuit, the MC33034 decodes rotor-position input signals from the motor's three position sensors into the signal sequence required to drive six external power transistors.
An on-chip PWM circuit takes care of the motor-speed control. This circuit includes a sawtooth oscillator, PWM comparator, error amplifier, and PWM latch. The top- and bottom-side outputs both turn on and off to commutate the appropriate windings as the rotor moves; the bottom-side outputs also supply constant-frequency, variable on-time PWM to the motor (Fig 2).

The duty cycle is proportional to the difference between the error-amplifier output and the sawtooth signal. For a 0 to 100% duty cycle, this error signal must be able to vary between the sawtooth signal’s valley voltage ($V_v=1.5V$) and peak voltage ($V_p=4V$). $R_T$ and $C_T$ establish the sawtooth-oscillator frequency. $C_T$ charges from the reference output through $R_T$ and discharges through an internal saturated transistor.

This PWM scheme is more power efficient and provides better speed control (especially at low speeds) than do conventional linear control schemes. It’s more efficient because the output devices turn off when the motor reaches operating speed. The speed control is better because the PWM scheme always supplies a constant voltage amplitude; traditional linear-control methods reduce the magnitude of the output voltage. A lower voltage may not be high enough to allow the motor to generate sufficient torque to move its rotor at low speed.

**Overload protection is built in**

The MC33034 includes a current-limiting circuit that controls overcurrent conditions caused by a motor overload or a failure in the output-power circuitry. (You can also use this current-limiting feature to operate the motor in a constant-current mode.) Use a small-value resistor ($R_{SHUNT}$) as the current detector. If you connect $R_{SHUNT}$ between the power-drive device’s emitter or source and ground, you can monitor the entire motor-winding current flow. A voltage comparator in the MC33034 compares the voltage drop across the shunt resistor with an internal 100-mV reference voltage. Whenever the load current reaches a predetermined user-specified value, the comparator output turns off all the outputs and keeps them off until the sawtooth oscillator resets the latch in the next PWM cycle.

**The ability to stop is important**

Braking capability is important in many positioning and motion-control systems. The MC33034 provides dynamic braking whenever the brake input pin is high. A high signal turns all bottom drivers on and all top drivers off. This creates a back-EMF current, which flows into the ground connection through the three power transistors and generates braking torque that forces the motor to a quick stop.

The brake function overrides all other functions so it can stop the motor in case of an emergency. During a braking sequence, the resistance of the conducting bottom transistor and the motor-winding resistance are the only factors limiting peak current. Therefore, you must choose the bottom power switches carefully to make sure that the current doesn’t exceed device ratings. If the motor is running at maximum speed and has no load, the back EMF can be as high as the supply voltage, and the peak braking current may be twice as high as the motor stall current at the start of the braking cycle.

To supply the speed reference voltage and to power Hall-effect switches in low-voltage applications, you can use the temperature-compensated reference-voltage regulator on the MC33034. This reference voltage is fixed at 6.25V (±5%) over temperature, has a temperature coefficient of less than 100 ppm, and provides an output-current capability in excess of 20 mA. The regulator has current-limiting protection during overload or short-circuit conditions to protect the IC from catastrophic failure. If this output shorts to ground or gets pulled below 4.5V, an on-chip undervoltage lockout halts the system.

You can use an external npn power transistor as an emitter-follower if you need to boost the output current. The 6.25V reference level is adequate for powering Hall-effect sensors, even when you take the $V_{BE}$...
PWM is more power efficient and provides better speed control than conventional linear control systems.

drop of the external series-pass transistor into account. This approach lets you power the Hall-effect switches and other ancillary circuits from a low voltage source.

High temperatures cause no problems

The MC33034 has on-chip circuitry that protects both external components and the chip itself. For example, an integral thermal-shutdown circuit will turn off all the output drivers if the IC’s maximum junction temperature is exceeded. When the shutdown circuit activates (typically at 170°C), the MC33034 acts as though its enable pin is at ground level. If the MC33034 is physically close to the motor and the power output stages, it can also protect these components.

A triple undervoltage-lockout circuit will shut down all output drivers if the supply voltage to the IC or the bottom drivers falls below 9V, or if the reference-voltage output falls below 4.5V. This prevents abnormal or unpredictable chip operation, and also prevents damage to the IC and external power-switch transistors. It guarantees that the IC and sensors are fully functional under low-supply conditions, and that there is sufficient bottom-drive output voltage.

All these abnormal conditions (as well as the two illegal position-sensor codes) will turn on the fault output. The open-collector fault output provides diagnostic information when a system malfunction occurs. It has 16-mA sink-current capability and can drive an LED to provide a visual fault indication. The fault output is active low whenever any of the following conditions exist: The enable input is at logic zero; there’s an illegal sensor input code; the thermal-shutdown circuit is enabled; the supply voltage falls below 9.1V; the reference voltage is less than 4.5V; or the current-limit input exceeds 100 mV.

If you connect the fault output to the enable input, any of these fault conditions will stop the motor. An RC network located between the fault output and the enable input will compensate for high start-up currents by delaying a fault-output signal from the current-limiting circuit when it detects excessive currents. The RC network will allow the MC33034 to ignore short-duration fault conditions; if the fault lasts longer than the RC network’s time constant, the system will shut down and will have to be reset manually.

System-configuration decisions are next

Closed-loop systems offer better performance than open-loop ones, but they also entail additional design considerations. The MC33034 is primarily an open-loop control circuit, but it does include on-chip functions to aid the implementation of closed-loop systems. A fully compensated op amp, which is also configured as an integrator, can operate as an error amplifier. A user

![Diagram](image-url)

Fig 3—Although the MC33034 is basically an open-loop device, you can operate it in a closed-loop system.
can access both inputs and the output, and thereby configure a closed-loop system.

One way to do this is to feed the speed-sampling signal to the inverting input of the error amplifier. The on-chip reference regulator will supply the voltage value needed for the speed setting of the error amplifier's noninverting input. If you use the rotor-position sensors as a tachometer, differentiate each of the pulses, and then integrate them over time, you can generate a voltage that's proportional to speed. The error amplifier will compare this voltage to the speed-set voltage to provide PWM control.

For tighter speed regulation, you can use the MC33039, a closed-loop speed-control adapter specifically designed for use in brushless dc motor control systems. Using this 8-pin IC with the MC33034, you can achieve precise speed regulation without using a magnetic or optical tachometer.

The MC33039 monitors the brushless motor rotor-position sensors, digitally detects each sensor signal transition, connects them via an OR gate at the latch-set input, discharges C_T, and generates an output pulse at the f_OUT pin. This pulse has a well-defined amplitude and programmable width (determined by the values of R_T and C_T). The average value of the output pulse train will increase with the motor speed. Feeding this signal through a lowpass filter or integrator, you generate a dc voltage that's proportional to speed.

Fig 3 illustrates how to connect the MC33034 properly in a typical closed-loop application. With the error amplifier in the MC33034 configured as an integrator, it's possible to achieve constant speed down to 100 rpm. Output pulse amplitude is constant with temperature and is controlled by the supply voltage on V_CC. Typically, you can derive this voltage from the V_REF output of the MC33034; the MC33039 provides an 8.25V shunt zener regulator for systems that have no regulated power supply.

**Power-stage designs are simpler**

Current sense-cell MOSFETs (called SenseFETs) significantly improve overcurrent protection in brushless motor drives. The MC33034 is designed specifically to work with these devices in the lower-half positions of a 3-phase bridge. Thanks to this design, sense power is reduced by an order of magnitude, and the cost and board space associated with power sense resistors are eliminated (the scheme requires only one ¼W sense resistor).

In the top half of the bridge, fourth-generation n-channel MOSFETs have the kind of drain-source diode characteristics that a motor bridge needs. Commutating SOA exceeds maximum diode current ratings at BV_DSS, and reverse recovery time is less than 100 nsec. This combination of characteristics eliminates the need for series-blocking and parallel fast-recovery diodes—devices typically required with first-generation power MOSFETs. From a systems point of view, an MC33034 front end maximizes these advantages because it has an architecture that lets you bootstrap the upper n-channel devices.

**Sense-cell FETs minimize insertion losses**

Sense-cell FETs eliminate the insertion loss normally associated with power sense resistors, and they interface readily with the MC33034. As Fig 4 illustrates, you can tie all three sense-cell-FET mirror terminals together and feed the signal to the MC33034's current limit input.

A dual source arrangement in each sense-cell FET splits motor current into power and sense components. Of the FET's individual cells, 99.9% are tied to the conventional source pin; motor current flows directly to ground through these cells. The remaining 0.1% have source connections that tie to the mirror terminal internally and to R_SENSE externally. The power-cell to mirror-cell ratio and the value of R_SENSE combine to determine the sense current. Low R_SENSE values (which equate to low sense voltage values) improve measurement accuracy. For this reason, the MC33034's current-limiting threshold is set at 100 mV.

Because only one bottom transistor is on at a time, you can easily connect all three mirror leads into one sense resistor. With this arrangement, you reach a current-trip threshold if excess current appears in any of the three phases. If you insert a single-pole RC filter between the sense resistor and the MC33034's current-limiting comparator, you'll eliminate the noise spikes that inevitably occur at R_SENSE.

There are three sources for these spikes: reverse recovery current from the upper freewheeling diodes, capacitive coupling within the sense-cell MOSFETs, and a transition spike caused by higher sensing gain in the linear transition region. Fortunately, this noise usually lasts less than 100 nsec and is easy to filter out. Filter time constants on the order of 1 to 10 µsec adequately suppress the noise, and they are consistent with a power MOSFET's ability to withstand large overload currents for a short period of time.

You can use the sense-cell FET's drain-to-mirror
Braking capability is a very important function in many positioning and motor-control systems.

On-resistance ($r_{DMON}$) and drain-to-source on-resistance ($r_{DS(ON)}$) to derive a rough value for $R_{SENSE}$. Current limit occurs at 100 mV, and

$$V_{SENSE} = I_D \cdot r_{DS(ON)} \cdot R_{SENSE} / (r_{DMON} + R_{SENSE}).$$

Therefore, current limit (in amps) occurs at

$$I_{LIMIT} = 0.1(r_{DMON} + R_{SENSE}) / r_{DS(ON)} \cdot R_{SENSE}.$$  

A rather complex debiasing effect occurs as the value of $R_{SENSE}$ increases and limits the accuracy of this calculation. In such cases, data-sheet curves will provide better results.

N-channel FETs complete the bridge

P-channel FETs or pnp Darlingtonso are the easiest power devices to use in the top half of the output bridges, but both have serious drawbacks. A Darlington's minimum saturation voltage causes problems in low-voltage systems. Moreover, its collector-to-emitter diode's multimicrosecond reverse recovery time is less than desirable at any voltage. P-channel MOSFETs don't have any obvious limitations, but do exact a significant cost penalty.

If you can bias fourth-generation n-channel MOSFETs economically, these devices are a much better choice. The reasons are quite straightforward. In addition to very low on-resistance, fourth-generation n-channel MOSFETs have drain-source diodes that are extremely compatible with motor drive needs: They are both fast and rugged. Reverse recovery times are comparable to discrete fast-recovery rectifiers—typically tens of nanoseconds. The drain-source diodes will commutate full-rated drain current through voltages to $BV_{DSS}$. This ability shows up in a commutating safe operating area (CSOA) curve that is bounded by $BV_{DSS}$ and the maximum specified drain current.

Two factors make it easy to bias fourth-generation n-channel devices: the MC33034's architecture and the configuration of a brushless dc motor's windings. Fig 4 illustrates an economical bootstrap bias scheme that

---

**Fig 4**—Sense-cell MOSFETs are well suited for brushless dc motor drives, and they interface readily with the MC33034.
takes advantage of both. The MC33034's 15V supply charges bootstrap capacitor C, through D, whenever Q4 is on, and phase A's output voltage is in a low state. When Q4 turns off, D back-biases as phase A's voltage rises. With D back-biased, C maintains its voltage and provides a bias that floats above the motor rail and turns Q4 fully on. The other two phases operate in a similar fashion.

In some types of applications, this bootstrap technique has refresh limitations. Periodically, you have to refresh the charge on the capacitor to provide bias for the upper devices. In brushless motor drives, normal commutation of the motor refreshes the bootstrap capacitors, making the scheme quite attractive. However, there are conditions that require careful consideration.

At startup, there is no charging path for the bootstrap capacitors until one of the lower output transistors turns on. This transistor will charge its corresponding bootstrap capacitor, but it will provide no direct charging path for the other two phases. Because the upper transistor in one of these other phases must turn to get the motor rolling, you'll have to initially charge all three bootstrap capacitors.

The brushless motor's winding configuration will handle this task in low starting-torque applications such as fans and blowers. Assuming that all three upper devices are off, both wye and delta structures allow one lower transistor to pull down the voltage at all three phases. This assumption is valid until low motor voltages charge all three bootstrap capacitors and the appropriate upper leg turns on. At this point, the motor starts to turn, and Q4, Qb, and Q4, alternately turn on to provide the refresh. The level shifter in Fig 4 aids this process. The shifter requires no bias current (other than leakage) from the bootstrap capacitor whose upper transistor is on.

The MC33034's brake design can also aid startup. Applying a logic one to pin 23 turns off all three upper power transistors and turns on all three lower devices. This action, of course, charges all three bootstrap capacitors. To start high torque loads, simply apply a short pulse to the brake input.

Similar considerations apply to stall conditions and again, the level shifter's design is a key factor. You achieve maximum performance when you turn off a ground-referenced current sink to turn on each upper transistor. With this topology, the bootstrap capacitor only has to supply leakage current to keep an upper device on. As a result, hold-up times on the order of minutes are easily possible. With the level shifter and the 10-µF capacitors shown in Fig 4, the hold-up time is approximately one minute. The MC33034's brake design also simplifies stall recovery. A logic one at the brake pin will simultaneously limit dissipation and provide maximum breakaway torque when you attempt to make a restart.

µC enhances control characteristics

As mentioned earlier, brushless dc motors are finding their way into equipment that requires low-cost intelligent motor control. On the low end of the scale is the reversible motor being used in household appliances. A somewhat more sophisticated example is an automotive air-conditioning evaporator, where the brushless dc motor must automatically adjust the fan speed to maintain a constant temperature within the vehicle. This level of control requires a closed-loop feedback circuit to maintain the correct speed for a constant temperature. On the high end of the scale (a control loop or an intelligent garage door opener), the control system's complexity may well require the use of a single-chip µC.

A single-chip µC, with internal nonvolatile memory, will also add flexibility to the control system. The µC can perform many tasks that historically have not been economically feasible. For example, you can use the
memory to store user preferences for specific motor-system settings. You can also use it for multilevel speed control, controlled start and/or stop, locked rotor timeouts, or as an interface to data networks through serial communication channels.

In essence, the µC manages the entire brushless motor system. In the example of Fig 5, the MC68HC11 µC is configured with the MC33034 and six power MOSFETs. Three of the MTP10N10M FETs have a built-in current-sense capability. After going through conditioning circuitry, these current-sense signals (which represent a normal motor condition or a motor overload condition) feed back to the A/D converter in the MC68HC11 and to the MC33034. When the MC68HC11 detects a motor overload, it counts the overload as an event and initiates a predetermined course of action.

The µC timer allows the overload to continue for a period of time based on how much time has elapsed since the last overload. This wait period accommodates the heat buildup that occurs when the motor overloads or stalls on a repetitive basis. The timer allows the motor to have a high starting torque when cold, but it protects the windings, bearings, and drive electronics when the motor's temperature has become dangerously high because of repeated starts with a faulty load. EDN

Authors' biographies

Daniel Artusi is a director of marketing at Motorola Inc (Phoenix, AZ) responsible for power transistors, power MOSFETs, and power MOS ICs. With the company 10 years, he is a member of IEEE. In his spare time, Daniel dabbles with personal computers and photography.

Warren Schultz is a principal engineer at Motorola Inc. In this position, he investigates applications for power transistor and smartpower ICs. With the company 15 years, Warren holds a BSEE degree from Lehigh University and an MBA from Arizona State University. Warren has two patents pending for his work with the company's smartpower transistors.

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Although the LED-display driver circuit of Fig 1 includes several ICs, it costs only half as much as a single-IC version—Intersil’s ICM7228, for instance. What’s more, the multiple-IC circuit lets you display letters and segment combinations unattainable with the single-IC circuit. You can implement Fig 1 if your system’s unregulated supply has a little excess capacity; if the µP has a little extra processing time; and if you have access to a handbook or application note that contains the display-driving code for that µP.

IC’s quiescent current is relatively high (70 mA max), but the display’s segment currents come from the power supply’s unregulated side. If necessary, you can further unburden the regulated 5V output by choosing a lower-current 74LS145 decoder. The LS145’s higher V<sub>C</sub><sub>ON</sub> may cause a problem, however. (A CMOS 74145, if available, would eliminate concern over the quiescent current.)

As shown, three lines from the µP enable IC<sub>5</sub> to drive eight display characters. Each line can sink as much as 80 mA. For an efficient and attractive display, you should keep the scan rate high and the blanking time short. (The IC is capable of scanning as many as 10 lines, and these lines can drive a keyboard as well as the display.) IC’s CLK input requires a signal with fast transitions, so you should use an HC00 or equivalent for IC<sub>6</sub>; a CMOS 4011 is too slow. Connecting the output-enable input (OE) to the System-Reset signal gates the display off until the µP is reset. To display a decimal point or other indicator, add a discrete npn transistor and another 100Ω resistor.

The transistor array may need a heat sink if the unregulated voltage is high. Connect bypass capacitors close to the IC and, to further reduce noise, run the power-supply traces in parallel to pins 5 and 15 where possible.

To Vote For This Design, Circle No 747

*Fig 1—Operating under microprocessor control, this low-cost, 8-character, LED-display driver lets you display any combination of character segments.*
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D/A converter generates ramp waveforms

J Millar and TG Barnett  
*The London Hospital Medical College, London, UK*

Fig 1's circuit uses a 12-bit, CMOS D/A converter to generate precision ramp and triangular waveforms. Developed as a stimulus for instrumentation in electrochemical research, the waveforms have low offset and low offset drift over time.

A CMOS-compatible, 3.2768-MHz oscillator (not shown) drives the 12-stage, ripple-carry binary counter (IC). In turn, IC's Q output (1.6384 MHz) drives the cascaded 4-bit binary counters (IC, IC, and IC) in parallel. The counters' three groups of four output bits drive the D/A converter, IC.

If the Q output of IC (indicated by a dashed line) drives the 4-bit counters' U/D (Up/Down) inputs, the circuit will produce a 200-Hz, triangular waveform (Fig 1).

**Fig 1**—This circuit's 4-bit counters drive a 12-bit D/A converter, which produces precision ramp and triangular waveforms.
2. If you connect the counters' U/D inputs to 0 or 5V, the circuit will produce a repetitive rising- or falling-ramp waveform (also shown in Fig 2).

Most D/A converters produce a voltage glitch at the major-carry code change; for Fig 1's circuit, the glitch occurs at the up/down transitions. You can eliminate this glitch by avoiding the major-carry code change, which occurs at count 2048. (For example, to drive the U/D inputs, use IC7's Q4 output instead of Q3.)

To Vote For This Design, Circle No 748

---

Fig 2—Depending on how you connect the pins in Fig 1, you can achieve triangular or ramp waveforms.

---

Flip-flop debounces mechanical switch

Al Turing
Thwing-Albert Instrument Co, Philadelphia, PA

The circuit of Fig 1 is suitable for use with the manual-interrupt switch in a µP system. By debouncing the NC contact of a pushbutton switch (S1), the circuit ensures that VOUT produces only one negative pulse each time S1 is depressed. (For active-high interrupts, you can use the flip-flop's Q output.)

S1 is spring-loaded in the NC position as shown, which holds the reset input (pin 1) low, and which in turn holds VOUT high. When depressed, S1 momentarily switches to the NO position and pulls the flip-flop's CLK input low (with no effect on VOUT). The NO closure breaks as you withdraw your finger, and the resulting low-to-high transition clocks in the data input (D=1), which drives VOUT low. VOUT returns high when S1 returns to the NC position. Any bouncing at that time has no effect on VOUT because the CLK input remains high.

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---

Fig 1—By debouncing the pushbutton switch's NC contact, this flip-flop circuit ensures a single pulse from VOUT each time the pushbutton switch (S1) is depressed.

---

EDN September 3, 1987
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Prices (ea.): P $9.95 (6-49), B $24.95 (1-49), N $27.95 (1-49), S $26.95 (1-49)

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<td>Min. 20dB Stop Frequency (MHz)</td>
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<td>460</td>
<td>520</td>
<td>570</td>
<td>660</td>
<td>720</td>
</tr>
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</table>

Prices (ea.): P $12.95 (6-49), B $27.95 (1-49), N $30.95 (1-49), S $29.95 (1-49)

Prefix P for pins, B for BNC, N for Type N, S for SMA
DESIGN IDEAS

Frequency divider generates 50% duty cycle

Andrzej Partyka
Ademco, Syosset, NY

Fig 1 is the general representation of a digital frequency divider that divides by any odd number \((M = 2N - 1)\) and always produces an output with a symmetrical duty cycle. (The duty cycle for an ideal waveform is \(t_L/(t_L + t_H) = t_L/T\), where \(L\) and \(H\) refer to the low and high portions of the waveform, and \(T\) is the period). The duty cycle of the divide-by-\(N\) circuit’s output can range from \(1/2N\) to \((1 - 1/2N)\).

Fig 2a shows the same divider circuit for the case \(M = 3\) (and therefore \(N = 2\)). Because the duration of each half period at \(V_{OUT}\) is \(1\frac{1}{2}\) CLK periods, one output period equals three input periods. Note that you can simplify some applications by using the Q outputs for the A and B waveforms (in place of Q).

To divide by a higher odd number such as 9 (\(N = 5\)), you can use any available divide-by-5 circuit—e.g., the 74XX90 decade counter in Fig 2b. The output duty cycle of the internal divide-by-5 circuit will not affect the output symmetry of the overall divider.

By adding an AND gate, you can build a programmable circuit that divides by any integer greater than 2 and produces a symmetrical output (Fig 3). The delay through a long divider chain, however, limits the maxi-
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DESIGN IDEAS

mum CLK frequency; that is, the sum ($t_{SUM}$) of the propagation delays in the XOR gate, N-divider circuit, 2-divider circuit, and Control gate must be less than one-half the CLK period ($t_{CLK}/2$).

You can increase the maximum CLK frequency by adding a flip-flop (Fig 4). In this configuration, only the lower of two constraints ($t_{FF}<t_{FF/2}$ and $t_{FF}+t_{SUM}<(N-1/2)t_{CLK}$) limits the CLK frequency. A circuit using LSTTL logic, for example, imposes a 5-MHz limit on Fig 3 and a 12.5-MHz limit on Fig 4.

Fig 4—Adding a flip-flop (IC1) to the Fig 3 circuit enables operation at a higher CLK frequency.

Program converts binary to BCD code

Anthony J Miller
NASA, Greenbelt, MD

BCDCON, the assembly-language subroutine of Listing 1, converts binary-coded numbers to BCD. Developed for use in Z80 and 8085 µP systems, the routine can handle decimal numbers as large as 1,999,999 (1E847F in hex notation). Larger inputs will produce an error. Because the software uses a shift-and-justify algorithm instead of lookup tables, the size of the input number doesn't affect the conversion time.

The routine occupies 24 bytes of memory. It converts eight bits at a time, starting with the most significant byte. Depending on the input magnitude, the BCD results return to the A, B, and C registers and a 1-bit carry digit. To use the routine, you enter the most significant bits.

LISTING 1—CONVERSION SUBROUTINE

```
0030 ORG 30H
0030 BCDCON XOR A
0031 LD B, A
0032 LD C, A
0033 AGAIN DL L, 0H
0034 MORE LD H, A
0035 RLC D
0036 LD A, C
0037 ADC A, A
0038 DAA
0039 LD B, A
0040 LD A, H
0041 ADC A, A
0042 DEC L
0043 JP NZ, MORE
0044 RET
```

; THIS SUBROUTINE CONVERTS BINARY DATA PASSED IN THE D
; REGISTER TO BCD RESULTS WHICH ARE BUILT UP AND LEFT IN
; THE CARRY BIT, A, B, AND C REGISTERS. CONVERSION IS PERFORMED EIGHT BITS AT A TIME. CONVERSIONS GREATER THAN EIGHT BITS ARE PERFORMED BY ENTERING (CALLING) THE ROUTINE AT "AGAIN".

; CLEAR ACC AND FLAGS
; CLEAR B
; CLEAR C
; USE LAST LOOP COUNTER

; SHIFT BY ADC, SET FLAGS
; ADJUST RESULTS

; DEC LOOP COUNTER
; TEST FOR COMPLETION

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LISTING 2—CONVERSION EXAMPLES

Example of use to convert a large number (21 bits):
LD D, (Most sig byte)
CALL BCDCON
LD D, (Next most sig byte)
CALL AGAIN
LD D, (Least sig byte)
CALL AGAIN
(Results are in the carry, A, B, and C)

Example of use to convert a 16 bit number:
LD D, (Most sig byte)
CALL BCDCON
LD D, (Least sig byte)
CALL AGAIN
(Results are in the A, B, and C registers)

Example of use for 8 bit conversion:
LD D, (Byte)
CALL BCDCON
(Results are in the A, B, and C registers)

significant byte of the binary number, call BCDCON, enter the next most significant byte, call AGAIN, enter the least significant byte, and call AGAIN one more time (Listing 2). Calling BCDCON resets the A, B, and C registers for the next conversion.

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<th>G4B</th>
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*No NC contacts

### General Purpose Relays

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- Provides a 2k-byte onboard data buffer

The V-ARC02 is a VME Bus board that allows you to interface VME Bus systems to Arcnet token-passing networks. The board, which is based on the SMC-COM9026 Arcnet controller IC, includes a 2k-byte network data buffer. It operates as a VME Bus slave interface with 8-bit data access to the controller chip and interrupt-control registers, and 8- or 16-bit access to the data buffer. You can locate the board on any 4k-byte boundary within the VME Bus memory space, using either 16- or 24-bit addressing and selectable address-modifier decoding. You can direct the interrupt to any one of the seven VME Bus interrupt levels, and you can program the 8-bit interrupt vector. Two lead-out options allow you to interface to the network via a front-panel BNC connector or via a coaxial lead to a remote, chassis-mounted connector. The vendor is developing driver software for a number of real-time multitasking operating-system kernels and is porting its high-level Cimnet protocols for DEC systems to the V-ARC02 board. This software will allow you to network 68000-based VME Bus systems to DEC systems running RSX or VMS. V-ARC02, $1765.

Comenedec Ltd, 6a School Lane, Hopwas, Tamworth, Staffs B78 3AD, UK. Phone (0827) 286180. Circle No 354

DATA-LINK BOARD
- Provides IBM-3270 emulation
- Implements SNA architecture

The SICC-SNA double-Eurocard VME Bus data-link controller emulates IBM-3270 terminals and printers with SNA (systems network architecture), allowing you to...
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CIRCLE NO 17

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Tel: (415) 961-3901, Telex: 172172, FAX: (415) 969-1409

CIRCLE NO 50

COMPUTERS & PERIPHERALS

implement program-to-program communication and file transfer between VME Bus and IBM systems. The board supports synchronous data-link control (SDLC) or X.25/LLC at the data-link level; at the SNA level, it supports multiple type-2 physical units and as many as 32 type-1, -2, or -3 logical units. In addition to handling SNA commands, the board handles bracketing, chaining, segmenting, and elementing protocols. The board operates as an A32/A24; a D16 VME Bus master; and an A16, D8 bus slave. It also has a VME Bus interrupter. Onboard firmware handles the SNA-level functions, and both data and status information are available to the host system via shared RAM. The vendor offers a driver for the Unix System V operating system and is developing a range of utilities and emulations. Around DM 14,500.

Stollmann GmbH, Max-Brauer-Allee 81, 2000 Hamburg 50, West Germany. Phone (040) 3890030.

Circle No 355

PORT EXPANDERS
- Operate at selectable speeds from 300 to 38,400 baud
- Expand RS-232C port to as many as eight ports

The Data Manager 4x4 and the Data-Net 1551 port expanders are designed for the sharing of printers and plotters with a number of computers and workstations or for intercomputer communications. They are buffered with 256k bytes of RAM (expandable to 1M byte), and they operate at user-selectable speeds from 300 to 38,400 baud. The ROM-resident software consists of
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For applications ranging from consumer goods to industrial controls, P&B relays have the features you need for 1 milliamp through 30 amp switching on your printed circuit board. These cost effective relays meet requirements established by international regulatory agencies. Many models are available from stock, and they’re all built to the same exacting specifications that have made P&B relays the standard of the industry.

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T70 relays are low-cost, SPDT units offering silver or silver-cadmium oxide contacts for loads from 1 milliamp through 10 amps. Available with an immersion cleanable, sealed case.

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RK series relays feature 8 mm coil-to-contact spacing for 4,000 volt isolation. SPDT models switch loads to 20 amps, and DPDT models switch up to 5 amps. Both sealed and unsealed versions are offered.

30A Workhorse
T90 relays have SPDT contacts of silver-cadmium oxide for 30 amp loads or silver for loads up to 15 amps. Available as an open relay or sealed for immersion cleaning. A snap-on dust cover is offered for open models.

Quick Connects, Too
T91 relays feature the same ratings as T90 relays and provide both quick connects and printed circuit terminals for load connections. Sealed and dust cover versions are available. Optional case provides flanges for panel mounting and quick connects for all connections.

Find Out More
Contact us today for details on P&B printed circuit board relays. Call toll-free 1-800-255-2550 for the name of your nearest P&B distributor or sales representative. Potter & Brumfield, A Siemens Company, 200 South Richland Creek Drive, Princeton, Indiana 47671-0001.

Regional Sales:
Braintree, MA, (617) 848-6550; Mission Viejo, CA, (714) 582-1231; Princeton, IN, (812) 386-2130; Bristol, England, (0454) 616263.
six commands that are issued from either a computer or a terminal; according to the manufacturer, these commands offer all the functions necessary to exploit the system's full potential. The Data Manager 4x4 is an 8-port system with four RS-232C ports. You have the option of buying the four extra ports as additional serial ports or as a combination of serial and Centronics-compatible parallel ports. Data Manager 4x4, $795; 6-port RS-232C system, $695.

Integrated Marketing Corp, 1031-H E Duane Ave, Sunnyvale, CA 94086. Phone (408) 730-1112.

Circle No 356

FORTH COMPUTER

- Allows program development in Forth or assembler
- Provides onboard peripherals and interfaces

When connected to a dumb terminal, the TDS9090 single-board computer is a complete Forth language-development system. You can add disk storage for programs by connecting the board to an IBM PC or a BBC computer. The board includes a ROM-resident Forth language kernel and an assembler. By storing generated code in either nonvolatile RAM or EPROM, you can also use the board in a target system. The board is based on the HD63A03YFP µP, and all the µP's on-chip functions—including two timers, synchronous and asynchronous serial ports, and a versatile interrupt system—are available via Forth instructions or via the assembler. Also included on the board are 30k bytes of RAM for storing source code or data, 16k bytes of EPROM/nonvolatile RAM for firmware, 256 bytes of EEPROM, 35 parallel I/O lines, two RS-232C serial interfaces, a watchdog timer, and an expansion-box interface. You can interface the board to an 8x8 key matrix and an LCD, and you can use two of the parallel I/O lines as an I/O interface. The ROM-resident Forth is an extended version of Fig-Forth with Forth words to support all the onboard peripherals, as well as the keyboard and LCD interfaces. The TDS9090 measures 100x72 mm and requires one 6 to 16V supply. It consumes an active supply current of 15 mA typ, and it has a low-power operational mode that reduces current consumption to 3 mA. The development board, complete with an 8k-byte nonvolatile RAM and a single-user Forth license, costs £194.95. Target-system boards are available for £99.95 (25).

Triangle Digital Services Ltd, 100a Wood St, Walthamstow, London E17 3HX, UK. Phone 01-520 0442. TLX 262284.

Circle No 357

I/O ADAPTER

- Adapts three iSBX I/O modules to the IBM PC/AT
- Puts three different I/O functions into a single PC/AT slot

The LSXB-Mother/AT is an add-on board that can interface as many as three iSBX I/O modules to the IBM PC/AT or IBM 7552 computers. It can handle three 8/16-bit iSBX modules, and it supports both the system-interrupt and the DMA features of the iSBX bus. You can route the interrupt and DMA requests.
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CIRCLE NO 102
TAKE A CLOSER LOOK AT MULTIFILAR® MAGNET WIRE.

Whenever two or more magnet wires travel together, MULTIFILAR magnet wire is worth a closer look. This parallel-bonded, color-coded magnet wire offers many benefits for both small and large users.

Engineers should specify it when they’re concerned with space, weight and reliability. Where consistent capacitance and impedance characteristics are needed, MULTIFILAR magnet wire outperforms windings where two separate magnet wires are used.

Production users benefit from increased layer winding speeds, reduced labor and handling. Color-coding assists in conductor identification and reduces termination errors.

MULTIFILAR magnet wires are custom produced by MWS. We guarantee flat, parallel construction in an array of sizes 16 AWG and finer, with up to 20 conductors in some sizes.

Both round and flat constructions are available. Color-coded conductors are available in most insulations with up to 10 different colors in some sizes. Conductor separation is also guaranteed with certain bonding mediums.

For an even closer look, send for a free sample, specifications and ordering information. Production minimums are as low as 500 feet.
from the iSBX modules to any of the 11 interrupt or seven DMA lines available on the PC/AT. The I/O base address is also user programmable. The board allows you to take advantage of the many iSBX modules that have been developed for control applications. Because the board supports three modules, three different I/O functions can occupy a single PC/AT slot, thereby conserving slot space. Three 8/16-bit data-bus iSBX connectors are available. When you add modules, you must take care not to exceed the current available from your system configuration. $199.


Circle No 358

ANSWERING MACHINE

- Board for the IBM PC/XT, PC/AT, and compatibles
- Digitizes caller’s voice and stores it on hard disk

The CAM turns any IBM PC/XT, PC/AT, or compatible PC into a smart telephone-answering machine, according to the manufacturer. Using its onboard µP, the board digitizes the caller's voice and stores it on the computer’s hard disk. Because the device is resident in memory, it is fully operational even when the PC is running other programs. The board requires the following for operation: one expansion slot; MS-DOS or PC-DOS version 2.1 or higher; a hard-disk drive; a floppy-disk drive for initial program loading; a 384k-byte RAM with at least 256k bytes of user memory; an 80-column display and adapter; a standard telephone line capable of Touch Tone operation; and a standard Touch Tone telephone. The board uses a proprietary voice-compression algorithm to store 1 sec of speech in 3k to 3.5k bytes of disk storage space. Some of the features include Multiple-Voice Mailboxes, which allow you to have your own mailbox (with passwords for privacy); Message Forwarding, which allows the device to call you at another location and deliver the message as it is received; Call Transfer, which allows you to transfer calls to another extension instead of leaving a message; and Remote Operation, which allows you to change almost any system parameter remotely from a Touch Tone telephone. $349.

The Complete PC Inc, 521 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 434-0145.

Circle No 359

**NEW!**

**5-500MHz ECL Oscillators**

DIP to 200 MHz

<table>
<thead>
<tr>
<th>Frequency</th>
<th>5-200 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply</td>
<td>-5.2V (-4.5V optional)</td>
</tr>
<tr>
<td>Accuracy</td>
<td>±10, ±15, ±25 or ±50 ppm</td>
</tr>
</tbody>
</table>
| Stability | Std: ±25 ppm over 0°/+70°C  
Opt: ±5 ppm over 0°/+50°C  
±50 ppm over -55°/+125°C |

CO-430 Series

100K ECL to 500 MHz

<table>
<thead>
<tr>
<th>Frequency</th>
<th>150 - 500 MHz</th>
<th>Complementary Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply</td>
<td>-4.5V (-5.2V optional)</td>
<td></td>
</tr>
<tr>
<td>Accuracy</td>
<td>±10 ppm (±1 ppm optional)</td>
<td></td>
</tr>
</tbody>
</table>
| Stability | Std: ±25 ppm over 0°/+70°C  
Opt: ±3 ppm over 0°/+50°C |

CO-233KEQ Series

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The Crystal Oscillator Company

CIRCLE NO 19
DC/DC CONVERTER

- Output sections isolated from the input and each other
- Six-sided shielded case eliminates RFI problems

The 12Q15.050 operates from a 12V dc input and provides two ±15V dc outputs at ±50 mA each. Both dual output sections are isolated from the input and from each other. The unit has a 6-sided shielded case that eliminates RFI problems. The internal switching frequency (63 kHz free running) is unaffected by load or line changes. A switching-frequency synchronization pin lets you run the converters at frequencies ranging from 70 to 110 kHz. The input/output and output/output isolation equals 500V dc, and the operating range spans -25 to +90°C.

$110. Delivery, stock to six weeks ARO.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911. TLX 338506.

Circle No 360

CERMET TRIMMERS

- Can withstand vapor-phase reflow cycles
- -55 to +125°C operating range

The ST-5 and ST-6 Series units are multturn and single-turn trimmers, respectively. They can withstand vapor-phase reflow cycles to 215°C for three minutes and are sealed to prevent immersion problems. The trimmers have 10Ω to 2-MΩ resistance values and operate over a -55 to +125°C range. The maximum input voltage is 200V dc; power rating equals 0.25W at 85°C for the ST-5 and 0.5W at 70°C for ST-6 units. Rotational life specs at 200 cycles. ST-5, $2.82; ST-6, $0.78 (5000). Delivery, eight to 12 weeks ARO.

Mepcopal Co, 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332.

Circle No 361

DISPLAY

- Receives and transmits data at 1200 or 9600 baud
- Integral self-diagnostic test checks display functions

The Model 3601-36-240 is a 6-line×40-character (5×7-dot matrix, 5-mm-high) vacuum-fluorescent display. The unit’s serial input conforms to RS-232C with CTS (clear to send) and DTR (data terminal ready) or to RS-422 standards. It can receive and transmit data at 1200 or 9600 baud. An integral test program checks all display functions. After the test, the module displays its repertoire of 96 ASCII characters. The module will also display scientific, general European, Scandinavian and German characters. In addition, you can define other character patterns and download them into any or all of the ASCII locations. $478 (100). Delivery, four to six weeks ARO.

IEEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 362

RELAYS

- UL recognized and CSA approved
- 100,000-operation lifetime

KHA Series relays are UL recognized and CSA approved. They are available with six different contact materials, in both 2 Form C (dpdt) and 4 Form C (4pdt) arrangements. Contact ratings range from dry cir-
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516-666-8000
TLX: 6711657

CIRCLE NO 51

EDN September 3, 1987
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- 80 direct keyboard commands
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$175

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- Built-in operating system. 12K operating system allows for immediate solutions to complex problems.
- Four input/output ports. Plug in ROM Software modules or add to existing memory capacity with plug-in memory modules.
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- HP41CX:312 bytes of memory or 446 data registers plus time and calendar functions.

HP-41CV
Mfg. Sugg. Ret. $179

$126

HP-41CX
Mfg. Sugg. Ret. $249

$179

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Financial Calculator

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*Price reflects $10 mail-in rebate from Hewlett-Packard.

Mfr. Sugg. Ret. $72

Elek-Tek Price

$62

Your Final Cost

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AMPLIFIER

- Available in TO-8 hermetic package
- Minimum gain of 12 dB

The thermal dissipation characteristics of the UTO-1023 make it very useful in high-density applications. The thin-film amplifier provides a 12-dB min gain (13 dB typ) from 10 to 1000 MHz. Other specifications include an 8.5-dB min noise figure, 24.5 dBm min of output power at the 1-dB compression point, and input and output VSWR of 2:1 max. All specifications are guaranteed over a 0 to 50°C range; slightly reduced specifications apply over the full -55 to +85°C military range. The unit is available in a TO-8 metal and glass hermetic package or in the TC-1 sealed aluminum case with SMA-type connectors. $72.

Circle No 367

OPTICAL MODEM

- Requires no external power-supply connection
- Extends RS-232C limit to 3.5 km

The LDM80 fiber-optic modem is completely powered by the host RS-232C port signals. The unit works with a wide range of fibers. Using 100 µm-core fiber with 4 dB/km attenuation, you can extend the RS-22C transmission limit to 3.5 km. Designed for full-duplex asynchronous operation, the modem provides complete EMI/RFI protection and eliminates ground loops. If the fiber cable breaks, a detector circuit detects the loss of light and puts a spacing condition (or break) on the host system's Receive Data pin. The LDM80 has LED indicators. A switch lets you easily connect to either DTE (data-terminal-equipment) or DCE (data-communications-equipment) ports. The operating range spans -20 to +70°C. $98.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 366

OPTICAL TO Fiber Optic Modems

- All HP Accessories Discounted Too!

Circle No 21

EDN September 3, 1987
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¹IBM PC AT are trademarks of the International Business Machines Corporation.
COMPONENTS & POWER SUPPLIES

POWER SUPPLIES

- Meet VDE, IEC, UL, and CSA standards
- Offer output overload protection and soft start

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Power General, Box 189, Canton, MA 02021. Phone (617) 828-6216.

Circle No 368

DC/DC CONVERTERS

- 6-mV p-p typ noise spec
- −40 to +100°C operating range

These dc/dc converters are pin-for-pin compatible with over 30 competitive models. Output power is 9W max; ripple and noise specs 6 mV typ. Two versions are available: The PWR5104 provides a ±12V output, whereas the PWR5105 has a ±15V output. Both operate from 5V inputs. Their accuracy is 0.5% typ, and their temperature coefficient (over the −25 to +85°C range) is ±0.01%/°C. Both converters feature input and output filtering, a 6-sided shielded case, and output short-circuit protection. The operating range spans −40 to +100°C. The rated isolation voltage is 750V dc min, and the barrier leakage (15 µA rms) is 100% tested at 240V ac. $29.75 (1000).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 369

HIGH SPEED, AUTO INSERTABLE, CMOS

PLASTIC DIP OSCILLATOR!

The new EPSON SG-51 Series plastic dip CMOS crystal oscillator has typical 5 nsec rise and fall times. And it occupies about half the board space of the metal can oscillator it replaces. Both versions of the SG-51, 4-pin and 14-pin, are auto insertable using standard dip equipment, and the 4-pin fits the same hole pattern as metal can types. With tri-state output, low power consumption, high speed and now 4-pin or 14-pin plastic dip... the Crystalmaster is first again!

OUTPUT FREQUENCIES

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>5.0000 MHz</th>
<th>10.0000 MHz</th>
<th>15.0000 MHz</th>
<th>20.0000 MHz</th>
<th>25.0000 MHz</th>
<th>30.0000 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time (nsec)</td>
<td>5</td>
<td>10</td>
<td>15</td>
<td>20</td>
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<td>10</td>
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<td>30</td>
</tr>
</tbody>
</table>

EPSON AMERICA, INC.
OEM Division
Component Sales Department
5415 Kashiwa St, Torrance, CA 90505
Telephone (213) 534-4500 • TELEX 664277 • FAX (213) 539-6423

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OEM Division
Component Sales Department
5415 Kashiwa St, Torrance, CA 90505
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CIRCLE NO 22

EDN September 3, 1987
MEGA BIT EPROM SUPPORT IS HERE

In the full featured Model 2A Programmer from PROMAC

- UNIVERSAL SUPPORT
  Of devices up to 40-pins and up to 4M bits, single chip processors, and even E & E PLDs.

- FAST INTERFACES
  Serial data up to 19.2K baud, 10 popular data formats, full remote control, and a parallel port for fast data transfers — important with the new larger devices.

- SIMPLE OPERATION
  A20 x 2 LCD gives full prompting, and functions can be selected by menu.

- FULL SIZE BUFFER
  A 4M bit (512K byte) buffer is ready for larger future devices. Plus full editing capabilities and 16-bit or even wider data handling.

- FAST PROGRAMMING
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Call today, and be ready for the future.

PROMAC Division
adams macdonald enterprises, inc.
800 AIRPORT ROAD
MONTEREY, CA 93940
TEL.: (408) 373-3607 TLX: 882141

CIRCLE NO 108

EDN September 3, 1987
CONVERTER

- Bidirectional and optically isolated
- Operates on 12V supply

The Model 422CL converter is bidirectional and optically isolated. One channel accepts RS-422A data and outputs current-loop signals; the second channel accepts current-loop data and generates RS-422A signals. A male DB25P connector provides the current-loop interface and a female DB25S connector handles the RS-422A interface. The converter supply requirements are 12V dc at 100 mA. No other power supply is required as long as the existing current-loop interface is active. $44.95.

B&B Electronics Manufacturing Co, Box 1008, Ottawa, IL 61350. Phone (815) 434-0846.

Circle No 370

RELAYS

- Four independent relays housed in one package
- Optical coupling provides 3750V rms input/output isolation

This family of modular devices contains four independent optically coupled 20A solid-state relays in a single industry-standard hockey-puck package. The internal circuit design uses optical coupling to provide 3750V rms input-output isolation, current-regulated 3 to 32V dc inputs, and triac outputs rated at 500V pk with internal snubbers for reliable operation over a 24 to 280V rms load voltage range. Two versions are available: zero voltage turn on and phase-controllable random turn on. UL recognition and CSA certification are pending. $25 (OEM qty). Delivery, stock to six weeks ARO.

Silicon Power Cube Corp, 6015 Obispo Ave, Long Beach, CA 90805. Phone (213) 634-9390.

Circle No 371

TUSONIX

If you’re looking for an economical source for Custom Filter Assemblies

Tusonix’ expertise can reduce your costs with improved PPM quality and yield

When it comes to custom packaging EMI/RFI Feed-Through Filters and/or Filter Capacitors, Tusonix’ in-house assembly capability provides you with a reliable, low cost source. Our expertise in the manufacture and array assembly of quality EMI/RFI Filters and Filter Capacitors results in substantially improved efficiency. Every assembly is 100% tested in Tusonix’ quality assurance laboratories prior to shipment.

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Fax: 602-744-6155

CIRCLE NO 23
NEW PRODUCTS

INTEGRATED CIRCUITS

FILTER

• Provides 10 filter functions
• Conforms to IEEE/Bell and CCITT standards

You can configure the XR-1020 as one of 10 filters, which can characterize telephone lines and other telecommunications links. It conforms to the IEEE standard 743/Bell Systems technical reference 41009 and the CCITT (International Consultative Committee for Telephony and Telegraphy) Series 0 recommendations. The device requires only external 3.579-MHz-crystal and digital control inputs. The repertoire of filter functions includes a C-message and a C-notch filter, a psophometric filter, and an 825-Hz notch filter. The device also functions as a program-weighting filter, 3- and 15-kHz flat filters, a 1-kHz bandpass filter, the lowpass portion of a 50-kbps filter, and a peak-to-average ratio filter. It has a power-down mode for battery-powered operations and comes in a 28-pin ceramic DIP. $63 (100).

Exar Corp, Box 3575, Sunnyvale, CA 94088. Phone (408) 732-7970. TWX 910-339-9233.

Circle No 372

A/D CONVERTER

• 16-bit resolution
• 2-µsec conversion

The ADC1600-2 A/D converter performs a 16-bit conversion in just 2 µsec. Its internal sample/hold amplifier requires another 2 µsec, bringing the conversion time for the

Thermography enters the information

With the advent of the Hughes Aircraft Company Probeye 7300 Thermal Video System, thermal imaging has entered a new age—the Age of Information.

In a single package, the Hughes Probeye 7300 Thermal Video System gives you a powerful, intelligent laboratory system with instant field diagnostic capability. Immediately select, store, quantify and analyze. And, most importantly, understand the information—with more speed and accuracy than ever before! Hughes has leapfrogged the competition with state-of-the-art features that can't be matched by any other system.

Start with superior resolution—240 infrared lines to the inch. Not just on the monitor, but also in the eyepiece of the portable imager. Which means you can perform on-the-spot detection and analysis in up to 128 distinct levels.

All-electric operation does away with liquid nitrogen or argon gas. The imager uses ac or battery power for full field portability—it goes wherever the information originates.

Fully automatic operation allows you to concentrate on detection and analysis. Precise comparisons are facilitated by built-in features. There's no exhaustive training process. No delays. Just point and read. And, the design is extremely functional—in addition to the portable imager and attached CRT viewfinder, the system includes a processor with built-in, full-function keyboard and a high resolution RGB color monitor.
combination to 4 µsec max. The separately controlled, byte-wide, 3-state outputs allow interface to an 8- or 16-bit data bus. The package is a 3.576×5.50×0.062-in. module that has EMI shielding on five sides. The device operates with 5V and ±15V supplies and consumes 7.65W typ. $1120 (100).

Intech Advanced Analog, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. TWX 910-338-2213.

Circle No 373

DSP EEPROM

- 32010-µP architecture and instruction set
- Includes 2.5k bytes of EEPROM

The DSP320EE12 is the industry’s first monolithic digital-signal-processing µP that includes EEPROM, according to the manufacturer. Operating at 20.5 MHz, the CMOS device is pin-compatible with the standard 32010, and it runs software written for that µP. The EEPROM’s ability to accept and store new commands enables the chip to fine-tune its performance without intervention by an operator. Applications for it include intelligent FIR filters, adaptive LANs, equipment diagnostics, and instrument self-calibration. Applications include intelligent FIR filters, adaptive LANs, equipment diagnostics, and instrument self-calibration. The device features an 8- and a 16-bit data interface, special operating modes for improved factory testing, the capability for reprogramming on a standard PROM programmer, and an inhibit circuit that prevents inadvertent data writes during power-up or supply glitches. Security mechanisms prevent unauthorized internal or external access to the EEPROM code. $100 (100).

General Instrument Microelectronics, 2355 W Chandler Blvd, Chandler, AZ 85226. Phone (602) 963-7373.

Circle No 374

MODEM IC

- Includes differential phase- and frequency-shift key functions
- Incorporates both transmit and receive filters

The TSG7515 is a single-chip full-duplex voice-band modem compatible with CCITT V22 A-B, Bell 212A, and Bell 103 standards. Its transmission section includes differential phase-shift keying (DPSK) and frequency-shift keying (FSK) modulation functions, plus transmit...
BEFORE PC-TRON

AFTER PC-TRON

Finally, a fuse that protects the board, Bussmann current-limiting PC-Tron!

Before the Buss PC-Tron, fuses performed a limited function on printed circuit boards. They protected equipment against fault currents, but not the printed circuit board's components; transistors could explode, and traces might vaporize. Until now designers have had to live with these service costs and liability potentials. Now the new PC-Tron fuse greatly reduces these risks. Unlike glass-cartridge and other subminiature fuses, the PC-Tron is current-limiting. Its low let-through energy capability protects the transistor and all board components. With all that, the PC-Tron also reduces production costs significantly. It takes 89% less space than a glass-cartridge fuse and is automatically insertable, board washable and wave solderable.

SEE THE DOCUMENTARY VIDEO

See the PC-Tron fuse in action in a new videotape. See how it can help you to design in circuit protection never before possible and with production economies. For a showing write PC-Tron Videotape, Bussmann Division, Cooper Industries, Box 14460, St. Louis, MO 63176; phone (314) 394-BUSS.
INTEGRATED CIRCUITS

signal filtering. The receive section includes filtering and carrier detection functions, and DPSK and FSK demodulators. The chip also contains a voltage reference, clock generation circuitry, and control registers that allow you to select bit-rate, operating mode, transmission type, character length, overspeed, communication standard, and test-loop operation. The TSG7515 is packaged in a 28-pin DIP and typically consumes less than 100 mW of power. $18 (1000).

Thomson Semiconducteurs, 45 Ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 204780.

Circle No 375

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000. TLX 730643.

Circle No 376

SUPPLY MONITOR

- Monitors three power supplies
- Detects transient faults

The S2862 power-supply monitor can detect positive or negative transients that appear on any one of the three power-supply voltages it monitors simultaneously. The device contains three window comparators with external resistor-programmable switch points, a 2.5V bandgap reference, a hold comparator, and four open-collector output drivers. All four drivers turn on (low) when the chip detects a fault on any of the three supplies, and they remain low for an interval determined by an external hold capacitor. You can set thresholds within 1.25% of desired
MODULA 2
PASCAL

Cross-Compiler Systems

High performance, field-proven software development systems producing extremely compact, fast-executing, ROMable output code.

Each cross-development package includes:

- C, Modula 2, or Pascal Cross-Compiler
- Macro Relocating Cross-Assembler
- Object Code Librarian
- Object Module Linker
- Hexadecimal Format Loader
  (S-Records, Intel Hex, Tek Hex)
- Standalone Support Library
  (EPROMable, with full floating point support)

All languages can be intermixed with assembly language.

Targets supported:

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6801/03
6809
68HC11
68000/08/10/12
68020/881/851
32000/32/81/82

Available for following hosts:

VAX: VMS/UNIX/ULTRIX
PDP-11: UNIX/TNIX/VENIX
68000: UNIX System V
PC, XT, AT: MS-DOS
PowerNode: UTX/32

Siltronic Ltd, 436 Hazeldean Rd, Kanata, Ontario K2L 1T9, Canada. Phone (613) 836-5003. TLX 0533936.

Circle No 377

CMOS ADC

- 12 input channels, one serial data output
- Provides a sample rate of 32,258 samples/sec

The monolithic CMOS TLC1541 is a 10-bit A/D peripheral chip that includes an input 12-channel analog multiplexer, a 10-bit sample/hold A/D converter, and associated control circuitry. One input channel is connected to an internal voltage reference for use in the self-test mode. The device performs a conversion in 21 µsec max. The time for channel access plus conversion is 31 µsec, or 32,258 samples/sec. The output data is in serial format. The chip's maximum clock frequencies are 2.1 MHz for the converter and 1.1 MHz for the I/O. The part operates with a 5V supply and dissipates 6 mW. It comes in a 20-pin plastic DIP or a plastic leaded chip carrier. $7.25 (100).

Texas Instruments Inc, Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 378

CMOS EPROMs

- 35-nsec access times
- 16k-bit and 32k-bit capacities

The WS57C256F (32k-byte x 8-bit) and WS57C257 (16k-byte x 16-bit) CMOS electrically erasable PROMs (EEPROMs) offer 35-nsec access times. This speed matches that of traditional bipolar-type PROMs. The EEPROMs offer low power consumption (350 mW) and in-circuit programmability. The key features include a 10k erase/write cycles/byte (1M cycles typ), a 50-nsec chip erase, 5V operation, and power up/down protection circuitry. In addition, the chips have data-bar polling, a 20-nsec chip-enable output time, a JEDEC-approved pinout, and a latched timer that allows an automatic byte-erase before write. The 38C16 comes in a 24-pin ceramic DIP, and the 38C16 is available in a 28-pin ceramic DIP. Both models are also available in a 32-pin chip carrier: 38C16, $27; 38C32, $38 (100).

Seeq Technology Inc, 1849 Fortune Dr, San Jose, CA 95131. Phone (408) 432-9550.

Circle No 380

INTEGRATED CIRCUITS
Don't Make Your LCD Commitment Until You've Talked to Hitachi

Hitachi Wrote the Book on LCD Technology

Whether you're looking for thorough engineering support, leading edge technology, or high production volume, Hitachi should be your source for LCDs. From our smallest 8-character-by-1 line display, to the 640-by-400 pixel LM252X, every product gives you Hitachi's famous quality and reliability. And now, many displays are available with backlight capability.

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TEST & MEASUREMENT INSTRUMENTS

REFLECTOMETER

- Accommodates two lasers
- Has 28-dB dynamic range

The HP 8145A optical time-domain reflectometer has a 28-dB dynamic range (for 1300-nm, single-mode, fiber-optic cable). You can power the instrument from ac and dc sources: 90V to 260V ac or 9V to 30V dc. The unit has a plug-in, nonvolatile memory that can store 100 traces and related annotations. It can also print out a copy of the screen on the firm’s Thinkjet printer without the aid of a controller. You can lock out various portions of the instrument’s user interface to suit laboratory or field-service applications. You can install 1300- and 1550-nm laser modules. $24,000 to $35,000. Delivery, eight weeks ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office. Circle No 381

LEAD STRAIGHTENER

- Handles pin-grid arrays with 10x10 to 20x20 pins
- Doesn’t scratch pins

The Model 1020 pin-grid array lead straightener aligns the pins of 10x10 to 20x20-pin PGAs using different fixtures. The unit accommodates pins bent as much as 30° from the vertical axis; it straightens each pin to within ±0.005 in. of its axis. To make allowances for variations in pin-to-body registration, the straightener locates PGAs by the pins rather than by the body. The manufacturer claims that the straightener will not scratch the gold finish of the PGAs’ pins. $5000.

Integrated Concepts, Box 23613, San Diego, CA 92123. Phone (619) 224-9584. Circle No 382

Four Compact Ways to Record Test, Measurement and Process Control Applications.

From our 5 oz DPU-10 to the DPU-20, the DPU-21, or high-resolution DPU-43, Seiko Instruments’ thermal printer family packs plenty of capability, with crisp ASCII alphanumerics, super-quiet operation, speeds to 1.5 lines/sec and flexible panel mounting. Applications span process control to security to data logging to medical systems—and much more.

The capability grows with the family: expand columns to 40; print width to 3.5 inches; use 7 international character sets, condensed or enlarged lines, 3 bold face formats and graphics.

With their 8-bit parallel* interfacing, small footprint and light weight, Seiko thermal printers easily integrate to host systems. Data buffers, character generators and print timing controllers help assure reliable results and trouble-free operation.

Specifications

<table>
<thead>
<tr>
<th>Model</th>
<th>DPU-10</th>
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<td>3 max</td>
<td>3.8 max</td>
<td>3.5 max</td>
</tr>
</tbody>
</table>

Give your applications the quality output they deserve—with a Seiko thermal printer. Call now for full details: (213) 530-8777. Seiko Instruments USA, 2990 W. Lomita Blvd., Torrance, CA 90505. TWX: 910-347-7307 • FAX: (213) 539-8621

*The DPU-43 also supports RS-232C interfacing.

SEIKO Instruments USA
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The survival of today's combat helicopter depends on keeping a low profile. Abbott's BC100 triple output, switching DC-DC converter helps the Lynx helicopter achieve this low profile.

The BC100's low 1.875" profile allowed 100 watts to fit into a tight space requirement. At the same time, the Lynx helicopter was able to take advantage of the economy and reliability that come from using a standard product, the BC100.

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For other applications that call for small yet powerful converters, Abbott offers both 100 and 200 watt models. Each available in single and triple configurations. And all with a wide array of options available.

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**Experience.** Start with the basics. Make sure your supplier has extensive board and system level problem solving experience. Nobody in VME has more than 30 years. Except Plessey Microsystems.

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CIRCLE NO 154

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MICROSYSTEMS

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EDN September 3, 1987
TEST & MEASUREMENT INSTRUMENTS

BOARD TESTERS

- Perform analog and digital in-circuit tests
- Use IBM PC as controller

The 1800 Series pc-board testers perform both analog and digital in-circuit tests. The testers come in two models: the 1800, which is prewired for as many as 640 test points (the standard version has 384), and the 1820, which is prewired for as many as 2048 test points (the standard version has 512). The testers have a dual vacuum system, power conditioning, and programmable power supplies. They require an IBM PC/XT or PC/AT for control. The system software uses a spreadsheet-like test-program entry instead of a proprietary test language. The analog section offers 6-wire measurements and test stimuli to 15.9 kHz. The digital section can impress 2 million vectors/sec. Model 1800 (with 384 points), $49,750; Model 1820 (with 512 points), $69,750.

Zehntel Inc, 2625 Shadelands Dr, Walnut Creek, CA 94598. Phone (415) 932-6900. TWX 910-385-6300.

Circle No 383

EEPROM PROGRAMMER

- Programmer works with IBM PC
- Unit costs $345

The Writer-RX is a single-socket (28-pin) EEPROM programmer that you can control with a dumb terminal or an IBM PC. The programmer does not require personality modules in order to accommodate different devices. It has a 32k-byte data RAM and handles 2816 EEPROMs and 2716 through 27256 EPROMs; 27512s require two programming passes. The unit comes with IBM PC software. $345.

Bytek Corp, 1021 S Rogers Circle, Boca Raton, FL 33431. Phone (800) 523-1565; in FL, (305) 994-3520.

Circle No 384

ISDN TESTER

- Simulates ISDN terminal or network-termination equipment
- Monitors all S0 interface traffic

The TE-921 ISDN simulator/analyzer allows you to develop ISDN terminals and terminal adapters without having to gain access to an active S0 interface. It implements

EDN September 3, 1987
CCITT I.430 recommendations for layers 1 and 2, and you can simulate some layer-3 functions for network terminations. When you use the instrument in conjunction with a suitable protocol analyzer, you can test network terminations by simulating an ISDN terminal, or you can test ISDN terminals by simulating a network termination. The instrument also monitors S0 traffic and displays B1-, B2-, and D-channel data on its built-in LCD or on an RS-232C-connected terminal. You can operate the D-channel in the level-2 transparent mode or in the level-3 network-simulation mode. The level-3 mode implements the correct procedures for establishing a call to the terminal. You can switch both the B1 and the B2 channels to RS-232C or TTL-level interfaces to obtain transparent 64k-bps data transmission. Alternatively, you can switch one B-channel via a built-in codec to a handset, while the other B-channel carries transparent data transmissions. The analyzer comes in a second version in which the general functions of level 2 are handled automatically and the level 3 functions allow the activation or deactivation of a connected ISDN terminal. Around DM 23,000.

**More than a digital oscilloscope**

**Modular 6 channel – Transient-Recorder – Krenz TRC Series 6000**

Extensible up to 48 channels  
0.1% accuracy  
Sample-Rate  
up to 50 MHz  
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See us at MIDCON '87, booth #963
BUS EXPANDER

- Increases IEEE-488 bus length
- Provides RS-232C control of IEEE-488 buses

The Delta IEEE-488 bus expander allows you to increase the number of instruments in an IEEE-488-bus system from a maximum of 14 to a maximum of 27. It also allows you to control two localized IEEE-488 buses via an RS-232C serial port.

LOGIC ANALYZER

- Analyzer possesses eighty 100-MHz channels
- Has built-in floppy-disk drive

The K450B logic analyzer has 80 channels and can acquire data at 100 MHz (with 10-nsec resolution). Multiplexing the channels lets you capture 40 channels at 200 MHz. The analyzer has an Auto-Setup button that automatically measures logi-threshold levels, adjusts the sample clock, and configures the display. The analyzer displays data in state, timing, µP-disassembly, or graphic formats. The analyzer can automatically arm itself after comparing captured data with reference data. It can also automatically store captured data on its built-in floppy-disk drive. Microprocessor-specific pods and disassemblers are available for common 8-, 16-, and 32-bit µPs. The analyzer has six edge-sensitive and six level-sensitive external-clock inputs. It has RS-232C and IEEE-488 ports. The 16- to 80-channel versions cost $13,795 to $27,995.

Gould Inc., Design & Test Systems Div, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 538-9320; in CA, (408) 988-6800. Circle No 389
PLD DESIGN TOOL

- Provides multiple entry modes
- Has automatic logic reduction and factoring

FutureDesigner is a menu-driven program that integrates schematic capture, behavioral logic specification, interactive design verification, and logic synthesis. During entry, you can describe each part of your circuit in the terms best suited to it; that is, you can describe it by means of hierarchical schematics, state diagrams, logic equations, or truth tables. During interactive verification, the program detects and helps you correct connectivity errors and other common design errors. It performs automatic logic synthesis, which optimizes the performance of the design by means of logic reduction and factoring that eliminates redundant circuitry. You can simulate your design's performance with the help of the vendor's Dash-
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Single, dual and triple output power supplies with pins for PC board mounting or with screw terminals for chassis mounting. Input voltage: 105-125 Vac, 47 to 420 Hz. Single outputs from 1 to 75 Vdc, to 2.5 Amps. Duals from 1 to 28 Vdc, including ±12 Vdc and ±15 Vdc models to 0.5A. Optional 230-volt input. All models UL recognized.

Also available are DC-to-DC converters for inputs of 5, 12, 15, 24, 28 and 48 Vdc. Single output models provide from 5 to 28 Vdc at up to 1.25A; duals have tracking ±10, ±12, ±15 and ±18 Vdc outputs at up to 300 ma/output. Line regulation, ±0.02%; load regulation, ±0.05%. Short circuit protection. High input/output isolation. Electrostatic shielding on all six sides. Typically 65% efficient.

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CADDOCK's Precision and Ultra-Precision Resistor Networks provide a designer's choice of performance that will optimize solutions in precision analog circuit designs.

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Standard Type T912 and T914 Precision and Ultra-Precision Resistor Networks.

Standard models of the Type T912/T914 Precision and Ultra-Precision Resistor Networks combine all of these performance characteristics:

- Absolute Tolerance: 0.1% for all resistors.
- Ratio Tolerances: 0.01% and 0.005%.
- Ratio Temperature Coefficients: from 10 PPM/°C to 2 PPM/°C.
- Absolute Temperature Coefficient: 25 PPM/°C from 0 °C to +70 °C.
- Shelf Life Stability of Ratio for Six Months: within 0.005%.

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For Type T912/T914 data, circle Number 201.

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- Includes OS/2 kernel, macroassembler, and C compiler
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The OS/2 Software Development Kit allows you to start developing applications software to run under OS/2 on 80286- and 80386-based machines. The tool kit consists of a prerelease version of the OS/2 system kernel and technical specifications for the kernel and for the OS/2 LAN manager. It also includes new versions of the vendor's macroassembler (MASM) and C compiler, the CodeView debugger, and other software-development tools, including a programmer's text editor. The price of the development tool kit includes one year of technical support via the vendor's DIAL (Direct Information Access Line) electronic mail service, and also subscribes you to the Microsoft Systems Journal. Updates will include the OS/2 Windows specification and software, as well as the LAN Manager software and associated utilities. $3000.

Microsoft Corp, Box 97017, Redmond, WA 98073. Phone (206) 882-8080. TLX 328945.

Circle No 393

IMAGE COMPRESSION

- Compresses/decompresses Fax images
- Permits use of most common monitors and printers

TMSFAX software lets you compress an MS-DOS raster-image file, using the CCITT Group 3 or Group 4 Fax algorithms, and then store the data as another MS-DOS file on your IBM PC. You can also decompress data received from MS-DOS file-storage devices—such as Fax machines, CD-ROMs, and WORM optical disks—and send the image to the screen or to a graphics printer. The decompression time ranges from 10 to 45 sec, depending on the image content and the processing power of the PC. Because the compression and decompression operations are completely performed by the software, they aren't fast enough to handle real-time images received from a Fax modem, but you can store such images and then decompress them off line. The vendor also offers two facsimile-function libraries. The Compression Applications Library manages all file functions for compressed images, but allows you to pass image headers and raw image data between your application program and the compressed file; the Decompression Applications Library keeps track of all display-device parameters, letting you write monitor- and printer-independent facsimile applications more easily. OEM purchasers of 100 copies of the software can obtain the libraries at no additional charge. $95 (10).

TMS Inc, Box 1358, Stillwater, OK 74076. Phone (405) 377-0880.

Circle No 394

DATA ANALYSIS

- Enhanced program provides vectors and matrices
- Built-in programming language for customized applications

Release 3.0 of the RS/1 data-analysis software package runs on a variety of VAX minicomputers under the VMS operating system. The package maintains compatibility with earlier versions of RS/1 (statistics, graphics, curve fitting, and modeling) as well as with the ven-

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- Ratio Temperature Coefficients: 50 PPM/°C, 25 PPM/°C, 10 PPM/°C and 5 PPM/°C from 0°C to +70°C.
- For Type T1794 information, circle Number 204.

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- Ratio Temperature Coefficients: 80 PPM/°C, 50 PPM/°C, 25 PPM/°C and 15 PPM/°C from 0°C to +70°C.
- For Type 1789 information, circle Number 205.

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The graphics editor comes with the package: This one is menu-driven and guides new users through the graphics-development process. Release 3.0 also has an improved directory structure, which retains the command forms of earlier versions, yet increases the limit on text size from $2^{15}$ to $2^{21}$ bytes. The package includes procedures to convert existing RS/1 data objects to the new directory structure. It also has a data-smoothing technique that helps users to identify trends that may not be apparent from an examination of the raw data. $3900 to $79,000, depending on computer configuration.

BBN Software Products Corp, 10 Fawcett St, Cambridge, MA 02238. Phone (617) 864-1780.

Circle No 395

C COMPILER

- Conforms to the proposed ANSI standard
- Comes with built-in editor and linker

Turbo C is a C editor, compiler, and linker that runs on the IBM PC and compatibles. The compiler conforms to the Kernighan/Ritchie and proposed ANSI standards and is compatible with other compilers that follow these standards. The compiler can compile code for six memory models: Tiny, Small, Compact, Medium, Large, and Huge. Its use of near and far pointers lets you take full advantage of the 8086 µP's architecture by means of a mixed-model technique. The vendor claims that Turbo C has a compilation speed of 10,000 lines per minute. The run-time library contains more than 300 functions that you can call from within your C programs. The math functions conform to the IEEE floating-point standard, and they emulate an 8087 math coprocessor if one is not present in the system. The vendor will offer complete source code for the run-time library at $235 in the third quarter of 1987. The package includes a built-in editor, linker, and Lint error checker. Within the integrated environment, you can switch from one facility to another without returning to the OS. $99.95.

Borland International, 4585 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (408) 438-8400. TLX 172373.

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<table>
<thead>
<tr>
<th>Model name</th>
<th>Number of dots</th>
<th>Duty</th>
<th>Dot pitch (mm)</th>
<th>Outline dimensions (mm)</th>
<th>Option (EL Back Light)</th>
<th>Recommended controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLX-1181*</td>
<td>640 x 400</td>
<td>1/200</td>
<td>0.35 x 0.35</td>
<td>276 x 168 x 12</td>
<td>O</td>
<td>T7779</td>
</tr>
<tr>
<td>TLX-832</td>
<td>640 x 200</td>
<td>1/200</td>
<td>0.375 x 0.375</td>
<td>293 x 97.6 x 14</td>
<td>X</td>
<td>T7779</td>
</tr>
<tr>
<td>TLX-561</td>
<td>640 x 200</td>
<td>1/200</td>
<td>0.35 x 0.49</td>
<td>275 x 126 x 14</td>
<td>O</td>
<td>T7779</td>
</tr>
<tr>
<td>TLX-711A*</td>
<td>240 x 64</td>
<td>1/64</td>
<td>0.53 x 0.53</td>
<td>180 x 68 x 12</td>
<td>O</td>
<td>(T6963C)**</td>
</tr>
<tr>
<td>TLX-341AK*</td>
<td>128 x 128</td>
<td>1/64</td>
<td>0.45 x 0.45</td>
<td>93.2 x 86.6 x 12</td>
<td>X</td>
<td>T6963C</td>
</tr>
</tbody>
</table>

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Computer Products Inc, 2900 Gateway Dr, Pompano Beach, FL 33069.

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Computer Industry Almanac Inc, 8111 LBJ Freeway, Dallas, TX 75251.

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EDN September 3, 1987
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**Pro-Log Corp**, 2560 Garden Rd, Monterey, CA 93940.

Circle No 404

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**App note on fiber-optic LANs**

The 4-pg application note, *Testing Fiber Optic LANs*, covers the testing requirements of most of these devices, including Ethernet and token-ring LANs. The topics examined include testing fiber-optic cables, troubleshooting systems, and margin testing.

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Mentoring
A subculture success some engineering companies would like to duplicate

Deborah Asbrand, Associate Editor

Chuck Kingsford-Smith thought he was a pretty good engineer when he graduated from Louisiana State University in 1955. He had no trouble getting a job and went to work shortly after graduation for Westinghouse in Metuchen, NJ. But not long after he began working with other, more experienced engineers, Kingsford-Smith’s confidence dissolved. Fellow engineers, he discovered “could think circles around me. Compared with them, I wasn’t very good at all.” The engineers on Kingsford-Smith’s team, however, were sympathetic. “They wanted me to learn,” he says, “and they were willing to put up with my amateurishness.”

Mike Perkins’s first few months in engineering proved equally unnerving. Engineers at the company he joined had private offices, which made it that much more difficult for him to approach them with his frequent questions. “It’s intimidating to have to walk into another person’s office and ask them questions like ‘Is it okay to read technical magazines on the job?’” says Perkins, now a project manager for Hewlett-Packard’s Roseville, CA, Networks Division. “In the first several months, I wasn’t sure what I was supposed to be doing.”

An engineer’s foray into industry may be colored by understandable trepidation: Not only do recent college graduates need assistance in finding their way around the corporate sphere, they need to fine-tune their engineering skills, which in most cases have not yet been put to practical use. “Schools teach basic theories, but in electrical engineering, there are so many jobs that there’s no way you can be prepared for all of them,” says Perkins. “After 13 years in industry, there are still lots of jobs I’m not prepared for.”

Much postcollege training is performed by industry, and, more specifically, by other engineers. An important part of the indoctrination process for many engineers has been the cultivation of a mentor, an ally who can alleviate some of the stress by lending technical expertise, company know-how, or both. Mentoring is a time-honored if inexact process based on the often elusive chemistry that develops between individuals. It’s always existed as a kind of subcultural phe-
nomenon in engineering, but now companies are trying to bring mentoring into the corporate mainstream by encouraging its proliferation and, in some instances, by matching mentors and "mentees."

Many engineers recall having had a mentor in their early years, and even those who didn't find one particular person to work with usually managed to find a senior team or project member who was unperturbed by their frequent queries. "Whether or not you had a mentor, you always found someone to answer your questions," says Don Tellian, a lab engineer at Hewlett-Packard's Roseville Networks Division.

Solving crises of confidence

Indeed, questions—and self-doubt—plague many young engineers. Assuaging those crises of confidence is an important part of mentoring. "I had some pretty grave doubts that I'd picked the [right] profession," says John Lang, whose first job was as a junior engineer with Sylvania in Williamsport, PA, in 1952. "When I was in school, I got grades to gauge how I was doing, but in business, you don't have that. . . . I was miserable and not sure whether what I was going through was normal."

Lang found his engineering experience enriched when he began working with a senior engineer several months after joining Sylvania. "He was enormously helpful," Lang remembers. "I could go in and ask him silly stuff. I could show him a circuit I was working on and ask him what he thought of it. The presence of a mentor clarified a lot of issues for me."

Having survived his own bout with anxiety, Kingsford-Smith, a designer for Hewlett-Packard's Lake Stevens Instrument Division in Everett, WA, now tries to minimize the first-job jitters of young engineers. "People tend to panic when the problem isn't yielding to their best attack," he says. In such moments of frustration, it's easy for young engineers to forget the problem-solving methodologies they were taught and to give in to the confusion. "There are ways to stand back and look at the problem and choose a strategy that restores calm and confidence to the new engineer," Kingsford-Smith says. "It tells him that he is going to be able to solve this problem after all."

Manfred Bartz needed just this kind of reassurance when he joined Hewlett-Packard as a 23-year-old neophyte in 1980. Told to design an output amplifier, Bartz quickly encountered difficulty with some of the amplifier's feedback mechanisms. Kingsford-Smith lent his experience to help Bartz. "I was taking it on single-handedly and ran into a snag," Bartz recalls. "Chuck was generally known as a local guru; it was a natural thing to have him come on board."

Mentoring extends beyond the pairing of a senior engineer and a newcomer. Some engineers remember having not one mentor, but several. And the process transcends the boundaries of age. One engineer says he's been a mentor to a man 10 to 15 years older.

Because it's based on chemistry—on two people with a special rapport or shared technical interests who swap questions and ideas—mentoring is likely to be haphazard. "When it's informal, you're never quite sure what questions you can ask," says Perkins. In addition, not everyone can juggle their schedule to accommodate casual, albeit work-related, discussions. And when finding a mentor is left to chance, not everyone who needs a mentor may get one.

To fill these gaps and to make better use of mentoring's cost-effective training methods, some companies are lending a hand to the mentoring process by matching newly hired or transferred engineers with seasoned project members who can answer their questions.

Hewlett-Packard implemented a mentoring program at its Roseville Division after a 1985 survey revealed R&D engineers there found new engineers' training inadequate. In post-survey analysis groups, the engineers related in detail the quandary that faces new project members. "The project manager dumps a huge stack of reading material on your desk and tells you that you need to get up to speed," says Hewlett-Packard training-specialist Sue Sower. "At the same time, you need to begin contributing to the project team."

The program has teamed 10 experienced engineers with new or transferred project members and also with summer students. Both Hewlett-Packard administrators and engineers who participated in the program are happy with the results but admit that it's not an unqualified success.

Organizing mentor relationships

Organizing the mentoring process has definite advantages, participants say. "If it's formal, the person who is the mentor has allocated time to it," says Tellian, who worked with the engineer who replaced him when Tellian moved to a new position. "When it's informal, you just hope you catch someone at a good time and that they're in a good mood that day."

Mike Perkins says he has always coached younger engineers. But participation in Hewlett-Packard's structured program means his su-
pervisor knows and approves of the additional demands on Perkins's time. As a result, his technical assignments are lightened enough to give him the time he needs—usually two to three hours per week—to devote to mentoring. "The formalizing gives it better structure and recognition," says Perkins.

**Formalized programs' drawbacks**

Formalizing what is essentially an informal process, though, can lead to special difficulties. For one thing, support for the program may be spotty, because not all engineers agree that mentoring should occur, let alone be encouraged. "A few people spoke out against the program," says Sower. "They said it didn't work, that it didn't allow engineers to use their initiative, and that we'd be babying them."

Analog Devices' Lang has heard the same criticisms from engineers at his company, where mentoring is encouraged but not organized. "Some are even antagonistic about it," says Lang, who three years ago left engineering to become manager of technical training for Analog Devices. "They think 'I learned the hard way, and [the young engineers] are going to learn the hard way, too.'"

Even those individuals who are interested in mentoring don't necessarily make good mentors. "A mentor really needs to have some teaching skills and be able to communicate effectively," says Sower.

The crucial element missing from formal programs is the personal chemistry that makes spontaneous partnerships click. "You can't put people together and assure they're going to be friends," says William Sackett, associate dean for engineering and science at the University of Minnesota and retired vice president of research for Honeywell. "There's a chemistry involved. The payoff has to be that both the mentor and mentee enjoy spending time together."

Successful mentoring is more subtle and complex than it may seem at first glance. Sackett speaks from experience of the difficulties involved in establishing mentoring partnerships. Several years ago, he watched a mentoring program for women managers at Honeywell quickly grind to a halt. Although that program failed, Sackett remained interested in the mentoring process. He tried—with no more success—to be a mentor to some of the managers working for him. "Some of them came to me and said 'leave me alone,'" he remembers.

Sackett had discovered a cardinal rule of mentoring: Unless it's carried out correctly and unless participants develop a liking for each other, the relationship lacks the mutual interest that makes it desirable to begin with.

"I liken the mentoring relationship to a marriage," says Boston University professor Kathy Kram. "It's based on chemistry between two people and a certain amount of fantasy about the relationship. Arranged marriages don't work, and arranged mentorships don't work either." Honeywell eventually abandoned its formal programs in favor of seminars on the mentoring process designed to nurture mentoring relationships.

Whatever form it takes, mentoring's biggest payoff may be the soothing effect it has on a newcomer during his or her first few months on the job. Perkins considers this a practical benefit, not a perquisite. "I'm an advocate of reducing anxiety," he says. "Why have more than you need?"

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This Manager will be responsible for the design, development and transfer to Manufacturing of new CMOS products. Technical duties will include Development Scheduling, Design Supervision and Cost Definition of new products. Managerial responsibilities may involve department budgeting, recruitment of technical staff and cost studies of future advanced design approaches.
Eight years experience in the industry with a minimum of at least four years in a supervisory role. CMOS circuit design and/or logic design experience preferred. System hardware experience helpful.
BSEE or equivalent required. MS and/or MBA desired.

CMOS DESIGN ENGINEER
Responsible for all aspects of design, development and transfer to manufacturing of CMOS VLSI products. This may include logic design, circuit design, characterization, failure analysis and the supervision for layout and test.
This position requires a minimum of two years design experience in CMOS digital logic and/or circuit design.
MSEE / BSEE or equivalent required.

BIPOLAR DESIGN ENGINEER
Design and coordinate all technical activities associated with obtaining design approval on bipolar digital logic circuits such as PLA, and 100K ECL.
Three to five years of design experience on bipolar digital circuit and logic design required. Successful candidate will have designed TTL, 100K ECL, or PLAs.
MSEE / BSEE or equivalent required.

CAE ENGINEER, DEVELOPMENT ENGINEERING DIVISION
Considerable systems level experience with the VAX VMS operating system, including software installation, performance monitoring, systems tuning, and resolution of day to day challenges in an operations department.
Experience with any of the following would be helpful: VAX clusters, networks, interfacing or peripherals, modern programming language, spread sheets, statistical packages, 4GL and databases.
BSEE, BSCS or equivalent required.

SYSTEMS ANALYST, DEVELOPMENT ENGINEERING DIVISION
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- **SR. PRODUCT ENGINEER**
  BSEE/MSSEE with 4 years plus experience in analog product engineering.

- **SR. ANALOG DESIGN ENGINEER**
  BSEE/MSSEE with 4 years plus experience in designing complex analog ICs in either Bipolar/Bipolar enhanced MOS. Mentor/VAX necessary, familiar with SPICE.

- **SR. PRODUCT ENGINEER**
  BSEE with 4 plus years related IC manufacturing experience.

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LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

Machine-vision market held back by myopia

The market for machine-vision systems and components should expand from $285 million in 1986 to $2.7 billion by 1991, according to Electronic Trend Publications (ETP) of Saratoga, CA. This leap represents a healthy compound annual growth rate of 56.5%. Still, the market-research firm maintains that these figures could be substantially higher were it not for a pervasive lack of vision, a “spreadsheet myopia,” at the management level of manufacturing companies.

The primary advantage of this equipment is improved quality. ETP found that automated inspection of incoming parts was 97% effective in eliminating failures; under the best conditions, human inspection is 78% effective.

According to ETP, uncertainty on the part of users blurs their vision and consequently curbs the industry’s growth. This confusion stems in part from the industry’s youth and from the inadequate financial models used to analyze cost vs. payback. ETP performed case studies in various market sectors, including the automotive, biomedical, commercial aerospace, defense, electronics, food and beverage, light industrial, and robotics manufacturers. By 1991, the electronics sector is expected to consume 39% of the total market, surpassing the $1 billion mark. The automotive sector will claim 28% of the market, amounting to $751 million in sales.

Marked distinctions appear when the US market is divided according to function. The largest growth market by far involves robotics. Although the market for robotic guidance and adaptive control systems should only reach $188 million by 1991, a relatively low figure for the industry, it will enjoy a 128.8% growth rate during the period from 1986 until 1991. The market for the entire function area of guidance, control, and robotics will leap from $86 million in 1987 to $564 million in 1991. Applications involving quality assurance, test, and inspection will account for $1.69 billion in 1991, up from $185 million in 1986. This growth represents a 55.6% rate of change for those applications that entail gauging, inspection, verification, and flaw detection.

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<tr>
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<tbody>
<tr>
<td>QUALITY ASSURANCE, TEST, AND INSPECTION</td>
<td>$185</td>
<td>291</td>
<td>461</td>
<td>746</td>
<td>1191</td>
<td>1690</td>
<td>55.6%</td>
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<tr>
<td>GAUGING</td>
<td>77</td>
<td>118</td>
<td>180</td>
<td>280</td>
<td>435</td>
<td>617</td>
<td>51.6%</td>
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<tr>
<td>INSPECTION</td>
<td>57</td>
<td>91</td>
<td>151</td>
<td>256</td>
<td>416</td>
<td>590</td>
<td>59.6%</td>
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<tr>
<td>VERIFICATION</td>
<td>28</td>
<td>41</td>
<td>58</td>
<td>82</td>
<td>113</td>
<td>161</td>
<td>41.9%</td>
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<tr>
<td>FLAW DETECTION</td>
<td>23</td>
<td>41</td>
<td>72</td>
<td>128</td>
<td>227</td>
<td>322</td>
<td>69.5%</td>
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<tr>
<td>PARTS IDENTIFICATION</td>
<td>$35</td>
<td>50</td>
<td>72</td>
<td>116</td>
<td>170</td>
<td>242</td>
<td>47.2%</td>
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<td>CHARACTER RECOGNITION</td>
<td>15</td>
<td>23</td>
<td>36</td>
<td>56</td>
<td>76</td>
<td>108</td>
<td>48.4%</td>
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<tr>
<td>IDENTIFICATION</td>
<td>20</td>
<td>27</td>
<td>36</td>
<td>56</td>
<td>94</td>
<td>134</td>
<td>46.3%</td>
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<tr>
<td>GUIDANCE, CONTROL, AND ROBOTICS</td>
<td>$51</td>
<td>$86</td>
<td>$144</td>
<td>$233</td>
<td>$397</td>
<td>$564</td>
<td>61.7%</td>
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<td>INVENTORY MONITORING</td>
<td>11</td>
<td>18</td>
<td>29</td>
<td>35</td>
<td>57</td>
<td>54</td>
<td>37.5%</td>
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<tr>
<td>SEAM TRACKING</td>
<td>20</td>
<td>36</td>
<td>50</td>
<td>82</td>
<td>132</td>
<td>188</td>
<td>56.5%</td>
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<tr>
<td>PROCESS CONTROL</td>
<td>17</td>
<td>23</td>
<td>36</td>
<td>58</td>
<td>95</td>
<td>134</td>
<td>51.1%</td>
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<tr>
<td>ROBOT GUIDANCE AND ADAPTIVE CONTROL</td>
<td>3</td>
<td>9</td>
<td>29</td>
<td>58</td>
<td>113</td>
<td>188</td>
<td>128.8%</td>
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<tr>
<td>MATERIALS HANDLING</td>
<td>$14</td>
<td>28</td>
<td>43</td>
<td>70</td>
<td>132</td>
<td>188</td>
<td>68.1%</td>
</tr>
<tr>
<td>SORTING, BIN PICKING, PACKAGING, PALLETIZING</td>
<td>14</td>
<td>28</td>
<td>43</td>
<td>70</td>
<td>132</td>
<td>188</td>
<td>68.1%</td>
</tr>
<tr>
<td>TOTAL SYSTEMS</td>
<td>$285</td>
<td>$455</td>
<td>$720</td>
<td>$1165</td>
<td>$1890</td>
<td>$2684</td>
<td>56.5%</td>
</tr>
</tbody>
</table>

* CAGR = COMPOUND ANNUAL GROWTH RATE

(SOURCE: ELECTRONIC TREND PUBLICATIONS)
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| MODEL     | FREQ. RANGE (MHz) | GAIN MAX. | NF dB | OUT/PWR dBA | DC PWR mA | PRICE $ (
<table>
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<tbody>
<tr>
<td>MAN-1</td>
<td>0.5-500</td>
<td>28</td>
<td>1.0</td>
<td>8</td>
<td>4.5</td>
<td>60</td>
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<tr>
<td>MAN-2</td>
<td>0.5-1000</td>
<td>19</td>
<td>1.5</td>
<td>7</td>
<td>6.0</td>
<td>85</td>
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<tr>
<td>MAN-1LN</td>
<td>0.5-500</td>
<td>28</td>
<td>1.0</td>
<td>8</td>
<td>2.8</td>
<td>60</td>
</tr>
</tbody>
</table>

††Midband 10f, to ±0.5dB ††dB Gain Compression
Max input power (no damage) +15dBm. VSWR in/out 1.8:1 max.

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