- VME BUS CHALLENGES MULTIBUS I AND MULTIBUS II
- TEST DRIVING A SILICON COMPILER
- PRINTED CIRCUIT BOARD DESIGN
- MICROSTORAGE • GRAPHICS ARCHITECTURE
Whether you need a turn-key system or a peripheral to connect to your computer, the TRAPIX™ 5500 Image Processors have been carefully designed to meet your specific needs. They're compact and rugged enough to withstand most hostile environments, yet they carry a commercial price tag and are backed by a full year factory warranty — the best in the industry. They don't require special power or air conditioning and they use standard programming languages and operating systems — features designed to make them easy to own and use.

It's both flexible and expandable. Even the smallest TRAPIX™ 5500 is a full-function, image processor that can grow to meet your future requirements. Its modular design and Q-bus/Unibus architecture let you develop cost-effective solutions for any image processing application. To tailor your own solution, simply select any subset of the following capabilities:

**Image Acquisition**
- Monochrome, binocular, color or multispectral input.
- Camera, CCD, infrared or video tape
- Line scan or array to 2048 x 2048
- Analog or digital to 12.5 MHz
- 8-, 10-, or 12-bit digitization

**Image Storage/Retrieval**
- Up to 16 Mbytes of dual ported image memory
- From one to 32 bits per pixel
- Images to 4096 x 4096 pixels
- Real-time disk storage up to 6800 images

**Image Processing/Analysis**
- Real-time logical, arithmetic processing
- Convolution, warping, and FFT
- Morphological, machine vision processing
- Continuous interpolated magnification/minification
- High-speed vector generation
- User-programmable 32-bit signal processor (TMS-320)
- Real-time histogram generator

**Computing/Networking**
- Standalone with internal LSI-11 or MicroVAX
- Bus-connected to any Q-Bus or Unibus computer
- Easily interfaced to non-DEC computers
- Ethernet, DECNets, IEEE 488

**Software**
- Proven library of ready-to-use image processing and analysis functions
- Turn-key and custom software availability
- Support for Fortran, C, Pascal and assembly language
- RT-11, TSX-Plus, RSX-11M, VAX/VMS, UNIX

As you can see, the TRAPIX™ 5500 offers a clear solution to your image processing requirements. For more information or applications assistance, call or write RCI.


RECOGNITION CONCEPTS, INC.
924 Incline Way, P. O. Box 8510, Incline Village, Nevada 89450 (702) 831-0473 Telex: 753168

INNOVATORS IN IMAGE PROCESSING®
Now your computer can have 20/20 vision.

Datacube continues to be the single source leader in image processing and graphics for your Multibus, Q-Bus, and now IBM PC's. Solutions are available from single boards to fully integrated systems. Resolutions range from 320H x 240V to 1400H x 1100V with pixel depths from 1 to 24 bits.

The new SP-123 offers advanced signal processing of high resolution black & white or full color images at the rate of 14 megapixels per second.

The new IVG-128 is a complete video acquisition and display module on a single IBM PC compatible card. It features input & output look up tables, an 8-bit digitizer, and RGB 8-bit outputs.

The new DC-1000 and DC-1500 systems are complete workstations capable of video acquisition and image processing.

Datacube products provide reliable vision and real time image processing for robotics, medical imaging, surveillance, inspection, teleconferencing, animation, etc. And at surprisingly low prices.

Call or write for our new Product Guide of Multibus, Q-Bus, and IBM PC compatible boards and systems. Datacube Incorporated, 4 Dearborn Road, Peabody, MA 01960, Telephone: (617) 535-6644.

Western Sales Office: Telephone: (408) 737-9978.

Datacube

Circle 4 on Reader Inquiry Card
Single board solutions for 16/32 bit "open systems" in industrial, business, and scientific environments

If your application requires advanced technology available in production quantities if quality, reliability, and price/performance ratio are the major criteria for supplier selection — then compare our product portfolio with other alternatives.

- Three CPU's for most applications from intelligent I/O controllers to multiuser/multitasking environments with powerful UNIX* or real time operating software PDOS* and up to 1M byte of on-board memory: CPU-1B, CPU-2, CPU-3.
- Two DRAM Boards: 512KB and 2MB; two SRAM Boards: 128KB and 512KB. RAM/ROM Board: 512KB (max.); DRAM-1, DRAM-2, SRAM-1/2, RR-1/S/E
- Mass memory interface boards with either direct control of up to seven drives (WFC-1) or intelligent VMEbus interface to SASIbus with DMAC (SASI-1).
- Six-channel serial I/O board with Multi-Protocol-Communications-Controller (SIO-1).
- 32-channel parallel I/O boards either optically isolated (1000V) with DMAC (PIO-1) or TTL-level with 64 mA drive capability signals (PIO-1).
- Intelligent high resolution graphics subsystem (master/slave) with resolution of 1024 x 1024 pixels and up to 12 bits of pixel depth. Powerful graphics operation through local 68000 MPU in parallel with 7220 graphics controller(s) GDC-1M/1S.
- Winchester/Floppy drive modules with up to 80 M bytes: WFMOD-20/80.
- Auxiliaries: Backplanes, chassis, power supplies.
- A variety of Software Products, e.g.:
  - PDOS* — Real-Time, Multi-Tasking, with Basic interpreter, Pascal, Fortran 77, and C Compilers.
  - COHERENT* — UNIX* V.7 compatible with C Compiler, Pascal and Fortran 77 in preparation.
  - UNIX* — System V, Multi-User, Multi-Tasking.
- In development: memory boards with byte parity and 32 bit addressing; dedicated LAN-Controller; high performance communication I/O.

Supported by a worldwide network of distributors and representatives, FORCE Computers is recognized by its customers (and competitors) as the leading supplier of 68000/VMEbus board products.

*PDOS is a trademark of Eyring Research, COHERENT is a trademark of Mark Williams Co., UNIX is a trademark of AT&T.

Consider, compare, and contact: FORCE COMPUTERS, INC.
TECHNOLOGY TRENDS

14 CAD / Designing ICs With A Silicon Compiler • Gate Array Design Update — Design Verifier Flags Potential Problems

22 Software / PC-Based Software Produces High Resolution Graphics Files

24 ICs / 64K X 1 SRAMs Vie For DRAM Applications

26 Communications / Options Multiply For High Speed Unibus Communication • Fiber Optic Transmission Schemes Expand Standard Local Area Network Possibilities

10 Editor’s Comment

12 Hotline

80 Product Index

81 Reader Service

94 New Product Focus

100 New Products

123 New Literature

124 Calendar

124 Advertiser Index

ON THE COVER

Currently the only widely supported 32-bit bus structure, the VME bus, is being considered by many systems integrators as a logical 32-bit upgrade solution to their existing Multibus designs. The front cover this month depicts three new products from Motorola Microsystems including a 68020-based CPU board. Photo courtesy Motorola Microsystems, Inc.

FEATURES

34  Systems Architect's Guide To The VME Bus
    by Dave Wilson
    At the present time, only a few buses can support 32-bit processors — VME, Multibus II, NU Bus and Futurebus. Of these, only one CPU board is available on the Multibus II, none on NU Bus or Futurebus while VME sports over 30.

43  Little Drives That Can
    by Bob Hirshon
    Mass memory devices fitting the 3½” form factor have emerged to fill the demands of designers who need to get the most out of every cubic centimeter.

53  Graphics Architecture — New ICs Promise Better Performance
    by Gregory MacNicol
    Driven by user demands for faster, smaller, more capable and less expensive computer graphic systems, semiconductor manufacturers are introducing chips that provide rapid bit-mapped medium to high resolution displays.

63  Peripheral I/O Processor Speeds VAX Performance
    by H.D. Meitzen and Delbert L. Taylor
    The optimum computer system for work such as seismic processing, signal processing in data communications, and real-time graphics combines a multi-user interactive environment for controlling data processing with an I/O subsystem that permits peripheral devices to exchange data at very high speeds with minimal attention from the host.

69  Printed Circuit Board Design Demands Versatile Integrated Tools
    by Julie Pingry
    Board design programs need flexibility and interactive features to accommodate mixing TTL with ECL, CMOS and discrete analog devices on increasingly dense and large boards.

79  DMA Controller Relieves Host Of I/O Management
    by Scott Searcy
    I/O subsystems for high-performance computers must not only process and transfer large amounts of data, but also interface to a large number of peripheral devices.
LET RETICON PUT THE VISION INTO YOUR NEXT DESIGN.

Because we offer the broadest range of image sensors available—from linear to area and circular arrays—it's easier for you to find the right one for your application. And in case you can't, we're prepared to put our experience and expertise to work for you in developing a cost-effective custom configuration that meets your needs. Thousands of EG & G RETICON solid state image sensors are already in use in applications such as page and character scanning, spectroscopy, robotics, and non-contact inspection instruments.

Contact us today for complete information. At RETICON, the solution to your imaging application is within sight. EG & G RETICON 345 Potrero Ave. Sunnyvale, CA 94086-4197 (408) 738-4266 Chicago (312) 640-7713; Boston (617) 745-7400; Japan 03-343-4411; England (0734) 788666; Germany (089) 92692-666.

Circle 6 on Reader Inquiry Card
32 BIT TECHNOLOGY FROM A 2 BIT START-UP?

ABSOLUTELY!

We're Goodspeed Systems. And although we're new on the scene, we've been doing big things. We took an exciting new chip set — National's 32000 Series — and created a 32-bit single board computer. The GS-32 delivers true 32/32 performance — plus some big advantages no one else can match:

**The Time Advantage:** We can shorten your time to market with our tested, proven boards. The GS-32 is available now; there's no wait for the 32-bit power you need today.

**The Design Advantage:** Our flexible, fully socketed design offers 32-bit processing, up to 2 MB memory, I/O and mass storage interfacing, *all on a single board*. It's ready to plug in or expand to your specs. Software options scaled to your application level, too. Now you can have 32-bit performance without a workstation or even card cage.

**The Price Advantage:** The GS-32 delivers full 32-bit performance at a fraction of the cost of bussed systems. Our price-to-power ratio is unmatched. And that means it can slash your overall system costs for that competitive edge.

The GS-32 from Goodspeed Systems. The little company with the big board. If you're ready for 32-bit technology, call for the name of your representative:

**1-800-243-8160**

**GOODSPEED SYSTEMS**

23 Main Street, P.O. Box 29, East Haddam, CT 06423

Circle 8 on Reader Inquiry Card
EVERYONE IS TALKING ABOUT OPTICAL DISK TECHNOLOGY. ALCATEL THOMSON GIGADISC DELIVERS IT!

Gigadisc, the new laser memory system developed for low-cost storage of large quantities of data is proving itself in field applications worldwide.

If you require a high-capacity random access memory which includes non-erasable removable media with excellent archival properties, Gigadisc is the right product for you. To maintain the lead in today's competitive market, you need the Gigadisc to deliver an attractive system offering low-cost on-line and off-line storage.

Features like one gigabyte-per-side capacity, random data retrieval, SCSI interface and a field-proven design make Gigadisc one of the most appealing laser optical memory products available today.

In the U.S.A. call (213) 543-5537
In France call (1) 630.24.72

Alcatel Thomson Gigadisc
210 Avenue J, Suite D
Redondo Beach, CA 90277

Circle 7 on Reader Inquiry Card

REPRINTS

DIGITAL DESIGN will reprint any article from past or present issues. Reprints are custom printed. Minimum order: 1,000 copies. Purchase order or letter of authorization required.

Allow one month from receipt of order for delivery, unless previously arranged and confirmed.

Advertisements alone can also be reprinted. Call (617) 232-5470, and ask for reprints.
Sell someone a Genicom 3000, and it may be some time before you hear from them again.

From offices to factories across the country—hour after hour, day after day—Genicom 3000 printers have been proving their quality and reliability under even the toughest conditions for years. The result has been a large number of very satisfied customers, which means a large number of satisfied OEM's. But durability is only part of the Genicom 3000 printer advantage.

The Genicom 3000 family of printers offers multi-model flexibility combined with single design simplicity to give OEM's real dollar savings with price/performance matching for every customer. Parts commonality. Easier servicing. Single source supply. Plus you can select speeds from 180-500 cps draft/EDP, 45-100 cps NLQ, single or multimode printing, automatic sheet feeders, document inserters, multi-color printing and graphics, plus more. There's such a diversity of models, features and options, you can choose just the right printer and you don't have to pay for things you don't need.

See how long you can keep your customers satisfied... with the long lasting, field proven printers that have earned the respect of OEM's nationwide—the Genicom 3000 family.
EDITOR'S COMMENT

DIGITAL reDESIGN

As promised last month, this is our first issue incorporating Electronic Imaging into Digital Design. The merger effects a number of important changes in this magazine.

To accommodate additional graphics and imaging articles, along with our usual subjects, the feature section of Digital Design has been divided into four subsections: Electronic Imaging, Systems Architecture, Semiconductor Technology and Design Technology. The systems, semiconductor and design sections are what we have been doing all along; imaging is new.

Although graphics, array processsing and much of the other coverage in Electronic Imaging fall within our normal purview, articles with a purely imaging cast are new to Digital Design. To help us keep it all sorted out, Andrew Wilson, Executive Editor of Electronic Imaging, will be responsible for the expanded graphics and imaging coverage.

Systems architecture covers our traditional computer-related subjects. That includes computer systems, peripherals, buses, communications and expanded software coverage. Technical Editor Brita Meng will be in charge of the section.

Because semiconductor advances make most systems progress possible, Digital Design has always provided IC coverage. Now we are formalizing it with a feature section devoted exclusively to semiconductor technology. Our Executive Editor, David Wilson, is responsible for this section of the magazine.

In the past, Digital Design has offered a great deal of design coverage such as PC board and gate array design, workstations and development systems. Because of the importance of these topics to design engineers, a section of the magazine is now devoted to design technology. Senior Technical Editor Ron Collett is responsible for the section.

Each of the feature sections will have at least one article per issue and often more. Our goal is to provide balanced editorial every issue. To ensure that balance, the Technology Editors in charge of each of the four sections will continually track their segments of the industry, keeping up to date on the latest technology.

All of the Technology Editors have degrees in either Electrical Engineering or Semiconductor Physics. But despite their broad knowledge of the industry, they know that they cant do it all themselves. So they will be looking for help in the form of good contributed articles.

We've made a few other changes as well. Last month you saw the replacement of Departments with Technology Trends and the addition of New Product Focus reports. Now the whole news section of the magazine has been redesigned to pick up many of the visual elements of Electronic Imaging.

For example, Update has been replaced with Hotline (as in Electronic Imaging) to underline the immediacy of news in that section. Technology Trends has picked up the graphics style of Electronic Imaging's news section but otherwise remains the same as established last month. Staying on top of the news is Senior Editor Julie Pingry's responsibility, although much of the input will come from the Technology Editors.

All of these changes represent a commitment to our readers. We are trying to provide the best written, most balanced design editorial package in the industry. Let us know how you feel about it.

—John Bond, Editor in Chief
An Array Processor this fast and flexible can’t sell for only $4100.

Or can it? The imaging requirements of a geophysical research project at sea demanded intense mathematical calculations. An array processor was the answer. But space aboard the ship’s computer was limited. Only a single Multibus* slot remained. Marinco engineers, driven by necessity, pushed beyond the horizons of conventional array processor design.

A Single Board
They discovered how to shrink circuits to a single board — and to do so without sacrificing performance. In fact, they enhanced it. Keeping signals within a single board actually made significant speed gains. Then they added other performance enrichments such as memory mapping and an auxiliary port for direct high speed I/O.

Easy to Program
Perhaps as important, the board is easy to program, even for someone with only high-level language experience. Standard routines may be adapted. Or new ones created. Marinco’s assembler automatically generates the microcode and tracks the 48-bit control word.

Imaging Productivity
The speed and flexibility of the APB-3000 series can dramatically increase your imaging productivity. Use it for coordinate transformation, hidden line removal, vector-to-raster conversion, interpolation, image enhancement and many other operations.

Very Low Price
Even with all these advantages, Marinco innovations make it possible to offer the Multibus version for only $4100, quantity one, U.S. price. IBM PC and PC AT versions are also available.

Can an array processor this fast and flexible really sell for such a low price? Thanks to practical demands and Marinco innovations, it can. Call us toll-free for details.

Specifications
Program Memory 2K X 48-bits Data Memory 8K words Data Word 24 bits long, 8-bit exponent, 16-bit mantissa (floating pt.) or 16 bits (integer).

Marinco Computer Products
9940 Barnes Canyon Road
San Diego, CA 92121
800-587-0461
1-800-421-4807
in Calif, 1-800-421-4808
Telex 3719117

Circle 17 on Reader Inquiry Card

Marinco, a HELIONETICS Company

*Multibus is a trademark of Intel Corp.
32-BIT BIT-SLICE ADDED TO STANDARD CELL LIBRARY  Wafer Scale Integration is slated to announce the addition of a 15 MHz 32-bit CMOS bit-slice processor to their standard cell library at the Custom Integrated Circuit Conference in Portland, OR this month. In the third quarter, WSI plans to offer the processor as a standalone chip.

EDIF VERSION 1.0 RELEASED  The Electronic Design Interchange Format (EDIF) specification is now available to industry. EDIF can be used as a standard interface between engineering, design, test and manufacturing tools. The first meeting of the EDIF Users' Group will be June 27 during the Design Automation Conference in Las Vegas.

STRETCHED DISK FACILITY OPERATIONAL  The process development and pilot production plant for 3M's stretched disks has begun operation. Stretched disks promise higher recording capacity than floppy disks, yet use flexible media to circumvent the high cost and fragility of rigid disks. Current 5 1/4" versions hold about 12 Mbytes and may reach 100 Mbytes.

FAULT-TOLERANT SYSTEM ANNOUNCED BY IBM  The System/88 is IBM's first fault-tolerant computer; the system is supplied by Stratus Computer under an agreement for IBM to buy and resell some Stratus products. The System/88 is based on Stratus 32 processors and software.

8086/8088 FAMILIES IN CHMOS  Intel has announced that their 8086/8088 microcomputers and peripherals will be produced in CHMOS. 80C86 and 80C88 parts will be fully compatible with the existing NMOS versions. Samples of the CHMOS kits are available now, and quantity production is scheduled for fourth quarter.

THREE GaAs VENTURES TAKE-OFF  Gallium arsenide manufacturing plants have recently been completed by Honeywell and Ford Microelectronics. Tektronix introduced its first GaAs product in December 1984, but has just formed a subsidiary for GaAs IC marketing and manufacturing called TriQuint Semiconductor. The Honeywell line is expected to be in full production by July, and Ford is shooting for the third quarter.

BOTH 4.2 AND SYSTEM V UNIX PORTED TO APOLLO  Apollo Computer Inc. has become the first computer manufacturer to offer both Berkeley 4.2 and System V UNIX on a 32-bit workstation. The twin port, called Domain/IX, allows users to run either 4.2 or System V or both simultaneously on the same node.

MAINFRAME LINES TO VIE FOR IBM MARKET  Both National Advanced Systems and Burroughs have introduced new mainframe computer lines. These come in the wake of IBM's Sierra and appear aimed at the same markets.
DON'T LET SPEED SLOW YOU DOWN.

The Mostek BiPort FIFO takes your processor out of the loop.

Until now, buffering two devices with different data rates meant one of two things. Either extra hardware design effort. Or software loops to slow your processor down while it's waiting for a peripheral or a coprocessor to be available.

But now there's a better way. The BiPort™ FIFO from Mostek. You can do away with the need for extra hardware design and software loops, and let your processor operate at its optimal performance level.

Our MK4501 is a 12.5 MHz CMOS device with access times as fast as 65 ns. It can handle asynchronous and simultaneous reads and writes from each respective port. And its 512 x 9 architecture is fully expandable by word width or depth. It even has a retransmit capability.

There's nothing quite like it. Except our MK4511. The MK4511 is similar, but has the added advantage of being a true dual-port RAM that's randomly-accessible for bi-directional applications.

So put a speedy end to your interface problems. Call or write Mostek for more details.

Mostek Corp., 1215 W. Crosby Road, MS1051, Carrollton, Texas 75006, 214/466-7479. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5.681.157-9.

BiPort is a trademark of Mostek Corp.
TECHNOLOGY TRENDS

CAD

Designing ICs With A Silicon Compiler

Digital Design is currently implementing a crosspoint switch onto a gate array. (See Digital Design, January, February, March 1985). In addition to the gate array design, we recently implemented the same circuit using a silicon compiler from Silicon Compilers Inc. (SCI) of San Jose, CA.

Genesil System Description

The Genesil silicon compiler system hardware consists of a VAX 11/750, 4 Mbytes of main memory, 450 Mbytes of Winchester disk storage, a 1600 bpi tape drive, four 1024 x 780 color terminals and a mouse. System software includes packages for function synthesis (i.e., the compiler), auto place-and-route, functional simulation, timing analysis and geometric layout.

Integrated circuits are designed with the Genesil silicon compiler using a hierarchical set of objects: chip-set, chip, module and block. Blocks, the most primitive objects, are synthesized according to the needs of the user. Modules are composed of blocks and other modules; chips are modules that have bonding pads, and chip-sets are collections of chips.

The first step in the design process is to select a generic type of function from the function set menu. Next, the block is tailored to the design's requirements by selecting the electrical and functional parameters necessary to implement a specific instance of that function. Genesil automatically flags electrical, timing and clocking violations and prevents blocks violating these rules from being synthesized.

Once the block is defined, Genesil compiles three distinct views: the geometric view (i.e., the actual transistor layout), the timing model and the functional model. These models can be used for immediate verification by the system's timing analysis and functional simulation subsystems. Based on Digital Design's gate array design experience, separating timing from simulation is far more efficient than performing the two analyses concurrently.

After verification is complete, the circuit undergoes place-and-route. Routing priorities can be assigned to various signals so that critical paths are made as short as possible. No other user input is required. All bus signals are routed together, providing for a more efficient chip layout and maintaining bus timing integrity. The router also sizes power and clock lines to minimize resistances. At the same time, Genesil checks that interconnects will be able to maintain proper current densities and signal levels. After the chip is automatically placed and routed, the circuit is again simulated and its timing verified using actual wire delays.

Preparation for tooling is the final stage of the silicon compilation design cycle. In readying the chip for fabrication, Genesil produces a magnetic tape containing a layout optimized for a specific foundry fabrication line. At present, Genesil can generate NMOS designs. However, SCI will shortly introduce software that allows designers to build CMOS devices.

Genesil automatically generates a full report of the design that includes detailed manufacturing instructions. In addition, the designer can produce timing data sheets at any level from block to chip-set, document ROM and PLA truth tables, and generate hard copies of block, mod-

Figure 1: As opposed to specifying a design in terms of logic elements, silicon compilation is based on the high level architecture of the design. The architectural specification is made up of inputs, outputs, control lines, clock, power and ground. The specification shown illustrates the parameters of Digital Design's digital crosspoint switch.

Figure 2: After exploring several architectural possibilities, Digital Design and the SCI Applications Engineers concluded that this would be the best implementation of the crosspoint switch. The final design consists of two data paths, an 8-to-1 by 4 mux and a decoder PLA. In this schematic, only the data path is shown.
A CRASH COURSE IN DISK AND DRIVE TESTING:

**Disk Testing**
ADE RVA instruments will show you how to test excessive acceleration, flatness, radial waviness, datum positioning, axial run-out and thickness.

**Spindle Testing**
Learn the nuances of testing axial and radial runouts, bearing quality, axial/radial acceleration, non-repetitive runout, radial resonance, wobble, and high frequency vibration.

**Head/Assembly Testing**
ADE RVA instruments give you advanced instruction on head positioning accuracy, head motion studies, dynamic flight characteristics, pitching and rolling.

ADE RVA instruments maintain quality control from design through production. Only ADE systems can measure dynamic displacements from tenths of microinches to thousandths of an inch from 0 to 50 KHz frequency response.

ADE Corporation
77 Rowe Street
Newton, MA 02166
Telephone: (617) 969-0600
Telex: 922415

Circle 29 on Reader Inquiry Card
ule and chip specifications.

**Taking Genesil For A Test Drive**

Like most engineers given a design task, we were accustomed to working with gates, registers and multiplexers. Despite a clear understanding of how the chip was intended to function, we did not attack the design from a system level approach. Instead we began describing the circuit at a detailed level (i.e., flip-flops and multiplexers). This was the wrong route to follow because the silicon compiler’s strength is in removing the designer from specifying logic.

To exploit Genesil’s power, we began to formulate the crosspoint switch’s architectural, or block level, description. A specification emerged based on the switch’s inputs, outputs, control lines, clock, power and ground (Figure 1). Once described at this level, several architectural possibilities were proposed. The most efficient solution seemed to be a 4-bit parallel data path structure. The switching function would be accomplished by a general input port, a general output port and a tri-state bus connecting the input and output stages. In addition, a programmable logic array (PLA) would be used to decode the input control lines. The decode mechanism configures the switch for routing signals between the input and output stages. This architecture was entered, compiled and plotted for silicon area in less than one hour.

Since the circuit was not yet simulated, the design was far from complete. However, we did have the die size, performance and propagation delay data necessary to make informed trade-off decisions. Of paramount importance is whether this implementation of the crosspoint switch satisfies cost and performance requirements dictated by the design specification.

In discussing how to reduce die area with several SCI system engineers, an input multiplexing scheme using random logic, (i.e., four 8-to-1 multiplexers) emerged. Genesil’s function set includes random logic. Other building blocks found in Genesil that were unnecessary for this design include RAMs, ROMs, FIFOs, Stacks, 4- to 32-bit wide data paths, ALUs and Barrel Shifters. Since the input stage uses multiplexers, the remainder of the data path must handle output multiplexing and latching (Figure 2). In this instance, splitting the output muxing into two sections provided increased floorplanning flexibility. The resulting crosspoint switch architecture consists of two data paths, an 8-to-1 by 4 (depth) mux and a decoder PLA (Figure 2).

After entering the architectural modifications, the chip was again compiled. In conjunction with compilation, the new architecture was combined with a standard pad ring, routed and plotted (Figure 3). It took three hours to input the updated architecture and pad ring, to compile and to route. Naturally, before transforming the design to silicon, the switch would undergo more simulation and timing analysis. The circuit uses 891 transistors. Comparing overall die size to active area (Figure 3) shows very inefficient silicon usage. The “core,” or active area, is less than 5% of the total chip size. Actual chip size is dictated by the bonding pad size. Implementing the design on two chips instead of one would reduce the number of pads on each chip. Each of the resulting ICs would be approximately one-fourth the size of the present implementation. Moreover, two smaller devices would be less costly than one larger part. Of course, if decreased chip count is the ultimate system goal, the single chip route would be followed.

The primary advantage of silicon compilation is the speed it provides for custom IC design. The entire implementation of this chip, including exploration, took only five hours. In addition, this technology offers the ability to explore alternate architectures rapidly. Analyzing size and power consumption of several different implementations of the same design offers the designer tremendous leverage throughout the design cycle. As a result, architectural creativity is maximized.

At the same time, however, a silicon compiler is a sophisticated tool that demands an experienced system design engineer. In order to utilize the full power of Genesil, the designer must be intimately familiar with system design considerations. Although Genesil can be used by logic designers, an understanding of system design is needed to exploit the silicon compiler’s capabilities. A true systems architect would be the best candidate to use Genesil.

— Collett
One of the easiest ways to interact with a computer is through a touch activated display. One that lets you merely point your finger at what you want your computer to do. With touch, even the most complex application can become user friendly. And less susceptible to user error.

But the advantages of the highly reliable infrared touch input systems have been overshadowed by cost. Placing them out of the range of medium to low-cost turnkey systems manufacturers.

Which is the main reason Carroll Touch completely redesigned its line of touch input products. We call it Smart-Frame™. Because it contains a powerful microprocessor built into the frame. And because it uses scanning infrared technology—a touch technology which is incredibly reliable, rugged, accurate, and fast. A technology Carroll Touch pioneered and refined.

As a result of the Smart-Frame design, Carroll Touch units contain 45 percent fewer components than before. Which means the cost to you is about 50 percent lower too.

We think that's pretty smart. And Carroll Touch did it just so you could get in touch. Today.
Design Verifier Flags
Potential Problems

Digital Design published a three-part series on designing a digital crosspoint switch using a CMOS gate array in January, February and March of this year. The vendors participating in the project are LSI Logic (Milpitas, CA), Valid Logic Systems (San Jose, CA) and Datacube (Peabody, MA). LSI is supplying its cell library; Valid's contribution is the Scaldsystem workstation; and Datacube designed the circuit. Since the project was still underway when Part III went to print, progress reports will be published periodically. This update focuses on the network summary generated by LSI Logic's Design Verifier.

The Design Verifier, highlighted in Part II, runs on Valid's Scaldsystem. Its purpose is twofold: to provide the designer with statistically based interconnect wiring delays for simulation and to generate a network summary. The information compiled in the network summary includes network connectivity, number of gates used, number of bonding pads required, number of I/O pins required and percentage of interconnect wires that can be automatically routed.

After entering the schematic and compiling the logic, the designer invokes the Design Verifier. The most difficult step in using this tool is choosing the right gate array. LSI Logic offers three array families: the LL3000, the LL5000 and the LL7000. The LL5000 Series satisfies our performance requirements, so a particular chip in that family must be selected. Since only a preliminary estimate of the circuit's size is available, picking the proper array is done by trial and error. The crosspoint switch (Figure 3) has an estimated gate count of 1400 gates. Among the various arrays in the LL5000 family, the LL5140, a 1404-gate chip and the LL5220, which has 2224 gates, potentially satisfy the circuit's requirements.

Both devices were input to the Design Verifier. Each run executed in less than two minutes; the results are given in Figures 1 and 2. As shown, the switch uses 1263 gates. Even more important is wireability, which indicates whether a particular chip meets the needs of the design. This percentage is calculated as a function of number of gates used, average pins per net (i.e., average fanout per node) and number of signal nets, excluding outputs.

Other information gleaned from the summary includes the number of additional VDD and VSS pads, a comparison of total number of chip pads to number of array pads actually consumed and maximum pins per net. Extra VSS and VDD pads are necessary because certain buffers in the circuit require added current drive capability.

Several problems with our design are flagged by the Design Verifier. The most
At last, convincing hard copy from your high resolution display.

Presenting the Honeywell VGR 5000. It delivers true-to-life hard copy from a slew of video sources including 60 Hz noninterlaced displays with 1280 x 1024 resolution.

It interfaces directly with the video display using simple BNC cables. No CPU time or special software required. It even provides copy from monochrome or RGB displays in just 14 seconds.

And when you examine the contrast, density, and gray scale qualities of its hard copy, you’ll see something you don’t usually see from a video graphic recorder: Every last detail.

For information contact Bob Shipman, (303) 773-4651, Honeywell Test Instruments Division, Box 5227, Denver, CO 80217-5227.

Together, we can find the answers.

Honeywell

Circle 25 on Reader Inquiry Card
critical problem is a need for 116 array pads (i.e., bonding pads). Neither the LL5140 nor the LL5220 have enough bonding pads for this circuit configuration. Only 92 pads are available in the LL5140 and 114 are provided in the LL5220. Therefore, the design must be modified.

One solution is to use internal buffers drawing less current. LSI Logic offers several different buffers. The high current driving (8 mA) buffers originally used require twice as many I/O pads and more power and ground pads than 4 mA buffers. Changing to these low current buffers will reduce the number of pads needed by about 30.

A second problem is routing the chip. Assume for the moment that the number of pads will be reduced to 86. At first glance it appears that the LL5140 would be the best choice. But using the LL5140, the autorouter can make only 88.68% of the connections. Since the LL5220 is a much larger device, the autorouter can perform 100% of the routing. The issue is whether to manually route the remaining connections of the LL5140 or use the LL5220. Each solution has a drawback. Manually routing the chip could require many additional man-hours to complete—if 100% routing is possible at all. On the other hand, the LL5220 is more costly, and using it wastes approximately 700 gates. These gates could be utilized if more logic were put onto the chip, but this may also create problems. Additional logic, in this instance, demands more bonding pads. Moreover, adding circuitry not part of the original design specification would require spending more time on the project. The upshot would be an extension of an already delinquent project's design cycle.

The ideal solution would be to use an 1800-gate array, but LSI Logic does not offer such a chip in the LL5000 Series. Problems of this nature are discussed at length in Part I (January 1985).

The next update report will cover which array is to be used and the basis on which that decision is made. Details on the feasibility of manually routing the LL5140 or simply using an LL5220 will be provided. Timing verification and simulation results will also be included.

— Collett
Six reasons why professionals continue to choose Vectrix for quality IBM XT/PC graphics.

Even though IBM offers a color graphics card, professionals still choose Vectrix. It's not surprising. Especially once they've seen us in action. Professionals know that our VX/PC Board Set delivers the quality and performance they need for serious color graphics.

The VX/PC Board Set provides advanced features that help simplify sophisticated graphics design. Besides displaying 512 simultaneous colors from a palette of 16.8 million, the VX/PC supports an extensive library of on-board graphics macros for ease of programming and fast design, as well as full emulation of the IBM color card. And, an on-board 16-bit microprocessor frees your computer to concentrate on other tasks.

But that's not all. Our 9 bit planes add an extra dimension of sharpness and clarity to your image that must really be seen to be appreciated. That's why it's not surprising to see Vectrix color cards in applications such as medical imaging, weather satellite data mapping, computer aided design and drafting, and graphics arts, to name a few.

What you will find most surprising, however, is the price. Our VX/PC Board Set was designed with the OEM in mind. So when comparing the performance of Vectrix with the competition, check the price too. You'll like what you see.

For more information, contact Vectrix Corporation, 2606 Branchwood Drive, Greensboro, North Carolina 27408. Phone (919) 288-0520. Telex 574417.

Circle 55 on Reader Inquiry Card
PC-Based Software Produces High Resolution Graphics Files

High quality presentation graphics displays such as scientific plots require high resolution. Although scientific calculations are often performed on personal workstations, the graphics resolution of the IBM PC is not adequate to create accurate detail. A software package from Scientific Endeavors (Kingston, TN) produces complex scientific plots on the IBM PC.

Called GraphiC, the software is a set of C programs for creating plots, graphs and text for scientific and engineering applications. Although the program runs on a PC, the resultant graphics are not limited to the IBM PC display resolution. For high resolution display, the software can create a display list output file for driving Tektronix-compatible output devices. This is useful for entering and previewing scientific data or formulas on the PC, then displaying the results on plotters or high resolution display devices that read Tektronix files.

This software directly addresses the needs of scientific environments. These settings require high quality graphics images but may mainly use limited resolution computer hardware. However, many academic, scientific and industrial organizations do have access to devices that read Tektronix graphics files. Therefore, the authors of GraphiC turned to the IBM PC for program and graph development and to Tektronix format for intermediary display files. This combination creates the accurate plots and displays needed while allowing users to manipulate information on their personal workstations.

GraphiC is modeled around DISSPLA from ISSCO (San Diego, CA). The GraphiC package is a collection of graphics routines written in C. Users can write simple C programs and use the graphics subroutines for creating complex plots. Hidden line and 3D routines are standard (Figure 1). All plots are created with the Tektronix format 4096 x 3120 pixel resolution. In addition to graphics capabilities, GraphiC also has 10 fonts, four of which are simultaneously available. Greek letters and math symbols are available in two fonts. Unlimited levels of superscripts and subscripts may be employed. All font heights are continuously variable.

Features of GraphiC include the ability to zoom, shrink and shift. Routines are available for creating linear, log, semi-log, log-log, 3D and contour plots. An error file is created during execution for debugging. If a plot requires a font not on the current disk, the letters would not be seen, and a file indicating a file not found would be created. GraphiC can reconstruct any Tektronix file from another computer, providing the entire plot was created in graphics mode.

One of the useful features of GraphiC is the ability to print plots on popular dot matrix printers. A C. Itoh or Epson printer can print a 96 x 144 pixel per inch image, whereas an Okidata yields somewhat lower resolution.

GraphiC is designed for use with several compilers; however, the DeSmet compiler is recommended. Complete source code is provided so the end user can create and modify programs. If the user's system has an 8087 installed, which is highly recommended, the software will access and utilize its capabilities. The result is faster execution of arithmetic-intensive graphics such as 3D.

The software was tested at Digital Design using the DeSmet compiler. A program was written to display a 3D plot on the PC and create a Tektronix file. The file was then displayed on a Qume QVT-211GX terminal, which has 4010/4014 capability. The resolution quality of the Qume was excellent. A complex 3D display using an 8087 took approximately 10 seconds.

Figure 1: GraphiC can display a 3D plot with hidden line removal and text like this one in approximately 10 seconds. Though the program runs on an IBM PC, display list output files are in Tektronix format for high resolution display and printing or plotting.

-MacNicol
For 13 years some of the biggest names in the business have been bringing us their toughest power supply requirements.

Why? Because we work with them, beyond their specifications. Quickly. Effectively. Creatively.

How? By being highly sensitive to their needs. By working closely with them to develop the power supply that meets both their specifications and their system's requirements. By value-engineering our design before production to insure a cost-effective product. By carefully balancing materials and manpower to maintain flexibility.

PSI is committed to meeting International Safety requirements. We have developed a Safety Certification Package with all the data and specs needed to obtain approval from UL, CSA, and VDE, and other certifying organizations. And we are authorized to self-certify power supplies.

Whether your power supply requirements are simple or complex, bring them to us. Power Systems, Inc. Where powerful solutions are everyday achievements.

To find out why Power Systems, Inc. should be your power supply vendor, contact:
Power Systems, Inc., 12 Tobey Road, Bloomfield, Connecticut 06002, Tel. (203) 243-0357, TWX 710-425-8778

Power Systems, Inc.

Circle 19 on Reader Inquiry Card
The increasing size of main memory in multiprocessor systems demands that memory ICs be small, fast and inexpensive. Static random-access memories (SRAMs) are small and fast, and require no refresh circuitry. However, high prices have kept SRAMs out of most main memory applications, where dynamic random-access memories (DRAMs) are preferred. SRAMs have become special-purpose devices used primarily by systems architects requiring low power consumption, high speed, board space savings or ease of use.

Nevertheless, companies such as Fairchild Camera and Instrument Corp. (Puyallup, WA), Hitachi (San Jose, CA) and Inmos (Colorado Springs, CO) are very optimistic about the future for the new generation of 64K SRAMs. According to Dan Pichulo, SRAM product marketing manager at Hitachi, SRAMs organized as 64K x 1 lend themselves to several applications.

One possible use of these devices is as the main memory for either mainframe computers or superminicomputers. High performance machines demanding very fast access times may find CMOS SRAMs comparable in speed to ECL memories, without the problem of high power dissipation. Richard Phlegar, memory products planning manager at Fairchild's Memory and High Speed Logic Unit, believes that SRAMs with the x1 organization are particularly well suited to error detection and correction in mainframes and minicomputers. However, unless the costs of SRAMs decrease, a main memory using SRAMs may not be forthcoming in the near future.

The good access speeds of SRAMs may also make the devices viable as fast writeable control stores for software. A nonvolatile memory such as a ROM can take up to 150 nsec to access the software program; for some users, this may not be fast enough. Present 64K x 1 SRAMs have access speeds between 45 nsec and 70 nsec. In addition, the CMOS SRAM can almost function as a nonvolatile memory due to its low power requirements—a battery would maintain the current necessary to retain memory.

By far the largest potential applications for the 64K x 1 SRAM are cache and buffer memories for high performance systems. The mismatch between microprocessor speed and DRAM memory speed has caused system architects to rely on caches in order to minimize frequency of access to main memory. With new MOS SRAMs offering higher speeds and lower power dissipation, the switch from ECL parts to SRAMs for cache memory applications will certainly continue.

Fairchild, Inmos and Hitachi have taken similar manufacturing approaches to their 64K x 1 SRAMs: the memory cell is processed in NMOS and the peripheral support circuitry is CMOS. Kirk MacKenzie, Vice President of Marketing and Sales at Quasel Inc. (Santa Clara, CA) approves of the mixed process devices, saying that it may be the most cost-effective way to produce low power, high speed SRAMs. NMOS allows a higher density storage element and enables a smaller die size than a fully CMOS SRAM. CMOS peripherals reduce power dissipation problems. In addition, CMOS circuits are more resistant to soft errors.

Even with the access time improvements made on MOS SRAMs, several supercomputer and superminicomputer manufacturers still feel that the new generation of 64K x 1 devices are simply not fast enough. They would like to see the larger SRAMs comparable in access time to smaller SRAMs such as the 16K x 1, which can now reach speeds of 25 nsec. If SRAM manufacturers can push the 64K x 1 SRAM to those times, then perhaps systems architects for those larger systems will view the device as a better upgrade.

—Meng
Talk about easy interfacing.
You can take a ZETA 824 or ZETA 836 plotter and plug it into virtually any computer made.
What’s more, you’ll be ready to run because our plotters understand a variety of computer protocols. Select the model for your application then just plug in and plot.
In fact, we’re a plug compatible replacement for many plotters from HP, CalComp and Tektronix. Some models of our plotter can even run directly from your IBM cluster controller. Now that’s easy interfacing.
When it comes to your favorite application packages, you’ll be on safe ground too. Packages such as CADAM, TechniCAD, Euclid, P-CAD, AutoCAD and many more.
The most productive plotter for the money.
You’ll be getting the highest output plotters for the money with our new ZETA 824CS and ZETA 836CS. More finished plots. More productivity. Plus, these “D” and “E” format plotters let you run either single sheet or roll media.

Easy-to-use touch controls.
Your time is valuable. So we’ve made our touch controls simple—yet powerful. Set speed, pen pressure, liquid ink parameters, electronic limit sensing, windowing, scaling—all at the touch of a finger, Self-test and diagnostic plots too. Let us show you dozens of other time-saving operations in a brief demonstration.

Plotter specialists.
We’ve been designing hardware interfaces, plotting language emulators and high performance pen plotters for over 14 years. Nicolet also provides you with worldwide sales and service support.
Give us a call. See how easy it is to join the crowd.

Call (415) 372-7568.
Nicolet Computer Graphics Division, 777 Arnold Drive, Martinez, CA 94553
TWX 910-481-5951

Nicolet
Computer Graphics Division

CADAM is a trademark of CADAM, Inc.
TechniCAD is a trademark of Tektronix, Inc.
Euclid is a trademark of MATRA DATAVISION, Inc.
P-CAD is a trademark of Personal CAD Systems.
AutoCAD is a trademark of Autodesk, Inc.

Circle 18 on Reader Inquiry Card
COMMUNICATIONS

Options Multiply For High Speed Unibus Communication

A single Unibus board may now provide 1 Mbit/sec or faster data communication for DEC minicomputers. The DMZ 32 from Digital Equipment Corp. (Maynard, MA) provides a 1.544 Mbit/sec T1 trunk for 24 multiplexed lines; it comprises a distribution panel and a Unibus module. DEC is also manufacturing a 1 Mbit/sec interface board for links to AT&T’s Datakit Virtual Circuit Switch. The KMS11-K will be offered by AT&T Technologies (Morristown, NJ). For host-to-host links, Advanced Computer Communication (Santa Barbara, CA) offers the ACP 6100 (Figure 1) for nonmultiplexed T1 connection.

AT&T’s Datakit-to-Unibus board will provide a multiplexed channel between computer and data switch. This board will operate at 1 Mbit/sec, not the 320 Kbits/sec of products linking AT&T 3B computers to Datakit. Initially, AT&T will use the KMS11-K internally for telephone company links. Distributors of Datakit as a twisted-pair local area network will also offer the board.

Although the DEC and the ACC boards both have Unibus and T1 interfacing, they serve different purposes. T1 speed is used on DEC’s product as a trunk for multiplexing up to 24 lower speed lines, while ACC uses the entire channel for a single 1.544 Mbit/sec link. The DMZ 32 is an extension of DEC’s asynchronous multiplexer line (Digital Design, March 1985), in which distribution panels are used for multiplexing and demultiplexing channels (Figure 2).

DMZ 32 panel may be next to the computer or remote, connected by two cables for the T1 link. The Unibus board at the host contains RAM shared by the Unibus and the 1.544 Mbit/sec T1 line.

An active distribution panel manages the individual terminal lines. Maximum speed on each line is 19.2 Kbits/sec. The DMZ 32 provides modem control and split baud rate on all lines. The system also has DMA capability on transmit. The board architecture speeds communication functions, and the distribution panel off-loads line handling.

With the ACC front-end processor board, Unibus computers can transmit and receive one full-duplex channel of HDLC at 1.544 Mbps. While the DEC board uses shared RAM between the Unibus and the T1 interface, the ACP 6100 centers around a four-port DRAM array surrounded by four 68000 microprocessor buses (Figure 3).

Each bus in the “Quadbus” system is independent and electrically isolated, resulting in high throughput and minimum waiting for bus access. RAM access is made central to the system, not the microprocessor bus, since memory is what peripherals need. Individual bus segments are connected or disconnected according to bus activity.

In addition to the 68000 CPU bus (CBUS), there is a peripheral bus (PBUS), a DMA bus (DBUS) and a Unibus (UBUS). Three-state buffers isolate each bus from memory signals. An 8409 provides DRAM timing and control.

Figure 1: Host-to-host communication at 1.544 Mbits/sec is provided by ACC’s ACP 6100 Unibus board. A four-bus architecture is used to achieve such high speed.

Figure 2: T1 speed of 1.544 Mbits/sec is used as a trunk to multiplex up to 24 channels in the DEC DMZ 32. T1 and Unibus interfaces share on-board RAM. The distribution panel in the background handles multiplexing and demultiplexing of individual lines.
WINCHESTER, FLOPPY AND TAPE
All on one board

Our OMTI 5400 SCSI (SASi) controller offers Winchester, floppy and tape support all on a single 5¼" footprint PC board. By using our proprietary VLSI chip technology, we were able to squeeze all these functions onto a board size that most controller companies are still using for single function controllers. This means increased capability and improved cost-effectiveness in your application.

As a forward-looking OEM, you want multifunction SCSI (SASi) data controllers that meet your needs today and can meet the challenges of future developments in peripheral device technology. As you would expect, we've applied our new technology to meet these challenges in a whole family of SCSI (SASi) data controllers, the OMTI Series 5000.

UNBEATABLE FLEXIBILITY
Our OMTI Series 5000 family of SCSI (SASi) controllers supports industry standard ST506/412 5¼" fixed and removable Winchester disks. 5½" and 8" floppy disks and QIC-02 compatible streaming tape. Each controller is SCSI (SASi) compatible to protect your software from change as you add next generation disk and tape technologies. And they are all second-sourced to guarantee availability.

HIGH PERFORMANCE
The Series 5000 controllers provide consecutive sector, non-interleaved data transfer and multisector buffering between host and peripherals. In addition, our data buffer supports simultaneous transfers between Winchester and streaming tape for fast image backup operation. No other manufacturer offers you performance like this!

EASY TO USE
Our high-level SCSI (SASi) command set off-loads your host CPU. Only one command is required to completely backup or restore Winchester data to and from tape, all without host intervention. Separate host-initiated commands allow selective file backup and restore. A sophisticated 32-bit ECC and automatic error retry means that reliable data is always available to the host. Finally, automatic Winchester flaw management handling prevents disk defects from corrupting your system.

To learn more about the OMTI Series 5000 data controllers, please contact us for additional information.
biration and timing to determine which of the buses gets memory cycles is implemented in PALs. The PBUS is given highest priority for memory access because it may interface to high burst rate devices like network controllers. Next priority is the Unibus, then the DMA bus and lowest priority is the CBUS.

Since 68000 and Unibus memory organizations differ, data transfer between the two is via the DBUS interface. A four-port 68450 DMA controller programmed by the 68000 exchanges bytes in a word for transfers to and from the Unibus. The 68450 also ties into an 8068 for data encryption. This security feature meets National Bureau of Standards Data Encryption Standards (DES).

Using the four-bus architecture of the ACP 6100 for a single channel provides speed adequate for computer-to-computer transfers. In contrast, most communication lines operate at several hundred Kbits/sec maximum. ACC calls this the first iteration of the Quadbus architecture and plans to use it in other products where RAM access is the bottleneck.

These are only three of the available Unibus communications products. Since they occupy only one backplane slot, a variety of connections can be made from one host. Microprocessor control and shared RAM architectures will allow communication boards to act as front-end processors and extend access to valuable resources.

—Pingry

Fiber Optic Transmission Schemes Expand Standard Local Area Network Possibilities

Fiber optics suppliers have long been seeking nontelephone applications for the technology. Now fiber optics can realistically compete in the active local area network market. Several companies have had optical links for single node connection into a coaxial cable network for years. Totally fiber networks have been available from only a few sources and operate on a passive star scheme. WhisperNet, an all-fiber network from FiberCom (Roanoke, VA), is an active ring topology Ethernet, more like coaxial systems (Figure 1).

Fiber optics are best suited to point-to-point links, mainly because taps (as in a bus configuration like Ethernet) cause large power drops. The all-optical 802.3 Ethernet systems that have been available for several years have put point-to-point links from all nodes into a central wiring cabinet (Figure 2). Within the cabinet is an optical star coupler, where input signals are distributed to all output fibers. Both Siecor (Hickory, NC) and Codenoll Technology (Yonkers, NY) use this star-shaped broadcast system.

One reason that these optical networks do not use a physical ring is that if any node in a ring fails, the entire network goes down. FiberCom has a bypass scheme that assures the network will continue to function even if three consecutive nodes have failed. Fully reversing bypass switches developed and produced by Kaptron (Palo Alto, CA) used at each WhisperNet station provide this ring reliability. With star-shaped networks, the active collision detection components in the central cabinet can also bring down the entire network if they fail. Siecor has
High Speed Battery-Backed Static RAM Functions as Nonvolatile Primary Memory for Your System Without Special Software Interfaces

All of DTI's CMOS RAM boards feature low power CMOS design, 5 year (Lithium) or 3 month (NiCad) data retention, automatic memory protect, and full compatibility with bus specifications:

**MULTIBUS** • CBC 512/24 Series
- 16K up to 512K-byte versions
- 16, 20, or 24-bit addressing
- On board bank-switching option gives 1M byte RAM access for 16-bit address bus; 16, 32, or 64K bank sizes
- All-CMOS single board computers with nonvolatile CMOS RAM also available

**Q-bus** • LM 1164 Series
- 16K up to 64K-word versions
- 22-bit addressing
- 4K-word base address boundaries
- Selectable write protects on 8K-word boundaries
- 0.5" card spacing

**VMEbus** • VM 256 Series
- 16K up to 256K-byte versions
- 24-bit addressing
- 8, 16, 32-bit data transfers
- Switch selectable write protects at front panel
- Variable access timing

**Custom Design/Manufacturing**
- Advanced CMOS design methods
- Fast prototype turnaround
- Competitive volume pricing

For more information on DTI's RAM products, CMOS CPU boards for the MULTIBUS®, CMOS MULTIMODULE®, and custom designs, contact Bill Long, CBC Product Manager at (601) 856-4121

P. O. Box 748, Ridgeland, MS 39157
Telex 585326
addressed that problem by providing collision detection in the transceivers and a fallback passive mode for the wiring center.

Despite the limitations of point-to-point networking, some other features of fiber optics are attractive. It is immune to EMI and RFI; many current optical links are installed to minimize induction effects from lightning or industrial equipment. Conversely, since signals are optical and not electrical, they do not radiate. This makes meeting FCC regulations easier, and WhisperNet can meet military Tempest specs as well. Optical links are free of ground loops and dielectrically isolate attached devices. In addition, bandwidth is broader (requiring no equalization), and attenuation rates are much lower for optical cable than for coaxial. Longer transmission links can be made without repeaters using optical fiber.

Fiber optic data communication links are mainly used to extend the distance between two devices. This benefit may extend to optical networks as well. Ethernet nodes on a coax system are specified at a maximum of 1.8 km apart with 500 meter maximum segments. Siecor claims Net 10 segments can be up to 2.5 km long. To maintain total Ethernet compatibility including propagation delay, Siecor uses the same 2.5 km end-to-end maximum as coax systems.

The WhisperNet ring can be up to 4 km end-to-end. Whereas the 1024 node maximum Ethernet configuration using coaxial cable can cover 5 square km (1.9 square miles), a WhisperNet network of 1024 nodes can cover 50 square km or 19 square miles. This assumes multiple rings, such as one on each floor of a building or one 4 km ring in each building of a campus linked together to make a large system. How Ethernet timing is achieved over these longer links and whether it is strictly 802.3 compatible has been questioned. The extra distance, however, can be a major advantage in using optical cable. FiberCom claims they meet all performance specs.

In the maximum node 5 square km coaxial system, about 100 repeaters are needed. Unlike signals in coaxial cable, optical signals do not attenuate rapidly. The optical network covers 10 times the area but needs no repeaters. The number of repeaters is not the only part of a coax network that is more expensive than the optical equivalent. Optical cable is now as inexpensive as $0.60 per foot, compared to over $2.00 for Ethernet coax.

Installation costs of optical cable networks have always been an advantage because the thin cable is easier to carry, bend and maneuver. In some instances, Ethernet cable is so bulky that it will not fit in remaining duct space. Until recently, however, transmitter and receiver component costs have more than offset the installation savings. Dropping prices of optical cable and components have allowed FiberCom to proclaim their network lower cost than coaxial in most instances. Siecor points out that a central star eases diagnostics and fault isolation, one of the largest factors in installation.

The 1024 node limit is not necessarily the maximum number of devices that can be connected. Computers, terminals or other devices link into a WhisperNet either through TFT-10 transceivers or communications servers called WhisperServs. Servers can link up to 32 devices into the network. In the Codenoll Codenet system, an optical star coupler is needed for every 16 nodes. Stars can be connected together for a "snowflake" topology network. Either Codenet 2020 transceiver boxes or transceiver hybrid modules used on a circuit board connect nodes to the star coupler.

Wiring centers for Siecor's Net 10 include star couplers with 8 x 8 (8 input and 8 output = 8 nodes), 16 x 16 or 32 x 32 ports. As the star broadcasts a signal to all input ports, passive taps pull
Microbar's K-2 family takes the "what ifs" out of designing your next system.

In the SBC business, playing "wait and see" simply doesn't make for leadership. It doesn't make market leaders out of OEMs and system integrators, either. What's needed is foresight—for prudent planning. And flexibility—for fast response to change.

Microbar's K-2 family of Multibus™-based SBCs demonstrates the idea. They're a pure example of look-ahead, ready-for-anything design—the kind of design that can add "front runner" to your reputation.

The K-2 family, for example, lets you set the pace in performance. Because you get 12 MHz operation—with no wait states—for 128K to 3M bytes of memory. You're also perfectly positioned for smooth transition to the full 32-bit 68020 K-2 boards coming this year.

Further, the K-2 family has expansion modules that easily take you to two megabytes of on-board high-speed RAM. Or up to one megabyte with ECC, if you like.

There's a lot more. Memory management modules, for instance. That offer the Unix™-oriented two-level paging. And that make implementing the 68010 virtual memory a snap.

No doubt. The K-2 family reflects thinking that puts "what if" worries to rest. That lets you begin now at any performance or capability level knowing you've maximized future options. And eliminated potential "dead ends."

Of course, looking forward—objectively—is a Microbar tradition. We do it well because we're independent. And because SBCs are our only business. That's what keeps us ahead. That's what keeps you ahead. Better write—or phone toll-free—and find out more. Now.

Within California: (800) 421-1752
Outside California (continental U.S.): (800) 821-1011

Circle 11 on Reader Inquiry Card

"Multibus is a trademark of Intel Corp.
"Unix is a trademark of Bell Laboratories, Inc.
part of the signal off (Figure 3) into collision detect electronics (CDE). Since the signals here are not electronic the CDE cannot use voltage differences to detect collisions like coax CSMA/CD systems. A collision is determined by the presence of more than one signal.

There is no center in Whispernet, which means collision detection resides in the transceivers. As with a coax network, the 8-wire transceiver cable provides one pair for collision detection, one for transmit, one for receive and one power pair. To further enhance industry compatibility, Whispernet will run standard XNS and TCP/IP protocols. The WhisperServ communication servers, supplied by Bridge Communications (Cupertino, CA), can be specified as servers for either protocol. Actual throughput is 200 packets/sec; with 512 byte XNS packets, the maximum throughput is about 1 Mbit/sec.

Ethernet is not the only network being implemented in fiber optics; Raycom Systems (Boulder, CO) offers ARCNET products. Datapoint’s (San Antonio, TX) ARCNET is a 1 Mbit/sec token-passing system, and Raycom offers transceivers and a three-port active hub. These products can be used for an all-fiber network or be combined with coaxial cable into a single network.

The star-shaped ProNet local area network from Proteon (Natick, MA) has been promoted as operating on either twinax (shielded twisted pair) or fiber optics. Two versions of the ProNet token-passing network are available: totally compatible 10 Mbit/sec and 80 Mbit/sec systems. Both ProNet 10 and ProNet 80 are star-shaped logical rings that use the same wiring center concept as Siecor and Codenoll fiber optic networks. Proteon networks include networking software and can use all or part fiber for cabling.

Though commercial systems may be years off, an ANSI committee is working on a 100 Mbit/sec optical ring network standard called FDDI. A high-speed network chip set for this optical scheme may be available as soon as the specification is complete. Texas Instruments and Motorola are designing encoder/decoder chips for this 80 Mbaud throughput. Advanced Micro Devices (Sunnyvale, CA) is also designing several ICs to support that type of network. IEEE 802.8 is a fiber optic task force looking into several issues of optical network schemes.

In addition to these complete optical network systems, an array of companies provide single links into various standard networks. ARCNET links are available from Grass Valley Group (Grass Valley, CA) and Canoga Data Systems (Canoga Park, CA). Optical Ethernet link extenders are sold by Canoga Data Systems as well as the firms offering complete systems. Optelecom (Gaithersburg, MD) provides a link into Apollo’s Domain network.

Optical links have been used in selected places to solve problems, primarily the distance limits of coax but also to guard against lightning or noise damage to signal integrity. Schemes like Whisper-Net and Net 10 may be used for entire networks. Suppliers of other types of fiber optic systems are also looking carefully at the LAN market. Corning Glass Works (Corning, NY) has announced the dB fiber, optimized for networking applications. This is a good sign that networking is becoming a significant market for fiber optic systems.

—Pingry

![Figure 2: The Net 10 system from Siecor Electro-Optic Components uses optical fiber cable medium, shown here with orange jacketing. Small transceiver boxes are used at the nodes, and the large case in the center of the photo is the central Star Wiring Center. The star coupler is hidden here by the coils of fiber from individual nodes.](image)

![Figure 3: Collision condition determination is performed in the central wiring center in the Net 10 Ethernet-compatible optical network. Signals output from each node are broadcast to other points in the network by the star coupler. Part of the signal is tapped off for collision detection. If the collision detect circuitry senses more than one transmission, it sends a jam signal to the input side of the star coupler. Each transceiver sending data notifies the attached node of the collision. The node then times out and tries to retransmit.](image)
THE EMS EDGE

WEIGHT
SPACE
PRICE

PERFORMANCE
Your VME advantage: VMEbus products are designed with your high performance system in mind. Electronic Modular Systems provides TOTAL system function on one board.

REAL TIME APPLICATIONS
CPU-2RT
- 12.5 MHz 68000 processor in pin grid package
- Dual serial ports capable asynchronous and synchronous communications
- 3 16-bit timers
- 16 bits of parallel I/O
- 128 K of dual ported dynamic RAM, upgradable to 256K
- Sockets for 2 EPROMs (Capacity to 128K bytes)
- Sockets for 2 static RAM devices (Capacity to 16K bytes)
- On board VME arbiter so the CPU-2RT can occupy slot 1
- 68450 4-channel DMA (optional)

UNIX® APPLICATIONS
CPU-1
- MC68000 processor
- MC68451 memory management unit
- 256K of onboard memory
- 1K Boot Prom
- RS-232 Port
- Centronics Printer Port
- Floppy Disk Controller for controlling up to 4 x 5.25" or 8" floppy disk drives with DMA
- VMEbus System Interface consisting of:
  - DTB Arbiter
  - DTB Requester
  - DTB Slave Logic
  - Interrupt Handler
  - Bus Time Out Logic
  - System Clock Driver
  - Jumper selectable RWD/ROR

And Support Systems from EMS

VME HD-1
- HARD-DISC CONTROLLER
- 4X5/16 DRIVES
- SEAGATE ST 506 INTERFACE
- 6800 CPU
- INTERRUPT LEVELS/VECTORS ARE PROGRAMMABLE

VME ICC-1
- Z 80 CPU
- 1 PARALLEL PRINTER PORT
- BUFFER, MAX 12 KBYTE
- 4 KBYTE DUAL PORT RAM
- Firmware optimized for UNIX

VME MEMORY BOARDS
- 512 KBYTE — PARITY
- 512 KBYTE — ERROR CORRECTION
- 2 MBYTE — PARITY
- 2 MBYTE — ERROR CORRECTION
- ON-BOARD REFRESH
- ACCESS TIME 270 NS

SOFTWARE SYSTEMS
- UNIX V SINGLE-USER
- UNIX V MULTI-USER
- CPYM 68K
- FORTRAN — 77
- BASIC BASIC
- COBOL
- UCSD PASCAL

Call or write today for our comprehensive product catalog or for further information about EMS CPUs.

4546 Beltway
Dallas, Texas 75244
(214) 392-3473

Robert-Koch-Strasse 1-3
D-6078 Neu-Isenburg, W. Germany
Ph. 011-49-6102-3117

*UNIX is a Registered Trademark of AT&T Bell Laboratories.

Circle 22 on Reader Inquiry Card
In a recent survey, Gnostics Concepts estimated that the single-board computer market would grow to $1.55 billion by 1988. Gnostics predicted that the Multibus I and the Multibus II were projected to take the largest share—44%. The VME bus is expected to have a 19% share.

There are several reasons why the VME's marketshare may be larger than predicted. One of the main indicators of the success of any bus structure in the marketplace is the number of smaller players with vertical market niches who endorse a given specification. Over the past few months, several of this type of manufacturer have either announced products based on the VME or disclosed plans to bring out new products in the next few month. In many cases, these companies virtually own a niche within the Multibus I marketplace.

Xylogics (Burlington, MA), for example, whose customer base includes Sun Microsystems (Mountain View, CA) and Masscomp, has long held the lion's share of the Multibus I disk controller market. However, Xylogics's latest disk controller, dubbed the 751, is based on the VME architecture. The board can control two SMD drives at data transfer rates from the disk up to 2.4 Mbytes/sec and DMA speeds of 10 Mbytes/sec.

Metacomp (San Diego, CA), who possibly has the largest part of the Multibus I intelligent communications controller business with its MPA-2000, has announced plans to enter the VME market with a similar product. Datacube (Peabody, MA), a more vertically based company, also recently disclosed information about a VME board set designed for electronic imaging that can be mixed and matched to a particular customer's requirements. As with any engineering decision, there are trade-offs when deciding which bus structure to endorse.

At the present time, only a few buses can support 32-bit processors—VME, Multibus II, NU Bus and Futurebus. Of these four, the only products commercially available are on the VME and the Multibus II. Of these products though, only one CPU board is available on the Multibus II, the recently announced...
286 board from Intel (Hillsboro, OR). VME, on the other hand, sports over 30 manufacturers (Table 1). Such companies as Motorola (Tempe, AZ) (Figure 1), Ironics (Ithaca, NY) and Matrox (Quebec, Canada) even have 68020 designs on the market today.

An important consideration when deciding which bus structure to endorse is not only the number of manufacturers, but also the potential upgrade path for the product. Multibus I has the largest portion of the OEM board marketplace; a share that is not likely to disappear overnight. Many designs in the market are based on 8-bit CPUs, and the sheer volume of vendors of Multibus I products will make it easy for the systems integrator to upgrade to 16-bit solutions. Furthermore, some smaller vendors have even proposed to upgrade to 32-bit solutions. It is likely that this may lengthen the life of the bus, too.

In the past, the limitation of a 16-bit bus structure has prevented true 32-bit µPs from being available on Multibus I systems. True 32-bit µPs with 32-bit internal and external data paths could not effectively be used on the Multibus I because two 16-bit memory accesses are required for each 32-bit memory access. But Owl Computer (Encinitas, CA) has effectively attacked this problem in the same way that DEC has attacked the design of the MicroVAX I (based on the Q-Bus). Instead of using the Multibus, Owl has chosen to implement a proprietary “over the top” bus between its NS32032-based CPU board and a dedicated memory board. The processor, therefore, does not require the use of the Multibus to access main memory.

The systems integrator may not require additional Multibus memory boards to configure a system although additional Multibus memory boards can be used to increase the total amount of memory. Currently, Owl offers a minimum of 256 Kbytes and up to a maximum of 4 Mbytes.

Although the upgrade path to 32-bits is obviously a smoother road on the VME than on the Multibus I, those designs based on the Multibus I have used mainly Intel iAPX processors. The VME, on the other hand, is primarily a 68000 family-based bus (Table 1). Hence, the problem for those systems integrators wishing to switch from the Multibus I to the VME bus becomes more of a software issue than a hardware issue.

To address the problem of migrating from an older bus structure to a new one, Intel initially promised they would provide an interface from the Multibus I to the Multibus II, but so far no such interface product has been announced. When Sun Microsystems was looking for a 32-bit bus for future workstations in October 1983, it examined both the Multibus II and the VME bus and chose to go with the VME bus. According to Vice President of Technology Andy Bechtolsheim, the Multibus II is the strongest for tightly coupled multiprocessors, but weaker for single-processor systems. This is because the Multibus II is a synchronous bus in which the master and the slave have to synchronize the bus. This maximizes available bandwidth in multiprocessor systems, but degrades performance for a single-processor system with asynchronous master and slave because of the number of synchronization points. Multibus II also required custom-bus interface circuits that were not available.

Sun's implementation of the VME bus was done on triple height/full depth Eurocards (366.66 mm × 400 mm) so that major system components could be placed on a single board.

Figure 2: Sun Microsystems' VME-based workstation is based on triple-height full-depth Eurocards.
Multibus II system builders may find that they are faced with the same space constraint problems as their VME counterparts, especially if they wish to include all the features of the bus such as unsolicited data messages and sequential transfers. NCR Corp. (West Columbia, SC) has already proposed a triple height version of the Multibus II, but has been forced to design three custom 84-pin gate arrays to support the advanced features of the bus. For the OEM, the form factor of newer buses is a vital consideration. Products available on the VME today are most commonly found in a single or dual category. But as the use of custom VLSI increases and number of dedicated VME ICs from Signetics (Sunnyvale, CA) and Motorola increases, the single-height module may become more popular.

One company banking on that trend is Microcosm (Beaverton, OR). It recently entered the VME market with a line of VME products that center on a cache-based 68000 board. The companies' future product plans include a VME bus system controller board, an EPROM/Static RAM board and a 512 Kbyte dynamic RAM board. Microcosm's main competitor is Mizar (St. Paul, MN) who has been in the market with a 68000-based single-height VME card for some time.

Another interesting fact to consider when choosing a bus structure is the systems integrators' familiarity with the older bus structures and their modes of operation. In terms of its structure, it would be more appropriate to class the VME in a group of older bus structures, such as the S-100 and the Multibus I, rather than directly compare it to the Multibus II. However, this may turn out to be more of a benefit than a detriment to the success of the bus. Going the VME route, the systems integrator would clearly not have to go through a re-education process as he may have to with Multibus II.

The major market for both the Multibus I and the VME is the area of real-time control. One of the most important requirements of this market is to provide an interrupt handling and generating mechanism to schedule various tasks. In many machine control situations, a number of dedicated processors are controlling an external process. In most cases an architecture of this kind is a single handler system which has a supervisory processor that receives and services all bus interrupts. This allows the supervisory processor to service all interrupts in a prioritized manner. The dedicated processors are not required to service interrupts from the bus, but give primary attention to the interrupts received from the machine or process they control.

In the Multibus I system, the interrupt service lines (IN1D* to INT7*) are used by any bus module to activate an interrupt service request from the system master. A requesting device activates the interrupt signal and keeps it active until serviced (IN1D* has the highest priority). An interrupt acknowledge (INTA*) is generated during interrupt cycles on the bus. It is

### VME Product Quick Reference Guide

<table>
<thead>
<tr>
<th>CPU/MPU</th>
<th>68000</th>
<th>Z-80</th>
<th>80186</th>
<th>Z8000</th>
<th>16000</th>
<th>Form Factor</th>
<th>Single</th>
<th>Dual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arcom Control Systems</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Single</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Astraea</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Dual</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Beston</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Colex</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compcontrol</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dec-Tec</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Systems</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dy-4 Systems</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ebnek</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Elec. Mod. Sys.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electronic Solutions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eltec Electronic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Force Computers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hubner &amp; Worm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intac</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integrated Solutions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ironics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Kontron Mikrocomputer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Manudax</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Micro Computer Systems</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Microsys</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mizar</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Motorola</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Omnibyte</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pacific Microcomputers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PEP Electronik Systeme</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Performance Tech.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Philips International</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sigen</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signetics/Philips</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sky Computers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Systemforschung</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>United Technologies – Mostek</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wormald</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Non. Std. depth**

Table 1: Over 30 CPU products are available on the VME bus. Note, however, the lack of Intel processors that are supported.
DY-4 SYSTEMS INC., one of North America's most successful producers of VMEbus products, now offers a fine array of expertly crafted VME modules and UNIX based development systems - perfect for all your demanding 16/32 bit applications. Stringent manufacturing and quality control ensure a reliable product with maximum power and integrity.

DY-4 realizes the full potential of the powerful VMEbus architecture by using an extended depth Eurocard format of 233mm x 220mm. By increasing functionality and allowing processor, memory and I/O combinations, and bus controller functions on a single board, DY-4's format offers higher performance than competitors' equivalent configurations.

DY-4's commitment to R&D is reflected in its continuing new VME product development, including intelligent communications controllers, SMD/ESMD controllers and 9-track tape controllers. DY-4's VME series currently includes:

- **DSM-6816** - a UNIX based development system.
- **DVME-102** - 68000/68010 CPU with MMU, dual-ported serial I/O and 256K/512K/1 Mbyte DRAM.

DYME-105 - 68000/68010 CPU with dual-ported serial I/O and 14 bytwide sockets.

**DVME-207** - With 6 serial RS-232C/422 channels and 2 parallel I/O ports.

**DVME-357** - A 512K Byte memory board with 1 Megaword per second raster video port. Supports 16032 bit VMEbus readwrites.

**DVME-503** - Universal memory board with 32 28-pin wide sockets. Supports 16/32 bit VMEbus readwrites.

**DVME-712** - Intelligent Z80A peripheral controller with RS-232C/422/16, 64K DRAM with parity, floppy disk controller, SAS interface and DMA.

**DVME-778** - Colour graphics controller supporting 640 X 480 X 4 (1024 X 768 X 2), NEC 7220 GDC, look up table, 3 4-bit D/A converters, mouse input and parallel printer port.

**DVME-909** - A 19-inch rack-mountable system chassis with 9 slot VME card cage, power supply and forced air cooling.
used to freeze the interrupt status of all the interrupt controllers in the system and then get the interrupt vector address from another module in the system. Multibus supports two interrupt implementation schemes: nonbus vectored and bus vectored.

The VME also has dedicated signal lines for handling interrupts. Although the VME bears some resemblance to the Multibus I, it is in the area of handling interrupts that the VME and the Multibus II differ the most. In the VME system, dedicated modules are specified for interrupt handling and generating. This relieves other masters in the system from this task. However, Intel has chosen to handle interrupts without dedicated devices. Intel's solution is done through a message passing routine from one master to another.

The interrupt scheme on the VME bus consists of an Interrupt Handler and an Interrupter. The signals involved are seven priority Interrupt Request lines, IRQ1*-IRQ7*, one Interrupt Acknowledge line, IACK*, and two Interrupt Acknowledge Daisy-chain lines, IACKIN*/IACKOUT*. The Interrupt Handler generates the interrupt acknowledge signal, which drives the interrupt request lines, IACKIN*/IACKOUT*. The seven interrupt request lines IRQ1*-IRQ7* are driven by the Interrupter. The way the interrupt portion of the VME bus works is similar to the way the arbitration portion of the bus works. The seven prioritized Interrupt Request lines, IRQ1*-IRQ7*, work in much the same way that the bus request lines work. When a device wants to access the bus, it generates a bus request with one of the four prioritized Bus Request lines, BRx*. Similarly, a device that wishes to generate an interrupt will drive one of the seven prioritized Interrupt Request lines, IRQx*. The interrupt request lines are driven by the Interrupt, and the Interrupt Acknowledge line is driven by the Interrupt Handler. The Arbiter monitors the Bus Request lines, and when the bus is available, it will drive the appropriate bus grant line. The Interrupt Handler monitors the seven interrupt request lines, and when the bus is available, it will drive the Interrupt Acknowledge line.

To ease the design of VME board level products, Signetics has recently added two new devices to its list of VME interface products—an interrupt generator (68154) and an interrupt handler (68155). The Signetics 68154 interrupt generator provides an interface between the interrupting device and the VME bus (Figure 3). The device has three primary functions: to generate bus interrupt requests, to sit in the interrupt acknowledge daisy chain and to allow a status/ID byte (interrupt vector) to be supplied to the system if needed.

The 68154 provides a vehicle for interprocessor communications on an intelligent peripheral controller board or a CPU board. Local data pins (LD1-LD7) serve as a local data bus. This allows a local master to access two internal registers of the 68154. During an interrupt acknowledge, the 68154 will allow for a status/ID byte to be supplied to the system. The 68154 supplies seven of the eight needed Status/ID bits. The user is allowed to externally supply the least significant bit (LSB), typically the system address line A1 of the Status/ID byte. The IRQ1*-IRQ7*, DTACK and BD1-BD7 outputs require external buffers to provide adequate drive to the system bus. BUFEN provides the output enable control for the data buffer that is required for BD1-BD7.

Complementing the 68154 is the 68155, an asynchronous interrupt handler. The 68155 can handle interrupts from 14 sources: seven bus interrupt requests generated on the IRQ1*-IRQ7 inputs, six local interrupt sources generated on the LRQ1*-LRQ2 inputs and one nonmaskable interrupt which may originate locally or from the system (such as the systems AC fail signal).

Interrupt handling on the Multibus II is done in a completely different way. For example, there are no signal lines on the iPSB to handle interrupt; interrupt generating and interrupt handling is under the control of each individual master in the system. When a device wants to interrupt another device, it does so by passing a message to that device. This involves arbitrating for the bus, gaining access and passing the information. Message passing is achieved through a particular address space called the message address space.

Figure 3: Signetics' 68154 interrupt generator provides an interface between an interrupting device and the VME bus.
Complete hardware support for the VME bus user.

The hardware support for a bus system based on the Eurocard form factor needs very specialized experience. BICC-VERO have that experience and our worldwide reputation is unquestionable.

Users of leading bus systems have already benefited from your expertise with such hardware products as backplanes, extender boards, prototyping boards, card frames, connectors and power supplies — and that’s just to start with.

Now we have combined all of these products into a total capability and have produced a range of Microrack Systems.

For the VME bus user BICC-VERO now offers from stock, a full range of P1 and P2 backplanes with either “on-board” or “off-board” termination and extender boards, as well as the standard products you will require to build your microprocessor system.

Telephone or write for further information on VME bus support hardware.

Whatever your system configuration, BICC-VERO have the experience and the hardware to support you.

DATA FILE
* P1 and P2 Backplanes
* Extender Boards
* Prototyping Boards
* Card Frame Systems
* Power Supplies
* Connectors

BICC-VERO ELECTRONICS INC
40 Lindeman Drive, Trumbull, Connecticut 06611 U.S.A. Tel: (203) 372 0038, Fax: 203-372-6224. FAX: 510 227 8890.

Circle 30 on Reader Inquiry Card

Leaders in Microprocessor Backplanes
In the past six months, a great deal of marketing activity and several documents have attempted to compare the VME and the Multibus II. Many have added a great deal of confusion rather than clarification to the situation. The whole issue of what the difference is between an asynchronous bus and a synchronous bus has been confused, mainly to the advantage of the VME camp.

The VME bus is an edge-sensitive asynchronous protocol whereas the Multibus II is a level-sensitive asynchronous protocol. The Multibus II technique has been named synchronous because of the presence of a central clock. The difference between the two techniques is the time window within which signals are considered valid. With the edge sensitive technique, the signal lines are always considered valid and any state transition (signal edge) will be acted upon as soon as it propagates from one board to the next. The level sensitive technique utilizes a central clock to define regular small time windows during which the signal lines are valid. This technique requires that all signals are settled and remain stable (at one level) during any valid time window. These differences are illustrated in Figure 5.

Apart from the asynchronous versus synchronous issue, the Multibus II may now be perceived as an architecture that is unsuitable for applications in real-time control systems, primarily due to its novel message passing architecture. This, however, is clearly not the case. When Intel announced its set of boards (Digital Design, February 1985, p. 24) it did so with the real-time operating system iRMX86. Furthermore, Intel actually claims that the Multibus II is faster than the VME in real-time applications. Whether this is true or not, it does appear that the two buses will compete in the same market.

References

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful .................................................. 601
Useful .......................................................... 602
Somewhat Useful ........................................... 603

Figure 4: Typical system configuration for the Signetics 68155 asynchronous interrupt handler.

Figure 5: Edge-sensitive versus level-sensitive handshake techniques (shown is block write).
“Put all your eggs in one basket and watch that basket.”

Mark Twain
Puddinhead Wilson’s Calendar

Mizar’s energy is focused on VME.

We were pioneers in VME technology... among the first to offer a VMEbus board. And, from the beginning, we’ve been convinced of the potential of VME. So convinced, in fact, that we’ve committed ourselves and our futures solely to VME. As Mark Twain advised, we’ve put all our eggs in one basket... and we’re watching that basket very carefully.

As the VMEbus market grows and expands, so does our basket of VMEbus products. Today, we have the largest, broadest line of VMEbus products in the world... from a variety of single and double height VMEbus boards to systems and software. Which means when you deal with Mizar you can select individual products or order a complete system, fully assembled and tailored to your specific needs, if you prefer.

What’s more, our vast product line is backed by a dedicated, knowledgeable, accessible staff of VMEbus experts who are committed to being the best in VME.

We’ve put all our eggs in one basket... and we’re watching that VME basket grow. We’re Mizar... the VMEbus authority.
Now there's a complete, integrated line of Multibus™ and VMEbus system enclosures that lets you match your system needs today — with the flexibility to expand or reduce your requirements in the future.

For Multibus, choose from visually-compatible 4, 7, 10, 12, and 15-slot enclosures with Multi-Cage® card cages and backplanes, all designed to meet FCC class A EMI/RFI requirements with typical systems installed. The 7-slot upright DeskMate™ and the 7-slot tabletop models have room for two half-height 5¼" peripherals, plus an additional 5¼" full height Winchester drive. All but the DeskMate are available for rack mounting.

For VMEbus, there are 5, 7 and 12-slot models, with peripherals available on the DeskMate, rack mount and tabletop 5-slot versions. All use Electronic Solutions' VMEasy™ card cage and backplane design for rugged, reliable card mounting and easy servicing. If you're into Multibus now, you can even convert your enclosures later for VME.

Talk to us about your unique requirements. Build upon the industry's most comprehensive system of Multibus and VMEbus enclosures, and reduce your lead time to market. We'll provide front or rear card loading, or special slot spacing, special power supplies, or I/O connections. See how our custom design gives you an entire enclosure line instead of a single box.

Electronic Solutions' entire line is backed by our three year limited warranty — your assurance of built-in reliability.

Call us today, and find out how Electronic Solutions can make the difference in your system packaging.
Mass memory devices fitting the 3½” form factor have emerged to fill the demands of designers who need to get the most out of every cubic centimeter.

Engineers designing systems for space-constrained applications ask a lot of their mass storage devices. Disk and tape drives for such applications must pack nearly as much data as standard-sized drives with far more recording surface area. They must use less power than standard-sized drives. They must cost less since the total cost of the final system will probably be low. They must withstand far greater thermal stress since they will be installed in a tight spot with little space for heat dissipation and, if the system is portable, they may travel from a freezing car to a warm office. And they will be expected to withstand extreme shock and vibration—even though standard-sized drives have been known to crash as a result of doors slamming several offices away.

Over the past year, the number of companies building drives to meet these demands has grown considerably. Today, a variety of flexible disk, magnetic tape and rigid disk drives are available that fit the sub-4” form factor.

Common Requirements For Portability

Sub-4” drives are increasingly being used in such portable applications as transportable computers, portable test equipment, data logging and consumer electronic devices. In addition to small size and low weight, certain requirements are common for all of these applications: resistance to shock and vibration, low power consumption, high tolerance to temperature variation.
tions and low cost.

**Physical dimensions.** Although most drives claiming to fit the 3½" footprint have the same faceplate dimensions set by Sony's (Park Ridge, NJ) current microfloppy drive—1.625" × 4"—there are exceptions. Hewlett-Packard's (Greeley, CO) Winchester follows Sony's original microfloppy footprint which was 2" × 4". Winchester drives from Rodime (Boca Raton, FL) and SyQuest (Fremont, CA) use sub-4" media, but overall drive width is larger than the Sony standard footprint because the drives were introduced before the Sony footprint was adopted as a *de facto* standard.

Some microfloppy drives are actually slimmer than the standard form factor and have larger bezels available for applications where they must fit an existing standard footprint. Finally, it is important to remember that published drive dimensions often exclude control electronics and shock mounts.

**Shock and vibration tolerance.** Resistance to shock and vibration is of particular concern for rigid disk drives operating in a transportable environment. Fortunately, merely downsizing the drives helps make them shock resistant. Short R/W head armatures are resistant to torque and vibration stress, as are the smaller platters and the drive shell.

Low mass heads and sliders are also more tolerant to shock and vibration. Plated or sputtered media resists damage during head/media contact. If oxide disks are used, a dedicated landing zone or, even better, retractable heads minimize damage.

Most transportable applications also require some form of shock mounting. Depending on the amount of isolation required, this can add considerably to the drive's dimensions since substantial sway space may be necessary for the shock mounts to function effectively.

Winchester drives vary greatly in the amount of shock mounting they require to achieve their published specs. Hewlett-Packard claims that their sub-4" Winchester drive needs no shock mounting. Others provide so much sway space that the drives may take up more room than a 5¼" Winchester (but presumably provide far more shock resistance).

Especially with Winchester, shock and vibration specifications should be viewed skeptically. "Anyone can print '40 Gs' on a spec sheet," says Alan Shugart, President of Seagate Technology (Scotts Valley, CA). "Whoever has the newest brochure has the best specs."

**Power requirements.** Power consumption is a major concern in most portable applications. Most sub-4" memory devices keep power consumption down by use of CMOS components. In addition, they inherently require less power because they use smaller disks or less tape; and the drive motors, which account for most of the power consumption, are correspondingly smaller. Tape drives draw the least power, ranging from a low of under 2W to 10W. Microfloppics require from 3W to 10W, and sub-4" Winchesters can draw up to 15W for multiplatter models.

**Thermal considerations.** While most mass storage devices can count on relatively stable operating climates, tolerance to extreme thermal changes is a necessity for sub-4" mass storage devices that travel out of the office. Read/write errors or data loss due to thermal off-tracking is the primary concern.

The solution is either to be extremely conservative at the head/media interface (writing wide and reading narrow) or to use a servo positioning system to actively keep the heads on track. The conservative approach means lower capacities because of lower data densities. The servo approach allows high densities, but also adds expense and complexity.

**Cost.** Target applications for sub-4" tape and microfloppy drives are frequently systems with a total cost of under $1500. Those using sub-4" Winchesters may cost only a little more. Therefore, there is little demand for "premium" micro drives. All of the problems associated with downsizing the drives and designing them to withstand the rigors of a mobile environment must be accomplished as cheaply as possible, with special attention given to low cost, high volume production. As a result, there is a considerable gap between what is technologically possible and what is actually available.

**Microfloppy Disk Drives**

After several years of industry wrangling, Sony's 3½" microfloppy has emerged as the industry standard. Even though the media and the drives have undergone so many refinements that today they bear little resemblance to those originally introduced by Sony, the 3½" diskette diameter remains unchanged. With the support of Hewlett-Packard, Apple and IBM, microfloppy disk drives using other sized media are destined for decreasing niche applications. Now that the dust has settled, both media and drive manufacturers can gear up for volume production, which will be essential to the success of microfloppies.

**Production Moves Off-Shore**

With the departure of Shugart from the market, Tandon (Chatsworth, CA) remains as the only large US-based manufacturer.
A fast 12.5 MHz 68000 VME SBC with 16 RAM/ROM sockets. Designed for your sophisticated control applications.

The OB68K/VME is an extremely powerful, complete stand alone microcomputer board that is functionally interfaced to the double height (6U) VME bus and is fully compatible with the VME bus standard (Rev. B) by way of the P1 connector.

**FEATURES:**
- Powerful 12.5 MHz 68000R12 16/32 Bit CPU
- 8 pairs of 28 pin sockets for ROM/RAM
  - ROM 2732, 2764, 27128 or 27256 (at least one pair required).
  - RAM 2K x 8 or 8K x 8 static
- Offboard I/O space 64K bytes (short Address Modifier code)
- (7) Prioritized-BUS or AUTO VECTORED Prioritized Interrupts (One Non-Maskable)
- (2) RS-232C Serial Ports utilizing one 68681 DUART
- (2) 8-bit Parallel I/O Ports with two control lines utilizing one 68230 PI/T
- (1) 16-bit Timer/Counter (in 68681)
- (1) 24-bit Timer/Counter (in 68230)
- System controller functions are supported. They consist of:
  1. 4-level Prioritized bus arbiter
  2. 16-MHz system clock
  3. Power-on Reset Generator
  4. Manual Reset Generator
- (1) System watch dog timer
- All System controller functions may be inhibited for Multi-Master System use if desired.

Our extensive quality control procedures give you a highly reliable product backed by Omnibyte's two year limited warranty. Software available for the OB68K/VME includes the optional VME1 BUG™ monitor/debugger and a variety of other packages. Find out more about our OB68K/VME. Write or call our Sales Department for our free data sheet or send $10.00 for a detailed technical manual. Contact our Marketing Manager, Peter Czuchra.

OMNIBYTE CORPORATION
245 W. Roosevelt Rd.
West Chicago, IL 60185-3790
(312) 231-6880
Intl. Telex: 210070 MAGEX UR
of microfloppy drives. Japan has always dominated the market based on Sony's lead. But today the entry of other large volume foreign manufacturers has all but eliminated the US. In 1984, manufacturers not based in the US accounted for 97% of all microfloppies shipped, according to Disk/Trend (Los Altos, CA), a market research firm specializing in mass memory. The completion of large microfloppy drive production facilities in Japan indicates that Japan should continue its dominance of this market for the foreseeable future.

Small Differences
The lack of distinguishing characteristics among microfloppy drives shows that standardization has finally taken hold. Designing a drive to fit a standard footprint, using a standard interface with a standard, interchangeable media, all at the lowest possible cost, doesn't leave much room for innovation. However, there are a few small exceptions.

For applications in which space is more important than a standard footprint, several microfloppy drive manufacturers build low-profile low-weight drives. JVC (Elmwood Park, NJ), Citizen (Santa Monica, CA) and others offer drives just over 1" in height (rather than the standard 1.625") and weighing a little over one lb. Where size and cost is even more critical, and capacity and interchangeability are not, Tokyo Electric Co. (Tokyo, Japan) offers a 2½" microfloppy that records up to 64 Kbytes on a single spiral track.

Citizen offers a top loading, rather than front loading, version of its microfloppy (Figure 1). And Au Peripheral Products (San Jose, CA) has a microfloppy drive that it claims offers recording characteristics superior to those of the big company drives, at a comparable price. President Sik-Kee Au, formerly with IBM, hopes to offer an alternative to the mass produced drives imported from overseas.

Microfloppy Trends
Last year, microfloppy disk drives accounted for more than 10% of all floppy disk drives sold, according to Disk/Trend. By 1987, they should account for more than 30% of all drives shipped.

Thus far, most of the microfloppies have been single-sided drives, but double-sided, 1-Mbyte microfloppies are now becoming available and will account for an increasing number of the sales. This year drives with 1.2 Mbytes of formatted capacity should be announced. The media supply is beginning to catch up to demand and should bring prices down. Low cost, readily available media will go a long way in helping microfloppies compete effectively against 5¼" minifloppy drives.

Sub-4" Tape Drives
There are a number of tape drives fitting into a sub-4" footprint. They may use minicartridge media, cassette (also known as miniature reel-to-reel) media or drive-unique media. For applications that don't require fast access times, such as data recording devices, some test equipment and very low-end computers, they may serve as primary data storage devices. However, they more commonly provide removable, back-up mass storage for Winchester drives.

Minicartridge drives. Minicartridges were developed by Hewlett-Packard 10 years ago and then licensed to 3M (St. Paul, MN). Dubbed the DC100, they were scaled-down versions of 3M's DC300 quarter-inch tape cartridge and were used extensively by HP and DEC in their intelligent terminals, small computers and test equipment. They contained 140' of 320 oersted and .15" wide tape, and capacity was under 1 Mbyte.

In 1979, Irwin-Olivetti built a 5¼" Winchester drive with a built-in DC100 drive for back up. The Irwin DC100 drive had 5 Mbytes of formatted capacity. When Irwin-Olivetti became Irwin Magnetics (Ann Arbor, MI), they left the Winchester business and focused exclusively on the DC100 tape drive.

Last summer 3M announced the DC1000, a DC100 with 185' of 550 oersted tape, which allows capacities of 10 Mbytes or more. More recently, 3M announced the DC2000, using quarter-inch tape in the same minicartridge shell, which allows capacities from 20 Mbytes to 40 Mbytes. As a result, other companies have joined Irwin in making minicartridge tape drives, and many more are eyeing the market.

Figure 3: Tallgrass Storage Devices, like Irwin Magnetics and APTEC, now offers minicartridge tape drives for OEMs. The Grasshopper currently uses 3M's DC1000 minicartridge and will accommodate the quarter-inch tape DC2000 minicartridge when it becomes available later this year. This will allow a capacity of 40 Mbytes.
THE PEOPLE WHO GIVE VMEbus WHAT IT NEEDS MOST, GIVE YOU THE MOST VMEbus MEMORIES. PLESSEY.

Plessey Microsystems makes life easy for the VMEbus designer with the most comprehensive range of VME memories in the world. All backed by Plessey's worldwide resources, technical support services and total corporate commitment to VMEbus.

Plessey VME Memories for your systems. The Plessey VME memory range includes every popular memory technology, including DRAM, ROM/EPROM and fast static RAM. As shown in the accompanying table, our capacity range spans 128 Kbytes to 3 Mbytes with EDC and 4 Mbytes with parity DRAM. Plessey VME memories are available with full 32 bit support to take advantage of the MC68020 and NS32032. So, no matter what VME route you're taking, there's a Plessey memory to take you there better.

<table>
<thead>
<tr>
<th>Plessey VMEbus MEMORIES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Capacity</td>
</tr>
<tr>
<td>4 Mbyte DRAM*</td>
</tr>
<tr>
<td>3 Mbyte DRAM*</td>
</tr>
<tr>
<td>2 Mbyte DRAM</td>
</tr>
<tr>
<td>1 Mbyte DRAM*</td>
</tr>
<tr>
<td>3/4 Mbyte DRAM</td>
</tr>
<tr>
<td>512 Kbyte DRAM</td>
</tr>
<tr>
<td>512 Kbyte EPROM</td>
</tr>
<tr>
<td>128 Kbytes SRAM</td>
</tr>
</tbody>
</table>

* with optional daughter board
+ on-board battery backup

Plessey VME: a continuing commitment. Plessey VME memories are just a part of the rapidly expanding range of Plessey VMEbus board level products which also includes single board computers; controllers, graphics and I/O boards; backplanes; power supplies; software and firmware, including languages, operating systems and drivers; and of course that famed Plessey guarantee and backup. With even more Plessey VME on the way.

For details on Plessey VME memories or our other VMEbus products and capabilities, call or write Plessey Microsystems, One Blue Hill Plaza, Pearl River, NY 10965, (914) 735-4661 or toll-free (800) 368-2738.

Or use the coupon below.

Plessey Microsystems
Circle 27 on Reader Inquiry Card
Ironically, Hewlett-Packard, who used the minicartridge extensively when there was little outside interest in it, has moved slowly away from the media and now appears ready to phase it out in favor of the standard DC300/600 quarter-inch cartridge. "They're basically stretching right now to get 10 Mbytes on a DC1000," explained Frank Carew, R&D section manager for HP's tape activities. "So our focus is on the larger cartridge. We're hesitant to commit to devices that are 20 Mbytes or less."

Meanwhile a number of companies are anything but hesitant about developing drives for the DC1000/2000 media. One reason is that the minicartridge, unlike the standard quarter-inch cartridge, is small enough to fit into a sub-4" form factor. Some companies believe it will be the ideal back-up companion for sub-4" Winchester disk drives.

In addition to Irwin Magnetics, APTEC (Columbia, MD) and Tallgrass Storage Devices (Boulder, CO) are currently offering minicartridge tape drives. And some manufacturers of DC600-based tape drives are planning to introduce minicartridge drives. Therefore, the Quarter-Inch Cartridge Working Group (QIC), a committee consisting of company representatives dedicated to developing standard recording formats and interface specifications for DC600 cartridge drives, spun off a sub-group to work out standards for DC1000/2000 drives. A standard spec would, in theory at least, allow media interchange between drives from different manufacturers. Despite Frank Carew's contention that current drives already push the capacity limits of the media, the QIC group plans on packing 40 Mbytes onto a single minicartridge.

**Cassette drives.** Another group working on a 40-Mbyte standard spec for a sub-4" form factor tape drive is D/CAS. The media is a slightly modified audio cassette, manufactured specifically for data storage use. The companies currently involved are Memtec, (Salem, NH), Raymond Engineering (Middletown, CT), Braemer (Burnsville, MN), Teac (Montebello, CA) and Verbatim (Sunnyvale, CA).

Capacity is less of a problem for cassette drives because cassettes contain about twice the recording area of a DC1000 minicartridge and about 50% more area than a DC2000. Memtec announced a 40-Mbyte 5 3/4" half-height drive two years ago and has been shipping them in quantity since last fall. The delay in a 3 1/2" form factor version is more a result of a slowly developing market than of any technical difficulties. Cassette drives would seem to be ideally suited to 3 1/2" Winchester back-up applications and media is already available from Verbatim.

**Drive-unique media.** Why would a tape drive manufacturer build a drive that uses nonstandard media? "We control our destiny because we have the design of both (drives and media)," explains Frank Gilovich, Chief Executive Officer of Interdyne (Van Nuys, CA). "The Irwins and the Memtecs are controlled by somebody else." Interdyne's 3 1/2" form factor 1DI000 (Figure 2) uses 2 1/4" reels of quarter-inch tape to store up to 20 Mbytes of data. A future version of the drive uses half-inch tape to store 40 Mbytes.

"Everyone's talking about standards," says Gilovich. "There's really only one true tape standard, and that's IBM machines that are single reel, self- threading and fixed head. And the reason it's a standard is that it's very easy to interchange." Interdyne's drive is also single reel, self-threading and fixed head and, presumably, easy to interchange. To ease OEMs' concerns about supplies of the media, Interdyne recently licensed Shape (Biddeford, ME), a leading manufacturer of video tape cassettes, to produce the Interdyne tape reel.

Entrepo (Sunnyvale, CA) also produces a small footprint tape drive with unique media. But while Interdyne looks to 40 Mbytes, Entrepo builds drives storing 256 Kbytes on a "microwafer." They plan to undercut low-end floppy drives, providing slightly less capacity and much slower access time but at a third of the price. Target applications include low-end personal computers and intelligent typewriters. OEM price of the drives is between $20 and $30.

**Sub-4" Winchesters**

Available from over a dozen manufacturers and ranging in capacity from 10 Mbytes to 50 Mbytes, sub-4" Winchester drives have finally moved from the drive designers' drawing boards to the systems designers' drawing boards. This year the results will become apparent as a new crop of personal and portable computers are announced sporting the sub-4" drives.

Most of the sub-4" Winchester makers cite ruggedness as the chief advantage of their drives, but few demonstrate it quite as graphically as Hewlett-Packard. To illustrate their 10-Mbyte drive's tolerance to shock, they attach the drive to a chain and enclose the drive in a plastic box. Potential customers are invited to pull on the chain while the drive performs data seek operations. "I think most people were impressed," says Rex James, HP's operations manager for Winchester activities.

The HP drive still on track by means of servo information interleaved in each sector, "not just a wedge servo, with information once around the track," explains James. The hard sputtered media, which HP makes itself at its Boise, ID factory, coupled with light minicomputer-like R/W heads, prevents damage to the recording surface.

HP offers just a mechanics-only drive. They chose not to incorporate a standard ST506 interface, and the drive has a transfer rate of 4 Mbits/sec, rather than the ST506 standard 5 Mbits/sec rate. Their target customers must be willing to build their own controllers, or buy them from a third party. Adaptec has worked with HP to develop a SCSI controller for the drive.

"We're talking to a number of people who are willing to design their own controllers with unique interfaces on their internal buses, and for them the ST506 interface is not a prerequisite," says James. "Quite frankly, there are other people that we have talked to that would very much like to have a 506," he adds, "and, we aren't providing that."

Avoiding the ST506 interface makes the drive family easier to upgrade and, ultimately, allows systems integrators to develop a less costly mass storage subsystem, according to James. "We left the interface on the Winchester such that it did not require a microprocessor on board... Then a high level controller
Designing new equipment that features thermal printing? Work with us.

Not only can we keep things quiet, chances are we've already solved some of your design problems on paper. Appleton Thermal Paper, of course.

As leaders in thermal paper research, our chemists have developed a wide range of thermal paper grades with various temperature sensitivities. In fact, the design problems you're seeing on paper might be eliminated by using one of our papers.

So, if your new model hasn't left the drawing board yet, work with us. We can keep your project as quiet as the paper it uses.

Circle 23 on Reader Inquiry Card
No Other Controller
Now Available Interfaces
5-Channel PTD
Disk Drives
for Real-Time Digital Video Imaging...

CONCEPT 21

This is the only PTD (Parallel Transfer Disk) Disk Processor that's now available so you can control FUJITSU Model M2350A (or equivalent) Disk Drives for use in image processing, digital film animation, flight simulation, seismic recording or medical imaging applications.

Here's a brief outline of the capabilities CONCEPT 21 offers:

• 9.3 Mbyte/second transfer rates for storage and retrieval of 512 x 512 x 8 bit images at 30 frames/second
• 16 and 24 Mbytes/second and higher data transfer rates can be achieved by parallel configurations
• 1.9 gigabytes total storage using four M2350A Disk Drives
• 16-bit parallel high speed imaging bus
• Error Correcting Code and Cycle Redundancy Check

Call For Details.

STORAGE CONCEPTS
3198-G Airport Loop Dr, Costa Mesa, CA 92626
Phone: (714) 557-1862 • TWX 910-595-1597

SYSTEMS ARCHITECTURE

could be used, for instance SCSI, which uses a single microprocessor and controls both the interface and the drive itself, therefore, providing a lower system integration cost."

Upgradability was also a key reason to avoid the ST506 interface. "As we develop future drives," explains James, "...that will improve capacities from 10 to 20 to 40 to 80 Mbytes, we can stay with that same high level controller and not have to redesign that interface in the system."

Newbury Data (Staines, Middlesex, England; Woburn, MA) has a somewhat different approach with its 3½" Penny drive. It stores 50 MBytes, unformatted, on four plated disks and has an average access time of 40 msecs. Aimed at less sophisticated OEMs, the drive uses a standard ST506 interface. Newbury Data also offers mounting kits for installing the drive into a half-height or a full-height 5½" Winchester footprint. In all, Newbury Data has done everything to make their drive easy to integrate with a minimum of effort.

Drives from the major domestic Winchester manufacturers also use the ST506 interface, but have far lower performance and capacity than the Newbury drive. Seagate, Tandon, Miniscribe and others all offer low cost drives targeted at the high volume needs of the major OEMs.

Although they historically haven't competed effectively in the small Winchester market, Japanese drive manufacturers also are looking at the 3½" market. Hitachi (Torrance, CA) and Nippon Peripherals (Kanagawaken, Japan) have already introduced competitive products into the US market; NEC (Boxborough, MA) and others will join them soon. Bruce Thatcher, Director of Marketing for NEC Information Systems' Peripheral Products division, predicts that beginning in 1986, the 5½" market will slowly decline to a million units annually, and 3½" disks will rise to 2.75 million units annually. In addition, he forecasts that OEM prices for 3½" drives will drop steadily during this period—to $180 from $380.

Micro-Memory Outlook

For all types of sub-4" mass storage products, the next year looks good for systems designers and difficult for drive designers. Many drive manufacturers—both foreign and domestic—see the sub-4" drive market as crucial to their future. They are determined to establish themselves in the market, no matter what it takes. This is already resulting in price wars in a market that isn't yet big enough to fight over.

For systems designers, this means drives at low prices, from multiple sources. However, the continued existence of those multiple sources depends on how quickly the market for sub-4" drives develops. And any development will depend on the ingenuity of the systems designers and their ability to exploit sub-4" drives in the next generation of personal computers, portable computers, subsystems, test equipment and other applications that require a lot of memory in a little space.

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful ........................................... 607
Useful .................................................. 608
Somewhat Useful ..................................... 609
DEFLECTION

AMPLIFIERS

FEATURES

Powerful: To 20 amps, 60 volts
Fast! To 6\(\mu\)s scan & retrace
Wide Bandwidth: dc coupled up to 4MHz
Stable: To 10\(\mu\)A/°C drift
Accurate: To 0.001% linearity

SPECIFICATIONS

APPLICATIONS:

CRT Projection Displays
ATC Radar Displays
CRT Flight Simulators
CRT Test & Measurement

Film Recording Systems
Flying Spot Scanners
E-Beam Welding
E-Beam Lithography

MODEL NO.

DA-PP1
DA-PP2N-7
DA-PP4N-7
DA-0420
RDA-1220-S86 (Lab Standard)
RDA-1220-S86C (Water Cooled)
DA-PP2N-5
DA-PP4N-5
DA-PP8N-5
RDA-1635
RDA-1255
RDA-0660
RDA-0960
RDA-1260 (Lab Standard)
RDA-1660 (Lab Standard)
RDA-2060

OUTPUT RANGE

2 amps, 20 volts
4 amps, 20 volts
8 amps, 20 volts
4 amps, 20 volts
12 amps, 20 volts
12 amps, 20 volts
4 amps, 35 volts
8 amps, 35 volts
16 amps, 35 volts
16 amps, 35 volts
12 amps, 55 volts
6 amps, 60 volts
9 amps, 60 volts
12 amps, 60 volts
16 amps, 60 volts
20 amps, 60 volts

For complete details circle reader service number or call CELCO today with your CRT display requirements.
DSP Systems' fixed point, Digital Signal Processing boards provide cost effective array and FFT processing because they contain all the functions you need on either one or two boards. Furthermore, your design costs are minimized by easy-to-use instructions that control execution of signal processing functions. As a result, your overall costs can be as much as 90% less than other systems with similar capability.

Use of high speed, low power VLSI lowers your power requirements and equipment size by as much as 90%, compared to older generation array processors.

A new addition to our product line, the Multibus A/D Converter (MAD), contains a dual-ported, dual-buffered RAM that can provide DMA data at a 2 megawords/sec rate.

And, for those who want to customize microcode, there are Multibus (MAP-DS) and VMEbus (VAP-DS) development systems whose cross-assemblers employ quasi-English, "user-friendly" commands that simplify the addition of macroinstructions.

Compared to other signal processors of similar performance, DSP Systems' boards offer the lowest cost per function, per unit time, in a fraction of the size.

All FFT and array processor boards include: 50 KHz real time processing analog bandwidth, on-board HAMMING weighting and built-in self-test.

**FFTIB FFT PROCESSOR**
- Multibus-compatible
- 12 Easy-to-use Instructions
- Single-board FFT
- Up to 12 Mega OPS
- 8.6 msec for 1024-PT FFT (Complex)
- FFT/IFFT and Power Magnitude Instructions

**AP-4 MINI-ARRAY PROCESSOR**
- Multibus-compatible
- 16+ Easy-to-use Instructions
- Single-board Array Processor
- Up to 12 Mega OPS
- 8.5 msec for 1024-PT FFT (Complex)
- Peak Pick Instruction
- On-board DMA
- Optional Block Floating Point

**VAP-64 MINI-ARRAY PROCESSOR**
- VMEbus-compatible (16 Bits)
- 21+ Easy-to-use Instructions
- Two-board Array Processor
- Up to 10 Mega OPS
- 10.3 msec for 1024-PT FFT (Complex)
- Up to 64K Dual-Port RAM
- Complex Demodulation
- On-board DMA
- FIR Filter and Peak Pick
- Block Floating Point

**MAD-12 MULTIBUS A/D CONVERTER**
- Multibus-compatible
- Dual-port, Dual-buffered 4K RAM
- On-board Anti-alias Filter
- Supports High Speed DMA
- 25 KHz to 500 KHz Sample Rate
- 12 Bits Resolution
Driven by user demands for faster, smaller, more capable and less expensive computer graphic systems, semiconductor manufacturers are introducing chips that provide rapid bit-mapped medium to high resolution displays. Until recently, the low resolution home/game computer market was the primary volume market for chips aimed at graphics. User demands for greater performance have spurred the development of several graphics chips. These products not only work faster, but also offer new architecture schemes for graphics display.

The ICs attempt to address two fundamental issues: speed and functionality. Before the introduction of these chips, designers faced tight architectural constraints. The host CPU was required to control and to execute complex graphics functions while also being responsible for memory control. The new ICs free the host CPU from graphics functions and avoid memory contention problems. The result is much faster graphics systems capable of true graphics interactivity.

Technological developments are not the only factor in the increasing quality of graphics systems. Dropping memory costs and availability of high quality, inexpensive RGB monitors are also contributing factors. Monitors with resolutions of over 1024 x 1024 pixels previously were expensive and poor quality. Now there are more manufacturers, and many offer display resolutions of over 2000 x 2000.

Users now expect such features as zoom, pan and color to be standard. New features are being requested such as display list memory, fast block moves, raster ops, large and available video space and simultaneous multiple plane addressability. With resolutions of over 512 x 512 pixels and multiple bit planes, implementing these functions using generic components presents very serious technical problems.

A major problem with graphics architecture is the video refresh rate. The video refresh controller must supply data to the video output hardware where the pixel display time is less than the memory cycle time in video output hardware. Video refresh rate is closely tied to memory bandwidth. The use of faster memory chips solves the problem but means higher component costs. The next problem is the ability to read, modify and write to display memory without contention problems or update speed loss. Demanding applications increase the architectural problems in today's graphics systems.
Memory

Memory has been and still is the key issue in graphics systems. Memory used for graphics applications is different than conventional computer memory. The issue is not just one of speed, cost and size, but how the memory is used architecturally. The memory organization controls performance through such factors as the relationship of memory speed to display update/refresh bandwidth, memory size, organization and overhead requirements. Despite the declining cost of memory over the last few years, price, as well as availability and organization of memory, is still a critical issue.

A fundamental problem in bit-mapped displays is that pixel generation occurs during refresh requiring a high memory bandwidth. Memory bandwidths of 100 MHz or more are common in medium to high resolution systems and at this rate, bandwidth requirements are too high even for static RAMs. The problem is further compounded at higher resolution. External buffering, blanking (flash mode) or unusual retrace periods also burden bandwidth.

Novel schemes have been devised for graphics applications to help solve some of the problems. Some of the solutions are based on standard DRAMs with special fast cycles. Innos (Colorado Springs, CO), for example, integrates a CAS before RAS into their line of 64K DRAMs. Texas Instruments’ (Dallas, TX) new 256K DRAM family can employ the CAS before RAS. RAS only refresh or hidden refresh cycling. Other solutions rely on video bus exchanges, bus arbitration or cycle stealing. Fast static RAMs are sometimes used as a solution in spite of their expense. The Metheus (Hillsboro, OR) 2500 series of display controllers, for example, uses 70 nsec static RAMs for display memory. Another alternative is double buffering where two separate display planes are used, one for display and the other for writing. However, this scheme means the cost of twice the display memory.

Approaches such as nibble mode and static column addressing are sometimes used. Static column decoding is an access mode that eases the raster display bandwidth problem by providing high speed access to a serial bit stream. The fast access also allows cycle stealing so that a pixel processor can “steal” random update cycles during display time as well as during blanking intervals. Static column addressing used with an optimized memory technique called symmetrical cell addressing allows better update performance. Symmetrical addressing assigns a rectangular area of the screen to the same row address, rather than organizing the RAM row addresses along scan lines.

TI introduced a memory chip last year called a Video RAM, or VRAM (Figure 1). The TMS4161 is unique because it was specifically designed for graphics applications. The dual-ported nature of the TMS4161 allows a graphics processor to control the DRAM portion of the device. Pixel data for refresh display is provided through the use of an on-board 256-bit shift register. The combination of shift register and 64K × 1 RAM significantly reduces costs and parts count while supporting pixel clock rates from 5 to 150 MHz. TI claims that using the chip in a 1K × 1K black and white system would reduce parts count by 72 chips (48 memory and 24 logic) using 16K × 1 chips. Chip reduction using 16K × 4 chips would be 24 chips.

An application note from TI describes a 640 × 480 display where five devices per pixel plane are used. One approach uses external parallel to serial registers for each plane, whereas another approach uses the 256-bit serial shift register to link the ICs of each plane together. Use of the TMS4161 allows almost 100% access to the display memory for updating. An additional use of the 256-bit shift register is the clearing of a display. Loading the VRAM’s memory with 256 0s and loading them into the shift register erases a complete screen image in only 255 cycles.

As a result of the popularity of the concept of on-board shift registers for VRAMs, several memory manufacturers have announced plans to introduce their own versions soon. The TI unit will probably have variations, such as a decrease in the number of tap lines in the shift register.

Although it may seem better to use larger memories such as the 256K × 1, they also have bandwidth problems. 256K × 1 DRAMs can store a 1024 × 1024 pixel display, but all the data cannot be accessed from them in time to support the dot rate of 12 nsec. Thus, graphics designers prefer nibble mode where data can be read in ×4 increments.

An additional, but often overlooked, aspect of graphics architecture is the power supply for the massive amount of RAM. Although static RAMs use more power than dynamic RAMs, dynamic RAMs must be refreshed. The amount of inrush current required to refresh Mbytes of memory can easily cause a strain on marginal power supplies and can cause the display system to oscillate audibly.

Many manufacturers have developed parts that reduce power consumption while increasing speed. A 35 nsec 16K × 4 static RAM from Lattice Semiconductor (Portland, OR) consumes only 100 mA during its active state. NEC (Mountain View, CA) has developed a memory chip that is able to hold the entire contents of a video display. The μPD41221 DRAM uses a 75 nsec serial access scheme to store 320 rows of 700 columns (224,000 bits). Because of its unusual organization, the memory requires 320 refresh cycles every 2 msec. This refresh rate allows from 1 to 700 bits to be shifted in a single scan period. Additionally, it has a counter which can be set, reset, incremented and decremented.

VLSI Graphics Display Controllers

Ever since the introduction of the 7220 from NEC in 1981, graphics display controllers have made a major impact in the...
ASTRO HAS DESIGNS ON YOUR MONITOR, NOT JUST A PRETTY PICTURE

ASTRO DESIGN Inc. is the leading supplier of programmable video signal generators and other graphics related equipment and systems such as image processors and graphics processors. Most American and Japanese CRT monitor manufacturers and a number of European manufacturers are using our products to test, evaluate, and demonstrate their products efficiently and effectively. Satisfied customers — all.

Some of the patterns that can be generated are:
- Character patterns
- Gray-scale patterns
- Color-bar patterns
- Center marker, edge and corner markers, etc., etc.
- Circular patterns
- Dot patterns
- Cross-hatch patterns
- Window patterning functions

This is a sample display frame generated using the VG-807A. It shows the superimposition of circular patterns, cross-hatches, horizontal color bars, vertical gray-scale patterns, a center marker, and six windows on a gray background plane.

THE VG-807A PROGRAMMABLE VIDEO SIGNAL GENERATOR.

The ultimate in programmable video signal generation is here. The VG-807A Programmable Video Signal Generator lets you generate virtually infinite varieties of video signals for testing, adjustment, evaluation, and demonstration of your video display/output devices — from commercial CRTs to the latest in super-high resolution CRT monitors, laser printers, etc.

FEATURES

THE VG-807A FULLY PROGRAMMABLE: Press a few keys and you get a new video signal tailored to your own needs. All timing parameters can be programmed. All outputs can be controlled. All patterns and colors can be combined at ANY frequency.

USER ROM FOR INSTANT LOADING OF PROGRAMMING DATA: The programming data for over 100 signal formats can be loaded in the form of a preprogrammed 8K byte ROM inserted in the user ROM socket.

SIMPLE TO OPERATE, EASY TO USE: A large, easy-to-read 20-character by 2-line fluorescent alphanumeric display guides the operator in a simple conversational mode.

LARGE VARIETY OF OUTPUT SIGNALS: All types of video signals are output separately.

VIDEO OUTPUTS:

SYNC OUTPUTS: H-Sync, V-Sync, H-Drive, V-Drive, and composite Sync.

SUPER-HIGH RESOLUTION: Signals for super-high resolution monitors can be generated with H-Sync frequencies up to 200 kHz and dot clock frequencies from 5 to 160 MHz.
- H-Sync periods: 5.00 µs ~ 81.92 µs in 20 ns steps.
- V-Sync periods: 100 H ~ 4000 H in 1H steps.

SUPERB PATTERN GENERATION FUNCTIONS:
- The most complex of patterns can be generated with utmost ease due to the use of the following four basic planes in addition to windowing functions that allow flexible operations on window areas selected anywhere in the display area.
  - Graphic plane: 2048 × 2048 dots giving high resolution.
  - Color bar plane: Freely selectable width, color combination, and intensity.
  - Gray-scale plane: Gray-scales with up to 127 levels can be displayed with freely programmable bar width and initial intensity.
  - Background plane: The intensity and color of the background plane can be set as required.

YOUR IMAGES ARE OUR BUSINESS

Call or write TEAM SYSTEMS for more information or application assistance.

Test & Measurement Systems, Inc.
349 Cobalt Way, Suite 301
Sunnyvale, CA 94086
Tel: (408) 720-8877/78/79.

ASTRO DESIGN Inc.
graphics market. Over 40 companies depended on the 7220 for their graphics display systems last year. The 7220 is second sourced by such major firms as Intel, with its 82720, and Thompson-EFCIS, with its 9367. The success of the 7220 confirms the validity of using a VLSI chip to centralize and to control graphics functions.

Some of the target goals of the next generation of display controllers are implementations of graphics standards, use of the 16 basic logical operators (AND, XOR), raster operations, programmable transparencies of the background, windows with management and high speed control of pixel data to and from the frame buffer. Several IC manufacturers are presently developing products that will support many of these functions.

A chip set from NCR (Colorado Springs, CO) and a set from Hitachi (Tarrytown, NY) represent the second generation of graphics controllers. The NCR 7300 Color Graphics Controller (CGC) works with the 7301 Memory Interface Controller (MIC) to form the basic blocks of an intelligent graphics system (Figure 2). Central to the performance of the chip set is the ability to translate high level graphics commands into machine language instructions. Additionally, the set can perform fast block transfers with raster ops, such as read-modify-write, being executed during display transfer. Memory management, DMA, cursor control, internal color look up table and analog RGB outputs are provided in the 7300, allowing display of 256 simultaneous colors. The system is designed to incorporate such graphics standards as CORE, GKS and NAPLPS. The architecture helps programmers by providing control of the memory refresh, window management and soft font text generation.

The Raster Memory Controller (RMC) and the Raster Memory Interface Controller (RMI), both from Motorola (Phoenix, AZ), have features that are intended for low-cost systems. The chip set can display 320 × 210 pixels with 16 displayable colors in the NTSC format. The RMC can display eight sprites (bit-mapped blocks) and can provide smooth scrolling, alphanumerics and memory control.

The Advanced CRT Controller (ACRTC) from Hitachi performs such advanced graphics functions as drawing of primitives, split screens and windows, clipping and X-Y addressing (Figure 3). The X-Y addressing must be computed by the processor for each pixel using other architectures; this takes up valuable time. The 8 MHz unit can draw up to 2 million pixels per second. The controller is comprised primarily of three processors: the drawing, the display and the timing processors. Other functional blocks such as the CPU interface, DMA and interrupt controller and CRT interface constitute the support circuitry. The drawing processor interprets commands into the physical pixel addresses. The display processor controls the screen format and display parameters for driving the display. The timing processor controls the internal timing in the chip, as well as the correct timing for the display. The chip is unusual because it has independent 8-bit read and write FIFOs for transferring main memory to display memory. This lessens bus traffic contention during data transfer and increases speed.

A recent trend is the use of chips that provide specialized functions. For example, the new TMS32020 chip from TI is designed for signal processing and is excellent for specific arithmetic problems. The TMS32020 supports 3D rotation which requires scalar-to-vector conversion in real time. Normally this floating point calculation is done on the host microprocessor.

The architectures of the latest graphics controller chips make it clear that the industry is supporting bit-mapped displays rather than table-look-up graphics and text. Bit-mapped displays represent exactly what is in memory on the display.

**CPU Vs. Bit-Slice**

A major influence on the speed of graphics systems has been the implementation of bit-slice architectures. The ability to efficiently microcode wide-word architecture outweighs the problems encountered in programming unusual and untested code. Programming time is much longer with microcode than with conventional languages having good support tools. Raster Technologies has taken the bit-slice approach, as has Metheus. They use the AMD 2900 series of bit-slice chips and support circuitry. In addition to using bit-slice technology, both companies use generic microprocessors such as the 68000 and Z80 for general I/O management.

Qubix (San Jose, CA), the manufacturer of a computerized technical publishing system, chose to use a distributed function architecture consisting of multiple 68010s for their 2240 × 1680 × 1 pixel display. Using dual-ported RAMs, the 64K × 64 bit-bit-mapped system runs at a clock rate of 155 MHz. By scanning in 64-bit raster words, the system operates on only 1/64 of the clock rate, which is about 2.2 MHz.

Parallax (Sunnyvale, CA) uses a different approach. The bit-slice architecture is not implemented by commercially available bit-slice CPUs but through the use of discrete TTL. The versatility gained by this architecture on their 1000 Series of board level products allows a drawing speed of 88 million pixels per second at a resolution of 1024 × 768 pixels, 60 Hz, noninterlaced. The vector draw rate is 1 million pixels per second. Use of Programmable Logic Arrays (PLAs) and simulation before construction makes the design efficient and well tested.

Several companies are now using AMD's newer 29116 series of bit-slice devices. The 29116 combined with the AMD 29516/517 16 × 16-bit multiplier makes possible multiple intensive rotation algorithms in 65 nsec per multiply.

**Going Custom**

The problems encountered in determining what to load in the bit map has led several system architects to seek alternatives to
In the past 20 years, we’ve helped a lot of people — from all areas of electro-optical imaging — go dry. We’ve simply convinced them, with 3M Dry Silver Papers and Films, that dry is definitely better. That it’s faster, cleaner and more economical than conventional wet-processed materials.

Working with OEM's, our product improvements have helped the imaging industry make giant strides in hardcopy system design, with fresh ideas and new solutions to problems. For a wide range of imaging applications requiring photographic quality with dry instant processing, 3M Dry Silver continues to be the answer.

So it’s no wonder the electronic imaging world is going dry. And now there are more reasons why you should, too: 3M's new generation of high performance Dry Silver Papers and Films. You'll get fast, permanent hardcopies of your data that are sharper, cleaner and easier to process than before. Here's why:

**Spectral sensitivity from UV to IR**

The 3M Dry Silver process uses photo-sensitive compounds which can now be tailored to obtain desired spectral sensitivity, from roomlight handling ultraviolet sensitive materials to infrared sensitive materials suitable for use with IR semiconductor lasers.

**Photographic resolution and quality**

3M Dry Silver Papers and Films offer photographic quality similar to wet-process materials. Plus they’re faster and more economical. Resolution in excess of 150 line pairs/mm is possible with our papers and 300 line pairs/mm for films.

**Increased sensitivity**

Significant increases in sensitivity over our previous materials are now a reality. If faster writing rates or low energy light sources are problems, this improvement may be your answer.

**Faster, totally dry processing**

New processing techniques and systems have increased the quality and access time associated with dry processing. We now offer our processing know-how, OEM sub-assemblies and finished units to OEM's and end-users interested in going dry.

Don't be content to watch your world go dry around you. Find out how you can too. Contact us today!

**Imaging Products**

**Imaging Systems Division 3M**

223-25N, 3M Center

St. Paul, MN 55144

3M hears you...

Circle 65 on Reader Inquiry Card
relying on a host CPU or commercially available products. Sun Microsystems (Mountain View, CA) incorporates the concept of RasterOps which allows rectangular areas of raster display data to be modified according to a preselected operation. This concept grew from the early days of Smalltalk and was implemented on the Xerox Alto computer as BitBlt, for Bit Boundary Block Transfer. The function is now implemented on a custom VLSI chip created by a silicon compiler. The design of the chip at Silicon Compilers (Los Gatos, CA) took only five months and replaces about 80 TTL packages. The chip uses a 16-bit data path and can handle 256 functions, including all bitshifts and bitmasks. It is now manufactured and sold by VLSI Technology (San Jose, CA).

Xtar (Elk Grove Village, IL) offers a two-chip set that computes the pixel-by-pixel calculations for drawing into the frame buffer quickly. The Graphics Microprocessor (GMP) is a 16-bit processor designed to work with the Video Shift Register (VSR), which controls 16K x 4 DRAMs. Xtar claims the GMP/VSR combination can display 168 million pixels/sec. The key to this speed is the internal architecture that allows filling of polygons during a single memory cycle. Segments of 64 or more pixels can be drawn at about 5 nsec per pixel.

Weitek (Sunnyvale, CA) has focused on the high end of computer graphics architecture by providing a fast floating point chip and two specialized chips aimed at solid modeling applications. Called the tiling engine and transformation processor, the ICs are only available on a Multibus board set. The boards allow high-level equations that describe a parametric cube patch and display the image at 100,000 3D points per second. These ICs facilitate the computation-intensive transformation process.

The floating point chip has found its way into many high-end systems, such as the One/380 from Raster Technologies, a manufacturer of high end graphics display controllers. The Weitek chips were also chosen for Sun Microsystems's newest color graphics display.

Faced with the traditional set of graphics architectural problems, Mindset (Sunnyvale, CA) chose to use a full-custom graphics coprocessor chip set. Consisting of a graphics coprocessor chip and a display processor chip, the set produces display resolution of 320 x 200 at 16 colors from a 512 color palette. The chip set can produce eight different bitblt operations that are Basic operations or set by a series of masks.

Also relying on the capabilities of dedicated, custom VLSI, Silicon Graphics (Mountain View, CA) addressed the most basic problem with displaying complex images: numeric computation. Using 10 to 12 Geometry Engines provides 32-bit floating point calculations for real-time 3D display. A newer Geometry Accelerator assists the Geometry Engines by buffering data for maximum system throughput and converting user's data into floating point format. This addition to the original architecture has increased speed of display by 10 times.

Lexidata (Billerica, MA) uses a custom gate array to integrate video shift registers for their 60 Hz, noninterlaced graphics controller system. Fifteen thousand gates were implemented to provide a mixture of TTL and ECL for I/O. The video shift register gate array allows an eight plane, 1280 x 1024 resolution memory and display system to be put on one PC board. The gate array provides 80 bits of high speed latches, a 20-bit shift register to make the beginning of a video pipeline and a 20:1 multiplexer for pixel read back. For eight planes of memory, four arrays are required. The part has low enough gate delays to provide the 112 MHz operation.

**Adding Glue**

Glue chips, common to all architectures, can be a major cost factor and source of potential problems. Too many generic TTL ICs for support of VLSI or special functions can change the cost of a system, making it unprofitable. This is a serious consideration in all graphics systems. One solution is the use of PLAs. Raster Technologies uses a CMOS 750 gate array replacing a 15 sq. in. board. Cost savings such as this are important, as is increased reliability, especially for a system that uses a dot clock of over 100 MHz.

TI has a solution that effectively uses their 4161 VRAMs. The Video System Controller (VSC) is a single chip that replaces the additional circuitry that is usually required for memory support and control in display systems. The VSC provides for DRAM refresh and CRT control; it is programmable, allowing different horizontal and vertical intervals, interlacing control and external sync. The VSC supports resolutions up to 4K x 4K. The combination of the VSC plus VRAM provides a solution to the basic problem of accessing video memory for data modification during display. The approach TI is taking departs from the graphics controller tack. The use of the VSC/VRAM is designed to access and modify memory of the bit map in contrast to pre-processing the data for display.

There is another serious architectural consideration basic to all graphics systems. After the graphics data is created in memory, it must be driven as an output to the display system. This has posed problems in the past as the bandwidth has gone beyond 100 MHz. The components that presented a major block a few years ago were the digital-to-analog converters. In the last
At last. Someone has taken the pain out of image processing. Imaging Technology now offers low-cost, easy-to-use, interactive software that makes the most of its popular and powerful PCVISION™ Frame Grabber.

Now professionals in any field can perform sophisticated image processing operations using their personal computers. Radiologists can enhance X-ray images; astronomers can find new stars; microbiologists can explore intracellular space; educators can teach the world to see. What can you do? Imagine the possibilities.

The PCVISION Frame Grabber fits into any empty slot in your IBM, PC, XT, or AT (or 100% compatible). It features 8-bit digitization, input and output look-up tables, and 512x512x8-bit (256K bytes) onboard frame memory, not to mention RGB or pseudocolor output. All the raw power you need for your application.

**ImageAction™** is our new menu-driven image processing software package. Over 80 functions — arithmetic, geometric, convolutions, and more — are available at the touch of a mouse button. OEMs and system integrators can use ImageAction to test concepts and procedures, then implement products with ITEX/PC, a callable library of ImageAction subroutines.

No complicated installation. No programming. No debugging. No waiting. No pain. Image processing at your fingertips.

For more information about these products or our complete line of Multibus®- and Q-Bus™- compatible image processing modules, call our Sales Department at (617) 938-8444 or write to the address below. Dealer inquiries are also invited.

Imaging Technology Inc. 600 West Cummings Park/Woburn, MA 01801/(617) 938-8444/Telex: 948263

PCVISION, ImageAction, Imaging, and the Imaging logo are trademarks of Imaging Technology Incorporated. Multibus is registered trademark of Intel Corporation. Q-Bus is a trademark of Digital Equipment Corporation.
two years or so, several vendors have created components that are directly targeted at graphics systems.

One problem with graphics architecture was the conversion of TTL signals to high speed ECL. Using a combination of monolithic and hybrid technology, Analogic (Wakefield, MA) created an 8-bit, 150 MHz D/A converters that converts the TTL signal to ECL internally and drives a 75 Ohm monitor. Monolithic D/A converters are available with 8-bit precision at conversion rates of 125 MHz from TRW (La Jolla, CA). To further ease system integration, Intech (Santa Clara, CA) offers a D/A converters in a hybrid package that accepts all three RGB inputs and includes a 256 x 8 color look-up-table with an update rate of 100 MHz. The importance of these components rests in the fact that analog circuitry is very difficult to manage at high clock rates and without analog expertise. A well-thought-out architecture can be executed poorly with disastrous results.

Comparing Architectures

With the flurry of activity in graphics design, two fundamental directions of the architecture exist: incorporating graphics intelligence and functions on VLSI and controlling the video memory better. The goal of incorporating graphics intelligence and functions on VLSI is to use a chip smart enough to execute high level commands, to control video memory and to control the display functions. With video memory control, the goal is to optimize the memory so that a processor can read-modify-write without interrupting the display. This means control of the graphics functions can be incorporated easily by the processor, window memory or multiple memory planes. With the use of host-based intelligence and with control of easily accessible video memory, greater versatility can be achieved.

While both alternatives acknowledge the importance of the VRAM, controversy still exists regarding the display controller route. Proponents of the VRAM approach claim that the support circuitry of the VLSI approach is expensive, constrained and takes up too much board area. Proponents of the VLSI approach argue that software is a key issue, and the implementation of software into hardware is faster, more efficient and easier.

A difficulty in comparing graphics architectures or systems stems from nonuniform benchmarks. Many vendors highlight specifications that are somewhat true, but in practice seldom achieved. The fill rate is a common example where the specifications are made under optimum conditions. Without regard to setup times and word size, the figures are meaningless. It is clear that a common benchmark is needed where the coordinates (floating point or 32-bit), polygon number and size are specified. Until a standard is accepted, buyers will be confused and the game of "specmanship" will hinder the growth of the graphics industry.

The demands of users of computer graphics systems are fueling the competition for better, faster and less expensive systems. It will not be long before systems that are truly interactive and answer the needs of end users are available.

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful ........................................ 610
Useful ................................................ 611
Somewhat Useful .................................. 612
**INTRODUCING THE D 256 VISION DEVELOPMENT SYSTEM.**

Name your vision application need: Quality Assurance, Process Control, OCR Applications, Classification and Sorting, Machine Monitoring and Safety, Material Handling, PCB Inspection, Image Processing, Keyboard Inspection, Robot Guidance, or Educational Applications.

Now you can develop the vision programs you need with The D 256 Vision Development System from IRI. The D 256 is a stand-alone system based upon the new world standard multi-user program development environment: UNIX, and IRI's unique Iconic Kernel System (IKS®). The IKS is a software package that provides a comprehensive set of over 300 software modules which can be used as vision software "building-blocks," for your application development. This means that now you can develop programs on the D 256 which can operate on the D 256 or on any IRI P 256 Target System—the vision price/performance leader for inspection and other industrial applications.

If you're considering developing computer vision systems for your applications, look to the D 256 Vision Development System from IRI. And, our worthwhile line of options including color input and output. The IRI D 256 user-friendly programming systems are now operating at major corporate research labs in the U.S., Europe and Japan. Get in touch. We'll be happy to show you ways to develop your vision. For a demonstration, more information, or a direct quote, call: Richard Carroll, V.P. Sales (619) 438-4424.

International Robomation/Intelligence
2211 Las Palmas Drive, Carlsbad, CA 92008

THE BEST VISION INDUSTRY HAS EVER SEEN.
Circle 63 on Reader Inquiry Card
Introducing the Aptec 2400 I/O Computer – a new class of computer that can increase the throughput of VAX-based systems as much as 40X. Simply. And economically.

By eliminating the I/O bottlenecks that limit performance, the Aptec I/O Computer makes your peripherals work faster and more efficiently. Including disks and tapes, APs, graphics/image processors, and special purpose devices.

It lets you achieve true supercomputer performance with any VAX by allowing efficient integration of multiple array processors.

And, the Aptec I/O Computer permits dramatic new levels of performance in real-time data acquisition and analysis.

Not since the array processor has any development done so much to boost the performance of minicomputer systems.

Here's how it works: The Aptec I/O Computer creates an independent, 24 MB/sec, FILES-11 I/O environment that allows VAX-shared peripherals to transfer data at full speed, free from VAX bandwidth limitations.

From 1 to 200 MB of high speed memory is directly accessible by your attached peripherals and VAX.

And, the Aptec I/O Computer provides the intelligence to control peripherals, data transfers and peripheral computations—with minimal involvement of the VAX CPU, the VMS operating system or the Unibus.

Peripheral operations become more efficient. Attached processors work at peak efficiency. And your VAX is free to provide better service to your on-line users.

Learn how the Aptec 2400 I/O Computer can unleash the performance potential of your VAX system. For the complete story on this exciting new class of computer, write or call Aptec today.

The Aptec I/O Computer will unleash the performance potential of your VAX.

Aptec Computer Systems, Inc.
10180 SW Nimbus Ave.
Portland, OR 97223
(503) 620-9840
Telex 467167

VAX, Unibus and FILES-11 are registered trademarks of Digital Equipment Corp.
©Copyright 1985 Aptec Computer Systems, Inc.
Peripheral I/O Processor Speeds VAX Performance

by H.D. Meitzen and Delbert L. Taylor, Information Products Systems, Inc.

Computer systems for seismic processing, signal processing in data communications, real-time graphics and high-resolution scanning in medicine handle massive amounts of data. In geophysical exploration, for example, raw seismic data is collected on magnetic tape in contiguous records typically 1 Mbyte and up. The full digital file of acoustic measurements recorded in one test shot amounts to about 6 Mbytes today and is expected to reach 65 Mbytes within a few years — and even a small ground survey can easily require 5,000 shots.

The optimum computer system for work like this combines a multiuser interactive environment for controlling data processing with an I/O subsystem that permits peripheral devices to exchange data at very high speeds with minimal attention from the host. In off-line seismic systems, it becomes feasible to process very large files very quickly. In on-line applications, such as graphics and communications, large amounts of data can be processed in real time. In a multiuser environment, concurrent operation of two or more independent seismic processing terminals or graphics workstations enhances the productivity of both users and computer resources.

The multiuser interactive environment needed for control can be provided by the VMS operating system and DEC's VAX computers. The interactive environment provides the flexibility needed in exception processing: users can examine early results and, if necessary, modify processing parameters for the rest of the run. On the other hand, running programs as is requires attention only in set up.

The high-speed I/O system is provided by the IPS 6000 Peripheral Processor System, which is housed in a backplane module that mounts inside standard VAX cabinets. The subsystem's bandwidth and dedicated intelligence help create an overall processing capacity equivalent to mainframe systems. In comparison with the customized superminicomputers currently in use, the combination of a VAX system and IPS 6000 has nearly twice the I/O bandwidth at about two-thirds the total cost.

Extended VAX Capabilities

The typical VAX-based seismic processing system in Figure 1 provides the two users on the left with the resources to retrieve files of seismic data from reels of magnetic tape, have the data processed as required in an array processor and store the output on magnetic disk or back on tape, perhaps in several different formats and subsets.

Between the time a raw seismic file is copied off tape and finally stored on tape or disk, the data has very likely passed several times over the internal Synchronous Bus Interface (SBI) that forms the backplane of the VAX-11/780's board cage and through board-level Unibus bus adaptors (UBAs) and Massbus bus adaptors (MBAs). The Unibus channels handle multiplexed I/O traffic to and from tape drives and array processors; the Massbus channels handle block-mode traffic to and from the system and data disk drives.

Capacity of the system in Figure 1 — the number of Mbytes it can process in a second — is determined by the bandwidths of the data paths between the computer and main memory at top and the various peripheral devices below. The SBI itself has a bandwidth of 13.3 Mbytes/sec; the bandwidths (or aggregate data rates) of the Unibus and Massbus channels are, respectively, 1.5 Mbytes/sec and 2.2 Mbytes/sec for the VAX-11/780. The bandwidths of the Unibus and Massbus channels are wide enough for typical VAX applications but can limit performance in handling the special demands of seismic and high-volume real-time systems.

The principal extension of VAX hardware architecture through the IPS 6000 subsystem must then be wide bandwidths into and out of the SBI — wide enough so that the SBI is being used at nearly its maximum bandwidth (during portions of the seismic processing cycle in which it is active). In conjunction

Figure 1: A VAX-based seismic processing system provides the users on the left with the computer resources to retrieve files of seismic data from magnetic tape, demultiplex the file, have the data processed in an array processor and store the output on tape or disk.

H. D. Meitzen is President and Delbert L. Taylor is Engineering Manager of Information Products Systems, Inc. located in Houston, TX
with this, the subsystem must also support very high data rates for direct transfers between peripherals (during portions of the seismic processing cycle in which the SBI is not active). Fast direct transfers are necessary in handling multiple array processors and the new tape and disk drives, which have progressively higher data capacities and transfer rates.

Multiple array processors are designed to provide users with dedicated or shared array processors for the seismic data they are currently processing. Array processors, which have typical data rates of about 4 Mbytes/sec, perform two types of on-line processing tasks, relatively simple data conversions and complex matrix manipulations. Integer to floating point conversions are performed on very large data arrays: a single array of raw marine seismic data, for example, consists of 3000 scans of 4 bytes of data in each of as many as 1024 channels (96 to 240 channels are typical now). On-line matrix manipulations in seismic processing extrapolate velocity data to create a subsurface density profile, and the resulting model is analyzed by changing velocity data.

The high performance tape drives used today in seismic processing have densities of up to 6250 bpi and data transfer rates as high as 780 Kbytes/sec. In the near future, tape densities will be over 18,000 bpi in 18-track transports, and transfer rates will be more than 3 Mbytes/sec. A typical disk access time today is 26 msec, and data transfer rates are up to 2.2 Mbytes/sec.

The highest performance magnetic disk drive that is currently supported for in-process storage with the IPS 6000 is the IBIS Winchester drive based on 3380 technology. The IBIS has an access time of 16 msec, and data transfer rate of 12 Mbytes/sec; its data capacity is 1200 Mbytes formatted or 1.2 Gbytes.

The trend in seismic processing is toward archiving on larger and larger disks rather than on tape. Optical storage devices such as Storage Technology Corp.'s 3380 will have data capacities on the order of 4 Gbytes and offer significantly lower cost per stored Mbyte, about $0.05, in comparison to about $0.09 for tape, and superior data density (in Gbytes per cubic inch). Moreover, magnetic tape must be rewritten every two years, whereas optical disk storage is permanent.

**System Design**

The capabilities of the seismic processing system in Figure 1 have been extended in Figure 2 by adding the IPS 6000 Peripheral Processor System. The high-speed data path is IPS 6000's Star channel, a time division multiplexed (TDM) bus synchronized with the VAX's SBI. The Star channel provides for communication of commands, data and status (including addresses) as well as priority information and clock signals. Its bandwidth is 40 Mbytes/sec; that is, the 64-bit-wide channel transfers 64 bits of information in each 200 nsec TDM time slot. This bandwidth is large enough so that one Star channel can handle concurrent data transfers over two 13.3 Mbyte SBI's on the host side and between several sets of devices on the peripheral side.

Data is transferred between the SBI and Star channel over one to four SBI port interfaces which translate between the communications protocols on the SBI and Star channel. An SBI port duplicates the functions of a Massbus adaptor (RH780-A) and has twice its bandwidth. The SBI ports support all types of peripheral devices that are on the Unibus and Massbus devices in Figure 1. Although, like the Massbus adaptor, an SBI port can transfer data to only one device at a time, one Star channel is capable of supporting as many as 10 active SBI ports (4 Mbytes/sec each).

**Channel Controller**

The channel controller has three principal functions: mapping physical data formats between the SBI and Star channel, furnishing diagnostics access to the IPS 6000 subsystem and executing I/O command queues. Mapping registers are under firmware control on the controller, instead of in hardware on the Massbus adaptor. The controller automatically runs channel diagnostics on start-up and provides an RS-232-C communications interface for remote diagnosis. Any register in any device on the Star channel can be read or written into, which is useful for external control of the I/O process.

The intelligence in the channel controller is based on a custom AMD 29116 16-bit bit-slice microprocessor in order to attain an execution speed high enough for the channel. Since the controller handles words from 48 to 64 bits wide, a less expensive off-the-shelf 16-bit integrated microprocessor would have been too slow because it breaks up words for transfer.

**I/O Command Queues**

The I/O commands involved in controlling data transfers between peripheral devices would normally be provided by the VAX host with an interrupt for each successive command (Figure 1). With the IPS 6000, the time required for multiple interrupts is saved, and system performance improved, by writing the entire I/O command queue into the controller in one burst of as many as 64 commands. This can be accomplished either from the VAX host to the controller over an SBI port or from a personal computer or other independent processor linked to the controller's RS-232-C port.

In a typical seismic procedure, a test data file is read from a tape over the Star channel, SBI port and SBI into VAX main memory. The data is demultiplexed from channel array to linear form and transferred back over an SBI port and the Star channel to an in-process disk. In the meantime, the VAX host has data-downloaded to the channel controller the particular I/O command sequence the user has specified to control transfers of the linear file into and out of an array processor (the transfers typically involve large numbers of small data blocks, ranging between 1024 and 4096 bytes in length). There may be several passes through an array processor using different algorithms.

An image processor can be expensive. Unless it's the FD5000. For $11,500, you can purchase an 8 bit frame buffer with driver software. And the system doesn't stop there. As your needs expand, so will the FD5000 to a full 32 bit image processing system for advanced applications.

Check these basic and optional features:

**Flexible Architecture:**
Two 12 bit deep images or three 8 bit images with 4 bits of color or monochrome overlay provide monochrome, pseudocolor, and true color.

**60Hz Flicker-Free Display:**
Bright, flicker-free image display at 60Hz; 30Hz for image processing and real time input.

**Feedback Processor:**
Five times faster than host-based operations for convolutions, digital filtering, interactive math, regions of interest, and recursive filtering.

**1024² x 32 Bit Memory Arrays:**
Optional memory configuration provides user choice of image size and processing precision to display through 512² viewport.

**MINI-LIPS Image Processing Software:**
Interactive keyboard control; prompts for filters, real-time math, Look-Up Tables, histograms, geometric operations, utilities, and image storage; demo programs include source code.

**The Closer Look:**
The FD5000 will minimize the load on your host CPU and your processing staff. Peripheral or stand alone configurations are available.

**Give Us A Call:**
We'll be happy to discuss your application needs and the FD5000 at your convenience.

Gould Inc., Imaging & Graphics Division
1870 Lundy Ave., San Jose, California 95131
Telephone (408) 263-7155 TWX (910) 338-7656

European Headquarters
Tegernsee Landstrasse 161, D-8000 Munchen 90, West Germany
Telephone (089) 6-92-79-06 Telex 5218078 GOUI D

Circle 28 on Reader Inquiry Card
provided by the VAX host as needed.

**I/O Control Units**

There are special I/O control units for disk drives, tape drives and array processors. All have buffers, ranging from 16 Kbytes to 256 Kbytes in size, to compensate for differences in data transfer rates among peripherals and between peripherals and SBI ports. Like the channel controller, all control units are based on AMD 29116 16-bit bit-slice technology.

There are two types of disk control units for the IPS 6000 and both can handle as many as four drives. The enhanced Storage Module Device (SMD) serial interface unit supports and aggregate data transfer rate as high as 24 Mbytes/sec. The modified Intelligent Peripheral Interface (IPI) unit supports the IBIS disk drive. Disk drives that are compatible with either type of control unit appear to the VAX host’s VMS operating system as either a Digital RM or RPseries drive. VMS modifications are therefore not required (drives emulating RM can be linked to the same control unit as drives emulating RP).

The I/O control units are also compatible with VMS-standard diagnostics. The disk control units support full-track buffering (eliminating rotational latency in sequential operations) and extended disk I/O features (remote position sensing, overlapped seeks, mapping two or more logical units into one physical unit). The tape control unit supports three interface standards: ANSI, STC and Telex. Each unit controls up to eight drives.

There are I/O control units for three makes and speeds of array processors: Star Technologies (100M FLOPS), Numerix (30M FLOPS) and Floating Point (10M FLOPS). One control unit is required for each array processor.

Maximum system performance is attained with one array processor for each concurrent processing task. As long as it has adequate execution speed, however, an array processor can be shared by two or more tasks under control of the channel controller.

**System Configurations**

The three standard IPS 6000 subsystems, which contain different numbers of SBI ports and I/O control units, are identified by the widths of their backplane modules that are mounted in the VAX computer’s CPU board cage or extension cabinet. The 4’ model (which supports the subsystem in Figure 2) fits into the cage space normally occupied by a four-board MBA and consists of six extended-hex boards: two SBI ports, three I/O control units and one channel controller. Board space has been reduced — an SBI port provides the same functions as an MBA on only one board — through extensive use of bit-slice and gate array technologies.

The 3½” IPS 6000, which occupies the SBI terminator’s space (the terminator is plugged into the back of the IPS 6000 module), comprises one SBI port, two I/O control units and one channel controller. The 8” model, which occupies the space of two MBAs, comprises four SBI ports, eight I/O control units and one channel controller.

As limited by the addressing capability of a 32-bit host, the IPS 6000 can support very large data bases. The 8” module, for example, has a maximum configuration of four disk drives on each of eight control units. Maximum data storage with IBIS 1.2 Gbyte disks is then 38.4 Gbytes.

**High Reliability Systems**

The representative system configuration in Figure 2 can be modified in a number of ways to meet the needs of different types of applications. For example, the host can be the smaller VAX-II/750, the more powerful VAX-II/785 or any other larger member of the VAX computer family. There can also be two hosts to provide additional capacity and high reliability or fault tolerance. The two high reliability systems in Figure 3 and 4 are based on a single host and dual hosts, respectively. In Figure 3, two Star channels on the same SBI provide duplicate high-speed paths to dual-ported drives and array processors. The system will continue to operate when a single fault occurs at any point below the SBI. In Figure 4, there are also duplicate hosts, SBIs and system disks to attain extremely high reliability in real-time systems such as for nuclear reactor control and satellite communications processing.

---

**Figure 3:** A high-reliability system based on a single-host computer provides duplicate high-speed paths over two Star channels to dual-ported drives and array processors.

**Figure 4:** All elements are duplicated, including hosts and system disks, to achieve high reliability in real-time systems such as nuclear reactor control and satellite communications processing.

---

**How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.**

- Very Useful .................................................. 616
- Useful ......................................................... 617
- Somewhat Useful ............................................. 618
MIP-512 - The Single Board Multibus Machine Vision System

- 512 x 512 resolution
- 8 bits/pixel up to 24 bits/pixel
- 4:3 or 1:1 aspect ratio
- 16.7 million color LUT
- Hardware pan, scroll and zoom
- Dual ported video RAM for true OMA
- IEEE-796 (Multibus) compatible

Image processing technology need not cost an arm and a leg. With the Matrox MIP-512 you can get full 8 bit data acquisition, 8 bit image storage and 90ns/pixel image processing all on one Multibus board and for only $2,995 in singles.

REAL-TIME IMAGE ACQUISITION
An 8 bit flash A/D converter is used for digitizing an external video signal. External sync genlock or internal sync generation are software selectable. On-board programmable offset and gain controls and input look-up tables are provided for real-time pre-processing of raw video data.

IMAGE STORAGE AND DISPLAY
The MIP-512 contains 256K Bytes of dual ported video RAM for storing a 512 x 512 x 8 image. Images can be loaded or unloaded from Multibus to video memory under DMA control in just a fraction of a second.

- 8 bit frame grabber
- 90ns/pixel video ALU
- IP software library (C, Fortran)
- Image processing functions:
  - addition & subtraction
  - averaging
  - convolution (N x M)

The MIP-512 supports instantaneous pixel by pixel panning and scrolling of images, and zooming by a factor of x2 or x4. Up to 256 colors or shades of gray can be displayed from the 16.7 million color LUT.

REAL-TIME IMAGE PROCESSING
A 90ns/pixel video ALU is provided for performing real-time arithmetic and logical operations on image data. The MIP-512 supports several standard image processing functions including frame addition and subtraction, exponentially weighted frame averaging, low and high pass filtering and convolution with an N x M kernel. All computations are performed at high speed by the MIP-512 without burdening the host CPU.

In addition to state-of-the-art graphics and imaging boards, Matrox also supplies monitors, cardcages, CPU cards, memory boards and communication controllers for complete OEM display system requirements.

Call now for a complete documentation package.
THE SAM SYSTEM
MEGA-BYTE
High Performance Multi-Port Mass Memory
MB/SEC

FOR INTENSE I/O PROCESSING:
ON:  FLOATING POINT SYSTEMS
DIGITAL EQUIPMENT CORP.
PERKIN-ELMER
GOULD-S.E.L.

FOR:  REAL-TIME SIMULATION
DATA ACQUISITION
COLOR GRAPHICS
ARRAY PROCESSING

- LARGE MEMORY CAPACITY
- MEMORY HIERARCHY CAPABILITY
- FIVE SAM ACCESS MODES
- SIMPLE INSTALLATION

- FAST DATA TRANSFER RATES
- MULTI-PORT ACCESSIBILITY
- SEPERATE HIGH SPEED BUSES
- LOW COST ($2K per MB)

Very large capacity SHARED ATTACHED MEMORY (SAM) systems are available for custom installation into your computer system. With this multi-port mass memory system, your computer can more effectively manage extremely large data arrays during intense I/O processing. The SAM-500 chassis holds 96MB (12 I/O ports) and the SAM-600 chassis holds 128MB (8 I/O ports). Each chassis can support an 80MB/sec data transfer rate. Four chassis may be daisy chained together for a capacity of 512MB at 320MB/sec. Also, SAM storage modules can be directly attached to provide an additional storage capacity of 9,600MB at a 36MB/sec rate. With a wide range of configurations possible, the SAM system is flexible, expandable, adaptable, and affordable.


Texas Memory Systems, Inc.
9888 Bissonnet #470, Houston, Texas 77036
(713) 771-8200
TLX-792449

Circle 50 on Reader Inquiry Card
Printed Circuit Board Design Demands Versatile Integrated Tools

by Julie Pingry, Senior Editor

Makers of printed circuit board design automation tools are hard-pressed to keep up with designers' desire to use new components and packages. PC board layout systems that allow different pad shapes, specifying device areas on both board sides and fine traces on multiple layers for surface mounted devices are only one aspect. Board design programs need flexibility and interactive features to accommodate mixing TTL with ECL, CMOS and discrete analog devices on increasingly dense and large boards.

Integration of design stages to allow accurate updated documentation is critical as well. If there is a problem or gap while the circuit is being designed (especially common with R&D situations and new types of boards), the engineer should be able to revise a board being laid out by simply changing the schematic. The reverse, back annotation, is also important to design integrity. This allows a schematic to be updated with reference designators and pin numbers as components are placed and swapped for optimum routing.

Interactive changes at every turn allow circuits to meet design constraints. Every board must not only meet speed and function requirements, but also be manufacturable. Some board design systems handle many types of components easily. In contrast, fast and efficient automatic layout algorithms often recognize fewer part types. Computer-aided design programs should not take away engineers' ability to use all of their experience to advantage.

Using Non-TTL Components

Different kinds of devices, like ECL, CMOS and discretes, operate best with particular connection schemes. Since the mainstay of logic components is still TTL, these connections must usually be mixed with TTL-type traces on a board.

Almost all PC board layout systems claim that analog components are handled easily and can be intermixed with digital. However, the way that discrete parts and DIPs are mixed can vary greatly. Autoplacement programs that do not differentiate between analog and digital may place discretes together rather than in association with various ICs.

Another difference is that DIP components generally need

Layout systems must operate by section to combine TTL, ECL, CMOS, DIPs, SMDs and discrete components on a board.

only 25- or 50-mil grids and diamond-shape pads. Discrete analog parts present particular problems to automatic placement packages and autorouters that only operate on standard grids. Many systems allow users to define grids as fine as one mil. Nevertheless, placing and routing to these grids is usually only interactive. This means the process of laying out and routing a board including discretes may take nearly as long with CAD as by hand.

Though some systems now offer fine-grid automatic routines, increasing the possibilities for pad placing and trace routing 25- or 50-fold significantly increases software, processing and memory requirements. One way that grid-based systems may handle off-grid parts is to autoplace and route to the grid and then post-process to actual placement. The danger is that design rule violations may be introduced when components are moved back to actual positions. Current revisions of programs such as Scicards address the severe limits grid-
based algorithms place on design by moving to a gridless system. With gridless programs, the disk space and CPU power of the layout system set limits on board and trace parameters. The algorithm itself is virtually limitless.

High frequency design is particularly tricky. Many high speed designs use ECL components. However, improved CMOS processes yield high speed devices, and transmission line theory may soon apply to these components as well. A number of PC board design systems treat high-speed components the same as any others. On systems that allow the designer to set special restrictions on particular signals or groups of signals, ECL parameters can be met. But this method requires lengthy pre-design work.

One approach is to have a special system for high frequency, as Zuken America (San Jose, CA) does. Their Analog Designer uses the same file format to define the graphic library as plotters use. Therefore, curves on the Zuken system are as accurate as a photoplotter can generate them, and not just orthogonal and 45° traces. With these curves, a fast signal won't propagate in a straight line instead of following the bend. Users of most systems must modify traces by hand for curved corners.

If ECL figures prominently in a company's boards, PC board CAD systems with special ECL design rules checking (DRC) and a special ECL router package will be helpful. Companies offering this feature include Racal-Redac (Westford, MA) with Maxi and Visula, Scientific Calculations (Fishers, NY) with Scicards and ASI (Brookfield, WI) with PRANCE. More restricted algorithms for routing, as well as strict design rules checking, help ensure that high speed circuits will operate as planned. Zuken's system allows designers to create a look-up chart for spacing requirements on the basis of line voltage. The system then autoruses high-voltage nets with more spacing than others, as the user specifies. Trace parallelism and net analysis programs are included in the Scicards 85.01 revision, scheduled for release next month.

Traditional orthogonal routers tend to create jagged traces that look like stairsteps and are longer than they need to be. Zuken, Calay (Irvine, CA) and Cadnetix (Boulder, CO) provide packages that minimize trace stairstepping to straighten and thus shorten lines after routing is complete. Short traces are always desirable, but with high-speed logic, the difference may be between proper and faulty circuit function.

Routers like the Applicon Bravo PCB that can place traces at 45° angles instead of just orthogonally have less need for this post-router processing. Look for 45° autorouting in updated versions of layout systems such as Scicards soon (Figure 1). To reduce the risk of crosstalk, automated programs should also check for parallel traces that are too close together for long runs.

**Designing With New Packages**

Two thrusts in system design, higher performance and smaller area, are converging into a demand for more functions per unit space. Complex devices may now be packaged in any of a variety of pin grid array, leadless and surface mounted devices (SMDs). These packages present a big challenge to board design and manufacture.

Most PC board design systems allow the designer to specify size and shape of the package and pads. Still, most systems do not address non-DIP packages well. SMDs are not on 100-mil centers like DIPs, so their pads tend not to fall on 25- or 50-mil place-and-route grids. Since there are several SMD package types, only a few with standard footprints or outline, they cannot yet be added to standard shape libraries. In addition, pads and component spaces should appear on only one side of the board. In designing two-sided boards, nearly all systems now require the engineer to place each part on one side or the other. Even companies like Cadnetix that provide a special SMD handling capability make two-sided placement manual.

Some newer board design systems like the Visula system from Racal-Redac will permit automatic swapping between two sides. Automatic layout programs as used by some service bureaus like Algorex and RDS AutoMate (Palo Alto, CA) also perform swapping between sides. Though these programs have not been available for in-house design use, Data General's (Westboro, MA) agreement with RDS AutoMate covers Auto-
CAD without CACHE™ is like life without water.

Now CACHE brings the CAD design process to life with the information you need. No more long dry spells while you wait for your CAD Library to be created. CACHE offers the design engineer a comprehensive component library of standard and semi-custom IC's that support logic design and physical layouts for engineering workstations and turnkey CAD systems. With the information from CACHE at your fingertips, you can shorten your design path, reduce design costs and improve productivity. So learn how to breathe new life into CAD with CACHE. Call us or send in the attached form today.

Call: 1-800-443-INFO
303/694-4200 (Within Colorado)

Tell me more about how CACHE can add life to my CAD system.

Name ___________________________________________
Title ____________________________
Company ___________________________________________
Address ___________________________________________
City ___________ State _______ Zip ________

Send to: INACOM International, 4380 South Syracuse Street, Denver, Colorado 80237

Circle 3 on Reader Inquiry Card
Mate's two-sided autoplacement program (Figure 2). The processing and memory requirements of packages with these advanced algorithms are, predictably, fairly large.

The density of boards using small, high-pin-count component packages may require multiple trace layers. Including power and ground layers, Scicards handles 20 layers. The new revision will handle 32 layers. Calay can route 8 signal layers; Cadnetix and VR's (Austin, TX) Merlyn systems route up to 24 trace layers; Vectron specifies 25. Racal-Redac's newest systems will handle 16 layers, up from four. ASI claims that hardware places the only limit on the number of layers PRANCE can lay out. Though current designs may not require many layers, high limits are better insurance for future needs.

CAD Systems for multiple signal layers need different routers. Most programs route two layers at a time. To better distribute density over the entire board, a few companies offer simultaneous routing on several layers. For example, Calma's T-Boards routes four layers at a time; Applicon claims multi-layer routing with the Algorex software as well. Autorouters in the 32-layer Scicards release will operate on all layers at once.

Buried vias are often used for SMDs and complex multilayer boards. With multiple signal layers, vias may only need to go between pairs of layers and not all the way through the board. This is a feature many companies' multiple layer systems already have. Some who do not, like Applicon, claim that through-holes may be more cost-effective in manufacturing than buried vias. Though few current designs really require the space on each layer that unused vias occupy, space saving is undoubtedly gaining importance.

Since a vast majority of boards currently use few if any SMD or exceptionally high-speed parts, systems must accommodate combinations of TTL, ECL, DIPs, SMDs and CMOS discrete components without bogging down unduly. To place and route mixed component boards, CAD systems must provide optimized routines for each type of component. Placement and routing programs should be specified by nets, layer, name pre-fixes, individual signals or physical section of board.

**Ways To Skin The Cat**

Key to mixing different technologies and packages is the system's ability to work with only part of a board during an operation. CAD system flexibility includes three other main features. First is a combination of automatic and interactive routines for placement and routing. Although a fully automated batch system may speed the design, critical component placement and trace routing are nearly always best done by the engineer. Second is a variety of algorithms available for each task. Third is DRC override, which also enhances the designer's ability to complete the board. All of these make automated design more like manual design.

The origin of a PC board design system may indicate its interactive capabilities. Those that originated in a design service bureau environment will tend to accommodate large boards and nearly any type of component but have few or no interactive features. Vectron Graphics (Santa Clara, CA), for example, began as a bureau. ASI is still primarily a service bureau, but they now offer PRANCE users a routine to allow some interaction via Megatek color graphics terminal plus IBM PC AT. And Applicon's agreement with Algorex permits both powerful automatic routines and interactive capabilities.

Most CAD systems concentrate on routing, but placement can aid efficient autorouting. Optimizing placement routines are standard with Telesis' (Chelmsford, MA) EDA-3000 PCB; Calay autoplacement software anticipates their router's algorithms and places components according to how easily connections may automatically be made. RDS Automate concentrates a good deal of effort on placement as well.

Another feature that can ease autorouting is placement histograms, which show density of connections on the board as it has been placed. Very dense areas appear as peaks on PRANCE and Telesis density histograms. Manual re-placement can level out the graph, or several placements can be displayed for the most promising.

Automatic routing programs are notoriously inflexible. Static router programs that lock a trace into place as soon as it is routed
FREEDOM to interface the bus independent OMNI 1000 GDC to your host via DMA, Parallel I/O or Serial RS-232C with off-the-shelf hardware available for most bus architectures.

FREEDOM to reduce software development cost. Use the OMNI 1000 GDC together with OMNILIB host interface library (FORTRAN or C) for full GKS compatible functionality.

FREEDOM to reap the benefits of the OMNI 1000 GDC multiple processor design. Overall system performance is enhanced by local scale, rotate, translate, polyfill, drag, clip, highlight, rubberband, etc. provided by the display list processor.

FREEDOM to choose the OMNI 1000 GDC configuration which fits your needs; circuit board only, rack-mount/tabletop enclosure or complete graphics terminal.

The OMNI 1000 GDC is a single board graphics controller with display resolution of 1024 x 1024 x 8 planes. High performance graphics, segmented architecture, bus independence and an extraordinary high level of field proven reliability are hallmarks of the OMNI 1000 GDC.
can block pins, making connection fails that must be manually maneuvered to open paths to the pin and complete routing. Others rip up completed routes to connect fails. This is normally done in a batch after an analysis of hot-spot areas that are too dense to complete all traces. Some systems, such as Applicon's Bravo, allow trace-at-a-time rip up. With this scheme, only one trace is unconnected rather than the entire hot-spot area. The intent is to leave intact as many good routes as possible.

Interactive routers are not as critical with efficient automated routing algorithms. If the user can set parameters and fix critical paths in advance, any routing program is more flexible. Combining several routers may be even better. For example, Vectron's router uses pattern fitting first. This router tries to create straight, then L-shaped with a via and inverse L traces first, for the cleanest possible initial routes. After this, the system runs an exhaustive Lee algorithm router (the most common auto-route algorithm) to finish.

Other approaches include even more routers. Scicards has five different routers; PRANCE has four, as do Racal-Redac's larger systems, and Telesis workstations and Racal-Redac's PC-based systems (Figure 3) use three routers. Normally, if only one rip-up algorithm is available, full re-entrance for user interaction is critical. Exhaustive rip-up autorouters generally run for several hours, and intervention may allow more reasonable completion times.

The goal is not just to autoroute 99% of the board in the shortest possible time; it is to finish routing a board that has optimum performance and is fully manufacturable. Often, the 1% not routed by automatic routines is nearly impossible to route. Sometimes, that 1% cannot be completed in the time that a full 10% could be done after a combination interactive and automatic route. And experienced designers can often foresee problems with particular ICs, traces or nets that no algorithm can handle.

Two approaches are generally taken to design rule checking. On-line DRC (Figure 4) generally does not let spacing violations occur. Though this is an aid to users doing interactive work, it can slow down a program considerably. In addition, designers often violate design rules intentionally to make difficult connections and complete dense boards.

Many systems provide batch DRC. Output of a batch check is generally a netlist mismatch or spacing violation list; the best of these programs also provide a visual display of where rules have been violated (Figure 5). The designer can then find and fix unintentional violations, leaving intact those that were introduced to allow completion.

With several approaches available at each design stage, the options of manual design are combined with automated speed. Either full re-entrance at every step of an automated process or a full complement of algorithms used by the automatic router can provide this range. Some of the faster routines are the least flexible and create boards that are difficult to complete and to manufacture.

**ECOs and Back Annotation**

The normal design cycle begins with schematic capture, from which a netlist is generated. Once the design has been verified, placement and routing programs take over, and after optimum layout, artwork and machine tapes are generated. All of these stages are becoming computerized, and though this speeds the process, applications must be integrated for smooth hand-off from engineer to layout designer to manufacturing personnel.

Entering schematics on a small computer is extremely attractive; many firms use IBM PC software for front-end engineering from FutureNet (Canoga Park, CA), Case Technologies (Menlo Park, CA) and P-CAD (Los Gatos, CA). Companies using a mainframe or service bureau for routing may invest in a minicomputer or supermicro-based workstation for several other functions. For this to be effective, interfaces must be written between systems.

Vendors of all levels of CAE and CAD products are developing interfaces that allow not only uploading a netlist to a mainframe, but also downloading for back annotation of schematics. Formatting a netlist for use on another system is only part of the information flow needed; an engineer must be able to make circuitry changes at any point needed as well as be advised of pin and gate assignments finalized during placement and routing. The engineer must also be able to specify pins that cannot be swapped, maximum line lengths and line widths for critical paths in the job library.

Back annotation may be automatic; generally, it is preferable
NEW EL and VF DISPLAY MODULES

GRAPHICS MODULES

Electroluminescent Graphics Module with powerful drawing processor using GCI (VDI) industry standard syntax. 512 x 256 pixels.

TEXT MODULES

Electroluminescent Text Module allows 24 lines by 80 characters, double wide, double high characters, many other features.

Electroluminescent Display Modules from Digital Electronics Corporation

Vacuum Fluorescent Graphics Module. Controller has dual processor pipelined architecture for fast speed. 320 x 240 pixels.

Vacuum Fluorescent Text Module allows up to 240 ASCII, ECMA and KATA-KANA characters, parallel or serial input.

Vacuum Fluorescent Video Module accepts NTSC standard RS170 signals, has 16 gray levels, 3.75” x 5.00” screen size.

Vacuum Fluorescent Text Module allows 2 lines by 40 characters, same features as above. Only +5 vdc power needed.

Vacuum Fluorescent Text Module, super fast bit mapped display. 256 x 64 pixels.

Vacuum Fluorescent Text Module, 40 characters. Above three modules available in high brightness and extended temperature range versions also.

Vacuum Fluorescent Text Module, 2 lines by 20 characters, loaded with features!

* MANY MORE! Over 25 standard models available!

WORLDWIDE DISTRIBUTION

THE DISPLAY INNOVATORS

DIGITAL ELECTRONICS CORPORATION

26142 Eden Landing Road • Hayward, CA 94545 • (415) 786-0520
Telex: 172073 DIGELEC HYWD • Facsimile: (415) 786-1040

Circle 62 on Reader Inquiry Card
to have a command for batch back annotation. That way, until all of the design is finished, no interaction between schematic and layout is required. Accurate documentation available to the engineer at every step eliminates time wasted on work with faulty circuit designs. Interfaces between design tools and simulation and test systems are also critical.

Users may want to use engineering workstations to enter schematics and to format the netlist for larger computers for PC board layout and routing systems. HP 1000-based Zuken systems interface to Daisy and Mentor front-end workstations via IGES files. Likewise, Computervision's CADDs 4X and Metheus-CV workstations can communicate for updating schematics on the Metheus workstation.

For a complete design cycle, Metheus-CV also provides an interface into GenRad's (Santa Clara, CA) HILO logic simulator (Figure 6). FutureNet schematic capture, which interfaces to several PC board layout systems, offers HHB Softron's (Mahwah, NJ) CADAT logic simulation with their IBM PC XT or AT CAD system. Cadnetix also offers CADAT with their schematic entry and board placement and routing tools. Companies like Calma provide a variety of software tools to cover engineering, verification, design and test.

One way of assuring integration of software for various design stages is to get all of the packages from one company. Racal-Redac uses several different hardware bases that share a common binary database structure. This provides all users and applications rapid response to even complex commands. Using an IBM AT or XT, autoplacement may be performed in seconds, routing in a few minutes. Very large designs can be shipped off to a VAX-based Redac Maxi system over RS-232. Even vendors of mid-range workstations like Telesis now provide back annotation to IBM PCs.

Documented Circuits Inc. (Kingston, Ontario, Canada), Vectron, Calma (Santa Clara, CA) Cadnetix and others tout total solution systems (Figure 7) with schematic entry as well as placement and routing capability. Integration can be on common hardware; Data General (Westboro, MA) offers Cericon's AI-based schematic entry system and RDS Automate layout and routing software. Scientific Calculations offers the Schematic package for a front-end to Scicards. A master file in the Vectron system keeps all nomenclature used for one part, and a back annotation command can attach updated reference designators to a schematic. Although most companies' PC board design programs have some weak links, forward and back annotation are best served by one-vendor solutions.

Beware The Panacea

There are clearly many approaches to designing a board at each step of the way. Different CAD vendors have focused on different aspects of the problem, and finding one piece may or may not help speed the completion of the puzzle. Versatility, choices and completeness take many forms. With the array of PC board design methods provided by various layout systems, comparison may be difficult.

Potential customers must be wary of vendor claims. Some of the most widely installed CAD systems are "multiplication," which means they perform mechanical and 3D design as well as electronic. This may be appealing, but the specific demands of electronic design are often not well addressed, leading to long, frustrating PC board design cycles.

Figure 7: From the orange menu box on the Cadnetix screen, a board with all ICs placed is chosen. Note that the menu on the right side uses icons as well as English words to display function choices for all stages of board design.

Fully automated placement and routing packages speed up part of the cycle, but often leave the most difficult nets for the designer to connect. Overall design time may increase with faster automatic functions. A prime example of this is auto-router advertised as 100% routers. There will always be some boards that cannot be routed to completion. Furthermore, these are usually rip-up routers that blindly connect as much of the design as possible and then disconnect areas of the board with fails, repeating the process as each rip up creates new problems in adjacent areas.

One feature that can shorten routing completion time is intelligent placement packages. Asked about their autoplace program, most companies say theirs is as good as any; this is not a good sign. Forecasts of density and routability from initial placement speed the entire cycle greatly.

Perhaps the most comprehensive wool-pulling act of PC board CAD companies is benchmarks. Companies can play all sorts of tricks to make their systems appear fast. Users should never give the vendor a design in advance, and once the benchmark begins, the user should stay through the entire ordeal. Online design rule checking can be turned off to speed programs; be sure to request documentation of either batch or ongoing DRC. Finally, there should be criteria other than layout speed. For example, are there extra vias? Could line lengths be shorter? If the board is not 100% routed, are the unconnected traces the most difficult? And above all, is the board manufacturable with the customer's technology? Two or three fine traces between pads may not be feasible, while six simpler layers, though expensive, could provide the same functions.

The board from a CAD system should be totally finished, from schematic to artwork and manufacturing output tapes, in less time than without it. Speed is just one factor. Design automation is only a help if the finished product is as good as an equivalent hand-design or better. In many cases, designer intervention will be needed to achieve this optimum design.

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful ...........................................604
Useful ...................................................605
Somewhat Useful .....................................606
Even under real-world conditions, THE EYE™ from Analog never blinks.

At last, there's a practical way to achieve increased productivity with zero defects. Because despite the tough demands of factory life, The Eye never blinks.

We've optimized our IVS-100 intelligent vision system for the real world, not idealistic test lab settings. Its unmatched 256 gray level capability and high resolution (512 x 512 pixels) enable it to compensate for uneven lighting and still pinpoint subtle defects. It's the first system to incorporate Intel 80286/287 microprocessors and the Intel 80186 I/O processor, so it can handle images and make decisions in synch with the highest production speeds. What's more, The Eye can communicate with host computers, and it interfaces with plenty of peripherals. And because it adapts readily to specific applications and configurations, The Eye can be integrated into your factory's plans with amazing ease.

As for the price, it's surprisingly down-to-earth.

Best of all, The Eye is backed by Analog Devices, a $300,000,000 company with the factory automation know-how to match our state-of-the-art technology. We'll be here today and tomorrow, offering all the support you'll ever need. We'll tell you up front whether The Eye is right for your application. And if it is, we'll work with you to find the best possible solution—and make it a reality.

So look into The Eye. For the full story on our IVS-100, call Sandra Perry or Alan Berger at (617) 329-4700, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.

The first machine vision system designed to cope with reality.
IRONICS — The Full-Line High-Performance Leader in VMEbus

Ironics VMEbus boards and VMEsystems provide the OEM and Systems Integrator with a powerful, productive development environment and a full spectrum of high performance, cost effective target solutions. The Ironics Technical Support Group adds the customer support and service necessary to make your next project a reality. Call us today.

IRONICS Incorporated
Computer Systems Division
742 Cascadilla Street
Ithaca, N.Y. 14850
607-277-4060  Telex: 705-742

Circle 38 on Reader Inquiry Card
DMA Controller Relieves Host Of I/O Management
by Scott Searcy, Intel Corp.

I/O subsystems for high-performance computers must not only process and transfer large amounts of data, but also interface to a large number of peripheral devices. Traditionally, an I/O board has been used to meet these system needs. The Intel 82258 pipelined 16-bit advanced DMA processor combines many of the I/O capabilities of a board onto a single chip (Figure 1).

Command chaining and data manipulation capabilities of the 82258 enable it to execute sophisticated channel programs in memory-based command blocks. The data chaining feature of the 82258 allows it to either gather a link of data blocks into a single area or scatter them in the reverse operation.

Optimized for the iAPX 86 microprocessors, the 82258 has an on-chip bus interface for full CPU memory addressability with the pipelined, nonmultiplexed 80286 bus as well as the multiplexed bus of the 80186/88 and 8086/88. Both local and remote interfaces with the processor are supported.

Device Architecture
The 82258 has four channels (called selector channels 0-3) that can service high speed peripherals, generally block devices such as Winchester and floppy disk drives. Each selector channel comprises its own dedicated register set and three control lines. Peripherals initiate DMA requests by activating the DREQ (DMA request) input. The 82258 acknowledges that it has recognized the request by activating the DACK (DMA acknowledge) output. When used by a peripheral, the bidirectional EOD (end of DMA) line tells the 82258 to terminate the current transfer. The controller uses the EOD line to inform the peripheral as well as the CPU that the current transfer has been completed and that the status of the transfer is available.

Selector channel 3 can be programmed as a multiplexor channel to support up to 32 subchannel requests. Subchannels typically handle slow-to-medium speed character devices like CRT terminals and line printers. One or more 8259A interrupt controllers multiplex, arbitrate and prioritize the subchannels (Figure 2). After receiving a request, the master 8259A signals the DMA controller via the I/O request (IOREQ) line that a subchannel needs servicing. The DMA controller responds with two I/O acknowledge (IOACK) pulses, which strobe the 8259A to make the interrupt vector available on the data bus. The interrupt vector is used as an index into a multiplexor table to obtain the address of the command block for the appropriate subchannel. The command block is then executed.

Using the multiplexor channel, DMA processing can be provided for a wide variety of devices with just four channels. High speed devices can get the majority of the servicing, while low speed devices share the servicing and transfer rate of one channel.

Like the 80286, the 82258 recognizes two separate address spaces, I/O and memory, and allows all transfer permutations between or within the two spaces. To perform these transfers,

Scott Searcy is an 80286 Applications Engineer for Intel's High Performance Microprocessor Operation in Santa Clara, CA. He has a BS in Computer Science from Purdue University.
PRODUCT INDEX

To help you find the products that you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a circle number for additional information on that product. Bold type indicates advertised products.

**Computers/Systems**
- Aptec 62 69
- Heurikon 116 79
- International Robomation/Intelligence 61 63
- Numerix C4 53
- Accell Technologies 107 161
- Adage 100 215
- Calma 100 156
- Cromenco 100 163
- Cyborg 100 164
- Data General 102 158
- Esprit 100 216
- Gould 107 155
- Microware 94 230
- Opus Systems 100 219
- Perkin-Elmer 102 218
- Racal-Dana 107 165
- Sunrise Electronics 100 157
- Texas Instruments 102 217

**Mass Memory**
- ADE 15 29
- Alcatel Thomson 122 86
- Gigadisc 8 7
- Ito Inc. 122 86
- Storage Concepts 50 20
- Texas Memory Systems 68 50
- C. Itoh 105 213
- Control Data 109 174
- Storage Concepts 96 235
- Telex 109 175

**Input/Output**
- Carroll Touch 17 1
- Honeywell 19 25
- Maxi-switch 106 45

**Printers/Plotters**
- Appleton Thermal Papers 49 23
- Genicom 9 57
- Nicolet 25 18
- Acromatics 109 168
- Digital Equipment Corp. 96 231
- Genicom 109 176

**Displays/Terminals**
- Chrislin Industries 120 145
- Honeywell 19 25
- Maxi-switch 106 45

**ICs/Minicomputers**
- Hytek Microsystems 105 85
- Mostek 13 16
- AMD 115 200
- Analog Devices 115 189,188
- Analogic 117 199
- Burr-Brown 114 191,193
- General Instrument 117 126
- Integrated Device Technology 117 205
- Intel 115 142
- Micro Linear 115 204
- Monolithic Memories 114 137
- Motorola 116,114 133,132
- Motorola 114 131
- National 114 127,128
- Semiconductor 114 143
- SCD 115 135
- Signetics 115 205
- Standard 117 202
- Microsystems 117 202
- Teledyne Semiconductor 117 130
- Zyrex 114 129

**Middleware/Embedded Devices**
- BICC-Vero 39 30
- Electronics Ltd 42 15
- Financial Protection Devices 123 90
- Mupac 112 70
- Schrock 104 52
- Scientific Micro Systems 89 26
- Zolltech 101 12

**Components**
- Data Delay Devices 118 84
- ITT Electro-Optical 105 41
- Simpact Associates 111 31
- Sperry/Aerospace & Marine Corp. 122 37

**Communications**
- GTE Communications 99 117
- Fujitsu America 112 170
- IBM 105 169

**Software/Firmware**
- INACOM International 71 3
- Research Systems 102 71
- Alcyon 122 227
- Caeco 121 179
- LMI 122 222
- Rapidtech 94 234
- Structural Dynamics Research 122 185

**Boards**
- Andromeda Systems 107,109 76,67
- John Bell Engineering 109 91
- CSPI 91 60
- Datacube 1 9
- Diversified Technology 29 36
- DSP 52 21
- dy4 37 9
- EMS 33 22
- Force Computers 2,3 58,59
- Goodspeed 7 8
- ICs 78 38
- Matra 11 17
- Matrox Electronic Technology Inc. 67 51
- Microbar 31 11
- Mizar 41 32
- Mostek 87 44
- Number Nine 103 64
- Omnimbyte 45 10
- Omnimcomp Graphics 73 35
- OMTI Scientific Micro Systems 27 61
- Plessey Microsystems 47 27
- Systech C3 81
- Techvu 107 43
- Advanced Computer Concepts 119 196
- Andromeda Systems 118 207
- Burr-Brown 121 145
- Chrislin Industries 120 152
- Crompton 98 232
- Cubit 118 144
- Data Translation 119 151
- Dilog 119 150
- DSP Systems 121 148
- EMS 119 210
- Emulex 121 146
- Gespoc 119 206
- Matrox Electronic Systems 120 147
- MBD 121 149
- Microdesigns 120 208
- Mintronics 121 154
- Parallax 98 233
- Peritek 120 153
- Princeton Graphics Systems 120 211
- Seattle Telecom and Data 119 209
- Verticom 120 192

**Test Equipment and Instrumentation**
- Hitachi 117 201
- Minarad Systems 100 195
- Tektronix 107 159

This index is provided as an additional service. The publisher assumes no liability for errors or omissions.
CALL FOR PAPERS:

Topics of Interest:
We invite technical papers of recent and novel developments in all areas of Computer Aided Engineering and Design. Topics of interest include, but are not limited to the following:

- CAE/CAD
- Engineering Workstations
- Design Test
- Future Trends
- Simulation
- CAE Tie-In with ATE
- Fault Simulation
- VLSI Design
- Design Test/Verification
- Board Design
- Prototype Evaluation
- System Design
- Layout Tools
- Human Factors/Engineering
- Data Base Issues
- Productivity Improvement
- PCS for CAE/CAD
- CAE/CAD Management
- Silicon Compilation
- System Economics/Justification
- Expert Systems
- Test Program Generation
- Design Test
- Future Trends
- CAE Tie-In with ATE
- VLSI Design
- Board Design
- System Design
- Human Factors/Engineering
- Productivity Improvement
- CAE/CAD Management
- System Economics/Justification
- Test Program Generation
- Future Trends
- CAE Tie-In with ATE
- VLSI Design
- Board Design
- System Design
- Human Factors/Engineering
- Productivity Improvement
- CAE/CAD Management
- System Economics/Justification
- Test Program Generation
- Future Trends
- CAE Tie-In with ATE
- VLSI Design
- Board Design
- System Design
- Human Factors/Engineering
- Productivity Improvement
- CAE/CAD Management
- System Economics/Justification
- Test Program Generation
- Future Trends
- CAE Tie-In with ATE
- VLSI Design
- Board Design
- System Design
- Human Factors/Engineering
- Productivity Improvement
- CAE/CAD Management
- System Economics/Justification
- Test Program Generation
- Future Trends
- CAE Tie-In with ATE
- VLSI Design
- Board Design
- System Design
- Human Factors/Engineering
- Productivity Improvement
- CAE/CAD Management
- System Economics/Justification
- Test Program Generation

The CAD/CON Conference is devoted entirely to the field of Computer Aided Engineering and Computer Aided Design, with emphasis on the use of computers as aids for the design through prototype evaluation of electronic components, boards and systems. We encourage papers on today's problems and solutions to these problems in addition to enhancements perceived for the future. Formal technical and application sessions are presently planned for the Conference. Formal papers will be required for the technical sessions and short presentations will be required for each application session panelist.

If you are interested in presenting papers at the conference, please submit an abstract (200-500 words) and your biography. Please be sure to include your name, title, company, address, phone number and appropriate subject category. All selected papers will be published in the proceedings for the conference.

Abstract Submission Form
Please attach this form with your abstract or paper idea.

Name ____________________________
Title ____________________________
Company _________________________
Address __________________________
City __________________ State ______ Zip ______
Phone No. ( ) _______ ___________ ext. ______
Paper Subject ______________________

Please complete one: Abstract attached ________ Abstract to come by ________
the 82258 uses either a single-cycle or a two-cycle method. A single-cycle transfer offers the advantage of speed. Although two-cycle transfers require an additional bus cycle, they allow additional data manipulation operations with the data transfer.

In single-cycle transfers, an address is put out during the single-bus cycle to access a byte or word in memory. The peripheral is selected by the DACK signal asserted by the 82258. Data travels directly between the selected I/O peripheral and memory (or addressed peripheral), not passing through the controller. Since the data is sent directly to the destination, only two of the concurrent data manipulation operations are possible: mask/compare and verify-and-save.

During a mask/compare operation, the DMA controller masks the source bytes or words and compares the result with the value stored in the channel's compare register. At the completion of single-cycle transfers, it is only possible to determine whether a mismatch or match existed in the block. This mask/compare operation can be used to search through a data block for a specific byte or word and halt when it is found. The verify-and-save operation is used to compare the source data block with another block in memory. This is useful for comparing data block identification headers.

Although two-cycle transfers typically require an additional bus cycle, they are more flexible. Data is actually stored in an internal register of the DMA controller on its way to the destination. As a result, more data manipulation operations are possible. For example, the mask/compare operation can be halted when the first instance of a mismatch or match is recognized. Unlike the single-cycle verify-and-save, the verify-and-halt operation transfers no data, but simply performs a block compare. As with the two-cycle mask/compare, however, the transfer can be halted on the first instance of a mismatch (or match).

Two functions are possible only during two-cycle transfers: translate and automatic assembly/disassembly. During translate, each source byte is used as an index into a translation table from which the destination byte is derived. Automatic assembly/disassembly supports transfers between dissimilar bus widths, allowing 16-bit processors to interface transparently with 8-bit peripherals.

<table>
<thead>
<tr>
<th>Type 1 Command</th>
<th>Type 2 Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA Transfer</td>
<td>DMA Transfer</td>
</tr>
<tr>
<td>Conditional Jump</td>
<td>Unconditional Jump</td>
</tr>
</tbody>
</table>

Figure 3: Command chaining uses two types of commands. Type 1 commands specify the DMA transfer and type 2 commands determine the flow of control. Complex "programs" can be described using command chaining.

<table>
<thead>
<tr>
<th>Type 2 Command Blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type 2 Command</td>
</tr>
<tr>
<td>16-Bit Displacement</td>
</tr>
<tr>
<td>Absolute JUMP</td>
</tr>
<tr>
<td>Unconditional STOP</td>
</tr>
</tbody>
</table>

Figure 4: Type 1 short command blocks contain all of the parameters needed for a transfer. For simultaneous operations, the extension block is needed, and the status block is optionally included if specified in the command extension word. Type 2 command blocks specify jumps and stops which can be conditionally performed on status information.

**System Configuration**

A microprocessor system can be configured using the 82258 either remote or local. As a remote device, the DMA controller can act as an I/O processor and maintain minimum communication with the processor. In this mode, the processor can access its own resources over the system bus while the 82258 controller performs transfers across its resident bus on which its own memory and peripherals reside.

Alternatively, the 82258 can be installed for local mode operation, which has been optimized to support the 80286. For this mode, the 82258 is a coprocessor sharing the system bus resources with the CPU. These shared resources can only be referenced by either the processor or the DMA controller at one time, somewhat reducing system throughput. However, local mode uses less board space and minimizes chip count since the controller shares the bus support components of the processor.

In both local and remote modes, the main exchange of control information between the processor and the registers of the 82258 is through command blocks located in memory. The DMA controller can be mapped in either memory space or I/O space. The locations a controller occupies are decoded into its...
EIKONIX** high-performance digital imaging cameras offer unique capabilities that clearly distinguish them from all others.

**CCD or Photodiode Technology**
Only EIKONIX offers a choice of high-resolution cameras employing either linear CCD (charge-coupled device) or photodiode technology. In fact, EIKONIX offers the highest-resolution CCD camera available anywhere, with up to 20 million pixels per image (4096 x 5200).

You can choose the economy and low-light capabilities of a CCD camera, or the greater dynamic range of a photodiode camera, without sacrificing high resolution.

**Color or Monochrome**
Only EIKONIX has a family of high-resolution cameras available for either monochrome (256 gray-scale levels) or color (a palette of 16 million colors) applications.

**More User Control**
Only EIKONIX cameras use a precision stepping-motor/lead-screw/ball-screw stage mechanism, which provides precise positioning of the array and eliminates one-dimensional smearing. In addition, this mechanism allows asynchronous operation, so the user can control both scan speed and data collection rate. This eliminates the need for a separate "frame grabber" or dedicated processor, and frees the host computer for multi-tasking.

**Buy Just What You Need**
Only EIKONIX' broad product line lets OEMs and end users match needs precisely. Configurations range from bare-bones digital camera heads through complete image acquisition subsystems, including cameras, light sources, control electronics, imaging software, and interfaces for many widely used computers (including most DEC and Multibus-based systems).

**More Applications**
Only EIKONIX offers the performance and flexibility to handle the broadest range of the most demanding applications, including mapping, engineering drawing digitizing, graphic arts, CAD/CAM input, office automation, X-ray storage and analysis, textile pattern design, geological imaging, communications, animation and microscopy.

**EIKONIX Know-How**
Only EIKONIX digital imaging products are backed by our 17 years of experience in matching advanced electro-optical technology to a widening world of applications.

To find out what we can do to support your digital imaging applications, contact EIKONIX, 23 Crosby Drive, Bedford, MA 01730, (617) 275-5070.

© Copyright 1985 EIKONIX® Corporation. DEC is a trademark of Digital Equipment Corporation. Multibus is a trademark of Intel Corporation.
chip select signal, providing access to its internal registers. These registers are divided into a set of five general purpose registers and four independent sets of channel registers.

General registers specify system parameters such as channel priorities and bus widths, optimum bus loading, channel command (start, stop, single step) and current status. Channel registers (one set per channel) hold all of the transfer specific parameters like source and destination addresses, byte count, channel command and mask/compare values. All but one of these channel registers are loaded from the command blocks by the chip itself to execute the transfer. Therefore, the slave interface is used mainly to set the general registers and the channels' command pointers, or to examine the value of the registers during debugging efforts.

All of the information needed for the 82258 to perform a transfer is stored in the CPU in control blocks for each channel. After the command pointer register is assigned, the CPU reads the starting address of the command block and a start channel command is given. The controller then loads that particular channel's registers. When synchronized externally, the 82258 then waits to perform the transfer until it receives the DREQ (or IOREQ) from the device needing service. If synchronized internally, the 82258 begins the transfer immediately when the start command is issued. This is particularly useful for memory-to-memory transfers.

**Command Structure**

Command chaining is accomplished by placing individual DMA transfer command blocks sequentially in memory (Figure 3). In this way, once one DMA operation is completed, the internal registers are loaded from the next control block and the next operation is started. The 82258 knows that it must stop making transfers when it fetches a command block which contains a "stop" command.

Two types of command and associated control blocks are used in command chaining (Figure 4). A type 1 command block describes the actual transfer that is to take place, specifying the addresses and the byte count. If needed, the translation table pointer and mask/compare values are also included in an extended type 1 command block. A status word and, optionally, a status block are updated when the 82258 finishes the DMA transfer. Type 2 command blocks provide a mechanism to branch to another transfer or to stop the selector channel (or subchannel) currently running.

A type 2 command checks the information in the status register, which is written to the command block at the end of each DMA operation. The system then makes a conditional jump (absolute or relative) or a conditional stop. The four conditions which can be tested are termination due to reaching the byte count, a match or mismatch occurring in a mask/compare transfer, a mismatch occurring in a verify transfer and receiving an external end of DMA signal. Unconditional branches are also possible by testing all of the status bits since at least one will be set. This branching mechanism gives the 82258 the intelligence to perform sophisticated operations such as error detection and processing.

Data chaining allows the 82258 to organize data before and after transfers. For example, one block of data may need to be dispersed into several different blocks, or vice versa. This is called scattering and gathering of data. For DMA controllers with no data chaining capabilities, either separate transfers must be specified or the CPU has to manage the data blocks before and after the transfer. In contrast, the 82258 controls all of the scattering/gathering and only one DMA transfer command is needed. This is accomplished by regarding the source or destination address as a pointer to a list of data blocks. The list can be either a sequential list or a linked list (Figure 5).

Data blocks in sequential lists are described contiguously in memory, as if they were in an array. The 82258 transfers one block and then proceeds to the next one, needing only 1 µsec of linking time, until it sees a block which has a byte count of zero. Though the speed is attractive, it is difficult to perform insertions and deletions on sequential lists. Flexibility is the overwhelming advantage of linked list chaining (Figure 5). Here, the structure describing the data blocks contains a pointer to the next block to be transferred, and insertions and deletions are performed by rearranging those pointers between blocks. The 82258 requires slightly more linking time when using linked list because of the additional pointer, but that additional time will be offset if the chain list is modified often.

![Figure 5: Data chaining gives the 82258 the capability to scatter or gather data blocks. Linked list chaining (left) is flexible, allowing insertions and deletions to be made easily. List chaining (right), however, requires less space and less linking time between blocks.](image-url)
OEMs get products to market faster with SMS microcomputer foundation systems, storage systems and Winchester controllers. These products already support popular operating systems such as iRMX*86/286, Xenix**, CP/M*** and others.

Whether you select 8086, 80286, 68000, Z8000 or another Multibus* single board computer you can choose the SMS product to fit your packaging needs.

one or two 5-1/4" floppy disk drives, one 8" floppy, a 5-1/4" streaming tape and includes a Multibus backplane — all in a single 5-1/4" enclosure.

An integrated “System Foundation Module” contains all the peripheral control logic plus operator status, test and set up capability without taking any backplane space.

For high volume or unique packaging requirements the FWD8001/FWD8006 single board controllers are INTEL*215 compatible and support 8" Winchester/floppy, 5-1/4" Winchester and 5-1/4" or 8" floppy disk drives.

Table top or rack mount enclosures are also available for the Model 40.

If you have your own Multibus backplane, plug in the SMS 8000 Model 60 storage system. It occupies only 5-1/4" of rack space and comes in all the peripheral configurations of the Model 40.

The attractive floor standing SMS 8000 Model 40 microcomputer system provides from 10 to 280 Mb of 5-1/4" Winchester storage,
The 82258 would work particularly well for high performance systems, in which peripherals tend to adversely affect system devices such as Winchester and floppy disk drives are tied directly to the workstation. The 82258 can support this variety of local and shared resources.

Fast devices are allocated to selector channels 0-2 of the 82258 because their performance depends upon fast transfer rates. Single-cycle transfers result in 8 Mbyte/sec bursts for one channel. Since both UNIX and XENIX systems heavily utilize the Winchester disk for code and data swapping, fast transfers are essential to system efficiency. However, if the DMA command block uses the verify or mask/compare features, the data rate will drop to 4 Mbytes/sec for two-cycle transfers.

Slower devices that generally require a lower burst rate are handled with the multiplexor channel. A combined data rate of 275 Kbytes/sec is supported by the multiplexor channel for single-byte or single-word transfers. This same data rate could also be achieved for a single subchannel burst. If each of the 32 subchannels maintained an asynchronous rate of 9600 baud (approx. 960 bytes/sec), only 23% of the 82258's channel capacity would be used. Consequently, selector channels would be able to obtain most of the chip's bandwidth.

The multiplexor channel will support all the user terminals of this multiuser workstation. In systems without a DMA controller, terminal I/O is typically handled through interrupts that signal the CPU that an external controller, such as the 8274, requires servicing. In its DMA mode, the 8274 will issue separate requests for transmitting and receiving data. These requests are acknowledged with an encoding of the DACK signal from the 82258. By using individual requests, the DMA controller does not need to look at status information to determine which operation is requested. Consequently, the overhead involved in servicing requests is minimal.

An alternative approach to using two subchannels per CRT terminal is to use the single interrupt signal from the 8274 when it is in interrupt mode. The serial controller generates the single interrupt signal to request a transmit or a receive operation. To determine which operation is needed, the 82258 can read the status registers of the 8274 with a type 1 command. Using a type 2 command, the 82258 would then branch to the appropriate command block for the needed operation. Reading status information imposes overhead in manipulating the serial controller in interrupt mode, but it offers the advantage of using only one subchannel per terminal.

Because the 82258 uses 24-bit pointers to the data areas, it can address the same 16 Mbytes of memory and 64 Kbytes of I/O space that the 80286 can. The DMA controller, however, does not directly support virtual addressing of a processor running in protected mode. It performs its operations only with physical addresses that were translated by the 286 from virtual addresses. This is not a problem because the operating system kernel is responsible for checking all of the protection rules when command blocks are created. The kernel is the only software allowed to access the registers of the 82258. Therefore, the system will be secure even though the controller uses physical addresses.

Tight coupling between the DMA controller and the 80286 in local mode configuration saves space. Both the 82258 and

Figure 6: An 80286-based workstation provides an example of the benefits of using the 82258. Local mode gives a compact CPU-to-82258 interface while three selector channels and a multiplexor channel give fast service to a wide variety of resources. If channel 3 were not used as a multiplexor channel, it could be used as another selector channel.
Mini-MAP makes it practical to apply array processing to general-purpose scientific and engineering computing.

**Practical in terms of use:** Mini-MAP's compiler allows you to program the array processor directly in FORTRAN. An assembler, a linker, and a debugger are also part of the package. Plus you can use our library of over 250 highly optimized scientific subroutines.

**Practical in terms of throughput:** Because it is an array processor, Mini-MAP increases the computing speed of a mini or supermini computer as much as 10 to 100 times. Where it takes a typical minicomputer minutes to perform tasks such as image rotation, Mini-MAP reduces interactive response times to seconds. Your computer may require hours to perform each step of a trial-and-error-process such as simulation, but Mini-MAP, can zip through in mere minutes.

Mini-MAP is available as an economical, four-board set or as a packaged system. Now, with Mini-MAP, OEMs can offer their customers a better product at lower costs. Mini-MAP's low power demands, small size, and high reliability make the package extremely attractive. And end users will find our FORTRAN compiler and other software tools minimize program development costs.

Some practical things to know about Mini-MAP:
- 32-bit DEC™ floating point format
- Interfaces to DEC PDP-11, LSI-11, and VAX-11 series
- Up to 16 MBytes of data memory
- 1024 x 1024 2-D FFT in 8.8 seconds
- Extensive software tools plus dedicated applications assistance including training, convenient parts depots, and field service staff support our worldwide installations.

To find out how Mini-MAP can work for you, call toll free 1 800 325-3110.
the processor use the bus support components; the 82288 bus controller, a 82284 clock generator, the 8282 latches and the 8286 transceivers are shared. This local mode of operation regards the 82258 as a co-bus master with the 80262 using the HOLD/HOLDA arbitration protocol. When the DMA controller wants control of the bus, it asserts its HOLD signal. The CPU responds with a HOLDA signal which allows the 82258 to take control of the bus. When the 82258 releases the HOLD, the 80262 regains the bus after inactivating HOLDA.

Division of bus utilization between the 82258 and the 80262 can be optimized by manipulating the values of the GBR (General Burst Register) and the GDR (General Delay Register). The GBR specifies the maximum number of continuous bus cycles for which the controller can control the bus. The burst counter is decremented by one for every bus cycle that the 82258 controls the bus. When its value reaches zero, the controller releases the bus and starts decrementing the delay counter which gives the minimum number of clocks between burst accesses. When its value reaches zero, both the burst and delay counters get loaded from the GBR and GDR, allowing the 82258 to request the bus, again using the HOLD/HOLDA protocol. These registers and their associated counters give the user programmable control of the system bus loading and prevent the 80262 from being denied access to the bus.

With the advent of the 82258, functions such as error handling and retry attempts are possible on a DMA controller. The command blocks that control the 82258 are prepared exclusively by the kernel of the operating system. The kernel builds the appropriate sequence of type 1 and type 2 commands in a memory area, then writes the starting address value of the command block to the CPR (Command Pointer Register) at the address at which the on-chip register is mapped. When a start channel command is then written to the CCR (Channel Command Register), the 82258 will wait for a DREQ signal if it is synchronized externally, or immediately begin execution of the command block if synchronized internally. Each channel and subchannel may use a separate command program.

A read from the Winchester disk illustrates how command chaining can be implemented to perform operations normally handled by the 80262 (Figure 7). Given a read command and its associated cylinder and head numbers, the 82062 Winchester controller retrieves data from the disk and puts it in an external sector buffer. The 82258 is then responsible for moving the data between the controller buffer and system memory. Before the transfer to system memory can be done, the DMA controller will check that no error was detected by the 80262 and that the data header matches what is expected. If there was an error in the disk controller operation, DMA execution stops. A mismatch between the header and the expected string results in the data still being transferred, but the MHeader variable is loaded with a value of all hex Fs. When the CPU receives the EOD interrupt from the 82258 signaling that the DMA was completed, it will be able to look at the status register, the CPR, and the value of MHeader to determine the cause of the DMA termination. Without command chaining, this complete read function would not be possible.

In the Winchester read operation, data could be used for the setup of a hardware prototype test board. The first section of the data sector describes the test parameters which the CPU uses to initialize the test vehicle. The two data blocks that follow the test parameters are actually manipulated by the test board and occupy noncontiguous addresses. Data chaining allows the data transfer to be specified with one command block, making efficient use of the control space. An alternative to data chaining is to use command chaining to simulate the function of a data list. However, this technique uses more space and requires more linking time than data chaining. List and linked-list data chaining provide an efficient and versatile method of scattering and gathering data.

Two variations of the standard transfer are shown in the disk reading example: transfers without a source and transfers without a destination. If specified in the type 1 command, the 82258 will take the value of the low byte or word of the source pointer and use it as a literal value which it will transfer to every destination byte, useful when initializing a data block to a particular constant. To read (not transfer) the value of a single byte or word, the type 1 command indicates that no destination is used. The data actually goes to the internal data assembly register (DAR) where a comparison can be made on it.

**I/O On A Chip**

As 80268-based systems increase in performance, corresponding I/O management capabilities are needed to support their performance. Jointly defined by Intel and Siemens, the 82258 is the result of an attempt to meet these requirements on a single chip. The 82258 provides 80268 and other iAPX 86 CPU systems a large bandwidth supported by its maximum transfer rate of 8 Mbytes/sec. Its four channels and unique multiplexor channel also allow systems to interface with a large number of I/O devices.

![Diagram](image-url)
NEW
intelligent
PC
ENHANCER

Now your operators and machines can speak the same language...
...plain English

256 messages your Programmable Controller couldn’t put into words…until now!

Adds operator prompting and diagnostics to your PC…at a very low cost.

Your equipment operators don’t speak in output codes. But your programmable controller does.

Bridge this communications gap with our Intelligent PC Enhancer (W424-4040). It stores 8,000 characters total—enough for 256 messages of 32 characters each. Displays them in English.

No more wasted time looking up code numbers or searching for the source of equipment shut-down.

Four lines totaling 96 alphanumeric characters appear instantly. These ½” high bright orange neon 14 segment characters are easily seen under any industrial lighting conditions. They get the operator’s attention fast! Even in direct sunlight.

Cherry’s Intelligent PC Enhancer spells out canned messages, system fault signals, production data, warnings and diagnostics. Features a visual cursor. A flashing mode to attract attention. A real time clock and RS232 output for print statements. A scrolling mode for longer messages. Has full ASCII input and accepts logic levels from 5 to 24 volts. All in a housing with a NEMA 12 compatible bezel.

Call or write for a free 8-page instruction booklet…written in plain, simple English.

Or, say it in one line!

Cherry W424-105B, 24 characters in 1 line accepts serial and parallel ASCII.

Cherry W424-105D, 24 characters, has all the great features of the W424-4040 in a single line.
NEW PRODUCT FOCUS
SYSTEMS

First Hardware Accelerator For Spice Program

MicroSim Corp. (Tustin, CA) has developed the PSpice Turbine, the first accelerator designed for one of the Spice circuit simulators. With the Turbine, PSpice runs the same speed as Spice on a VAX 11/780 (with the floating point accelerator). This performance level significantly reduces expenses required for time sharing.

Housed in a standalone chassis about the same size as the IBM PC chassis, the Turbine interfaces to the PC through an interface card that plugs into a short slot in the backplane. A 6' ribbon cable in turn connects the card to the Turbine. With the exception of distortion (DISTO) analysis, PSpice offers all the capabilities of Spice. When using the Turbine, all PSpice features are available, including the User-Changeable Models option which allows a user to customize device equations through access to Fortran source code. Another option, the Probe graphics postprocessor, supports the IBM color graphics adapter, the Hercules graphic adapter, the Okidata ML92 and ML93 printers and the Epson FX-80 and FX-100 printers. The current maximum circuit size when using the Turbine is 200 transistors.

Self-test diagnostics are performed whenever the Turbine is powered up. Upon failure, the faulty board will be bypassed, and the Turbine will continue to run at a slightly slower speed. The defective board can then be replaced at any time. The price for the PSpice Turbine (including the PSpice program and user’s manual) is $19,500.

— Lamneck
Circle 230

SOFTWARE

Software Converts Fortran Programs To C

As the number of UNIX and C users increases, there is a trend to standardize the programming environment to support C and its utilities. A common problem has been the transition from one language to another. A major investment in programs written in other languages such as Fortran creates a problem: Should the programs be translated or should new programs be written from scratch? Although it has difficulty handling large programs, Fortrix-C from Rapidtech (New York, NY) offers a solution to this common problem by transforming Fortran programs and files to C.

The operation of Fortrix-C is based on query. After asking for information about the program, such as whether it is a main program or subroutine, the program accepts the Fortran program line-by-line. A well-commented Fortran code will still retain its original comments into the C program. This process makes comparing code easy to debug and modify. The process of conversion involves parsing each line, identifying its function, determining the best approach for converting and generating the C function.

Configured to meet the requirements of the UNIX environment, the package includes integer to string converters, space allocation and string parsers. All control statements, such as Do, Goto, If Else and Continue, are converted to the equivalent of C instructions and program format. Fortrix-C takes all functions and subroutines and recasts them as C functions. Dummy variables within the functions are identified by address so that variables may be passed between the program called and the calling program. All format statements are made into a separate file. This produces a modified Fortran-like file for processing. Fortrix-C also separates all Implicit, Common, and Equivalence statements and declarations into intermediate files. Warning statements and queries of ambiguity are created during conversion. Error validation is incorporated because of the parsing process. Several types of errors are trapped and flagged with diagnostic constructions for debugging.

The C code produced by Fortrix-C is longer than Fortran when converting I/O calls. The loadable module occupies about 35% less disk space because Fortran does not show all of its I/O processing in its source code. Rapidtech claims the resulting C program runs about 15%-30% faster than its Fortran equivalent and transfer rate is 600 lines/min.

Fortrix-C requires a good understanding of Fortran and is available in three versions: -C, -C+ and C. The -C version is standard. The C+ version includes the ability to handle Common and Equivalence statements and provides for character and I/O control. The C is all of the above for a non-UNIX system. The program is available in either disk or tape format.

—MacNicol
Circle 234
"It's easy to spot the difference between our IBM PC-based frame grabber and the others."

High performance and affordable cost, just $1495 for a single plug-in board.

Unlike other video I/O systems, the new DT2803 provides real-time image capture capabilities, digitizing a 6-bit video field every 1/30 second. An on-board, memory-mapped, dual-ported frame store memory (256 × 256 × 8) makes it ideal for the IBM PC's 64K buffer size. And for real number crunching, the DT2803's external ports interface to high speed co-processors.

With our software package, VIDEOLAB™, the DT2803 is easy to use for image operations like averages, histograms, and convolutions.

So, if your application is manufacturing/automatic inspection, robotics, or medical research, our new high performance video I/O board will really open your eyes – at an unbeatable price.

Call (617) 481-3700

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646.
In Canada: (416) 625-1907.

IBM PC is a registered trademark of IBM. VIDEOLAB is a registered trademark of Data Translation, Inc.

Circle 14 on Reader Inquiry Card
**Ink-Jet Printer Combines Color Printing And Graphics Processing**

Described for use as a shared resource, Digital Equipment Corp.'s (Maynard, MA) LCP01 ink-jet color graphics printer produces color output on both paper and transparencies. It contains an integral on-board J-11 graphics processor that handles the display file processing of REGIS, GIDIS, NAPLPS or Color Sixel formatted data and a page buffer memory that takes the burden of the graphics processing off the host system.

Working with the VAX, PDP-11 and Professional 350 computers, the printer connects to the host CPU by a standard serial-line interface (RS-232-C or 20 mA). With a print resolution of 154 dots per inch, the LCP01 produces eight true colors (yellow, magenta, cyan, red, blue, green, black and white) in up to 216 combinations and shades. Print image resolution is $1536 \times 1152$ dots (maximum).

Hard copy graphics are produced in approximately two minutes per copy on A or A4 size paper. The printer feeds, processes and stacks 100 sheets of paper or 50 transparencies automatically; transparencies are completely dry when taken off the printer. The LCP01 also features self-test diagnostics.

The LCP01 is compatible with PRO/GIDIS (Graphics Interface Descriptor Instruction Set); DECSlide, a menu-driven text and diagram-generating tool; DECgraph, an interactive business graphing tool that generates six different types of graphs; and Datatrieve office software. Price for the printer is $14,595.

—Lamneck

**Controller Sustains 8.1 Mbyte/sec Data Rate**

The Concept 21 from Storage Concepts (Costa Mesa, CA) represents the first off-the-shelf disk subsystem to support a sustained transfer rate of 8.1 Mbytes/sec for the M2350 parallel transfer disk drive from Fujitsu America (Santa Clara, CA). Intended to support the real-time needs of such applications as image processing and satellite communications, the controller also handles burst transfers as high as 9.3 Mbytes/sec when all five of the disk drive's read/write channels operate at their 1.86 Mbyte/sec peak transfer rate. Previous implementations required several disk drives and several disk controllers to achieve multichannel operation.

Central to the design of the disk controller is a 80 word by 16 byte FIFO that buffers the data being transferred from the disk for easy handling by the dedicated processor. As a result, sustained or burst data transfers occur even during track-to-track seek operations. Furthermore, the Concept 21 formats disk surfaces (20 in all) in such a way that data transfers continue after one-half of a disk revolution rather than a full revolution. By staggering the zero logical sector from cylinder to cylinder, track-to-track seek times are minimized as each succeeding cylinder is at a minimum physical distance away from the next zero logical sector.

Users can also access the disk drive's 474 Mbyte storage capacity in a single-channel mode for data transfers to the host computer requiring less than the full data transfer speed. The controller uses separate buses for commands taken from the host CPU and the actual transfer to the dedicated processor. The host adaptor communicates with the system bus at a rate of 1.8 Mbytes/sec, with the high-speed port operating at 8 Mbytes/sec. As a result, high-speed transfers incur no overhead on the host system bus once the command has been issued.

The Concept 21 follows error correcting code and data and cycle redundancy check on headers in both system disk and data disk operating modes. Layered error handling and sector skipping specifications have been defined with an emphasis on five channel operation.

No extensive modifications of existing device drivers are needed other than a small device driver that links its 50-pin data and command bus to the host adaptor. The commands that need to be implemented are limited to diagnostics and maintenance (e.g., format bad sector), head positioning while seeking and read/write operations in single channel and five-channel modes. In addition, the controller can support as many as four parallel-transfer disk drives.

—Aseo

**PERIPHERALS**
THE GATE TO A SMARTER STD BUS.

STD BUS has always been a smart choice for flexible, cost-effective Z80® systems. And now, Mostek has made it smarter still. By adding a proprietary gate array to provide more intelligence to your system.

Our family of intelligent STD boards all feature a Z80 processor, DMA controller and on-board memory. And our custom gate array, which took three man years to develop. But that's where the similarity ends. Because we've provided different features on each board to make sure you get the best possible performance from each.

For example, we've got intelligent serial boards for short (250 feet) and long (1 mile) communication distances. We have another that implements the IEEE 488 General Purpose Interface Bus standard with speeds up to 300 Kbytes/second. And an IPIO with 32-bits of parallel I/O, suitable for high-speed control and data transfer.

The point is, Mostek designed these to be the most sophisticated STD BUS boards available today. Which is one more way in which we show our continuing commitment to STD BUS.

So to give your system some extra smarts, contact Mostek Corp., 1215 W. Crosby Road, MS1051, Carrollton, Texas 75006, or call 1-800-635-0200. In Texas, 1-214-466-8801. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5.681.157-9.

Z80 is a registered trademark of Zilog, Inc.
Graphics Boards Support Video Applications

Two of the four new video support graphics boards from Cromemco.

The computer graphics marketplace is becoming more diverse and segmented because generic graphics hardware cannot do all things for all users. Video is an important and sometimes overlooked segment of this market. The hardware for video systems represents different architectural concerns. The resolution of a video-oriented system is fixed below 525 lines, and the importance of colors, frame capture, signal quality, speed and versatility is higher and different than with CAD systems.

Two board manufacturers recently introduced products supporting video functions: Cromemco (Mountain View, CA) and Parallax (Sunnyvale, CA). Cromemco has four new boards that use the S-100 bus which, combined with their SDD digitizer board, forms the company's S-series of graphics interface boards. The four boards, which support either NTSC (National Television Standards Committee) or PAL standards of video transmission, are a video generator, a video memory controller, 256K of dual-port memory and a color modulator board. Together the boards provide a 256K color palette with image overlaying, full color digitizing, 4-1 continuous zoom, panning and scrolling and image wrap-around.

The video generator and memory controller work together to form the basic system that generates a 756 x 484 pixel display from a 1024 x 1024 image space. Three memory controller boards can be combined for independent zooms and pans. The dual-ported memory allows access or update of the image by the CPU or DMA device, and up to six can be used simultaneously. The importance of dual-ported memory means that the display board can be accessing memory while the CPU may be modifying the data. The net result is higher speed of operation.

The modulator board takes the RGB signals from the video generator board or another source and converts it to a professional quality composite signal.

Each graphic memory board holds 512 x 1024 4-bit nibbles or image space. If two boards are used, either a 1024 x 1024 x 4-bit or a 512 x 1024 x 8-bit image can be stored. Four boards can store a full 1024 x 1024 image with the capability of displaying 256 simultaneous colors. The digitizer board of S-series is capable of accepting a color camera or VCR input and outputs an RGB signal for computer manipulation, display or special function device. Together, the system is capable of creating special effects, interactive graphics for training, pattern recognition and simulation.

The video board from Parallax is actually an extension of their 600 series of their Multibus-based graphics display system. The board is designed for real-time video digitization in a professional environment. The video circuitry resides on the 600-8 which is an add-on board. It makes the standard 16 color board (600-4) into a 256 color (8 bits each for RGB) system.

The capabilities of the graphic display system allow NTSC signals to be an input or output. The NTSC input signal is decomposed into its RGB components and control of hue, saturation and contrast is adjustable via trim pots on the edge of the board. For black and white signals, a 6-bit gray scale is used. The color scaling is a mapping of 6 bits of RGB into 3 bits of R and G and 2 bits of B. The estimation of colors can be increased in apparent quality through hardware dithering. Dithering is the process of redistribution of colored pixels to increase the apparent depth of colors through the creation of mixed intermediate colors. One of the colors can be used as video for overlaying. The overlay generator is a 2:1 digital multiplexer that mixes the digitized video signal with the color map of the 600.

-Cromemco
-Circle 232
-Parallax
-Circle 233

The 600 series video/graphics controller from Parallax.
Shape The Future
Share The Pride

Pioneering has been our business since 1891. Today, we're still leading the way toward shaping the future of modern telecommunications. Digitalized switching and transmission systems, advanced integrated circuits, new dimensions in fiber optics... all assimilated to shape the direction of tomorrow by the professionals at GTE.

We are currently seeking degree-level candidates with 3+ years experience in the following areas.

TRANSMISSION SYSTEMS

Specify, design, document and test systems hardware. Projects will include PCM subscriber and high speed digital multiplex systems, ISDN projects, etc. Experience in designing digital multiplex products, switching circuits, PLLs, clock recovery circuits, diagnostics hardware, microprocessor interface circuits and/or line-trunk-service circuits. Exposure to semi-custom/custom integrated circuits extremely helpful.

BUSINESS SYSTEMS

Responsible for design and development work on PABXs, call processing, data collection and database systems for business communication products. Experience in hardware design, software systems and/or datacomms is preferred.

We invite you to share the pride with GTE by becoming part of tomorrow's telecommunication task force today! Please send your resume or letter of qualifications to the address listed below. We are an equal opportunity employer.

m/f/h/v.

GTE COMMUNICATION SYSTEMS
Human Resources Dept. 7120
2500 W. Utopia Road
Phoenix, AZ 85027

Communication Systems
Working Together To Be The Best
COMPUTERS/SYSTEMS

CAD Workstation For IC Layout

Powered by the Data General 32-bit DS/4000 CPU, the GDSII/32 workstation is linked to larger GDSII systems based on the DG Eclipse computer. The system includes 2 Mbytes of RAM, a hardware floating point accelerator, a 737 Kbyte floppy disk drive, a 15 Mbyte cartridge tape unit, two 5 1/4" Winchester disks with a total of 210 Mbytes and an integrated I/O controller board. The GDSII/32 also offers a graphics display terminal with $1024 \times 1280$ resolution, 60 Hz noninterlaced color monitor and 4-bit planes. Price is around $95,000. Calma, Santa Clara, CA

Supermicros With 16 Mbyte ECC RAM

Available with 4, 8 or 16 Mbytes of error-correcting RAM, the CS-400 Supermicrocomputer offers a choice of a 140 Mbyte or 280 Mbyte high speed hard disk drive, controlled by the STDC controller, with cache memory. The system comes with a standard 5 1/4" floppy disk drive (390 Kbytes) and a 32 Mbyte cartridge tape drive for backup. All models are delivered with UNIX System V installed and have a capacity of 21 boards. Cromemco, Mountain View, CA

Infrared Spectral Analyzer

Designed to make measurements from .7 to 20 microns, this dedicated spectral radiometer, Model SA-1 Infrared Spectral Analyzer, offers a choice of fields-of-view, spectral regions and detectors. Consisting of an optical head and electronics, the Model SA-1 can display either volts, irradiance, radiance or temperature for any spectral region. The standard instrument uses a 1 cm diameter collecting optics which gives the system a 2° field-of-view. Minarad Systems, Fairfield, CT

UNIX/Coprocessor Subsystem

Designed to convert an IBM PC to a 32-bit UNIX workstation, the Opus 516 Personal Mainframe consists of a complete port of UNIX System V (Release 2.0) and a 32-bit coprocessor for the IBM PC and plug-compatible computers. The coprocessor is based on National Semiconductor's Series 32000 chip set. With standard memory management and floating point processing capabilities, memory on the Opus 516 is expandable to 2 Mbytes. Also included are C and FORTRAN 77 compilers, an assembler and debugger. Price is $3,140. Opus Systems, Los Altos, CA

Raster Graphics Workstation

Introduced as an alternative to the IBM 5080 Graphics System, this raster graphics workstation, the 6080, is based on the "Ocean" graphics engine. The 6080 features a 50 nsec/pixel drawing speed, local pan/zoom/scroll and local highlighting techniques. Among the software packages that run with the 6080 are CADAM, CATIA, Integrated Prance CADAM (iPC); CBDS2, CAEDS, McAuto's Unigraphics and Precision Visuals' DI-3000. With 256 Kbytes of system memory, expandable to 1.25 Mbytes, the 6080 includes a 19" 1024 x 1024, 60 Hz noninterlaced display with antiglare screen. Prices range from under $18,000 to $22,000. Adage, Billerica, MA

XENIX 3.0-Based Multiuser System

Supporting up to four users with expansion available for up to eight users, this multiuser supermicro system uses Microsoft’s XENIX Release 3. The Esprit X16 implements a network-in-a-box architecture and uses terminals as user workstations. With an 8086 16-bit CPU, the X16 comes with 512 Kbytes of RAM standard and 13 offered with 40 Mbytes or 105 Mbytes of 5 1/4" Winchester disk storage. Providing a parallel printer port and an RS-232 serial port, the X16 offers an optional Multibus-compatible expansion chassis with six slots for Multibus-compatible boards. Price is $9,000. Esprit, Montgomeryville, PA

In-Circuit Programming System

Designed to program several boards at once and up to 32-bit-wide words in its standard configuration, the Z-2500 In-Circuit Memory Board Programming System is a disk-based bench-top, programmer. Housed in a 1/4" thick aluminum chassis containing a 125W switcher, two 8" double-sided, double-density disk drives, 64K RAM and a Z80A-based computer, the system is self-calibrating, using a built-in .05% reference. Sunrise Electronics, Glendora, CA

IBM PC Data Acquisition/Control Signal Conditioning System

The Analog SC Series of rack mounted signal conditioning products includes a variety of modular plug-in input and output capabilities for direct conditioning of thermocouples, RTDs, Strain Gages, mV Frequency and 4-20 mA process signals. SC backplanes are designed to accept direct sensor input and provide cold junction compensation for thermocouples and excitation voltages for 2-, 3- or 4-wire RTDs and strain gages. All analog SC modules are fully isolated to ±1500 VDC and operate over a -25°C to 85°C range. Cyborg, Newton, MA
THE VQ-11 SERIES...  
GET THE Q-BUS SYSTEM PACKAGE THAT YOU WANT
CUSTOM OR STANDARD — ZOLTECH DELIVERS

BUY IT COMPLETE
• CPU: 11/23, 11/73, 68000, MicroVAX
• MEMORY: Up to 4 million bytes
• MASS STORAGE: Virtually any combination of removable and fixed devices including 5" and 8" floppies, Winchester and tape. Capacities to 190mb. Emulations from TU58 to MSCP.
• SERIAL I/O: DL, DZ, DH, and DHV
• SPECIAL PURPOSE: Analog I/O, graphics, array processors, counter-timers...
• SOFTWARE: Single or multi-user, utility, development, and application.

Your exact configuration!

BUILD IT YOURSELF
• VQ-11/Model 30: The INTEGRATED system chassis includes 8x4 Q-22 card cage, quad-output power supply, full control panel, superior cooling, mounting hardware and power wiring for mass storage devices and a rear I/O connector panel that is compatible with, but more flexible than, the DEC Micro/PDP-11. Rack-mount, "Tower," and desktop enclosures are available.
• VQ-11/Model 20: The CARD CAGE ONLY chassis — based on the Model 30, but does not provide for internal mass storage.
• VQ-11/Model 16: MASS STORAGE SUBSYSTEM chassis — based on the Model 30, but does not provide for an internal card cage.
• VQ-11/Model 11: The MINIMUM system chassis — includes only the empty metal shell of the Model 30 and the AC power input components.

Just the components that you need!

Zoltech manufactures a variety of systems and other Q-Bus related components. The VQ-11 system packages are designed to maximize reliability and versatility while minimizing cost and lead time. Call or write today for a quote or for our catalog of system packages, boards, drives, software and accessories available for your Q-Bus needs.

Call or write today
ZOLTECH CORPORATION
7023 Valjean Avenue, Van Nuys, California 91406 USA
(818) 780-1800 Telex 755451
Representative and dealer inquiries are invited.

Circle 12 on Reader Inquiry Card
**The Art of Image Engineering**

**A Case Study**

**Customer:**
The machine tool division of a Fortune 100 Company with a reputation for leadership in industrial inspection.

**Solution:**
The Digital Graphic Systems 1611 with its onboard 8086 image processor, associated firmware and optional frame grabber.

**Result:**
The market introduction of a reliable high-speed multitasking image processing system — of industrial quality — for industrial environments.

---

**Enhanced Supermini**

Enhanced to support up to 16 Megabytes of directly addressable memory, the Model 3210 superminicomputer is part of Perkin-Elmer's Series 3200 family. Using the firm's OS/32 operating system, the Model 3210 runs all PE languages including its Fortran VII family, Pascal, COBOL, Basic and Coral 66. The XELOS operating system, a derivative of AT&T's UNIX System V, is also available for the Model 3210. Other members of the PE Series 3200 family of superminis include the 3205, the 3230, the 3250XP and the 3200MPS. Perkin-Elmer, Oceanport, NJ

Circle 218

---

**Data Reduction and Analysis.**

**Publication Quality Graphics.**

**Image Processing.**

**IDL software integrates it all**

- Compatible with VAX/VMS™ computer systems, most graphic terminals and image display systems
- Lets you see your data at every step
- Allows immediate interactive compilation and execution
- Vector and array operators for powerful interactive capabilities

Quickly transform your raw data into results using IDL's advanced features, including: Statistical Analysis, Interpolation, Smoothing, Curve Fitting, Data Editing, Modeling, Interactive Graphics, Image Processing Display and Analysis.

To receive our informative IDL brochure call or write:

RESEARCH SYSTEMS, INC.
2021 Alton St. Denver CO 80207 (303) 399-1326

Circle 71 on Reader Inquiry Card

---

**New Products**

**Enhanced Supermini**

An enhanced version of the company's MV/1000 supermini, the Eclipse MV/10000 SX superminicomputer is based on a single-board processor that uses ECL macrocell microcircuitry developed by Motorola. Also announced are 256 Kbyte DRAM-based memory boards (4 and 8 Megabytes) that enhance the maximum configurability of the Eclipse MV/10000 SX to 32 Megabytes. The coprocessor has a dedicated control store and microsequencer to store and execute its own 115-line microcode instruction set.

Data General, Westboro, MA

Circle 158

---

**Briefcase-Size PC**

The latest addition to the TI PC family, the Pro-Lite computer features a 12" LCD that shows 80 columns x 25 lines. With up to 768 Kbytes of RAM, the Pro-Lite can accommodate software packages like Ashton-Tate's framework. The entry-level configuration includes 256 Kbytes of memory, a 16-bit 80C88 CPU, with an 80C87 numeric coprocessor available as an option. The 10.5 lb Pro-Lite has a single, 3½" floppy drive; diskette storage capacity is 720 Kbytes. A second disk drive and a battery pack can be added and an optional 300 baud modem is also available. Price is $2,995.

Texas Instruments, Dallas, TX

Circle 217
Can you picture a single-board PC graphics controller with 32-bit planes?

The New REVOLUTION™ 512 x 32.

We built a combination of advanced capabilities into the latest Revolution board...like our unique megabyte of multi-ported display memory, 16 million colors with overlay capabilities, hardware zoom and optional video broadcast compatibility. The kind of architecture you'd like to specify for your system needs.

Our single-board design won't tie up the PC's expansion slots and power supply. And you can update the screen with uninterrupted bus access to our memory-mapped display buffer. A feature that gives you speed and programming versatility with a minimum of effort.

Compare our specs and prices and you'll see why Revolution graphics controllers are a part of the most advanced and competitively-priced PC design systems available today. Not tomorrow. Not someday.


It's here.
VMEmbus makes all the difference when backed by Schroff.

Available from stock
a totally integrated subrack system
conforming to IEC 297-1/3/-3A,
DIN 41494 and the forthcoming
IEEE specification.

VME Backplanes J1, 5/9 and 20 slot
VME Backplanes J2, 5/9 slot
VME Test Adaptors · Power Supplies
DIN/IEC Connectors · WW Boards
Prototype Boards
Desk Cases · Waterproof Cases
Cabinets

The precision, ruggedness,
versatility, elegance
and power of the Schroff
VMEmbus product range

For the facts ask the experts.
Enquire now for your VME Products Brochure
which includes details of our Special
Test Package Offer.

Circle 52 on Reader Inquiry Card

Schroff Inc. · 170 Commerce Drive
Warwick, R.I. 02886 · Tel. (401) 732-3770
Telex 952175 · Telefax (401) 738-7988
Production and Distribution in the U.S.

Our Representative for Canada:
A.C. Simmonds + Sons Ltd.
975 Dillingham Road · Tel. (416) 8398041
Pickering Ontario L1W 3B2 · Tx 06981383
NEW PRODUCTS

PERIPHERALS

Compact Modems
Converting data for transmission over leased telephone lines between terminals and host computers, these modems (the 3833 and the 3834) operate at 2,400 bps and 4,800 bps in networks using sync data transmission. These shoebox size modems are fully compatible with IBM communication network management and problem determination programs. The units also include an extended diagnostic function which permits remote diagnostic tests. Price is $1,700 (3833) and $2,600 (3834). IBM, Rye Brook, NY Circle 169

Microterminal
Requiring only one host communications port or multidrop address, this Microterminal, the TM200, provides a data entry and display station with I/O capability. Internally, it consists of a logic board and a keyboard/display module. The 0.21" high 40-character green vacuum fluorescent display can be read from a distance of 10' in a variety of ambient light conditions. The display message, up to 80 characters long, can be scrolled bidirectionally. Burr-Brown, Tucson, AZ Circle 178

3½" Microfloppy Drives
Featuring a 3½" format, the YD-600 Microfloppy disk drives are offered in two models: the YD-620/25 providing 0.5 Mbyte on 80 tracks and the YD-640/45 with 1.0 Mbyte double-sided storage on 160 tracks. The drives are interface-compatible with most 5¼" drives and consume 3W power. With MTBF of 10,000 POH, transfer rate for both models is 250 Kbits/sec. The YD-620/25 has a 5 msec track-to-track access time and a track density of 67.5 tpi with an 8547 bpi recording density. The YD-640/45 has a 3 msec track-to-track access time and a track density of 135 tpi with an 8717 bpi. C. Itoh, Los Angeles, CA Circle 213
LEADERSHIP!

Maxi-Switch is out front in keyboard technology

Have you taken a close look at Maxi-Switch lately? We're the company that introduced conductive elastomer keyboard technology in 1981. Maxi design leadership is proven on the job, every day, in thousands of terminals and personal computers.

Our conductive elastomer switch features "Maxi-Touch," with unique tactile response. It's rated at over 50 million cycles. Typists appreciate the comfortable low-profile design and smooth key action. Engineers appreciate the new technology, its simplicity and long life.

This keyboard is offered in an IBM PC format for OEM customers, and with a matching enclosure, cable and connector for PC and PC-XT keyboard replacement. Users can choose the standard keytop layout, an enhanced version, or the increasingly popular Dvorak format.

Apply Maxi's conductive elastomer keyboard technology to your keyboard problems. Call the Leader for price and delivery.

Enhanced version, 8500 Series Keyboard.

See us at

COMDEX Spring '85
May 6-9, 1985
Atlanta Apparel Mart,
Atlanta, Georgia

THE MAXI-SWITCH CO.
9697 EAST RIVER ROAD • MINNEAPOLIS, MINNESOTA 55433
(612) 755-7660
TWX 910-576-2690

Circle 45 on Reader Inquiry Card
NEW PRODUCTS

50 MHz Pattern Generators

Used as standalone stimulation sources or linked with data acquisition to provide a test system for debugging and verifying components, boards and systems, these pattern generation modules (91S16 and 91S32) operate at up to 50 MHz. The 91S16 module features 16 data channels of algorithmic pattern generation along with two strobes and two clocks. The 91S32 offers 32 data channels (stored pattern generation), four strobes and four clocks. Prices are $6,900 (91S16) and $10,400 (91S32). Tektronix, Beaverton, OR Circle 159

Full-Function Industrial Computer

Designed for mid- to upper-range industrial automation applications, this mid-range dedicated computer, the 984 Programmable Controller (PC), offers options for machine diagnostics and arithmetic equations. Communications capabilities include three built-in ports that allow two users to extract information from the PC through host computers. The 984 also incorporates a tamper-proof memory, bit slice technology and a handheld data access panel. Price, with 16 Kbytes memory, is $6,200. Gould, Rolling Meadows, IL Circle 155

Data Acquisition/Control System

This data acquisition system (Model 1150) collects analog and digital data, compares it with previously programmed limits, generates control actions based on the comparisons and reports the collected data and control actions over the IEEE-488 GPIB. A GPIB system controller may be programmed to scan analog and digital signals to detect any out-of-limit states, at which time the system controller assumes control as necessary. Price is $1,895. Racal-Dana, Irvine, CA Circle 165

Database Hardware Sorter

Designed to offload a host's data sequencing overload and accelerator database set operations, the DBA 1000 Database Accelerator consists of a front-end processor, memory control unit and from one to five self-sorting memory modules. The front-end processor, incorporating the 80186 µP and multiported memory, communicates via Ethernet LAN with the host. Accell Technologies, San Diego, CA Circle 161

Full-Function Industrial Computer

Designed for mid- to upper-range industrial automation applications, this mid-range dedicated computer, the 984 Programmable Controller (PC), offers options for machine diagnostics and arithmetic equations. Communications capabilities include three built-in ports that allow two users to extract information from the PC through host computers. The 984 also incorporates a tamper-proof memory, bit slice technology and a handheld data access panel. Price, with 16 Kbytes memory, is $6,200. Gould, Rolling Meadows, IL Circle 155

Data Acquisition/Control System

This data acquisition system (Model 1150) collects analog and digital data, compares it with previously programmed limits, generates control actions based on the comparisons and reports the collected data and control actions over the IEEE-488 GPIB. A GPIB system controller may be programmed to scan analog and digital signals to detect any out-of-limit states, at which time the system controller assumes control as necessary. Price is $1,895. Racal-Dana, Irvine, CA Circle 165

Database Hardware Sorter

Designed to offload a host's data sequencing overload and accelerator database set operations, the DBA 1000 Database Accelerator consists of a front-end processor, memory control unit and from one to five self-sorting memory modules. The front-end processor, incorporating the 80186 µP and multiported memory, communicates via Ethernet LAN with the host. Accell Technologies, San Diego, CA Circle 161

UNSURPASSED SPEED
ANDROMEDA MM 22
QBUS 2MB MEMORY

■ Fast—30NS Access Time (Din to Reply) ■ Low Power— + 5V, 1.0 AMP ■ Memory Size Of 256KB, 512KB, 1MB, 2MB ■ Block Mode ■ Parity CSR ■ LSI—11 And Micro Vax Compatible ■ Competitively Priced ■ Available Now

QBus — Digital Equipment Corporation Trademark

ANDROMEDA SYSTEMS
9000 ETN AVENUE, CANOGA PARK, CALIFORNIA 91304 U.S.A.
(818) 709-7600
TWX 910-494-1248

Circle 76 on Reader Inquiry Card
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance. Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance. Without complex adjustment electronics, and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.

How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

The result: a triumph over the convergence factor. Find out what it can do for your next color terminal or monitor, and ask about our full line of quality color and monochrome CRTs. Write or call: Panasonic Industrial Company, Computer Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5278.

Panasonic Industrial Company

The achievement of Panasonic high resolution in-line color CRTs.
**NEW PRODUCTS**

**Portable Thermal Printer**

On ordinary or thermal paper, this thermal/thermal transfer portable printer, the TMP-21, prints 80 cpi with a 16 x 10 dot matrix. In the graphics mode it performs bit imaging with a 16 x 960 matrix. The TMP-21 prints at 30 cps and is capable of standard or enlarged 40 cpi printing. The battery-powered unit uses 4 C cells or an optional AC adapter. A standard parallel-Centronics interface or an optional RS-232 interface is available. Price is approx. $200. *Acroamatics*, Danbury, CT Circle 168

**Dot Matrix Printers**

These 3000 Series printers, offering speeds from 45 to 400 cps, are included in the Tempest product line. The 3184, 3304 and 3404 are among the new additions to the Tempest Series. Each model offers draft printing at speeds from 180 to 400 cps, letter quality printing from 45 to 100 cps and high resolution dot addressable graphics. Available options include fonts, eight color process printing and paper handling accessories. *Genicom*, Waynesboro, VA Circle 176

**GCR Tape Subsystem**

An addition to the firm's Shamrock GCR tape subsystem family, the Model 9270 Shamrock is a 75 ips start/stop, autoload/autothread vacuum column tape drive with embedded GCR formatter. Dual and tri-density models (6250/1600/800 bpi) are offered. The peak throughput rate at 6250 bpi is 468.7 Kbytes/sec. Fully compatible with the 9250, 50 ips start/stop tape drive family, the 9270 offers Pertec STC and Telex interfaces. The Price is $15,899. *Telex*, Tulsa, OK Circle 175

**1600-Line High-Resolution Video Camera/Monitor**

Achieving 1600-line resolution, this video camera, the Precision 81, features multirate scanning of up to 2048 lines, 40 MHz bandwidth, plug-in bandwidth filters and adjustable transfer characteristics. Also announced is the HR-2000 solid-state Video Monitor that offers 2000 TV lines of resolution. Features of the HR-2000 include auto-locking to multiple scan rates, 50 MHz bandwidth, differential inputs, variable video enhancement, selectable A-B video input and separate data input channel. *Dage/MTI*, Michigan City, IN Circle 194

**Internal Hard Disk Drive For PC/AT**

Designed to be housed inside the IBM PC/AT, this 30 Mbyte hard disk drive (StorageMaster 630) has a typical access time of approximately 30 msec. Two storageMaster 630 Winchester drives can be housed side by side in the PC/AT processor cabinet and operate with the resident PC/AT disk controller. Each drive comes with an adaptive software diskette that allows users to operate the drive with standard PC DOS Version 3. Price for the StorageMaster 630 is $2,145. *Control Data*, Minneapolis, MN Circle 174

**UNSURPASSED FLEXIBILITY ANDROMEDA UDC 11 MSCP DISK CONTROLLER**

- Controls any combination of a Winchester Cartridge, and Floppy Drives
- Rx50 Floppy Compatible
- St 506 Winchester Compatible
- MSCP (Mass Storage Control Protocol)
- Over 50% faster than DEC RQDX1
- Block Mode DMA
- LSI 11 and Microvax Compatible
- Drive configurations stored in EE Rom for user convenience
- Available Now

LSI 11, Micro Vax, DEC, MSCP and QBus are Digital Equipment Corporation Trademarks
St 506 trademark of Seagate Technology

**ANDROMEDA SYSTEMS**

9000 ETON AVENUE, CANOGA PARK, CALIFORNIA 91304 U.S.A.
(818) 709-7600
TWX:910-494-1248

Circle 67 on Reader Inquiry Card
Prime Time Reading

Upcoming Editorial Preview

To provide you with the most balanced design coverage in the industry, each month DIGITAL DESIGN will cover four major technology areas: Systems Architecture, Electronic Imaging, Semiconductor Technology, and Design Technology. It's reading you won't want to miss!

JUNE

- Speech Recognition — Systems Architecture
- Robotic Vision Systems — Electronic Imaging
- CMOS — Semiconductor Technology
- Microprocessor Development Systems — Design Technology

JULY

- Floppy Drives, High Level Languages — Systems Architecture
- Array Processors, Graphics Processors — Electronic Imaging
- EPROMS/EEPROMS — Semiconductor Technology
- Logic Simulation — Design Technology

AUGUST

- Printers/Plotters — Systems Architecture
- High Resolution Graphics Boards — Electronic Imaging
- Digital Signal Processors — Semiconductor Technology
- Standard Cells — Design Technology
Simpact Solves Your DEC Communications Problem!

We started with DEC's MICRO/T-11 16-bit PDP-11 microprocessor so you can use your host's software development tools to write programs using the familiar PDP-11 instruction set.

Then we married the MICRO/T-11 to multiple Z8030 Serial Communications Controllers to create a family of front-end processors that can support nearly all serial protocols, standard or custom.

All ports on our FEPs are individually programmable for baud rates, synchronous and asynchronous protocols, RS-232C, RS-449 (RS-422, RS-423), MIL-188C and MIL-188-114.

We also built in 22-bit hardware memory management so you can download sophisticated application tasks and still have plenty of room for data storage.

Finally, we added firmware for boot loading, self-test diagnostics, and program debugging. But the hardware is only half the story...

**Powerful Package of Software Tools**

Because we understand what it takes to develop and support a communications system, we created a software toolkit to make our family of FEPs easy to use. Starting with our proven, memory-resident Real-Time Executive, we added a sysgen program to develop down-loadable, runtime images. We also designed efficient drivers for RSX and VMS operating systems so host applications programs can easily talk to our FEPs with simple QIO calls. To help you get started with your project we provide complete software documentation and hands-on training classes.

**Standard Protocol Software**

We can also provide turnkey packages for Telenet certified X.25 LAPB protocol software (CCITT 1980, Levels 1, 2, and 3) and HDLC (LAPB) frame and link level software. More standard protocols are on the way.

For the **UNIBUS**
Model ICP1600:
Eight fully programmable comm ports
256K RAM, DMA transfers to host
Single hex-height card
Up to eight ICP1600s per UNIBUS
$4975. (single quantity)

For the **Q-BUS**
Model ICP1622V:
Four fully programmable comm ports
128K dual ported RAM
Single quad-height card
Up to eight ICP1622s per Q-BUS
$3000. (single quantity)

**Port Expander**, Model EXC1612:
Gives the ICP1600 or the ICP1622V twelve additional programmable RS-232C comm ports
Optional DMA capability for two ports
Single quad-height module for UNIBUS or Q-BUS
$2400. (single quantity)

**Software Toolkit**
Model QX100:
For RSX or VMS operating systems
Includes Training Class
$5000. (one time charge)

Let us solve your DEC communications problem. Call us today at (619) 565-1865.
NEW PRODUCTS

**Touchscreen Development Kit**

Developed for the firm's Touchscreen, this Engineering Development and Evaluation Kit is comprised of a 9", 12" or 13" neutral-density analog-contoured touchscreen, a controller interface, demonstration programs, design manual, connectors and mounting adhesives. The Touchscreen is a transparent resistive touchsensor that achieves 4096 x 4096 screen resolution and 1% linearity. Price for the kit is $2,400. **Dorman Borgdnoff**, Andover, MA

**Intel chose Mupac to develop a packaging system for their NEW Multibus II.**

*Here's why:*

Intel liked the systems approach of our standard packaging hardware. It's modular, it's flexible and it's designed to work as one integrated system to solve your special packaging needs.

This same approach is used with Multibus compatible packaging, making Mupac the ideal choice for your Multibus packaging requirements.

Our system is flexible, compact and reliable. It can handle from 2 to 26 panels in easy to use modular increments. Features include panel guides on .60 and .75 inch centers, a backplane designed to eliminate crosstalk and noise, terminated bus lines and provisions for parallel priority. Look to Mupac for the same reasons that Intel chose us to develop a packaging system for Multibus II. We're FIRST with multiple solutions to Multibus compatible packaging.

*Multibus is a registered trademark of Intel Corporation.*

**14,400 BPS Trellis-Coded Modem**

An addition to the fixed line of modems, the M1926L 14,400 bps Trellis-coded modem is a standalone unit for use on four-wire leased lines. It can also operate at fallback speeds of 9600, 7200 or 4800 bps in compliance with CCITT V.29. A built-in six-channel multiplexer allows up to six 2400 bps channels to be transmitted simultaneously over a single based telephone line. The M1926L has an automatic adaptive equalizer that can bridge dropouts of up to two seconds. Price is $6,875. **Fujitsu America**, San Jose, CA

**Video Color System**

Designed to record and replay pictures in slow motion, this high speed Video Color System can be used for time-study. A rotary shutter changes the normal 1/60/sec exposure rate of video cameras to 1/1,000/sec and up to 1/10,000/sec. Every color picture, with time and date recorded on it, can be moved to any part of the picture. Every tape can hold 324,000 pictures. All 60 pictures/sec, as recorded, can be seen in sequence at any playback speed. **Sun Vision**, Waukesha, WI

**MAY 1985**

*DIGITAL DESIGN*
Tap into the world's most fertile market of over a billion people. Set up your own factory, your own wage scale, your own worker incentives. Hire hard-working, pragmatic, proud and frugal people. Bring along your technology, your marketing capability and your capital.

This is the new policy of an enlightened People's Republic of China under its "Open Cities" program. It means that United States businessmen now may run their own enterprises, or joint venture with Chinese counterparts if they prefer—without government interference. This incredibly successful program has already resulted in forty-two new enterprises and seventeen joint ventures.

We can bring you together with the right people—without bureaucratic drag—without lengthy negotiations. You'll deal with decision makers, who have full authority to act. As official representatives under contract to the Government of the People's Republic of China, we are empowered to arrange direct negotiations between principals.

Invite us to send you information about our service. It will include the list of over 100 manufacturing projects now being accepted under China's "Open Cities" program.

Address your inquiries to George Mattson, Director, Asian Operations.

The Allan R. Hackel Organization Inc.
Established 1954

Advertising Agency Associates • AAA Media Management • AAA Asset Management
Box 69, 1330 Centre Street, Newton Center, Massachusetts 02159 (617) 965-4400

Circle 66 on Reader Inquiry Card
NEW PRODUCTS

COMPONENTS

On-Chip Address Latching For CHMOS EPROMs

An enhanced version of the 27C64 CHMOS EPROM, this 64-Kbit CHMOS EPROM (87C64) contains the interface circuitry required to connect it with Intel CHMOS microcontrollers and µPs, thereby reducing chip count and eliminating the need for an external latch. Developed using the firm's CHMOS II-E process technology which uses epitaxial processing, the 87C64 has a maximum access speed of 200 nsec. In quantities of 10,000, the 87C64 sells for $14.70. Intel, Santa Clara, CA Circle 141

Plastic D/A Converters

Designed for digital audio, three new models of the PCM53 Series of plastic-packaged 16-bit monolithic D/A converters includes an internal zener voltage reference, a resistor ladder network, current switches and a fast-settling, low-noise output op amp. The Series now has two electrical grades: JP and KP. All offer 16-bit resolution, a 96-dB range and 16-bit monotonicity. Total bipolar drift and bipolar zero drift are typically ±25 ppm of FSR/C and ±4 ppm of FSR/C, respectively. Burr-Brown, Tucson, AZ Circle 191

ECL 1K RAMs

Designed for high speed scratch pad, control cache and buffer storage applications, these three RAM devices feature full on-chip address decoding, separate data inputs, noninverting data outputs and an active low write enable. The MCM-1042 is a 1024-bit Read/Write RAM with 256 words x 4-bit organization; the MCM10422L10 has a 7 nsec typical address access time (TAA) and 10 nsec max. A reduced speed version, the MCM10422L15, has a TAA of 15 nsec max. Motorola Semiconductor, Phoenix, AZ Circle 131

ALS-Equivalent CMOS Logic Family

This fully 54/74ALS-equivalent CMOS logic family, AHCT, will include approximately 150 part types, with the first 22 octals available now. AHCT devices provide 4 nsec typical gate delays and 3-state outputs with high drive current (IQL = 24mA at VOL = 0.5V) for direct bus interface. At 4.5V to 5.5V, the devices operate over the full commercial range of -40°C to +85°C and over the full military range of -55°C to +125°C. The first available devices include buffers and bus drivers, transceivers, flip-flops, latches, decoders/encoders and multiplexers/demultiplexers. Zytex, Sunnyvale, CA Circle 129

One-Time Programmable and Fast-Turn ROMs

Packaged in 24-pin plastic DIPs, the MCM68769 is an 8K x 8-bit MOS OTP ROM and the MCM68768 is an MOS 8K x 8-bit Fast-Turn ROM. Both devices are mutually compatible, TTL compatible and pin compatible with the MCM6876 UV EPROM and MCM68366 Mask Programmable ROM. Operating voltage range, using a single +5V power supply, is +4.5V to +5.5V. Operating temperature range is 0°C to +70°C with power supply current at 85 mA max. Maximum access times from address are 300 nsec and 350 nsec. Maximum access time from Output Enable are 150 nsec and 120 nsec. Motorola, Austin, TX Circle 142

Double-Bit Error Checker/Corrector

An expansion of the firm's (DP8400) family of memory interface devices, the DP8400-2-16-bit Expandable Error Checker/Corrector contains a 16-bit detect/correct function in a 48-pin DIP. Word sizes can be expanded to 32 or 64 bits. When used with a 10 MHz CPU, the DP8400-2 allows for write cycles with no wait states and read cycles with one wait state in the always-correct mode. The DP8400-2 also features a bidirectional syndrome port and supports byte parity checking generation and correction. Price in 100s is $49.95. National Semiconductor, Santa Clara, CA Circle 132

Digital Logic Devices

Introduced as a pin-compatible licensed alternate source for Motorola's MECL10KH family, this family of 12 ECL devices (ECLI10KH) includes gates, multiplexers, latches and special function devices. Typical propagation delay for the ECLI10KH devices is 1 nsec with a max rise-and-fall time of 2.2 nsec (1.6 nsec typical). Power supply current for each device varies (lowest is 29 mA) and power dissipation averages 25 mW per gate. Housed in 16-pin ceramic or plastic DIPs, the ECLI10KH devices operate on a power supply of -5.2V, ±5%. Monolithic Memories, Santa Clara, CA Circle 137

256K DRAM Controller/Driver

Eliminating wait states, replacing discrete logic controllers for addressing and driving more than 2 Mbytes of DRAM, the DP8419 single-chip 256K DRAM Controller/Driver works with CPUs at 10 MHz or more. This ALS-type device offers on-chip DRAM address multiplexers, delay lines, on-board high-capacitance drivers and a refresh counter. With automatic refresh and access modes (1 and 5), the DP8419 drives 88 DRAMs (50 pf load) over the full temperature (0°C to +70°C) and operating supply range. The DP8419 is housed in a 48-pin DIP. National Semiconductor, Santa Clara, CA Circle 127

2-Micron MicroCMOS Gate Arrays

An expansion of the SCX6200 family of MicroCMOS gate arrays, the SCX6206 (6000 gates), the SCX6218 (1800 gates), the SCX6232 (3200 gates) and the SCX6244 (4400 gates) feature 2-micron drawn geometry with 1.4-micron effective channel length allowing sub-nsec gate delays. Allowing TTL and CMOS compatibility, outputs are selectable for 1, 2 or 4 mA drives. The SCX6200 Series features dedicated, multiplexed Dflip-flops incorporated into the internal array core, as well as built-in self-test circuitry. National Semiconductor, Santa Clara, CA Circle 143

12-Bit A/D Converter

Using CMOS and laser-trimmed bipolar die, the ADC674A is a 12-bit successive approximation A/D converter. With no missing codes over temperature (0°C to +75°C; -55°C to +125°C), the ADC674A is fully specified for operation from +5V and ±12V or ±15V supplies. Full scale and offset errors can be trimmed to zero externally. Internal scaling resistors provide selectable analog input signal ranges of 0 to +10V, 0 to +20V, ±5V and ±10V. Max conversion time is 15 µs (100s), while bus access time is 150 nsec. Price in 100s ranges from $39.25-$153. Burr-Brown, Tucson, AZ Circle 139
NEW PRODUCTS

New Gate Array Architecture

Using a new gate array architecture, this family of CMOS arrays, the P2L (Programmable Performance Logic), achieves standard cell gate densities while retaining gate array turnaround time. P2L provides programmable speed/power product of individual gates, the ability to incorporate ROM and PLA on the array and the ability to achieve high fan-in with one logic delay level. The P2L CMOS family is available in arrays up to 9000 gates in plastic and ceramic packaging.

Integrated Logic Systems, Colorado Springs, CO Circle 142

Bipolar Array

The FLEXX array offers both gate arrays and standard cells on the same chip. Using an oxide-isolated ISL process that provides typical per-gate propagation delay of 900 psec and allows designers to create application-specific designs of up to 2000 gates, the FLEXX array employs the "soft macro" structure. The initial FLEXX array ISL library consists of 50 soft macros developed to emulate 7400 TTL functions. A FLEXX array IC is capable of replacing up to 100 SSI and MSI logic ICs. Signetics, Sunnyvale, CA Circle 203

16-Bit A/D Converter

Achieving a 17 μsec maximum conversion time, the AD376 hybrid 16-bit A/D converter guarantees no missing codes to 14 bits over a 0°C to 70°C temperature range. Specified for operation with ±1V DC and +5V DC supplies, the converter typically consumes 1100 mW. Guaranteeing maximum linearity error of ± 0.006% FSR for the 1 grade, the AD376 accepts bipolar input signals of ± 2.5V, ± 5V, ± 10V and unipolar inputs of 0 to +5V, 0 to +10V and 0 to +20V. Prices in 100s are $189 and $219. Analog Devices, Norwood, MA Circle 198

64 Kbit PROM

Organized in 8K x 8 bits, the AM27S49 64 Kbit bipolar PROM is available in 40 nsec and 55 nsec commercial versions. This PROM incorporates three-state outputs and features platinum-silicide fuses. Produced in this firm's proprietary IXOM-S process, a scaled, ion-implanted, oxide-isolated bipolar process, the AM27S49 has applications in high-density microprogrammed control store memory. Housed in a 24-pin 600-mil ceramic package, the 55 nsec version is priced at $72.50 and the 40 nsec device is $108, each in 100s. AMD, Sunnyvale, CA Circle 200

Photomultiplier Tubes

Accurate and reliable, the XENIX-200 detector is designed for use in PC/AT compatible PCs. This photomultiplier tube is ideal for high-speed, high-resolution applications such as CT scanners, scientific instrumentation, and medical imaging. Consult the manufacturer for complete specifications and pricing information. XENIX, Sunnyvale, CA Circle 135

64K DRAMs For PC/AT Compatibles

Designed for use in PC/AT compatibles, the MSM3764A 64K DRAM is functionally compatible with its predecessor DRAMs; it is fully decoded and organized as 65,536 one-bit words. With 128 refresh cycles at 2 msec and noncritical clock timing requirements, the MSM3764A requires a single +5V supply with ±10% tolerance and is TTL compatible. Three access speed ranges are available: 120 nsec, 150 nsec and 200 nsec. Packaged in a 16-pin plastic DIP, the MSM3764A is priced according to range. Oki Semiconductor, Sunnyvale, CA Circle 197

DIGITAL DESIGN • MAY 1985
New Products

Linear Mosaic Arrays
Each semicustom chip in the FB300 Series of linear mosaics is composed of distinct component groupings that fit together like individual tiles, forming a mosaic. Each tile is treated like a mini chip designed so one or more macro cells fit on each one. Currently, a library of 24 macro cells are defined for the FB300 Series. The Series features transistors with 1 GHz ft and a dual layer metal for circuitry interconnection. The FB300 Series is supported by the firm’s CAD package, Linear CAD 1, which performs schematic capture and SPICE circuit simulation on the IBM PC and compatibles. Micro Linear, San Jose, CA

MOSFET Switching Power Supply
An addition to the firm’s “S” Series of MOSFET switching power supplies, this four-output, 175W unit features a 50 kHz switching frequency and built-in brownout protection. At outputs one through three, load regulation is 4% across the no-load to full-load range. At output four, the load is regulated ±4% over the same range. The unit reliability exceeds 78,000 hours MTBF on a demonstrated basis. NCR, Lake Mary, FL

Fiber Optic Lamps
Interfacing directly with fiber optic cables, assemblies and single fibers, these miniature Fiber Optic Lamps, the LI006 and L8006, form an intense spot of illumination at a distance of 1.0 mm from the tip of the lamp. The LI006 interfaces with single fibers of 10-500 microns in diameter and operates at 3.5V. Operating at 5.0V, the L8006 interfaces with larger size bundles and assemblies. Both are priced at $5-$6. Gilway Technical Lamp, Woburn, MA

DMA Controllers
Designed to support the M68000 MPU family, these DMA controllers (MC68440, MC68442 and MC68450) are directly compatible with the M68000 as well as with the VMEbus and VERSA-bus. The MC68440, a two-channel DMA device, supports a 24-bit linear address space. The MC68442 is an extended version of the MC68440, with 32 bits of linear addressing and an additional function output. The MC68450, a four-channel DMA controller, is upward pin and register compatible with the MC68440. Motorola, Austin, TX

UNIX SystemV Interactive Streamer
Ethernet Multiuser Unix

Minibox—Heurikon’s new multiuser, multitasking workstation—puts the power of the MC68000/68010 microprocessor (8 or 10 MHz) and the flexibility of UNIX all in 1.5 square feet of desk space. Designed with the OEM in mind, Minibox gives you these features and capabilities you’ve been searching for: Electronic mail • Interprocess communications (IPC) • Fully integrated streaming tape drive, up to 280 MB of Winchester storage • 1 MB floppy drive • UNIX System V or III • Ethernet (TCP/IP) for fast expansion and networking • Floating Point Processor • CPM Shell for CP/M-to-UNIX link • Hotline customer support.

Heurikon
3281 Lithium Drive Madison, WI 53713 Wisconsin 608 271 8700 Texas 699232
1-800-356-9602

Circle 79 on Reader Inquiry Card

Circle 204

Circle 136

Circle 190

Circle 133
NEW PRODUCTS

Precision Analog Converter

Containing the analog circuits necessary to make a dual slope integrating converter, this CMOS A/D converter, the TSC500, can be used in applications at 8- or 14-bit resolution with only a software change. The TSC500 features a differential analog input and reference for ratiometric conversion with a zero scale temperature drift of 2µV/°C. Nonlinearity is 0.005% max, with differential nonlinearity at 0.002% max. The CMOS differential input leakage current is 15 pA max with resolution guaranteed at 50 ppm. Teledyne Semiconductor, Mountain View, CA

Circle 130

8-Bit Microcomputer In SNOS

With 32 bytes of EEPROM, in two 16 byte banks, as well as 512 × 512 bit program ROM and 32 bytes of RAM, the PIC16E57 8-bit microcomputer uses a SNOS process. The on-chip voltage synthesizer uses the standard 5V power source to generate the EEPROM write voltage. Pin compatible with the PIC16E57, the PIC16E57 provides EEPROM instructions that allow it to read and write to EEPROM registers. Available in temperature ranges from -40°C to +110°C, the PIC16E57 is priced at $3 in 50K quantities. General Instrument, Hicksville, NY

Circle 126

Enhanced Floppy Controller

The FDC 9266 enhanced floppy disk controller combines the FDC 765A with the FDC 9229 Floppy Disk Interface Chip in a 40-pin DIP. Maintaining software compatibility with the FDC 765A, the FDC 9266 can control up to four drives: single or double sided 3 1/2", 5 1/4" or 8" drives. Its programmable sector size capability allows the FDC 9266 to interface to CP/M and MS-DOS. Working in DMA, processor polled or interrupt mode, this controller also features a built-in precompensation generator. Price in 100s is $25.30. Standard Microsystems, Hauppauge, NY

Circle 202

4-Bit Composite Video D/A Converters

These TTL compatible converters in the AH8304 family are available with or without memory and feature advanced single chip design. The AH8304 is a self-contained, 4-bit composite video subsystem in a 24-pin DIP. The AH8304TM color-mapped triple (RGB) 4-bit video D/A converter has color look-up table memory designed for the color graphic system. The AH8304TC is a triple video DAC-only version for use with systems that require a different configuration of look-up table memory. Analogic, Peabody, MA

Circle 199

CMOS 32-Bit µP Development

Fabricated in 1.3 micron CMOS, 2-layer metal process technology and containing over 300,000 transistors, this 32-bit microprocessor test chip operates at 5 MIPS. The Micro 32 test vehicle incorporates a proprietary pipelined system architecture and a cache memory scheme permitting high speed interface with I/O processors and file processors. Featuring a 200 kbit ROM with a 50 nsec cycle time and a 32-bit ALU, the chip measures 6.5 mm × 9.0 mm. No definite packaging configuration has been chosen. Hitachi, San Jose, CA

Circle 201

CMOS FIFO

The IDT 7101/7102 CMOS parallel In-Out FIFOs are built with a RAM Pointer architecture, eliminating fall-through time and allowing for a faster read/write cycle. The IDT 7202, a 1024 × 9 organization, and the IDT 7201, a 512 × 9 organization, achieve commercial access times of 50 nsec, 80 nsec and 120 nsec, and military access times of 55 nsec, 85 nsec and 120 nsec. Operating requirements are 80 mA: commercial and 100 mA: military units. On standby, the power requirements drop to 8 mA and 15 mA, respectively. Integrated Device Technology, Santa Clara, CA

Circle 205

10-Bit 800 Nsec A/D Converter

With an 800 nsec max conversion time, this 10-bit hybrid A/D converter (AD ADC-816) specifies a typical conversion time temperature coefficient of ±0.06% /°C. Guaranteeing max differential linearity of ±0.5% and no missing codes, the 816 provides a pin-selectable
The Ultimate Delay Line
Now! Available In Two Configurations.

Auto-Insertable
- 5 Outputs, Equally Spaced
- Input and Outputs T^2 L Buffered Delay
- Delays—4 NS to 500 NS
- Precise and Stable Delays
- Competitively Priced
- Quick Delivery

Surface Mount

Internal reference and three unipolar input ranges: 0 to -5V, 0 to -10V or 0 to -20V; and three bipolar ranges: ± 2.5V, ± 5V or ± 10V. Three grades are available in 0°C to +70°C, -25°C to +85°C and -55°C to +125°C. Analog Devices, Norwood, MA

Circle 138

BOARDS

STD Bus Boards

Five 6502-based board level computers have been announced by Cubit. Both NMOS and CMOS CPU boards feature serial and parallel I/O, memory and peripheral control capabilities. Programming can be done in Basic or Assembler running under Cubit's DOS/65. Forth will be available soon. Peripheral support is provided by an intelligent CRT/printer/keyboard controller. Cubit, Mountain View, CA

Circle 144

Q-Bus Winchester/Floppy Controller

Compatible with DEC's MSCP software, the UDCII dual-width Winchester and floppy disk controller is compatible with the Q-Bus. Under MSCP, the UDCII allows the use of ST506 interface drives of any capacity. Hence, system integrators can design MicroPDP-11 and MicroVAX-I and II compatible systems with RX50 emulation. The UDCII can also control any combination of up to four Winchester cartridge and floppy drives. Price is $1,795. Andromeda Systems, Canoga Park, CA

Circle 207

1-Mbit Bubble Memory Eurocard

Compatible with the G-64 bus, the Gesbul-1 1-Mbit bubble memory board is organized as 128 Kbytes of nonvolatile magnetic storage. The board uses a DIN 41612 indirect connector and is powered by a +5V and +12V on the G-64 bus. Using a bubble memory device and associ-
**NEW PRODUCTS**

- **Asyc Controller For LSI-11**
  Maintaining software compatibility with DEC's DZII subsystem, the Optimux/8DZ async communications controller allows users to interface up to eight devices per controller card. Contained on a dual-height PCB that connects to its DEC H3006-compatible distribution panel, the controller allows up to 16 lines to be interfaced to the LSI-II system from each panel. Providing 15 software-selectable data transfer rates from 50 bps to 19.2 Kbps, it contains a 64 character receive FIFO buffer. Price is $770. *Dilog*, Anaheim, CA

- **IBM PC Processor Board**
  Intended to increase the processing speed of the IBM PC and XT, the Model PC-286 processor consists of a single PCB containing an iAPX286 processor chip, room for an optional 80287 math coprocessor and up to 640 Kbytes of RAM. The PC-286 can be run at 4, 6 or 8 MHz and may include 256K to 640K RAM. A piggyback card can add from 512 Kbytes to 2 Mbytes of additional RAM. The PC-286 board replaces the 8088 chip with a 40-pin header, allowing the PC-286 to take over the PC bus completely. *Seattle Telecom and Data*, Redmond, WA

- **Image Processing Boards For VMEbus**
  Designed for machine vision, imaging and graphics applications using the VMEbus, the VMACC-Series boards are especially built for high speed enhanced image processing. The boards include: the Image Acquisition Board which interfaces to linear CCD-array camera including programmable video tables for preprocessing; the Image Buffer Board: 256 Kbyte RAM for refresh of 512 x 512 matrix in 17 msec; and the Image Processing Boards such as Convolution, Streaming and VARDIG that perform image algorithms for dimensional and/or surface analysis. Price ranges from $2,000 to $5,000. *Advanced Computer Concepts*, Costa Mesa, CA

- **VMEbus Microcomputer Board**
  Designed for real-time processing applications, this VMEbus-based microcomputer board features a 12.5 MHz 68000 in a pin grid package. With async and sync dual serial communications ports, the board provides three 16-bit timers and 16 bits of parallel I/O. The CPU-2RT can access 128K dual-ported DRAM, upgradable to 256K with no wait states. Sockets for two EPROMs and two SRAMs are available as well as an onboard VME arbiter, allowing the CPU-2RT to occupy slot 1. Price is $2,450. *EMS*, Dallas, TX

- **Intelligent Controller Interfaces Bitbus**
  Part of a line of distributed control modules compatible with the Intel Bitbus network, the DT901 Intelligent Stand-alone Controller interfaces the Bitbus to iSBX modules for remote measurement and control. The DT901 functions as a remote controller or an I/O expansion device. As an intelligent controller, it monitors the multiple process points status and executes user-supplied control software. As an I/O expander, the DT901 collects measurement and control information and transfers data via the Bitbus to the host. Price is $495. *Data Translation*, Marlboro, MA
TEAC VTRs Can Take It

IBM PC Color Graphics Board
Plug-compatible with IBM's Color Graphics Adapter, the ColorView graphics board provides 32K memory, allowing the user to create two complete pages in the graphics mode. ColorView also features two true colors (1 of 16 for the foreground and 1 of 16 for the background) in the IBM high resolution graphics mode. Display memory can be accessed at any time by the microprocessor without causing glitches on the screen. Price is $289. Princeton Graphic Systems, Princeton, NJ

Single-Board Multibus Image Processor
Performing real-time image processing and image display on a single Multibus board, the MIP-512 contains a 16.7M color palette. With data storage and 256 Kbytes of on-board RAM that provide 512 x 512 resolution with 256 colors/pixel, the MIP-512 also offers a 90 nsec bit slice ALU. The dual-ported RAM allows memory mapped CPU access and true DMA. Eight input and eight output look-up tables are available. Price is $2,995. Matrox Electronic Systems, Dorval, Quebec

Double Wide SBX Board
Combining two independent RS-232-C or RS-422A/449 serial I/O channels, a battery-maintained real-time clock/calendar and 2 Kbytes or 8 Kbytes of battery-maintained CMOS RAM, the UDX-221 Multifunction Multimodule plugs directly into any iSBX bus compatible host board. Each of the UDX-221's two serial channels may be configured for EIA RS-232-C or RS-422A/449 interfaces with async, bit-sync or byte-sync formats. Each channel has its own baud rate generator and may be operated from 37.5 bps to 1.23 Mbps. Microdesigns, Tucker, GA

Graphics Controllers and Displays
Drawing images at 1M pixels/sec, these plug-in graphics controllers, the M-16 and M-256 provide 16 and 256 colors, respectively from a palette of 4096. The drawing capability is generated by the firm's two-micron CMOS graphics controller chip set with an on-board 68000. To operate with the controllers, a 60 Hz noninterlaced RGB display, the CD-1, with 640 x 480 resolution has also been announced. Controllers range from $2,250-$2,850 and the display costs $1,025. Verticom, Sunnyvale, CA

EDC Memory and Software Support
Built for the LSI-11/73 and MicroVAX, the CI-1173-EDC Memory with error detection and correction and a software support module for Q-Bus compatible systems is available in configurations ranging from 256 Kbytes to 2 Mbytes on a single card. Worst case access and cycle times are 60 nsec and 240 nsec, respectively. Internal and distributed refresh are built into the memory, which requires less than 900 mA power from a +5V battery source for up to 2 Mbytes of memory. Chrislin Industries, Westlake Village, CA

NEW PRODUCTS
NEW PRODUCTS

32-Bit Logic State Analyzer

When plugged into an IBM PC, XT or compatible expansion slot, the PCI-4304-1 transforms the computer into a 32-bit logic analyzer. The PCI-4304-1 system includes a plug-in PCB, 3' ribbon cable and instrument pod that extends from the computer to the digital system under test, a set of color-coded input leads with probe clips and the system operating software. The data path is 32-bits wide, data setup time, 20 nsec and data hold time, 0 nsec. With 1024 x 32-bit words memory, the PCI-4304-1 is priced at $2,750. Burr-Brown, Tucson, AZ Circle 145

VMEbus Mini-Array Processor

An enhanced version of the firm's first VMEbus mini-array processor (VAP-64), the VAP-64B fixed-point mini-array processor provides three more instructions and is fully compatible with the VAP-64. The 21-instruction set includes complex demodulation, an FIR instruction and Peak Pick instruction. The VAP-64B also features 10 MOPS, 50 kHz real-time processing bandwidth and built-in self-test. DSP Systems, Anaheim, CA Circle 148

20 MHz Q-Bus SMD Controller

With data transfer rates up to 2.5 Mbytes/sec, the MLSI-DK11 disk controller will operate disk drives with SMD interface that can operate at the standard SMD rate of 1.2 Mbytes/sec as well as drives with 1.8 or 2.4 rates. The MSLI-DK11 has up to 22-bit direct DMA data transfer addressing range and Block Mode DMA data transfer capability. The controller can support two physical drives at 1 or 2 logical units per drive for a maximum of 4 logical units. Price is $2,330. MDB, Orange, CA Circle 149

Compact Q-Bus Interface

Compatible with DEC's DZVII, the Octomux 8-port async multiplexer has 8 ports in a dual board. With programmable baud rates to 38.4 Kbaud and a double density distribution panel, the Octomux features character length, parity, stop bits and Transmitter Enable. On-board DIP switches permit selection of base address, interrupt vector, interrupt priority and baud rate table. Four addresses access six device registers. Mintronics, St. Paul, MN Circle 154

Color Graphics Card For IBM PC

Providing an optional parallel printer port and composite color output on a single short slot board, the Persys ShortPort Color Card is fully compatible with standard IBM color graphics software and monitor. Video output is direct drive (IRGB) or optional composite color output. Graphic character display is 7 x 7 dot characters in an 8 x 8 field. Alphanumeric display mode is 40 characters x 25 rows, low resolution and 80 characters x 25 rows, high. Emulex, Costa Mesa, CA Circle 146

SOFTWARE

Interactive Design Rule Checker

Designed for VLSI layout on the Designer III workstation, the CAEPAC III Design Rule Checker software package checks for violations interactively as each element is placed or modified. When a violation in the design rules occurs, CAEPAC III highlights the area and displays a user-defined error message. The software allows designers to see violations as soon as they are created. This occurs in real-time during layout and editing. Caeco, Tucker, GA Circle 179

Real-Time Intelligent Machine Interface

Enabling LISP programs or expert systems to deal with real-time processes, the RTIME (Real-Time Intelligent Machine Interface) is designed for the firm's family of LISP machines. Written in C code, RTIME uses the parallel processing capabilities of the Lambda/Plus series of LISP machines, which feature both a dedicated LISP processor for AI-related tasks and an MC68010 numeric copro-
Io Incorporated

INTRODUCES

9 - TRACK TAPE INTERFACES

SCSI/9-TRACK

FEATURES
• Supports the standard SCSI command set for a non-direct access tape device
• Standard PERTEC compatible tape formatter connectors
• Parity generation and detection to tape formatter
• Flexible speed and density selection
• Selectable retries on read and write
• High speed -1M Byte/second burst throughput

402VME 9-TRACK

FEATURES
• Direct Memory Access Controller
• Interfaces to ANSI Standard 9-Track Tape Formatter
• Host Adaptor for SCSI/SASI Disk Controller
• Two RS-232 Serial Ports with Handshake
• Full Vectored Interrupt Support of All Devices
• Double-Height VME Eurocard size

FOR INFORMATION ON THESE AND OTHER VME PRODUCTS PLEASE CONTACT THE FACTORY:

Io Incorporated
2430 N. HUACHUCA DR. TUCSON, ARIZONA 85745
(602) 792-0969

What’s Your Angle?

Sperry’s new MEI-60 mini electronic inclinometer is the low cost answer for your angle measurement applications. Not just another angle sensor, the MEI-60 is a precise, self-contained inclinometer featuring:

• Outstanding performance — resolution to 1 arc sec., range ± 60 deg.
• Simple integration — your choice of digital or analog I/O
• Economy — prices starting at less than $100

Sperry Corporation
Aerospace & Marine Group Sensing Systems
P.O. Box 21111
(MS DV-2B)
Phoenix, AZ 85036-1111.
(800) 545-3243.

Circle 37 on Reader Inquiry Card
NEW LITERATURE

Structured FORTRAN With WATFIV. This 500-page third edition by John B. Moore discusses how to run WATFIV jobs under the CMS operating system and how to use the interactive debugging facilities available with WATFIV. Sections have been added to emphasize the use of top-down design and stepwise refinement in algorithm development.

Reston Publishing Co. Circle 255

Forth—Tools and Applications. This 150-page book by Gary Feerbach and Paul Thomas demonstrates the development of Forth-based tools to help the programmer design and debug Forth applications. Programming design aids are hinted at, debugging techniques are shown and utilities are analyzed. Listings for Forth routines are provided by line numbers, rather than screens.

Reston Publishing Co. Circle 252

FORTRAN 77 For Scientists and Engineers. In this book, J. N. P. Hume and R. C. Holt acquaint students with the ideas and technical terminology connected with computers and provide a detailed presentation of programming so the computer can be used professionally. Programming is taught using the FORTRAN 77 language.

Reston Publishing Co. Circle 253

Introduction to Computer Engineering Hardware and Software. This third edition, written by Taylor L. Booth, discusses the various classes of digital information processing systems and devices and the interrelationship between the hardware and software techniques that can be used to solve a particular problem. The unifying theme throughout the book is the concept that the steps involved in solving a problem must first be represented by an algorithm.

John Wiley and Sons Circle 254

Linear ICs Reference Book. This 34th edition of Linear ICs, published by D.A.T.A. Inc., lists 15 component categories and 62 specific device functions within those categories. Manufacturer information is compiled in one section and a cross-referencing "Functional Equivalence Index" lists currently available linear ICs from 80 manufacturers by pin-for-pin equivalent groups, with generic numbers that refer directly to schematic drawings.

D.A.T.A. Inc. Circle 259


CC Exchange Circle 260

PC Data Acquisition/Control Interface Handbook. This 68-page handbook from MetraByte Corp. describes the firm's line of data acquisition and control plug-in interface boards for the IBM PC, XT, AT and compatibles. Included in the book are detailed sections on applications, configuration guides and a utility software description.

MetraByte Corp. Circle 258

Programming For People/Pascal. David Kay presents the fundamentals of computer programming, using Pascal as the example language in his 640-page book. The book approaches issues such as employing logical, disciplined algorithmic problem solving methods, managing the complexity of large systems and understanding the reasons behind the rules.

Mayfield Publishing Co. Circle 256

Printed Circuit Design and Drafting Manual. This 220-page manual and catalog from Bishop Graphics lists printed circuit design and drafting products. Divided into two segments, the manual is an expanded product catalog and an updated technical manual. New products included in the book cover Bishop's line of microelectronic art- way patterns. Also included is the Accupunch deal system punch, designed to give users the hole pattern of their choice for overlay drafting applications.

Bishop Graphics Circle 262

NEW BATTERY HOLDER PACKS
PC BOARD MOUNTABLE

Available with 6" leads or male and female terminals

Tin plated cold rolled steel spring

For AA and AAA batteries

Accommodates NiCd, Carbon-Zinc or Alkaline batteries

2 and 3 cell packs available

Tapered Beam Fit

Outline of battery and neg/pos direction finder

Two countersunk holes thru bottom for eyestop and screw mounting

Self-contained pack prevents contamination from battery leakage

Molded-in terminals for wave soldering

Batteries are series connected

Spring clip for easy battery replacement—no soldering

Tin plated cold rolled steel terminals

We develop custom designs. For all the details, call or write:

Memory Protection Devices inc.
320 Broad Hollow Road, Farmingdale, N.Y. 11735 • (516) 454-0340

Circle 90 on Reader Inquiry Card

DIGITAL DESIGN • MAY 1985

123
## Calendar

**June 3**
Technology Issues in Networking Seminar
New York, NY. Contact: Robert Weiner, Technology Concepts Inc., Old County Road, Sudbury, MA 01776. (617) 443-7311.

**June 3-5**

**June 4-6**

**June 6-7**
Networking IBM PCs and Compatibles Seminar. Raleigh, NC. (Also five other dates and locations) Contact: Center For Advanced Professional Education, 1820 E. Garry St., Suite 110, Santa Ana, CA 92705. (714) 261-0240.

**June 9-11**

**June 9-13**
Computer Vision And Pattern Recognition Conference. San Francisco, CA. Contact: IEEE Computer Society, 1109 Spring St., Suite 300, Silver Spring, MD 20910. (301) 589-8142.

**June 10-11**
Artificial Intelligence Seminar. Dallas, TX. Contact: Ken Orton, Future Computing Inc., 8111 LBJ Freeway, Dallas, TX 75251. (214) 437-2400.

**June 10-13**
Short Wavelength Laser Systems Course. Dallas, TX. Contact: Engineering Technology Inc., PO Box 8859, Waco, TX 76714-8859. (817) 772-0082.

**June 12-15**
ATE East Conference and Exposition. Boston, MA. Contact: Stephen Schuldenfrei, Morgan-Grampian Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215. (617) 232-EXPO.

**June 19-21**
Nepon East Exposition. Boston, MA. Contact: Cahners Exposition Group, Cahners Plaza, 1350 East Touhy Ave., PO Box 5060, Des Plaines, IL 60018. (312) 299-9311.

**June 19-21**
Local Area Networks Seminar. Cambridge, MA. (Also in St. Louis, MO—June 5-7 and Albany, NY—June 12-14) Contact: Center For Advanced Professional Education, 1820 E. Garry St., Suite 110, Santa Ana, CA 92705. (714) 261-0240.

**June 23-26**
Design Automation Conference. Las Vegas, NV. Contact: Lawrence O'Neill, Bell Laboratories (213 327), Crawfords Corner Rd., Holmdel, NJ 07733. (303) 530-4333.

**June 24-25**
Micro-Mainframe Links Seminar. Seattle, WA. Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

**June 25-27**