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Illustration by Bill Morrison

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SourceGate is a window driven high level language debugger designed to support the Huntsville Microsystems 200 series of in-circuit emulators.

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For more details about "IDA," Computer Design’s Instant Data Access see page 94

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TECHNOLOGY & DESIGN REPORTS

Automation improves speed and accuracy of software testing
Testing complex software applications is a tedious task best left to machines. New methods of automating the process promise payoffs in terms of shipping higher-quality products.
—Tom Williams

Separating hype from reality in benchmarking
Benchmarking simulators is a tough job that tests users and vendors alike. But with adequate cooperation between the two camps, meaningful results can be achieved. —Mike Donlin

COVER STORY

High-performance networks challenge Ethernet
A half-dozen high-performance network interfaces—including three proposed standards—dominate the industry. Though each has advantages in its particular area, price/performance will undoubtedly push the market toward a single approach.
—Warren Andrews

DESIGN STRATEGIES

Video teleconferencing on British shores
Designing a video teleconferencing system involves building bidirectional equipment that can capture and compress video and audio images from one location and transmit them to another, where the signals must be received, decompressed and reconstructed. —Dave Wilson

PRODUCT FOCUS

Logic analyzers tackle the "deeper" problem
Perhaps the greatest opportunity to shorten the design cycle comes from spending time more effectively in the lab.
—Jeffrey Child

COLUMNS

MIXED-SIGNAL DESIGN —Stephan Ohr
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Hitachi enlists systems design house to support its ASIC users

With its launching of a third-party ASIC design center program last month, Hitachi America (Brisbane, CA) has given its users access to a level of systems engineering expertise they themselves may not have. “As ASIC technologies become increasingly complex, the mix of customer requirements and expectations also becomes more sophisticated,” explains ASIC marketing manager Joe Bunik. “Today’s leading customers are not just looking for yesterday’s training on patchwork tools and a grab bag of workstations. In addition to an industry-standard environment, they’re looking for a support infrastructure which has the systems-level expertise and high-performance design techniques that will let them achieve a fundamentally superior ASIC solution.”

Hitachi’s appointment of Locus (Madison, WI) as an authorized design center is the first of several regional agreements it will be developing to support its users. Remarkably that Locus is not just a CAD shop but is an experienced systems design and manufacturing operation in its own right, George Saul, director of marketing, says, “This depth of systems expertise at the ASIC level is critical to the effective implementation to stay competitive in the lucrative Japanese EDA marketplace.”

Teradyne sells EDA tools

Teradyne EDA (Santa Clara, CA) has completed its departure from the front-end CAE business by selling its Aida test software to Crosscheck Technologies (San Jose, CA) and its line of Vanguard Schematic design systems to Sophia Systems (Tokyo, Japan). Though the deal is still pending, Crosscheck will immediately support present Aida users and will hire core engineering and marketing personnel from Teradyne.

The acquisition will give Crosscheck the ability to go beyond chip-level design to system-level testing and diagnostics. Crosscheck’s present tools are applicable mainly to complex asynchronous circuits with multiple gated clocks. The Aida tool targets synchronous designs and is particularly useful in system-level debugging.

Sophia has been a Vanguard distributor for several years, and will obtain worldwide distribution rights with the acquisition. The vendor will sell, service and support Vanguard, and plans to enhance and expand the product line to stay competitive in the lucrative Japanese EDA marketplace.

—Mike Donlin

Neural net chip powers first commercial application

An analog neural network IC developed by Synaptics (San Jose, CA) is now powering an optical check reader built by Verifone (Redwood City, CA). The chip, called the I-1000, consists of two parts. The first is a neural network-based image-sensing array that imitates the early vision processes occurring in the retina before information is passed to the visual cortex of the brain. The second is a neural network trained by example to recognize the patterns of characters on a check being slid through a slot in the reader.

Neural networks are characterized by their ability to learn by example. In the case of the I-1000 in this application, the learning was done off-line via computer simulation and the results transferred to mask layers in manufacturing the chip. One might think of it as an Electrically-Trainable PROM (ETPROM).

Synaptics was founded by Frederick Faggin, coinventor of the microprocessor and cofounder of Zilog, and Carver Mead, of VLSI and Silicon Compiler fame. The design for the I-1000, of course, exists in a silicon compiler and can be expanded, reconfigured and retaught for other practical applications that may present themselves.

—Tom Williams

Bulletin board for fuzzy logic

A semipublic bulletin board for people interested in fuzzy logic has been established by Aptronix (San Jose, CA). Called FuzzyNet, the bulletin board has two levels. There is a level for the general public interested in news and developments in the industry. It will provide an electronic mail system and access to articles and news on applications tools and the like.

A second level will be for registered users of Aptronix’s fuzzy logic development environment, called Fide. At this level, users will be able to seek on-line help and exchange applications and experiences regarding the use of Fide. FuzzyNet is up and running now, but is still building a base of users and information. The number is (408) 428-1883.

—Tom Williams

Cadence backed in push to extend Verilog methodology to VHDL

A dozen or so electronic systems companies and ASIC vendors are backing Cadence Design Systems (San Jose, CA) in an attempt to extend Verilog ASIC modeling practices to VHDL, which so far lacks any standard modeling methodology. The intent of the group is to submit a proposal to the appropriate standards organizations outlining how the adaptation of Verilog’s predefined logic primitive set, standard interchange format for delays (Standard Delay File), timing model, and timing checks—all in VHDL source code—would accelerate the availability of ASIC libraries in VHDL.

The initiative has been endorsed by Alcatel NV, Bell Northern Research, Epson America, Ericsson Telecom AB, ExperTest, Harris Semiconductor, National Semiconductor, NEC Electronics, North Oaks EDA Consulting, Oki Semiconductor, S-MOS/Seiko, Sunrise Test Systems, Texas Instruments, Toshiba, the VHDL Technology Group, and Xilinx. I.M. Dodd, director of tools and technologies at Alcatel’s Paris headquarters, says, “Let’s move past the problems that have al-

Continued on page 12
When Every Nanosecond Counts
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<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>PROPAGATION DELAY (Max)</th>
<th>OUTPUT ENABLE (Max)</th>
<th>OUTPUT DISABLE (Max)</th>
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<tr>
<td>Buffers</td>
<td>4.1ns</td>
<td>5.8ns</td>
<td>5.2ns</td>
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<td>Transceivers</td>
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<td>Registers</td>
<td>5.2ns</td>
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<td>Latches</td>
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Continued from page 10

ready been solved by the industry and focus on things that need our attention, like subsets for synthesis and acceleration.”

EDA vendors of VHDL tools will most likely withhold endorsement until they receive some confirmation that the Cadence-backed initiative is about the advancement of technology, rather than the advancement of Cadence. A hands-off policy, once a strong technical proposal has been submitted to the appropriate forum—which would appear to be VHDL International—might be the confirmation they’re waiting for.

—Barbara Tuck

PC multiprocessing bus waits for the 586

Whether you prefer to call it the 586 (or, as Intel prefers, the P5), samples of the latest 80X86 microprocessors reportedly will be delivered to beta customers sometime between now and November’s Comdex. Companies that have seen advance technical specifications are apparently impressed with the device.

In fact, designers at Corollary (Irvine, CA) are impressed enough to refocus their strategy for C-bus II, a multiprocessing bus architecture for the PC, and orient it exclusively toward the P5. The original plan for C-bus II was to build a multiprocessing chip set targeted for a 50-MHz 486 and to follow that with MIPS R4000 support.

“C-bus II is CPU-independent, so for a 50-MHz 486 and to follow in the future we can support other processors,” says Corollary president George White. “Whether you prefer to call it the R4000 processor have, however, had some influence on the C-bus II design. “When we had planned to build an R4000 version of the C-bus II chip set, the R4000 crowd wanted more memory to support the R4000’s 64-bit virtual address space,” says White. As a result, Corollary expanded the physical memory space of the C-bus II from 2 Gbytes to 32 Gbytes.

“It’s probably a good idea for P5s as well,” he adds. The change in memory space is the only modification to C-bus II’s feature set as announced last year.

Along with Microsoft (Redmond, WA), Corollary has also announced the development of an implementation of Windows NT that takes advantage of the C-bus II multiprocessing architecture. C-bus II also supports Unix System V Release 4.0 and Santa Cruz Operation (SCO) MPX.

—Jeffrey Child

New support policy for SBus

Sun Microsystems Computer Corporation (SMCC—Mountain View, CA) is updating its SBus support policies this month to provide a greater level of support to SBus developers and to focus its support in critical areas. Last quarter’s SBulletin (see “Sun curtails support,” Computer Design, June 1992, p 132) reported that Sun was curtailing its SBus support and would no longer accept inquiries from developers.

SMCC has apparently rethought its position and now says, “Market development engineering will continue to provide phone, fax and e-mail support on demand for hardware, firmware and software queries from the SBus developer community.” The company reports the greatest number of questions received has concerned software. As and SMCC nears the introduction of Solaris 2.0, the staff is expected to be busy preparing for the transition. For that reason it states: “We will probably respond less quickly to your requests than we have in the past,” but will acknowledge receipt and provide an estimate of when it can service the request.

In addition, SMCC stressed it will make a major effort to aid SBus developers in their transition to Solaris 2.0 DDI/DKI interface. The company will make available a migration kit with sample drivers, a Device Drivers Manual, manual pages for the DDI/DKI routines, and data structures and a white paper on porting to Solaris 2.0.

—Warren Andrews

Dazix joins the synthesis pack

Capitalizing on a partnership with AT&T Bell Laboratories (Murray Hill, NJ), Dazix (Huntsville, AL) has entered the competitive synthesis arena with a suite of tools called Dazix Synergy.

The tools, which support the synthesis of VHDL, Verilog and the C hardware description languages, face stiff competition from industry leader Synopsys (Mountain View, CA), as well as Cadence Design Systems (San Jose, CA), Mentor Graphics (Wilsonville, OR) and Viewlogic Systems (Marlborough, MA). Dazix director of marketing James Ulatowski promised that its solution would be more integrated than those of the competitors, but gave few specifics to support the claim.—Mike Donlin
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While the drive for bigness may be irresistible, big isn't necessarily better.

Barnum would be proud

The 29th staging of the Design Automation Circus—excuse me, Design Automation Conference—is over, and most of us on Computer Design have finally wound down enough to make some observations about DAC, and about trade shows in general.

I've come to the conclusion that, while the drive for bigness may be irresistible, big isn't necessarily better. DAC has become a big show, not so much in terms of the number of exhibitors—there were only about 120 this year, although that's not small—or in terms of the number of attendees—attendance was reportedly down 30 to 40 percent compared to last year—but in terms of the staging. Gigantic booth areas, huge audiovisual presentations complete with barker's and a vast array of T-shirts and giveaways somehow seem more appropriate to a Comdex—basically a consumer/reseller/retailer-oriented show—than to a conference and exhibition where the exchange and acquisition of technical information, as well as taking the first steps toward an intelligent buying decision, should be the most important consideration. It's now become extremely difficult to separate the signals from the noise if you're an editor, much less an attendee, and to have your signals heard above the noise if you're an exhibitor, especially a small exhibitor.

Computer Design, for example, sent three technical editors to DAC and, well before the second week in June, they were all being bombarded with requests to attend one-on-one meetings, press conferences, breakfasts, lunches, dinners, hospitality suites, and entertainments. And, of course, they were all being bombarded by the same exhibitors. Some tough choices had to be made: visit with a large vendor, or a small one or an up-and-coming one; give someone an hour or only a half-hour; go to the Nixon library, see The Phantom of the Opera, or have dinner at The Cellar. The decisions about what vendors to see on the floor, what exhibitor presentations to attend or what audiovisual extravaganzas to mill about watching must have been just as difficult for the engineering attendees, although most of them probably didn't receive the same number of invitations for breakfasts, lunches, dinners, and entertainments—unless they were big customers or potential big customers, which is understandable.

And, finally, DAC had to be daunting for the small exhibitors, those with only one or two booths. How do they catch an attendee's attention when there's a barker giving a pitch in front of a 10-foot screen? (I can't figure out why anyone would listen to a barker in front of a 10-foot screen, but ...) Just as an editor might miss something new or significant, so will a designer if a smaller vendor can't get the designer's attention or can't get his message across because of the noise.

Unfortunately, big shows can become victims of their bigness, especially when smaller conferences and exhibitions come along that provide a saner forum for the exchange of information and intelligent buying decisions. We hope that DAC doesn't suffer the tribulations of a couple of other big shows we know.
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- 32-bit read/write buffer FACT QS (74ACT3283T)

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CALENDAR

CONFERENCES

July 26 - 31
SIGGRAPH '92
McCormick Place, Chicago, IL.
This year's conference theme is "Insight Through Images," a theme that will be portrayed through an extensive program of courses, panels and an exhibition. More than 25,000 people are expected to attend this leading forum for computer graphics hardware, software and systems. There will also be an electronic theater and art show. Contact: ACM SIGGRAPH '92, PO Box 95316, Chicago, IL 60694-5316, (312) 644-6610, Fax (312) 321-6876.

August 12 - 14
Windows & OS/2 Conference
World Trade Center & Hynes Convention Center, Boston, MA.
More than 20,000 attendees are expected at this conference which focuses on the two key personal computer graphical interfaces of Windows and OS/2. There will be technical sessions on programming in the Windows and OS/2 environments. The exhibit will include a test drive center where computers are set up for attendees to try the latest applications. Contact: CM Ventures, 5720 Hollis St, Emeryville, CA 94608, (415) 601-5075, Fax (415) 601-5075.

September 15 - 17
Buscon '92 East
Hynes Convention Center, Boston, MA.
Buscon '92 East is the event where the BUSCON/92-EAST® products, technologies and components related to bus- and board-level design can be seen. The technical conferences, designed and coordinated by Computer Design and Military & Aerospace Electronics, are highly focused, in-depth seminars that explore the hottest issues from SCI to Futurebus+, RISC and embedded PCs. There will be half-day and full-day tutorials and more than 200 exhibitor booths. Contact: Registration Department, Buscon '92 East, 200 Connecticut Ave, Norwalk, CT 06856-4990, (800) 243-3238, Fax (203) 857-4075.

September 22 - 24
Unix Expo
Jacob K. Javits Convention Center, New York, NY.
The ninth annual Unix Expo will showcase Unix/Open Systems products, standards and services to an audience including corporate end users, resellers and systems integrators. The expo and conference will analyze current trends in the Unix community, including the move toward Open Systems computing, multimedia and the corporate world's increasing use of Unix as a platform for achieving open systems. Contact: Bruno Blenheim Inc, Fort Lee Executive Pk, One Executive Dr, Fort Lee, NJ 07024, (800) 829-3976 or (201) 346-1400, Fax (201) 346-1532.
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Test automation for ICs is finally taking its rightful place alongside design automation in importance. The problem of creating an efficient and exhaustive set of test vectors for an IC has always existed, but its enormous difficulty has consistently eluded automated solutions. Recently, some new approaches to automatic test design have matured to the point of commercial viability and are causing electronics designers to reevaluate their approaches to test. Fortunately, these tools come at a time when test generation has emerged as a bottleneck in getting new, high-quality electronics to market.

The goal of test automation is to accelerate test program development to achieve shorter time-to-market, higher-quality tests and reduced testing cost. Many test tool paradigms meet these objectives by trading off increases in silicon or design costs. It is important, therefore, to answer some end-product economic questions before evaluating any test automation solution: How much defect coverage does my product market require? What degradation in performance or chip cost can my end product accept? How many vectors can my foundry afford to support?

How much is good enough?
Recent studies by major electronics corporations and universities are helping to answer the question of how much coverage is good enough. The evidence clearly demonstrates the financial advantage of increasing defect coverage from less than 85 percent to more than 95 percent. This higher degree of testing reduces ‘passed’ defects by more than 15,000 parts per million of the total production run. Each company must translate for itself the savings that this provides in fewer service calls, reduction in bad inventory and elimination of expensive rework. These are typically large numbers, but perhaps of more importance is the company’s improved quality image in the marketplace.

The task facing every test automation tool is basically the same: to find the minimal set of chip input that will push a possible error at any circuit node to the chip output for detection. Most solutions simulate electrical failures at each node, and then search forward through the logic for an unblocked path to the output (observability) and backward for a path from the input (controllability). The real difficulty comes in trying to navigate the heavily interdependent, clock-sensitive logic as the software looks for these pathways. For most designs, the search space approaches infinity, making unguided probes impossible. For example, an IC with 40 flip-flops and 100 I/Os has $10^{150}$ possible logic paths, which is orders of magnitude greater than the number of particles in the universe.

The original automatic test generation (ATG) programs required only a structural netlist of the circuit, and so imposed little if any change on the design. The netlist information proved insufficient, however, to guide ATG and the test coverage results were poor. Today’s netlist-driven ATG products offer improved search algorithms and guidance file inputs, but the increasing complexity of designs continues to make the computer run-times unrealistic. As a result, users of these tools end up adding nearly total design-for-test structures to the sequential logic in their designs.

The name of the game is trade-offs
There are many factors which decide whether a company can accept a new design methodology for test development. The major trade-off occurs between the expected defect coverage of the test automation, and its impact on both the current design environment...
and the silicon implementation. Defect coverage includes both static fault coverage at each node and detection of other common manufacturing flaws such as delay faults, transmission line effects and inadequate drive. Many of these latter errors can only be discovered by performing the tests under the IC’s intended operating conditions.

**Static vs. dynamic test**

The ineffectiveness of netlist-driven ATG software has led some people to believe that the only solution to the IC test problem is to ‘invade’ the design with static test logic. This simplifies the task of creating high-static-fault-coverage tests by eliminating the sequential time sensitivity of the logic. The most mature of these methodologies is scan. It works by dedicating a minimum of three additional IC pins to a daisy-chained connection of all the storage elements in the design. During test mode, the storage chain is controlled by the scan pins, and can be set to known values for ATG. The result is typically high static fault coverage.

Scan design requires 10 to 30 percent more silicon, depending on acceptable levels of performance degradation, to implement the chain connection. Therefore, it can have significant penalties in die costs, speed and power consumption. In addition, scan mandates adherence to a set of design rules that may mean a change of style for designers; it can also constrain the use of many common design practices. One of the often unmentioned trade-offs with scan is that important manufacturing flaws in a die are not discovered because the chip is being tested statically rather than at the dynamic operating speed.

Another test insertion methodology which addresses the issue of testing at operating speed is offered by some ASIC foundries. This technology uses a grid of test structures laid over a gate array base wafer to provide a high level of circuit node observability in the ultimate design. The controllability issue for testability is still being addressed. As is the case with scan, designers have to consider the additional silicon costs and performance degradation of this new technology. Until it gains wider acceptance, foundry choice is limited to selected technology licensees and device families.

**Next step—test synthesis technology**

The newest of the emerging test automation solutions takes advantage of the trends toward logic synthesis and top-down design. This test synthesis technology, developed by ExperTest, uses the logic-synthesis register transfer level (RTL) model to guide ATG through the circuit. Knowing how the ASIC or custom IC works, the program can efficiently navigate even very complex control logic, such as coupled state machines. Typical benefits are much shorter computer runtimes, fewer vectors and coverage of between 95 and 100 percent, without the added overhead of scan.

In addition, this new ATG is ideally suited for optimizing the use of IDDQ testing. IDDQ can target CMOS-related faults not covered by the normal stuck-at model, but the tester measurements should be minimized because of their time duration.

The real benefit of using the design model to automatically create the test program is the linkage it provides between the two worlds. The designer can begin synthesizing test vectors at the beginning of the product cycle and can therefore evolve design and test concurrently. Like a smart test engineer, the model-driven ATG points out testability problem areas. The designer or test engineer can either let ATG automatically synthesize fully functional logic enhancements for test, or the change can be easily amended to the design model.

ExperTest ATG encourages functional testing, but it supports full scan, partial scan, built-in self-test, and boundary scan, to ensure compatibility with existing test methodologies. The flexibility, efficiency and quality that synthesis provides to design can now be applied to test.

For many technical markets in the 1990s, customer-measured quality will provide key product differentiation. From top to bottom of the electronic product manufacturing chain—including chip set vendors, board manufacturers, system integrators, and capital equipment providers—the supplier selection will be based on delivering ‘known good’ product. Incomplete tests on a $10 ASIC that causes an explained system crash on a $10,000 computer, a $500,000 communication switch or a $1 million medical imager won’t be tolerated. Whether the ultimate test automation choice for a particular design is scan, test point insertion or design-driven ATG, the advantages provided by higher test coverage will be felt throughout the entire company and economy.
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**Split decision on HDLs forces VHDL/Verilog coexistence**

Barbara Tuck, Senior Editor

If you’re fed up with arguments concerning the advantages of VHDL over Verilog or vice versa, and you simply want libraries and tools that help get your job done, you now have a good chance of getting your wish. VHDL and Verilog vendors are trying to figure out how the two hardware description languages can coexist, since designers are obviously not of one mind when it comes to an HDL of choice. VHDL vendors have accepted that those who made Verilog a de facto standard are not going to abandon it quickly. And Verilog vendors have only to look at the growth of VHDL use to accept that it has, indeed, established itself as a worldwide standard.

**Where does that leave users?**

If you’re a VHDL user, you’re left with IEEE on your side, a well-defined language that’s being updated this year and a plethora of tools from which to choose, although most are immature and many don’t conform fully to the 1076 specification. On top of that, you now have IEEE approval on the STD LOGIC 1164 nine-state multivalued logic system (MVL-9), and at least one ASIC vendor has begun delivering models. But you don’t have a standard timing methodology. “VHDL has a long way to go before we would sign off on it,” comments Laurin Ashby, manager of the Chandler Design Center for the ASIC Division of Motorola (Chandler, AZ), which today signs off on Verilog. Though VHDL is a very good high-level modeling tool, it can’t match Verilog at the gate level, says Ashby. “If VHDL gets to the point where it can model to the detail of Verilog, we’d support it,” she says. If you’re a Verilog user, you most likely have all the models and high-performance simulation you need, but IEEE acceptance is still ahead of you. You also have to wonder whether most of the newer tools with high-level system capability will be developed in VHDL, and if so, if you’ll be pressured eventually to switch to VHDL anyway, particularly if you work for a multinational company.

If you use both VHDL and Verilog, you’re left with a duplication of tools and models, none of which operate together, unless you happen to be a VHDL customer of Cadence Design Systems (San Jose, CA), using your Verilog models on VHDL-XL.

In short, whatever you’re using, you’re left with a design methodology full of holes, one that needs a lot of work before it will facilitate full-system designs. Though one language is the best answer over time, it’s not impossible to have multiple languages, according to Cadence’s president and CEO Joe Costello. He adds, “The tragedy [would be] if there are two HDLs, and we don’t make them workable for the system designer.” Costello states that the semantics and syntax of VHDL and Verilog may not be the same, but that standard practices for the two could be.

**Common ground**

It’s the standard practices and standard operating environment that make Verilog look better than VHDL on the implementation side, Costello explains, whereas VHDL, with its high-level constructs, is more robust at the system level. “Why not take everything you possibly can from the standard practices and operating environment of Verilog and incorporate them into VHDL to make it workable?” he asks. Cadence has decided to stay with its VHDL-XL, which shares simulation algorithms with Verilog-XL, instead of putting its support behind the Valid/Intermetrics VHDL simulator. VHDL-XL will have full language support by the fourth quarter, according to Costello.

He urges fellow vendors to stop hassling over languages and serve the user by putting energy into simulator performance, model availability, higher-level constructs, and methods of hiding the complexity of VHDL for ease-of-use. And he has a message to you, the user: “Take a leap of faith. Be part of the team that makes VHDL successful. VHDL is a long way from success at this point. There’s too much vendor influence in VHDL and not enough input from users. Take control of both VHDL International (VI) and Open Verilog International (OVI) and combine the best of both worlds.”

Andreas Hohl of Siemens (Munich, Germany) is chairman of...
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VHDL and Verilog makes sense. "There's no need to mix the languages," says Hohl, "but Verilog extends VHDL. "If VHDL claims experience could be helpful with rec

The VHDL Forum for CAD in Europe. He agrees that from a user's point of view, the coexistence of VHDL and Verilog makes sense. "There's no need to mix the languages," says Hohl, "but Verilog experience could be helpful with recommended practices." Much more effort is required, according to Hohl, to establish VHDL. "If VHDL claims to be a system language, we need to extend it to cover all system components, including analog and mechanical." Asked about the feasibility of merging VI and OVI, Hohl says the two groups might at least share common projects.

Discussions are indeed taking place between VI and OVI on the interoperability of VHDL and Verilog models. As chairperson of the VI Technical Advisory Committee, Dave Coelho, who's also executive vice-president at Vantage Analysis Systems (Fremont, CA), has entered into discussions with Hal Alles, corporate architect for Mentor Graphics (Wilsonville, OR), who chairs an OVI committee looking at model interoperability. "A special project committee sponsored by both groups is quite possible," reports Coelho. "We'll look at a whole range of solutions, including the possibility of VHDL and Verilog simulators talking to each other, as well as the possibility of translating models from one language to another."

I Getting together on timing

The second area being considered as a possible common VI/OVI project is the review of the VHDL timing problem and establishment of a standard back-annotation file format for VHDL. VHDL designers going to silicon today have to use proprietary tools and ad hoc methods to settle timing issues. Though VHDL does contain configurations that can be used for this purpose, the methodology is reportedly clumsy, inefficient and not at all practical for large ASIC designs. Dr. Vassilios Gerousis, CAD system evaluation manager at Motorola (Chandler, AZ), chairs both an OVI committee on library modeling and a VI-sponsored IEEE working group evaluating a timing methodology for VHDL. Such a duplication of efforts has led to expectations that a special project group might be formed that would span both VI and OVI.

In the meantime, Cadence has proposed its Standard Delay File (SDF) to the IEEE working group as a neutral format for storing delay information. SDF is currently being widely adopted by ASIC vendors of Verilog libraries. VHDL purists might argue that SDF is external to VHDL, but Victor Berman, responsible for language strategy at Cadence, as well as being chairman of the North American Chapter of the VHDL Analysis and Standardization Group, says, "I don't deny it's outside the spec, but this is engineering, and the name of the game is to get the job done. Sometimes purity has to suffer for efficiency."

Mentor Graphics, which recently announced a multiphase program that will incorporate Verilog-XL into the Falcon Framework so that you can have access to Verilog as well as VHDL, had hoped that its Advanced Modeling Process (AMP) modeling specification would be adopted as the industry standard. Mentor is likely to insist that some of AMP's attributes are incorporated into SDF, or whatever timing methodology is finally adopted. SDF seems to have the edge since it has been adopted for Verilog.

If Verilog and VHDL are to be used together, it would make sense for the delay format of the two to be the same, independent of both languages and reflecting the physical hardware, according to Berman. Not only would the same timing semantics for simulation make sense if you were modeling in VHDL and Verilog together, but it also would if you were using the two HDLs separately, since it would let you compare what's happening with the expectation of similar results. For ASIC vendors, the same timing semantic for Verilog and VHDL would mean developing a single delay calculator, with a little difference perhaps in output formats for the two.

I Cast your vote

Ultimately, it will be you, the user, who'll decide whether you want a single language over the long term. In the meantime, get in touch with VI and OVI and ask what you would get out of becoming a member. Since the IEEE is today the keeper of VHDL, it seems that a merger of VI and OVI is way more complicated than it might sound, as well as being highly unlikely from a political point of view, so you'll have to decide between VI and OVI, or you can join both. Watch, though, for special project groups that span the two.

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Superscalar Sparc chips offer performance gains, compatibility

Tom Williams, Senior Editor

Superscalar design has now come to Sparc RISC architecture. In efforts to boost performance while avoiding many of the system design pitfalls caused by cranking up clock speeds to 100 MHz, Cypress Semiconductor (San Jose, CA) and Texas Instruments (Dallas, TX) have opted for parallel instruction launch and multiprocessing based on the widely popular Sparc architectural specification. Each has announced superscalar implementations of Sparc that will allow virtual drop-in performance upgrades for existing system designs and will run existing binary code—with significant performance gains.

The Texas Instruments TMS390Z50 SuperSparc CPU chip and the Cypress CYM6200 HyperSparc family of processor modules differ significantly in management, bus interface, 20-kbyte instruction cache, and 16-kbyte data cache. TI's design uses 3.1 million transistors on a 15.8 mm² die; it's implemented in TI's 0.8-µm Epic IIB triple-metal BiCMOS process. The Cypress CYM6200 family, which initially will have three versions, is based on three ICs in its HyperSparc chip set integrated on an M bus module.

The CYM6200 family of modules consists of three elements: the CPU, the CY7C625 cache controller/MMU tag unit, and two or four CY7C627 cache data units. Modules in the family differ by having one or more CPUs and two or four cache units (128kbytes or 256kbytes respectively). The CY7C620 CPU includes integer and floating-point units and an 8-kbyte two-way set instruction cache; it's capable of launching two 32-bit instructions per cycle. It contains 1.2 million transistors. The cache controller/MMU unit controls the cache memory units that are not integrated on the CPU and also interfaces to the M bus at 40 MHz. The CPU modules communicate via a proprietary intramodule bus that can scale in speed as the internal CPU speed is scaled upward to 100 MHz, while maintaining a separate clock for interfacing with the M bus.

The TI SuperSparc chip also maintains separate clocks—not, as in the Intel 80486, a single clock with divided frequencies—so that the processor can run faster than the interface to the M bus for ease of upgrading system performance.

According to Roger Ross, president of Ross Technology (Austin, TX), the Cypress subsidiary that developed HyperSparc, cost played a major role in the decision to partition the design among IC modules. "When you double the size of a piece of silicon, you double its price," he says. Also, he noted that Ross Tech-

In the Cypress HyperSparc CY7C620 CPU, the two-way set associative instruction buffer can store 2,048 64-bit instructions. The core data path handles all integer instructions, plus load and store. It has eight overlapping register windows and eight global registers (136 total). The core instruction scheduler decodes, groups, schedules, and dispatches instructions. It can launch two instructions per clock cycle to any two of the four logic blocks (load/store, branch/call, integer, and floating-point).
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nology's approach to building chips as if they were software projects makes it easier to partition the work, by using a smaller design team and putting off the commitment to actual physical layout until late in the design cycle.

**Modules do even more**

The major area of competition—and no doubt the largest market—for Cypress and TI will be in M bus modules, since TI will be offering a family of M bus designs as well. The SuperSparc M bus module consists of a single CPU chip on a standard M bus plug-in board. A module with more external cache memory is also available in the form of the Multicache module, which includes the SuperSparc multicache controller and 1 Mbyte of SRAM cache memory. In 1993, TI will introduce a dual-CPU Multicache module. All “glue logic” for multiprocessor interfacing is incorporated on-chip on the TMS390250.

In addition to running on the M bus, the TI Multicache modules can be selected to operate on the X-bus packet-switched mode developed by Xerox for very large-scale multiprocessing. The X-bus interface is contained in the SuperSparc cache controller, and can interface with up to four system buses via bus adapters. Where M bus can handle up to four CPU modules, X-bus designs can be implemented with up to 64 modules—which could approach 10 billion instructions per second at 50 MHz. Cypress hasn’t specifically targeted its modules for use on X-bus, but “there are good technical ways to get there,” according to David Ditzel, director of the Advanced Systems Group at Sun Microsystems (Mountain View, CA).

Interestingly, both TI and Cypress developed their superscalar Sparc implementations in close cooperation with Sun. Sun is still evaluating which of the offerings it will select for its system designs. With 63 percent of the Sparc market worldwide, Sun will represent the plum in terms of design wins. But, as Ditzel points out, TI and Cypress/Ross “have made different trade-offs in different directions and neither CPU will go into all platforms.” Cypress’ stated aim in implementing a smaller number of transistors per die and using a two-metal CMOS process was to build a CPU module for volume manufacturing suited for low-cost desktop systems. The eventual pricing announcements from Cypress should tell the story there.

**Performance gains right away**

Both TI and Cypress are claiming immediate performance gains of 2 to 3× over previous Sparc implementations using existing applications and compilers. Actual performance differences between RISC chips are always hard to quantify without exact measurements that deal with such questions as: how many Specmarks at what clock speed with what cache? The two companies’ claims also quote different clock speeds and make the usual differing estimates of the other’s performance when doing comparisons.

But Eric Schmidt, president of SunTech, Sun’s software business development branch, says the real story is in the software compatibility that comes with the performance gains. “At least a doubling in performance at the same clock speed simply
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<td>x 4</td>
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*Self Refresh 1DW- Dual Write Enable 1DC- Dual CAS 1FPM- Fast Page Mode 1SC- Static Column 1OE- Output Enable
by plugging in a different M bus module is a virtual certainty in both cases, even if we wait until later to sort out the details." Add the multiprocessing capability offered by both vendors, and price/ performance will go even higher. Schmidt notes that Sun's new Unix operating system, Solaris (Versions 1.0 and 2.0 are out), already has multiprocessor support. He predicts that future systems will be "multiprocessing multithreaded everywhere."

While these gains are available immediately on the hardware side, compiler technology will take some time to exploit the opportunities offered by the new implementations. Schmidt wouldn't speculate as to what increments of performance improvement could be expected from compilers that could take advantage of such things as scheduling instructions for parallel execution and making more efficient use of the pipeline. Wayne Rosing, president of SunLabs, Sun's R&D group, suggested, though, that users would be "pleasantly surprised."

Sun's Ditzel points out, however, that advances in compiler technology in the Sparc world usually benefit all Sparc hardware implementations. Furthermore, code generated by a compiler tuned for the Cypress or TI superscalars would still run on other Sparc implementations, even if not as efficiently.

As to development support, SunPro, Sun's development tools branch, has announced support for the TMS390Z50 with its Sparcworks suite of development tools. At the same time, SunPro announced that it was working on releases of its tools, especially compilers, that could further exploit the TI SuperSparc's superscalar features. Sun hasn't made any announcements regarding support of the HyperSparc, but existing Sparcworks tools will be binary-compatible as well.

For its part, Texas Instruments is supplying a $50,000 system design starter kit consisting of a SuperSparc simulator that includes additions for caches, MMU and store buffers, a Verilog model that allows behavior modeling of the CPU and the Multicache/bus controller, and a JTAG-based scan tool for boundary-scan testing of board- and system-level designs. The kit also includes documentation and an M bus designer's guide.

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Tool suite targets 32-bit microcontrollers

Tom Williams, Senior Editor

The complexity and specialization of today's 32-bit designs are throwing new challenges at development tool vendors. Complexity translates as 32 bits, and specialization means microcontrollers with all their application-specific peripheral devices, such as timers, I/O, RAM, ROM, and DMA controllers. The upshot is that ever larger and more complex programs have to be created and maintained by an engineering community that's facing shortages of both people and experience. The task of producing tools that are affordable, adequate to the job at hand and usable by this overstressed community has become daunting.

According to Richard Jensen, vice-president of new business development for Applied Microsystems (Redmond, WA), 32-bit embedded systems are making increasingly heavy demands on software engineering resources—roughly double the demands of 16-bit projects. By contrast, the demands on hardware engineers have risen only moderately.

System know-how

The fragmentation of applications into specialized areas is driving two trends. One is, of course, that semiconductor vendors are addressing specialized application areas (automotive, military/aerospace and communications) with specialized microcontrollers. The second is a crisis in experience. There's a serious shortage of experienced software engineers, although software engineering is only part of the problem. A good programmer may not have adequate knowledge of the application being programmed, and a person with detailed knowledge and experience of the application may not be an experienced programmer.

"Application experience is a far more valuable thing to put on a team than programming experience. A company doing a sonar is better off getting a chief petty officer off a submarine, and they'll teach him how to program," says Jensen. But somebody has to know the insides of the processor or microcontroller to help him out, Jensen adds, "and that pressure is being put on the tool companies." So, on the one hand, an applications expert has to learn enough about general-purpose programming to apply his or her knowledge, and, on the other hand, tools have to shield this expert from the need to deal with the detailed inwards of the specialized and very complex microcontrollers being worked with.

Estimates by Applied Microsystems show that a typical 32-bit embedded system project may have from three to five hardware engineers, but requires between 10 and 30 software engineers. With that many people being paid hefty salaries, a development organization faces the challenge of how to give them all useful tools without spending itself out of existence, how to keep them all productively busy and how to achieve the best time-to-market.

One caveat Jensen offers is this: "Doing your own real-time kernel is the worst business decision you can make." In this situation one or two engineers are doing what vendors who are experts in the field have already done very well, while the rest of the team is waiting to start the project. Beyond that, Applied Microsystems is pushing its concept of a proper mix of tools in an integrated environment that includes software simulation for binding code to the hardware environment and emulation for solving the most complex timing-related problems.

Where it was once acceptable to equip each of the one or two software engineers on an 8-bit project with his or her own $5,000 emulator, emulators for 32-bit microprocessors are too expensive for the larger teams of engineers needed for this work. But the generic activities remain the same: write and debug the code's logic, bind it to the target hardware's physical environment and check and debug timing-related issues.

Tackling 32-bit controllers

Applied Microsystems has made an aggressive thrust in one segment of the 32-bit microcontroller arena with suites of tools for three members of Motorola's CPU32 family. The supported processors are the 68330, 68340 and 68333, each of which is based around the 68020 CPU core but with its own mix of on-chip peripheral devices. The company's strategy is to emulate the core processor and isolate the application-specific functions—to switch to a dif-
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different microcontroller, then, you need only change the probe head and software on the same emulator box.

The CPU32 family of development tools consists of an instruction set simulator, a CodeTap hardware debugging probe and a 32-bit emulator. All tools are tied together via Applied Microsystems' Validate/XEL interface, which is based on Hewlett-Packard's Softbench environment.

With the instruction set simulator, you can begin developing and debugging target-specific code on the host system before any target hardware is available. You can write high-level source code on a PC, Sun or DEC workstation, compile it to the target code and debug at either the source or assembler level. The simulator is aimed at solving problems of code logic that are not dependent on hardware but are usually the most numerous in any operation. With prices starting at $2,000, the simulator can be provided for almost everybody on a project.

For the majority of hardware-related integration problems—that is, fitting the code to the target environment in terms of I/O addresses, memory ranges for ROM and RAM, interrupt lines, and other factors—Applied Microsystems supplies a CodeTap tool for each of the three supported members of the CPU32 family. CodeTap's probe head carries a microcontroller plus a monitoring chip that lets you set hardware breakpoints and debug code in the hardware environment without actually using any of the target's memory or I/O resources. Debugging doesn't include the detailed timing-dependent problems which require a full emulator. But with the EL3200 emulator selling for about $20,800, the $6,500 CodeTap provides a cost-effective solution for the hardware-binding class of problems.

Applied Microsystems will also be sourcing Motorola's single-board evaluation boards for the CPU32 family. Those who want to get started running code immediately on target hardware need only plug the CodeTap head into the evaluation board. Of course, the evaluation board may not have all the characteristics of whatever specialized system is under design, but it provides a means of making progress at the

"Application experience is a far more valuable thing to put on a team than programming experience."

—Richard Jensen
Applied Microsystems

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hardware/software integration stage before a final design prototype is ready.

Finally, Applied Microsystems has developed a version of its EL 3200 emulator for the CPU32 family. The EL 3200 comes with a probe head for one of the supported microcontrollers; the other heads and their associated software can be substituted. An optional 16-bit logic state analysis probe is available for monitoring points of interest in the target system.

**Emulator's new features**
Among the new features of the EL 3200 are the ability to set breakpoints in ROM or in shared or dual-port memory—especially useful for embedded systems—as well as its dynamic pin tracking. The 68330 and 68340 have pins that can be configured in software to serve different functions. For example, the upper eight address lines can be used first as address lines and then switched to act as a parallel port. What's more, this can be done dynamically as the program is running. The EL 3200 can keep track of such switchable pins by monitoring the instruction stream via the instruction pipeline and instruction fetch signals, looking for writes to the internal registers that configure the states of the external pins.

The proliferation of microcontrollers has presented a large challenge to tool vendors, because no single CPU can cover all the vertical markets. But as Jensen notes, "This is an expanding market because they [the semiconductor manufacturers] are doing this, they're getting greater application opportunities." Given the intricacies of the different controllers, the prospects for tool vendors to provide adequate tools for developing systems are also quite challenging. Meeting that challenge will require ever more effort from tool vendors, as well as cooperation from semiconductor vendors.

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CIRCLE NO. 29
Major board vendors keep up with shift from traditional bus-based systems

Warren Andrews, Senior Editor

Although the standard-bus industry continues to leverage its way into proprietary-bus solutions in many application areas, the same standardized boards that are replacing proprietary solutions are being abandoned by designers who have traditionally relied on them to build systems around non-proprietary buses, primarily because of size and cost. In response, board vendors are beginning to offer alternatives which may be the first steps in a changing of the guard, fragmenting once-sacred VME application areas.

The processing power and I/O now available on a single board are making it possible in many cases to eliminate a backplane and interface circuitry, as well as software for multiple-board solutions. On the other hand, another set of applications is emerging that's so complex that new multiboard solutions are being sought.

There's been change for some time at the high end, what with multiprocessor boards, fault-tolerant hot-swap systems and fast crate-to-crate communications, but low-end systems are just starting to veer away from the traditional. The first to take advantage of the shift from traditional VME use has been Sun Microsystems (Mountain View, CA), which not only offers an alternative to VME, but announced it will soon get out of the VME business altogether in favor of its single-board solutions depending on SBus modules.

Force Computers (Campbell, CA) has followed Sun's lead by offering its 2S board, primarily a VME single-board computer without the VME interface. Unlike Sun, though, Force plans to remain a power in the VME business. In fact, it's part of Sun's strategy to transfer its technology to Force, so that the latter company can continue to support those of Sun's customers wishing to stay with VME solutions.

The most recent company to offer what is essentially a 'busless' solution is Motorola (Tempe, AZ), which will offer both a VMEbus and a busless version of its latest SBC, the MVME162. But Motorola's approach varies significantly from that of both Sun and Force.

First, of course, it's based on the Motorola processor, not on Sparc. But other differences are equally significant. "The MVME162," says Jerry Gipper, Motorola's director of VME components marketing, "is targeted at a specific group of users, both in the VME and stand-alone versions. It's designed to be flexible and easily configured to adapt to a wide variety of applications in the industrial control and automatic test equipment areas."

The MVME162 is also quite different from any of the company's earlier single-board efforts. For example, it offers no Unix support, being designed exclusively for real-time applications. And it offers a large number of different memory configurations, as well as Ethernet, SCSI and floating-point support. (The basic board is fitted with a Motorola MC68LC040 processor, a 68040 with the floating-point unit stripped off and low-power memory buffers added.)

First with IPs
But the most important difference between the MVME162 and any other Motorola offering—and any other mainstream 6U VME board, for that matter—is the inclusion of sockets for three or four IndustryPack modules for including special functionality. IndustryPacks, devel-

MVME162 block diagram

Motorola has broken with tradition and may be setting a major trend with its MVME162 single-board computer, which is offered with or without a VME interface, and with three or four IndustryPack sockets for I/O modules. This board is designed to sell with a 25-MHz Motorola 68LC040 (68040 without FPU) for under $1,000 in OEM quantities.
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CIRCLE NO. 30
It's an open standard, is bus-independent, has multivendor support, offers a double-size option, and modules available fit closely with the target application area of industrial automation." Gipper also points out some of the other features of IndustryPacks, including two clock speeds, all logic pins fully defined, CMOS interface levels for low power, 50 or 100 I/O lines per module, good interconnection with the

Motorola has either three or four sites for IndustryPack modules to be included on its MVME162 single-board computer. IndustryPacks are compact boards (1.8 \times 3.9 \text{ in.}) with two 50-pin connectors, identification PROM and on-board Pi filters.

carrier board, module identification PROM, and amenability to high-density surface-mount designs.

"The IndustryPack concept," says GreenSpring's executive vice-president, X. Kim Rubin, "was created to mate with the VME form factor, either 3U or 6U, to provide an efficient I/O flexibility not available with other technologies. Compared, for example, with SBus, IndustryPacks are very low-cost and provide just what's needed for industrial control applications."

One up
Apart from providing a very flexible platform, 27.8-Mips performance with a 25-MHz 68040 or 68LC040, versions with and without VMEbus interface, and a variety of Industry-Pack options, Motorola's coup de grace is price. According to Gipper, the board in a standard VME configuration is expected to sell for "well under $1,000 in OEM quantities." This makes it one of, if not the, lowest-priced, full-featured SBCs on the market.

Gipper claims that the combination of Motorola's manufacturing technology for its six-sigma quality line with the anticipated sales volume of the new board makes the low price possible. In comparison, Motorola's previous price leaders, its MVME147 and MVME167 products, have been at close to twice the MVME162's price. (There have been periodic reports, however, that prices have been substantially lowered on these parts to meet the demands of very large customers.)

Motorola's use of IndustryPacks marks the first time any of the top ten VME board makers have adopted a standard mezzanine bus. The exception has been Force, which has included SBus slots on its SBCs as part of its arrangement with Sun. Motorola's adoption of GreenSpring's IndustryPacks, however, is not part of any major technology-swapping arrangement, though Motorola will be reselling GreenSpring's modules.

More important, Motorola's move may mark the beginning of a shift for VMEbus-based systems. Traditionally, users of VME in industrial control applications have relied on multiple VME boards to implement a complete system. This necessarily included a backplane, as well as the software to make sure everything ran smoothly across the VMEbus—something of a problem in the past. Now, with the shrinkage of semiconductor geometries and the broad availability of ASICs, it's possible to condense the functionality of several boards onto a single one.

Users are anxious to take advantage of the resultant smaller space, lower cost and higher reliability inherent in such single-board, busless approaches. But developing suitable products has turned out to be more of a job than simply reconfiguring a standard board. In Sun's case, its approach was to deliver a full board-based Unix platform with the versa-
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tivity of SBus modules. Motorola, on the other hand, is vying for a big chunk of the industrial control business by offering a variety of modular I/O approaches and flexibility, as well as a standard-bus option.

While Motorola is the first major VME maker to offer both a bused and busless version of its SBC, GreenSpring itself offers a single-board busless board utilizing Motorola's 68332 communications processor along with a number of IndustryPack sites. The board GreenSpring has dubbed the Platform 332 supports six Industry Packs and, according to GreenSpring president Henry Lehmann, "offers VME performance and software compatibility without a backplane."

New technologies advanced

Bringing out a busless 680X0 board may not be a big shot in the arm for the VME industry, but it may well forward two technologies. First, PC platforms have enjoyed a relatively uncrowded field for small, embedded SBCs. Users with applications that called for more than a PC, yet who couldn't afford the space and cost of a backplane-based system, often elected proprietary approaches. Now they have an alternative.

Second, Motorola's move may well put IndustryPack on the map as a viable technology. Though IndustryPacks have been around for quite some time, their use hasn't exactly grown explosively. Motorola's approach has created an opportunity which may well attract followers. The approach provides a sensible alternative for relatively low-performance I/O without the need to go to a full VMEbus board, or to provide a custom solution.

It will probably be some time before the jury is in on the new Motorola offering—samples of the board won't be available for another month or so. But development alternatives are already available in terms of a standard MVME167 combined with a GreenSpring IndustryPack carrier board. In addition, IndustryPacks have apparently been used in a number of systems utilizing proprietary boards in the recently completed European Disney entertainment complex. And IndustryPacks are used by GreenSpring as well as some 20 other companies in a wide variety of applications.

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EDA vendors unveil tools for rules-driven layout

Mike Donlin, Senior Editor

In this photo of Cadence's Preview floorplanner, a critical path is displayed graphically and highlighted for analysis. In the lower part of the screen, a table compares the highlighted path's estimated delay versus the user-specified timing constraint.

Many IC companies are lining up behind the doctrine of concurrent engineering and embracing the end of the "over the wall" methodologies of the past. Traditionally, design engineers created and simulated the logical portion of an IC or ASIC and then passed the resulting netlist information to the layout specialist for component placement and routing. This method removed the design engineer from the physical implementation of his or her ideas, and often resulted in costly iterations.

Bridging the gap

Bridging the gap between the two camps is difficult, however, because many designers don't want to get involved with the drudgery of physical layout, and layout specialists don't often cross over into the hallowed halls of the design engineer. EDA vendors are responding to this dilemma with tools that tie vital design information to the physical design of the silicon, in effect making rules-driven layout a reality.

"Some of the most essential data is in the critical timing paths," says Isadore Katz, vice-president of marketing for the IC design division at Cadence Design Systems (San Jose, CA). "Growing chip complexity and submicron geometries are making timing constraints tighter than ever, and it's important that they're dealt with early in the design phase. In yesterday's standard designs, for example, a typical 5-ns clock skew budget translates to about 1.5 m of wire. Today's budget is more on the order of 100 ps, which comes out to about 3 cm of wire. Obviously there's no room for error in the place-and-route domain."

To help designers and layout specialists meet these tight timing constraints, Cadence has recently released Preview, a foundry-independent automatic floorplanning and analysis environment for IC design. According to Cadence, Preview links logical and physical design by bringing floorplanning and analysis information to an early stage in the design cycle, which will give designers confidence that their designs will meet size and performance goals on the first pass through physical place-and-route.

"Floorplanning is important because it gives the designer critical timing information, such as interconnect delay, while the design is in the flexible concept phase," says Donna Rigali, senior product manager at Cadence. "Floorplanning isn't the same as actual placement, because it's tied to the logic design portion of a product's development. It's high-level partitioning information as opposed to final cell or gate placement."

Preview contains tools for prediction of timing, size, congestion, and routability. Given a set of design constraints, the tool analyzes alternatives and creates a floorplan which the designer can optimize for performance.

"These types of tools are necessary for our leading-edge customers who are megahertz driven," says Fuad Musa, director of strategic CAD programs at the ASIC division of the Motorola Semiconductor Products Sector (Phoenix, AZ). "From a silicon point of view, things like parasitic and wire delays are becoming a bigger factor in terms of the percent of the total delay. The more that you know about these effects when you're conceptualizing a device, the more intelligence you'll build into your designs. This leads to better optimization of the design and more performance from the silicon. It also gives you more confidence that the device will work and keeps you from being too conservative with the resources that the technology offers."

Winning designer confidence

If there's a flaw in all this, it's the assumption that designers will trust automatic design tools enough to actually use them. EDA vendors have to win converts to the concept that software can be a reliable guide for an experienced designer who may be directed by the tool to alter a design.

"We believe that chip complexity will force the issue," says Bruce Yanagida, manager of software architecture and manufacturing operations at Cascade Design Auto-
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I TECHNOLOGY DIRECTIONS

CAE/CAD TOOLS

It's next to impossible for a designer to keep track of all the rules during a product's development. By bringing process-specific design rules to the front of the cycle, we've relieved the engineer from worrying about violating a rule that will haunt him later. It's also important to keep the tools interactive, so that a designer can go in and tweak the automatic tool's results for best performance.

At last month's Design Automation Conference in Anaheim, CA, Cascade unveiled its IC design suite, Epoch. The tools target performance-driven layout and feature a collection of module libraries, including standard cells, memories and datapath elements. An interactive timing analysis capability keeps the designer involved in the project. By incorporating IC-specific information into the tool set, Epoch accepts user constraints and uses timing and load analysis to drive placement, routing, buffer sizing, power and clock distribution, and is critical to ensuring a design's accuracy," says Barry Roitblat, Cascade's director of marketing. "Particularly with submicron technology, you have to model the chip so that when it comes back as a device you have some degree of confidence that it will behave the way you think it's supposed to. This means accurately modeling the delays of components and interconnects so you can do a distributed analysis of the delays to avoid things like race conditions in the final design."

Keeping designers involved
Interactive floorplanners, like Cadence and Cascade's, are targeted at skeptics who might not trust a fully automated tool and are also aimed at seasoned designers who know more about their processes than could ever be built into software. For example, Cascade's FloorPlanner, part of the Epoch suite, lets you change the placement or orientation of a cell, swap cells, reshape a cell or group of cells, or regroup sets of cells into flexible blocks. This lets you improve chip density or minimize route lengths.

An improvement in chip density, however, is often achieved at the expense of overall route minimization. Routes are minimized by placing cells closest to other cells with which they communicate most heavily. FloorPlanner graphically displays the amount of this communication as force vectors, represented by an arrow originating from the center of a cell, which sums up the length and direction of the nets connected to that cell. Any movement of a cell in the direction of the arrow will tend to reduce the length of the routes connected to that cell.

All of these tools are aimed at narrowing the gap between concept and reality, but they also let you get the most from the final silicon. There's a fine line between squeezing as much performance from a device as possible and being too careful and not designing up to the technology's full potential. "Silicon vendors tell you that they have 40 or 50 or 60 percent utilization of actual gates," says Motorola's Musa. "That's quite a range, and just how much you're going to get from your final design depends on how well the design is thought out. It's not unusual for a customer who's pushing the maximum number of gates in a design to find out that the silicon vendor couldn't place and route it and had to take something out or change the design. No one needs that kind of aggravation. With the right tools, you know your limitations and capabilities early on, so you get what you designed."
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Automation improves speed and accuracy of software testing

Testing complex software applications is a tedious task best left to machines. New methods of automating the process promise payoffs in terms of shipping higher-quality products.

Tom Williams
Senior Editor

There's an old cliché that says if you put enough monkeys in a room with enough typewriters for long enough, they'll produce all the great works of literature. For a long time there's been a similar myth about software testing. But locking a bunch of college students in a room with unlimited pizza and turning them loose on a software product can no longer be considered a credible form of software testing—if it ever was. Today's software products have become so large and so complex, and in many cases so critical to life and safety, that a more systematic and disciplined approach to software testing has become imperative.

But exhaustive software testing entails two elements that discourage human operators and make them prone to mistakes: repetition and tedium. Creative people such as programmers instinctively balk at the idea of long hours exercising every function of an enormous program over and over with the only variety being different input values to be compared with different expected outputs.

Now that an ever-growing number of applications, including a large number of embedded systems, are using window-based user interfaces, the problem is only getting worse. If anything cries out for automation, it's a way to thoroughly test software.

Help is on the way

Fortunately, a number of tools at a range of prices and offering a variety of capabilities are appearing to help developers automate the testing process at the user interface level. Basically, testing at this level entails supplying the system's various functions with inputs and comparing the system's reaction with expected outputs. It also includes deliberate attempts to crash the system so that the code that's finally shipped doesn't fail because of wrong inputs.
I SOFTWARE TESTING

For embedded systems, there's also a need to exercise inputs and outputs that aren't addressed by the user interface but that, in the final product, are used by sensors and actuators. Still, even those tools that are limited to testing at the graphical user interface (GUI) level can greatly reduce the amount of testing tedium for embedded systems which require interaction with a user via a GUI.

GUI-oriented testing tools come in two basic flavors: software-only tools that reside on the same CPU with the application under test, and hardware-assisted tools that run on a separate platform and intercept the signals of the application system's keyboard, mouse, video, and other I/O. As you can imagine, there's a significant price differential between the software-only variety and the tools based on separate hardware.

Software-only test tools such as MS-Test from Microsoft (Redmond, WA) and SQA Robot from Software Quality Automation (SQA—Lawrence, MA) have become practical with the advent of window-based GUIs that have a solid application programming interface (API). Both MS-Test and SQA Robot reside in memory on the same machine that's running the application under test. They can achieve a high degree of nonintrusiveness to the application because they interact with it only via the Windows API, the same as a user would.

I Staying out of the way

The issue of being nonintrusive is a hotly contested one among test tool vendors, with the hardware-based toolmakers claiming totally nonintrusive testing. When it comes to window environments such as Microsoft's or X Windows, David Snow, SQA's vice-president, points out, "Lots of things are supposed to coexist on the desktop. So guess what? If Robot is going to bring down your application, so is your word processor."

Hardware-based testing tools, such as TestRunner from Mercury Interactive (Santa Clara, CA) and Ferret from Tiburon Systems (San Jose, CA), do attempt to keep absolutely isolated, not only from the software application under test but also from the hardware platform and operating system the software's running on and under. Each system consists of a personal computer that runs the test software to control and monitor the system under test, along with a connector box that intercepts the keyboard, mouse and video signals of the target machine. The program running on the tester platform can then input keystrokes and mouse movements directly via the hardware lines of the application platform.

The hardware-based testers can also pull the video signal off the target and compare the screen produced by the application—pixel by pixel, if need be—with the expected resulting screen stored on the test platform's disk. Both TestRunner and Ferret include hardware accelerators for image processing. They can capture full-screen images from the target and quickly compare them with screens stored on their internal disks.

Standing somewhere in between is another GUI-oriented test tool, AutoTester Plus from AutoTester (Dallas, TX). AutoTester Plus comes in both a character-oriented and a Windows version, and can run either target-resident or on a separate platform. Another product from Mercury is a software-only test system called XRunner, which resides on X Windows systems and interacts via the X Windows window manager.

I Tool differences

Along with their relatively high price tags, the hardware-based systems do offer some capabilities not available from the software-only tools. For one thing, if a test causes an application to completely hang up the system, the hardware-based tester can do several things. It can be programmed to halt and dial the test engineer at home in the middle of the night, or it can log the failure, reboot the application system, go to a known state, and continue testing. The hardware-based systems can also monitor I/O lines other than those accessed by the user, which is an advantage when testing those parts of an embedded system that aren't directly touched by the user interface. Such a system can even be used to control a simulator—perhaps running on yet another platform—which will send input data to nonuser I/O ports which can be correlated with the testing at the user interface level.

Both Ferret and TestRunner, since they interact with the target only via user interface lines and are independent of the target's operating system or window API, can be applicable to more than one target. TestRunner will work with IBM PCs, Macintoshe s, Unix workstations, and others. Ferret has interface adapters for DEC, Sun, Silicon Graphics, X terminals, and many more. The result is that you have to learn only one set of testing tools to be applied to many different target systems.

According to Mercury's director of marketing, Tall Aben, another advantage of a hardware screen image processor/comparator is that it accurately reproduces varying delays in responses that might confuse a system that was simply playing back a script. "I could play back a window normally 99 times and have it pop right up," she says, "but what hap-
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Letting testing to find the bugs.” So testing to prove to your condition that can cause failures and see how the system reacts. “If a program calls for a value between 1 and 1,000,” says Pope, “put in ‘ABC’ and it shouldn’t blow up.” It should return an error message or provide some kind of “soft landing” that won’t cause a general failure or a possibly catastrophic action. One need only remember the story of the bug in a fighter plane’s navigation software that caused the aircraft to flip upside down when it crossed the equator—a bad interpretation of the term “down under.”

At the foundation of all GUI-oriented testing tools is the ability to emulate a user by capturing and playing back his or her interaction with the application—recording keystrokes and mouse activity. Whether a testing tool is a software-only tool or running on separate hardware, the capture/playback approach has the immediate ability to do something. So testing tools have been provided with varying degrees of programmability in addition to their recording ability. For example, programmability lets you capture a series of keystrokes that exercise a feature and then embed those keystrokes in a loop. The exercise of the feature can then be repeated as often as desired while stepping through a series of input values or options, making it possible to extensively test the given feature automatically with a compact coded script. You could also run a series of operations in one mode, then switch to some other mode and replay the same operations many times without having to recapture or rewrite a script.

**First steps to automation**

The ability to program test scripts bestows the capability to begin automating the tedious testing process. But test-scripting languages by themselves tend to require a closely detailed knowledge of the code to be tested—more so than is required for creating scripts from straight capture/playback. The advantage is that such language-based scripts can be more systematic and compact. The SQA Robot tool, for example, supports capture/playback as well as the creation of scripts using Microsoft’s Visual Basic language. Visual Basic, as the name suggests, relies heavily on interaction with elements of the GUI and lets you build test cases without much detailed knowledge of the underlying code. But these test cases are more systematically programmed than mere capture/playback sessions.

For more detailed scripting, SQA has built-in hooks in SQA Robot to let it work with the MS-Test tool from Microsoft. Microsoft MS-Test includes, in addition to capture/playback capability, two levels of programmability for creating test scripts. FastTest works at about the level of Visual Basic working with SQA Robot. It lets you create test scripts for Windows applications that verify basic functions (such as the existence of an application’s menu items), respond to dialog boxes and save and open files. The ‘BListBoxExists’ function, for example, checks to see that a list box with a specific name exists and logs an error if it doesn’t.

At the next level, MS-Test provides a test programming language called TestBasic that provides familiar control structures such as FOR...NEXT loops and SELECT...CASE constructs to do things such as extensively embed captured keystroke sequences in loops to step them through sequences of data. MS-Test comes with four dynamic link libraries (DLLs), from which it can call a wide range of functions to test applications. Many DLL procedures cover events, such as the ability to send keystroke and mouse movements to an active window. Others check the existence or status of controls such as menu items, check boxes and list boxes. Still others let the tool capture and compare windows.

The higher the level of programming power you select for creating test scenarios, the more efficiency and detail you can expect from your tests. That greater detail, however, requires a closer knowledge of the program code and more preparation before testing begins. In fact, the Microsoft manual admonishes the user that “although it takes time to develop the test software, this time
Recent advances in PC-based software test automation, coupled with an ever-expanding array of PC-compatible boards and devices, have made it possible to automate the testing of embedded software systems by capitalizing on the PC's ability to emulate or communicate over a wide variety of protocols at a reasonably low cost.

Powerful and flexible PC-based memory-resident software-testing technology is now available which can execute co-resident with other applications, communications or emulation programs and drive them as directed by a script. Scripting languages support input and output to and from the screen, disk and keyboard, and provide logic to evaluate and respond to results while documenting exceptions.

This combination of software and hardware makes it possible to develop an automated test operator that can test any software executable by, or accessible from, a PC. The result is a fully automated test operator which can be easily and quickly configured for various devices and applications.

Testing fire alarms
Simplex Time Recorder Company (Gardner, MA), a premier vendor of electronic fire alarm systems, offers a sophisticated monitoring and response panel for detecting and responding to fire conditions in buildings. The panel's embedded software constantly monitors and interprets electronic signals from throughout the building, discerns the presence of fire and then performs an amazing series of tasks, including calling the city and fire authorities, describing the location of the building and nature of the emergency, rerouting air flow, and recalling elevators to the ground floor.

The panel itself sports a keyboard and LCD for manual operations. Still, given the possible combinations of conditions which could arise and the number of potential response actions, the testing effort for this system was daunting. Although manual testing could be performed via the panel for portions of the system, the electronic signals which are monitored and the automated responses can't be tested in this way.

To ensure the quality and reliability of the system over the large volume of potential conditions and responses, Simplex developed both customized hardware and software tools which were installed in a PC in combination with off-the-shelf cards. This system was then controlled by a scripting language to create and evaluate the various events.

First, Simplex designed a card which received data from the system and converted it to RS-232 protocol for transmission over a serial communications link to a PC. Running on the PC was a software shell specifically developed to receive, decode and display the data. This enabled the PC to evaluate the responses of the system.

A low-cost digital I/O board in the PC was used to cause the specific stimuli which were needed to create the test events. The board converted TTL output to the electronic signals which would simulate the actual conditions on the system and transmitted them to the panel, letting the same PC cause the events and evaluate the responses.

With this step completed, a test script library was developed to automatically apply and evaluate test cases from the PC. Test conditions were created by parsing and transmitting command sequences entered at the keyboard into the electronic stimulus needed to simulate a particular condition, then reviewing and evaluating the response as it was received over the communications port. According to Simplex's software quality assurance engineer, David Despres, "Our automated test bed has substantially improved our test coverage with less time and fewer resources."

Testing postage scale systems
Many electronic devices depend on human input. Applications ranging from appliance controls to automated tellers use embedded software applications to interact with a human being. In theory, these systems should be manually testable, but in practice, the potential combinations often exceed human endurance and capacity for consistency.

A leading vendor of postage scales and meters faced exactly such a problem. While office personnel across the nation use this equipment everyday without undue difficulty, actually recreating and verifying the complex matrix of rate schedules as applied to varying weights and zones presented a testing problem which surpassed the resources available for manual testing.

The scale system offered a standard RS-232 port through which the embedded software was loaded. This interface also provided a test port which could receive command sequences from a PC front end via an asynchronous communications link. Sequences were translated into events on the meter, such as weighing a package and selecting the class of service. The meter's response, which was the postage calculation, could be returned over the same interface.

The final layer was an automated scripting language which operated the front end, permitting test cases to be applied in an unattended mode. The test cases consisted of both the inputs (package weight, postal zone, class of service) as well as the expected output (the amount of postage due). Discrepancies and test results were automatically logged for later review and analysis.

The result was an automated software-testing system which could be connected to one or one hundred postage meters over standard communications lines, and which was capable of exercising thousands of test cases, 24 hours a day, seven days a week, in a consistent and repeatable manner. Following new loads of the embedded software or changes to the devices themselves, these test cases could be repeated automatically at a marginal cost in time and resources.

Naturally, the equipment itself was still subjected to literal hands-on testing to verify its mechanical integrity and reliability, but the complex underlying calculations in the embedded software system could be easily and accurately verified in an unattended mode.
is more than made up during the middle or later stages of testing." According to Microsoft product manager Audrey Watson, "If you're doing what you're supposed to be doing and building the test cases as you develop the product, you're more likely to use TestBasic."

Microsoft advises organizing test scripts into a hierarchical set of scenarios, cases and suites. A scenario tests one instance of a given feature, while a case is a collection of scenarios testing different aspects of that feature. A suite is a grouping of test cases around an application's general function, such as all items in the file menu. If features of the code are changed, you then know which scenarios or cases you need to go in and change as well. But the entire test hierarchy should then be run against the new code to see if the changes introduce any errors elsewhere in the application.

Making test programming easier

Everyone knows that a disciplined method of test development should go hand in hand with a disciplined process of application development. Test requirements should match those derived for the application in the front-end requirements analysis. There should be a link to the CASE tools used by the development team. But of course, that's seldom the way it works in the real world. The Software Engineering Institute (SEI) of Carnegie-Mellon University (Cambridge, MA) estimates that about 85 percent of today's software development organizations are operating at the 'chaotic' level, which is the lowest of five grades for the methodical and orderly development of software.

It's not surprising, then, that people want ways to make the creation of test scripts easier for existing code—and for working in an organization where all the disciplines of a CASE environment aren't in place. The Mercury TestRunner system, for example, does more than just capture user input while recording. It records user activity directly into a C-like language. That makes it much easier to figure out what's going on than is the case when dealing with a raw recording of keystrokes and mouse coordinates, and it facilitates adding automation elements such as loops and data tables.

Multimedia capability

In the Tiburon Ferret system, in addition to tools that aid in test script programming, bug report generation and deriving tests from requirements, there has been added a multimedia capability. "Despite the fact that we've put these tools in, if no one writes requirements down, who's going to do it?" asks Tiburon's Pope. For existing code or code created without systematic written documentation, Ferret offers the ability to interview the inventor on videotape and play back the interview in a window. According to Pope, "I can go find the guru who invented something and say, 'Can you tell me how this works?' and he probably will. If I say, 'Write it down,' he'll probably say, 'I'm busy.'"

Ferret also includes a handheld scanner for inputting handwritten notes, such as the results of a conversation over drinks that only exist on a cocktail napkin. Tiburon is now working on a Hypercard-like method of indexing such stored multimedia information to relevant parts of the project. "When you want to design a test, call up the interview and find out what the thing is supposed to do," says Pope.

Automating test generation for existing code is also a big part of what AutoTester does. In its character-based version, AutoTester can automatically analyze a program's screens and create templates. In addition, the test engineer can write scripts that don't contain the actual data used in exercising the code. The test data, inputs and expected results can then be kept in separate files. In testing, the input data elements are applied to a given script or screen template and the output of that screen is compared with the expected results.

According to AutoTester's Brown, automating template generation and keeping test data in separate files has several advantages. For one thing, it makes test suites easier to maintain. When a function changes, you generally know which screen is affected and can go in and change that template. "Just as you wouldn't hard-code data for your programs, we don't hard-code data for our test cases," Brown says. This lets the test engineer spend more time on creating test data that will really exercise the system and, since

---

This sample of a FastTest script from MS-Test exercises the calculator application and compares the result with an expected result stored in the Windows clipboard.

```
**************************************************
****This script tests the capability of the Windows
****Calculator to send data to the clipboard correctly.
****Lines preceded by asterisks are comment lines.
****Commands beginning with an "X" are FastTest
****function names. The "F4" command closes the
****Calculator window.

*XInclude 'FTEST.INC'

****Set log options and start the Calculator:
XLogOn
XLogBanner "Starting Clipboard Test"
Viewport Clear
XStartApp "C:\WINDOWS\CALC.EXE";;

****Perform a subtraction:
XType "888"
XType "."
XType "333"
XType "-"
XStartApp "C:\WINDOWS\CALC.EXE";;

****Verify that the expected result of the
****(555) is the same as the value currently held in the
****Clipboard:
XClipboardCmp "555"
XAlt ["F4"]

END
```

This sample of a FastTest script from MS-Test exercises the calculator application and compares the result with an expected result stored in the Windows clipboard.
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tests are generated from the program’s own screens, less time on defining the templates and scenarios themselves.

Careful planning still needed

For all automated aids, however, the admonition to plan carefully and design systematically is still a wise one. As one user, Keith Davis, director of QA applications at Borland International (Scotts Valley, CA), puts it, “Automation is a separate component to the test process, and you need to really plan for it. You have to really think about what the process is and how it fits into your system.” One of the payoffs of automatic testing, says Davis, is that you can run tests unattended and get feedback on the product while devoting creative human resources to things other than running manual tests.

As a vendor of one of the more expensive test systems, Tiburon’s Pope comments about the cost of testing: “There are three costs associated with buying a test tool. The initial investment is the most obvious cost. The second is what it takes to set it up, learn to use it and use it the first time. The third cost is how much it costs to use the tool every other time you use it. You can buy a $400 tool that costs you $100,000 to use for a year.”

Against the costs, you’ve got to weigh the benefits of shipping quality software. “You can’t put a price on it,” says Borland’s Davis, “even if it cost $250,000 to do the installation. If we ship a product with bugs in it, we become an acquired company.”

Tiburon’s Pope points out that SEI estimates the costs of bugs that get out into the field to be between $4,000 and $16,000 per bug when you figure 800-line support, finding bugs as customer goodwill and the expenses as overhead. “You need more than a test-execution tool to get this job done, or all that will happen is you’ll be doing the same things faster but no better.”

SQA Robot is designed to work within an environment provided by another SQA tool, SQA Manager. SQA Manager includes a database and project-management utilities so that various people working on a project can look at the data involved in specifying requirements, designing and executing tests and comparing the results of tests with the original requirements. It’s also able to accommodate MS-Test through the hooks built into SQA Robot.

For those more sophisticated developers using CASE tools, Snow notes that the use of dataflow diagrams allows a better functional understanding of the code to be tested. Still, “it’s possible to check function points and still leave a very large part of the code untested,” Snow says. So other tools such as profilers and coverage-analysis tools are needed to provide a level of confidence that the tests that have been designed really exercise a known portion of the code.

The industry average is that most code goes out with at best 50 percent coverage,” says Richard Conley, vice-president of software management products for Veritas (Santa Clara, CA), which makes code-coverage analysis and simulation tools for the Unix environment. “We once found 90 test cases that seemed to be really doing something turned out to be hitting only one particular branch and [provided] only 10 percent coverage,” says Conley. “So the organization thought it was doing something but had no good insight into how much of the code was being exercised.”

Veritas’ VistaTest system incorporates the ability to analyze code and predict how much effort will be involved in testing it; it also performs coverage analysis. VistaTest can then flag portions of the code that haven’t been touched by the current suite of tests, so that the test engineer can use that information as feedback to design tests for more complete coverage. “But,” warns Conley, “just having 90 percent coverage doesn’t mean that the code is 90 percent perfect.”

Not all code, such as calls to the operating system, is easily accessible from the user interface—in the sense that a user can say, “If I click this menu item, I will cause that OS call.” The VistaSim simulator is able to go in and place error conditions into less accessible places, such as the interfaces between application OS calls and the kernel, so the tester can examine how the code reacts. VistaSim also uses random error seeding as a gauge of the thoroughness of testing.

In random error seeding, the simulator seeds the code with known errors and keeps track of their locations. The test engineer can then run his test suite and determine how many of the seeded errors are detected. This can in turn serve as a gauge for how effective the overall test suite is. Even if the developer decides that it’s not cost effective to test 100 percent of his code, he or she needs tools that can give a confidence level.

Confidence in the quality of testing comes from three things: the fact that you’re not turning up bugs; your knowledge of how much of the code you’ve covered; and the ability to predict how many bugs might be left, derived from error-seeding analysis. It would be ideal to know that you’ve covered every part of the code and found every bug. Lacking that, it’s at least helpful to know where you haven’t been.
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<table>
<thead>
<tr>
<th>Part Number</th>
<th>Cache Hit Access/Cycle</th>
<th>Cache Miss Access/Cycle</th>
<th>Direct Array Access/Cycle</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5M44009TP-10</td>
<td>10ns/10ns</td>
<td>70ns/280ns*</td>
<td>70ns/140ns</td>
<td>TSOP**</td>
</tr>
<tr>
<td>M5M44009TP-15</td>
<td>15ns/15ns</td>
<td>75ns/300ns*</td>
<td>75ns/150ns</td>
<td>TSOP**</td>
</tr>
<tr>
<td>M5M44009TP-20</td>
<td>20ns/20ns</td>
<td>80ns/320ns*</td>
<td>80ns/160ns</td>
<td>TSOP**</td>
</tr>
</tbody>
</table>

*Cache hit cycles can resume after one miss access time, while the copy-back completes in the background.

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Separating hype from reality in benchmarking

Benchmarking simulators is a tough job that tests users and vendors alike. But with adequate cooperation between the two camps, meaningful results can be achieved.

Mike Donlin, Senior Editor

Anyone who’s participated in a simulation benchmark knows that it’s a lot like test-driving a car, except that you’re learning to drive while you’re evaluating the product. Though the term benchmark conjures up a suite of tests that will ensure the simulator you purchase is the right one for your designs, a closer look reveals that finding the best simulator is a task fraught with difficulties.

Are your designs mostly digital? Are they mostly analog? Are you pushing silicon or circuit-board technology so that timing becomes critical? Do you have modeling expertise? The list is practically endless and the resulting confusion over just what makes a good benchmark has frustrated the EDA community, both vendors and users, for years.

The stakes are high, too. Not only are simulators costly, but the very nature of analog simulation requires you to bank on its ability to make accurate predictions of your design’s behavior. You’ll be depending on it to help you debug your circuit. And you’ll spend a staggering amount of money and time on model development to drive the simulator. A wrong decision can ruin a company’s reputation, and making the right decision can still eat up dozens of man-hours of evaluation time.

“Generally, vendors don’t like benchmarking,” says Hal Alles, corporate architect at Mentor Graphics (Wilsonville, OR), “because it’s like buying a lottery ticket—a lot is left to chance. If vendors do get involved, and we all do, it’s best to take control of the situation as soon as possible. And that should serve as a caution to the user community. Right off the bat, every simulator has built-in limitations—that is, every simulator makes certain assumptions about how the real world is going to behave. If customers aren’t really involved in the benchmark, if they don’t understand these assumptions, they might end up with a simulator that isn’t right for their designs. It’s easy for any vendor to tune a benchmark to make his simulator look good. That’s why it’s foolish to let any one vendor run the show.”

Though it would seem only logical for customers to get involved in a benchmarking operation, the task is so daunting and time-consuming that many users might be tempted to take the easy way out and just send some
**BENCHMARKING**

representative circuits out for evaluation by the simulation vendors. This can be a costly mistake. First of all, as Alles points out, almost any savvy vendor can fudge benchmark results in his or her favor. Second, an uninvolved customer will be stuck with a simulator that he or she knows little about after the benchmarking is over. Even seasoned designers find the benchmarking process frustrating, mainly because the time spent evaluating competing products isn't necessarily time spent producing a design.

“We once performed benchmarks for a whole summer and never got any real satisfaction,” says Terry Coston, director of design systems at Harris Semiconductor (Melbourne, FL). “We ended up putting together a simulator with Verilog and Spice and it's doing the job, but arriving at that solution wasn't easy. The most important thing is to get the simulator in-house and do it yourself. Remember, no vendor has ever lost a benchmark.”

*Should vendors run the show?*

For obvious reasons, it would seem that vendors would want to run the benchmarking show, but this isn't always the case. Customer involvement will pay off after the purchasing decision is made, vendors contend, because the customer will have chosen a simulator that actually works with his or her designs. Vendors know that a sale made under false pretenses will only come back to haunt them.

“Just throwing a schematic at a vendor without a clear description of the conditions in which it's going to operate is a mistake,” says Kevin Jorgensen, product marketing manager at Viewlogic Systems (Marlborough, MA). “It's in everyone’s best interest to really look at what the customer is doing. That means working with the customer and coming up with a real engineering application after the benchmark is done. This gives the engineer doing the evaluations something he can show to his peers that will be used to develop a real circuit. Customer participation is crucial.”

Many vendors also agree that customers should know whether the circuits they're benchmarking have problems. They might use older circuits that had bugs, or they might bring in circuits that are under development with unknown bugs. In either case, the resulting benchmarks can show real results because the simulator will prove its mettle by debugging actual design flaws.

“If I were the customer, I'd write my own benchmarks,” says Paul Wang, vice-president of the CAE division at Contec Microelectronics (San Jose, CA). “It's a tough but worthwhile job. Surprisingly enough, many customers come to us with a circuit to simulate and don’t know what the results should be. It’s far better to design and measure a representative circuit and see which vendors can simulate it accurately.”

*Easier said than done*

The problem lies in designing a circuit that will be global enough to ensure simulation success in future designs, while being specific enough to ensure an even playing field among the competing simulators. Even simulation benchmarks sponsored by unbiased third parties can breed confusion, as was demonstrated by the IEEE-sponsored Bipolar Circuit and Technology Meeting (BCTM) held in Minneapolis in September of 1990.

Each of the participants in the BCTM was given a design specification for a fictitious 12-bit successive approximation register (SAR) analog-to-digital converter. Process models for the converter were provided by the BCTM. The object of the benchmark was to simulate the entire converter through a complete conversion cycle (13 clock cycles) and report on maximum conversion time, time required for simulation and limiting factors of the design.

The converter was an excellent device for testing mixed-signal simulators because the circuit relied on both analog-to-analog and analog-to-digital feedback. Because many of the commercially available mixed-signal simulators either don’t handle mixed-signal feedback or are hard to use with feedback loops, the circuit promised to be a challenge for the participating EDA vendors. The good news from the competition was that most of the vendors were successful in simulating the circuit. The bad news was that there was no clear winner, as each vendor could lay claim to some performance advantage over the others. Why the confusion?

“The BCTM benchmark had some undefined parameters,” says Viewlogic’s Jorgensen. “Though the circuit was well defined, we didn’t have a clear idea of the conditions that it would operate under. There was no set clock rate, for instance, and that caused some problems. After all, no circuit operates in a vacuum.”

Both vendors and users alike, therefore, must define how a circuit is going to be used in a design, or a benchmark can produce ambiguous results. “In the BCTM example, it
would have been very important to know what we were trying to accomplish," says Shawn Hailey, president of Meta-Software (Campbell, CA). "If the purpose of the overall design was speed, then it might be necessary to push some components to their limits. We found out, for instance, that in that design there were a couple of op amps that were marginally unstable. An abstract simulation wouldn’t have caught that, but if the circuit wasn’t going to be running at speed, it wouldn’t have made a difference."

The upshot of BCTM, then, is that you have to know where you’re headed before you start out, a condition that can’t always be met in a benchmarking scenario. So where do you start? Most vendors agree that the best place is with your product—what are you designing?

Printed circuit board (PCB) designers will need to run their simulation benchmarks differently than IC designers. "PCB or system engineers will probably be using a lot of standard parts in their designs," says Prasad Subramaniam, supervisor in the CAD/CAE product management group at AT&T Bell Laboratories (Murray Hill, NJ). "They may not need to write a lot of models and can depend on commercially available hardware and software models for simulation. In other words, they can assume that the components are good and concentrate on how they use them. Silicon designers, on the other hand, will be using A-D converters, phase-locked loops and op amps, which can be very vendor-specific regarding the fine points of their operating parameters. Good device models become critical to the operation of the circuit. In each case, the simulators are doing different things and therefore need to be benchmarked differently."

Simulation trade-offs
In addition to keeping your ultimate goal in mind, it’s necessary to evaluate performance features that will be crucial to your final choice. Some simulators sacrifice accuracy for speed, a trade-off which seems fatal, but isn’t necessarily a flaw if you’re going to use the simulator continuously during a design process. "You might get away with a fast behavioral simulator if you’re going to use it primarily to search for design errors," says Brian Miller, simulation product manager at Teradyne (Boston, MA). "In a scenario like that you’d be looking for a partial, rather than a full-bore, simulation. A less accurate behavioral evaluation might be alright under those circumstances."

Even in design environments where there’s leeway in the accuracy department, the speed-vs-accuracy debate rages. Naturally, no simulator is worth anything if it’s not somewhat accurate, but the level of accuracy can be leveraged for speed, a choice that demands that you know how much you can sacrifice and when. Analog circuits are notoriously slow to simulate, but demand a high degree of accuracy or the final design may not work at all. A purely behavioral approach to an analog circuit might produce good results for design verification, but might fall flat for debugging critical circuits.

The problem with behavioral analog simulation is deciding which

![Transistor model benchmark results](image)

Accurate modeling information is of paramount importance in benchmark results. In (A), this model of a transistor was quickly extracted and might be presented as "accurate to 3 percent." But a 3 percent accuracy in current tells you very little about the accuracy of the conductance $G_{ds}$ (resistance of the transistor) in saturation. (B) takes a derivative fit of $G_{ds}$ and shows that the output impedance is off by a factor of two, in spite of the 3 percent accuracy in $I_{ds}$ (current drain to source). Both models were provided by Meta-Software's Meta-Labs Division.
An interactive method of benchmarking makes the user a participant in the evaluation process, yet still lets the vendor show the simulator's full capabilities. Such benchmarking, for example, was performed by an analog circuit designer who evaluated the Saber simulator from Analogy. The benchmark circuit he chose was a phase-locked loop (PLL) design. Even though his company designs a number of different types of circuits, the PLL was chosen because he was having trouble designing and accurately simulating these types of circuits. He also had substantial lab data to eventually check the accuracy of the simulation results.

The first step was to 'water down' the circuit. This meant simplifying it into a more general configuration. By doing this, the user created a circuit that more accurately represented the design process without disclosing proprietary information.

The diagram of the PLL circuit is shown above right. The topology and component values chosen were not necessarily the best PLL design, but they sufficed for illustrating the simulator's capabilities. (Actually, some of the worst circuit designs often show the most about a simulator's capabilities. If all circuits were perfect, simulators wouldn't be necessary.)

What results do you need?
The second step of this benchmarking process was the most critical. What type of results would give the customer the best information about the circuit? It's important to ask this question without assuming anything about the simulator's capabilities—let the vendor worry about how to get the answer for now. For this circuit, the important measurements were frequency capture time (the time it takes for the PLL to lock into the desired frequency) and frequency jitter (the amount of variation the PLL will have once it's in lock).

But this still wasn't all the user wanted. He needed to know what values to choose for the PLL's low-pass filter frequency poles and amplifier gain to get the lowest capture time and frequency jitter. These circuit parameters are nearly impossible to calculate by hand if there are nonlinear devices in the circuit. In this circuit, the frequency-vs.-voltage function of the VCO was nonlinear.

Now, the vendor began actively participating in the benchmarking process. With the vendor's knowledge of the simulator and a clear definition of the ultimate goal, a procedure was devised that would show how well the simulator could perform the desired task. To accomplish the particular tasks of the PLL benchmark, a four-step procedure was incorporated by the Analogy application engineer.

The benchmark begins
First, the engineer determined that two devices weren't available with the simulator's standard library—the phase detector and the VCO. Both were created with Saber's Mast modeling language. The VCO was particularly interesting because the frequency-vs.-voltage function was determined by a set of value.
fast simulation times were a must. To enable parameters to be varied, fast simulation times were a must. Single simulations with Spice took over three hours. By using mixed-mode simulation and some behavioral models for selected devices, that simulation time was cut to under two minutes.

To measure the capture time and frequency jitter, special measurement models were created with Mast. These models automatically measured these two parameters and displayed their values during the simulations. These models were eventually added to one of the standard Saber model libraries.

The last operation was a parameter sweep. This function let the user automatically sweep any of the circuit parameters while performing multiple simulations. The final results are the curves shown at left. The X-axis of the graph represents the resistance of the feedback resistor in the amplifier section. The Y-axis represents both the capture time and frequency jitter of the PLL. Here now was a single, concise graph that showed the engineer the nonlinear performance of the PLL. The engineer could easily determine the trade-offs in circuit performance with this information. In addition, the Analog Application engineer showed how statistical Monte Carlo analysis could be used for further analysis of the circuit.

The final step of the benchmark was to have the user take over the simulation of the circuit. He then modified the simulated circuit himself to the exact structure of the real circuit. By having the vendor perform the original simulation, the user skipped the beginning of the learning curve and could get hands-on experience using the simulator with a circuit he was familiar with. Comparisons between the final simulation results and lab measurements showed excellent correlation. The results of the benchmark showed the simulator's full capabilities to solve problems that were relevant to the user's particular needs.

behavior you're going to simulate,” says Meta-Software’s Hailey. “I've seen perfectly fine behavioral models that gave a good rendition of voltages but had nothing in the current domain. They were awful when it came to things like system-level ground bounce. The behavioral concept was all right for portions of the simulation, but the unspecified behavior of the circuit could have been disastrous for the final design.”

To get around these hazards, vendors advise their customers to partition their designs into critical paths for detailed simulation and less critical paths for behavioral analysis. But in mixed-signal designs, circuit partitioning isn’t as simple as it seems. Obviously, some components are purely digital and some are purely analog, but there are some hazy areas, such as the analog effects in digital circuits, where you must make partitioning decisions. As always, there are trade-offs involved.

In general, an analog model of a circuit will be more accurate than a digital one because the digital model is an approximation of a circuit's behavior. When the approximation is good, there's at least a factor of 10 difference in simulation speed, because a digital simulation is following an event cue whereas an analog program is integrating a set of coupled, nonlinear differential equations.

There are other advantages to the digital approach if the approximation is accurate. Digital simulation can apply worst-case timing analysis and fault simulation to portions of the circuit—a capability that's lacking in analog simulation. In addition, digital simulations can use hardware models, a capability that's particularly useful when there are complex devices such as microprocessors in your design.

When all is said and done, however, a lot of the decisions about partitioning a circuit come down to the expertise of the designer. The critical thing to remember when benchmarking an analog simulator is that you are working with models, not real devices. Understanding this limitation is critical when you're evaluating a simulator. You must understand the trade-offs when using a Spice model, a hardware model or a behavioral model. You can use a transistor as either a linear device or a switch, but you have to know the consequences of your decision.

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I Divide and conquer

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I Speed traps

All of these trade-offs are, of course, in the interest of speed. Unfortunately, speed is an area where vendors can play games with simulation results, so the buyer has to beware. "We believe that the best measure of a simulator's speed is events per second," says Michael Massa, president of Evaluations Per Second (Waltham, MA), "where an event happens when the output of a gate changes. Some vendors use evaluations per second, which measures inputs to a gate. In an event-driven simulator, the only real activity is when an output changes, not an input. Evaluating inputs can give high numbers to a simulator's benchmark figures, but doesn't really reflect what's going on in a circuit. Besides it's overkill."

Massa also cautions against arcane methods of evaluating a simulator using a 'gates per second' figure. "Older simulators looked at all the gates on every time tick," he says. "That produces an even higher number of evaluations with even more time wasted."

Even when you know the definition of the speed terms applied in a benchmark report, there are still subtle ways that the numbers can be presented. Timing information can be incorporated into the equation in such a way as to give skewed results. "My definition of events per second is to look at a bunch of two-input gates that have all the inputs wired together going to a clock that doesn't overlap the propagation delay through a device," says Rich Goesch, engineer at OrCad (Hillsboro, OR). "Let's say you have a device with a 5-ns propagation delay. You use a clock that exceeds 5 ns on the low and high pulse and you use that to evaluate events per second. I've seen benchmarks from an accelerator company that boasted 100,000 events per second, and all I got with their product was 50,000. They used an inverter and matched the propagation delay to the clock input and effectively doubled their performance. You have to be careful of the games vendors play."

I Easy does it

In addition to the speed/accuracy claims and counterclaims of vendors, there can also be gamesmanship in ease-of-use features. While
these features are important, they really aren't at the heart of what a simulator does. In other words, a colorful, multiwindowed environment is useless if you don't get accurate results. The user community has made it clear that it doesn't want to make confusing transitions as it moves around its design environments, and vendors have responded with easier-to-use graphical user interfaces. But caution is advised when putting too much emphasis on look and feel. “Don't get carried away with the niceties,” warns Marsha Huff, applications engineer at Racal-Redac (Mahwah, NJ). “If customers limit themselves to demos and marketing hype, they might end up dazzled with a lot of smoke and mirrors and end up with a simulator that doesn't fit their needs. A good user interface is important, but not nearly as important as knowing what the simulator's doing.”

A less obvious side of the ease-of-use portion of a benchmark is ease of integration. This benefit might not be as easy to quantify in a benchmarking scenario where evaluations per second and successful convergence are the buzzwords. But a simulator doesn't run in a vacuum—you must be able to backannotate results into the front end of the design or iterations can become tedious, time-consuming affairs.

“We've seen our share of simulators that were fine performers but which no one used because they were impossible to integrate,” says George Edgar, applications engineer at Jet Propulsion Laboratories (Pasadena, CA). “If you have to pop up all kinds of schematics and input probes, it’s easy to get lost. We had one large vendor in here, whose name I won’t mention, who gave a good demo but whose product simulator that can't help you debug your design isn't very useful.”

The effort of the CAD Framework Initiative (CFI) are going a long way toward resolving these inconsistencies, but until standards are hammered out users must be wary of simulators that won't cooperate with the rest of a design environment.

“You should always be aware of the global engineering task,” says Dundar Dumlugol, director of simulation modeling at Cadence Design Systems (San Jose, CA). “You have to look not just at the time spent in simulation, but at the time spent in the entire design process. This means a simulator must have features that let you analyze the data that the simulator has produced. You have to look at netlisting, how easy it is to access your results, waveform-analysis tools, and post-processing functions in general. A

**Service is key**

All of these ease-of-use features indirectly point to one thing—vendor support after the sale. Unfortunately, this feature isn't obvious at benchmarking time. “We've been burned by vendors who became invisible after the sale,” says Larry Hamilton, supervisor of test engineering at E-Systems (Dallas, TX), a defense contractor that makes computer systems. “When you're in the middle of a design problem, the last thing you need is the runaround from the vendor. If it takes several days to get a return call from the support people, you're in trouble.”

With all of the perils in benchmarking simulators, it's no wonder that users and vendors alike are put off by the task. A vendor that wins a benchmark under false pretenses is saddled with an unhappy customer and a potential for a bad reputation. A user that chooses the wrong simulator will face years of frustration or possible unemployment. But with all of its pitfalls, benchmarking is still the only way to find out if a simulator will fill the bill. The best weapon, then, is being informed.

“An uninvolved customer is deadly,” says Teradyne's Miller. “If you're a designer with a problem, you have to rely on your simulator to help you solve it. Now maybe that simulator will help you debug 90 percent of your circuit. Is that unknown 10 percent going to be irrelevant or is it going to shut down the fab? If you don't know the answer to that, you're asking for trouble.”

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CIRCLE NO. 44
High-performance networks challenge Ethernet

A half-dozen high-performance network interfaces—including three proposed standards—dominate the industry. Though each has advantages in its particular area, price/performance will undoubtedly push the market toward a single approach.

Warren Andrews, Senior Editor

Ethernet, the de facto computer industry network standard, is more than 10 years old and is starting to show its age. Though it enjoys by far the largest installed base of any approach, its maximum transfer rate of 10 Mb/s—and real-world transfer rate of only about 2 to 3 Mb/s—is far from satisfying current, not to mention future, needs. It's now many generations behind the succession of CISC and RISC processors that call for communications with a greater transmission bandwidth. That Ethernet has survived as long as it has is more a testimony to the vacuum in networking technology than it is to the inherent vitality of the standard.

But that vacuum is about to be filled with new approaches, most of which have promised to bring communications bandwidths to the Gbit/s range and beyond. These include FDDI (Fiber Distributed Data Interface), Fiber Channel and ATM (Asynchronous Transmission Mode) among the proposed standard approaches offered, as well as a small number of other, specialized, semiproprietary approaches—ScramNet from Systran Corporation (Dayton, OH), Universal Memory Network from Computer Sciences Corporation (Lompoc, CA), MCP from Ironics Corporation (Ithaca, NY), HiPPI from Research Network, and a whole host of other proprietary approaches.
I NETWORK INTERFACES

What will determine both high volume and flexibility, but some companies achieving cations eventually—

and this is true whether it’s the best solution technologically or not. What will determine this winner isn’t going to be raw bandwidth or flexibility, but some combination of features with the key element being price/performance. And, of course, what will drive price/performance won’t be just the design approach and manufacturing technology; it will be sales volume.

Leading the way, therefore, will be those companies achieving both high volume and high performance—most notably, workstation manufacturers. The volume leaders at this point, Sun Microsystems (Mountain View, CA), IBM (Armonk, NY), Digital Equipment Corporation (Maynard, MA), and Hewlett-Packard (Palo Alto, CA), are all straddling the fence with regard to network interfaces.

Playing catchup

“We’re hitting a bandwidth crisis now, driven by both increasing Mips and increasing I/O requirements,” says Fred Sammartino, manager of high-speed networking and advanced development at Sun. “Processor performance has been doubling about every two years. And like anything experiencing that kind of exponential growth, it appears to start out slow then turns a corner and goes through the ceiling. We’ve been living in a period of blissful ignorance where we’ve lived with 10 Mbits/second Ethernet.”

Sammartino explains that Ethernet has been helped along by partitioning systems into smaller seg-ments, which in turn are boosted by high-performance routers and concentrators, but “all of a sudden,” he adds, “you just run out of bandwidth. And because of the exponential growth of processor performance—and therefore network bandwidth requirements—once you run out of bandwidth, you’re suddenly on a downward spiral which is very hard to get out of.”

I Which way to go?

FDDI, as currently defined, only carries transfer rates to 100 Mbits/s, or about 12.5 Mbytes/s. But FDDI has a leg up because there are already a handful of chip sets on the market that support it, and a number of networks currently use it. Also, discussions are underway to scale FDDI up an order of magnitude—to a Gbit/s.

Alternatives to FDDI are few at present, and as yet none has been designated as a standard. The ATM approach is still undergoing solidification as a standard; it’s expected it will be at least a year before things are settled out enough to start manufacturing chips and boards. For Fiber Channel there are other considerations.

“Fiber Channel isn’t really a network interface at all,” says Steve Sibley, IBM’s manager for the IBM/HP Fiber Channel alliance (Rochester, MN). “It’s primarily designed to attach systems with a point-to-point link in a channel-type environment, and to map existing interfaces such as HIPPI and SCSI into a single standard.” Although Fiber Channel was designed as a peripheral interface, some companies are already looking at manufacturing high-performance Fiber Channel switches, and others want to incorporate standard networking protocols into it, such as TCP/IP (Transmission Control Protocol/Internet Protocol) and OSI (Open Systems Interconnect). In addition, a study group is considering putting an ATM structure on Fiber Channel.

ATM is also undergoing specification, and a standards group is hard at work hammering out final details. In addition, there already exists an ATM chip consortium trying to design a chip set to implement the standard. The word from these groups is that the first practical ATM implementation won’t take place until

I Irons vice-president of engineering Tom Rich stands next to his company’s very high-speed data blaster as it transfers data from one computer to another. “Unlike traditional network and even reflective memory approaches,” Rich says, “the Irons approach looks almost like a DMA transfer, letting the receiving processor have immediate access to the data without having to find it in the address space.”
well into 1993 or early 1994, and it will perhaps be 1995 before volume implementations arrive.

No need to wait

"FDDI is here now," says Joel Silverman, product manager for VME board maker Radstone Technology (Montvale, NJ), "and it satisfies customers' needs. There's little question that faster, more elaborate and even scalable interfaces are required, but people aren't going to wait until 1993, 1994 or beyond." Silverman adds that even though FDDI has been around for several years, it's only been in the last year or so that companies have been able to develop subsystems that make it practical.

"One of the keys to providing a practical FDDI interface," says Silverman, "has been to put as much of the network protocol intelligence onto a separate intelligent subsystem, to offload the protocol management from the host. Even a powerful host processor such as a Motorola 68030 or '040 can be brought to its knees if it gets involved doing protocol processing along with its other tasks."

But even with the benefits of an intelligent subsystem, FDDI has yet to live up to its rated performance. Few FDDI systems, if any, operate near the maximum bandwidth of 12.5 Mbytes/s (100 Mbits/s), and many systems achieve little better than 2- to 3-Mbyte/s rates. Even these rates, however, offer a major improvement over existing Ethernet connections.

FDDI is increasingly being used as a network backbone, rather than a desktop interface, primarily because of cost. Though there are now a handful of different FDDI chip sets, they're far from the point on the cost/volume curve where they make an inexpensive desktop interface. Furthermore, FDDI is currently defined as a fiberoptic interface, and it requires costly LED lasers and photodiode/phototransistor receivers, in addition to special connectors and splicing. Adding to the problems is the fact that most existing buildings are wired with the FDDI PMD sublayer, thanks to its use of combined data link transceivers and integrated FDDI media interface connectors. It also employs the new SparcLite embedded processor.

Sammartino explains that, although FDDI transfers information at 100 Mbits/s, the line rate (baud) is about 125. "In comparison," he adds, "the line rate for ATM is 155, and, though somewhat higher than FDDI's 125, is close enough to allow the two to share the same technology. The technology exists today to run those signals over existing twisted-pair copper wire and stay within tolerable bit error and EMI."

Sammartino feels strongly that the availability of copper interfaces will be a compelling force in the implementation of next-generation networking technology. "Fiberoptic interfaces," he says, "will be too expensive for a real desktop LAN solution for quite some time." He explains that he's seen quotes of more than $50 per interface going out to the 1995 time frame. He believes this will make the price of a fiberoptic inter-

Radstone Technology's FDDI-1 advanced architecture controller board for VMEbus, introduced this spring, is billed as the first 6U VME board to provide dual FDDI nodes in a single VME slot. Radstone claims the board is in full compliance with the FDDI PMD sublayer, thanks to its use of combined data link transceivers and integrated FDDI media interface connectors. It also employs the new SparcLite embedded processor.
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**Moving with Fiber Channel**

Fiber Channel has already been four years in the definition, “but we hope,” says IBM's Sibley, “that the definition will be completed by next year, with the emergence of products early next year.” It doesn’t look as if many will wait for the finalization of the specification to start developing products, however. IBM and Hewlett-Packard have already developed and are marketing an OEM Fiber Channel board.

Robert Nunn, marketing director at Vitesse Semiconductor (Camarillo, CA), reports that his company, working with two partners (Interphase and Seagate), will soon announce a major Fiber Channel effort, including the definition of a Vitesse-developed GaAs chipset. Nunn, like Sibley, doesn’t compare Fiber Channel to a telecom approach such as Sonet (Synchronous Optical Network), but does rule out using its definition as a high-performance network interconnection scheme.

Douglas Felder, vice-president at Chi Systems (Pleasanton, CA), takes the same view. While Chi is currently working on HiPPI-based interfaces, Felder believes this will be a subset of Fiber Channel as soon as the technology reaches the level that chip sets are available. He says that Chi is presently working on interfacing Sun, Silicon Graphics and other workstation platforms, as well as high-performance storage systems, into what he calls a “HiPPI network.”

**Going HiPPI**

The prototype of this network, according to Felder, is being developed at Lawrence Livermore Laborato-

ries (Livermore, CA), with a number of companies participating. The consortium of companies, known as National Storage Labs, includes IBM Federal Systems, IBM Storage Systems and Network Systems, in addition to a number of workstation makers. The companies are providing materials and expertise to tie together a high-performance network test bed. The software tying the network together is being developed by General Atomics' Unitree division.

IBM and Hewlett-Packard have gotten together to develop a family of OEM Fiber Channel products designed to serve everything from desktop PCs to high-performance workstations. At the heart of the companies’ approach is IBM's laser technology; IBM's been able to use relatively low-cost lasers such as those found in compact disc players in high-speed networks. Here an IBM researcher examines a Fiber Channel board.

The objective of the consortium is to demonstrate that it's possible to transfer data at HiPPI rates. “Until now,” says Felder, “the only standard that's been available is FDDI, which limits transfer rates to 10 to 12 Mbytes/s. With HiPPI we've been able to demonstrate rates of 100 Mbytes/s.” Existing systems are using conventional parallel HiPPI schemes with copper cables; however, fiber-based HiPPI is already in the wings.

“HiPPI,” says Felder, “is here now, and we have many systems in the field and working. Fiber Channel started out as a relatively simple fiber option to the HiPPI hard-wire, but the option grew as those defining the specification kept adding feature after feature. It got to the point where it is now well defined, and a viable option, but it's still at least two years away.”

Fiber Channel, according to Sibley, has also been defined to include different rates, from the lowest of 133 Mbits/s, doubling through 266, 531 and on up to 1.062 Gbits/s, the fastest rate currently specified. “The decision to layer Fiber Channel into the four segments,” Sibley adds, “lets users looking at different implementations adapt the standard to their specific needs.” Those using SCSI, for example, may not need the higher data rate, and will not be forced into a more expensive solution than they need. If HiPPI has to be accommodated, the faster transfer speed will be needed.

In addition, different rates let different technologies provide the most efficient operation, given some combination of data rates and distance. The Fiber Channel standard makes provision for lower-speed copper interconnection, as well as for multi- and single-mode fiber. The ideal solution is some “mix-and-match” combination of speed, medium and distance to provide the most economical result.

And it looks as if Fiber Channel is becoming very affordable. Prices for fiberoptic transducers have come down significantly, says Sibley, thanks to IBM's pioneering use of the same laser technology developed for commercial compact disc players in fiberoptic transducers. This has lowered the cost of a node from close to $1,000 to only a few hundred dollars. “And costs will continue to drop as volume picks up,” says Sibley.

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CIRCLE NO. 47
measures 1.5 x 4.5 in., and provides a full "byte-to-light" interface at transmission rates of 266 Mbits/s. It includes the optical link, encoder, clock recovery unit, and laser safety circuitry. "We expect these prices to drop to below the $100 mark by mid-decade [1995]," says Sibley. Of course, he adds, the price level will depend on distance and performance parameters. He expects to be offering a faster version of the unit soon, but he wouldn't commit to a firm timetable.

Sibley anticipates that even when the Fiber Channel rate reaches the Gbit/s range, interface circuitry will still be in silicon, as are IBM's existing chips. "We don't see the need for GaAs interface technology for at least the next generation or so," says Sibley. He claims that conventional silicon is more reliable and less expensive.

Sibley adds that IBM is also looking at copper approaches, but has not yet determined if they'd be practical. "We're looking at maintaining a very low bit error rate, in the range of 10^{-12} to 10^{-15}, and presently we don't see being able to maintain that level at the kind of data rates we're looking for."

At the higher transfer rates, factors other than simple interface IC fabrication can be strong considerations. One of these factors is receiver technology. As rates increase, the receiver becomes more difficult to build. "Hewlett-Packard has a lot of expertise in receiver technology, and that's one of the reasons we decided to team up with it in this Fiber Channel project," explains Sibley. Other factors in high-performance Fiber Channel systems are manufacturing technology and overall optical approach.

**Not a network?**

Though Sibley and some others are quite adamant that Fiber Channel isn't a network approach, others such as Felder aren't so sure. Felder even refers to some HiPPI implementations—as well as migrations to Fiber Channel—as networks. Although FDDI doesn't fit into the traditional topology of a network in terms of providing a ring or daisy-chain structure, network characteristics can easily be accommodated through high-speed switches and routers.

Sibley believes that the cost of various communications schemes will come down to a point where both a high-performance peripheral interface (such as Fiber Channel) and a high-performance network can co-exist. Such a system could conceivably implement a Fiber Channel link to a high-performance disk array, and an FDDI or ATM connection to a LAN or WAN.

While this scenario may make some sense theoretically—just as a SCSI channel may coexist with Ethernet—it may not be practical to have a pair of Gbit/s channels going on and off the desktop. Such a system could require two special switches, one to network the disk array, the other to handle local area or global networks. Special bridges might also be required between the network and peripheral interfaces.

On the other hand, the scenario may not be so outrageous when one considers the type of work being done at National Storage Labs, where multiple computers—workstations as well as supercomputers—are tied into large, shared-storage subsystems such as disk arrays. A HiPPI or Fiber Channel interface could handle accesses to the storage facilities, a different network interface would handle interfaces within nodes in a system, and yet a third interface—to either individual machines or network concentrators—might handle the interface to wider area networks.

**Network performance and cost**

There's presently a gap between LAN and WAN performance and affordability. WAN capabilities such as those provided by Sonet are available, but not in a cost-per-node range to make them at all practical. LANs are not growing as rapidly in speed as are WANs, but they'll approach affordability in the near future. The ATM proposal would provide a middle ground to bring telecom-type technology into a reasonably economic range.
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Network Interfaces

"It just makes a lot of sense to me," says Bill Kehret, president of Themis Computer (Pleasanton, CA), "if a single interface could be developed to handle all three situations." While it’s not clear that a single interface can meet all the needs of a high-speed, point-to-point link such as Fiber Channel, as well as provide the flexibility of a WAN or LAN, at least the second two requirements can be satisfied.

Enter ATM

On one hand, those firmly behind FDDI are looking to increase the flexibility of the interface, adding a structure that will make it compatible with telecommunications systems. On the other, the ATM group is working to define a separate subset of the broadband ISDN (Integrated Services Digital Network) specification. "And, if it could also include a subset of the Bellcore-developed Sonet scheme, it would automatically provide a seamless connection between both local and wide area networks," says Sammartino.

Asynchronous Transfer Mode refers to the way packets are formatted and switched through a network, but it doesn’t necessarily specify the physical layer or explain how the information is transmitted on the wire. In broadband ISDN, ATM and Sonet are coupled, but in LANs, they won’t necessarily share the same transmission technology. "But," adds Sammartino emphatically, "I’m a firm believer—and Sun is also—that if a solution could emerge that is a subset of Sonet for the local area, it would greatly simplify the entire issue." The trick, he says, is to find a subset that is fully compatible with, yet inexpensive enough for, a local area network. This will undoubtedly involve the development of a compatible chip set. Today, Sonet costs $1,000 a node, which wouldn’t be a practical desktop solution.

"We’re still in the early definition stages of ATM," says Sammartino, "so there really isn’t any quantity of products available. Though there are a handful of parts available, we consider them generation zero." He believes real ATM devices, including both standard boards such as SBus boards and chips, will be available during 1993. At least one SBus ATM board is reportedly available from Fore Systems (Pittsburgh, PA), which is also readying an ATM switch for the market. Micro Pacific Research (Vancouver, British Columbia) also already offers an ATM switch. And a recent survey showed that several other firms plan to offer ATM hardware during 1993.

"The heart of this approach is the ATM packet specification, which defines 53-byte cells," says Kehret. "The size of the cell is small enough so there is virtually no latency in a packet transmission, yet large enough to allow it to be scaled up to and beyond the Gbit/s range."

The ATM group is looking at the basic Sonet rates for incorporation into both a WAN and a LAN. These rates have thus far been defined as:

- OC-1 51.840 Mbits/s
- OC-3 155.520 Mbits/s
- OC-9 466.560 Mbits/s
- OC-12 622.080 Mbits/s
- OC-24 933.120 Mbits/s
- OC-36 1866.240 Mbits/s
- OC-48 2488.320 Mbits/s

"Some of the first implementations we’ll see," says Kehret, "will be based on the OC-3 and OC-12 rates, to take advantage of existing interface and cabling technology, as well as to be consistent with readily available telecom interfaces." What Kehret envisions is a totally transparent WAN/LAN, such that work...
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stations could plug right into a high-speed network and have a seamless connection to other machines in the same room or building, as well as with any on the same network, anywhere in the world.

The ATM approach has a strong following at Apple, Digital, Sun, and others, though much of the progress to date is kept tightly under wraps. Even the ATM chip consortium is very secretive about emerging developments. But the group has a problem stretching the 125-Mbit/s line rate of FDDI to the 155-Mbit/s rate of ATM OC-12.

**Hedging a bet**

The need for more flexibility, particularly as multimedia becomes a reality, is becoming a major concern for network managers. This problem is being addressed aggressively by the FDDI group, which includes many of the same participant companies as the FDDI, HiPPI and ATM groups.

Second-generation FDDI provides upward compatibility from the first generation, but adds circuit-switched service to FDDI's existing packet-data service. The new service is intended to support isochronous data — data which must be delivered in regular amounts at uniform time intervals. A major advantage of an isochronous LAN is the ease with which it can be connected to WANs, making it attractive for such applications as desktop video conferencing. Isochronous data structure mates well with the cell-based approach of wide-area communications — essentially ATM.

But FDDI-2 uses the same 100-Mbit/s bandwidth as its predecessor, FDDI. The basic service also shares its ring-and-packet service with the isochronous service in the second-generation specification. At present, there's no FDDI transmission-rate hierarchy established, and many considering the approach feel that it may not provide the expandability needed for future generations of processors.

"There is always a bottleneck in network approaches," says Sammartino, "and the only way to solve the problem will be to add bandwidth." He explains that the useful life of a typical Ethernet system has been greatly expanded through clever organization of the network's topology. Using switched networks and hub concentrators, instead of conventional multiuser drop approaches, it's possible to increase the effective bandwidth of standard Ethernet.

This approach in essence gives each user their own bandwidth through a direct connection to a hub rather than sharing the bandwidth with other users on a single line.

"But," Sammartino continues, "the problem is that when these are installed in a real environment, usually something like a client-server environment, the advantage erodes. It frequently happens that while the added per-user bandwidth lets users look essentially at an empty network, the server (or wide-area network or other facility) will be loaded up and unavailable. An escape — a higher-bandwidth connection — is always needed to go to a server or routers or wide area network."

With networks such as FDDI, there will always be a bottleneck of some kind or other. "Because of ATM's scalable approach," concludes Sammartino, "there's always a next step — a faster but seamless interface — to handle the higher-speed server or wide-area network requirements."

**Networks for real time**

The next generation of network interfaces is anything but "conventional," but it can't always handle the needs of some specialized, high-performance, real-time systems. Applications such as large simulators.

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**Fiber Channel structure**

<table>
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<th>Layer</th>
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<td>IPI-3, SCSI, HIPPI, BLOCK MUX, OTHER</td>
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<tr>
<td>FC-3</td>
<td>COMMON SERVICES</td>
<td>266 Mbit/s</td>
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<tr>
<td>FC-2</td>
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<td>531 Mbit/s</td>
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<td>FC-0</td>
<td>PHYSICAL LAYER</td>
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Fiber Channel has been defined with five protocol layers, F0 through F4, the latter being the I/O channel analog to the ISO/OSI network layers. The physical layer (F0) has been defined in four speed ranges, from 133 Mbit/s to 1.062 Gbit/s. Transmission medium technologies appropriate to each, along with maximum transmission distances, are indicated below the physical layer.

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**Network Interfaces**

Where in the world stations could plug right into a high-speed network and have a seamless connection to other machines in the same room or building, as well as with any on the same network, anywhere in the world.

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CIRCLE NO. 48
Proprietary solutions fill gaps left by standard networks

At least one major workstation manufacturer is fond of saying "The network is the computer," but today's users are apt to retort, "Yes, and the network is too slow!" In simple terms, both workstations and open-architecture real-time systems are evolving much faster than the standard network products intended to interconnect them. For example, it's taken our industry about 10 years to progress from Ethernet to FDDI, a change representing about a twelvefold increase in speed. In the same 10-year period, system throughput demands have probably increased by a factor of 40 or more—since bus widths have quadrupled (from 16 to 64 bits) and CPU clock speeds have increased by a factor of 10 or more. The challenge is to provide connectivity solutions which can keep up with the systems they serve.

One response to this problem has been to replace or augment traditional peripheral buses (for example, SCSI), LANs (for instance, Ethernet) and serial-based connections with new, standardized, high-speed networks and network technologies. Some examples of this approach include FDDI, Fiber Channel, SCSI-2, and Sonet. These new networks and media systems offer the expected benefits of standardization, and provide significant performance gains over their predecessors. Even so, once you take into account the operating system overhead needed to manage network protocols, there remains a sizable gap between available network speeds as compared to present system connectivity needs.

Meeting the need for speed

A second response has been to create fast, low-overhead, proprietary data-transfer systems capable of exceptionally high data-transfer rates. Proprietary systems can do a good job of improving system-to-system data-transfer rates, subject to specific design trade-offs. Proprietary systems are differentiated in terms of the size of data transfer for which they are optimized, the data-delivery mechanisms they provide, the transmission media used, network configurations, and protocol structures (if any). Let's examine each of these differentiating factors:

- **Transfer size optimization:** Some systems perform well when transferring small messages, but tend to have lower absolute speeds when performing large transfers. Other systems are tuned to handle large block transfers with very high absolute speeds, but prove less efficient when handling smaller control-oriented messages.
- **Data-delivery mechanisms:** Some transfer systems (especially reflective memory systems) transfer data from the source to "bulletin boards" in the destination chassis. Typically, the data receiver either polls the bulletin board to look for incoming data, or is interrupted by the bulletin board when a message arrives. An advantage of the bulletin board approach is simplicity; in many cases, a simple data write is all that's needed to initiate a transfer. Other transfer systems follow a DMA transfer model, where the transfer initiator writes a small data structure which defines all aspects of the desired transfer. Once started, the transfer pulls a specific amount of data from a specific source, and delivers the data to a specific destination address in one or more remote chassis. An advantage of the DMA transfer approach is specificity and low overhead: once the transfer's described, data is moved to the precise destination address with no further intervention from the participating systems. Some, though not all, systems provide a synchronized broadcast mode which lets you transmit to multiple receivers at once.

- **Transmission media:** Although some wireless/cableless systems are available, most proprietary systems use either wire-based or fiber-based interconnects. Wire systems have the advantages of speed, ease of configuration and low cost, but they also have the limitation of relatively short interconnect runs. Fiber systems offer the advantages of very good speed and distance capabilities, but they come at relatively higher costs.

- **Configurations:** The simplest proprietary systems provide point-to-point system connections. Multisystem configurations include ring, star and linear multidrop topologies.

- **Protocols:** In some systems, data is transferred in a protocol "wrapper," with wrapper size varying from system to system. In evaluating systems using such wrappers, it's important to realize that the wrapper consumes some portion of the available transfer bandwidth. Typically, the fastest systems make every effort to minimize (or eliminate) this un

R. Chris Martens, director of marketing, Ironics, Ithaca, NY

with literally hundreds of different processors call for special communications systems. In response, a number of different approaches have emerged which bypass the traditional network and, in some way or other, let the memory of one computer talk directly to that of another.

This communication can be in the form of a common memory shared by two machines, such as Systran's ScramNet, or it can be a direct memory transfer—essentially a remote DMA—such as Ironics uses in its approach. Both approaches offer different advantages and are usually tailored to specialized applications.

Systran's ScramNet is a replicated, shared-memory network with a 150-Mbit/s data rate. The network communicates over a fiberoptic cable and is designed to update any system's ScramNet memory, from 128 kbytes to two Mbytes in size. "By providing a direct memory-to-memory transfer," says Tom Bohman, Systran's ScramNet product manager, "we're able to transfer information directly, without software protocols. Unlike FDDI or other approaches, ScramNet lets an application program in one computer communicate its data directly to an application in another computer in only a few microseconds. The network is designed for real-time systems where throughput isn't the only factor, but the age of the data is also a critical parameter."

The interface control document for ScramNet is a memory map, says Bohman. Since every computer is
getting a local copy of the physical memory space, software engineers running the application simply need a map to describe where the data is located, where it's coming from and what format it's in.

"ScramNet is really the network alternative to a physical shared memory," continues Bohman. "It has the same data-link and immediate data-sharing characteristics as physical shared memory."

Computer Sciences Corporation’s Universal Memory Network (UMN) takes an approach similar to Systran's. The company claims its technology provides near-simultaneous access by all devices on the network to data designated as common or shared. The reflective memory scheme is almost a subset of Systran's approach, but provides a semaphore capability to let devices exchange control information over the network. UMN operates at a rate of 40 Mbytes/s.

Even when such standard networking protocols as these are eliminated, data still may not get to a critical processing node and be acted on fast enough. "In these applications," says Tom Rich, vice-president of engineering for Ironics, "conventional LANs have to be augmented with a high-speed data-blasting channel."

Rich comments that some approaches have tried to use conventional networking technology but run into problems on two fronts: first, the bandwidth is too low, and second, host-processor intervention would not.

In an ideal world, traditional networks would be reasonably priced, easy to install and to use, and faster than the systems they connect. Until we reach that ideal, however, combinations of traditional data links and fast proprietary networks will provide the best blend of standardization, user-friendliness and high performance—at price points which make sense.

Sonar analysis system

![Diagram of Sonar analysis system]

- DSP/feature extraction module
- User interface module
- Data acquisition/signal conditioning module
- Ethernet
- 30 Mbytes/s multidrop proprietary network
- IEEE-488

Proprietary data-transfer systems can provide real speed advantages compared to traditional networks, especially when they're carefully matched to exact transfer requirements of the systems to be linked. Proprietary systems, however, are not a panacea and should not be regarded as outright replacements for traditional networks. For now, the cost of speed almost always entails a move away from the conventional seven-layer Open Systems Interconnect (OSI) network model.

Subdivide and conquer

Instead of viewing traditional networks and proprietary systems as an "either/or" proposition, one powerful approach is to distribute connectivity loads across both traditional networks and proprietary channels. A good strategy is to use traditional networks as a command and control channel, passing small messages at moderate speeds, while using proprietary systems as independent bulk data channels, blasting large blocks of data between systems at high speeds. In this way, proprietary channels augment, but do not replace, traditional networks, and each channel is used to service the types of transfers for which it is best suited. In typical applications, traditional network links serve as a common resource linking all chassis or nodes in the system, while nonstandard channels are used to link system elements which demand hard real-time data transfers.

The figure shows a block diagram of a sophisticated Sonar analysis system. The installation employs a combination of traditional and proprietary data channels. The system has five main elements: two separate data-acquisition/signal-conditioning modules (one for each main Sonar array), two separate DSP/feature-extraction modules (one serving each associated data-acquisition module) and one user interface module (synthesizing output from each of the two DSP feature-extraction systems).

Each data-acquisition module feeds preconditioned input data to its associated DSP/feature-extraction module via an IEEE-488 link. Both DSP/feature-extraction modules are linked to each other, and to the central user interface module, via two quite different kinds of networks. A conventional Ethernet link lets the user interface module pass command and control signals to either or both DSP/feature-extraction modules, and also lets messages pass between the DSP/feature-extraction modules. For fast bulk data transfers, such as are needed as Sonar array displays are updated or compared, a very high-speed (30+ Mbytes/s) proprietary multidrop network is provided. In this scheme, traditional and proprietary networks play mutually supportive roles and succeed, where a purely traditional or proprietary solution would not.

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Computers and network components: the latest releases of the Open Systems Interconnect (OSI) standard for network technology.
Network Interfaces

is required to act on received data. “Even with specialized real-time networks, the processor still has to go out and look for the particular address location of transferred data,” he adds.

To eliminate these problems, Rich says that Ironies uses a DMA model to eliminate latency—the receiving processor’s memory itself is updated, so it doesn’t have to go out

What’s really needed is to go into a type of network structure that is scalable, so it not only solves today’s problems but has a plan for the future.

—Fred Sammartino,
Sun Microsystems

and look for updated information. Ironies’ MCPL approach uses a full 32-bit-wide datapath capable of saturating a VMEbus. Rich also hinted that a next-generation data pump utilizing a 64-bit architecture and providing full concurrent transmission and reception in an ASIC chip will soon be in the offing.

The future beckons

Planning activity in the advanced network arena is reaching a fever pitch, yet solutions appear to be painfully slow in coming. FDDI, for example, has been under development for a decade—and it appears to be suffering from a bit of a backlash. Ethernet, though closing in on a 20-year tenure, has sold more in the past two years than in the previous 18. While no one has explained exactly why this is so, it has to be due in part to the fact that simple, twisted-pair solutions have come down into the mass-market price range. But certainly another factor is that customers have been waiting for a next generation that just hasn’t emerged. For some, the wait may have been too long.

Although FDDI is here now, as Radstone’s Silverman points out, it still has some hurdles to clear. Because the copper interface hasn’t yet been defined, the only real solutions are fiberoptic. And the infrastructure for fiber just isn’t here yet. In addition, it’s an expensive solution—not just for the transducer components, but for the connectors, assembly and other factors involved in working in a new medium.

And just as copper-based FDDI emerges, it looks as if ATM will be coming out, too. ATM approaches haven’t seen much use outside a relatively closed consortium—even the telephone carriers don’t have a handle on it. So, while they battle to put together the ATM specification, different groups within the same company are feverishly working on FDDI.

It’s often the case when a number of different technologies are vying for leadership that one will have a discernibly stronger position. This can be by virtue of stronger technology, backing of a major market player to the exclusion of others, or acceptance by a major application area. None of these factors are in place and, in fact, trends are made even more confusing by multiple heatedly pursuing multiple choices.

No clear winner will emerge in the next year or so, but what at one time appeared to be a clear field for FDDI may now be somewhat cluttered. The ATM approach espoused by the consortium makes a lot of sense, provided it can be practically implemented. And if it can also be tied in as a full subset of Sonet, it would clear the way for a network from desk to desk.

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Postscript

Network interfaces are suffering from the same turmoil that’s affecting other standards, including bus, peripheral and memory interfaces. The problem is that the current generation of interfaces is obsolete, before the next generation has hit.

Solutions such as FDDI—an order of magnitude faster than Ethernet—were thought to be able to handle the anticipated traffic from future generations of processors, but are already falling short.

The other facet of the network dilemma comes from LANs. LANs satisfied the needs of system users throughout the 1980s where network nodes were largely located in a single office or building. Now though, with the expansion of services available and the global approach to business, it’s critical to have access across the globe as fast as across the room.

Current networking approaches are falling pitifully short.

There may well be a single solution to both the problem of a faster, scalable technology as well as one which will cope with the seamless integration of local and wide area networks. This single solution could be the approach taking advantage of a subset of the ISDN specification. ATM as a network interface is just beginning to emerge. If the specification settles out as expected, it will supply a full subset of both ISDN and Sonet.

Though there are no “ideal” solutions, ATM solves a lot of problems with a single approach. Fixes to FDDI such as FDDI2, are just that, fixes or Band-aid solutions which only temporarily solve the problem.
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**DESIGN STRATEGIES: TELECOMMUNICATIONS**

**Video teleconferencing on British shores**

The British Telecom design team: Front row, left to right: Steve Banthorpe, manager of aesthetics; Richard Gedge, overall manager; Shabir Azani, responsible for forward coding; Maurice Perini, responsible for parts of core coding loop in codec; Adam Guest, camera control system; Allister Kemp, microprocessor control system. Back row, left to right: John O’Donnell, video demultiplexer; David Norman, technical support; Peter Forty, head of codec development group; Stephen Jackson, channel interface; David Dolby, originator; Richard Whiting, technical support; Richard Incoll, technical support. Absent from the photo are: Tony Leaning, architectural design; Steve Barnes, audio system manager; Wesley Pretty, software development.

Designing a video teleconferencing system involves building bidirectional equipment that can capture and compress video and audio images from one location and transmit them to another, where the signals must be received, decompressed and reconstructed. This is no mean feat. A design team must have expertise in both video and audio technology, as well as in telecommunications equipment design.

In 1988, a team of engineers at British Telecom (Martelsham Heath, Ipswich, England) assembled to design the VC2100 video codec. Over the last two years, this equipment has been integrated into the VC5000 video teleconferencing system.

The electronics in a video teleconferencing system consist of a video and audio codec (coder/decoder unit) connected to an interface that links the codec to different telecommunications networks—this is the VC2100. In addition, a dedicated control system must be designed to provide the interface between the user and the VC2100 codec. This is the VC3200, or terminal management suite (TMS); it provides control for cameras, monitors, audio/picture switching, and user functions. Both these components make up the VC5000 videoconferencing system.

In operation, up to six video sources may be connected to the system. The TMS is used to provide the selected source for transmission to the VC2100. Up to three incoming, or previewed, pictures are shown to the user on the monitors.

The custom computer system in the VC5000 cabinet can be divided into two sections. In the bottom half of the cabinet is the TMS, which lets you control the teleconferencing environment—setting up the cabinet to match the dynamics of the room, selecting audio levels and switching video sources among the various monitors and cameras. In the top half of the cabinet, a second rack contains the video codec, audio codec and transmission-control electronics.

Dave Wilson, Senior Editor
According to Peter Forty, head of the codec development group, it was a conscious decision of the design team to separate the electronics control of the user's environment from the core video codec. That way, third-party codecs could be integrated into the unit if needed, while still providing the overall functionality that was required.

Both the video codec and the control section were designed around modular board components. The codec design is similar in dimension to triple-height VME cards that plug into a backplane bus, while the TMS resembles 3U VME. The British Telecom bus, however, is proprietary in nature. Many backplane bus signals are specifically used to route video signals around in real time; the speed of the bus is closely coupled to the coding algorithm used in the design. "In order not to compromise the reliability of the codec and get the throughput, it was necessary to design our own bus," says Forty.

**Many standards, one system**

According to Mike Carr, head of the video systems section, the company needed to bridge between two different line and picture rate standards—PAL (Phase Alternation Line) in England and NTSC (National Television System Committee) in the United States—before the codec could be developed. It's not cost-effective or practical to build custom PAL teleconferencing systems for the U.K. market that would be incompatible with custom NTSC solutions developed for the U.S.

The British Telecom solution was to develop yet another standard—CIF, or common intermediate format. Using it, any video teleconferencing system can capture video in either NTSC or PAL format, convert it to the CIF format, process the data in that format, and then output in either PAL or NTSC format.

To accommodate the CIF standard, the codec contains video input and output sections that convert the CIF format used for internal processing to the television standard of the country to which the equipment as well as controlling the video picture quality, at either full CIF or QCIF (quarter CIF) resolution. Also, the control card can change the audio/video mix—more compression can be applied to audio than video and vice versa. In addition, it can select a data port to which to send a fax or to bring terminal communication from one end of the system to the other.

The key component of the video compressor is the motion estimation board. Processing the data from the current and previous frames, then comparing the pictures and finding the best fit with a motion vector, is the most compute-intensive task of the whole Px64 compression algorithm, says Forty. "In the encoder, it is unnecessary to perform motion compensation, but in the decoder you must be able to accept motion-compensated data streams. You can trade off how you perform the motion estimation and compensation in the encoder," he adds.

Indeed, the H.261 standard lets you perform ±15 search windows and provide a vector to the line, but because it's so compute-intensive, different approaches can be used that are still compatible with the standard. "A lot of the proprietary chip sets that are becoming available now are based around ±7 search windows," says Forty. "That's not full search. We have implemented a full-search algorithm that compares every single one of the search positions of the previous data with the current data and arrives at the one position that gives the least energy for the search." On the British Telecom board, the motion estimation processor has been implemented in eight Motorola ASICs, with a ninth for memory control.

British Telecom decided on the Motorola parts when building the original demonstration vehicles for H.261. On the first demonstrator, each of the processors that computed one row of an 8 x 8 block of picture data was a single card of
TTL adders and multipliers. "To shrink that to a size that was cost-effective," says Forty, "each of those cards had to be one ASIC. We ended up with eight cards with eight ASICs on each card to perform motion compensation." For its part, the VC2100 represents the next level of integration: each of the eight-ASIC cards has become one ASIC. The ±15 frame search operation can be performed on a single board. In the next-generation design, the eight ASICs will be shrunk into two.

### FPGAs and ASICs
Throughout the design of the codec, British Telecom made heavy use of programmable devices, PROMs as well as PALs and Xilinx FPGAs. In that way, the design team was able to keep track of any changes in the H.261 compression standard, even while the hardware was being designed.

At the time the system was developed, the final H.261 specification hadn't been agreed upon. "The order in which the H.261 picture header information was sent to the line changed," according to Stephen Jackson, channel interface manager. "There were also changes to the DCT function." But using FPGAs helped. "Within an hour we could reconfigure those programmable devices to cater for every change we were called upon to make," he adds.

That, of course, necessitated partitioning the system architecture—deciding which functions were to be put into gate arrays and which were to go into FPGAs. "We were very conscious of which elements were constants, as well as which were variables," says Jackson. "In addition, we looked at which functions could provide us with a building block that could be used in other designs. We left those things that were subject to change in programmable form."

The Xilinx philosophy matched that of the British Telecom engineers. Forty says, "When developing hardware, we prefer to make a stab at what we want the function to be, and then debug that function in real time in the hardware rather than do a lot of simulation, attempting to get the thing right the first time. With video, the biggest aid to debugging is to see the video." Forty doubts whether a simulator that could simulate the operation of the design could have provided the turnaround time his team desired.

In addition to semicustom ICs and FPGAs, British Telecom worked with Inmos (Almondsbury, Bristol, England) to define the characteristics of a DCT chip. Although the DCT function itself is fixed, the final DCT specification isn’t absolute. It lets you build DCTs with different internal rounding, truncation and accuracies, provided that they meet the overall accuracy required. The accuracy was specified so that, given the rate at which the video picture is updated, the two ends of a video teleconferencing system keep track of one another.

After motion compensation and filtering, the data is passed to another board across the backplane bus, where a difference operation is performed on the new video in the current frame and the motion-compensated video in the previous frame. Then a DCT is performed, followed by quantization—a process that requires that the data be transformed from block to zig-zag format. Once quantized, the data is run-length encoded, then passed to a buffer control and out to a line interface card.

British Telecom used a TMS320C15 from Texas Instruments (Dallas, TX) to perform the rate-control function inside the

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**TMS control system**

![Diagram of TMS control system](image)

The complete British Telecom video teleconferencing system—the VC5000—comprises the VC2100 codec and the terminal management suite (TMS), or VC3200. The 3200 was developed separately from the 2100 and provides the user interface and control system for the cabinet, since a codec alone can’t provide those functions. Shown here is a block diagram of the TMS.
DESIGN STRATEGIES: TELECOMMUNICATIONS

codec. Deciding on the chip was easy. According to Forty, "The designer was familiar with the chip and it also had the amount of I/O that was required. It was fairly cheap, too."

In operation, the buffer containing the video and audio data provides status information to the TI rate-controller processor. It's obviously important to control the buffer, so that the rate at which the buffer is written into equals the rate at which data is taken out. Depending on the status of the buffer, the processor decides how to control the flow of data to it—whether or not to drop a frame, or whether to intercode or intracode the data.

The processor is also fed information from the motion compensation processor regarding the fit between the previous and current frames. The TI DSP chip makes the decision as to whether motion compensation is necessary or not. "If it's a really ropey fit," says Forty, "it probably isn't worth performing compensation." The chip also takes input from the user, making trade-offs regarding the characteristics of the preferred image. These include the preferred picture size, frame transmission rate and picture quality.

As far as test and diagnostic system maintenance are concerned, British Telecom designers also planned ahead. A dedicated board inside the codec is responsible for

Looking at standards

To understand the functions performed by the video codec, it's first necessary to understand the H.261 standard or Px64 compression algorithm commonly used in video-based telecommunications. Px64 codes a video frame that's been divided into blocks for transmission using discrete cosine transformation (DCT), quantization and run-length coding techniques. If interframe coding needs to be performed, the frame to be coded is stored in memory, in addition to being coded and transmitted as bitstream output. In this way the frame (or, more accurately, 8 x 8 blocks within the frame) can be compared to corresponding blocks in the next frame to be transmitted. A motion-estimation processor compares the image stored in memory to the next transmitted image. A vector is created that relates the values of the prior block to the current one. The differences between the two frames, as well as the motion vectors, are then fed to the DCT, quantizer and entropy coders before transmission.

"Fundamentally, you take differences between each frame, transform the differences and line code them. Part of that process is to perform run-length coding on the data to reduce the amount that needs to be transmitted," says Peter Forty, head of British Telecom's codec development group. Using difference information substantially reduces the amount of data that needs to be compressed, since most scenes in teleconferences contain only small regions of change while other areas remain constant.
online checking. It determines if the codec is working correctly, and in production testing it can be used to test each board in isolation. “It allows us to ‘loop out’ each board,” says Forty, “and even in some cases to go to a finer resolution than that. We take all of the other boards, except the board that we are interested in, out of the loop and then apply a source from the test control card to the card under test and see if the data coming out of that card is what we expect to see. The card also provides a direct interface to the user. It has all the terminal drivers, as well as the code for interacting with a remote terminal to set up the call.”

Networking it

In any videoconferencing system, designers can expect to work with a variety of data at different clock speeds; and all of it must be synchronized before the codec will operate correctly. Video, audio and the channel interfaces must be locked to a reference clock on the network. “One of the most difficult things in the design of a video/audio codec is ensuring that the devices that are supposed to be locked together are locked together and that you don’t get interference from the different clocks that are floating around,” says Forty.

“With the channel interface, you probably have ten or more clock sources,” he adds. Forty was reluctant to reveal how such engineering challenges were solved by British Telecom. The solution appears to be part of the “secret sauce” involved in the design.

As to networking the system, British Telecom supplies a variety of different interfaces to accommodate different speed and transmission requirements. There is an interface to a 4-kbit/s channel which, with an external terminal adapter, allows connection to ISDN (Integrated Services Digital Network). The unit can also provide 56,000 channels for the US27 standard. Yet another standard, RS449, a clock and data interface, can be operated at any rate from 56 kbits/s up to 2 Mbits/s. In the main codec itself, the primary rate channel interface (PRI) is implemented on a single card, with four option slots provided for enhancements; one of those is normally taken up by the 2B access or connection to ISDN or to a terminal adapter.

British Telecom’s latest video tel- econferencing system is already in the works, and will be announced within a few months. We can expect that Peter Forty and his team have again reduced the size of the motion estimation processor through further levels of integration, and have integrated many of the functions previously handled by FPGAs into large, full-custom ASICs. The resulting system may simply house a single bay of electronics, perhaps in as few as three to four boards. As British Telecom continues its work with Motorola, the actual parts designed into next-generation British Telecom systems may eventually become standard parts offered by Motorola on the open market. They may embrace not only the Px64 standard, but also the MPEG multimedia compression and decompression standards as well.
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- The BUSCON East Show Guide will focus its value-added editorial on the trade-offs involved in choosing a standard-bus architecture for a board-level implementation of a product versus a non-bus implementation; on the trade-offs involved in choosing a microprocessor or microcontroller for building bus-based or non-bus implementations; and on the issues involved in choosing the optimum operating system or kernel for the particular microprocessor architecture that will be used in an embedded or real-time application.

- Included will be a general overview of the market for embedded and real-time systems written by Senior Editor Warren Andrews. Rounding out the report will be selected viewpoint articles from the leading experts in the development of architectures, operating systems and kernels, and real-time software development tools.

Distribution: The guide will be polybagg ed along with the Eastern portion of COMPUTER DESIGN's August issue for a total distribution of 50,000+. In addition, a special mailing will go to all of the preregistrants...and it will be distributed to each attendee at the show.

Issue Date: August 1, 1992

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P}rhaps the greatest opportunity to shorten the design cycle comes from spending time more effectively in the lab. While innovations in front-end tools have enabled designers to rapidly create designs on paper, and advances in manufacturing processes let you make up prototypes nearly overnight, most engineers still spend over half the design cycle in the lab, trying to sort out whether the design they created really works.

Logic analyzers, with their ability to passively observe circuit activity, play a key role in this process, helping designers discover logic system bugs and aiding them in refining their hardware/software integration process. And because emulators don’t exist for many of the newest microprocessors, logic analyzers often provide the most sophisticated tool available for critical development work.

Faster, wider and deeper are still the demands that drive the development of logic analyzers. To meet the demands of today’s faster and more complex microprocessors, these devices must be able to monitor signals at high rates, provide more channels to watch address and data buses and supply more memory to display larger segments of monitored waveforms.

### Speed, channel count up

Responding to designers’ demands, logic analyzer vendors have made steady advances in speed and channel counts over the past year. As the table shows, several analyzers offer synchronous clock speeds of over 100 MHz, while asynchronous clock rates above this figure have become routine. Likewise, channel counts of over 100 are now fairly common—even at maximum sampling rates. Less progress has been made in memory depth, although some vendors are making a concerted effort in this area.

Reflecting the opinion of several vendors, Jim Stager, vice-president of marketing at Biomation (Milpitas, CA), thinks that memory depth is important in today’s design environment. “The industry seems to have caught up with the demand for faster and wider logic analyzers,” says Stager. “We have logic analyzers available with hundreds of pins. And we’re certainly keeping up with most of the microprocessors that are out there, and computers. But the depth game hasn’t been played to the full extent.” Biomation probably has the deepest logic analyzer available today, the K450M. A 100-MHz, 64-channel unit, the K450M currently offers 20 Mbyes of memory per channel. In addition, Biomation is sampling 80 and 320 Mbyes/channel in other versions.

While the price tag of $258,000 greatly limits the range of potential users for the K450M, Stager points out that there are applications where it can be essential. “If you want to perform cache tuning or see the probability of a particular instruction being executed during normal code operation, you can just record everything and do post-process analysis on it.” Benchmark testing is another application for which the K450M is appropriate. “For example,” Stager adds, “if you wanted to prove that a theoretical RISC processor will run faster than one that now exists, you could take a recording of the one that exists and code associated with it that it actually executed. Then you could match that up to a simulation model of your theoretical processor as it executes the same code.”

### The two extremes

As logic analyzer vendors continue to advance performance and integration, an interesting polarization has occurred. At the low end, led by Hewlett-Packard (Colorado Springs, CO), the traditional benchtop analyzer is now typically based on a logic-analyzer-on-a-chip solution. As a result, there’s little room for differentiation among these products, except on the basis of price. As the table shows, a handful of such products are available for under $5,000.

At the competitive high end of the logic analyzer market, activity is more diverse. For some time now, vendors have turned to modular solutions, helping both their customers and themselves preserve their investments by swapping in modules when it’s time to upgrade or add new features.

The latest module designed for Hewlett-Packard’s 16500-series logic analysis system is the 16542A, a 2-Mbyte data acquisition card.
## PRODUCT FOCUS: LOGIC ANALYZERS

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<th>Model</th>
<th>Max synch clock rate (MHz)</th>
<th>Max asynchronous clock rate (MHz)</th>
<th>Channels (state/timing)</th>
<th>Channels at sample rate (state/timing)</th>
<th>Memory/channel (state/timing)</th>
<th>Trigerring levels</th>
<th>Minimum glitch width (ns)</th>
<th>Price</th>
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<td>12</td>
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<td>$17,495</td>
<td>Optional: 128k memory, timing to 500 MHz and 1 GHz. Supports all micros to 68040, R3051 and 80486. Modular design allows 360 channels. Includes support for 50-MHz 80486. Optional 64k deep memory.</td>
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<td><strong>Hewlett-Packard Company Inquiries</strong></td>
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<td>204/204 (2 cards)</td>
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<td>4k - 8k</td>
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<td>32, 64 and 80 channel configurations; optional 100-MHz digital oscilloscope</td>
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<td>PM 3585/30</td>
<td>50</td>
<td>200</td>
<td>32/32</td>
<td>32/32</td>
<td>2k</td>
<td>8</td>
<td>3</td>
<td>$5,450</td>
<td>Dual analyzer-per-pin architecture, MS-DOS utilities, IEEE 1149.1 support, offers 2,000 symbol names</td>
</tr>
<tr>
<td>PM 3580/60</td>
<td>50</td>
<td>100</td>
<td>64/64</td>
<td>64/64</td>
<td>1k</td>
<td>8</td>
<td>3</td>
<td>$6,695</td>
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<tr>
<td>PM 3585/90</td>
<td>50</td>
<td>200</td>
<td>96/96</td>
<td>96/96</td>
<td>2k</td>
<td>8</td>
<td>3</td>
<td>$11,450</td>
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<tr>
<td><strong>Keithley Metabyte</strong></td>
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<td></td>
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<tr>
<td>PCIP-DLA</td>
<td>20</td>
<td>20</td>
<td>16</td>
<td>16</td>
<td>4k</td>
<td>2</td>
<td>2</td>
<td>$1,295</td>
<td>Stores and retrieves data trace sets in disk, overlays and compares two trace sets and does pass/fail comparisons on traces</td>
</tr>
</tbody>
</table>

**Compliments**

- MLAS-132: Portable, 8 - 16 bit disassemblers.
- CLAS4000: 19-in. display, Macintosh host.
- K1600: Analog display of all channels.
- HP16550A: Transitional timing, time and state tagging; glitch trigger; compatible with all previous preprocessing.
- HP1650 Series: 32, 64 and 80 channel configurations; optional 100-MHz digital oscilloscope.
- PM 3585/30: Dual analyzer-per-pin architecture, MS-DOS utilities, IEEE 1149.1 support, offers 2,000 symbol names.
- PM 3580/60: Same as above.
- PM 3585/90: Same as above.
- PCIP-DLA: Stores and retrieves data trace sets in disk, overlays and compares two trace sets and does pass/fail comparisons on traces.
<table>
<thead>
<tr>
<th>Model</th>
<th>Max sync clock rate (MHz)</th>
<th>Max sync clock rate (MHz)</th>
<th>Channels (state/liming)</th>
<th>Channels at max sample (state/liming)</th>
<th>Mean/Channel (res/imp) (bits)</th>
<th>Trimming levels</th>
<th>Maximum dwell width (ns)</th>
<th>Price</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Orion Instruments</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Include integrated 100-MHz, digital storage oscilloscope, 24-bit digital pattern generator, analog function generator</td>
</tr>
<tr>
<td>OmnLab 9360</td>
<td>34</td>
<td>204</td>
<td>96/96</td>
<td>16/16</td>
<td>128k - 512k</td>
<td>4</td>
<td>5</td>
<td>$12,550</td>
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</tr>
<tr>
<td><strong>Promark Technology West</strong></td>
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<td></td>
<td></td>
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<tr>
<td>PL 1000</td>
<td>200</td>
<td>1000</td>
<td>384/384</td>
<td>384/384</td>
<td>32k</td>
<td>15</td>
<td>4</td>
<td>$10,000 - $100,000</td>
<td>Operates under Windows 3.1. Optional pattern generator. Real-time comparator</td>
</tr>
<tr>
<td>KLA/2</td>
<td>350</td>
<td>2000</td>
<td>48</td>
<td>48</td>
<td>10k</td>
<td>2</td>
<td>0.8</td>
<td>$25,000 - $50,000</td>
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</tr>
<tr>
<td>PL 100</td>
<td>50</td>
<td>100</td>
<td>32</td>
<td>32</td>
<td>8k/16k</td>
<td>4</td>
<td>5</td>
<td>$5,000</td>
<td>Operates under Windows 3.1. Fits inside any portable or benchtop AT-compatible computer</td>
</tr>
<tr>
<td><strong>Rapid Systems</strong></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>R3200</td>
<td>100</td>
<td>25</td>
<td>24</td>
<td>8</td>
<td>8k</td>
<td>4</td>
<td>10</td>
<td>—</td>
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</tr>
<tr>
<td>R3600</td>
<td>200</td>
<td>50</td>
<td>32</td>
<td>8</td>
<td>8k</td>
<td>4</td>
<td>8</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>R3700</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>—</td>
<td>2k</td>
<td>2</td>
<td>25</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>R3800</td>
<td>100</td>
<td>50</td>
<td>32</td>
<td>—</td>
<td>8k</td>
<td>4</td>
<td>10</td>
<td>—</td>
<td></td>
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<tr>
<td><strong>Tektronix, Test &amp; Measurement</strong></td>
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<tr>
<td>Prism 3002CX</td>
<td>16</td>
<td>200</td>
<td>96/9</td>
<td>96/9</td>
<td>8k</td>
<td>7</td>
<td>—</td>
<td>$6,995 - $9,995</td>
<td>40-Mbyte hard disk, display, keyboard</td>
</tr>
<tr>
<td>Prism 3002CH</td>
<td>95</td>
<td>2,000</td>
<td>18/20</td>
<td>18/4</td>
<td>24k</td>
<td>4</td>
<td>2.5</td>
<td>$9,995</td>
<td>Same as above</td>
</tr>
<tr>
<td>1230</td>
<td>25</td>
<td>100</td>
<td>64</td>
<td>64/16</td>
<td>2k</td>
<td>13</td>
<td>5</td>
<td>$2,995</td>
<td>Digital oscilloscope module, user configurable</td>
</tr>
<tr>
<td>DAS9200</td>
<td>100</td>
<td>400</td>
<td>1536</td>
<td>1536/384</td>
<td>128k</td>
<td>16</td>
<td>2</td>
<td>$30,950</td>
<td>Pattern-generation performance analysis</td>
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<tr>
<td><strong>Trace-Tek Instruments</strong></td>
<td></td>
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<tr>
<td>16CS0A</td>
<td>35</td>
<td>50</td>
<td>16</td>
<td>16</td>
<td>1k</td>
<td>4</td>
<td>—</td>
<td>$1,295</td>
<td>Hand-held, battery-powered; PC software available</td>
</tr>
<tr>
<td><strong>VMetro</strong></td>
<td></td>
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<td></td>
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<tr>
<td>VME-STA</td>
<td>16</td>
<td>100</td>
<td>96/99</td>
<td>96/99</td>
<td>2k/16k</td>
<td>4</td>
<td>4</td>
<td>$10,850</td>
<td>VMEbus analyzer system; 2 slots, simultaneous, state, timing, and anomaly analysis</td>
</tr>
<tr>
<td>FBT-625</td>
<td>50</td>
<td>200</td>
<td>177/1705</td>
<td>177/1705</td>
<td>32k</td>
<td>16</td>
<td>5</td>
<td>$25,000</td>
<td>Futurebus+ analyzer system, 1 slot, simultaneous state and timing</td>
</tr>
<tr>
<td>M28T</td>
<td>10</td>
<td>—</td>
<td>56/—</td>
<td>56/—</td>
<td>8k or 32k</td>
<td>16</td>
<td>—</td>
<td>$9,500</td>
<td>Multibus II analyzer; 1 slot, 64 HW comparators</td>
</tr>
</tbody>
</table>
Each card provides 1 Mbyte/channel of memory with 100-MHz state/timing analysis across 16 channels. An HP-16500A mainframe may be configured with up to five 16542A cards. The configuration of cards can be varied, depending on whether depth or width is more important to you. The choice is between a maximum memory depth of eight channels by 10 Mbits/channel, or a maximum channel width of 80 channels by 1 Mbit/channel. By attaching probe cables from multiple HP-16542A cards through a memory expansion interface, you can access up to 10 Mbytes of deep memory without any additional circuit loading.

Also recognizing the demand for deeper memory, Tektronix (Beaverton, OR) has beefed up the memory in its Centurion, a module of Tektronix’s DAS9200 logic analyzer mainframe. Starting this month, the company intends to expand the Centurion’s trace buffer to a 512-kbit depth behind each of the card’s 1,536 channels.

A key factor behind the demand for deeper memory is the growing volume of software in modern embedded systems. With microprocessors racing at ever faster speeds, systems can crunch more code then ever in a shorter time. As a consequence, the software component of embedded systems has grown. While analyzers have traditionally been thought of as tools for debugging hardware, they’re also finding a role in software debugging and hardware/software integration.

**Software role**

To address the needs of today’s more software-intensive environment, Tektronix has teamed up with software development tool companies to create integrated tool environments. Last year, Tektronix and Microtec Research (MRI—Santa Clara, CA) teamed up to integrate a logic analyzer with software development tools. Called LA-Connect, the product combines C, C++ and Pascal cross-compilers and the X-Ray in-circuit source-level debugger with Tektronix’s DAS9200 logic analyzer. Other tools (such as instruction set simulators and in-circuit debug monitors) are supported by LA-Connect as well. LA-Connect provides an application note that tells you how to use Tektronix’s DAS9200 along with Microtec tools running on a workstation, so that the logic analyzer can provide the hardware breakpoints as you debug.

Microprocessors supported by MRI tools include the Intel i960, AMD 29000 and the Motorola 68000 and 88000 families. Expanding on LA-Connect to include 80X86 chips and tools, Tektronix recently an-
nounced a similar partnership with Concurrent Sciences (Moscow, ID). As a result, LA-Connect now integrates the Softscope source-level debugger and CSI-MON debug monitor from that company. Support for several popular 80X86 compilers is provided.

At the heart of LA-Connect is a software linker that extracts symbolic information from object modules and converts the data to a format that's readable by the logic analyzer. By downloading this data to the logic analyzer via Ethernet, you can take advantage of the capabilities of the DAS9200, such as hardware breakpoints and real-time, state and timing analysis. Designers can correlate the logic analyzer's real-time trace display with their high-level source code.

At a turning point

As design teams grow in size and faster 32-bit microprocessor designs become the norm, the demand for integrated tool sets is expected to increase. With this in mind, companies making high-end logic analyzers are planning their future products with a focus on interoperability.

"If you look at the spectrum of tools in the design environment that designers are working in, you see a lot of workstations," says Ken Panek, formerly a marketing manager at Tektronix. "The trend is to have these logic analyzers integrated at the workstation. That will start at the high end, because that's where the most powerful tools are."

The eventual goal is to let designers integrate hardware and software from within the same environment. "Maybe you could pull up and have a logic analyzer screen, then fill a trace buffer, and then link that back to your source code. These will make the logic analyzer more useful to software engineers by allowing them to stay in their host environment. Such solutions will require deeper memory. There is a trade-off between complex triggering (number of levels of triggering) and deep memory. But I think most users would vote for the deep memory and search for the problem, rather than having 14 levels of triggering," states Panek.

Michael Garber, product line manager for logic analyzers at Hewlett-Packard, agrees that integrated environments are the next step. "We're going to be seeing more connectivity with our customers' computers," says Garber. While the job of a logic analyzer is to capture data, interpreting that data can be a cumbersome task. Connecting a logic analyzer to a workstation and making use of software running on it may help that process. Adds Garber, "If you can just figure out how to hook it up and interpret what you see, its wonderful. That's how we're looking at the problem—trying to figure out how to help engineers do that."

CAE/CAD TOOLS

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- Educational Workshops
- Tutorial Sessions
- Panel Discussions
- Executive Keynote Speakers
- Conference Proceedings
- Exhibits
- Spouse Program
- Banquet/Luncheon Speaker
- Receptions
  (Details in Advance Program)

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Help or hindrance to ASIC technological competitiveness?
Top Level Synthesis --
Does performance meet expectations?

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- FPGA Design
- Designing Multichip Modules
- Mixed Analog/Digital Design
- Designing with ASIC Megacells
- Modeling Sub-Micron ASIC Macrocells

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- Samuel Liu
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- Mentor Graphics Corporation
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- Vertex Semiconductor Corporation
- Eastman Kodak Company

CIRCLE NO. 57
Sparcstation 10 achieves new level of modularity

The recent announcement by Sun Microsystems (Mountain View, CA) about its latest Sparcstation ended speculation on which processor the next-generation workstation would use. In addition to announcing support for Texas Instruments' SuperSparc processor, Sun also took the wraps off one of the most modular and extendable workstations the industry has ever seen.

The new workstation, Sparcstation 10, ends the initial numbering sequence, as well as quieting speculation over what a Sparcstation 3 will look like—there won't be one. The jump in numbering, the company says, is to stress that the new workstation is not simply a next level, but that it represents a leap in performance.

While the key to the new workstation's performance lies in the 3,000,000+-transistor SuperSparc processor (see "Next-generation Sparc—can less be more?" Computer Design, June 1992, p 118), clever memory design, new peripheral interface circuitry and use of the new SBus 64-bit specification all contribute to the 2 to 46 increase in performance over the previous generation. And if that's not enough, the Sparcstation 10 is the first commercial workstation offering built-in ISDN (Integrated Services Digital Network) capabilities.

At the heart
At the heart of the Sparcstation 10 is Texas Instruments' (Dallas, TX) SuperSparc, mounted on a plug-in module. While the first release of the Sparcstation 10 will include a single 36-MHz processor (Model 30), at least three other upgrades were announced at the first release: the Model 41 (40-MHz single-processor version), the Model 52 (with two 45-MHz processors) and the Model 54 (comprising four 45-MHz CPUs). According to Sun, a 50-MHz version will be available by year-end.

In addition, the Model 40 will include a 1-Mbyte external cache, while the 52 will have two Mbytes and the 54, four Mbytes. The external cache makes possible dramatic increases in performance, particularly with applications that can take advantage of this larger memory.

Sun is the first workstation maker to bring multiprocessing to the desktop. The capability boosts performance in many applications that can take advantage of the SuperSparc's multiprocessors—either by using multiple processors with each working on one of several applications, or with each working on different parts of the same application.

On the M bus
The Sparcstation 10's modular design is aimed at letting you quickly and easily upgrade the CPU as well as I/O. Not unexpectedly, the new workstation has SBus expansion slots—four instead of the three provided by the earlier Sparcstations. And the SBus slots are designed to support the latest version of SBus (initially B.0), providing full 64-bit transfers.

But SBus is only one of the modular features of the Sparcstation 10. The included Spare module, connected via the Sparc M bus, permits plug-in replacement of the processors. The module itself can contain one or two SuperSparc processors, along with some interface and cache logic. Units can accept up to two modules, each with two processors.

The M bus interconnect will also let you update processors as new generations come along. For example, a 50-MHz processor can replace the existing 40-MHz unit once the 50-MHz unit becomes available in quantity.

As promised by Sun's board-level group, the Sparcengine 10 (board-level implementation of the Sparcstation 10) will be available almost simultaneously with the desktop version. The single-processor version of the Sparcstation 10 will be available in the third quarter of the year, and multiprocessor versions are expected to be available in the fourth quarter. —Warren Andrews
Siemens intros new generations of 40-MHz 8- and 16-bit MCUs

In what it's billing as the world's fastest 8- and 16-bit microcontrollers, Siemens AG (Munich, Germany) has added higher-performance generations to its two lines. The SAB80C52 and its derivatives are based on the Intel 8-bit 8051 instruction set, while the SAB80C166 family, developed jointly with SGS-Thompson (Milan, Italy), is a proprietary 16-bit architecture. To these families have been added the SAB501, which at 40 MHz is the fastest 8-bit controller around, and the SABC167, which features improvements in interrupt response and on-chip features while running at the 40-MHz external clock rate of the SAB80C166.

8-bit anchor

The anchors of the 8-bit line are the SAB501 and C501-R, which are completely software-compatible with the ROMless and ROMed versions of the 80C52. In re-engineering the core, Siemens optimized the critical paths, tightened the geometry and went to a denser process, but resisted the temptation to reduce the cycles per instruction associated with any given instruction. As a result, the relative execution time for all instructions in terms of cycles per instruction is the same as with the SAB80C52.

The SAB501 is aimed at speed upgrades of SAB80C52 designs and for low-power applications. It can operate over a voltage range of 3.0 to 5.5 V over the standard 0° to 70°C temperature range. The speed limit at the 3.0-V level is 12 MHz, ranging up to the full 40-MHz speed at 5 V. At 40 MHz, the part delivers a 300-ns instruction cycle time. The derivative versions based on the 501 core, which have added peripheral devices on the die, are rated to work at 5 V only.

Siemens is introducing two derivative parts along with the 501: the 502 and the 503. The SAB502 includes 256 bytes of XRAM, 16 kbytes of ROM, eight data pointers, and two watchdog timers. Among other things, it's aimed at users of high-level languages who need more RAM and pointers. The peripheral devices are taken from designs used in an earlier part, the SAB80C517A, which were then reworked under the design rules for the 501 core. The second derivative part, the SABC503, incorporates a 10-bit A-D converter and two watchdog timers, which also come from the SAB80C517A design.

With the SABC167, Siemens has greatly enhanced the interrupt response performance over the SAB80C166, and has increased the overall performance by increasing the performance of the peripherals. The SABC167 has a 50-ns interrupt sample rate as compared to 200 ns in the SAB80C166. Its overall interrupt response time (the time from an interrupt being received until the processor begins executing the interrupt routine) is now 250 ns, down from 400 ns with the SAB80C166. In addition, the SABC167 has 1 kbyte of on-chip RAM to hold up to 32 register contexts if desired.

Packaged in a 144-pin grid array, the SABC167 is probably the biggest 16-bit processor ever. It supports 110 I/O lines, 16 10-bit A-D channels, 32 capture/compare channels, and 52 interrupt sources. It also features on-the-fly ability to switch between five different bus configurations. For example, you can switch between 8- and 16-bit bus widths, select whether the bus is multiplexed or not, and choose the number of wait states.

Library, custom modules to come

Siemens plans to migrate its microcontroller technology through the use of standard library modules (such as RAM, ROM, A-D converters, and pulse width modulators), as well as custom modules developed by Siemens or in cooperation with customers, moving gradually in the direction of full ASICs. Improvements in process technology are expected to be leveraged off the 64-Mbit DRAM work being done in cooperation with IBM.

On the 8-bit side, the SAB501 and 503 are sampling now and the 502 will sample in the fourth quarter of 1992. Production quantities of each are expected the following quarter. Quantity 10,000 pricing for the 501, 502 and 503 respectively is $3.50, $5.50 and $4.00. The SABC167 will sample in the third quarter of 1992 and will be in production in the first quarter of 1993. Quantity 10,000 pricing will be $30.00.

— Tom Williams

McUs at a glance

- SABC501 (8-bit)
  40 MHz
  300-ns cycle time
  300-ns interrupt response
  1.2-µs 8 x 8-bit multiply

- SABC502 (8-bit)
  256 bytes XRAM
  16 kbytes ROM
  eight data pointers
  two watchdogs

- SABC503 (8-bit)
  10-bit analog-to-digital
  two watchdogs

- SABC167 (16-bit)
  40-MHz clock
  50-ns interrupt response
  50-ns counter resolution
  78-kHz pulse-width modulator
  with 8-bit resolution
  144-pin PGA

Siemens Components
Integrated Circuits Division
2191 Laurelwood Rd
Santa Clara, CA 95054
(408) 980-4583

Circle 356
Tool targets transmission line effects in high-speed designs

Contec Microelectronics (San Jose, CA) has unveiled the RLGC Parameter Generator, a 2-D electromagnetic field solver that supports transmission line simulation for high-speed designs (R, L, G, and C stand for the per-unit resistance, inductance, conductance, and capacitance of transmission lines.)

The RLGC Parameter Generator uses a spectral domain analysis method to provide input to Contec’s SI (Signal Integrity) simulator for analysis of nonlinear electronic circuits, including the electrical effects of the interconnects.

Simulation requires accuracy

“Faithful simulation of high-frequency designs demands accurate characterization of transmission lines,” says Paul Wang, president of Contec’s CAE division, “because signal degradation effects such as crosstalk, mismatch and loss greatly increase above 40 MHz. We believe that we have a more precise solution for determining transmission line RLGC parameters than other solvers, which are dependent on the boundary element method.”

According to Wang, the spectral domain method eliminates the need to calculate the polarization charge at the dielectric interfaces, which lets the Parameter Generator accurately compute mode velocities and reduce the matrix sizes and number of unknown charges. “Our method doesn’t have to rely on broad assumptions, limited configurations or other shortcuts that can reduce the accuracy of the outcome,” Wang points out.

Other features of the solver include correct modeling of the edge condition, the ability to handle any number of dielectric layers and arbitrary conductor cross-sections.

The 2-D solver takes dielectric loss into account by calculating the G matrix at the specified frequency—a capability that Contec asserts is imperative for lossy substrates such as gallium arsenide. The tool also accurately computes the R matrix associated with resistive loss in the conductor as a function of frequency without making assumptions about the relative magnitudes of the depth of penetration and thickness of the conductor. This lets the SI simulator include skin effects. In addition to RLGC matrices, the tool calculates mode velocities, attenuation and characteristic impedances.

The RLGC Parameter Generator is available now. Licenses are priced at $4,500 for PC versions and $8,400 for versions that run on Sun and HP workstations.

—Mike Donlin

RLGC Parameter Generator at a glance

- Provides input to Contec’s SI simulator for analysis of nonlinear electronic circuits
- Features accurate modeling of the edge condition, the ability to handle any number of dielectric layers and arbitrary conductor cross-sections
- Accounts for ground plane and ground conductor resistances to simulate crosstalk
- Available now for $4,500 on PCs and $8,400 for Sun and HP workstations

Contec Microelectronics
2188 Bering Dr
San Jose, CA 95131
(408) 434-6767
Circle 351

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Software keeps track of timing delays and constraints

As system clock speeds routinely climb to 50 MHz and beyond, the timing relationships between components in a system become critical. A stumbling block in tackling these timing problems is the lack of accurate timing information for VLSI devices and microprocessors. Logic Modeling software keeps track of timing delays and constraints.

Behavioral-like Shell Software statements with the hardware modeler's ability to detect logic states, providing timing accuracy for full-function hardware models. To reduce pessimism and false errors caused by reconvergent fanout, Release 2.0 provides mechanisms for tracking input pin changes that cause changes on output pins of a hardware model. This capability provides common ambiguity elimination and makes min/max simulation more accurate by eliminating false errors.

**Propagating the unknown**

Unknown states generated during simulation typically represent design errors such as timing violations, state contention or an uninitialized condition. Release 2.0 features a proprietary unknown-propagation algorithm designed to accurately propagate the unknowns presented on a device's input pins, reducing pessimism and inaccuracies. The hardware modeler's unknown-propagation feature supports multisequence unknown propagation. The number of pseudorandom sequences is user-selectable and can be set within the Shell Software.

Release 2.0 is backward compatible with Release 1.3 and 1.2 software and will run with existing hardware models without any modification. Shell Software needs to be modified, however, to take advantage of the Release 2.0 timing features.

In addition to improving the quality of timing information for hardware models, Release 2.0 speeds overall simulation time, according to Logic Modeling. Generally, a hardware modeler offers better performance in simulation than gate-level or structural software models. On the other hand, the performance of long simulations for designs containing a large number of hardware models can be affected by hardware model evaluation time. Release 2.0 supports concurrent evaluation of hardware and software models. This lets the simulator parallel the evaluation of software and hardware models, eliminating any potential simulation idle time due to hardware model evaluations.

Release 2.0 is available now at no charge to users who are covered by software maintenance or standard system warranty. For nonmaintenance users, the upgrade will cost $10,800.

---

Mike Donlin

**Release 2.0 at a glance**

- Provides timing verification information to the LM family of hardware modelers
- Combines behavioral-like Shell Software statements with hardware modeler's logic state information for timing accuracy
- Features a proprietary algorithm to accurately propagate unknown states on a device's input pins
- Supports devices with up to 640 signal pins
- Backward compatible with previous releases

**Logic Modeling**

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Circle 357
SRAM, logic and analog functions from ECL customizable arrays

Synergy Semiconductors' (Santa Clara, CA) System Elements family of bipolar ECL arrays offers embedded SRAM blocks with speeds to 3 ns and compiled metal-only SRAM. Based on Synergy's Asset (All Spacer-Separated Element Transistor) technology, the 1.2-µm System Elements achieve a unity gain frequency of 17 GHz and feature unloaded gate delays of 70 ps at just 200 µA.

The devices' Ocean-of-Cells architecture offers you the ability to craft individual Asset transistors and available resistors into simple analog functions. With system clock frequencies above 1 GHz, the System Elements are suitable for applications in speed-critical products. Synergy jointly developed the new parts with Toshiba America Electronic Components (Irvine, CA), which will act as a second source.

The transistor-level structure of System Elements devices allows implementation of logic gates, SRAM cells or analog functions via personalization of metal layers only.

By not prewiring individual transistors into conventional logic gates, Synergy has built into its System Elements the capability to connect cell components to produce analog functions. Designers can construct analog functions within analog zones, isolated from surrounding digital circuitry by separate power, ground and I/O pins, dedicated bias generators and metal guard rings. Using as few as five transistors and three resistors, you can implement a no-frills analog building block such as a simple voltage comparator in one basic cell. The Asset cell also lends itself to low to medium-resolution A-D and D-A converters.

I Just the start

The initial four System Elements family members include one RAM-Intensive System Element (RISE) with embedded memory and three Universal System Elements (USEs) with nonembedded memory. The SY9BP6R4 RISE device has half a dozen blocks of 3-ns embedded ECL SRAM plus an Ocean-of-Cells array with up to 12,290 equivalent two-input gates of 70-ps logic. I/Os located at the left and right sides of the die may be configured for TTL levels as well as ECL. A six-transistor cell is the basic "core tile" of the SY9BP6R4.

The SY9BP6R4 RAM-Intensive System Element (RISE) has six independent blocks of 3-ns embedded ECL SRAM plus an Ocean-of-Cells array with up to 12,290 equivalent two-input gates of 70-ps logic. I/Os located at the left and right sides of the die may be configured for TTL levels as well as ECL. A six-transistor cell is the basic "core tile" of the SY9BP6R4.

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CIRCLE NO. 58
Standard linear parts from customizable arrays

With analog and mixed-signal circuits, there's an almost endless need for customization, but what I'm hearing about repeatedly these days is ASSPs—application-specific standard products. These are standardized industry-specific products—such as disk drive read channels and telecommunications modems—that are built around an array of analog or mixed-signal cells. Like digital gate arrays, they are configured by their metallization layers, and represent a relatively quick way to tweak performance or add special features to an otherwise standard product.

Linear arrays, however, present some architectural and manufacturing challenges, and very few manufacturers have been able to offer them the same way that, say, digital ASIC vendors have offered gate arrays and standard cells. Manufacturers whose early business consisted of analog arrays—Exar (San Jose, CA), GEC Plessey Semiconductors (formerly Interdesign, Scotts Valley, CA) and Micro Linear (San Jose, CA)—have migrated, with their customers' help, toward standard product offerings. These manufacturers never hid the fact that many of their standard offerings were based on linear arrays. But expertise in disk drive electronics or communications was inevitably more visible than the array-based implementation.

Change is in the wind

That seems to be changing now. Not only are manufacturers such as Micro Linear touting their array technology by showing catalogs of customizable ICs, but the number of array vendors is also growing. An increasing number of IC vendors are admitting, if not announcing, that they too build standard products based on linear array technology. The names include those companies with strong bipolar manufacturing expertise: AT&T Microelectronics (Reading, PA), Harris Semiconductor (Melbourne, FL and Somerville, NJ) and SGS-Thomson (Carrollton, TX).

The reasons for this trend are twofold. First, array technology has changed. New CAE tools, combined with tighter geometries and double- or triple-layer metallization, make for better silicon utilization. The resulting linear and mixed-signal chips are no longer as costly to manufacture as they once were. Second, customization demands are tending toward high-frequency and high-performance areas where the user expects to pay a premium. These are areas where the bipolar expertise of array vendors shows up best.

It starts with a linear array

The foundation for ASSPs is a linear array—a series of commonly used analog devices, such as small-signal transistors, perhaps a beta-matched input pair, larger driver transistors (mostly NPNs), thin-film resistors and capacitors, as well as more complicated devices such as op amps, comparators and voltage references.

These arrays are prefabricated and are available in many different sizes and types, depending on the target application. Implementation and customization of a circuit are accomplished by means of metallization. In the old days, you took home a drawing of the array and drew a metal mask on tracing paper, almost the same way you'd draw the interconnects between components on a schematic diagram. These days, with digitized cell libraries depicting available components, the metallization layers are drawn on personal computers or Unix workstation screens using CAE tools.

Moreover, the architecture of many commercial arrays has been altered. Since linear CMOS and mixed BiCMOS processes allow higher densities, simple transistors and op amp arrays can be pushed to the outer edges of a chip, while the inner cells can include some fairly complicated logic and signal-processing blocks.

In principle, a linear array is a good solution to the problem of fast turnaround. The chips are already made and you simply need to metallize them for your application. In practice, it can be a very expensive way to go. You're actually paying to have the IC devices manufactured twice—once to build the array and certify that all the devices are working and accessible, and again to metallize selected devices and verify that they still work the way you want them to.

Perhaps the only way to avoid paying for silicon real estate and testing you don't need is to obtain 100
percent utilization of the devices on any chip. But because analog circuits are often pieced together by individual circuit designers, almost as a work of art, there's very little consistency between circuit implementations—even for the same application. And, inevitably, analog array chips have a very low utilization. An 80 percent utilization—a borderline proposition for a digital gate array—can be an economic disaster on an analog array. A user might select 80 percent of the devices, but, because there's no consistency between analog device sizes, the 20 percent not selected could be power transistor drivers, which take up half the chip.

Better utilization

But the linear array vendors have become very sophisticated about size and arrangement of devices, gearing them in many cases toward specific industry requirements. A disk drive read channel or communications modem, for example, either of which may have begun life as a metallized array, is repackaged using ASIC standard-cell or handcrafting techniques to provide a tighter layout, smaller chip size and subsequently higher yields. Unused devices and circuit elements are typically eliminated in the process, but in certain areas of the chip the original array may be left intact. In this way an otherwise standard product—albeit, an industry-specific product—can be customized with minimal effort at a later date.

But the die-shrink that comes from knowing precisely what a customer wants also applies to the layout of the basic arrays. Devices that absorb large amounts of silicon area, such as power transistor drivers, are typically no longer included on most commercial arrays. Even the traditional real estate boom, such as thin-film resistors, are optimized in conjunction with laser trimming, to provide a range of resistor values in a very small area.

What Micro Linear calls its “application-focused arrays” include the FB3651 LAN transceiver, the FB3480 switch mode power supply controller and the FC3560 read channel array—arrays are specifically optimized for particular application requirements. The LAN transceiver array, for example, is geared toward 10Base-T applications. It includes nine timer cells, 12 analog function blocks, six high-frequency transmitter/receiver blocks, and 150 digital logic gates. This array has been the basis of standard products such as the ML4651/52 10Base-T transceivers and the ML4651 multiport repeaters.

The FB3480, similarly, includes an oscillator, voltage reference, error amplifier, 2-A output drivers, and is the basis for eight different catalog offerings.

The 10Base-T transceivers are based on Micro Linear’s bipolar FB3600 family, a set of 12-V arrays with 1-GHz devices. The power supply controllers are built around the FB3400 bipolar family, a set of 36-V arrays with 300-MHz devices.

The FC3560 read channel array, however, is based on the company’s FC3500 series of BiCMOS arrays. These arrays provide 5-V bipolar devices, including 4-GHz NPNs, 50-MHz PNP s and 50-mA power drivers, in addition to 1.5-µm linear CMOSs. Available analog circuit blocks include 8-bit A-D converters, 8-ns comparators and op amps with 100- and 350-MHz gain-bandwidth products.

Excited by speed

It's the fresh challenge of high-frequency applications—cellular telephones, wireless networks, fiber-optic links—that's encouraged manufacturers such as AT&T and Harris to show their capabilities in the linear array area. Both AT&T and Harris compete with complementary high-frequency bipolar processes. These are manufacturing processes that provide closely matched PNP and NPN transistors in terms of frequency response (ft), current gain (β) and silicon area. New-generation current feedback amplifiers, low-voltage drivers and receivers (that those that swing close to a +3-V power-supply rail) and push-pull amplifier outputs all depend on the use of matching PNP transistors.

Obtaining good PNP performance, however, depends on isolating transistors from interaction with other elements on the silicon substrate. There aren't too many ways of accomplishing this, and the ones that exist will raise the price of a high-frequency array. AT&T uses a junction-isolated process, in which a series of diffusions and implants converts an N region into a P for use by the PNP transistor. The process requires 18 to 20 masking steps. Harris uses a wafer-bonding technique, in which the isolation regions between transistors are formed by chemical etching through one wafer, which is actually glued through an oxide layer to another.

Products of the AT&T complementary bipolar IC (CBIC) processes include the ALA201/202 and the ALA210 UHF arrays. These arrays offer 12-V NPN transistors with a 4.5-GHz ft and 11-V PNP s with a 3.75-GHz ft. AT&T’s newest complementary bipolar process, the 6-V CBIC-V, provides 10.2-GHz NPNs and 4.8-GHZ PNP s, and provides the foundation for the ALA110 linear array.

In addition to its UHF-1 process, Harris trades on the experience of GE/RCA in linear arrays, suggests strategic planner Brian Mathews. The HTA3000 tile arrays offer 8-GHz NPNs and 4-GHz PNP s, and operate at up to 10 V. Devices built with the process include 850-MHz op amps and automatic test equipment pin drivers with better than 3,000-V/µs slew rates.

But don’t expect any of this high-speed technology—even array-based technology—to come cheap. While this is the area where six-week turnaround is most plausible, NRE—the front-end engineering cost—for a Harris HTA3000 array is “ballparked” at around $97,000.
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