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860 compilers on the way

Dual-instruction mode is one of the more-powerful features of the 860 chip from Intel, but only now have compiler vendors begun to support this mode. Without compiler support, which allows integer and floating-point calculations to be issued in parallel, much of the power of the 860 remains untapped.

The first compiler vendors supporting dual-instruction operation are Metaware (Santa Cruz, CA) and Green-Hills (Santa Barbara, CA). Metaware will support the function in Release 2.4 of its High C, currently in beta test, according to Michael Stebbins, systems engineer. Support from Green-Hills is under development, said Steve Lafferty, director of OEM sales.

Along with dual-mode instruction, software pipelining is another under-exploited 860 feature. Useful for performing repetitive operations that are independent of the results of previous operations (in applications such as vector processing), software pipelining will also be included in High C, Release 2.4.

Again, it's under development at Green-Hills. With these new compiler optimizations and more, Metaware claims that the 860 chip will benchmark at over 86,000 Dhrystones/s, a 41 percent improvement over the earlier release.

Unfortunately, compiler support for the on-chip 3-D graphics engine won't be forthcoming in the short term. Despite the lack of compiler support, the 860 is the 3-D graphics engine of choice in the workstation world.

—Dave Wilson

860 bugs kept under cover

Designers integrating 860 RISC boards into their AT or VME systems shouldn't expect their board vendors to supply a current bug list for the processor—they may not be allowed to. At least one board vendor has been required to sign a nondisclosure agreement with Intel (Santa Clara, CA) prohibiting the discussion of the bugs with customers. All of that vendor's customers have been asked to refer their questions to Intel.

"You can try to get this information from Intel, but it's the kind of stuff they really just guard [the expletive deleted] out of. They just don't want anyone to know. This is extremely aggravating for us because the customers want to know what these problems are too," one board vendor reported. Apparently, after nearly two years in the market, the 860 still has five bugs, one of which is said to significantly affect floating-point performance.

—Dave Wilson

"I'll support any standard as long as it's mine"

A large-scale lobbying effort by the newly named Advanced Computing Environment consortium has begun to sell software developers on a set of standards based on MIPS Computer Systems' RISC architecture. The standards embrace systems including laptops, PCs, workstations, and supercomputers. Among the major players in the 21-member group are Compaq Computer, MIPS, Digital Equipment Corp, Microsoft, and The Santa Cruz Operation. The group's efforts appear to focus primarily on the yet-to-be-available R4000 processor. The consortium has agreed on a variety of features that will provide both binary and source-code compatibility.

These efforts have groups of industry leaders poised for yet another clash over standards issues. "I'll support any standard as long as it's mine," commented one industry leader.

Groups supporting the Sparc and MIPS processors are amassing ammunition. The escalation in competitive maneuvering may explain why Sun Microsystems recently let some of its techies out of the laboratory to tour the country with studies pushing Sparc as the instruction set architecture with the brightest future (see "RISC instruction benchmarks spark performance debate," p 69). Sun is certainly at the top of archival MIPS' hit list and is no friend of the new consortium. Sun president Scott MacNealy was credited with commenting, "Those who can't compete, consort."

—Warren Andrews and Tom Williams

Mac clones inevitable

By delivering an Apple Macintosh-compatible operating system on disk and in ROM, three ASICs that replicate the logic of the Mac, and user interface software based on OSF's Motif, Nutek (Cupertino, CA) will enable OEMs to start designing Apple Mac clones. To get around legal wranglings, the Nutek operating system was written from the ground up and required more than a quarter million lines of code. The chip set has been prototyped and is currently going through simulation and validation. Shipable parts should be ready by the end of the year, according to Benjamin Chou, Nutek's president.

—Dave Wilson

Mentor's Falcon makes slow ascent

Mentor Graphics (Wilsonville, OR) has started shipping the first elements of its long-awaited Concurrent Design Environment, Release 8.0. Phase I of the Falcon Framework software, the Board Station printed circuit board design and analysis tool, as well as thermal-analysis and on-line documentation tools, will run only on older HP/Apollo Domain 400 workstations. Mentor hopes to have these tools up and running on Sun workstations by the end of the second quarter, with third-quarter releases running on the new HP 700 workstations.

The Phase II release will include tools for the design of hybrids, multichip modules and ICs. Phase III will include QuickSim II, Design Architect, System-1076, and VHDL synthesis. Some analysts are downplaying the importance of the Phase I tools because they target only printed circuit board design, which accounts for 15 to 20 percent of Mentor's revenues. Until more front-end tools are released, it's doubtful that Phase I will have much of an impact.

—Mike Donlin

Continued on page 10
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CIRCLE NO. 6
Another record-breaking SBC for Moto?

When Motorola rolled out a new CPU board at the most recent Buscon (January 1991), many in the audience expected the company to also announce the follow-up version of its MVME147. Instead, it introduced the next version of its 88000 RISC-based board, the MVME187. The MVME167, as the 68040-based board was expected to be called, remained elusive.

The 68030-based MVME147 set new price/performance standards for single-board computers when it was introduced. At a list price of $4,995 with very deep quantity discounts, the board was the most successful single-board computer ever offered. It’s reasonable to assume that the 040-based 167 board and 88000-based 187 will share many of the same features, ASICs and design as the 147. Word has it that the two boards were designed concurrently and that software problems held up further promotion of the 167.

With sampling expected to start sometime in July, Motorola expects the 167 to top sales of the 147. According to reports, the board is a “screamer” and, although the list price is rumored to be significantly below that of the 147, there’s no hint the company will tighten up on its discounting policy.

—Warren Andrews

Silicon Graphics hands off RISC, graphics expertise

A strategic agreement between Compaq Computer (Houston, TX) and Silicon Graphics (Mountain View, CA) is expected to pave the way for technology exchange and the joint technical development of future products. The plan includes Compaq’s purchase of a 13 percent equity stake in Silicon Graphics.

Silicon Graphics has agreed to share its Iris graphics library and its expertise in designing RISC-based systems, while Compaq will contribute its expertise in the EISA bus standard, VLSI design and high-volume manufacturing techniques. Using the newly acquired technology, Compaq is expected to build low-cost RISC-based systems with leading-edge graphics. The agreement benefits Silicon Graphics by further promoting its graphics technology. The Iris library is already licensed to IBM for use in its RS/6000 RISC workstations.

—Mike Donlin

Futurebus spec one step closer

With its March meeting, the IEEE 896 working group took another step toward completing the Futurebus+ specification. Negative ballots from the sponsor ballot phase of 896.1 (the logical layer) have been resolved, and the draft is out for another 30-day spin around the block. The physical layer and profiles are already out to the committee for its sponsor ballot phase. Ballot review and negative ballot resolution is expected for the next session.

—Jeffrey Child

Synthesis a hot topic at ASIC conference

Hundreds of Idea’91 conferencegoers left standing room only last month at the technical sessions on low-level logic synthesis. If the number of attendees at the sessions was any indication of how the technology is catching on, synthesis should be a mainstream design methodology before long.

At one session, Howard Landman, senior CAD engineer for logic synthesis at Sun Microsystems (Mountain View, CA), presented a user’s perspective. He told attendees that synthesis tools are not pushbutton, and that they leave many options for designers to explore. Designers should stop asking whether logic synthesis tools are better than human designers, Landman said, and instead ask whether a designer with synthesis tools is better than one without them.

—Barbara Tuck

Committee zeros in on FB military connector style

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Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

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Hard data isn’t so hard to come by

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A key element in making any choice is having the data. In the electronics/computer world, that means benchmarks. Unfortunately, getting objective benchmarks is extremely difficult. While potential users of a particular product—a printed circuit board layout tool, for example—might benchmark several prospective candidates, that data might not be comprehensive and would usually remain within the company. Vendors, on the other hand, routinely benchmark their own and competitive products and make the results public. But the objectivity of these benchmarks is always open to question.

Because user benchmarks may not be comprehensive and vendor benchmarks may be tainted by self interest, the electronics/computer publications you receive—Computer Design included—have been loath to use them. There's also the fear of offending present or potential advertisers if they don't do well in a benchmark. We think that's a mistake.

If a user or a vendor has benchmark data, we think you should see the results—incomplete or not, biased or not—and make up your own mind. Our editors will probe the benchmark data to uncover any underlying assumptions, discrepancies, biases or legitimate differences of opinion and point those out to you. Two of our editors, Tom Williams and Dave Wilson, have done just that in the Technology Updates section of this issue. And we’re going to do more.

Whenever possible and appropriate, we will publish any and all benchmark data our editors can lay their hands on. Editors will work relevant benchmarks into our feature articles and use benchmark data as a jumping-off point for our shorter, news-oriented Technology Update articles. You can help us in this effort by making our editors aware of any benchmark results you've compiled or been shown by vendors or colleagues. Give any one of our editors a call, or call me directly.
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May 12-15
CICC
Town & Country Hotel, San Diego, CA. Global communications is the theme of the 13th annual Custom Integrated Circuits Conference. The show will offer education, technical and new product sessions, as well as exhibits from semiconductor manufacturers, software tool vendors and design houses. Information: Roberta Kaspar, Technical Program Coordinator, 1597 Ridge Rd W, Suite 101C, Rochester, NY 14615, (716) 865-7164.

May 20-23
Spring
Georgia World Congress Center, Atlanta, GA. Spring is a new event that includes Comdex and the debut of Windows World, featuring products, support and education on Windows computing. Spring’s exhibits and conferences will focus on networked computing and multimedia. Information: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, fax (617) 449-6953.

May 20-23
Midwest Electronics Expo/PCB Expo
Minneapolis Convention Center, Minneapolis, MN. The Midwest Electronics Expo and the PCB Expo will conduct a joint conference program this year. The show will feature 30 conference sessions and tutorials, with 10 devoted solely to printed circuit board issues. Information: Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215-1135, (800) 223-7126, fax (617) 232-0854.

June 10-13
Nepon/East ’91
Bayside Exposition Center, Boston, MA. This conference and exhibition will feature products and technologies for the design, fabrication, assembly, packaging, inspection, and test of printed circuits and electronic assemblies. The expected 16,000 attendees will find 375 exhibitors, 17 technical sessions, 7 workshops, and 9 professional advancement courses. Information: Cahners Exposition Group, Cahners Plaza, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60017-5060, (708) 299-9311, fax (708) 635-1571.

June 17-21
DAC
Moscone Center, San Francisco, CA. The 28th annual Design Automation Conference, geared toward electrical engineers, computer scientists and management, will offer technical programs, tutorials and vendor exhibits. Two new panels, “Global Strategies for Electronic Design” and “Implementing the Vision: Electronic Design in the 1990s,” will target high-level management and project and group managers, respectively. Information: 28th Design Automation Conference, 7490 Clubhouse Rd, Suite 102, Boulder, CO 80301, (303) 530-4333, fax (303) 530-4334.

CIRCLE NO. 16

CIRCLE NO. 15
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<table>
<thead>
<tr>
<th>256K Family</th>
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<tbody>
<tr>
<td>PDM41256</td>
<td>32K x 8-28 lead DIP, SOJ, Cerpack, LCC</td>
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<td>PDM41258</td>
<td>64K x 4-24 lead DIP, SOJ, LCC</td>
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<td>64K x 4 with OE-28 lead DIP, SOJ</td>
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<td>1024K x 1–28 lead DIP, SOJ, LCC</td>
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<table>
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<th>4 MEG Family</th>
<th></th>
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</thead>
<tbody>
<tr>
<td>PDM4M096</td>
<td>512K x 8–32 lead DIP, Module</td>
</tr>
</tbody>
</table>

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CIRCLE NO. 18
G. Dan Hutcheson on: Mixed-signal technology

The mixed-signal IC is an emerging new technology that’s easy to overlook because on the surface it appears to be no more than a niche application. If the current trends hold true, however, mixed-signal ICs will be as important to computer designers in the ’90s as ASICs were in the ’80s. But like any new technology generation, mixed-signal requires an entirely new way of thinking.

One reason why it’s easy to overlook mixed-signal solutions is that in the ’80s the technology earned a reputation for being difficult to design. Adding analog, which is also difficult to work with, only made design more tedious and complex. But by bringing the power of digital VLSI to analog, it has been possible to introduce mixed-signal devices with integration scales and complexities that were only dreamed about a few short years ago. They offer digital’s ease of use with analog’s functionality. This new wave of devices is breathing life into new, unique designs that have until now been impossible for all but the most costly design targets.

Mixed-signal ICs follow a pattern in semiconductor technology. Every decade a new technology emerges that dramatically alters how systems are designed. In the 1960s, SSI/MSI IC logic blocks were the foundation for mainframe computers. Then in the 1970s, LSI microprocessors and memories brought forth the first powerful minicomputers, electronic calculators and video games. In the 1980s, VLSI ASICs let designers glue large blocks of processors, logic and memory together to bring mainframe computing power to desktops and laptops. ASIC design methods also allowed chips to bring workstations, personal computers and video games powerful graphics capability.

Each of these technology generations had several common characteristics. They typically gained momentum in the beginning of the decade; they had a new semiconductor technology as their key driver; they made use of the latest scale of integration; they integrated previously separate functions; and they let computer designers differentiate their products in new ways. Mixed-signal is the only technology available today that follows this pattern. Also, mixed-signal is difficult to clone, which protects developers of value-added systems.

Automation brought to bear

Prior to the ’80s, chip and board designs were laid out by hand. Designers were faced with the difficult task of keeping both the electrical design and its physical layout in order. There was a natural split between the two industries.

With the development of ASICs, designers had to integrate the printed circuit design layer with the silicon design layer. A design could no longer be conceptualized as a collection of catalog chips soldered to a board. What had previously been a board of chips became merged into functional logic blocks that were glued together in silicon. The barrier between what was on the board and what was on silicon became fuzzy. The design task would have been virtually impossible had EDA tools not been developed. And not only did EDA tools make it possible to manage these large designs, they also made it possible to build a business in ASICs.

In the early ’80s it was easy to think of both EDA and ASICs as separate trends in technology. ASICs were semiconductors, which were historically a commodity product. So semiconductor companies could focus on chip manufacturing and ignore how ASIC methodologies would affect design—and ultimately the market.

Also, circuit design and chip design had been separated between the systems level and the silicon level. So chip companies could confuse, or ignore, what was going on at the silicon level with the end objective, which was to obtain a working design. Many of the early leaders, such as Interdesign, made the error of believing that the responsibility for system design would continue to rest with the systems houses and unwittingly placed the burden of silicon design on the systems designer. Those that recognized the link between ASICs and EDA tools embraced both methods early on to simplify the systems designer’s task. Virtually every leader in ASICs today attributes
its early success to making EDA software a strategic component of its business.

**Evolution of mixed-signal**

Mixed-signal faces challenges today much like ASICs did last decade. The conventional view of many market researchers is one of those challenges. According to this viewpoint, future mixed-signal devices will have an ever-increasing analog content. Current analog content rates are typically estimated at 5 to 10 percent, and some industry experts project a crossover into the 50 percent region during the mid-1990s (see “Conventional Wisdom,” on facing page).

There are many reasons why this view is not practical. The first is a lack of good mixed-signal simulation tools. Without strong simulation tools, designs with high analog-to-digital content ratios need significant amounts of hand crafting and the intuitive knowledge of an experienced analog designer. Testing mixed-signal devices with high analog-to-digital contents is another area of difficulty. Consequently, designing mixed-signal devices with a high analog and digital content is both expensive and time-consuming.

Second, the pool of analog designers has been shrinking over the years, since analog has not been a popular area in which to work. Additionally, the long market life of most analog parts has meant that relatively few designers have been needed to service this market. The few designers that have remained in analog are the pioneers, and many of them are nearing retirement.

The conventional view that future mixed-signal devices will have ever-increasing analog content has its roots in the earliest announcements of digital applications where microcontrollers were being designed with analog I/O; however, this trend hasn’t continued. In contrast, analog circuits have had increasing digital content. Analog Devices has reported that a 12-bit digital-to-analog converter of the early ‘80s had 58 percent analog content with a mere 475 components. A state-of-the-art Delta Sigma A-D converter today has a 2 percent analog content with a total of 100,000 components. Consequently, the crossover point for analog and digital actually occurred in the mid-1980s (see “The Facts,” on facing page).

Additionally, mixed-signal ICs already account for 8.5 percent of the total IC market. Sales of mixed-signal ICs amounted to $4.4 billion in 1990. This included $0.9 billion in communications circuits, $0.7 billion in converters, $1.1 billion in interface circuits, $0.8 billion in integrated signal-processing circuits, and $0.9 million in other mixed-signal circuits. Another indicator of this technology’s importance is the market leaders in mixed-signal are all significant overall players in the semiconductor market. They include National Semiconductor, Texas Instruments, Analog Devices, Motorola, and Harris Semiconductor.

**A new generation of mixed-signal devices have emerged with integration scales and complexities that were only dreamed about a few short years ago.**

**Emergence of digitized analog**

A problem with the conventional view is that it is grounded in the physical attributes of the silicon, rather than the object: the signal. In silicon, according to this view, analog is analog and digital is digital. So mixed-signal must be the simple placement of the two on silicon.

The fact is that this is not the case. Thanks to the digital VLSI revolution of the ‘80s, it is now relatively easy to design and simulate digital circuits with hundreds of thousands gates and to implement analog functions in digital circuits. These circuits are a paradox because they’re not analog, but they’re also not digital in a pure sense. Pure digital is a control function, where analog is an information-bearing signal.

Consequently, a definition is needed to describe this newly emerging circuit. Much of the ambiguity in mixed-signal has occurred because it is so immensely tedious and complex. Some mixed-signal applications can’t logically be called digital. One example is digital signal processing. The central element of DSP consists of totally digital microcontrollers and multipliers. Still, they are digital elements that are designed for exclusive use in analog applications. Another example is LAN transceivers and subscriber line interface circuits. These circuits are highly digital, but are used for analog applications.

VLSI Research has coined the term “digitized analog” to define these circuits. They are ICs whose function is to aid in the mapping of analog system activities into digital system activities and vice versa. This includes transformations of digital signals into other digital signals when the end objective is to achieve a digitized analog function whose inverse mapping into an analog function will eventually occur.

**Digitized analog is unique**

It’s easy to think of digitized analog as merely converted analog with DSP; however, it is much more. These are just the transmission and engine of a totally new technology. Together, they result in totally new activities that employ digital circuits instead of analog. Digitized analog is the representation of analog signals in digital form. They can be filtered, analyzed and changed with software. Moreover, this can be done on the fly. This enables new functions which couldn’t have existed alone in either domain.

Some examples of digitized analog implementations in systems include the Patriot missile system, compact disk players, digital audio tape, laser printers, copiers, and ISDN. Examples of assemblies include signal generators, automatic braking systems and fuel injection. At the component level, examples range from a simple phase-locked loop to delta-sigma converters, image-compression circuits and image-transmission circuits.

These new types of circuits are evidence that mixed-signal is allowing designs that previously were not possible. Digitized analog nullifies the key criticism made against mixed-signal: that it is too difficult to design. Analog circuits can be designed with digital functional blocks. This eliminates the many parameters that must be tracked for each cell in a pure analog
PATTERNS OF CHANGE IN MIXED-SIGNAL ICs

While conventional wisdom has it that the crossover point for analog and digital will occur in the mid-1990s (top), some industry experts feel that it actually already occurred in the mid-1980s (middle). The resulting technology is digitized analog (bottom), or ICs that aid in the mapping of analog system activities into digital system activities and vice versa. According to some experts, digitized analog is the next wave in semiconductor technology.

Analysis of the interaction of the analog cells on the circuit is also simplified. Digitized analog circuits are a mathematical representation of what is normally represented with materials properties in pure analog. Consequently, they can be designed at the signal level without any concern about the enormous complexities of materials properties at the silicon level.

As a result, many other design barriers are broken down. Existing design tools can be used since the design is digital. Moreover, they can be developed in an evolutionary manner to meet the needs of digitized analog design. After all, Spice will be around for a long time for the purely analog portion. It won't be necessary to wait for the next-generation mixed-signal design tool. And the same will hold true for testing. Also, the aging pool of analog designers will give way to new breed of designers building new digitized circuits.

**Transparency a benefit**

Digitized analog won't merely push converters out to the periphery of the circuit; it will find its place right in the heart of the chip. In that way, it will be a mapping technique, rather than a conversion technique. The mapping ability of mixed-signal can make computers transparent to the user. In many cases with mixed-signal, users never need know that they are operating computers.

Take the modern auto, for example, with ABS braking, electronic fuel injection and engine control. Some cars already have several Mips of computing power. In the future, automobiles will also include smart power, noise cancellation and suspension control. All of this is transparent to users. Mixed-signal also has found its way into color pixelation, image synthesis, disk drives, loud speakers, and displays, to name a few technologies.

This will have significant ramifications for the system designer because modern mixed-signal system development is heavily steeped in converters, DSP, software, and standards development. But while mixed-signal simplifies the design problem, it does not eliminate it; design and simulation tools will still have to evolve.

Mixed-signal offers myriad new benefits and frees designers to think in completely new ways. The challenge, as with any new technology, will be in learning how to master it.

G. Dan Hutcheson is president of VLSI Research (San Jose, CA).
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**Table:**

<table>
<thead>
<tr>
<th>Array</th>
<th>Available Gates</th>
<th>Usable Gates (%)</th>
<th>I/O Wirebond / Tab</th>
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<tr>
<td>H4C027</td>
<td>27,000</td>
<td>19,000</td>
<td>160/188</td>
</tr>
<tr>
<td>H4C035</td>
<td>35,000</td>
<td>24,500</td>
<td>176/208</td>
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<tr>
<td>H4C057*</td>
<td>57,368</td>
<td>40,000</td>
<td>216/256</td>
</tr>
<tr>
<td>H4C086</td>
<td>86,000</td>
<td>60,000</td>
<td>260/304</td>
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<td>H4C123*</td>
<td>123,136</td>
<td>86,000</td>
<td>340/360</td>
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<tr>
<td>H4C161</td>
<td>161,000</td>
<td>113,000</td>
<td>344/404</td>
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<tr>
<td>H4C195*</td>
<td>195,452</td>
<td>136,800</td>
<td>376/444</td>
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<tr>
<td>H4C318</td>
<td>318,000</td>
<td>222,500</td>
<td>464/556</td>
</tr>
</tbody>
</table>

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Are secondary caches for the 486 worth the money?

Dave Wilson, Senior Editor

If the 386 needed a second-level cache controller, does that necessarily mean the 486 will? Some say yes, some say no.

The 486 chip from Intel (Santa Clara, CA) has 8 kbytes of on-chip cache. If that isn't enough, designers can choose from a host of peripheral cache controllers, both write-through and write-back, that will let them build second-level caches to improve cache hit rates. But some question whether the peripheral cache controllers are worth the money.

With each new member of the 486 processor family, they say, Intel adds yet another price/performance point to its PC processor family that makes it less likely that designers would add much extra value to their products through secondary caching techniques. "Intel's pricing on 486 processors is coming down quickly. Clearly, the 25-MHz 486 is priced to replace the 33-MHz 386, moving the 486 into the commodity market where motherboard cost is the most important factor," says Patrick Lee, vice-president of engineering at Cache Computers (Fremont, CA), a manufacturer of 486 PC motherboards. "You have to look at how to balance system performance as well."

Intel's 486 architecture is the key to its performance gains over the 386, as demonstrated by ability of an uncached, 20-MHz 486 system to outperform a cached, 33-MHz 386 system on integer benchmarks.

<table>
<thead>
<tr>
<th></th>
<th>20-MHz UNIX PERFORMANCE</th>
<th>33-MHz 386 DX</th>
<th>20-MHz 486 SX</th>
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<tr>
<td>SPEC INTEGER</td>
<td>7.7</td>
<td>10.2</td>
<td></td>
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<tr>
<td>DHRYSTONES V1.1 (VAX MIPS)</td>
<td>11.4</td>
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<td>DHRYSTONES V1.1</td>
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<td>7.9</td>
<td>11.6</td>
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</table>

Because the 8-kbyte cache already on the 486 chip uses a write-through technique, the number of write bus cycles on the 486 bus increases dramatically. Both Intel and Mosel (Sunnyvale, CA) have contrasted the bus cycle mix for an application running on the 386DX with the same application running on the 486 and found that the number of reads is dramatically lower because most reads are already well cached. It appears, then, that optimizing the memory subsystem for consecutive write cycles is the way to go.

The crucial issue might instead be how well write cycle memory optimization can be performed. Perhaps one way to find out would be to build a processor module with an added 256-kbyte, 32-byte line, 1-line/sector write-back cache, and to measure the bus traffic on the DRAM side of the module. In that case, the read/write prefetch mix might end up as shown in the bottom figure. Here, of the total cycles performed by the processor, the majority of the bus traffic external to the module is spent doing prefetch, and bus cycle time is clearly reduced.

Assuming that Intel's mix is right, write cycle optimization appears to be key. And write-back caching, rather than write-through caching.

<table>
<thead>
<tr>
<th>OS</th>
<th>READS</th>
<th>WRITES</th>
<th>PREFETCH</th>
<th>SECOND-LEVEL CACHE HIT RATE</th>
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</thead>
<tbody>
<tr>
<td>UNIX (avg)</td>
<td>25%</td>
<td>14%</td>
<td>61%</td>
<td>97%</td>
</tr>
<tr>
<td>DOS (avg)</td>
<td>29%</td>
<td>18%</td>
<td>53%</td>
<td>99%</td>
</tr>
</tbody>
</table>

Estimates provided by industry sources of the performance achieved by a 486 with a 256-kbyte, 32-byte line, 1-line/sector write-back cache show that write bus cycle mix can be reduced significantly.
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integrated circuits

A technology update

Data array is simply updated, without initiating any system cycles. On a read or write miss, it gets more complex. Either a read or write miss will generate a system fetch that brings new data into the cache, replacing older data in the cache. However, the data that’s replaced may be dirty, having been updated in cache since it was loaded from memory. This would require a write-back cycle to system memory to update its version of the data. In traditional single-ported write-back caches, this causes a penalty since the system read to fill the cache with new data must wait until the write-back cycle is completed. In the 443, however, hidden write-back cycles permit a background write-back while read and write cache hits continue uninterrupted.

A custom design

Perhaps the most impressive point about the chip, according to Lii, is that the dual concurrent bus controller will support the 486 dual-port burst cache memory. On the other hand, he says, the Mosel dual-port SRAM is a single-source solution and only works with that company’s cache controller. He also believes that the 64 kbytes of external cache provided by the Mosel chip is not enough for the 486. As a result, Lii has elected to design his own ASIC cache controller for the company’s latest project, a 486-based EISA motherboard. He feels that he can gain more in performance by implementing his own algorithm. “And it will cost less than an off-the-shelf part,” he adds.

In the custom design, Lii plans to combine a write-back cache controller with a write buffer as well as a dual-port DRAM controller—all in a single chip. “Our goal is to break through the cache memory bottleneck and at the same time break through the DRAM bottleneck in the EISA system arbitration,” says Lii. Normally, in an EISA system, if the 486 wants to access DRAM and the DRAM is not dual-ported, the processor must go through EISA bus arbitration to obtain DRAM ownership before accessing the DRAM. Lii feels that by implementing a dual-port DRAM cache controller he can reduce that bus arbitration cycle.
Communications Genius

With the development of the new Enhanced Serial Communication Controller (ESCC2), Siemens has demonstrated a new genius in high-speed multi-protocolling. The ESCC2 (SAB 82532) offers an extraordinary range of protocol options at a high-speed transfer rate of up to 10 Mbit/sec in synchronous mode. Supporting X.25 LAPB, ISDN, LAPD, HDLC, SDLC, and both ASYNC and BISYNC, the ESCC2 offers outstanding capabilities for a wide variety of applications. And it is as adaptable as it is powerful. The ESCC2's flexible 8/16-bit bus interface allows it to easily adapt to either Intel or Motorola microprocessors. Plus, it provides direct 8/16-bit accessibility to all registers, as well as DMA and both vectoring and non-vectoring interrupt modes. This ensures efficient data transfer to and from host system memory, for fast, accurate and reliable multi-protocolling.

For superior performance and flexibility, the ESCC2 features clock recovery up to 4 Mbit/sec, storage capability of 64 bytes in each of its four on-chip FIFOs and four encoding schemes: NRZ, NRZI, FMx and Manchester. In addition, it offers user-programmable features such as 16/32-bit CRC, time slot assignment, and an 8-bit parallel port. The result is an excellent CMOS device with only 40 mW power consumption for all kinds of multi-protocol applications.

For more information on the ESCC2, or to find out how you can receive your inexpensive PC-based evaluation kit (EASY 532), call 800-456-9229, or write: Siemens Components, Inc. 2191 Laurelwood Road Santa Clara, CA 95054-1514 And put the communications genius of Siemens to work for you.

CIRCLE NO. 21
time, specified at 8 ms.
For its initial foray into the 486 ISA market, Cache Computers had chosen a second-level write-back cache controller chip from UMC (Santa Clara, CA). "Using the UMC chip we found that less than 2 percent of the time the processor was going out onto the bus to write to the DRAM," says Lii. Read hit rate on the board, he claims, is running nearly 99 percent. For a write hit, it's around 96 percent.
Mylex (Fremont, CA) is another vendor that, like Cache Computer, believes the Mosel chip was a less-than-adequate solution: in its own EISA 33-MHz 486 motherboard, Mylex has elected to use 128 kbytes of write-back cache. Pioneer's Lee says he would consider the Mosel part as a contender for his next-generation design, along with another controller from Opti (Santa Clara, CA). The Opti chip is part of a two-chip set that includes a bus controller peripheral chip. It integrates not only the cache controller but a memory controller and it can support up to 512 kbytes of write-back cache.

"Boosting the performance of the cache isn't the only way to enhance system performance."
—Jack Lii, Cache Computers

Faced with a plethora of newer 486 Intel derivations that will cover an expanding spectrum of clock speeds, potential users of off-the-shelf cache solutions have split into two camps: one group that resorts to custom ASICs when their volumes get high enough and another group that doesn't believe in the benefits of cache techniques. Cache controller vendors may find themselves selling products to a very select customer base at the highest end of the performance range.

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Transputer performance boosted to 10x that of its predecessor

Tom Williams, Senior Editor

The first member of a new family of transputers has been introduced by the Inmos division of SGS-Thomson (Colorado Springs, CO). The transputer, code named H1, boasts an order of magnitude increase in all performance parameters, except power consumption. Performance has improved thanks to enhancements in the processor architecture as well as in the communications section of the chip, both of which now occupy approximately equal areas of silicon.

The H1 peaks at 200 Mips and offers 60-Mips sustained throughput with 25-MFlops peak and 10-MFlops sustained floating-point performance. Overall performance improvements include enhanced communications via the processor's four serial links. Each bidirectional link now runs at 10 Mbits/s in each direction.

Superscalar architecture

Gains in processing performance of the transputer come from a new pipelined superscalar architecture that passes multiple instructions per cycle down the pipeline, from a hierarchical memory scheme with cache hierarchy and from the reduction of cycle count for instructions. Most instructions now take between two and five cycles. In addition, fast CMOS process lets the part run at 50 MHz. Even with the enhancements and additions to the instruction set, the H1 maintains compatibility with the T805 transputer.

The H1's superscalar architecture supports multiple instruction units (IUs) that can execute in parallel for a sustained instruction rate of 4 instructions/cycle. The architecture is supported by an intelligent pipeline that automatically routes instructions to the proper execution unit without the need for a sophisticated optimizing compiler. The pipeline also has access to a 32-word workspace cache, which stores the most recently used local variables. The workspace cache eliminates in many cases the need to go to the on-chip cache for data.

Instructions are fetched in groups of four 8-bit instructions, that is, one 32-bit word. Operands for some instructions must, of course, be fetched on subsequent cycles, which introduces gaps between some instructions in parallel paths in the pipeline. But the hardware itself is able to avoid pipeline stalls. When a group of instructions is fetched, a hardware "grouper" scans them and decides which type of instructions they are and to which IU they should be routed. The grouper then re-sorts them onto the proper paths in the pipeline, which includes stages of instruction fetch, grouping, local cache access, address generation, memory read, execution, and memory write.

With this superscalar architecture, not every instruction will perform every function possible along the pipeline, and, as noted above, there will be times when not all instruction units are busy. The traditional way to handle such an architecture is to have an optimizing compiler analyze the code and schedule instructions to optimize the use of parallel execution units.

This involves inserting No-Ops into the code to avoid pipeline stalls when an IU will be idle. Instruction scheduling in hardware avoids padding the code with No-Ops, instead throwing them in at the last minute when the idle IU needs them. This avoids bloating the code with unneeded instructions (which is especially bad for embedded applications, because they seek to occupy minimal space). It also eliminates the processor overhead involved with fetching and processing No-Ops.

The workspace cache is also an important element in avoiding pipeline stalls. "You can think of it as internal to the pipeline," says Raul Diaz, senior field application engineer at Inmos. "So the pipeline, when it's.fetch-
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ing local variables, doesn't ever have to go to the on-chip cache because it has its own registers inside where it keeps the latest parameters." The workspace cache allows two reads and one write on every cycle, so statistically there's little chance of a stall during the cache access stage of the pipeline.

The on-chip cache itself is a fully unified set-associative 16-kbyte cache. It can store both instructions and data and allows 4 accesses/cycle. But the cache is also configurable. It can be set up as a 16-kbyte system RAM for use with compact embedded applications, for example, as an 8-kbyte RAM and an 8-kbyte cache, or as a full 16-kbyte cache. For those who wish to use a communications scheme other than the serial links manager David Dornblaser.

Another problem arises when there are more "channels"—software virtual links for communications between processes on separate transputers—than there are physical links. The solution on the T805 and earlier transputer models has been to write special multiplexing software, for which Inmos has developed libraries.

The H1, however, uses a hardware communications processor called the virtual channel processor (VCP) that can multiplex up to 16,000 virtual links onto one physical link. The VCP packetizes communications in 32-byte message packets, each of which gives a distinct header and end-of-packet (or end-of-message) field. The VCP automatically decodes the headers provided by the transputer architecture, there are instructions for support of shared memory and DMA-based coprocessors.

**Enhanced communications**

Current transputer technology allows interprocess communication via memory on the same transputer and via four serial links between processes residing on different transputers. But the complexity of a network can make applications development difficult and may make porting applications to new systems even more so. "Portable software demands that the details of the network be relatively transparent," says Inmos technical marketing manager David Dornblaser.

The C104 dynamic routing switch automatically reads message packet headers to make its routing decisions (A). If the output link is free, a temporary circuit is created to send the packet from input to output with no buffering (B). As the end-of-packet tail token is pulled through, the circuit vanishes (C).

Inmos, to tell which packet headers are to be routed to which physical links. As a packet comes in, its header is decoded, and the routing switches automatically create a temporary circuit for the data. As the end-of-packet "tail" passes through, the channel is closed, like dirt collapsing behind a burrowing earthworm. This is done with a latency of less than 1 µs. A single C104 can handle up to 32 physical links.

**Real-time enhancements**

In addition to its four serial communication links, the H1 also has four hardware interrupt lines that could be thought of as "bit links." They let a transputer either receive or generate interrupts. Error handling, which was a global function on the T805, now lets errors be handled locally on a per-process basis. A trap handler can be assigned to most processes to manage errors. For catastrophic errors—errors that have no assigned handling—a message can be sent to the system control process over an additional link, the control link. The control link is used exclusively to propagate an error message over an entire network of transputers.

Also new is a protected mode. Normal processes, called P-processes, run in user mode and are protected against other "untrusted" processes. They aren't allowed to access systems-level instructions, which are reserved for "trusted" or operating systems-level processes.

Inmos is porting real-time kernels and operating systems to the H1. One of these is the Chorus operating system by Chorus Systems, which includes a Unix-compatible programming interface. Real-time kernels include VRTX by Ready Systems and C Executive by JMI Software Consultants. According to Diaz, Inmos already has in place a suite of development tools including a C compiler and network configuration tools.

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80-MHz RISC processor screams through floating-point

Dave Wilson, Senior Editor

Companies introducing new RISC processors into today’s crowded market must be either crazy or extremely optimistic that they can bring something new to the processor party. Betting on the latter scenario, Micron Technology (Boise, ID), better known for memory technology than processor architecture, will roll out a new processor dubbed FRISC in the third quarter.

The objective of the FRISC project was to develop a 64-bit processor with fast context-switching time and high floating-point performance. By targeting embedded-control and signal-processing applications, Micron hopes to avoid direct competition with the likes of Intel and Motorola. Despite that fact, a comparison with the 860 from Intel (Santa, Clara, CA) will be inevitable.

The FRISC chip consists of seven functional units: the bus unit (BUSU); a program control unit/vector interrupt unit (PCU); an instruction fetch unit (IFU); a register file (RF); a block-transfer register scoreboard unit (BTRSU); a data load/store unit (DLSU); and an execution unit (EXU) consisting of a parallel floating-/fixed-point multiplier and a floating-/fixed-point adder/subtractor unit. The processor executes in a five-stage pipeline and can handle background block-transfer load/store operations, in addition to instruction buffer loading.

Banked, fully mapped system

The FRISC virtual memory system differs from the hierarchical memory caching technique supported by the Intel 860 design and is best described as a banked, fully mapped system. The 32-way, byte-addressable, interleaved memory supports a 12.5-ns cycle time both in the chip and to the Interleaved Memory Buffer (IMB) registers, a 20- to 30-ns DRAM page-mode cycle time and an 80- to 110-ns DRAM row/column cycle time.

A direct-mapped cache in the IMB MMU maps the virtual row address bits to the physical row address bits. This banked fully mapped virtual-memory scheme implies that the DRAM column addresses are both physical and virtual memory addresses. The IMB operates in a write-back manner with a page-mode write-back to the current DRAM page being performed only if there was a write to one of the eight 64-bit double words of that bank’s line.

“Such a memory architecture implies that the chip will be well-suited to data that is heavily vector-oriented,” says Scott Israel, director of marketing at Alacron (Nashua, NH), a manufacturer of 860 accelerator boards for the PC bus and VMEbus.

**FRISC vs. 860**

The 860 takes a more conventional hierarchical memory approach than FRISC. Designers can cache instructions, data and address translation information directly on chip.

There are other differences between the FRISC and the 860 in the way interrupts are handled and context switches are performed. On the FRISC, the PCU is responsible for generating the next instruction addresses that are directed to the IFU. The vector interrupt unit prioritizes one of 16 interrupts and sends the interrupt service address of the vector table to the IFU. Both preemptable and non-preemptable interrupts can be serviced by the unique design of the interrupt system. The interrupt latency can be as short as two machine cycles (24 ns) if a non-preemptable routine is not in progress. Since the entire set of pipeline registers are duplicated, a low-overhead real-time interrupt service routine could load or store data or refresh the DRAM and return to the current process in four machine cycles. The vector interrupt sub-unit and the block-transfer sub-units support message-passing communication in large-scale parallel applications, as in Mach.

The 860, on the other hand, is
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<table>
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<tr>
<th>VME</th>
<th>VSB</th>
<th>VBAT</th>
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<tr>
<td>- Captures up to 64K VMEbus events</td>
<td>- VSB State Analysis</td>
<td>- VMEbus Anomaly Trigger</td>
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<td>- Stores 96 VME signals with a time tag during each event</td>
<td>- Switches analysis between VME and VSB buses</td>
<td>- Screens 98 lines for 28 classes of violation</td>
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<td>- 50MHz VME Timing Analysis</td>
<td>- Synchronous sampling of VME/VSB events up to 25MHz</td>
<td>- Fully automatic with 104 preset triggers</td>
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<tr>
<td>- Bus Master Capability</td>
<td>- Slot number identification command</td>
<td>- 37 individual LED's and trigger outputs</td>
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<tr>
<td>- Printer/Passthru port for connection to Printer and Host Computer</td>
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<td>- Detects extra transitions on strobe line</td>
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Pushing back the limits of floating-point performance

While today's fastest microprocessors run the double-precision Linpack at 14 MFlops at best, the FRISC achieves a 340-MFlops double-precision Linpack (65-MFlops single-precision), using a bank-interleaved DRAM main memory. Micron Technology claims that this performance is relatively independent of vector size.

The FRISC CPU has a peak floating-point performance of 160 MFlops single precision and 80 MFlops double precision. A unique fully scoreboarded block-transfer unit supports double buffering of the 64-word five-port register file so that background load/store operations can occur in parallel while current data is being processed by the execution units.

Unlike the Intel 860's dedicated units for integer and floating-point calculations, the FRISC's floating-/fixed-point arithmetic sub-unit performs all 32- and 64-bit integer, signed, and single- and double-precision IEEE 754 floating-point instructions, as well as maximum, minimum and subtract/compute condition code instructions for each data type. Full support for IEEE 754 rounding and exception handling is provided. A new instruction can be issued every clock cycle. A floating-/fixed-point multiplier sub-unit performs all fixed- and floating-point multiplications, and a full-precision divide and square root.

All single-precision operations, mixed-precision operations and fixed-point operations can be issued every clock cycle. Double-precision operations can be issued every other machine cycle. Full support for IEEE 754 rounding and exception handling is also supported. Chained operations are directly supported for single-, double- and mixed-precision floating-point operations.

more software-intensive. It handles interrupts through the use of traps. Traps cause interruption of normal program flow to execute a trap handler program. Vectored interrupts must be implemented with vector interrupt controllers and software. Full hardware mechanisms to save and restore the machine state were considered unnecessary in the 860, and are performed in software.

The FRISC PCU also contains the master clock control circuitry to control the pipeline interlocks due to instruction buffer misses or block-transfer scoreboard hits, as well as the vector interrupt processing. Hardware control of pipeline interlocks reduces the burden on the compiler and is critical to achieving a tightly coupled processor and DRAM- and I&M-based memory system.

The IFU contains eight fully associative instruction buffers that are constrained to load using a least re-
cently used replacement strategy. In addition, a valid buffer permits the buffer loading operation to occur in the background, with the first instruction issue occurring once the first valid instruction is loaded into a buffer.

The DLSU performs all single and block-transfer load/stores to the five-port RF. Since all single or block-transfer pending loads are scoreboarded by the BTRSU, the RF can be made to operate as a double-buffered memory with a background load of new data, or to store processed data occurring in parallel with execution unit processing. The five-port RF allocates two read ports and one write port to the EXUs and one read port and one write port to the DLSU.

The BUSU arbitrates between the IFU and DLSU bus requests and generates all memory selection and timing. On-chip configuration registers permit the entire memory address definition and timing to be easily modified to suit a given application. Direct support of the write-back mechanism for the IMB MMU is transparent to the DLSU and further improves the performance of the system's average memory access time.

A board-level demonstration supercomputer using the FRISC processor will be produced in 256-Mbyte and 1-Gbyte configurations. The FRISC CPU and the eight IMB MMUS are each housed in 164-pin LCC packages and are mounted in a 4x4-in. mechanical assembly that utilizes a mainframe-grade AMP interposer interconnect system. The entire mechanical assembly will be thermoelectrically cooled so that the chip temperature is maintained at a constant 25°C. The board can operated in two configurations, either connected to a Sun host running Unix via a host interface unit and controlled with a remote procedure call mechanism, or operated in a stand-alone mode.

Although Micron is still in the early stages of software development, the company has examined the applicability of both VxWorks from Wind River Systems and the Lynx OS from Lynx Real-Time Systems. On the multiprocessing side the company is leaning toward supporting the Mach operating system, since hardware hooks for multiprocessing are provided on-chip. •

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CIRCLE NO. 28

COMPARISON CHART

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<th>DTI CAT1010 486</th>
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CIRCLE NO. 29
Interconnect key to speed of new programmable ASICs

Barbara Tuck, Senior Editor

The bottom line in the programmable-device market is to give designers the fastest time-to-market with the highest-speed device. The founders of Peer Research, now QuickLogic (Santa Clara, CA), having invented the original PAL devices at Monolithic Memories, can claim a familiarity with that market. QuickLogic principal John Birkner and his peers, convinced that a low-impedance interconnect is the solution, have created a highly conductive path, or ViaLink, between two metal layers of CMOS in their just-announced programmable ASICs (pASICs). VLSI Technology (San Jose, CA) is using a standard high-volume 1.2-μm CMOS logic process, jointly developed by the two companies, to manufacture the pASIC 1 family, expected to be in volume production by midyear.

For the ViaLink element in its pASICs, QuickLogic uses a high-resistance amorphous silicon, similar in electrical characteristics to the silicon dioxide that insulates the vias, or vertical openings, connecting one metal line to another. The application of 10 V to a via containing a specially deposited layer of amorphous silicon triggers a flow of programming current that permanently changes the structure of the silicon. The result is a metal-to-metal connection with a resistance of less than 200 Ω. Key to QuickLogic technology is the plasma-enhanced chemical vapor deposition equipment needed to deposit the amorphous silicon, equipment that wasn't available until a few years ago.

Essentially an antifuse structure created in a programmable via, the ViaLink interconnect emulates that of gate arrays by hooking logic gates together with real wires. Competitive devices, according to Birkner, simulate real wires with memory-type floating-gate structures or transistor pass-gates switched with RAM cells. These active connections, with effective resistances in the range of 2,000 to 3,000 Ω and high-parasitic capacitance, can severely limit device speed.

Programmable wires

QuickLogic claims the pASICs' hard-wired physical link and regular interconnect structure will let the devices maintain raw speeds even in fast pipelined designs. Speed-compatible with 80386, 80486 and RISC 1,000 Ω. "Actel goes down to the substrate and does its magic in the active area of the circuit," says Birkner. The QuickLogic via in which the link is formed is more than one and a half orders of magnitude thicker than an Actel dielectric antifuse, according to QuickLogic. The capacitance associated with an unformed ViaLink element is, therefore, many times lower.

The density of the QuickLogic pASICs "is a matter of definition," says Birkner. A count of what Birkner calls "honest gates" yields a 500- to 4,000-gate density range for the first parts to go to production. When compared with erasable programmable logic device or Xilinx Logic Cell Array gates, those counts would have to be upped to 1,500 to 12,000, according to QuickLogic, which claims that 20,000 gates are within the reach of the pASIC technology.

Granularity of pASICs

The pASIC logic cell has 23 inputs and consists of two 6-input AND gates, four 2-input AND gates, three 2:1 multiplexers, and a flip-flop. Each cell can accommodate logic functions up to 14 inputs and consists of two 2:1 multiplexers, and a flip-flop. Each cell can accommodate logic functions up to 14 inputs in width. All 200-gate array-like library macros have built-in scan cells. Flip-flops can be configured as a D, JK, T, or RS function, and toggle rates are over 130 MHz for a simple D flip-flop and over 110 MHz for a JK.

Each pASIC device consists of a matrix of logic cells between rows and columns of interconnecting metal. The densest member of the family at initial introduction, the QL16×24, contains 384 logic cells in a 16×24 array. According to QuickLogic, approximately a dozen equivalent gates out of each logic cell would be used in a typical application.

QuickLogic supports its devices with a Microsoft Windows 3.0-based environment (initial release will not support multitasking) on the personal computer. A database software architecture permits users to combine general-purpose third-party...
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An old argument: Can amorphous silicon conduct?

More than two decades ago, Stanford Ovshinsky began theorizing that amorphous silicon could match and exceed the semiconducting performance of expensive, carefully grown silicon crystals. The scientific community ridiculed Ovshinsky for his belief that an amorphous material, with atoms scattered randomly, could conduct electricity, and difficulty in manufacturing Ovshinsky’s “glass transistors” did little to lend credibility to his claims.

Ovshinsky did not let his detractors discourage him. The amorphous silicon-based, electricity-generating solar cells he makes at Energy Conversion Devices (Troy, MI) are attracting worldwide interest. The thin-film technique used to make the solar cells could be adapted to produce ICs, Ovshinsky says.

He has at least been recognized in the dictionary; the “Ovonics” entry credits the first two letters of the word to Ovshinsky’s name. Ovonics is defined in Webster’s Ninth New Collegiate Dictionary as “a branch of electronics that deals with applications of the change from an electrically nonconducting state to a semiconducting state shown by glasses of special composition upon application of a certain minimum voltage.”

The SPDE tools include automatic test vector generation. Placing and routing a pASIC can be done at the rate of 1,000 gates/15 min, according to Birkner, who says that the software is based on simulated annealing technology out of the University of California at Berkeley. At present, QuickLogic provides its own device programmer. QuickLogic communicates with third-party tools through a proprietary ASCII interface description, the QuickLogic Data Interchange Format, rather than through the EDIF (Electronic Data Interchange Format).

As QuickLogic releases information on its long-awaited pASICs, competitive device makers are doing anything but resting on their laurels. Altera (San Jose, CA), for instance, is just now revealing architecture details of its 0.8-µm CMOS MAX 7000 EPLD family. Parts with 10,000 and 4,000 gates will be introduced in the fourth quarter and the remaining members next year. High-end density is 20,000 gates, and in-system speeds have been boosted to 70 MHz from 50 MHz for MAX 5000 parts.

The MAX 7000 Programmable Interconnect Array has been enhanced to minimize additive delays associated with earlier devices. The improved interconnect introduces less than 2 ns of signal skew, compared with about 13 ns for MAX 5000 parts. By removing EPROM elements from the direct signal path, Altera has reduced across-the-chip logic delays to 15 ns.

MAX 7000 devices have five dedicated product terms per macrocell (up from four in the MAX 5000). Additional product terms can be borrowed from adjacent macrocells through the use of parallel logic expanders, new with MAX 7000 devices. The incremental-delay penalty for using parallel expanders is 2 ns/macrocell, down from the MAX 5000 6- to 12-ns penalty for shared expanders, also available on MAX 7000 devices with a fixed 6-ns incremental delay. A programmable speed/power trade-off option for the MAX 7000 parts involves a 10-ns speed penalty for quarter-power operation. The devices are register-configurable as D, T, RS, or JK flip-flops.

The Windows 3.0-based MAXPlus II toolset that supports MAX 7000 designs includes a multitasking capability. According to Altera, a 5,000-gate design typically can be compiled in 10 minutes or less with the new software. MAXPlus II also supports EDIF.

National Semiconductor (Santa Clara, CA) just recently announced a new electrically erasable CMOS PLD architecture that features a paged configuration, similar to that used in memories. The paged architecture of the 1,000- to 4,000-gate Multiple Array Programmable Logic (MAPL) family is aimed at sequential designs and consists of multiple PLAs interconnected via programmable macrostate registers and a global input bus. The macrostate register outputs have fixed feedback paths to the global input bus to determine which PLA “page” is enabled. Only necessary product terms are active and consume power, thus reducing current draw to 140 mA max.

The company guarantees a worst-case system speed of 45 MHz (with feedback) across the family of MAPL products. Programmable output macrocells can be configured to act as either DE-, JK-, RS-, or T-type flip-flops. National supports its MAPL architecture with its own Open Programmable Architecture Language software package.

Steadily mounting competition among complex PLD and FPGA vendors is making one-upmanship the order of the day. But architectural details and spec sheets aren’t enough to popularize a particular family. That comes only after designs have been completed successfully, and the resulting silicon matches design specs. Hopefully, the newer architectures and more sophisticated tools will let users design parts that perform as well as they look on paper.
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Because the reasons to look into 386 Smart Cache are really starting to pile up.
Supercomputer maker embraces standards

Warren Andrews, Senior Editor

Supercomputer maker FPS Computing (Beaverton, OR), formerly Floating Point Systems, has just announced its first supercomputer family that embraces a variety of industry standards from the Sparc processors to Hippi (high-performance peripheral interface) and VMEbus. And on the software side, the machine is fully Unix compatible. The supercomputer performance—533 Mips, 13.4 GFlops—is achieved using a combination of scalar, vector and matrix processors in the company's own massively parallel computer architecture.

And while much of the system incorporates standard architectures, the main processor bus handling the multiple processors, memory and I/O retains its proprietary identity. Unlike conventional backplane buses, the FPS 500 family of supercomputers uses what marketing vice-president Steve Campbell describes as a scalable interconnect architecture. The architecture is implemented in what he refers to as a "centerplane." The physical configuration is one in which the various processor, memory and I/O boards radiate off the centerplane much like spokes off a wheel. This also includes the memory system—a large hierarchical memory—and address translation and virtual caches.

Three types of processors share the centerplane: scalar, vector and matrix processors. Each processor is actually a group of parallel processors whose number is dependent on the application. The processors get their data from the main memory system and communicate to each other through the main memory.

According to Campbell, the centerplane comprises four buses with an aggregate data transfer rate of better than 1 Gbyte/s. The centerplane handles the dual role of minimizing distances—and therefore propagation delays—between boards, and reducing the length of the backplane and therefore the linear dimension of the machine.

Campbell emphasizes that FPS' 500 series will provide supercomputer users GFlops performance with the support of key industry standards. And, he points out, the prime element in providing the type of performance required is the ability to match—through the correct combination of processor quantity and type—the processing power to the customer's needs.

Coprocessing allows scaling

Campbell defines FPS' multiprocessing approach as a coprocessor approach, rather than an integrated approach such as that used by Cray's approach, the scalar and vector processors are treated as a co-processor, so if more scalar processing power is required, only scalar processors are added. Similarly, if only vector processing is needed, additional vector processors can be added without disturbing the scalar function. The coprocessor works like a shared memory-management-type connection where the scalar processor passes jobs across to the vector processor, freeing the scalar processor to do other functions and handle other parts of the application.

The system configuration—how many scalar, how many vector and how many matrix processors are included—in any given machine is determined by the particular application. In a scientific application, for example, says Campbell, more vector processors will be needed compared with a database management application, which would call for a higher component of scalar and matrix processors.

One key to operating in this coprocessing/parallel processing environment is that the operating system must know exactly how many of each processor are in the system. "The Unix operating system has full knowledge of the configuration of the machine, including how many and what kind of processor as well as the amount and type of memory," says Campbell. The Fortran and C compilers used in the system automatically generate vector code when the application calls for it.

And while Campbell touts the efficiency of the compilers, he admits that in some intense applications it's possible for a programmer to boost efficiency even more by writing code such that it is best suited for the mix of processors. "In most cases, the machine configuration should be transparent to the programmer," says Campbell. "Programmers need simply to write standard Fortran or C code."

I/O plugs into standards

The I/O subsystem on the FPS 500 series is a memory-mapped I/O with various flavors of I/O types ranging from processors handling VME to the latest high-performance approach such as Hippi. "VME is pretty much the I/O standard in the industry for large computer systems to interface disks, tapes and standard peripherals of various technology," says Campbell. Hippi is targeted at 800-plus Mbits/s (100-plus Mbytes/s) and is currently being considered as an ANSI standard.

In operation, the memory-mapped I/O is relatively simple.
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Basically the application program requests I/O, and the operating system posts a request for an I/O device to handle the operation. The operating system tells the I/O controller to perform the requested task and interrupts the application when the I/O transaction has taken place. "This results in a very high-performance asynchronous I/O capability," says Campbell.

"On VME—including VME64—we're capable of increasing performance through such techniques as using disk arrays, where data can be written (read) to multiple disks over multiple controllers," he says. "In this way it's possible to gang together multiple VME controllers resulting in an aggregate throughput greater than would be possible with a single device."

Even with these techniques, however, it's not always possible to achieve the types of data rates needed for many applications. "We have to go beyond that and look at things such as Hippi," Campbell says. "In addition to conventional peripheral interface, Hippi is being developed for a variety of other applications. For example, it can be used for high-speed communication from one computer to another, or as a high-performance interface for disk arrays.

"We have a strategic relationship with Maximum Strategies, which is building a Hippi-based disk array that supplies some 30-plus Gbytes of storage at something like a 120-Mbyte/s data rate," he says. "This will be interfaced to the FPS 500 through a built-in Hippi connection.

"There's a lot of 'rational' speculation that more and more high-end systems will be interfaced to Hippi as a means to get access to high-performance data and share data between systems. Further, work with vendors such as Network Systems Corp developing Hippi switches is making it possible for a single machine to talk to a high-performance switching system and have access to a variety of devices whether they be disk drives, computers, graphic frame buffers, or whatever."

With its advanced I/O capability coupled with a flexible massively parallel compute engine, the FPS 500 series is at the leading edge of high-performance computers and servers currently available. Its strong advocacy of industry standards makes it an attractive alternative to strictly proprietary solutions. Futurebus+-based solutions, however, are expected to be announced as early as later this year boasting the same type of performance, only with a standard processor/memory bus substituted for FPS' centerplane.

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set up.
Single-chip DSPs invade SBus

Warren Andrews, Senior Editor

S

Bus is rapidly becoming host to a variety of digital signal processing chips and data acquisition functions despite the limited board area (about 3x5 in.) and low-power budget allotted to the normally space-consuming, power-hungry functions. Ariel (Highland Park, NJ) offers two fixed-point boards based on Motorola's 56000 24-bit chip and one based on AT&T's DSP32C 32-bit floating-point chip. In addition, Vigra offers a 56000-TMS320C30 in the near future and, not too far down the road, squeeze the 96000 into an SBus form factor. And Sonitech's sales and marketing manager, John Collins, reports active plans under way to plant TI's next-generation DSP chip, the TMS320C40, on an SBus platform as soon as it's available.

But the integration of such complex floating-point functions on a tiny card requires a lot of design and manufacturing magic. The main job is to bring data acquisition circuitry on-board intended for hi-fi audio interface applications. Lock¬
boro has announced an SBus card based on Texas Instruments' 320C31, a scaled-down version of its 320C30. And most recently, Sonitech International (Wellesley, MA) introduced a high-performance SBus card based on TI's 320C30.

But that's just the beginning. Almost every manufacturer represented has plans to expand its SBus DSP offering soon. And undoubtedly some newcomers are ramping up for entry into the field. Sky Computers, for example, has already introduced an 1860/1960 coprocessor board and will undoubtedly migrate some of its other DSP technology to SBus. Ariel's director of marketing, Les Listwa, says, "We plan to put together an SBus board based on the DSP chip, connectors and memory take up almost 90 percent of the board area, leaving precious little real estate left for bus interface and boot functions. In fact, to bring memory up to the requisite megabyte, Sonitech had to resort to a plug-in memory module positioned over other components.

An I/O board market

"We've seen a tremendous response to our SBus board, particularly in applications where customers need to work with real-time data on a Sparcstation platform," says Collins. Ariel's Listwa shares Collins' enthusiasm but observes, "We've seen a lot of interest and inquiries, but sales are just now starting to ramp up."

But even early results indicate that SBus will be a winner in both commercial and industrial markets.

Sonitech's SBus DSP board is designed to take only a single slot. In many cases, as illustrated, two of the three standard Sparcstation slots are taken by double-width SBus boards such as the frame buffer shown.

DSP board makers hope to cash in on some of the business as Sparcstations are used in increasingly more scientific and industrial applications. Some caution, however, that the performance advantage currently enjoyed by the Sparcstation may be eroded by products such as the new EISA-based machine from Hewlett-Packard.

On and off the board

"When you're talking about something with the processing power of the 320C30, one of the critical factors is being able to keep feeding the DSP data," says Sonitech's Collins. All the DSP boards offer some provi-
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sion in addition to the computer bus to get data on and off the board. Ariel uses what it calls its DSP Port, which a number of DSP companies using the 56000 have standardized. It essentially brings out the data pins of the processor, letting it rapidly take and output data.

Sonitech provides a similar port using one of the TMS320C30 parallel ports to get data on and off the board. In addition, the serial ports of the DSP chip are brought out to the same connector. "We're in the process of designing an external SCSI interface—and perhaps other interfaces—to let users simply stream data off the DSP board," says Collins. "First, we need to do this externally because we can't really be sure of having another SBus slot available to tie SBus cards together internally. Many of the applications we've seen use a double-width SBus frame buffer or other function card leaving only a single SBus slot for additional adapters."

The need for getting on and off the board is driven primarily by the broad variety of applications in which DSP boards are used. Many applications call for some kind of spectrum analysis, which requires digitizing an analog signal and processing the resulting data. Sonitech, Ariel and other companies offer a stand-alone digital-to-analog/analog-to-digital converter to handle the job. "The product we offer is a 16-bit data acquisition box, which interfaces directly with our SBus card," says Collins.

But the reason for keeping the data acquisition section separate from the workstation and the DSP board involves more than simply the number of slots available. With 16 bits of resolution—approximately 1 part in 65,000—the noise within the workstation's enclosure, and coming in through its power supply, tends to greatly reduce the available resolution, says Collins.

Still other applications

While many applications call for some kind of data acquisition, says Collins, others require a different type of I/O capability. "For example, one of our customers uses our DSP board to perform vibration analysis of an oil-welling drill head to eliminate the need to pull the cutter head up for frequent examination," he says. "In addition to the 'go-no go' information on the drill head, all the information is logged and maintained as part of the well-drilling record." In this case, information is taken directly off the DSP card to an SCSI adapter where it's permanently logged on disk.

In still other areas, says Ariel's Listwa, DSP boards are used as accelerating coprocessors for the workstation. The data being processed can be anything from speech analy-
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sisi to specialized math processing. Still other applications are just opening up, including image and pattern recognition in everything from human physiology studies to automated inspection.

"Still many of our applications lie in audio," says Listwa, "and we're in the process of developing a 16-bit A-D, 20-bit D-A SBus card just for such applications." Though he anticipates that some of the noise from the computer system may compromise the final resolution, he says the company offers a personal computer-based product that provides about 90 dB signal to noise. He expects the SBus card to do as well.

Not just for desktops anymore

Though SBus DSP boards are starting to ramp up in volume, they're just touching the edge of the emerging market. According to Peter Palm, product line manager for Sun board/embedded systems products at Sun Microsystems (Mountain View, CA), Sun is doing a brisk business in board-level Sparcstations and will continue to ramp up as companies such as Foxboro begin to use Sparcstations as embedded computers.

A number of dedicated SBus add-on chassis are also emerging from companies such as Texas Microsystems. These provide the electronics to interface to an existing SBus slot and three—or more—additional expansion slots to add adapter boards. The major limitation to that approach is that the memory is mapped to only the original slot, and, depending on the expansion option card(s), memory space could be restricted.

Sun also offers its IE board—essentially a Sparcstation on 6U VME that's second-sourced by Force Computers (Campbell, CA). Force will also be developing a 2E Sparcstation II equivalent board to be released soon. Both of these single-board computers will work with a two-board SBus/VME adapter board introduced by Sun at Buscon '91/West.

With Sparcstations starting to invade the industrial marketplace, there will undoubtedly be a growing need for all varieties of I/O cards, from multiple serial channels to parallel I/O and from low-resolution data acquisition to all varieties of frame grabbers right through and beyond many of the DSP functions just emerging.

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CIRCLE NO. 40
Analysis tools help digital designers avoid analog speed traps

Mike Donlin, Senior Editor

As microprocessor clock speeds climb beyond the 20-MHz mark, electrical connections no longer behave as simple pathways that conduct signals from one device to another; instead they're complex transmission lines subject to a range of faults—namely crosstalk, ringing, time delays, parasitics, and impedance mismatches.

Because transmission line effects are getting worse and experienced analog designers are rare, sophisticated analysis tools are emerging that can simulate analog effects on digital circuits so that engineers can place components, connectors and cables for optimum performance. The Greenfield tool suite from Quantic Laboratories (Winnipeg, Manitoba), for instance, predicts faults by simulating the electrical effects of high-speed transmission lines on a variety of applications including printed circuit boards, hybrids and integrated circuits, as well as cables, connectors and other interconnect media.

The newest addition to the tool suite, BoardScan, is a circuit simulation tool that screens printed circuit board layout data and determines critical nets where crosstalk and signal integrity problems are likely to occur. The software calculates worst-case crosstalk, time delays and signal integrity parameters for critical nets. Results are then listed in a comprehensive net report. BoardScan makes these analyses by applying electromagnetic field principles to the traces, wires and interconnect media to determine their behavior. According to Quantic, this method is much more accurate than some analysis tools that rely on topographically rule-based violations.

"Many tools use heuristics as a rule of thumb and execute simple formulas to deduce where a circuit might run into trouble," says Quantic president Al Wexler. "We think that such estimates are a dangerous proposition. Our tool looks at a cross section of the circuit and calculates the electromagnetic characteristics of that circuit. By analyzing those characteristics and calculating the fields, we can judge the mutual inductance and capacitance of a circuit."

Once BoardScan has identified the critical nets, they can be analyzed in further detail with the Greenfield simulator, which also includes a schematic and graphics editor that lets designers correct the offending circuitry and then resimulate. The latest version of the simulator, Greenfield 3.0, accepts Spice transistor-based models. In addition, Quantic's library of drivers and receivers now includes behavioral models for Fast, ALS, CMOS, BiCMOS, and ECL devices.

Predicting the behavior of signals and crosstalk on complex circuits can help designers avoid costly rework of prototypes. In this example, Quantic Laboratories' Greenfield simulator models the propagation of a signal generated within a multichip module package passing through the leads of its ceramic package, across part of a printed circuit board, through a connector, and through a ribbon cable, and being received at another connector.
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**DESIGN AND DEVELOPMENT TOOLS**

Engineers who design high-speed circuits are faced with a dilemma: if a circuit is designed too conservatively—that is, if traces are placed far enough apart to avoid transmission line effects—then the layout will be large and inefficient, and performance will suffer. If traces are close enough to ensure high-speed performance, then these effects can cause a circuit to malfunction. Therefore, the more information a designer can get about transmission line effects before committing a project to prototype, the less likely that expensive rework will be necessary.

Though these transmission line effects have always existed to some degree, they generally didn’t cause too many problems in the larger, slower circuits of the last 20 years. And because these effects were easy to ignore, the analog design expertise that’s needed today to combat them is hard to come by.

"Remember, not too long ago the computer industry decided that the world was made of ones and zeros," says Al Wexler, president of Quantic Laboratories (Winnipeg, Manitoba). "And there was a wholesale decimation of analog engineering courses in the universities. Then as processor speeds increased, analog effects started showing up in digital designs, and we started seeing the consequences of the lack of experienced analog engineers. As speeds increase and geometries decrease, these problems will only get worse."

Transmit. Line Calculator tool accepts postroute data as well as network topology information entered manually. It then analyzes all the nets in a design using the same database from which the design will be built.

The tool then calculates the effects of loading and circuit topology on system timing and determines resulting signal quality. Signal waveforms are displayed so the designer can analyze the expected behavior of the circuit. The signal information generated by these tools during component placement and routing can then be back-annotated into Quad’s Modular Timing Verifier for comprehensive timing analysis at the system level. “Of course the watchword here is accuracy,” White says. “So we actually represent detail inside the pixel so the finite elements displayed aren’t simplistic representations.”

**Low-end tools available**

Of course not everyone can afford the comprehensive analysis tools such as those from Quantic Laboratories and Quad Design. But even smaller design houses with lower-speed products can benefit from some sort of transmission line simulator. Personal computer-based tools are available, such as the LineSim from HyperLynx (Redmond, WA), that give preroute simulation information to assist designers in component placement.

The LineSim software is an interactive tool that predicts circuit response and calculates board trace impedance. The circuit to be simulated is specified in a schematic where users can select transmission lines, resistors and capacitors via a mouse. The simulation itself is displayed in an oscilloscope format. To resimulate after a parameter change, the user modifies the schematic and replots. No recompilation or netlist step is required. The tool supports a library of digital devices that are modeled for device nonlinearities such as dynamic driver impedance and diode clamping. In addition, LineSim models printed circuit board trace geometries including microstrip, buried microstrip, stripline, and asymmetric stripline.

Though these tools offer varying degrees of accuracy and performance, they all have one thing in common—they give designers vital information during the place, route and simulation phase of circuit design.

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SOFTWARE COMPONENTS GROUP

CIRCLE NO. 42
RISC instruction benchmarks spark performance debate

Tom Williams, Senior Editor

Another salvo of benchmarks has been fired in the often-heated debate over the advantages and disadvantages of certain RISC architectures. A recent study conducted by Sun Microsystems (Mountain View, CA) has analyzed the Sparc and MIPS instruction sets using the widely accepted Spec benchmarks.

The analysis showed a small difference between the two processors in terms of the performance provided by their instruction set architectures. But after isolating architectural differences, the study concluded that the combined effects of the strengths and weaknesses of the compilers and library routines used on both processors failed to give either a clear advantage. MIPS Computer Systems (Sunnyvale, CA) has countered that analyzing instruction usage doesn't necessarily reveal anything about performance.

One of the authors of the study, Sun engineer David Ditzei, claims that it is not about performance, but only a look at efficiency of instruction set usage. Somehow, the issue of real-world performance seems to come up anyway.

Multiple performance factors

The analysis started from the premise that differences in instruction set utilization could only come from three sources: differences in instruction set architecture; differences in the compilers; and differences in the library routines, which may have been hand-coded and, hence, used different algorithms. One of the points conceded by the study is that even if a benchmark analysis is divorced from timing and system architecture influences, such as cache and memory organization, a raw instruction count doesn't necessarily reflect true performance. The study further concedes that to be fair there must include functions that cause delays similar to executing instructions. But using factors other than actual instructions to normalize the comparison of instruction usage gives MIPS an opening to claim that many other factors must be considered in evaluating the two processors.

On both MIPS and Sparc processors, for example, a load instruction is often unable to return its data before the cycle immediately following the load. MIPS requires a no-op instruction in the intervening time, delayed by the hardware interlock even though an instruction is not executed. Factoring out differences such as this produces a closer overall instruction count between the two processors. But it also opens the question, "Why not also count cache access and multiplexing and other elements of the processor that can cause delays?"

Benchmarks and architectures

The Spec benchmarks consist of 10 programs (six floating-point and four integer) written in C and Fortran. The benchmarks include compilation timing, PLA optimization, circuit simulation, chemical, thermodynamic engineering problems, matrix and Boolean equations. Different benchmarks were able to highlight some aspects of the architectural differences between the Sparc and MIPS. According to the study, the most significant architectural differences are that MIPS has only single-precision floating-point instructions, while Sparc has both single- and double-precision floating-point loads and stores while Sparc has both single- and double-precision floating-point loads and stores, giving Sparc an advantage in the float-

<table>
<thead>
<tr>
<th>BENCHMARK</th>
<th>MIPS INSTRUCTIONS</th>
<th>SPARC INSTRUCTIONS</th>
<th>MIPS/SPARC</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE2G6</td>
<td>21,569,202,673</td>
<td>22,878,017,309</td>
<td>0.94</td>
</tr>
<tr>
<td>DODUC</td>
<td>1,613,227,089</td>
<td>1,303,276,485</td>
<td>1.24</td>
</tr>
<tr>
<td>NASA7</td>
<td>9,256,812,144</td>
<td>6,614,656,686</td>
<td>1.4</td>
</tr>
<tr>
<td>MATRIX300</td>
<td>2,775,967,947</td>
<td>1,693,569,255</td>
<td>1.64</td>
</tr>
<tr>
<td>FPPPP</td>
<td>2,316,200,144</td>
<td>1,443,008,199</td>
<td>1.61</td>
</tr>
<tr>
<td>TOMCATV</td>
<td>1,812,691,974</td>
<td>1,626,342,454</td>
<td>1.11</td>
</tr>
<tr>
<td>FLOATING-POINT GEOMETRIC MEAN</td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
</tr>
<tr>
<td>GCCL.35</td>
<td>1,110,816,041</td>
<td>1,155,986,011</td>
<td>0.96</td>
</tr>
<tr>
<td>ESPRESSO</td>
<td>2,826,804,443</td>
<td>2,930,860,108</td>
<td>0.97</td>
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<tr>
<td>LI</td>
<td>6,022,855,076</td>
<td>4,661,320,853</td>
<td>1.29</td>
</tr>
<tr>
<td>EQNTOTT</td>
<td>1,243,469,361</td>
<td>1,321,536,444</td>
<td>0.94</td>
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<td>INTEGER GEOMETRIC MEAN</td>
<td>1.03</td>
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<td>OVERALL GEOMETRIC MEAN</td>
<td>1.18</td>
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Among the overall dynamic instruction counts from running the 10 Spec benchmarks, the overall mean ratio (bottom right) shows MIPS executing 18 percent more instructions than Sparc.
ing-point benchmarks. However, MIPS has a single compare and branch instruction, while Spare uses one instruction to set condition codes and another to branch. This gives MIPS an advantage in the integer benchmarks.

Some differences relate to the importance the architects of the chips placed on the trade-offs in implementing operations in silicon as opposed to library routines. The MIPS processor, for example, has multiply and divide/remainder instructions, while the Spare chip does not. As a result, Spare incurs a penalty on these operations, averaging 19.8 instructions/call for integer multiply and 35 instructions/call for divide/remainder. Spare, on the other hand, has a floating-point square root instruction while MIPS does not. MIPS, in turn, pays a penalty averaging 62 instructions/call for floating-point square root. Fortunately for both processors, the Spec benchmarks are not heavy with these calls. The worst-case benchmark for Spare uses 1.47 percent of the instructions for integer multiply and 2.20 percent for divide/remainder. Conversely, the highest percentage of floating-point square root instructions required of the MIPS chip is 2 percent.

According to the study, the compilers and the library routines affect performance. But again, most of the differences measured are the result of conscious trade-offs, and the net results on overall performance tend to cancel out.

The raw instruction data gathered using the Spec benchmarks showed the MIPS processor executing 18 percent more user instructions than the Sparc. However, when Sparc's non-instruction events, such as load-use interlocks, are brought into the

<table>
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<th>BENCHMARK RATIOS</th>
<th>MIPS/SPARC RATIO</th>
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<tr>
<td></td>
<td>FLOATING-POINT</td>
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<tr>
<td>TOTAL</td>
<td>1.3</td>
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<tr>
<td>TOTAL+</td>
<td>1.25</td>
</tr>
<tr>
<td>TOTAL++</td>
<td>0.86</td>
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</tbody>
</table>

Three ratios measure instruction set usage between MIPS and Sparc using the Spec benchmarks. “Total” indicates raw counts of user-level instructions. “Total+” shows the ratio considering other delay factors, such as trap handling and load-use interlocks. “Total++” shows the estimated effect of adding hypothetical instructions to both architectures to even out differences in instructions.

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picture, the difference drops to 9 percent. Finally, the study team estimated the effects of adding hypothetical instructions to each chip to factor out all architectural differences. What if MIPS had a floating-point square root instruction and Spare had integer multiply and divide/remainder instructions, for example? In that case, the difference would narrow to 3 percent in favor of MIPS.

But since RISC means "reduced instruction set," the two processor architectures have made different choices in terms of limiting the size of their instruction sets. As Robert Novak, product marketing manager for MIPS' performance group, says, "If we were to do an instruction count comparison of a CISC machine, versus a RISC machine, a CISC machine would have many fewer instructions than a RISC machine—but many more cycles." So performance really can't be divorced from the relationship between instructions executed, the cycles per instruction and other architectural overhead.

Neither has significant edge

Because RISC relies on intelligent use of a smaller number of instructions than CISC, RISC is more dependent on compiler technology and on efficient library routines for performance. The Sun study concluded that the combined strengths and weaknesses of the two processors' library routines and compilers do not give either the MIPS or the Sparc processor a clear advantage. However, since the hardware architectures are likely to remain stable for some time, practical progress in reducing the number of instructions used will probably come from improvements in compiler technology and fine-tuning the library routines.

Pure processor performance cannot be judged solely on the basis of instruction counts. Architectural features not directly related to instructions can also affect performance. According to MIPS' Novak, the MIPS processor can, for example, simultaneously access data and instruction caches, while Sparc can not—an element that must surely affect performance. If Sun is going to concede that there are some factors other than instructions executed that affect performance, it must admit to all of them. And if the results of Sun's own study were so close, designers must look at factors beyond instruction utilization to draw their own conclusions.

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ASIC complexity fuels drive to HDL design

Spiralling gate counts and time-to-market pressures are making HDLs mandatory. Designers must choose the right HDL and integrate it into their design environment.

Mike Donlin
Senior Editor

As design tasks get more complex and ASICs routinely surpass the 20,000-gate level, it's impossible for an engineer to visualize a design without using a high-level description. In addition to this "can't see the ASIC for the gates" problem, time-to-market pressures will require simulation at the architectural level as time-consuming iterations of a design become unacceptable.

High-level languages in general and hardware description languages (HDLs) in particular will do for hardware designers what C, Pascal and Ada did for software developers—free them from thinking about the minutiae of a design and let them optimize its behavior.

Quite simply, the HDL revolution addresses two increasingly important issues: circuit complexity and designer productivity. "Companies just don't have a choice anymore," says Patrick Beauvillard, technical marketing manager at Cadence Design Systems (San Jose, CA). "Even if it were possible to design a complex ASIC at the gate level, statistics show that about half the time it won't work when interfaced to the rest of the system. It's imperative to simulate performance at a high level of abstraction. You need an HDL to do this."

More-productive designers

"Another critical benefit of HDLs is designer productivity," adds Venktesh Shukla, the open Verilog program manager at Cadence. "With traditional methods an engineer might be able to design 30 to 50 gates a day. With an HDL, productivity is more in the neighborhood of 200 gates a day. Does this mean a company will need fewer logic designers? I don't think so. There are plenty of other tasks, like exploring design efficiency and real estate requirements before implementation, that need to be addressed."

In addition to increasing productivity, HDLs also decrease the costly portions of the design cycle, namely the test and debug of complex circuits.
"What you have is a shift in how engineers use their time," says David Coelho, executive vice-president of strategic planning and business development at Vantage Analysis Systems (Fremont, CA). "In a typical bottom-up approach, a designer might spend 10 percent of his time doing high-level architectural planning, 40 percent on gate-level design and 50 percent on test and debug. In a top-down approach, that shifts to maybe 30 to 40 percent for design description, but only 30 to 40 percent in logic design and only 20 to 30 percent in test and debug. By simulating at the front end, you don't have as many penalties at the back end."

HDLS also give engineers an opportunity to generate test vectors at an early stage in the design cycle. Products such as Test Compiler from Synopsys and Test Design Expert from ExperTest (Mountain View, CA) generate test programs from VHDL descriptions. "We find that if an HDL description is being written for synthesis, it's very close to what we need for test generation," says Charlie Miller, vice-president of sales and marketing at ExperTest. "We can tweak a description like that in a day or so. If the code has been written for simulation purposes, however, it might take a little longer because there are structures in there that have nothing to do with the physical implementation of the device and which don't translate into test parameters."

Thinking in code

Even though the debate over whether to use an HDL is subsiding, there are other issues, such as which HDL to use and how to implement it into a company's design philosophy, that are just beginning. The real question that fuels these debates is simple—how does a company get design engineers who are used to thinking in graphical or schematic terms to think of a design as lines of code?

The transition to an HDL methodology is usually not as much of a problem for engineers who have recently graduated from schools where software is part of the curriculum as it can be for designers who simply haven't had to work with or think about software. The push to adopt HDLS is real, however, and even experienced engineers are being forced to learn new ways. The transition is not always easy. "I guess you could say that at the outset, some people aren't wildly enthusiastic," says Terry Coston, director of systems development at Harris Semiconductor (Melbourne, FL). "But if you look at the history of EDA, it's full of the same kind of painful transitions. In the '60s and '70s engineers were forced to use traditional design methodologies, while in the '80s they were forced to focus on wiring up gates. In the '90s they are being forced to use HDLs."

Traditional design methodologies force designers to focus on wiring up gates. The HDL approach permits designers to work at a higher level, where the function and behavior of a device is considered before committing the design to a specific architecture.

Considering a device's functions and behavior first has its advantages. "Take, for instance, someone who's designing an adder," says Cadence's Beauvillard. "If the device has been designed with a schematic editor and it's not fast enough, there aren't a lot of options for improving its performance. A designer might optimize the place and route and get a 10 to 15 percent speed improvement, but if that's not enough, either the design has to be thrown out or the slower speed has to be designed around. With an HDL, however, a designer can evaluate the architecture and choose the best one before committing it to gates."

Some engineers are approaching HDL design methodology by adopting traditional software methods. In his VHDL training seminars, Bill Billowich, president and CEO of the VHDL Consulting Group (Allentown, PA), encourages this approach, especially for students unfamiliar with software design. "Anytime you tell a hardware engineer to take a design and start coding, he's probably going to be intimidated," says Billowich. "So I think the best method is to train someone how to approach the job. If a hardware designer asked a software engineer how to approach a 10,000 line piece of software, he'd get some
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VHDL, Verilog and UDL/I: An example-driven comparison

VHDL, the IEEE- and ANSI-standard hardware description language, is increasingly used in the defense and commercial sectors of the electronics industry for digital design. Verilog, a proprietary HDL recently placed in the public domain, is widely used in North America and Europe. UDL/I is the emerging Japanese standard HDL. Why are there three commonly used HDLs? What differences do they have? What are the differences between them? When should the use of one language be favored over another?

To compare these three HDLs, we can look at an example worked in all three languages. The model is a clocked, serial-input, parallel-output, 8-bit shift register with asynchronous, active-low clear. To more easily understand the examples, the language keywords used in each model are in bold type.

The VHDL model shown is built around the draft IEEE-standard multivalued logic model. VHDL allows signals of arbitrary scalar or composite type; we'll use the IEEE's proposed nine-state model, which comprises two main elements: the entity interface and the architecture body.

The entity interface, beginning with "entity ShiftRegister" and ending with "end ShiftRegister," describes the model's interface to the universe. Here, the ports, or signals that pass information across this interface, are listed. Each port has a mode, or direction of data flow, and a type. Type "Bit" is a single-bit defined by VHDL that indicates the port's mode. "Std_logic" and "std_logic_vector" are the nine-state scalar and vector types, respectively, of the IEEE logic model.

There's also an assertion statement in the interface to check that the shift register is not simultaneously strobed at the same time.

The architecture body, beginning with "architecture Functional of Shift-Register is" and ending with "end Functional," describes the structure or behavior of the model. Models may have multiple architecture bodies per entity interface. In this way, a collection of architectures may represent different organizations or different design abstractions of a model.

The functionality of this shift register is described with three concurrent statements. The first (immediately after the "begin") in the architecture drives the outputs as a function of the internal state, "v." The second clears the internal state whenever clear is low, and the final statement implements the shift logic.

If both the second and third statements are simultaneously active, then "v" will have conflicting drives applied to it. The IEEE logic model specifies a resolution function to handle such cases; "v" will be set to all "X"s in this case. Note that both of these statements are simultaneously active precisely when the assertion condition is violated.

Together, an entity interface and one of its architecture bodies compose a complete model.

Verilog version

The Verilog version of this model uses the built-in data type for signals—Verilog does not give you the choice of using your own—and is organized in much the same way as the VHDL version. But since Verilog doesn't separate the interface and body of a model, this model is built as a single module. Moreover, Verilog has only relative (or scaled), and not absolute, delays. Hence, we specify that the delay scale factor chosen for this model is 1 ns per unit at the top of the model. Finally, Verilog's built-in resolution mechanism handles the case where both the final two always block drive "v" at the same time.

Like Verilog, the UDL/I version allows the use of only its built-in, four-valued data type for signals. Also, the bits are numbered from zero to seven, and not from one to eight as in the other two examples, because UDL/I requires bits be numbered from zero. Other than this difference, the UDL/I model is very similar to the Verilog model.

As illustrated by these examples, the
A Verilog example

```
module ShiftRegister (CLR, CLK, SH, LR, S1, S2, Q, Output);

input CLR, // asynchronous clear
     CLK, // shift clock
     SH, // shift enable
     LR, // shift direction
     S1, S2, // shift control
     Q; // serial input
output [1:8] Output; // parallel output

reg [1:8] v; // register’s internal storage

always @(posedge CLK)
    if (CLR == 0 && CLK == 1 && SH == 1) $display("Shift register simultaneously strobed and cleared");

assign #30 Output = v;

always @(CLR)
    if (CLR)
        #12 assign v = 0;
    else
        #12 deassign v;

always @(posedge CLK)
    begin
        if (CLK == 1 && SH == 1)
            case (LR, S1, S2)
                'b000: v = {Q, v[1:7]};
                'b001: v = {1'b0, v[1:7]};
                'b010: v = {1'b1, v[1:7]};
                'b011: v = {v[8], v[1:7]};
                'b100: v = {v[2:8], Q};
                'b101: v = {v[2:8], 1'b0};
                'b110: v = {v[2:8], 1'b1};
                'b111: v = {v[2:8], v[1]};
            endcase
        end
    end
endmodule
```

A UDL example

```
IDENT: Registers;
NAME: SHIFT_REGISTER;
LEVEL: CELL;
INPUTS: SH, "shift enable";
         LR, "shift direction";
         S1, S2, "shift control";
         Q; "serial input";
OUTPUTS: OUT<0:7>, "parallel output";
RESET_PIN: CLR; "asynchronous clear";
CLOCK: CLK; "shift clock";

ASSERTION_SECTION:
    ASSERT (^CLR) & RISE(.CLK) & SH
    ELSE PRINT ('Shift register simultaneously strobed and cleared');
END_ASSERT;
END_SECTION;

BEHAVIOR_SECTION:
    BEGIN
        REGISTER: v<0:7> DELAY 12NS;
        OUT := v DELAY 30NS;
        IF ^CLR THEN
            RESET(v);
        END_IF;
        V := IF .SH THEN
            AT .CLK DO
        CASE LR || S1 || S2 OF
            #300: V<6,
            #301: V<6,
            #302: V<6,
            #303: V<6;
            #304: V<6;
            #305: V<6;
            #306: V<6;
            #307: V<6;
        END_CASE
        END_DO
        END_IF;
    END_SECTION;
END;
```
HDLs

valuable advice. The issues are the same for both hardware and software engineers, namely ones of modularity, commentary, partitioning, and defining interfaces up front.”

Thinking in pictures

Because some engineers are reluctant to change their methods of thinking and because portions of a design may be best left to a graphical methodology, some EDA vendors are coming out with products that let designers use a combination of block diagrams and HDLs. A tool called Express VHDL from i-Logix (Burlington, MA) lets users create a visual model of system specifications through Activity-Charts, which show data and control flows hierarchically, along with the system’s processing capabilities. These Activity-Charts translate into Statecharts, which describe the dynamics of a system and show the control aspects of the system’s functions.

The charts identify all possible states and the transitions between them, while labels on the transitions indicate when and under what conditions each transition will take place. The tool uses Module-Charts to describe the hardware and software components of a system and their relationship to the elements identified in the previous two such high-level descriptions will not be as efficient as software written by a good designer. In addition, some people think a large design can’t be conceptualized at a graphical level.

“It’s hard to picture a state machine bubble diagram stretching beyond two pages,” says the VHDL Consulting Group’s Billowich. “It’s difficult to think of a large project that way because after a while you have to think of a design as a classic enumeration of states. By the time you get to page five or six of a graphical representation of a design, you don’t know where you are or what connects to what. This isn’t to say that a graphical entry for VHDL is a bad thing—you just have to be careful how you design it.”

Still, because engineers are accustomed to using graphical representations for design definition, EDA vendors are pursuing ways to make such tools available. Mentor Graphics (Wilsonville, OR), for instance, acquired high-level graphical description tools when it purchased Silicon Compiler Systems (SCS). According to Mentor, the AutoLogic and LogicLib tools from SCS let ASIC designers raise the level of their design specifications from gates and improve the efficiency of those designs without having to learn new design practices. With these tools, designers can express functions with building blocks. These blocks can represent over 50 synthesizable logic functions including adders, ALUs, comparators, counters, multipliers, tally blocks, and Wallace trees. Custom functions can also be developed by users. The synthesis side of the tool accepts these blocks as input, as well as NETED schematics, netlists, Boolean descriptions, PLA tables, and finite state machines.

The goals of HDLs

Regardless of how a design is entered, it’s only useful if it can be simulated, synthesized down to an actual product and accurately documented. Interestingly enough, the three main HDLs in use today, Verilog HDL, VHDL and UDL/I (Unified Design Language for Integrated Circuits), were all designed with one of these capabilities in mind.

Verilog HDL from Cadence was developed as a high-level language for use with the Verilog-XL simulator by Gateway Design Automation, a company that was acquired by Cadence in 1989. The Verilog family caught on with a number of ASIC vendors because of its excellent simulation capabilities. According to Cadence, Verilog HDL is currently the most widely used HDL in the industry with over 10,000 users. In addition to its high-level description and simulation capabilities, Verilog HDL is also supported as a synthesis language. Although highly regarded, Verilog carries neither the DOD stamp of approval nor IEEE standardization (VHDL has both). In a move designed to keep Verilog HDL alive as a competing force against VHDL, Cadence opened the language as public domain software in May of 1990.

VHDL was designed for the U.S. government by Intermetrics (Cambridge, MA) to provide a standard way to document designs. Because VHDL provides a standard simula-
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SOLUTIONS

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Just starting to use language-based
Japan Electronic Industry Develop-
ment input language, it's supported
by most major CAE vendors' simu-
lators. Several companies, among
them Synopsys, Racal-Redac (West-
ford, MA) and Viewlogic, support
VHDL as a synthesis language. The
fast-growing acceptance of VHDL,
however, probably stems more from
DOD support and the IEEE en-
dorsement rather than its ease of
use or popularity. Many users feel
that because VHDL has so many
features and capabilities, it's diffi-
cult to use.

"VHDL was developed by soft-
ware designers," says James Vel-
lenga, manager of design represen-
tation at Racal-Redac. "I remember
in the '80s looking at some of the
original proposals for VHDL and
thinking that it wasn't being de-
signed for hardware designers; it
was being written for software de-
signers who didn't understand the
issues of synthesis and implementa-
tion. Restricting it would make it
more usable. People don't want 47
different ways of expressing some-
thing—it confuses them."

The most recent contender in the
HDL arena, UD/LI, is being de-
veloped by the Software Development
Committee, an organization of Ja-
panese electronics firms and the
Japan Electronic Industry Develop-
ment Association. Based on Nippon
Telephone and Telegraph's internal
HDL, UD/LI is primarily targeted to
drive register transfer level (RTL)
synthesis tools. Though the fact that
it's being designed to support syn-
thesis is attractive, the large market
share of Verilog HDL and the stan-
ardization efforts behind VHDL are
causing most EDA vendors to
take a wait-and-see attitude about
UD/LI.

HDLs for programmable logic
Most companies that support VHDL
and Verilog view these languages as
a way to design large ASICs and
even larger systems. But there are
other HDLs that are targeted to pro-
grammable devices such as PALs,
PLDs and field-programmable gate
arrays (FPGAs), and these are often
an entry point for engineers who are
just starting to use language-based
designs. Companies such as Data
I/O (Redmond, WA) and Mine
(Colorado Springs, CO) offer HDLs
that support the development of pro-
grammable devices. Because these
languages aren't intended for large
system designs, they're simpler to
use and don't need the complicated
simulation and synthesis constructs
of other HDLs because their target
devices can be programmed, tested
and reworked in a matter of
minutes.

"Our Abel language is designed to
work at the behavioral level," says
David Kohlmeier, division engineer-
ing manager for the design software
business unit at Data I/O. "We don't
get into structural issues such as
data paths. We can go from a de-
scription to a device, whereas VHDL
and Verilog produce generic netlists
and then need synthesis to get to a
particular part."

Even though these programmable
logic languages provide a migration
path for engineers to move from tra-
ditional methods of design entry to
HDLs for ASIC design, most vendors
of these tools and languages agree
that they will someday move into
VHDL either as a subset or by pro-
viding hooks for file input and out-
put. In fact, Viewlogic's VHDL syn-
thesis translates from RTL
descriptions to FPGA part formats.
According to Mine vice-president
Kevin Bush, "In the long term, we'll
end up with some form of VHDL in
our tools. When you have companies
like Mentor and Valid incorporating
VHDL into the suite of tools of which
you're a part, it's pretty hard to stay
on the sidelines."

Analog designs are one of the last
frontiers that need an HDL stand-
ard. Work on an analog HDL
(AHSL) standard is in its infancy,
with the IEEE SCC30 committee
looking into it as a language or an
extension of VHDL. One of the pro-
posals the IEEE committee is con-
sidering is the Mast AHDL from
Analogy (Beaverton, OR). Designed
for use with Analogy's Saber simu-
lator, Mast can be used to write mod-
els for circuit-level devices, such as
transistors and diodes, up to sys-
tem-level boxes, such as control
functions and differential equations.
Saber can then simulate these ana-
log parts, as well as ASICs, digital
components, lasers, motors, and
control systems. HDLs, whether graphical, textual
or some combination of the two, will
undoubtedly be a primary force in
the designs of the '90s. "Let's face it,"
says Dick Albright, director of mar-
keting for CAE products at Valid
Logic Systems (San Jose, CA). "If
you can keep a designer working at a
high level, you're going to increase
productivity. If I have a language, a
simulator and a synthesis tool, I
don't want my engineers wasting
their time laying gates out on a sche-
matic. To be competitive you simply
have to move to a higher level of
abstraction."
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<td>ST16C552</td>
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<td>4 UARTS with FIFO for VME-BUS</td>
<td>68 PLCC</td>
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CIRCLE NO. 55
Object-oriented tools expand the repertoire of real-time developers

Object-oriented programming eases problems caused by program size and complexity, and its benefits are coming to real-time applications.

Tom Williams
Senior Editor

Object-oriented software technology has become one of the major concerns of the computer industry for the ’90s. The hoped-for benefits of object orientation have spawned a huge amount of activity in the design of object-oriented languages, database systems, programming environments, and third-party support products. It has also raised a number of “cultural” issues that revolve around the way programmers do their work and how they must adapt to an object-oriented discipline.

The advantages offered by products and technology available today are causing many organizations to make a commitment to object orientation. Among these benefits are reusability of code, the ability to manage increasingly complex applications, and the ability to more easily extend and modify existing software products. And the benefits appear to apply to all ranges of applications. “The techniques really apply to any type of application that you’re creating and are almost independent of the language you’re using,” says Zack Urlocker, Turbo Pascal product manager for Borland International (Scotts Valley, CA).

David Hoffman, president of TeamOne Systems (Sunnyvale, CA), makers of the TeamNet product, which comprises software for development project management in CASE, CAD/CAM and CAE disciplines, says that object-oriented technology is especially appropriate for the engineering field because “one is dealing with objects such as circuits, ICs, software modules, and the like. And one needs to deal with these objects in a way that’s manageable.” He says that rather than having the behavior of objects that are known to the entire monolithic system, it’s easier to partition their behavior within the objects themselves, “because then you can reuse components more easily and the system is more scalable. You can evolve the system more easily.”

These observations touch on just some of the more formally defined characteristics that make object-oriented technology attractive. First, the idea of objects with attributes is not new. Integrated Systems (Santa Clara,
I OBJECT-ORIENTED PROGRAMMING

CA), a vendor of control engineering design software, developed a product called SystemBuild with which the user puts together control blocks in a hierarchy of functions and assigns behavior to design control systems. But it was possible to represent such an environment without using object-oriented programming internally. Michel Floyd, manager, CAE product development, at Integrated Systems, notes that the complexity of the product and customer demands for enhancements are forcing the company to make the "internal representation of its products object-oriented."

The move to object-oriented representation in the internals is seen as critical to both the development of new applications and the maintenance of existing products. "We found we just couldn't deliver what the customers were asking for in a timely manner," Floyd says. "We were constrained by the framework we had built for ourselves."

Languages and tools

Perhaps the most striking difference between modern structured languages and object-oriented programming is in the approach to constructing code. In languages such as Pascal and C, there's a relatively small list of reserved words and syntax rules out of which the programmer can construct enormously elaborate programs. In pure object-oriented programming, these words and syntax rules are encapsulated within a large number of "classes" of objects. A class describes a set of objects with similar characteristics.

An object is an "instance" of a class with an actual state (data) that can be acted on by the methods of that class. Programmers construct code by browsing the class library and selecting those objects that will do what the programmers want. Encapsulation also means the programmer can try out the objects' behavior on the spot to see if they are what the programmer really wants before including them in the program.

The two currently most popular languages for object-oriented programming, Smalltalk and C++, reflect this different approach to programming. Smalltalk is more than a language; it's a programming system. The user is forced to work within the object-oriented framework of browsing the class library, selecting objects, trying them out, and building them into the program. In C++, the programmer could choose to program entirely in standard C if desired, or to select only those objects the programmer wished to build into the code. While arguments can be made for the sink-or-swim method of Smalltalk, C++ is the most widely used language simply because of the vast number of trained C programmers in the world.

Objects in real time

For object-oriented development of embedded and real-time systems, C++ is clearly in the lead because it's compiled completely to object code. Smalltalk, on the other hand, uses a byte-code interpreter and until recently only came in versions that were integrated with the rest of the programming environment, such as browser, editor and debugger. The interpreted nature of Smalltalk has led to the conclusion that it must be slow, and in traditional computer architectures that has been the case.

Advantages of objects

The advantages of objects can be largely described by three words: encapsulation, inheritance and polymorphism. Encapsulation means that an object contains both a state and the operations that can be performed on that state. Actions on an object's state, called methods, are initiated by messages sent to the object. With encapsulation the user really need not worry about how an object performs its function but simply what it can and cannot do. Users can be confident that adding an object to existing code will not cause unpredictable things to happen to other parts of the program.

Inheritance is the ability to associate characteristics common to all members of a class of objects, lead, gold and iron, for example, all have the characteristics of metal. In object-oriented programming, subclasses of objects can inherit characteristics of the class they belong to. Drawing a square or a triangle uses methods inherited from the method of drawing a polygon. Different types of triangles inherit characteristics from the general class of triangle, such as having three sides.

Polymorphism means that an operation to be performed on an object is determined by the type of object it addresses. The same command to edit the drawing of an IC, for example, would act differently when applied to the drawing of a printed circuit board because the characteristics of the two objects are different as are the internal methods that act on them. But the programmer, as well as the user, need only deal with the concept of "edit." The ability to generalize behavior over many types of objects allows a higher degree of abstraction in software design since the programmer only has to think about specifying actions rather than the details of how to implement them.
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**CPU-40 PERFORMANCE CHARACTERISTICS**

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CIRCLE NO. 56
**OBJECT-ORIENTED PROGRAMMING**

On a modern RISC processor such as the Motorola MC88000, however, the entire byte-code interpreter and the Smalltalk virtual machine, which consists of about 100 byte codes or Smalltalk instructions, can run out of the on-chip cache.

Running the interpreter in the cache means that fetches from memory are a relatively small number of high-level instructions that generate greater numbers of machine code instructions out of the cache. That machine code runs much faster when it emanates directly from the cache than if it had been fetched from memory as normal compiled code would be. "That's going to make us rethink some previous assumptions about interpreted languages and speed," says Dan Goldman, vice-president general manager of marketing and advertising at Digitalk (Los Angeles, CA), publishers of the leading version of Smalltalk.

But speed isn't the only requirement for real time; preemptability and predictability are also essential. One characteristic of Smalltalk that has inhibited its acceptance for such applications is its automatic garbage collection facility. The danger is that the program might be garbage collecting—searching memory for program or data segments that are no longer active and reclaiming the unused memory blocks—when a critical interrupt could occur.

Recently, however, Object Technology International (Ottawa, Ontario) has modified Smalltalk/V in a licensing agreement with Digitalk for embedded applications. Embedded Smalltalk/V is available for the Motorola MC680X0 family of processors and also in versions that will run on top of commercial real-time executives such as VRTX by Ready Systems and VxWorks by Wind River Systems. Object Technology International (OTI) also provides a configuration control environment called Envy/Developer that has, among other things, a packaging facility, which can separate the execution material mix system—discrete process objects are arranged in a hierarchy such that each subordinate process reports conditions upward to its supervisor process and receives events from its subordinates. It can also send messages down to subordinates to cause them to change to a desired state. The highest priority is assigned to the lowest level of the hierarchy, the I/O.

In an application based on Forth's Event Control Management System—here a garbage collection facility, however, is not yet fully predictable. John Duimovich, manager of embedded systems at OTI, says the garbage collector has been built to "average out the pain of garbage collection on a workstation." The scavenger routine interrupts for about 0.001 seconds every 10 seconds. "However," he notes, "the best garbage collection techniques are not used for hard real-time yet ... where it's a predictable, schedulable action. Currently we don't have one of those, but it's a high priority for us."

Still, a great deal can be done in embedded control that does not need submicrosecond response times.

**Factory control systems**

A system for constructing modular factory control systems built on the object-oriented concept is the Event Control Management System (ECMS) by Forth (Manhattan Beach, CA). ECMS is based on software objects called processes and receptors. A control system can be constructed by assembling processes and receptors into a hierarchy in which a process receives input from a subordinate process, acts on that input and sends messages back down to its subordinate and/or reports its new state to its supervisory process.

A process can be thought of as a state engine that contains a state (data) and one or more actions (methods, in object-oriented terminology) that it can perform on that state. The actions it performs internally can cause its state to change to one or more different, defined states. A receptor is an object that is generally used for communication between processes and between processes and I/O. Receptors provide a means of bringing an event—such as the change in state of a digital point—to a process. Each higher level in the hierarchy allows a greater degree of abstraction in describing the system.

Interestingly, the lowest levels in the ECMS hierarchy, starting with the I/O level, have the highest priority. This means that in terms of levels of priority, the lower-level processes are handled before the higher-level ones. The entire hierarchy of processes is coordinated by an executive task running under Forth's pF/x real-time operating system.

**Databases aid design systems**

Complex data structures that don't lend themselves to the traditional relational database tools are typically found in applications such as engineering design and CASE, says Ian Schmidt, director of product marketing at Object Design (Burlington, MA), which produces ObjectStore, an object-oriented database system. One way design applications differ from general business applications is that they use...
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OBJECT-ORIENTED PROGRAMMING

Industry group working toward standards for object-oriented programming

To bring object technology into the mainstream, the industry must agree to cooperate. The Object Management Group (OMG) was founded in April 1989 to establish a framework for object technology supported by detailed and widely available interface specification. From just 9 initial members, the group has grown to more than 110 members representing over 80 percent of the companies pursuing object technology development. A nonprofit corporation, the OMG is headquartered in Framingham, MA with marketing offices in Boulder, CO. The OMG welcomes participation by both users and developers of object technology.

The Object Management Architecture (OMA) Guide, released in October 1990, was the first product of the group’s efforts. The OMA Guide contains the architecture for an object-oriented environment along with a glossary of terms to standardize the terminology used to describe object technology. The architecture forms the foundation for the OMG’s work. From this the group will adopt interface specifications that will let developers build products that fit into an integrated environment constructed from products offered by many vendors.

The architecture gives a framework for an object-oriented environment. The key elements are applications, shared facilities, common services, and the object request broker. Currently the OMG is working to adopt interface specifications that will support the passing of messages across an object-oriented environment. After the architecture, the most important element was deemed to be the ability to establish communications among the objects in an object-oriented environment.

The OMG’s work plan extends over the next two years. In that time the group will adopt interface specifications, based upon commercially available products, for applications interfaces, database interfaces and other specifications to support the adopted reference architecture. The group has recently issued a Request for Information for an object model, which is a formal description of the allowable behavior and visible characteristics of objects within an object environment. Once completed, the object model will act as a bridge for the many proprietary object models being developed.

In order for object technology to be widely and quickly adopted, it must adhere to a nonproprietary architecture with widely available interface specifications. This will create a market condition where both users and developers can buy and build products, confident in the ability of those products to communicate.

Chris Stone, president, Object Management Group

the concept of things being derived from other things. One creates something and then modifies it—but may wish to save the original version. Or, one takes an existing object and modifies that, creating different versions, or instances. A vast number of objects in engineering are represented as aggregations of parts or levels of detail or a combination of both. And the inheritance and encapsulation characteristics of object-oriented software technology fit such a means of representation naturally.

Schmidt also notes a particularly good fit between object-oriented languages and the kinds of entities that are stored in an object-oriented database, and that there are very few sophisticated applications that have a CAD or design flavor to them that aren’t being written in C++. “C++ is attractive because it almost has the capability within it for people to design their own language,” he says.

Users design their own classes and types starting with some basic given classes and then making modifications. Thanks to the property of inheritance, new instances of an object that a user creates can reuse the code of that class; the user changes or adds only those attributes that make the new object unique. “The beauty of this,” says Schmidt, “is that there’s a long start-up time to define your base classes. But you find that as you’re defining classes for your application, you keep borrowing from stuff that already exists, and before long, you’re writing less and less code.”

With encapsulation the user need not worry about how an object performs its function but simply what it can and cannot do.

Not only do new classes inherit the characteristics of previously defined classes, but it’s also possible to build in the characteristic behavior (methods) of the data objects. Because the behavior is built into the object, the user need not worry about the details of handling any given object since that object knows how to respond to messages it receives. “C++ gives you an incredible data modeling tool,” says Schmidt.

“You can treat the class ‘elephant’ the same as the class ‘integer’ (for example, store, delete, edit) because the language knows about all the things ‘elephant’ can do and how.”

And this is where the object-oriented language begins to overlap with the object-oriented database. Since both work with objects, and since objects are the same thing in both language and database—namely data and the methods to operate on that data—one can refer to objects in the database the same as if they were parts of the language. This is an essential feature for those who wish to use object-oriented databases in large design environments.

A user’s move to objects

Valid Logic Systems (San Jose, CA) has incorporated an object-oriented database in its newest product, called Design Manager. Design Manager fits into Valid’s Framework
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design environment and is a universal storage mechanism for managing data and the output of Valid tools. "You want to combine an object-oriented programming language with an object-oriented database and see how well you can map C++ classes into the database," says product manager Larry Rice.

The idea is that one can model all the types of data one wants to store in the system, and the database can accept them just the way they were modeled by the programming language. With a relational database, the programmer almost has to unravel the structure to deal with it and store it. As Object Design's Schmidt puts it, "That's almost like taking your car apart at night before you put it in the garage." ObjectStore, on the other hand, maintains the class hierarchy of stored objects. The database is retrieved in virtual memory, so that if a desired object is not in physical program memory, it's brought in from disk. This gives developers a "single-level store" of objects.

Object Design's ObjectStore database uses a virtual memory mapping architecture that can preserve the inheritance relationship of data objects. If an object is not in physical program memory, it's brought in from disk. This gives developers a "single-level store" of objects.

Making the move mentally

"Some people believe it (object-orientation) is the same old thing in new packaging," says Jeff McKenna, founder of McKenna Consulting Group (Portland, OR). "I don't happen to believe that. It's a fundamentally new way of thinking about software." Adopting an object-oriented programming discipline means changing some basic ways of thinking for an individual, and so it can entail some wrenching changes for an organization. And it must be remembered: in today's industry, programming is not an individual activity; it's an organizational activity that requires planning, coordination, communication, and management.

"Shifting to an object-oriented environment isn't worth it if the user's fundamental approach to programming isn't changed as well," says McKenna. "It's a lot of effort; there's a learning curve that takes about six months." But he cautions that while making the change isn't worth the trouble from the point of view of individual productivity, "it's worth it from the point of view of the reuse of software in the long term." So as an organization moves into an object-oriented mode, it will create objects tailored to its application needs that can be reused and shared among other members of the organization. Eventually, it will amass an inventory of commercially acquired and custom-designed—or derived—software components.

Increasingly, the programmer's job will entail finding the right component (object) for the job by browsing class libraries—much like hardware engineers perusing their Texas Instruments or Motorola data books. McKenna says that software engineering is going to have to change to where programmers are told, "What you read is more important than what you write." Finding the right objects and figuring out how to use them to build solutions will be the major activity.

But the cultural burden is not just on programmers. "Managers are rewarding programmers for writing code, so it's not in the programmer's interest to find an object that he can use because it doesn't add to his line count," says McKenna. So there has to be a way to reward programmers for delivering solutions to problems rather than grinding out and debugging code.

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Real-Time, On Time, All the Time!
Will monolithic or multichip processors win the performance race?

Alex Mendelsohn
Contributing Editor

The era of the million-transistor microprocessor is upon us. "Megachip" blockbusters—some executing 100 Mips or more—are becoming available in both RISC and CISC designs.

Semiconductor makers continue to refine and redefine the microprocessor, conceiving increasingly sophisticated architectures on multimillion-transistor chips. Other processor architects are opting for the increased design flexibility and higher manufacturing yields of multichip processor designs. Which camp is right? More important, can either stake a clear claim to the high end of the performance spectrum? Will the fastest processors be megatransistor monoliths or multichip devices?

One key for processor architects in the monolithic camp has been the ability to keep faster transistors productively used in VLSI. Transistor-rich logic blocks now let processors schedule multiple activities per clock cycle, creating parallelism at the chip level. And optimizing compilers, able to extract parallelism from source code, are getting better.

At the same time, the clock speed of processors is increasing. Even 8- and 16-bit single-chip microcomputers of conventional architecture now routinely run with 25- and 30-MHz clocks. Speeds over 25 MHz mean that system designers must be especially wary of potential performance penalties due to physical layout. While this would seem to favor integrating all critical functions on a single chip to minimize physical separation, the need to eventually access things off-chip keeps system layout effects a major consideration for monolithic architects.

IC makers are touting highly integrated CISC and RISC ICs and compilers. The recent superscalar, superpipelined debate has seen vendors announcing a spectrum of hardware/software architectures.

Partitioning is key

In the face of multiple unique architectures, partitioning is emerging as an issue. IC vendors extol VLSI—even ULSI—chips that integrate many systems-level features. But there's growing evidence that some of the largest, most-integrated silicon devices eventually may be constrained by packaging limitations and wind up in some sort of "micro-card cage" module. Texas Instruments, for example, is now experimenting with silicon "backplanes" and "plug-in" dice.

Some argue that well-partitioned silicon will become essential as the integration revolution continues. Many of the arguments in the partitioning camp make good engineering sense, especially from a cost-versus-performance point of view.

"The partitioning controversy is based on arguments between people who relate to instruction set architecture development in silicon versus those who have to write compilers and operating systems," says Phil Hester, director of IBM's Engineering Center for Advanced Workstations (Austin, TX). "It's a delicate balancing act.

Silicon or software?

"The compiler folks ask what silicon does at execution time versus what a compiler does at compile time," he says. "With today's multiple execution unit designs, some people believe it's efficient to move things such as handling responsibility away from silicon and into a compiler. Others feel it's better to add such functions to the hardware.

"Silicon is very precious to semiconductor makers, especially merchant market vendors," he says. "They want to reduce die size. So, they move functions to a compiler for things such as interlocking multiple execution units."

IBM's RS/6000 multichip design embraces the hardware approach, thanks to excellent compilers and well-developed and available fabrication processes. "We don't rely on software," Hester says. "We keep interlock handling on-chip because with our fab process we pay a minimum penalty in terms of silicon area.
and cycle time/clock rates. And we build a set of efficient compilers for a number of languages without having to tie specific implementation details to the compiler.

"It's true that the simpler you make a chip, the easier it is to prove that it works correctly. The more special cases a chip has to handle, the more design validation you have to perform, especially simulating gate level descriptions to convince yourself it'll work as designed."

A critical capability for IBM resides in its IC validation technology. "If you have hardware simulation engines that let you run a few hundred million simulation cycles per week, you'll come to different conclusions about partitioning issues than if you have to let simulations run for months," Hester says. "Testability is at issue too. If you have sophisticated validation tools, time-to-release-to-manufacturing penalties for IC makers are reduced."

Partitioning choices

Nathan Brookwood, marketing director for Intergraph (Palo Alto, CA), acknowledges IBM's leadership. "The fastest machine today, the IBM RS/6000, using a multichip CPU design, proves there really are multiple schools of thought about architecture and partitioning," he
says, "We eschew the semiconductor macho mentality in our Clipper chip set to get the highest possible performance consistent with reasonable cost."

Intergraph's Advanced Processor Division's latest Clipper (there have been three Clipper "compute engines" since 1985) is enjoying popularity in the company's RISC-based CAE products. The system makes use of minimal cache and offers moderately powerful floating-point ability.

Intergraph's approach relies on efficient partitioning, low-voltage logic, advanced packaging, and multichip modules (MCMs). The company's reason for using MCMs is multifaceted. Its chip set designers dropped logic operating voltage to 1 V instead of the more typical 5-V TTL or even 3.3- or 3.6-V levels. Of course, there were compromises. The Clipper chips require two voltages—5 V for internal logic, along with a reference signal, and 1 V for I/O signals. "But, as we lowered logic levels, we got away from using conventional or multilayer circuit boards and got onto a better surface in MCMs," says Brookwood. "Raw dice are bonded directly to chips rather than having packages placed on a board. MCMs give us control over parasitic capacitance and inductance."

Hybrid-like packages, eliminating long conductors between dice and packages, let Intergraph realize 1- or 2-ns off-chip delays. "It's almost as good as the on-chip prop delays people tout," Brookwood says. "With low-voltage logic and MCMs, you don't have to drive nearly as much capacitance."

Intergraph says wire-bonding techniques have dramatically improved over the past few years. Assembly yields and reliability are exceptional. "We don't sacrifice anything," Brookwood says.

MCM performance data from Texas Instruments (Dallas, TX) supports Intergraph's findings. TI's customized MCMs, based on molded modules using ceramic substrates, typically result in cost reductions from 2 times to as much as 10 times at the systems level.

TI found that stress, moisture and thermal sensitivity fell by 3 to 8 times with MCMs. Lead length reductions of 6 times resulted in inductance reductions of 60 times, with load capacitance lowered by 6 times. Critical path delays with MCMs were typically reduced by a factor of three, say TI engineers.

"The argument for large-scale integration is it eliminates interchip propagation delays like you have with multichip designs," says Intergraph's Brookwood. "But, megachips fundamentally constrain the hardware you can use in a system. Megachip vendors force architectural compromise. They want to put more and more on a single chip. If they leave things off, they create opportunities for competitors to provide functionality. They would rather not do that."

"And, when it comes to testing, with off-chip cache it's easy for a logic analyzer to trace program execution. With on-chip cache, you can't do that. The more highly integrated, the more difficult it is to know what's going on within the chip unless you want to pay a penalty in silicon real estate for diagnostics."

Transistor-bound caches

Another problem for monolithic processor architects is transistor cost of caches. "Many highly integrated chips typically have only 1-, 2- or 4-kbyte caches, which prove not nearly large enough," says Brookwood. "People will discover that they'll really need much bigger caches of 16 or even 64 kbytes."

IBM's Hester agrees. "If I had future submicron technology, I'd allocate more of the multimillion device budget on much larger caches to get the off-chip bandwidth requirements down. Then you'd see dramatically better single-chip RISC than single-chip CISC."

"Regardless of RISC or CISC, with single-chip technology, you're bandwidth limited getting in and out of a chip to main memory because of cache size limitations," Hester says. "That's why IBM chose multichips. We simply can't put enough devices on one chip today. We have separate chips for instruction and data caches. And separate ICs for the execution units for fixed point, floating point and branching."

Like Intergraph, IBM defined its own interchip logic for its fastest platforms. The highest-performance IBM RS/6000, the 41-MHz Model 550, with 0.5-µm effective gate length ICs, uses 3.6-V logic.

The big win: chip costs

Multichip proponents point to economics as a big factor. Wafer yields are key. Getting a big chip to yield acceptably, from an economic viewpoint, has always been recognized as difficult. In fact, most semiconduc-

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The economics of megachips

Intergraph's Clipper microprocessor uses superscalar dispatch and deep floating-point pipelines. Several moderately sized dice ensure worthwhile production yields and low program risk. In a paper delivered at Compucon recently, Intergraph's Howard Sachs, vice-president and general manager of the Advanced Processor Division, and Harlan McGhan, manager of analysis and application, make a case for multiple-chip microprocessors.

In their presentation, Sachs and McGhan note that a "pure" superpipelined microprocessor, able to operate in CMOS at speeds in excess of 100 MHz, would require an exotic and expensive memory subsystem. The other alternative is to implement large on-chip caches that require large die areas and consequently carry severe economic penalties.

The largest die feasible today typically supports only a relatively small cache (perhaps 8 kbytes or so). This means it's still necessary to construct off-chip secondary cache. The resulting multiple paths to and from memory for multiple load/store pipes become expensive and I/O-pin intensive. Required elaborate decode circuitry also tends to slow down overall processing.

4.5-million-transistor caches

The superfast Clipper microprocessor therefore relies on unpackaged die mounted in multichip modules. Purely on the grounds of cost-effectiveness, say the authors, it makes sense to implement microprocessors as a set of two or more moderately sized chips.

They cite the IBM RS/6000 as an example. It partitions 7 million transistors over nine chips. Of these, 4.5 million are expended just for cache. The accompanying graph illustrates a possible cost-versus-performance trade-off.

Given information about defect density ratios taken from a learning curve (see graph), it's possible to calculate \( Y \), the effective yield.

\[ Y = e^{-AD} \]

where \( A \) = area in \( \text{cm}^2 \) and \( D \) = defect density (number of defects/cm\(^2\)).

Applying this formula to the column for 2-cm\(^2\) die, the large area die generates just 70 candidates on a 6-in. wafer versus 146 on a 1-cm\(^2\) die. Assume the first year of production that the defect ratio is the typical maximum for a new process of 1.5 defects/cm\(^2\). Then, on average, just 3 of the 70 candidates will be good.

As the defect ratio drops in time, the number of good dice rises accordingly.

During the second year of production, at a ratio of 1 defect/cm\(^2\), yield triples to 9 good die. During the third year and beyond, when the defect ratio bottoms out at 0.5, yield nearly triples again to around 26 good die.

From this analysis a calculation of the cost of working silicon can be derived. Assume that a 6-in. wafer must bring $3,500 in revenue (including packaging). In the first year of making 2-cm\(^2\) die, the cost of working silicon is nearly $1,200. This drops to $389, and ultimately to $135.

Assume one of these "super" chips would be used in a system, and 100,000 systems a year would be sold over a period of three years. Total silicon costs would add up to $169 million.

Compare that with $42 million for the same period, but using two 1-cm\(^2\) die with exactly the same silicon area. There's a real savings of $127 million. It's four times as expensive to implement a microprocessor as a single megachip than as two smaller chips.

Of course, this simple "level sales" model can be accused of exaggerating tor vendors, when asked, are reluctant to talk about the subject, and are even more hesitant to provide metrics. "Things like megachips often happen more because they're possible than because they're sensible," says Howard Sachs, vice-president and general manager of Intergraph's Advanced Processor Division.

Intergraph's numbers show that monolithic designs with everything squeezed onto one chip push the practical limits of chip size. "Off-the-shelf processing equipment won't let you deal with chips larger than 2 cm\(^2\)," says Brookwood. "Mask repair and reticle size limitations pose manufacturing limits. We deal with world-class foundries, but the bigger the chip, the lower the yield. Regardless of vendor, yield goes down exponentially with area. From an economic standpoint, it makes a lot of sense to use multiple smaller ICs."

Intergraph's analysis point to the use of two small dice instead of one large one with equivalent area (see "The economics of megachips," above).

104 MAY 1, 1991 COMPUTER DESIGN
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CIRCLE NO. 25
FAST PROCESSORS

This photomicrograph of Motorola's existing 88200 RISC cache memory management chip illustrates vast expenditures of silicon real estate consumed by relatively small SRAM caches. Future higher-density devices will obviate the need to go off-chip for larger caches.

"Single-chip designers recognize the need for on-chip cache located near integer units (IUs)," says Brookwood, "but fast cache is tough to design. In a 33-MHz MIPS Computer Systems R3000, you need a 66-MHz cache. If you put it on-chip, how does the floating-point unit act with the cache?"

"Caches and FPUs are very consumptive of real estate. There's no middle ground where you can easily marry an IU and cache and still have a separate FPU. You can do it, but you lose performance." Not all RISC vendors agree. "Fast IEEE FPUs are something that RISCs have over CISC designs," says Martin Booth, senior product marketing engineer for RISC processor products at Fujitsu Microelectronics (San Jose, CA). "It's a function not only of the FPU definition but also of the interface between the IU and the FPU. A lot of design is moving toward integrating both on the same chip die. We do both with about 255,000 transistors."

Still, Brookwood contends that partitioning is better, emphasizing that interchip delays are not a problem at 1991 real-world silicon clock rates. "Our 50-MHz pipelined architecture requires an extra stage in the pipeline, but once the pipeline is filled, prop delay is not significant to throughput," he says.

Beyond 50 MHz

Will prop delays be more critical when ICs roll out of fab with transistors toggling at 100 MHz? "They might be," Brookwood says, "but calculations show that a single-chip 100-MHz design would only give a 10 percent better performance spec than a multichip design that would run at 90 MHz because of the interconnects. If you save 35 or 40 percent in cost, the 10 percent performance sacrifice figure isn't that significant. At 50 MHz, there's no trade-off."

But what about merchant market superfast products? It's one thing to be a captive supplier like Intergraph, and quite another if your silicon is fueling the vast commercial marketplace.

"We're driven by the need to deliver between a quarter and a half million 68040s in 1991. There's no right or wrong philosophy about partitioning," says Jim Reinhart, manager, M68000 marketing and applications at Motorola (Austin, TX). "It depends on what you're driven by."

Megachip technologies and partitioning are recognized as interrelated at Motorola. "Both factors play a strong role in one's thinking about the future," says Reinhart.

Cultural preference

"Motorola has a goal—call it a requirement—for future generations, including the 68040," Reinhart says. "It's to focus on single-chip designs. Everything has to be on one chip, from where you process the simplest integer instructions to where you get your main memory interface."

"Driven by the market, we believe customers must have such devices to help them build cost-effective systems. They must deliver competitive performance without having to resort to large external caches or other things that tend to dramatically increase systems cost and reduce performance by going off-chip. The fastest transistors and buses must be on-chip. Mainstream performance levels must be achieved with low-cost DRAM. Sixteen-way interleaving or large external static caches don't play into this definition."

"Sophisticated memory controllers are key, not just the size of caches. Memory controllers are measured by how well you handle cache hit-and-miss cases, as well as how well a processor handles a very complex set of memory events."

"Although much progress has been made with MCMs, I'd be surprised if you could come anywhere near the volume, cost and quality of what we're doing. MCMs do provide excellent results, but they're really much more suitable for lower-volume applications."

"Testability is also a mixed bag," Reinhart says. "We don't find MCMs more testable than monolithics. In fact, we have military customers who use MCMs; we sell them dice. For them, a big problem is final testing. We can do a much more thorough job when a chip is packaged than at die probe. We can test at a higher frequency. Wafer probes won't let us drive a 68040 die at 25 MHz under..."
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FAST PROCESSORS

thermal and electrical stress. There's too much inductance in probe fixtures."

But, systems flexibility still means multichip designs, some argue. For that reason, Hewlett-Packard (Cupertino, CA) used partitioned silicon rather than monolithic megachips in its Precision Architecture (PA) RISC. Forthcoming PA machines include 90-MHz CMOS five-stage pipelined CPUs that HP engineers anticipate will vie with competitive ECL implementations.

PA RISCs compete in both workstation and commercial markets based on adaptability. HP says its approach to superfast processing encompasses unanticipated demands. HP claims performance can be more readily scaled with cost by varying clock speed and cache parameters, which is made easier by partitioning.

Based largely on standard-cell control blocks, library-based data paths and PLAs, HP's fully static design avoids large on-chip caches. Claiming large caches display unacceptably high miss ratios when running the large benchmarks simulating multiprocessor workloads, PA relies on instruction store buffers that act like small associative caches.

Off-chip propagation delays between PA chips are shortened by low-voltage (3.3 V) drivers and controlled impedance signal buses plus low inductance power and ground lines. Machine cycle times are closely matched to typical SRAM cycle times, with unused cache cycles used to write specially buffered data to off-chip SRAM caches.

Partitioning for transputers

Different vendors use different partitioning approaches to extract benefits from VLSI. The Inmos transputer family from SGS-Thomson (Colorado Springs, CO), for example, has always used partitioning as a route to scalability. Transputer users describe the bounds of a system in software, and then implement it in just enough hardware to do the job.

Newest Inmos H1 chips are highly integrated CMOS VLSI devices. Individual H1 transputers are expected to execute more than 150 Mips peak (60 Mips sustained) and deliver greater than 20-Mflops. H1 chips should be able to execute up to eight instructions and generate two addresses per clock cycle. Significantly, the area of each IC measures less than 1 cm².

As pipelined superscalar devices simultaneously dispatching several instructions from cache, H1 transputers pack CPUs, scalar FPUs, 64-bit external data buses, and rather large 16-kbyte on-chip memories, which can be programmed to act as 8 kbytes each of instruction and data cache. Also included are programmable external memory interfaces. The transputer sidesteps external glue logic, supporting board-level designs using up to 16-Mbytes of off-chip DRAM.

But the real key is the transputer's interprocessor communication scheme, supported by Inmos' Occam language compiler. The ease in which users can create scalable concurrent processing arrays may be the transputer's trump card. Arrays of transputer chips communicate over serial message-passing links.

The latest H1 chips, however, targeted at higher-performance real-time and fault-tolerant concurrent systems, stick with the message-passing approach but with enhancements. The newest H1s have elaborate multiple 4-wire serial interfaces that are capable of transferring data at up to 80 Mbits/s. This contributes to a 10 times performance increase over predecessors.

Regardess of demonstrated cost-versus-performance advantages of well-partitioned, smaller-die-size chip sets, single-chip designs are stealing the limelight. First- and second-pass functionality of multimillion-transistor chips, clock rates pushing 50 MHz and beyond, relatively short 3- to 4-year development times, and the increased development of optimizing compilers are fueling the monolithic fires.

Complex architectures are now the rule. Some CISC processors are taking on RISC features. And RISC ICs, requiring less silicon real estate to begin with, are integrating previously separate peripherals on-chip.

Memory subsystems

Main memory limitations continue to impose complex cache and memory subsystem designs on users. Unique and varied secondary cache controller schemes are migrating on-chip. The trend is to integrate a first level of cache and resort to sub-25-ns SRAMs off-chip in secondary caches addressed over high-speed memory buses. But bandwidth is recognized as a bottleneck. Wider buses to secondary memory are needed.

MIPS Computer Systems (Sunnyvale, CA) has a new CMOS R4000 RISC architecture that uses a 64-bit external address bus. The chip handles addressing via a built-in 64-bit virtual address MMU, and includes internal 64-bit registers, buses and multiple execution units.

The R4000 design avoids problems surrounding multiple execution data dependencies. Unlike competitive RISCs such as Motorola's 88000, R4000s don't rely on mainframe-like scoreboard techniques to keep track of which instructions have been executed. Bypass circuits keep pipelines filled, and the chip's compiler handles the overhead.

Unlike R3000 predecessors that use five-stage pipelines (the latency of individual pipe stages equaled one clock period), 100 native MIPS R4000 chips implement a fine-grained pipeline. They issue two instructions simultaneously (the R3000 issues one).

The R4000 is noteworthy for its 100-MHz internal circuits, with the execution pipeline running 2 times as fast as instruction fetch logic.

By implementing a fine-grained pipeline, MIPS Computer Systems' R4000 "super-pipelined" chip issues two instructions simultaneously.

---

**R4000 PIPELINE**

```
<table>
<thead>
<tr>
<th>1 CYCLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF IS RF EX DF DS TC WB</td>
</tr>
</tbody>
</table>
```

IF: INSTRUCTION CACHE FETCH (FIRST ACCESS)  
IS: INSTRUCTION CACHE FETCH (SECOND ACCESS)  
RF: READ REGISTER FILE  
EX: ALU OPERATION  
DF: DATA CACHE FETCH (FIRST ACCESS)  
DS: DATA CACHE FETCH (SECOND ACCESS)  
TC: DATA TAG CHECK  
WB: WRITE BACK TO REGISTERS

---
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From the outset of the America project in 1985, we knew we needed to achieve significant advances over previous RISC architectures and the earlier IBM RT PC, IBM's first RISC-based Unix workstation. In 1986, we defined a second-generation RISC architecture that would come to be known as the Performance Optimization With Enhanced RISC (Power) architecture. Of primary concern was that the Power architecture and chip set needed to offer both scientific and commercial users the lowest price and highest performance possible. It also had to be extensible, so that it would carry the RISC System/6000 product line through several technology generations.

Building upon earlier work by John Cocke at IBM's Yorktown Heights Research facility (Yorktown Heights, NY), we determined that an architecture that permitted overlap of each basic function—branch processing, integer instruction execution and floating-point execution—would best meet this goal and achieve equivalent integer and floating-point performance.

We believed it was necessary for the Power architecture to provide instruction-level parallelism that could execute up to 5 instructions/cycle: one branch instruction, one fixed-point instruction, one condition register instruction, and one floating-point multiply-add instruction, which would be counted as two floating-point instructions.

Behind every architecture lies a series of decisions that build one upon the other; the Power architecture was no different. For me, four decisions, plus the software technology embodied in our compilers and operating systems, stand out in particular.

Starting from scratch

The RT PC had been introduced only months before we set out to define the Power architecture and chip set. Thus, the first decision we faced was whether to build upon the RT's architecture or to start from scratch. At first, we thought it might be possible to graft a superscalar architecture and other key design concepts onto the existing RT architecture, but we soon realized that would be extremely difficult. For one thing, the RT architecture wouldn't allow the exploitation of instruction-level parallelism we wanted to achieve in the Power chip set, and without that, we couldn't achieve our performance goals.

Even if we could extend the RT architecture to support superscalar implementations, we were certain it wouldn't scale much beyond that. A key design criterion for the Power chip set was that it would be extensible through several successive technology generations. We wanted the chip set to process at least 4 instructions/cycle in its first generation. While it might be possible to extend the RT architecture that far, we knew we could not extend the architecture any further, to implement 6 or 8 parallel instructions/cycle later on, for example, without significant reworking.

The RT had other limitations as well. It had only 16 general-purpose registers, for instance, while our design called for 32. We found that, with 16 registers, we kept running out of fixed-point registers, particularly in floating-point codes. This would severely limit our floating-point performance.

We determined that the Power microprocessor unit would have three separate processors—branch, fixed and floating-point. In the RT architecture, the fixed-point and the branch processors were the same. Separating these two processors would be difficult.

Finally, the RT processor required a coprocessor interface to floating-point extensions. In the end, we realized the RT architecture simply had too many limitations to meet our design goals. Of course, we were keenly aware that customers had already made significant investments in RTs, and that independent software vendors (ISVs) were porting their applications to the RT. At first, we thought that any new RISC CPU design should incorporate binary compatibility with the existing RT, to help preserve customer and ISV investments.

Maintaining binary compatibility, however, carried substantial performance penalties. Since this was to be an optimized architecture, we knew we had to avoid that. In the Unix market, source code compatibility was the norm and would give us an important performance advantage. So we opted for that.

Selecting a floating point

From the beginning, the Power architecture was designed to deliver the best price/performance possible for both commercial and scientific applications. Therefore, we sought to optimize the Power architecture for both integer and floating-point operations, respectively. Our goal was to execute floating-point operations at the same speed as integer operations. That meant the Power architecture had to complete one floating-point operation every clock cycle.

The question was, which floating point—370 hexadecimal or IEEE floating point? Standards drive the Unix market, and the IEEE floating point ranks as such a standard, especially among many mathematicians and scientific users. IEEE floating point was standard on the RT, for instance.

There was significant debate about whether we would give up too much performance implementing the IEEE standard. After drawing heavily on research at IBM's Yorktown laboratory, we were able to select an IEEE-compatible floating-point implementation with no significant performance penalties.

Partitioning chips

The next decision we faced was how best to partition the chip. We had three priorities: to optimize performance, to create a scalable architecture that would expand for low-end and high-end products, and to provide an implementation that would require minimal changes through several technology generations.

In the end, we determined that six unique chip designs would offer the best chance for successful scaling and a long life for the implementation. Those six include a branch processor, fixed-point processor, floating-point processor, MMU, the Micro Channel Architecture bus interface unit, and a data cache unit, implemented in combinations of two or four chips.

We also decided that the initial design point of the Power chip set would
perform at 25 MHz. That would give us an excellent lead in integer and floating-point performance for the first RISC System/6000 products, yet also let us de-vise faster clock cycles in successive generations. In fact, at the initial announcement we introduced a 30-MHz system as well as two 20-MHz systems. We also knew that chip-to-chip crossings wouldn’t drag down performance beyond 25 MHz, and that the memory interface could scale for additional low- and high-end systems.

With these two criteria defined, we designed the six chips, then optimized the chip-to-chip interconnects. In this way, we would be able to increase the clock frequencies without having to rework the entire chip set.

The proof of the success of our efforts was the announcement of RISC System/6000 Model 550 Powerstation Powerserver in October 1990. The 550 implements a 41-MHz design of the Power CPU in IBM’s latest CMOS technology.

- Verification tools

The scope of the Power chip set, with six unique chip designs, was considerably more complex than the three-chip RT design. We realized early on that traditional design verification and simulation tools—such as those used for the RT processor—would be inadequate for the task.

Moreover, time-to-market was crucial. We had to find a way to verify the new design as quickly as possible. Using tools such as those for the RT would have taken longer.

We turned to IBM’s mainframe designers for software simulation tools. Those tools let us run automated simulations overnight and randomly generate complex instruction sequences. With many of our traditional tools, we would have had to generate simulation codes manually, which would have limited the code our verification team could test.

IBM’s compiler and operating system technology played a crucial role in the success of the RISC System/6000. We couldn’t have achieved our ambitious performance goals for the Power architecture without the close cooperation of IBM’s compiler technology laboratory in Toronto, Ontario.

When we built the Power chip set, we implemented one of the first—if not the first—true superscalar RISC architectures. But the hardware’s ability to process multiple instructions in parallel would have been useless without compiler technology to exploit that. We worked closely with our compiler teams to generate code that could exploit the architecture to its fullest. They, in turn, provided us with insight into how we could best implement architectural elements to improve compiler performance even further.

In addition, earlier work on operating system technologies proved invaluable to providing the high reliability users achieve in the RISC System/6000 family’s AIX operating system—IBM’s implementation of Unix. IBM’s 801 project had developed its own operating system, called Control Program-Research (CPR). But, early in RT development process, the design team realized Unix had become a standard, especially for technical computing.

Therefore, it was decided that AIX would be the operating system for the RT and successive RISC-based products such as the RISC System/6000. Still, key technologies of CPR could be stitched into the AIX kernel on the RT and, later, the RISC System/6000. CPR technology improved AIX’s file system reliability and provided preemptible kernel routines, program management, dynamic binding, and other features. All of this remains transparent to the user, who sees a standard Unix interface on a system that is inherently more reliable.

- Foundation for the future

The Power architecture of today provides a solid and extensible foundation for future technology generations.

At the low-end, the original architecture will let us use fewer chips, which, in turn, will lower the cost of entry while maintaining performance. At the high-end, the Powerstation Powerserver 550 is only the beginning. We plan to offer increased performance in a number of ways: through faster clock rates, by exploring clustering and multiprocessor (MP) technologies, and by exploiting fiber optic link technology.

We also plan to extend the original superscalar concepts on which the Power architecture was based. Future iterations of the Power chip set will process even more instructions in a single clock cycle.

Using 64-bit data paths to cache and main memory as well as a 64-bit floating-point ALU, these very dense chips rely on a superpipelined architecture and this double-speed internal clocking to provide performance gains. MIPS’ approach includes hefty on-chip instruction and data caches (8-kbytes each) for its multiple execution units.

VLSI R4000s include FPU’s, IUs and control logic for cache-coherent systems, as well as optional secondary cache interfaces. The design is compatible with 32-bit forerunners and peripheral products and lets designers “tune” off-chip I/O for optimal cost/performance trade-offs using special selection circuits.

While MIPS indicates that lab version R4000 chips have been tested at 50 MHz, other vendors are announcing processors running even faster (although none so far sport 64-bit-wide address buses).

One high-speed single-chip design played center stage at this year’s ISSCC conference. Intel (Folsom, CA) reported development of a 0.8-mm, triple-metal CMOS implementation of the 80486 operating at 100 MHz.

Such a 486, if commercialized and properly supported with superfast packaging, peripherals and memory devices, would certainly boost the performance of applications software in the world’s largest installed applications software base—MS-DOS.

Intel’s racer, having seen silicon, integrates 1.2 million transistors in a fabrication process optimized for on-chip phase-locked loop timing circuits that slash setup, hold and output valid times. Intel says its vehicle is based on markedly reduced wire lengths, planar dielectrics, salicided gates and source drains, and tungsten-filled vias and contacts. These are factors that will play important roles in Intel’s much-closer-to-market 50-MHz 486.

- Embedded applications abound

“The newest technology and the fastest processors tend to debut in computer systems and workstations,” says Fujitsu’s Booth, “but, their impact in the embedded controller arena is equally significant.”

The 1-million transistor superscalar core from National Semiconductor (Santa Clara, CA) is a case in point. Tailored for on-chip digital signal processing, National’s high-throughput chip is aimed squarely at embedded applications.

Code-named “Swordfish,” Nation-
FAST PROCESSORS

486 I/O PERFORMANCE AT 100 MHz

Simulation results based on Intel's 100-MHz 486 processor illustrate how multipackage modules (MPMs) and multichip modules (MCMs) perform as devices get faster. A typical MPM might include a processor and an SRAM cache. An MCM would also include control circuitry, possibly mounted on a silicon substrate. The curves depict performance for pins both close and far from on-chip driver stages.

al's 100-Mips Type 32SF640 engine includes not one but two independent integer units, each with a four-stage pipeline. The dual execution units effectively execute two instructions per clock cycle.

But the parallelism doesn't stop there. Parallel execution of integer and DSP functions is handled by separate on-chip hardware. Execution of multiply/addition routines for DSP algorithms and floating-point calculations overlap with integer processing. On-chip instruction and data caches feed all four processing sub-blocks (any two of which can be simultaneously active).

Although National's latest creation includes a system interface at the data bus that is 64 bits wide, it uses a conventional 32-bit address bus. It's limited, therefore, to addressing a 4-Gbyte uniform address space. The Swordfish's data bus also dynamically supports 8-, 16- and 32-bit peripheral ICs. To minimize embedded cost, National expects Swordfish users will choose an optional clocking scheme that lets an external system bus operate at half the frequency of the chip's internal clock. The Swordfish design will read/write to relatively slow DRAMs and EPROMs—devices that are relatively inexpensive and readily available. Pipelined and wide-bandwidth interleaved memory are also supported.

As impressive as the CMOS Swordfish is, its primary caches are still relatively small. This is suitable, however, because a lot of embedded code—especially time-critical inner-looping routines—execute over and over and are generally less than 400 bytes. A 1-kbyte two-way set-associative data cache and a 4-kbyte decoded instruction cache is provided on-chip. Both are equipped with a locking mechanism to prevent replacement of data deemed performance-critical (National also uses bus snooping logic to ensure coherency between data cache and main memory).

National's preliminary data sheets discuss three versions of the Swordfish, running at either 33 MHz, 20 and 40 MHz, or 25 and 50 MHz. These clock speeds, when combined with the device's superscalar architecture, result in one very fast controller.

If it proves economically reproducible, it should find wide favor in commercial embedded graphics applications. A lot of sockets are waiting for 100-Mips processing in scanners, laser printers and fax machines, among others.

Raw clock speed, plus the ability to put more elaborate structures in silicon, drives the embedded control-effort at Advanced Micro Devices (Sunnyvale, CA) too. The company's new 29050 RISC embedded controller now packs 428,000 transistors—nearly a quarter million more than the widely used 29000 predecessors.

The small feature size CMOS 29050 clocks as high as 40 MHz. At this rate, a 29050, which includes an on-chip pipelined IEEE floating-point processor, can perform 34 sustained MFlops, peaking at 40 integer Mips and 80 MFlops (based on 4x4 and 1x4 graphics transforms).

Low- vs. high-density MOS

CMOS processes such as those of the 100-MHz Intel 486, National's Swordfish and AMD's 29050 dominate superfast single-chip news. CMOS density enables things such as multiple execution units and cache. But BiCMOS and bipolar ECL are gaining favor for high-speed, low-density logic used in superpipelined RISC approaches. BiCMOS and ECL designs offer better control over clock skewing in high-speed circuits, both partitioned and single-chip designs.

As for ECL, some experts predict a move away from the power-hungry logic, regardless of its obvious speed advantages. Motorola, for one, has dropped its plans to collaborate with Data General on a 100-Mips ECL.
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I FAST PROCESSORS

How high-end embedded processors are changing

The embedded processor market is changing. The traditional constraints of high performance and low system cost are no longer the only considerations. Designers of fax machines, laser beam printers, speech compression equipment, and image compression equipment are now demanding that embedded processors be customized for specific low-cost applications. This customization reduces the user’s time-to-market and results in a better cost/performance ratio.

While customization is receiving a new level of emphasis, the user’s need for performance is continuing to grow. It’s no longer sufficient for a processor to excel in a few specific benchmarks. A typical multifunction imaging application, such as a combination laser printer/fax machine, requires digital signal processing for the modern function, fast handling of floating-point operations for the Postscript interpreter, and integer arithmetic for image compression and system control. And the bus interface of such a processor must operate with low-cost memory arrays yet still deliver high performance. External caches are too expensive, so an innovative design approach is needed to achieve high system performance with DRAM arrays.

The design goals for the embedded processor core now called Swordfish were driven by these demands. The design’s dual pipelines, high-performance floating-point unit and DSP capabilities formed the basis of the architecture. The addition of on-chip instruction and data caches and the design of the processor’s bus interface were key to the ability to provide high levels of system performance with low-cost memory arrays. And on-chip peripherals were added to reduce the system board size.

An embedded architecture
We knew that by early 1991 we could produce a device that would have more than 1 million transistors and operate reliably at 50 MHz. The problem was where to allocate the transistors. We had to choose among larger caches, more execution pipelines, improved FPU performance, and a faster multiplier. We also faced the challenge of building a RISC processor while still maintaining compatibility with other members of National’s Series 32000 embedded processor family.

We could have chosen to define a more complex logic for issuing instructions, using out-of-order execution. Instead, because an optimizing compiler can reorder the code and yield about the same performance, we decided to allocate the transistors to modules that would have a greater impact on the total performance. The logic for issuing instructions, together with the instruction cache and the instruction loader, are key contributors to performance, so the greatest effort was concentrated on optimizing this path.

More high-end processors will include on-chip system modules, reducing the costs of systems.

The bus interface unit is one of the most sophisticated parts of the chip. This unit must deliver high performance for a wide range of memory structures. The bus interface unit provides full support for two interleaved memory banks by providing two sets of control signals. Furthermore, the unit can be programmed to operate at half the internal execution frequency. As a result, execution is fast, even with slow memory arrays.

Finally, we put a lot of effort into on-chip debug features. The most important feature is support of in-system emulation (ISE), with a special serial link from ISE equipment to the Swordfish processor.

Interdisciplinary cooperation
The design process of a complex processor requires the expertise and cooperation of many disciplines. The Swordfish design team comprised architects, chip designers, compiler experts, system designers, and a logic verification group, working together to define the architecture specification of Swordfish.

During initial definition of the processor’s architecture, we focused our attention primarily on the number of execution pipelines, the cache structure and the system interface. The architecture group built a performance simulator, and the compiler experts built a prototype compiler. Together both groups simulated different pipeline models with different instruction sets. At the same time, chip designers evaluated the feasibility of implementing the different models. By defining the compiler at the same time as the architecture, we were able to choose whether a function would be implemented in hardware or in the compiler. Next, we defined the caches and the system interface.

The bus was defined primarily by system designers. At this stage, we considered supporting half-frequency bus operation and interleaved memory configurations. We also integrated a system interface module into our performance simulator, enabling simulations of off-chip caches, DRAM arrays with in-page support and other memory configurations.

The result of this design effort was a RISC CPU core optimized for compute-intensive embedded applications. Its dual integer units, each with a four-stage pipeline, and its on-chip FPU with an array multiplier, and caches for instructions and data, allow a high degree of parallel execution of instructions.

Combined with clock rates up to 50 MHz, the architecture provides execution speeds up to 100 Mips. This superscalar RISC processor core is the first in a new generation of high-performance processors that will form the computational heart of embedded processors customized for specific applications.

The changes in the embedded processor market will continue to drive integration. More high-end processors will include on-chip system modules, reducing the costs of systems by providing greater functional integration. The common goal of embedded processor designers and users is ultimately to have a single-chip solution for a given application, requiring that a specific CPU core be integrated with a different set of on-chip modules for each application.

The main obstacle to high performance in the embedded control market is limited memory speed. Future processors will solve this problem using larger caches and wider buses. They will also provide on-chip support for interleaved DRAM arrays to narrow the gap between processor speed and memory speed.

Gideon Intrater, MSE, chief Swordfish architect, engineering manager, National Semiconductor design center
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CIRCLE NO. 66
FAST PROCESSORS

88000 spin-off. But not everyone agrees ECL’s days are numbered.

MIPS Computer Systems’ new systems-level server products, for example, built in conjunction with Prime Computer and Content Data Corp, are based on ECL microengines. NEC, MIPS’ foundry partner, is expected to start shipping volume production quantities of MIPS’ three-chip ECL RISC chip set.

And, it’s only been a short while since Bipolar Integrated Technology (Beaverton, OR) introduced an ECL FPU chip—the IEEE-compatible B3130.

“There are no fundamental manufacturing limitations facing ECL makers,” says Jim Peterson, vice-president of engineering at Bipolar Integrated Technology (BIT). “And, the inclusion of CMOS memory into ECL processes may actually accelerate ECL density and performance curves. Moreover, ECL processes are able to deliver the required clock frequencies to support superpipelining.”

Significantly, BIT’s bipolar process competes with CMOS for density. It trims power dissipation from bipolar’s typical 2 or 3 mW/gate to a few hundred mW/gate.

For now, the highly pipelined B3130 device is set to provide sustained performance at 200 MFlops. Sporting a 64-bit I/O bus, the B3130 incurs only 20-ns latency for ALU and multiply operations, resulting in 100 MFlops for random scalar operations and up to 100-Mips scalar performance. The chip concurrently executes ALU, multiplier and divide/square root operations.

BIT is already enjoying design wins for the B3130 and acceptance of the company’s bipolar technology. HP/Apollo has signed up to use the new chip, FPS Computing’s supercomputer is using BIT’s ECL-based Sparc RISC, and BIT has been selected by MIPS Computer Systems as the foundry for MIPS’ fastest R6000 32-bit processor in its ROC6280 RISComputer server.

BiCMOS gains favor

BiCMOS is gaining momentum too. Motorola is discussing its next-generation 88000 RISC product, the symmetric superscalar 88110. The chip is fabbed in triple-level metal 0.8-µm CMOS, but Motorola seems likely to use BiCMOS in a post-88110 family of highly parallel superscalar microprocessors.

These ICs will probably have very wide buses and 100-MHz speeds. The BiCMOS 88110 is intended to be object-code compatible with the original 88000, but it will feature multiple independent pipelined execution units.

ECL 88110s will likely have on-chip FPU, special graphics units for 3-D number crunching, demand paged MMUs and on-chip caches. Motorola says these RISCs will have less than 1.5 million transistors.

What do IC giants such as Motorola and Intel see in the future for fab technologies where 1.5 million device chips are considered sleek? In recent statements to the industry, Motorola discussed its dual-pronged BiCMOS RISC and CMOS CISC strategy. The company identified process technologies to achieve 4 times performance improvements on each generation of 88000 RISC throughout the decade.

Motorola predicts improvements in transistor density and speed thanks to BiCMOS. The company predicts over 100 million devices on a chip, clocking at over 300 MHz. Single-chip microprocessors will deliver 4 billion instructions/s performance by the year 2000, Motorola engineers forecast.

Intel also plans for 50- to 100-million transistor CPUs. Its Micro 2000 architecture includes ICs capable of 2 billion instructions/s, maintaining binary compatibility with the 386 family and MS-DOS/OS-2/Unix architectures.

Of course, such efforts will be incredibly costly. As performance competition heats up in CISC and RISC camps, processor makers must adopt new and increasingly expensive fabrication and test systems. Intel recently announced a $1 billion spending plan for an 8-in. wafer fab this year.

Pushing the limits?

With industry leaders such as Intergraph, SGS-Thomson and others capitalizing on small-die multichip systems and advanced packaging, one wonders whether megachips represent a viable course for future generations. Some industry analysts say no. They contend today’s fab technologies are rapidly approaching practical limits to feature size reduction. Conventional step- and wet and even dry plasma etching cannot meet the submicron challenge necessary to make ICs such as BIT’s and National Semiconductor’s feasible in the marketplace, they say. Particle control and clean-up techniques may not be adequate either. Moreover, many systems designers suspect on- and off-chip packaging and interconnect constraints will put a damper on further reductions in feature sizes, too.

Others disagree. “We’ve just opened a fab line with sub-0.5µm optical technology,” says Bob Rowe, RISC marketing manager at Integrated Device Technology (Santa Clara, CA). That company builds products based on MIPS Computer Systems’ RISC instruction set and architecture. “Remember, only a few years ago folks said the limit for CMOS was 1 µm, but that proved not to be the case.”

Rowe says there’s no reason why the trend shouldn’t continue. “Submicron fab makes 30-MHz clock speeds routinely possible. Look at
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our latest R3000 devices—40-MHz ICs are coming off the lines in economically feasible production quantities.”

Motorola’s Reinhart agrees. “At the present time the 68040 is 580x609 mils with 1.2 million transistors. It’s cost-effective, yet if you asked two years ago we would have said it wouldn’t have been.”

Today’s defect-reduction and yield-enhancement techniques enable manufacturability. “Our goal has been to consistently double performance,” Reinhart says. “We presently build 68040s in two-layer metal, 0.8-µm drawn feature size (0.7 L-effective) dimensions. We’ve also built a few 68040s with 0.65-µm features, and we’re qualifying this process for use later in the year. This will give a smaller die cost reduction and make possible 40 MHz.”

Submicron 68050s are coming

Notably, 0.65-µm is also the starting point for Motorola’s next-generation superfast CISC—the 68050. “To double the 040’s performance, we have to set a clear path to 0.5-µm CMOS,” says Reinhart. “We’ve already invested in a fabrication line for 8-in. wafers, with process capability for microprocessors with very fast SRAM.”

Regardless of the confidence semiconductor manufacturers express for optical lithography, resource-rich firms such as Motorola are also investing in X-ray lithography. Motorola is doing so in conjunction with IBM, Sematech and others.

“It’s a tremendously scary technology, though,” says Reinhart. “It costs millions just to build a required particle accelerator. One wants to be generating a lot of revenue to justify that.”

Reinhart says optical lithography will live on, even where it has recently been predicted to fall apart. “There’s no way to avoid X-ray in the future,” he says, “but is it at 0.5, 0.25 or less than 0.1 µm? We don’t know.”
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32-bit emulators struggle with processor complexities

Jeffrey Child, Associate Editor

With budgets tighter than ever, designers of 32-bit microprocessor-based systems may welcome any alternative to buying an emulator. Most admit, however, that there's no real substitute for a full-blown in-circuit emulator for debugging systems in real time. And as processor speeds reach 33 MHz and above, many are starting to question the feasibility of building emulators at a reasonable price.

The challenge for emulator manufacturers is to create emulators with the control capabilities needed to debug complex programs and to integrate complex systems. But accomplishing this for 32-bit devices is not an easy task, especially with the combinations of high speed and complex architectures found in today's high-end microprocessors.

As microprocessors have become more complex, so has the task of debugging and development. Faster devices can process more instructions, leading to larger applications, leading to more software. While around 80 percent of that software in a design needs to talk only to other parts of the software, there's still that important remaining part of the code that must interface with the hardware directly. Developing this 10 to 20 percent of code is the job of the emulator.

Network support

As a result of growing size of code, the ratio of software designers to hardware designers involved on projects has gone from 1:1 to around 10:1. This new design environment requires development tools that fit a team-oriented concurrent engineering methodology. Recognizing this, an increasing number of emulator vendors are including network support in their products so that emulators can pass code to other systems.

"A problem that comes up with 32-bit designs is that the scale of projects has changed, and all the managers and designers working on the project should recognize that," says Richard Jensen, vice-president of new business development at Applied Microsystems (Redmond, WA). "Tools are needed to support that different scale."

Design projects for 32-bit emulators are more complex, creating emulation problems for designers and cost problems for emulator manufacturers. "The first scale of problems is linear—wider addressing and data capability. That means more signals, more pins and more problems," says Jensen. "So from the number of added signals all the way to the amount of memory that's required, the tool is going to cost more to build."

Speed requirements also contribute to cost. The generally accepted rule is $1,000/MHz, which holds up reasonably well for most of the full-featured emulators (see chart, p 124). Applied Microsystems' latest offering, the EL3200, is a development environment for the Intel i960CA microprocessor. The system includes a 33-MHz emulator and a software development package. The emulator is designed to offer real-time transparent emulation to full i960 speeds with no wait-states. Special features of the i960 are supported by the EL3200, including pipelining, burst modes and the different bus widths. The emulator's trace-and-event system allows tracking and isolation of complex, real-time interactions between hardware and software. Full networking capability is provided for Sun Spare workstations and personal computer-compatibles.

Complex architectures

Another hurdle manufacturers of 32-bit emulators face is the sophisticated architecture of the latest processors. "It used to be that the logical execution flow and the physical execution matched. By observing the execution on the bus you could determine what was going on inside the chip," says John P. Romano, manager of research and development at Hewlett-Packard's Logic Systems Division (Colorado Springs, CO). In 32-bit processors that's no longer the case. Internal pipelines, multiple execution units for floating point and memory management, and on-chip caches all confound an emulator's ability to observe the internal workings of a chip. This complexity also inhibits the ability to correlate activity on the system bus with the high-level instruction the user expects to see. "You basically have to replicate the logic of the processor," says Romano. "Accomplishing this is becoming prohibitively expensive."

The Mice-V emulator for the i486 from Microtek International features an isolation mode that lets users remove the processor from the probe tip and still do emulation. The emulator doesn't need functional hardware to begin emulating—all that's required is a working clock signal.
### PRODUCT FOCUS: 32-bit Emulators

<table>
<thead>
<tr>
<th>Model</th>
<th>Speed (MHz)</th>
<th>Processor(s) supported</th>
<th>Overlay memory (bytes)</th>
<th>Number of break points</th>
<th>Number of breakpoints</th>
<th>Trace buffer depth (k)</th>
<th>Performance analysis</th>
<th>Price</th>
<th>Comments</th>
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<td><strong>Applied Microsystems</strong></td>
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<tr>
<td>EL3200</td>
<td>33</td>
<td>i960CA</td>
<td>4 M</td>
<td>53</td>
<td>4</td>
<td>8 k x 139</td>
<td>Y</td>
<td>$30,000</td>
<td>zero wait-state 20-MHz read and zero wait-state 30-MHz write; fully networked; Sun or PC hosts same as above</td>
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<td>EL3200</td>
<td>33</td>
<td>68020, 68030</td>
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<td>4</td>
<td>8 k x 139</td>
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<td>Sun network operation; SCSI communications; Sun, PC or VAX hosts</td>
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<td><strong>Cadre Technologies</strong></td>
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<td>25</td>
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<td>4</td>
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<td>2 k x 88</td>
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<td>source-level debug for C and Ada real-time source trace; Sun, PC or VAX host same as above</td>
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<td>50</td>
<td>16</td>
<td>2 k</td>
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<td>$14,955-$32,370</td>
<td>interfaces to assembly and C debuggers; supports 7 host systems</td>
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<td>8 k</td>
<td>Y</td>
<td>$24,995-$66,870</td>
<td>Ethernet interface; supports 7 host systems; low-capacitance probe head</td>
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<td>MIPS R3000, R3000A, R3001</td>
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<td>16</td>
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<td>Y</td>
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<td>Ethernet interface; supports 5 host systems; cross-development software</td>
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<td><strong>Hewlett-Packard</strong></td>
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<td>HP64774</td>
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<td>1 M</td>
<td>8</td>
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<td>1 k x 80</td>
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<td>$24,445</td>
<td>supports big- and little-endian byte ordering; supports several file formats</td>
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<td>$24,294-$30,554</td>
<td>precise dequeueing and analysis of code running in cache</td>
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<td>1 k x 80</td>
<td>Y</td>
<td>$39,960</td>
<td>active probe; extensive help; software dequeueing; custom memory mapper software dequeueing; full 68040 debug register support interfaces on the PC and HP4000 series 300/400 workstations</td>
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<td>$28,475</td>
<td>real-time transparent access to target memory; supports several file formats</td>
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<td>AT&amp;T DSP33C</td>
<td>64 k</td>
<td>8</td>
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<td>1 k x 64</td>
<td>Y</td>
<td>$28,503</td>
<td>download speeds exceed 1 Mbyte/min; cable adapters allow probing of PGA and PQFP packages</td>
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<td>HP64760</td>
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<td>HMI-200-68020</td>
<td>16, 25, 33</td>
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<td>256 k-4 M</td>
<td>8</td>
<td>4</td>
<td>two 4 k x 104</td>
<td>Y</td>
<td>$12,000-$21,000</td>
<td>integrated with window-driven debugger; real-time performance analysis operates transparent to system</td>
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<td>two 4 k x 104</td>
<td>Y</td>
<td>$16,000</td>
<td>same as above</td>
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124 MAY 1, 1991 COMPUTER DESIGN
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<tr>
<td>ICE386DX</td>
<td>25, 33</td>
<td>80386DX</td>
<td>128 k-2 M</td>
<td>12</td>
<td>4</td>
<td>4 k-96</td>
<td>optional</td>
<td>$22,500</td>
<td>windowed-interface; trace filtering</td>
</tr>
<tr>
<td>ICE486/33</td>
<td>33</td>
<td>i486</td>
<td>2 M</td>
<td>12</td>
<td>4</td>
<td>8 k-96</td>
<td>N</td>
<td>$38,000</td>
<td>execution trace instructions; sequential break points on events that occur from cache; trace filtering</td>
</tr>
<tr>
<td>ICE960-R3.0</td>
<td>16, 25</td>
<td>8088KA/KB</td>
<td>2 M</td>
<td>10</td>
<td>8</td>
<td>1 k-240</td>
<td>N</td>
<td>$16,495</td>
<td>module selection for symbol table improves download time; trace filtering</td>
</tr>
<tr>
<td>Microtek DSD</td>
<td>3300 NW 211th Ter, Hillsboro, OR 97124-7136 (503) 645-7333</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Mice-III</td>
<td>25</td>
<td>68020</td>
<td>1 M</td>
<td>7</td>
<td>8</td>
<td>8 k-96</td>
<td>Y</td>
<td>$16,500</td>
<td>code coverage option identifies code that is or isn't used</td>
</tr>
<tr>
<td>Mice-III</td>
<td>25</td>
<td>68030</td>
<td>1 M</td>
<td>7</td>
<td>8</td>
<td>8 k-96</td>
<td>Y</td>
<td>$18,000</td>
<td>same as above</td>
</tr>
<tr>
<td>Mice-V</td>
<td>33</td>
<td>80386</td>
<td>512 k</td>
<td>12</td>
<td>4</td>
<td>8 k-144</td>
<td>N</td>
<td>$25,000</td>
<td>—</td>
</tr>
<tr>
<td>Mice-V</td>
<td>20</td>
<td>80386SX</td>
<td>512 k</td>
<td>12</td>
<td>4</td>
<td>8 k-144</td>
<td>N</td>
<td>$18,250</td>
<td>—</td>
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<tr>
<td>Mice-V</td>
<td>33</td>
<td>i486</td>
<td>—</td>
<td>12</td>
<td>4</td>
<td>8 k-144</td>
<td>N</td>
<td>$32,000</td>
<td>can isolate the i486 chip from the emulator pod; permits debugging of nonfunctional hardware</td>
</tr>
<tr>
<td>Motorola</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>CDS32</td>
<td>25</td>
<td>68331/2</td>
<td>1 M</td>
<td>4</td>
<td>4</td>
<td>8 k-136</td>
<td>N</td>
<td>$7,950</td>
<td>runs on PC-compatible or PS/2 hosts; 16 software breakpoints</td>
</tr>
<tr>
<td>Softaid</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>CodeStalker 386</td>
<td></td>
<td>386</td>
<td>512 k</td>
<td>4</td>
<td>1</td>
<td>4 k-48</td>
<td>N</td>
<td>$9,995</td>
<td>fiberoptic link provides fast downloads (250,000 bytes/s)</td>
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<tr>
<td>CodeStalker 386SX</td>
<td></td>
<td>386SX</td>
<td>512 k</td>
<td>4</td>
<td>1</td>
<td>4 k-48</td>
<td>N</td>
<td>$9,995</td>
<td>same as above</td>
</tr>
<tr>
<td>Step Engineering</td>
<td>661 E Arques Ave, Sunnyvale, CA 94086 (408) 733-7837</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Adapt II Plus</td>
<td>33</td>
<td>AM29000, AM29005, AM29050</td>
<td>1 M</td>
<td>1</td>
<td>0</td>
<td>4 k-160</td>
<td>N</td>
<td>—</td>
<td>logic analyzer interface; zero wait-state overlay memory</td>
</tr>
<tr>
<td>Excel 930</td>
<td>40</td>
<td>Fujitsu SparLite MB69530</td>
<td>0</td>
<td>5</td>
<td>0</td>
<td>8 k-160</td>
<td>N</td>
<td>—</td>
<td>Ethernet interface; 32 external bits; cache reconstruction</td>
</tr>
<tr>
<td>ExpressPlus 960CA</td>
<td>33</td>
<td>i960CA</td>
<td>0</td>
<td>9</td>
<td>0</td>
<td>8 k-160</td>
<td>N</td>
<td>—</td>
<td>Ethernet interface; cache reconstruction</td>
</tr>
<tr>
<td>Adapt II</td>
<td>25</td>
<td>AM29000, AM29005, AM29050</td>
<td>1 M</td>
<td>1</td>
<td>0</td>
<td>4 k-160</td>
<td>N</td>
<td>—</td>
<td>logic analyzer interface; 32 external bits; zero wait-state overlay memory</td>
</tr>
<tr>
<td>Zax</td>
<td>2572 White Rd, Irvine, CA 92714 (714) 474-1170</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ERX-68030/20 HS</td>
<td>25, 33</td>
<td>68020/30, 68881/2</td>
<td>256 k-2 M</td>
<td>1,000,000</td>
<td>4</td>
<td>8 k-88</td>
<td>optional</td>
<td>$23,150</td>
<td>256-kx4-channel memory scheme allows over 1 million hardware breakpoints</td>
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<td>ERX-68030</td>
<td>20</td>
<td>68030, 68881/2</td>
<td>256 k-2 M</td>
<td>1,000,000</td>
<td>4</td>
<td>8 k-88</td>
<td>optional</td>
<td>$16,840</td>
<td>same as above</td>
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<tr>
<td>ERX-68020</td>
<td>20</td>
<td>68020, 68881/2</td>
<td>256 k</td>
<td>1,000,000</td>
<td>—</td>
<td>8 k-88</td>
<td>optional</td>
<td>$14,730</td>
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<tr>
<td>ERX-80386</td>
<td>16</td>
<td>80386, 80387</td>
<td>256 k-2 M</td>
<td>1,000,000</td>
<td>4</td>
<td>8 k-88</td>
<td>optional</td>
<td>$16,840</td>
<td>same as above</td>
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I PRODUCT FOCUS/32-bit Emulators

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**HP's 64000 series of emulators**

HP's 64000 series of emulators offers a feature called prestore, which is particularly important in larger applications. The emulator can be set up so that the trace buffer captures only write to this data area. If the prestore is on, it captures not only the write cycle but also the previous state; in other words, it identifies where the write came from. If a pointer value is misused in C, for example, prestore can capture information showing which piece of code uses that pointer and where the pointer received the wrong value.

**Cache problems**

On-chip caches provide advantages to aid system performance. They not only boost speed but also let instructions be executed inside the chip, freeing up the bus for other devices in the system to use. Cache can be a nightmare for in-circuit emulators as they try to match in-

---

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CIRCLE NO. 69

**CIRCLE NO. 71**
Instructions executed with corresponding bus cycles. Keeping track of instructions executed from main memory is straightforward, but when instructions are executed from inside the cache, no bus cycles are involved.

The 8-kbyte cache in the Intel 486, for example, complicates the job of an emulator. Some emulator vendors provide the option to turn off the cache while emulating, but by doing so the system is no longer running in real time. Other solutions involve using algorithms to estimate which instructions are in the cache. Intel, which also makes emulators, has an obvious advantage because it can tap into proprietary signals on the chip. Using these signals, Intel can identify exactly which instructions are being executed from in the cache. The 486 also contains debug registers that aren’t proprietary.

“The i386 and i486 were designed for debugging from the start,” says Tovey Barron, senior technical marketing engineer at Intel (Hillsboro, OR). “They both have debug registers that provide the capability to control events that occur in the chip, as a first step in that direction. As the caches get bigger, and the functions on the chip get more and more sophisticated, the debug capability built into the chip will have to become more sophisticated, because the emulator vendor will not be able to see into a chip through its pins.”

### On-chip support for RISC

Solving emulation problems of faster-speed RISC processors may also require on-chip circuitry that supports emulation. In fact, the lack of such on-chip support is a possible reason behind the lack of emulators available for RISC processors. When it comes to building an emulator for a Sparc or MIPS RISC processor, speed isn’t the fundamental problem. “RISC chips are easier to emulate,” says Applied’s Jensen. “The cache is outside, the MMU is outside, and there are no half instructions or byte-wide instructions. It’s all pretty balanced. The problem is that RISC processor designers have put very little in the chip that lets us get control of the processor.”

Despite the many concerns expressed about the feasibility of building emulators for tomorrow’s faster processors, some views are optimistic. “The market has proclaimed the end of emulators since about 1984,” when everyone was saying that it will be impossible to emulate the next generation of processors,” says Rick Leatherman, vice-president of marketing at Microtek International’s Design Systems Division (Hillsboro, OR). “Emulators can be built for almost any processor out there, as long as the speeds are within TTL limits. However, the price to support the faster speeds goes up exponentially.”

Even some of the high-end 32-bit emulators are not all that they could be. According to Leatherman, even sophisticated emulators require that a board be at least 75 percent functional before it could be of any use. To address this issue, Microtek’s Mice-V emulator for the 486 features an isolation mode with which a user can actually remove the processor from the probe tip. When the emulator is initialized and realizes that the processor is missing, it allows the user to stimulate the target system.

Full in-circuit emulation alternatives that offer some view into the internal workings of a processor are appearing. Texas Instrument’s scan-based emulation and Applied Microsystems’ CodeTap are two examples. But neither of these offer true substitutes for full in-circuit emulation.

“If you could come up with an instrument or a methodology,” says Jensen, “that lets you control the execution of the processor, provide visibility into the execution of that processor (even with interrupts coming in), and do it in real-time, then you’ve got a substitute for an emulator.”

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COMPUTER DESIGN MAY 1, 1991 127
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Simulation tool simplifies top-down analog design

One of the problems in migrating analog simulation into a top-down design environment has been the reluctance of analog engineers to work in software languages to describe analog behavior. In addition to this reluctance, there's no IEEE-sanctioned analog hardware description language (AHDL) for even the most willing engineer to embrace. Valid Logic Systems' Profile and Analog Workbench II may be the answer to this dilemma.

Profile lets analog designers describe blocks or entire circuits at the behavioral level by using a combination of graphics and text. The resulting models can be simulated in Workbench II, a mixed-behavioral and structural-level design environment. With this combination, engineers can adopt a top-down or bottom-up strategy, which is useful for large, hierarchical designs that must be partitioned across multiple design teams.

Strong models

Profile's graphical interface lets users create and simulate an architecture without having to resort to a language-based behavioral modeling technique. The Profile models also support user-specified error and warning messages, allowing in-process circuit diagnostics.

"Analog behavioral models are key elements of a good architectural design," says Eric Filseth, Valid's product marketing manager for analog CAE. "After all, if your specification is wrong, most probably the product won't work. But getting accurate analog models has been a real problem, especially for parts that aren't entirely electrical, like motors and sensors. The characteristics of such an electromechanical device have a definite impact on the circuit that drives them. So if you want to design a good circuit, you need a good model." A purely language-based approach, he adds, is not going to work until an AHDL standard is defined.

With Profile, Valid focused on ease of use: engineers aren't required to use the templates or compilation methods that are common and basic arithmetic. In addition to providing electromechanical device models for motors, solenoids and sensors, Profile can build mixed analog-digital models for components such as data converters and phase-locked loops.

Multilevel simulation

Once analog designers have developed Profile models, they can simulate and analyze their designs in Analog Workbench II. Multilevel simulations containing both high-level behavioral descriptions and transistor-level circuitry operate in the simulation environment. It's also possible to simulate systems in which some, but not all, of the blocks have been fully designed at the circuit level. This allows users to begin manufacturability, quality and reliability analyses at early stages in the design.

Profile models are fully compatible with all Analog Workbench II analysis tools including sensitivity analysis, pole/zero analysis, stress analysis, and parameter analysis. For specific needs, Valid also provides a User-Coded Models feature, which lets engineers write analog models in C or Fortran and simulate them in Valid's version of Spice, Spice Plus, along with conventional devices.

Profile is available now as an option to Analog Workbench II for $15,000. Analog Workbench II, including user interface, basic analysis tools and Spice Plus, is available on Sun, Digital and IBM RISC System/6000 workstations. Prices start at $12,000.

Valid Logic Systems
2820 Orchard Pky
San Jose, CA 95134
(408) 432-9400

Circle 351
Design system option generates DSP code from block diagrams

Two new options for Comdisco Systems' Signal Processing Worksystem (SPW), a CAD system for digital signal processing, let designers automatically generate program code from the same graphical description that can be used for the system architecture. These features give designers greater flexibility in partitioning their designs between hardware and software and in applying multiple processors to a system design.

The two new software generation modules, called MultiProx (MPX) and DSP ProCoder (DPC), fit into the SPW environment, which includes a graphical block diagram editor and a signal display editor that lets designers describe a DSP system in terms of signal flow blocks. SPW already can output VHDL and netlist descriptions for the design of ASICs and printed circuit boards.

Simple and automatic

MPX lets DSP designers partition a system block diagram into various functional regions to be executed by separate processors. The system then generates C code for each processor. DPC targets specific fixed-point DSP chips and automatically generates assembly language code from the signal flow block diagram.

MPX supports all the SPW application libraries, which include some 500 DSP signal blocks, from filter designs and encoder/decoder functions to math blocks. Users simply assemble the blocks with the SPW block diagram editor and then draw boxes around those portions of the diagram that they wish to run on separate processors.

The system not only generates the C code to run on the different processors, but automatically handles the details of interprocessor communication via shared memory. The links between modules can use either data flow designs or control flow designs. Users have the option to substitute their own interprocessor communication protocols.

The C code can then be compiled for any general-purpose processor or specialized DSP processor for which a C compiler exists. This allows designers to do a good amount of their design verification in an execution environment other than the final target system. It also lets them experiment with load balancing and identify possible bottlenecks among multiple processors. Decisions can also be made about possible hardware implementation of all or part of the design in ASICs.

Comdisco has initially targeted MPX at Texas Instruments' TMS320C40 and Motorola's M96002 DSP chips on chip-specific PC-based hardware and software development systems. In the future, Comdisco will target MPX and additional chips at different system buses, such as VMEbus and VXIbus; it also plans to add its own multiprocessor performance diagnostic tools.

More-specific option

DPC, like MPX, generates code from graphical signal flow diagrams. However, DPC is aimed at the efficient generation of assembly code and is therefore tailored for specific DSP chip architectures and instruction sets. The initial target processor will be Motorola's DSP56001, followed by Texas Instruments' TMS320C50.

Initially DPC will support fixed-point DSP chips where optimization is essential; later, it will be moved to support floating-point DSP processors. Currently it supports a library of 60 functional blocks and can generate one to three lines of assembly per kernel block.

Both MPX and DPC are based on an open architecture in which designers can add their own blocks or segments of code. Both code generator systems run on the same environments as the SPW—Sun, Hewlett-Packard/Apollo and Digital Equipment Corp workstations.

Both software modules are scheduled for shipment in the fourth quarter. MPX will cost $10,000; DPC will cost $15,000.

—Mike Donlin

A DSP ProCoder screen shows a signal flow block diagram created with the Signal Processing Worksystem's block diagram editor. In the accompanying window is 56001 assembler code that has been automatically generated directly from the block diagram.
Hardware modelers meet needs of small and large design teams

A typical circuit board today consists of a complex microprocessor and coprocessor, as well as a conglomeration of ASICs, standard parts, I/O, memory and glue logic. For such an arrangement to work, reliable models must be incorporated into a simulation environment to accurately predict prototype behavior. As clock speeds and device complexity increase, modeling technology must keep pace—a need that Logic Modeling Systems has addressed with the introduction of its latest hardware modelers, the LM-1200 and LM-500.

The LM-1200 achieves up to six times higher performance than Logic Modeling Systems’ first hardware modeler, the LM-1000, which was introduced in 1989. To do so, it uses a much faster CPU (the 25-MHz 68040), an improved network server and enhanced hardware-modeling algorithms. The system also hosts 8 Mbytes of memory (expandable to 32 Mbytes), which increases its fault simulation capacity by as much as a factor of 10.

Higher processing speeds let the LM-1200 support multiple design teams, all working concurrently with a variety of complex models. As many as 2,560 signal pins can be modeled on the Logic Modeling system, and support is provided for complex standard devices, including the 486, 68040, R3000A, and 29050.

In a nod to the needs of smaller design teams who might not be able to afford the horsepower of the LM-1200, Logic Modeling has also rolled out the LM-500. It supports devices as large as 160 pins, including the 80386, 68030 and 29000. The LM-500 supports more than 95 percent of the hardware models currently offered by Logic Modeling.

To support existing users, Logic Modeling also is offering an upgrade kit for the LM-1000. The kit, which will bring the performance of the LM-1000 up to that of the LM-1200, consists of a CPU board and software. Although the LM-1000 will be phased out of production by the end of June 1991, Logic Modeling plans to support existing systems.

The LM-1200, the LM-500 and the upgrade kit will all be available by mid-June. Prices for the LM-1200 start at $87,000. The LM-500 starts at $35,000. The upgrade kit costs $19,000.

—Mike Donlin

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Circle 352
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<tr>
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Single-chip decoder PLDs give users freedom of choice

Fast enough for systems with clock rates of up to 50 MHz, the 12-input, 8-output CY7B336, CY7B337, CY7B338, and CY7B339 BiCMOS programmable logic devices from Cypress Semiconductor let users tailor the products' benefits to their needs. With the PLDs, designers can either use 40-MHz-or-faster processors, or specify slower, less-expensive SRAMs for designs that use 33-MHz processors.

The 336 and 337 have registered inputs that make them compatible with RISC processors such as the MIPS R3000, the AMD 29000 and some Sparc implementations, all of which assert addresses for a short period around clock edges. The 338 and 339 have output latches to accommodate CISC processors such as the 80486, which does not issue an address with every clock and which removes addresses and data before the end of clock cycles. Users can also select the 6-ns 336 and 338, in which product terms are limited to two per output for speed, or the 7-ns 337 and 339, which have four product terms per output for implementing an addressing scheme with bank select and/or byte write control. The 338 is faster than, but similar in architecture to, Intel's CMOS 85C508 single-chip decoder.

Users pick the benefit

Designers can use the new parts either to significantly reduce system memory cost, or to use faster processors with faster memory, according to Cypress senior product marketing engineer, Robert Moore. "The fast decoders allow designers to make that trade-off between dollars and speed."

Cypress accomplishes that speed by actually implementing ECL circuitry, says Moore. The fuse-programmable BiCMOS features an ECL speed path, BiCMOS-level conversion circuitry and CMOS for control. Cypress uses the same BiCMOS to manufacture its 7.5-ns PAL22V10C-7.

The dozen input registers of the 6-ns 336 and dozen inputs of the 6-ns 338 capture data at the rising edge of the clock signal and forward information to a 24×16 programmable array. Processed data from the array is available to external logic via the eight output pins. One of the two product terms sums products from the array while the other controls tristate output buffers. All outputs of the 7-ns 337 and 339, which have 24×32 programmable arrays, can be tristated. Each of the four parts has an asynchronous output enable, power-on-reset and more than 2,001-V input protection from electrostatic discharge.

Packages for the Cypress decoders include 28-pin, 300-mil plastic and ceramic DIPs, SOJs, LCCs, and PLCCs. The 336 and 338 cost $16.35 (100s) and the 337 and 339 cost $14.30 (100s). Production quantities of the 338 and 339 are available now; samples of the 336 and 337 are available now, with production quantities expected next quarter.

—Barbara Tuck

Cypress Semiconductor
3901 N First St
San Jose, CA 95134-1599
(408) 943-2600

Circle 355

33-MHZ PIPELINED ADDRESSING WITH DECODER PLDs

Output latches in the 6-ns Cypress CY7B338 enable it to decode addresses in a CISC-based system, such as this 33-MHz 80386. The programmable logic device decodes the address data and maintains it on the bus until the next data screen. The effect is to allow cache design based on 45-ns SRAMs, instead of the more-expensive 35-ns devices required without the decoder PLD.
I NEW PRODUCT HIGHLIGHTS

INTEGRATED CIRCUITS

High-speed CMOS gate arrays integrate 150,000 gates

The CMOS-7 series of CMOS gate arrays from NEC Electronics offers up to 150,000 usable gates. At 0.3 ns for a power NAND gate, the devices also push the envelope of ASIC speeds. The CMOS-7's mix of density and performance is targeted to meet the integration and speed requirements of ASIC implementations in superminicomputers, high-end workstations, telecommunications systems, and instrumentation.

The devices feature a sea-of-gates architecture that provides gate complexities from 60,500 to 250,000 equivalent gates using four master-slice options. Power dissipation of the devices is 6.5-mW/gate. The parts have I/O pin counts from 220 to 488.

The CMOS-7 devices use the same cell library as NEC's previous generation ASICs, simplifying migration from the older 1.0-µm CMOS-6 series. More than 300 macrocells are available, including ROM and RAM macroblocks with built-in self-test circuitry.

Built with NEC's 0.8-µm channel-less architecture, CMOS-7 products use a self-aligned twin-well technology. The gate array chips are divided into I/O and internal cell areas. To isolate the internal cells from high-energy input signals, the I/O cell area contains input and output buffers. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design.

These transistors are sized to provide an optimum ratio of speed to silicon area.

The CMOS-7 series is supported by NEC's OpenCAD Design System. Aimed at reducing design cycle time and increasing the customer's control, OpenCAD lets NEC accept postlayout simulation results from customers and go directly to mask making.

Design kits supporting the CMOS-7 series are provided for use with Mentor Graphics on Apollo workstations; Valid Logic Systems on Sun workstations and PC platforms; and Dazix on Sun workstations and Daisy platforms.

CMOS-7 gate arrays are available in three package styles: PGA, QFP and PLCC. Pin counts range from 68 to 528. Prices range from 2¢ to 5¢ per available gate depending on quantities and package type.

Jeffrey Child

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CIRCLE NO. 78
Canon Laser Beam Printer Family

The Canon family of OEM Laser Beam Printer Engines comprises the largest installed base in the laser printer market. This success has been built on Canon’s well-documented reputation for reliability and low maintenance, innovation and high quality images.


As an OEM associated with Canon, you’ll work with a leader in laser technology and engine reliability. You’ll get the product and technical support you need to serve existing customers and respond to emerging market opportunities.

For more information, call 1-800-323-0766. Or write to Canon USA, Inc., OEM Operations, Printer Division, One Canon Plaza, Lake Success, NY 11042-1113.

Product specifications subject to change without notice.

LBP-LX Laser Beam Printer Engine
A compact, affordable printer engine ideal for desktop applications. Utilizes the disposable EP-L cartridge. Available in both Video (external OEM controller) and PCB (internal OEM controller) models.

- Monthly prints: 750
- Resolution: 300/400 dpi
- Print speed (PPM): 4
- Dimensions: 16.7”W x 14.1”D x 7.6”H

LBP-SX
The most popular laser beam printer in the world. Clamshell top cover permits easy access to paper path and disposable EP-S image cartridge. Available in Video and PCB models.

- Monthly prints: 5000
- Resolution: 300/400 dpi
- Print speed (PPM): 8
- Dimensions: 18”W x 19.5”D x 9.1”H

LBP-TX and LBP-RX

- Monthly prints: 5000
- Resolution: 300/400 dpi
- Print speed (PPM):
  - TX Simplex 8
  - RX Duplex 7 (impressions)
- Dimensions:
  - TX 18”W x 19.5”D x 12.5”H
  - RX 18”W x 25.0”D x 12.5”H

LBP-20
A heavy-duty laser beam printer for large-format printing. Modular design allows multiple product configurations.

- Monthly prints: 30,000
- Resolution: 300/400/480 dpi
- Print speed (PPM):
  - Simplex: Letter 20
    - 11” x 17” 10
  - Duplex: Letter 14 (impressions)
    - 11” x 17” 8 (impressions)
- Dimensions: 29”W x 24”D x 20”H

LBP-DX
Our largest-format laser beam printer. Outputs high-quality photographs, halftones and line art prints on vellum or paper. Ideal for engineering and graphics production. Handles 500-foot rolls of 24” wide paper or cut sheet sizes up to D (24” x 36”).

- Monthly prints: 5000
- Resolution: 400/508 dpi
- Print speed (PPM):
  - D size (24” x 36”): 3
  - C size (18” x 24”): 5
- Dimensions: 30”W x 39”D x 46”H
Controller moves PC architecture into embedded arena

The PC architecture is evolving into a control computer for embedded and real-time systems, not just for the Intel 80286 or 80386 found at its heart. As a result, users will be able to do a great deal of code development on standard PC-type platforms without the need for cross-compilation and debugging, which could greatly reduce application development time and cost.

Along these lines, Radisys has introduced a PC-compatible VMEbus controller, called the EPC-6, which can be used as a stand-alone control processor. The EPC-6 contains a 20-MHz 80386SX processor, an optional 387SX math coprocessor, up to 4 Mbytes of dual-ported DRAM, and 8 kbytes of battery-backed SRAM for storing critical data. It uses the ROMed version of Microsoft MS-DOS and includes a 16-kbyte instruction and data cache to increase performance for high-speed control functions. Radisys has taken advantage of the highly integrated, low-power core logic ICs that have been developed for laptop and notebook PCs to implement the architecture on a single VME card.

Flash memory the key

The EPC-6's 512 kbytes of flash memory is program storage, which is treated by the system as a solid-state disk drive, is key to its use in embedded applications. The drive can be formatted and downloaded with DOS-compatible files.

Most PC-based compilers generate code as relocatable .EXE files, and the disk format of the flash memory allows them to be stored and run in that format. Systems based on Intel CPUs, which use EPROMs for program storage, must first convert the code to a hex format with absolute addresses before it can be loaded into the EPROM and used by the system. The flash memory not only eliminates the need for this step, it makes it easier to dynamically download control programs and/or program changes directly from an attached PC or over a network.

The EPC-6 is implemented on a single-slot VME card. The VME interface includes master and slave capabilities, slot-1 controller functionality, and generation and receipt of all seven VMEbus interrupts. The controller also contains one EXMbuss expansion module slot. (The EXMbuss is an electrically compatible, but more physically compact, version of the AT bus.) The slot can be used for an Ethernet interface, VGA graphics support, extra RS-232 I/O, or a modem; VMEbus can then be used for high-speed I/O and communication with other real-time controllers.

Tailored to VME

In an embedded application, programs would normally communicate with the EXMbuss via DOS and BIOS calls, as would a normal PC. For VMEbus communications, Radisys supplies a library of software tools and modules, called EPControl, to allow system configuration, debug and communication via the VME backplane. Control applications communicate with the VMEbus either directly using the run-time library communication modules or via a real-time multitasking executive that can be loaded in memory. DOS does not participate in the real-time functionality of the EPC-6; it merely loads control programs and interfaces with ECM modules.

EPControl programs include configuration and set-up routines to establish I/O ports and format the flash solid-state disk. Debug software consists of a command line diagnostic program, called BusProbe, that allows the EPC-6 to manipulate the VME interface. It can read and write single addresses or blocks of VME memory, and manipulate interrupts and error signals. A standard DOS debugger gives access to the EPC-6 memory and I/O. The debug software can be invoked via a serial port or over the backplane.

The run-time software libraries can handle VMEbus interrupts, manage a VME window in local EPC-6 address space and do data transfers over the VMEbus. The libraries also support remote procedure calls (RPCs) to allow the EPC-6 to communicate in a multiprocessor environment. RPCs can take place over the VMEbus or serial I/O ports, or via Ethernet if an Ethernet card is installed in the bus slot.

The EPC-6 does not have a keyboard interface or on-board graphics display hardware. Application software development can take place in a number of ways. If the EPC-6 is being used in an environment that requires an embedded human interface, the computer supporting that interface can be used to emulate EPC-6 functions before the final code is downloaded to the EPC-6. Alternatively, a desktop PC can be used for software development up to the stage where it must be linked with the VME run-time library routines. It would then be transferred either by disk or Ethernet to an embedded PC with a human interface for final debugging and testing. The final system, however, will often contain only the EPC-6 and other VME cards that communicate via the EPControl software. Human access to such a system could then occur via serial ports or Ethernet, when needed.

The EPC-6 costs $1,995 in single quantities and $1,495 in OEM quantities.

---

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Circle 353
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Versatile I/O processor races at 10 Mips

Recognizing the need for fast I/O processing in systems using military interconnected buses, such as the Naval Tactical Data System and the MIL-STD-1553 Multiplexed Avionics Bus, Antares has developed a second-generation intelligent I/O processor for VMEbus environments. Based on a bit-sliced architecture, the board executes I/O operations at a 10-Mips rate. It can be tailored to service different I/O protocols simply by changing a piggy-back board containing bus-specific circuitry and PROMs with microinstructions set for the specific I/O protocol.

Capable of performing a variety of I/O-to-VMEbus transactions as either a VMEbus slave or master, the board makes virtually all VMEbus resources available to Antares’ microengine, which is at the heart of the board. Complete microcode drivers are provided on the board to simplify integration.

If users require a MIL-STD-1553 interface, for example, the microcode driver needed to handle that protocol is already resident. They merely have to install the proper piggy-back board and to provide the board with message-passing information.

Microengine heart of board

The Antares microengine, which is built around WaferScale Integration’s 2901 bit-slice processor, is made up of a 32-bit 2901 ALU, together with the 2910 microsequencer chip and microcode PROMs. The 32-bit ALU operates at a 10-MHz clock rate, resulting in the 10-Mips processing rate. A 32-bit 100-kHz real-time clock allows timing of I/O events with a 10-ms granularity. Combined with the fast PROMs, the design offers a highly programmable I/O interface path with the VMEbus interface.

All operations are controlled by microinstructions stored in 2 kbytes of fast, 64-bit-wide PROM. Each 64-bit word contains data, op-code and address information. Microinstruction pipelining is implemented to provide an additional speed boost. By always having the next instruction available, a PROM fetch cycle is eliminated.

Available now, the Antares I/O processor is offered on a single-slot 6U card. Prices start at $3,525.

Jeffrey Child
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CIRCLE NO. 80

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ABOUT S-BUS

S-Bus is on its way to becoming the standard mezzanine bus for Futurebus+. Motorola has already endorsed it for its Futurebus+ products and VITA is considering it as a standard mezzanine bus for Futurebus+

The advertiser's editorial copy will face its ad and provide a strong positioning statement.

- In total, a participant in the S-Bus advertising supplement receives a spread consisting of a full-page ad and an editorial positioning statement plus a 1/4th-page ad in the July-August S-Bus Showcase forums
- Reservations deadline is May 1, 1991
- Editorial and ad material by May 6, 1991
- Positioning of advertising will be at the discretion of COMPUTER DESIGN, with priority given to early commitments
- The back cover (in 4/C) will be available to a participant for an additional $5,000

ABOUT THE S-BUS ADVERTISING SUPPLEMENT

This supplement will open with a major editorial overview that discusses the opportunities and options S-Bus provides to today's technical decision makers.

Each participant will provide COMPUTER DESIGN with a full-page ad and editorial copy of approximately 900 words. This copy can detail whatever opportunities, benefits and predictions you choose. A black & white photo of the author (preferably your company's President, CEO or other high-ranking individual) will be included in the piece. Participants should also provide 40 words of copy for the July/August Showcase S-Bus forum.

The advertiser's editorial copy will face its ad and provide a strong positioning statement.

- In total, a participant in the S-Bus advertising supplement receives a spread consisting of a full-page ad and an editorial positioning statement plus a 1/4th-page ad in the July-August S-Bus Showcase forums
- Reservations deadline is May 1, 1991
- Editorial and ad material by May 6, 1991
- Positioning of advertising will be at the discretion of COMPUTER DESIGN, with priority given to early commitments
- The back cover (in 4/C) will be available to a participant for an additional $5,000

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SALES ENGINEER or SALES MANAGER demonstrated success with high-tech components, equipment, systems, datacom/telecom, networks, services. Distribution and direct sales experience in 15 Southeastern states, calling on management, engineering, specifiers, purchasing, BS-degree. Strong "hands-on" technical training/experience. Peter Alexander, P.O. Box 957111, Duluth, GA 30136 or call (404) 945-6950 (Atlanta).


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1991 UPCOMING ISSUES

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June 1 | Design synthesis | Mil-Spec standard buses — Warren Andrews | Op amps — Jeff Child
 | | Disk controller ICs | Multibus CPU boards — Jeff Child
July 1 | CASE for real-time programming | Mezzanine buses — Warren Andrews | DRAMs — Jeff Child
 | | Device modeling — Mike Donlin | Device programmers — Jeff Child
August 1* | Mixed-signal ASICs | Display controller ICs | Software-management tools — Tom Williams
 | | Barbara Tuck | CAD frameworks — Mike Donlin
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CIRCLE NO. 200

Computer Design May 1, 1991 149
As design engineers and managers you know that the higher speeds and greater complexity of electronic systems are making your jobs more challenging. As clock speeds climb to 50MHz and beyond, analog characteristics become major considerations for digital designs. In addition, demands for mixed-signal technology have increased in the consumer, automotive, and telecom markets. According to Technology Resource group, 40% of all ASICs will be mixed analog and digital by 1994.

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