How much can Design-for-Test reduce the need for testing?

A new long-word architecture could outshine RISC

DSP chips stalk industrial buses

16-bit MCUs diversify to survive
Who Said You Can't Have It All?

16 & 32-bit PROCESSORS
- Intel
  - 8088
  - 8088
  - 80286
  - 80386SX
- Motorola
  - 68000
  - 68010
  - 68020
  - 68030

STATIC & DYNAMIC MEMORIES
- 512K to 8 Mbytes
- Dynamic Memory Boards
- Universal EPROM/RAM
- Static Memory Boards
- System Expandable to 32Mb

COLOR GRAPHICS
- 640x480x256 Colors
- 800x600x256 Colors
- EGA
- VGA
- Touch Screen EL Display

ACCESSORIES
- Predecoded Prototyping Boards
- Terminal Strip Adapters
- Power Supplies
- Bus Extenders
- Packaging Products

MASS STORAGE
- 3.5" & 5.25" Floppy Disk Controllers and Drives
- ST506 Winchester Controller and Drives (up to 70 Mb)
- Intelligent SCSI Controller (up to 1 Gb)
- Tape Streamer

VISION SUBSYSTEMS
- 256 to 2048 Elements Linear CCD Cameras
- Matrix CCD Camera Interfaces
- Real-Time Image Processing Hardware

NETWORKING
- 10 Mb/s Ethernet
- 10 Mb/s X25
- 1 Mb/s GESNET
- 1 Mb/s Accnet
- 1 Mb/s IEEE 488
- 375 Kb/s Bitbus

INPUT/OUTPUT INTERFACES
- RS 232 / 442 / 485 SIOs
- Parallel TIL I/Os
- 10, 12 and 16-bit A/D & D/A
- Thermocouple, RTD, Resolver Interfaces
- Opto Isolated I/Os
- Mechanical & Solid State Relays

Whoever said that obviously doesn't know about GESPAC. With GESPAC, you get nearly 200 boards designed to work together, available under a single roof and backed by a team dedicated to your success. What's more, all of these boards are supported with two operating systems (MS-DOS and OS-9) a choice of Real-Time kernels, a choice of IBM PC or UNIX based cross development tools, and virtually one software driver for every board we make.

Call us today to receive the industry's most comprehensive catalog of microsystem solutions. See how GESPAC can help you build the system that best meet your unique specifications, in the shortest amount of time.

Call Toll Free 1-800-4-GESPAC or call (602) 962-5559.

USA - CANADA
50 West Hoover Ave.
Mesa, Arizona
85210 USA
Tel. (602) 962-5559
Fax. (602) 962-5750

EUROPE
Z.I. des Playes
83500 La Seyne France
Tel. 94 30 34 34
Fax. 94 87 35 52

INTERNATIONAL
18, Chemin des Aulx
CH-1228 Geneva Switzerland
Tel. (022) 794 3400
Fax. (022) 794 6477
Airflow
Adhere to the components that need cooling—the power supply and your boards. Separate chambers maximize cooling by channeling airflow and restricting recirculation.

The Last Word in System Packaging

Now you can benefit from 12 years of design experience and innovation that has made Electronic Solutions the industry leader in system packaging. The Omega™ Enclosures will give your VME or Multibus system the attractive exterior your image demands with a rugged, well-designed interior to withstand the most demanding environments. And besides the Electronic Solutions' full 3-Year warranty, the Omega bears FCC approvals and is UL, CSA, and TUV listed to get your system to an international market in the shortest time possible.

Call Electronic Solutions for the latest information about the best choice for your system package. It's the last system enclosure you'll need to see.

6790 Flanders Drive, San Diego, CA 92121
(619) 452-9333 FAX: 619-452-9464
Call TOLL FREE (800) 854-7086
in Calif. (619) 452-9333
CIRCLE NO. 2
Climbing takes skill, experience and teamwork. Reaching the top also takes leadership, forward thinking and focus. Since 1971, Standard Microsystems has applied this philosophy to the design and manufacture of standard and semi-custom integrated circuits.

Today, SMC’s engineering expertise and extensive SuperCell™ library, allows us to offer innovative and timely solutions to your unique application needs. Our portfolio focuses on networking and mass storage controller devices for the computer industry.

The next time you face a networking or mass storage challenge, call SMC. Discover how our cost-effective and technically superior products can help you climb ahead of your competition.

STANDARD MICROSYSTEMS CORPORATION COMPONENT PRODUCTS DIVISION

The Standard for LAN and Mass Storage ICs.

35 Marcus Blvd., Hauppauge, NY 11788 1516-273-3100 Fax (516) 231-6004

SuperCell is a trademark of Standard Microsystems Corporation.

CIRCLE NO. 3
Technology Updates

Integrated Circuits
New long-word architecture threatens to outshine RISC .................. 26
Denser, faster FPGAs encroach further on masked gate arrays ........... 30
Creative use of PLLs solves clock skew problem ...................... 40

Software
Industry group initiates object-oriented software standards ............. 46

Design and Development Tools
Speed and flexibility help PCB layout tools gain respect ................. 52

Computers and Subsystems
Fiber network supports distributed real-time systems .................. 60
Small, reliable STD SBCs move into PC territory ..................... 66

Technology and Design Features

DSP chips stalk industrial buses
Ripe for new roles, DSP chips are slowly making their way onto VME and Multibus boards. But system designers are tentative about the prospects .................. 73

16-bit MCUs diversify to survive
Seeking to secure their niche in the gap between cheap and powerful, 16-bit architectures take distinct approaches to meeting application demands .............. 83

Cover Story
How much can Design-for-Test reduce the need for testing?
Making a design functional and making it producible have been two different tasks. Now, test standards, tools and embedded circuitry move them closer together — and into designers' hands ......... 94

New Product Highlights

Product Focus
Standards breathe new life into 2,400-bit/s modem ICs .................. 117

Computers and Subsystems
VMEbus accelerator board offers 1.3M fuzzy-rule evaluations/s ......... 122
68040-based VMEbus board features intelligent I/O subsystem .......... 124

Software
VxWorks sports rewritten kernel, enhanced comm and windows features .............. 126

Design and Development Tools
New version of Abel tailored to device-independent design ............. 128

Open simulation system eases design of mixed-signal ASICs and ICs ........ 130

Integrated Circuits
C&T, Opti develop low-cost cache solutions for 386 chip sets .......... 132
Controller expands palette for color LCDs .......................... 134
Plessey joins digital synthesizer, I/O splitter .......................... 136

Departments

News Briefs .......... 8
Editorial ............. 12
Calendar ............. 16
Advertisers Index .... 144
For Designs That Demand a Lot of Memory,

When it comes to PCs, workstations, printers, and other computer-related products, end-users want smaller systems, maximum memory storage, and minimum power consumption. And they want it now. Which creates several problems for you. How do you reduce system size and power consumption yet increase memory capacity? And be first to market with your product? Oki offers some flexible solutions.

To begin with, our pin-for-pin compatible 4-Megs provide 4X the memory storage of a 1-Meg — without increasing space. Plus our 4-Megs have the lowest power consumption of any 4-Meg, making them ideal for laptops and other memory-intensive, power-hungry systems. Choose from a variety of packages too: DIP, SOJ, ZIP — and, later in 1990, an ultrathin TSOP, for even more space-saving advantages.

For higher density applications, select from Oki’s package-efficient family of SIMMs: 4-Megx8s, 4-Megx9s, and 1-Megx36s. Or we’ll work with you to design a custom SIMM that meets your unique specifications. All our 4-Megs and SIMMs are available now, so we’re ready to help accelerate your design time and your product’s time-to-market.

Call Oki today for qualification samples. See why so many companies are demanding Oki’s low-power, space-saving 4-Megs and SIMMs — and getting their leading-edge computer products to market so quickly.

Transforming technology into customer solutions
Demand Oki 4-Megs and SIMMs

### Oki's 4-Meg Product Line-Up

<table>
<thead>
<tr>
<th>Device</th>
<th>Organization</th>
<th>Access Mode</th>
<th>Speed Options (XX) Include:</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSM514100-XXYY</td>
<td>4M x 1</td>
<td>Fast Page</td>
<td>70 = 70ns (RAC)</td>
</tr>
<tr>
<td>MSM514101-XXYY</td>
<td>4M x 1</td>
<td>Nibble</td>
<td>80 = 80ns (RAC) 20ns (CAC)</td>
</tr>
<tr>
<td>MSM514102-XXYY</td>
<td>4M x 1</td>
<td>Static Column</td>
<td>8A = 80ns (RAC) 25ns (CAC)</td>
</tr>
<tr>
<td>MSM514400-XXYY</td>
<td>1M x 4</td>
<td>Fast Page</td>
<td>10 = 100ns (RAC) 25ns (CAC)</td>
</tr>
<tr>
<td>MSM514402-XXYY</td>
<td>1M x 4</td>
<td>Static Column</td>
<td></td>
</tr>
</tbody>
</table>

### SIMMs

<table>
<thead>
<tr>
<th>SIMMs</th>
<th>Organization</th>
<th>Access Mode</th>
<th>Speed Options (XX) Include:</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSC2341-XXYS8</td>
<td>4M x 8</td>
<td>Fast Page</td>
<td>70 = 70ns (RAC)</td>
</tr>
<tr>
<td>MSC2349-XXYS9</td>
<td>4M x 9</td>
<td>Fast Page</td>
<td>80 = 80ns (RAC) 20ns (CAC)</td>
</tr>
<tr>
<td>MSC2350-XXYS1P</td>
<td>1M x 36</td>
<td>Fast Page</td>
<td>10 = 100ns (RAC) 25ns (CAC)</td>
</tr>
</tbody>
</table>

CA Irvine 714/752-1643, Tarzana 818/774-9091, San Jose 408/244-9666 FL Boca Raton 407/394-6099
GA Norcross 404/448-7111 IL Rolling Meadows 708/870-1400 MA Stoneham 617/279-0293 MI Livonia 313/464-7200
NC Morrisville 919/469-2395 NY Poughkeepsie 914/473-8044 PA Horsham 215/674-9511 TX Richardson 214/690-6668

CIRCLE NO. 4
"All I'm doing is applying technology to solve the world human communications."

**HOW NATIONAL SEMICONDUCTOR IS HELPING YOU MEET THE CHALLENGES OF NEXT-GENERATION DATACOM AND TELECOM SYSTEMS.**

*Mike Evans*, National Semiconductor's Director of Strategic Applications, Integrated Systems Group, talks about applying high-performance VLSI solutions to communications problems.

**Achieving single-chip integration for IEEE 802.3 local area networks.**

"We're already a generation ahead in Ethernet chip design. We're the LAN market leader and the de facto standard in the industry. And now we've set a new standard in analog and digital integration with SONIC, for 'Systems-Oriented Network Interface Controller'. It combines a controller, an encoder/decoder, and a phase-locked loop onto a single chip that delivers a data rate of 10Mbits per second.

"It's the first device that implements all 802.3 network management functions. And the first capable of embedding the Ethernet control functions in 32-bit computer systems. High performance, low power, small footprint."

**Setting the pace for tomorrow's fiber-optic solutions with FDDI.**

"This is a quantum leap from Ethernet. Fiber Distributed Data Interface. It's the backbone of next-generation LANs. And it delivers at an incredible 100Mbits per second, and with an incredibly low bit error rate. We have a four-chip set, one in CMOS, three in BiCMOS. Our BiCMOS gives us the bipolar speed necessary for these data rates, with the CMOS density for high-speed logic functions. And we're already adding a fifth chip — a high-performance system interface. This is the frontier — and we're right on the edge of it."

**Creating the world's first analog programmable CODEC/filter.**

"Here's another example of how we're building on our leadership position. Our COMBO I, combined coder/decoder and filter, is already on nearly half of the non-captive analog linecards in the world. But the telecom market needs higher performance and more flexibility, so we've given
the world's most advanced
's most ancient problem:

them the COMBO II. Second-
generation, proven technology,
fully qualified, fully characterized,
in production. And it's the only
one in the world that is fully pro-
grammable for gain and hybrid
balance and time-slot assignment
and A- or µ-law...’

Bringing unprecedented
power and flexibility to
fax designs.

“If you think facsimile is ‘old’
technology, then you haven’t seen
our solution yet. Actually our
range of solutions — you can go
from low-end designs to high-end
designs without rewriting a single
line of code. Full 32-bit processing
power. Optimizing your fax func-
tions, but also allowing you to utilize
the processor for other functions
when it's not sending or receiving
faxes. So you can do PostScript
calculations, laser printing, network
management. Single chip, single
box, single company.”

Putting the pride of
National to work for you.

“'You know, communications
affects the whole world. But the first
step in communicating is over-
coming our natural reluctance to do
it. If I wanted to talk to communi-
cations experts, I'd call National.
That's where it starts.’

1-800-NAT-SEMI, Ext. 601
FPGAs make AT&T first
with complete ASIC line; Tl to follow suit

This month the first field-programmable gate array (FPGA) from AT&T (Berkeley Heights, NJ) will hit the market—with more expected in October and November—as the result of an agreement with Xilinx (San Jose, CA). That makes AT&T the first semiconductor vendor to offer standard-cell, gate array (through a recent agreement with NEC) and FPGA technologies.

On the first of next month, Texas Instruments (Dallas, TX) will become the second vendor to offer these technologies when it begins shipping FPGAs as a result of its agreement with Actel (Sunnyvale, CA). TI, in fact, will be the first to offer standard cells, gate arrays, FPGAs and PALs.

With ASIC designers looking to prototype with FPGAs and explore implementation trade-offs, it's likely that other semiconductor vendors will be scrambling to expand the breadth of their product offerings. They'll be motivated not only by a desire to gain a piece of the action in FPGAs, but also by the fear of losing market share to a competitor that's migrating from one ASIC technology to another. —Barbara Tuck

IBM and Sun settle
RISC patent dispute

IBM (Armonk, NY) has recently cast a long shadow over the RISC-based processor vendors. The giant has reviewed the patents resulting from John Cocke's pioneering mid-'70s work on the 801 computer project, and concluded that a number of RISC vendors were violating IBM patents. The potential implications for the industry are, of course, enormous.

The first company to publicly respond to the IBM initiative is Sun Microsystems (Mountain View, CA). Sun has entered a cross-licensing agreement with Big Blue that will result in the workstation vendor paying royalties to IBM, presumably for revenues on Sparc products. It remains to be seen whether the Sun agreement will cover other companies that produce Sparc-based products. And an even bigger question looms over the fate of vendors that have created other RISC architectures—some of whom may choose, for financial or political reasons, to resist IBM's claim.

—Ron Wilson

IEEE takes another
shot at the VHDL standard

A working group of the IEEE Computer Society has once again begun the task of producing a standard VHDL Language Reference Manual. Under IEEE regulations, an institute standard must be recertified every five years, and time is growing short for the original VHDL document, which was issued in December 1987.

The working group, laboring under the catchy title VHDL Analysis and Standardization Group (VASG), must produce a definition of language requirements and a language design, and then submit the results for balloting. They expect the balloting to begin in the fourth quarter of 1991.

Unlike the original round of VHDL work, which was driven primarily by the U.S. Department of Defense, the new version will include thoughts from European and Japanese sources—at least that's what VASG hopes. To this end, the group has included precisely one non-U.S. company in the membership of its six-member steering committee—Given this overt and the overwhelming indifference that European and Japanese managers have shown toward VHDL in the past, one is perhaps less than optimistic about the internationalization of the language.

—Ron Wilson

Futurebus+ profiles:
everyone wants one

One of the big virtues of the Futurebus+ specification is that it allows for an unlimited number of profiles, or physical/electrical implementations. First came the A profile, strongly backed by the VME Industry Trade Association.

Then Digital Equipment Corp (Maynard, MA) came along with its own ideas. DEC pushed the Futurebus+ working group into adopting an I/O-only profile of the bus—profile B. VITA has subsequently adopted both the A and B profiles. In addition, a profile for a desktop version of Futurebus+ has reached the status of a working group.

But neither the A nor the B profile dictates how fast the bus should run—it's implementation-dependent. John Theus at Tektronix (Beaverton, OR) believes a profile should exist that specifies minimum performance; he's now heading up a working group for a profile F—for fast. Profile F, now raised to the status of a working group, is looking to develop a specification for a bus with a minimum transfer rate of 500 Mbytes/s.

At the same time, the Navy (one of the movers in the early adoption of Futurebus+), decided it should have its own profile, and so has come up with a profile M—for, guess what? The Navy's looking at SEM E (approximately 6 x 6 in.) and SEM F (6U x 160) board sizes.

And not to be left out, the telecom makers, headed by Ameritech (Rolling Meadows, IL), are looking for their own profile T, which will probably fit on some larger-sized card to accommodate all the redundancy that will certainly be part of the profile. Both the M and T profiles have been raised to working-group status. —Warren Andrews

Mixed-signal ASIC market
to explode in the '90s

The Mixed-Signal ASIC Market Study recently released by Electronic Trend Publications (Saratoga, CA) reports that total worldwide sales for mixed-signal ASICs will increase from $557 million in 1989 to $2.8 billion by 1994, with the United States forecasted to hold the lead. While continuing to be the largest market sector, telecommunications will absorb a smaller portion of the total, with roughly 30 percent of the mixed-signal ASICs (down from 35 percent in 1989) going into modems, fax machines and LANs. Consumer, medical and automotive markets will be the fastest growing and will account for 28 percent of

(continued on page 10)
A One-Sided Comparison Between Synergy's SBCs and All the Others.

**Speed**

At up to 50 MHz and 20,000+ Dhrystones, Synergy VME and Multibus I 68030 SBCs are the undisputed speed leaders. Performance like this can only be matched by the newest RISC processors, but our SBCs are available now—with no software compatibility problems.

Process math at up to 30 MFlops with our optional floating point coprocessors, or, for memory intensive applications, add up to 32M bytes of DRAM and/or up to 2M bytes of zero wait-state SRAM.

If you have the need for speed, you need to call Synergy.

**Application Matching**

*Write your own I/O ticket!* We have an unbeatable list of features and options to exactly match whatever I/O requirements your project needs. *Real I/O choices,* with advanced intelligence, including Ethernet, X.25, SCSI and more than a dozen others are immediately available off the shelf—and if you don’t find exactly what you need, we design to order with unbeatably low NREs and fast turnaround.

If you’re still looking for an SBC that’s a perfect match, you need to call Synergy.

**Proven Support**

In the past four years, we’ve shipped thousands of Multibus I and VME SBCs to Fortune 500 companies and they keep coming back to us with their new projects. That’s because of our *top-flight engineering assistance, our on-time delivery and near perfect reliability record.* A record we think is so good, we’ve introduced an extended *3-Year SBC Warranty.*

If you need a Multibus or VME manufacturer you can count on, you need to call Synergy.

CIRCLE NO. 6

Call now at (619) 753-2191. We can FAX you the facts today!

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 (619) 753-2191 FAX: 619-753-0903
WinSystems breaks price barrier with STD PC

Amidst the mad rush for higher performance and more features, at least one company is turning the other way, making a low-cost, PC-compatible STD Bus-based board as an inexpensive drop-in solution for many embedded-control application problems.

Designed to operate either as a stand-alone single-board computer or as a host CPU supporting additional STD Bus I/O cards, the new board from WinSystems (Arlington, TX) is designed to sell for under $200 in OEM quantities, making it one of the lowest-priced PC-compatible single-board computers.

Although the new board doesn't have the sparkle of the company's full-featured 286- and 386-based versions, it has enough performance and I/O to tackle a variety of control applications normally relegated to far more expensive devices, according to Bob Burckle, WinSystems vice-president. The board is based on NEC's V40 processor and features three memory sockets for up to 1 Mbyte of storage.

—Warren Andrews

TI seeks to license new 3-D display technology

Texas Instruments (Dallas, TX) is looking for partners to help develop this year. Objectivity/DB has already made inroads into the CAD marketplace, particularly since being adopted by Valid Logic Systems (San Jose, CA) as the OODBMS for its Design Process Framework.

—Mike Donlin

New RAMDAC enhances VGA resolution

Image quality of VGA color displays can be enhanced with an anti-aliasing RAMDAC jointly developed by Edsun Laboratories (Wal­tham, MA) and Analog Devices (Nor­wood, MA). The digital-to-analog converter, called a continuous edge graphics D-A converter (CEG/ DAC), comes in a triple 6-bit version; a triple 8-bit version with a 256 x 24-bit color lookup table; and a version with a 256 x 18-bit color lookup table. All are completely VGA- and PS/2-compatible.

With only a modified software driver, the D-A converters can look at the transition between two screen colors and place interpolated color values into the pixels along the edge so that the eye perceives a smooth line without "jaggies." An­alog Devices claims that a 320 x 200-pixel VGA display has an apparent resolution enhancement of 1.280 x 1.024 pixels. But no additional information is on the screen, as there would be with an actual in­crease in pixel resolution. The parts are pin-compatible with RAMDACs now used in VGA graphics board designs.

—Ron Wilson
SCSI-2 is at your command with Rimfire 6600 Series Parallel Disk Array Controllers.

Discover unmatched performance and data integrity for mass storage applications—the Rimfire 6600 series of Parallel Disk Array (PDA) Controllers. The first array controller offering SCSI-2 as its host interface, as well as the first offered as a board level product, the Rimfire 6600 Series supports four data drives plus a single redundant drive. Because all disk data transfers occur in parallel, the array appears to

the host as a single SCSI drive. For you, that means excellent performance. Transfer rates and capacity four times that of an individual drive. And exceptional data availability.

In addition, the flexibility of the PDA controller allows the OEM to select drives from many vendors. It's compatible with SCSI, operates with off-the-shelf host adapters and is priced significantly lower than other solutions of equivalent capabilities.

For detailed information on the Rimfire 6600 Series, or other SCSI-2 compatible products, call Ciprico, the industry leader in technology, technical support, customer service and respondability at 1-800-SCSI-NOW (1-800-727-4669). European customers call our United Kingdom office, (0703) 330 403.

CIPRICO
2955 Xenium Lane
Plymouth, MN 55441

CIPRICO LISTENS. AND RESPONDS.

CIRCLE NO. 7
Touting our uniqueness

This issue of Computer Design boasts a new look. Or the cover, at least, boasts a new look. While we have a lot of fun coming up with the ideas for covers, we didn't change the look of the cover just for fun. We changed it because we had something to say.

For a few years now, Computer Design's covers have borne some variation of the tag line “The first magazine of system design, development and integration.” A magazine's tag line is intended to summarize, in as few words as possible, what's at the heart of the magazine—its reason for being, if you will. The words “The first magazine of system design, development and integration,” emphasizing our focus on hardware design, software development and hardware/software integration, accomplished just that. The problem, however, is that there are other publications, some of which you may receive, that cover much of the same territory.

Having conceived Computer Design 30 years ago, we like to believe that we were the first publication to tackle the hardware, software and hardware/software integration problems associated with the design of computer-based systems. Today, most of those systems are microprocessor-based, and Computer Design has stayed in synch with this evolution, bringing its system-level viewpoint to bear on the design of all sorts of products based on microprocessors and other ICs, single-board computers and even OEM computers. And while the tag line “The first magazine of system design, development and integration” defines the subject matter we cover, it doesn't say anything about how we cover it.

The many publications that serve your information needs fall essentially into three categories. On one hand, there's news, which provides the fundamental information of who, what, when and where. On the other hand, there's “how-to” editorial, which provides implementation-level detail. And then there's what we like to call “why-to” editorial. In contrast to news and how-to, why-to editorial attempts to make comparisons, place options and trade-offs in perspective and provide some insights into technology and design directions.

As a regular reader, you already know that Computer Design is firmly in the why-to category. That's what makes us unique, and we've decided to start touting that uniqueness. The key part of our new tag line, “Technology and design directions,” is what why-to editorial is all about. And just as why-to editorial and technology and design directions are an integral part of our editorial approach, we've now made technology and design directions an integral part of our masthead.
"THEY LAUGHED WHEN WE PLUGGED A PC IN OUR VME SYSTEM..."

"The pressure was on. Shorten our design cycle. Cut our software costs. Deliver the "gee-whiz" features customers wanted. But the old solutions weren't working. We needed a new approach. **We looked to the PC.** Others looked at us like we were nuts. They sent memos. *"The PC is not a real computer."* ... *"Not enough horsepower"* ... *"Just a pretty user interface"* ... *"It can't survive that environment.* **But the PC is going places.** Over 40 million are in use; 4 million in industrial environments. Another 1.4 million are expected on the plant floor this year. From the moment we plugged in a RadiSys Embedded PC, we understood why. **Software for PCs is abundant and inexpensive.** We had two dozen software houses fiercely competing to sell us high quality, man-machine interface software. Why should we reinvent the wheel? For multi-tasking operating systems, we could choose from Windows 3.0, OS/2, UNIX, VRTX—all with integrated VMEbus support from RadiSys. There is a wealth of development tools available to shorten design time. No wonder the PC is the world's most popular software development host. And PC-based networking is light-years ahead. **PC versatility is unmatched.** We can give customers what they want, right now. More options. Proven features. Everybody knows how to use the PC, our own team and our customers. And it's a sure bet that future application programs, languages and OS standards will run on it. **PC horsepower is up there.** The new Embedded 386 and 486 PCs have more than enough power to handle our mix of user interface and control functions. **We got the best of both worlds.** Plugging a RadiSys Embedded PC directly into the VMEbus gave us the full performance, ruggedness and reliability of the VME form factor, plus all the PCs software advantages. **You know the rest of the story.** That Embedded PC has the whole company laughing. All the way to the bank."

**Join the party!** Call RadiSys at 800/950-0044 (fax requests: 503/690-1228) for a catalog of Embedded PC Products and brochure "Open New Windows of Opportunity With Embedded PCs."

**RadiSys CORPORATION**

The Inside Advantage

19545 NW Von Neumann Dr. Beaverton, OR 97006 USA
(800) 950-0044
(503) 690-1229
Fax (503) 690-1228

Copyright ©1990 RadiSys Corporation, Inc. All rights reserved. EPC is a registered trademark and RadiSys is a trademark of RadiSys Corporation. Windows 3.0 is a trademark of Microsoft Corporation. OS/2 is a trademark of International Business Machines Corporation. UNIX is a registered trademark of AT&T. VRTX is a registered trademark of Ready Systems, Inc. 386 and 486 are trademarks of Intel Corporation.

CIRCLE NO. 8
Signetics. Because today's tomorrow's communication.

Philips Components
remote possibilities are on the horizon.

FOR DESIGN INNOVATIONS, YOU NEED A FULL-SYSTEM SUPPLIER WITH NO STRINGS ATTACHED.

When it gets down to the wire, there's no better solution for your telephone, cellular, wireless or computer connectivity designs than Philips Components-Signetics.

We offer a complete range of high-performance ICs to tackle your ever-changing needs.

For compact radio designs, choose from a complete range of RF products. Including RF amplifiers, mixers and IF stages. As well as our fully programmable, low-power synthesizer with an RF divide from 400 MHz to over 1 GHz.

Plus there's our fully integrated cellular chip set. It includes demo-boards, software and software support and is the only complete solution for designing cellular radio applications. With it you can reduce the size of your portable product by reducing your chip count by up to 90%.

And for advanced feature phones, we offer a complete telephone solution including transmission circuits and feature circuits.

Or for high-speed computer connectivity there's our advanced Ethernet® chip set and 100 Mbit fiber optic transceiver chip set. We also offer ICs that handle all popular protocols, including DUSCCs and UARTs.

We're building a broad base of state-of-the-art products utilizing our advanced, world-class BiCMOS process QUBiC. Combining the best features of Bipolar and CMOS, we're now creating new classes of high-performance devices within all our product families.

Each communication IC is an example of how Philips Components-Signetics is designing smarter devices to meet tomorrow's needs. Including the need for military products. So whether you're designing your first product or a new generation of products, remember that at Philips Components-Signetics we always keep the lines of communication open. Call now for your communications brochure: 800-227-1817, ext. 714AF.

Ethernet is a trademark of Xerox Corp.

Signetics
EXTENDING THE DIMENSIONS OF PERFORMANCE
SCHEMA MEANS PERFORMANCE

Over 15,000 engineers have chosen SCHEMA CAE products. Why? SCHEMA products offer the most power, the features, ease of use, and support that serious designers need...at an affordable price.

SCHEMA III, a powerful PC-based schematic capture system with workstation features such as unlimited hierarchies, smooth pan, direct PCB interface, AutoCAD DXF block output, 7000+ unique part library & extensive DRC's. Not copy protected. $495 worldwide!

SCHEMA PCB board layout tool with autoplacement, autorouter, graphic and manufacturing output options. 3,500+ part library. Act now and receive PCB, with Autorouter & Photoplot output for only $1495, a savings of over 20%!


SCHEMA SUSIE interactive logic simulator. Verify design in unit delay mode or actual timing to 10 picoseconds for TTL, CMOS, MPU, PLD and other devices. Auto test vector generation. From $995

FREE DEMO DISKS
FREE 1-800 SUPPORT
30 DAY MONEY BACK GUARANTEE
1-800-553-9119

CALENDAR

September 25-28
Embedded Systems Conference
Hyatt Regency, San Francisco Airport. ESC will offer 75 lectures and workshops, as well as an exhibition of embedded development products. Industry leaders will discuss topics such as improved product design, efficient code and effective product management. Information: Anne McAdams, Software Development Seminars, 500 Howard St, San Francisco, CA 94105, (415) 995-2472.

October 15-18
Buscon '90-East
Royal Plaza Trade Center, Marlborough, MA. This conference for bus board and systems-level technology will highlight issues and applications for embedded-systems programming, VME, Multibus II, PC bus platforms, emerging architectures and military applications. The exhibit will include over 200 booths featuring board- and systems-level components and software. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856, (203) 852-0500.

November 6-9
Software Development '90-Fall
Omni Parker House, Boston, MA. The conference will offer over 60 lectures and workshops in four areas: object-oriented programming, management, design methodologies and C language. An exhibition of software and development products and services will also be featured. An optional one-day seminar will focus on how to build, organize and manage more-effective project teams. Information: Software Development Seminars, 500 Howard St, San Francisco, CA 94105, (415) 995-2472.

November 13-15
Wescon
Anaheim Convention Center, Anaheim, CA. This year's conference will offer 36 technical sessions, 22 tutorials, a panel addressing professional concerns, and over 1,000 exhibits. A special exhibit will demonstrate the state-of-the-art in PC-based design tools. Also featured will be a panel of industry leaders discussing the interdependency of the world electronics market. Information: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668.

November 14-16
PROCIEM '90
Hyatt Regency Westshore, Tampa, FL. "Surviving in the '90s: CIEM in a New World Marketplace" is the theme of this year's conference on Productivity through Computer-Integrated Engineering and Manufacturing. The technical program will include panels on industrial applications in CIEM and NFS strategic marketing initiatives. Sessions will address issues of flexible manufacturing and knowledge-based systems, and design for manufacturability. Information: PROCIEM 90, Box 25000, Orlando, FL 32816-0177, (407) 249-6100.

CIRCLE NO. 9

FREE DEMO DISKS
FREE 1-800 SUPPORT
30 DAY MONEY BACK GUARANTEE
1-800-553-9119

OMATiON
CIRCLE NO. 9

16 SEPTEMBER 1, 1990 COMPUTER DESIGN
Motorola made us do it.

They made us an offer we couldn't refuse. They wanted our ES 1800 development system to support their new 68302 Integrated Multiprotocol Processor. Naturally, we jumped at the offer.

Which gives you a big jump on your competition. Because now you can put the ES 1800 to work debugging your design today, instead of waiting months for other development tools to roll out.

And the ES 1800 system flies at maximum-rated clock speeds. With a full set of tools to support the 68302's special features, including three serial controllers, seven DMA channels, and chip selects. Plus complete software development tools and host support.

What's more, we offer training, installation, and application assistance. All to save you time and money. All to bring your design to market faster. Just as Applied Microsystems has done with more than 12,000 systems worldwide.


Oh, and don't forget to thank Motorola.

© 1990 Applied Microsystems Corporation, P.O. Box 97002, Redmond, WA 98073-9702 USA. All rights reserved.


CIRCLE NO. 10
Fishing for a Video Display Board?

Catch the most powerful video options for your VME image display applications. Gang boards in parallel, program any sync waveform, even gen-lock to external video!

- 8 or 24 bit pixels
- Any frame size up to 2048x1024
- Programmable sync: RS343, RS170 or other
- Support software
- Pixel rates to 125 MHz
- 1 bit overlay plane
- Color or monochrome

Part of the Io family of high performance CPUs, computational and graphics products.

**486 25MHz**

**386 25/33MHz**

**SINGLE BOARD / AT COMPUTERS**

**80486-25MHz**
- 25MHz 80486 CPU w/Internal CACHE & Co-Processor
- Up to 16Mb of SIMM Memory
- 8KBytes of Internal CACHE
- 128Kb or 512Kb Secondary CACHE Daughter Cards Available
- 2/4 Way page Interleave Memory
- BIOS Shadowing
- Reset/Speaker/Keylock Connector
- ROM Based Utilities
- On-Board Lithium Battery

"19 Years of Quality Service"

**80386-25MHz**
- Up to 25MHz CPU w/CACHE
- Up to 8Mb of RAM Memory
- Supports up to 20Mb with DTI's
- Memory Daughter Card
- Optional 80387 Math Co-Processor
- Multi-Function I/O Cards Available

**80386-33MHz**
- 33MHz 80386 CPU
- 32,64 or 128Kb of CACHE
- 6 or 8MHz Bus Speed
- Up to 32Mb RAM
- COM 1 & COM2 (Up to 115Kb)
- LPT1 w/Bidirectional Mode
- Up to 2 Floppy Drives
- Future Domain Compatible SCSI Port
- PS/2 Mouse Port
- IDE Disk Drive Port
From any point of view, this 5 1/4" disk drive reflects Hitachi's superior technical expertise, high-performance, and quality. The DK515 features a fast 2.46 MB/sec. data transfer rate, an average access time of 16 ms, and a choice of ESDI, SCSI, or ESDM interfaces.

Like all Hitachi drives, the DK515 reflects quality, because all critical components—including heads, media, and servo systems—are designed, engineered, and manufactured by Hitachi.

Then, to make sure that Hitachi's strict standards of excellence are maintained, each and every drive is 100% burned-in and tested. The final result: a clear reflection of Hitachi's commitment to providing the very best in reliable, high-quality, high-performance disk storage. All this from a $48 billion company.

Available now!

For more information about Hitachi disk drives, call your local Hitachi Distributor listed below, or Hitachi at 1-800-283-4080, Ext. 877.

Hitachi America, Ltd.
Computer Division, MS500
Hinachu Plaza
2000 Sierra Point Parkway
Brisbane, CA 94005-1819

HITACHI
Our Standards Set Standards

Authorized Distributors
CONSAN 612-949-0053
(IL, IN, KS, KY, MI, MN, MO, ND, NE, OH,
Pittsburgh, PA, SD, WI)

GENTRY ASSOCIATES
800-877-2225
(AL, AR, CO, GA, LA, MD, MS, NC, SC, TN, VA)

R SQUARED 800-777-3478
(AZ, CA, CO, NM, OR, UT, WA, WY)

SIGNAL 800-228-8781
(CT, MA, ME, NH, RI, VT)

SPECIALIZED SYSTEMS
TECHNOLOGY 800-688-8993
(AR, LA, OK, TX)

CIRCLE NO. 15
MC68040 25-33MHz: 20MIPS. 3.5MFLOPs at 25MHz. Integral FPU, 2 x 4Kb Caches
2-16Mb DRAM onboard, Dual banked, Multiported to CPU, VME, VSB and LAN
Segmented Memory Protection for VME/VSB access
VME Rev C IEEE1014:
- System Controller
- Interrupter and handler
- 16 vectored interrupts
- DTB Master/Slave
- BLT transfers • 4Kb Mailbox
VSB Master/Slave
- Interrupter and handler
- 16 vectored interrupts
Ethernet IEEE802.3 with 32bit DMA Controller
128Kb to 2Mb EPROM in 2 JEDEC sockets
2 x RS232 • 4 x CIO • 12 x Counter/Timers
Software support includes:
- pSOS+™ Velocity • VxWorks
- TP-LX/68K V.3.2 implementation of UNIX

If you would like information on these, or any other Tadpole products, call us TOLL FREE on:
1 800 232 6656 for US enquiries
For European enquiries contact:
Tadpole Technology plc
Cambridge Science Park
Milton Road
Cambridge CB4 4WQ
ENGLAND
Tel: 0223 423030
Fax: 0223 420772
Tadpole Technology SA
44 Avenue de Valnons
77210
Avene Fontainebleu
FRANCE
Tel: 331 60 72 50 60
Fax: 331 60 72 51 11

Ethernet is a trademark of the Xerox Corporation
MC68040 is a trademark of Motorola Inc
IEEE802.3 is a trademark of Software Components Group
pSOS+™ Velocity is a trademark of Ready Systems
VxWorks is a trademark of Wind River Systems Inc.
40 BY TADPOLE

MC68040

TP40V VERY HIGH PERFORMANCE SINGLE BOARD VME COMPUTER

- MC68040 25-33MHz: 20MIPS, 3.5MFLOPs at 25MHz, integral FPU, 2 x 4Kb Caches
- 2-32Mb Exchangeable DRAM Module, Dual banked, quad-ported to SCSI, VME, LAN and CPU
- VME Rev C IEEE 1014:
  - System Controller
  - Interrupt handler
  - 4Kb Mailbox
  - DTB Master/Slave
  - BLT transfers
- SCSI interface on P2. 32bit DMA and NCR 53C90A achieving sustained data transfers up to 4.5Mb/sec
- Ethernet IEEE802.3 with 32bit DMA Controller
- RTC with 2Kb SRAM
- 8bit user I/O
- 2 x RS232, 2 x C/I/O
- 6 x Counter/Timers
- Software support includes:
  - pSOS
  - Velocity
  - VxWorks
  - TP-IX/68K V3.2 implementation of UNIX

CIRCLE NO. 19

Tadpole Technology
We're widening the scope of hard copy recording.

Raytheon has added a series of wide “flatbed” models to its quality line of thermal hard copy recorders. The new TDU-1950F and TDU-1200F units, in 19.5 inch (49.5 cm) and 12 inch (30 cm) configurations, respectively, provide enhanced vertical integration of data for a broad range of specialized applications.

The flatbed models join Raytheon’s established family of “free fall” thermal recorders – the TDU-850, with an 8.5 inch (21 cm) printing width, and the TDU-1200, with a 12 inch (30 cm) printing width.

Raytheon’s thermal recorders produce high resolution copy at high speeds and can generate full tonal images up to 256 multi-shade levels of true grey. Alternately, they can display digital data in crisp graphic or alphanumeric form using an optional IEEE 488 interface.

Traditional uses include CRT hard copy, military surveillance, spectrum analysis, LOFAR gram displays, ultrasonic production control, and facsimile transmissions. New and evolving applications include support for computer assembly testing and chromosome analysis in genetic research.

TDU’s print on paper, plastics or transparencies. They feature clean, odor-free, maintenance-free operation.

Make hard copy easy with today’s most versatile and reasonably priced thermal recorders. Call or write Marketing Manager, Production Components, Raytheon Company, Submarine Signal Division, 1847 West Main Road, Portsmouth, RI, USA 02871-1087. Phone 401 847-8000.

Raytheon
Much has been written about RISC's superiority over CISC. Many authors, myself included, have espoused the inherent strengths of RISC's instruction-set architecture—strengths that are now leading to rapid market share growth for RISC at the expense of CISC. Without exception, however, the many articles written about RISC from an applications perspective have been incomplete and somewhat disjointed. This is unfortunate, since the applications perspective is, in fact, the perspective of the end user.

The real question to be addressed isn't, "Which applications will RISC architectures penetrate?" but rather, "At what rate will RISC penetrate applications currently using CISC?" It's possible to break down the latter question along structured lines, first by reviewing the applications currently served by CISC architectures, and then by discussing the current and projected associated levels of penetration by RISC architectures.

RISC has penetrated five major applications areas to date: large-scale central processors (mainframes, supercomputers and massively parallel computers); medium-scale central/node processors (minicomputers, servers and fault-tolerant on-line transaction-processing systems); small-scale personal processors (desktop and laptop systems); embedded control for computer peripherals (laser printers, copiers, high-end disk and tape control, datacommunications control, X-terminals, circuit switching, add-in boards, imaging and graphics control); and specialized embedded control (automotive systems, such as engine control and antilock braking; cellular phones, pagers and telephone handsets; smartcards; cameras and other consumer electronics goods; and robotics).

Least obvious market

Large-scale central processors are the least obvious applications to be penetrated by RISC. That's because the majority of the revenue in this area currently comes from sales of IBM's mainframes and the IBM plug-compatible mainframes, and the IBM machines are modeled on a classical CISC architecture. Nonetheless, RISC has already begun to reshape the mainframe market, both through market dynamics and through architecturally transparent applications software methods.

Many market researchers have stated that growth in the classical mainframe market has slowed over the last 10 years to the point of virtually stopping. Much of this slowdown can be attributed to the change in computing away from batch processing on isolated, centralized mainframes and toward interactive computing on client-server networks. In this new computing structure, client systems (small-scale systems such as personal computers and workstations) are networked to server systems (such as file servers, network servers and compute servers), and almost all new growth in new applications is occurring at the client-system level.

Recognizing this fundamental change, mainframe manufacturers first attempted to reposition their systems as central file servers, but purchasers responded with mixed interest. Like all value-conscious consumers, these purchasers wanted to maximize price/performance and utility within their budgets. With amazing frequency, companies that would normally have purchased CISC mainframes for their central file servers chose high-end RISC-based computers instead.

So manufacturers of classical CISC mainframes are now responding to the price/performance assault of high-end RISC-based servers by themselves moving to RISC. The mainframe manufacturers, however,
must strive to keep binary compatibility so that they can keep their customers locked into their proprietary application software bases. CISC mainframe manufacturers, therefore, have begun the move to RISC by using RISC technology at any and all points within the mainframe where this can be accomplished in a transparent manner. This hybrid approach, however, is less cost-effective and will lose market share in the long run.

Unlike the mainframe market, the market for medium-scale central/node processors has been conspicuously penetrated by RISC. Such mainstream medium-scale system suppliers as IBM, Digital Equipment Corp and Hewlett-Packard have already introduced, or will introduce in the next 18 months, RISC-based systems that significantly overlap their CISC products. In addition to offering more aggregate performance than their CISC products, these vendors' RISC products have price/performance ratios that are 5 to 100 times better than those of their CISC offerings. But IBM and DEC, when their RISC systems are fully in place, may find themselves facing the precarious situation of potential revenue collapse, since they replaced expensive low-performance systems with significantly less expensive high-performance systems.

Besides IBM, DEC and HP, many other, more-aggressive companies have targeted the medium-scale computing area. These companies realized right from the start that systems based on inexpensive, commercially available RISC microprocessors would dramatically out-price and out-perform proprietary CPU architecture-based systems. They're all rapidly moving to RISC, having designed their systems with an open architectural migration in mind. Companies in this category include Sun Microsystems, which is developing a RISC central file server; Sequent Computer Systems, which is developing a RISC multiprocessor database server; and Solbourne Computer, Stratus Computer, ICL and Pyramid Technology, which are producing RISC multiprocessor servers. This list is by no means exhaustive, but it's significant that all of these vendors have endorsed RISC.

From a segment market share perspective, more than 75 percent of medium-scale central/node processors will be served by RISC architectures by 1995.

**Aggressive growth predicted**

Several market researchers reported this year that small-scale computers have become the single largest revenue-producing segment of the entire computer industry. Coincidentally, this segment produces the largest amount of aggregate revenue for suppliers of 16-32-bit CISC VLSI semiconductor products if one takes into account both the shipments of microprocessors and the shipments of all the central processor chip set functions: integer and floating-point units, memory-management units, cache control and first-level cache subsystems.

To date, the aggregate of RISC system unit shipments has amounted to less than 1 percent of the total system shipments within this segment; but this situation is changing rapidly. According to Ross Technology, RISC system shipments as a percent of the total small-scale system shipments segment are estimated to grow by more than 5 full percentage points annually for the next 10 years, resulting in RISC systems' constituting over 50 percent of the small-scale systems market segment by the end of the decade.

**Several factors play a role**

There are six factors facilitating the rapid market share gains of RISC system shipments in this market segment: the saturation and maturation of the IBM-compatible PC industry; the IBM-compatible industry's reliance on Intel's proprietary CPU architecture; the adoption of RISC by nearly all of the major computer manufacturers; the advent of open RISC architectures; the movement of RISC systems to the desktop; and the availability of shrink-wrapped RISC software.

As the IBM and compatibles PC industry nears its tenth year of existence, it's clear that this industry's growth rate has slowed dramatically and that profit margins have been strained accordingly, resulting in an inevitable industry shakeout. The majority of IBM PC and compatible suppliers' market share has coalesced around less than 10 companies. As a result, new companies aren't participating in this market subsegment and are migrating to RISC.

Regarding the second factor, the 80386 and 80486 processor introductions demonstrate Intel's strategy to provide the market with sole-sourced, proprietary microprocessor products. While this approach ensures Intel extraordinary profits in the short term, it also results in lost profits (and lost reinvestment potential) for IBM-compatible manufacturers, whose system selling prices are determined and strictly limited by the market. Intel's strategy also serves to stifle competition and innovation; system vendors are unable to differentiate themselves by producing various 80X86 implementations. The end result is that Intel's strategy is facilitating a more rapid adoption of RISC than might naturally occur.

In fact, there can be no more clear evidence of the movement toward RISC than the wholesale adoption and endorsement of RISC by nearly every major manufacturer of computer systems. In the context of small-scale computers, this movement in itself is a facilitator of the further adoption of RISC architectures by this segment. In other words, offering RISC systems in this market segment is quickly becoming a market requirement.

The availability of open RISC architectures in general, and Sparc in particular, will lead to "microarchitectural" competition: that is, many microprocessor suppliers will be designing RISC implementations in parallel. This explosion in innovation dramatically benefits not only the small-scale market segment by providing system suppliers with multiple, binary compatible choices for the system CPU, it also benefits the other market segments discussed in this article, as there will be a natural market segmentation among microprocessor designs. The combined R & D investment of suppliers designing to open RISC architecture standards is quickly beginning to dwarf the investment that is affordable by proprietary microprocessor suppliers.

Within the past 12 months, the industry has seen the introduction of RISC systems priced for the mass market. Though the majority of these products are in
These vendors claim that the embedded control vendors are exclusively targeting embedded applications and ignoring the central processor chip market. This is absolutely the case in unit terms, but it’s not true in aggregate revenue terms, when one includes the revenue obtained from sales of the entire central processor chip set.

Another fact demonstrating the fallacy of exclusively targeting embedded control is that the majority of embedded applications (97 percent of the units and 83 percent of the revenues) are served by 8-bit microcontrollers whose average price is less than $3.50. At current semiconductor learning curves, it will take through this decade for RISC implementations to achieve prices in this range. It therefore seems likely that microprocessor vendors choosing to exclusively target embedded control do so out of an inability to successfully penetrate the central processor market. In reality, architectural standardization flows out from the central processor. To win in embedded control, a microprocessor supplier must first win in central processing.

Of course, this doesn’t make embedded control a virtual nonmarket for RISC architectures. The point of these comments is simply to reinforce the fact that accurate market penetration projections should be based on the actual underlying market situation.

In the short term, RISC will successfully penetrate the computer peripheral portion of the embedded control market. This portion is the high end of this market segment, and typical applications share the characteristic that performance is a higher-priority criterion for system designers than price.

A significant number of the applications in this area are also sensitive to “central CPU architectural pull-through”; that is, designers of computer peripheral embedded subsystems (such as disk or datacomm controllers) are often influenced in the architectural selection for the embedded controller by the architecture used in the central processor of the system to which the peripheral will be interfaced. This phenomenon is largely a matter of convenience, since designers can significantly boost their productivity if they develop software on a system based on the same architecture that the embedded target system will use.

RISC architectures have received much press exposure in this market segment and, in fact, provide optimal solutions for these applications, easily surpassing the price/performance offerings of CISC in these areas. This market segment will be largely penetrated by RISC within the next three years.

On the other hand, RISC will be less quick to penetrate the market for specialized embedded control applications. In these applications, the embedded controller acts as the central processor of a self-contained system. The primary selection criteria for the central embedded control designer are price and available peripherals. Over 500 million central embedded controllers are sold each year at an average selling price below $3.50.

RISC’s penetration of this market segment will be slow, picking up speed only toward the end of the decade. At that point, RISC chips will be sold in the sub-$5 price range, and will support the type of on-chip peripherals needed for these applications.

Roger D. Ross is president and chief executive officer of Ross Technology (Austin, TX).
New long-word architecture threatens to outshine RISC

Ron Wilson, Senior Editor

The struggle between RISC and CISC has degenerated into trench warfare, with both architectural concepts holding on to well-defended application segments. But now an agreement between Atmel (San Jose, CA) and technology start-up Teraplex (Champaign, IL) promises a new microprocessor architecture, perhaps two generations beyond RISC, that could outflank both of the foes. The Minimum Instruction Set Computer (MISC) may be able to execute both RISC and CISC binaries faster than the CPUs for which they were written.

On the surface, the Atmel/Teraplex agreement seems like a simple technology exchange. Teraplex, a company primarily engaged in parallel-processing research, is looking for a vendor with both a hot CMOS process and excellent packaging technology to fabricate its pin-hungry computing elements. Atmel is a growing CMOS house without a major CPU in its product line.

But why would Atmel, generally a low-profile, conservative firm, venture off into parallel computing? The industry is, after all, strewn with the remains of exciting parallel-processor architectures that died looking for a profitable application. And why should a busy engineering manager care what Atmel builds for a research company? A coherent answer to these questions requires a close look at the Teraplex architecture.

Two steps from RISC

Perhaps the best way to understand the MISC architecture is to think of it as an evolution from RISC theory. From RISC, the new thinking draws at least two important concepts. First, RISC introduced the idea of short, simple instructions that could execute in a single machine cycle. Second, the RISC advocates proposed instruction scheduling—rerearranging instructions in a program to keep the pipeline full as long as possible.

These two concepts fit nicely into the next stage of evolution, the so-called superscalar architectures. In these machines, a number of independent RISC pipelines are combined into one CPU. Hardware in the control unit fetches instructions—often several at a time—and decides which of the available pipeline units can accommodate which of the pending instructions. Thus under ideal conditions the CPU can execute several instructions on each machine cycle.

A refinement of the superscalar approach has received a lot of attention in academic circles. Some architects point out that in a superscalar machine the sequence of instructions has great influence over the amount of parallelism the CPU can achieve. So it doesn’t make much sense to leave the instruction scheduling to chance. The advocates of this school suggest that, instead of a whole series of short instructions that get assigned to pipelines at run time, the machine use very long instructions containing one opcode for each execution unit in the CPU. The compiler can then pack operations into the long instructions at compile time, coming closer to optimum use of the execution units. These very long instruction words give the architecture its name: VLIW.

In theory VLIW machines should achieve high levels of parallelism. The compiler can pack operations into the long instruction words in such a way that most pipelines are full most of the time. But in practice, VLIW machines have demanded complex compilers, have had trouble running at high clock rates, and have been unable to get much benefit out of more than three or four concurrent execution units. The latter problem seems to be inherent in the structure of computer programs, rather than caused by hardware or compiler limitations.

Opening up the pipeline

In a way, the MISC architecture is a blend of superscalar and VLIW concepts. Like the VLIW machines, Teraplex’s MISC uses a long—128-bit—instruction format to control a number of execution units simultaneously. But the MISC architects have simplified the execution units until they perform rudimentary tasks that Teraplex calls “atomic instructions.”

“We use only nine generic operations,” says Teraplex president Philip McKinney. “Essentially, there is a functional unit in the CPU for each type of operation. In each instruction, a 64-bit field determines how data will flow through the functional units on that clock cycle. The instruction bits control the hardware directly and therefore there is no decoding delay.”

This arrangement gives the compiler control not only of instruction ordering, but of the sequence of the
"Reliability is essential when we're designing systems for military aircraft. Microware's track record with real-time system software made OS-9 our logical choice."

Systems Research Laboratories (SRL), a leading defense contractor, designs and builds avionics systems for the military. These systems include heads-up and heads-down displays, digital scan converters and electronic warfare equipment.

"Microware's OS-9 Real-Time Operating System provides the reliability we need to develop sophisticated avionics systems."

SRL had tried other systems, including "dumb" kernels, but none provided the reliability needed for their demanding military applications. Then, SRL turned to Microware's OS-9 Real-Time Operating System. "We looked at Microware's track record, as well as evaluated OS-9's performance in our units."

"Microware consistently develops and designs quality software products... Their OS-9 Real-Time Operating System was the logical choice for SRL."

Before SRL's systems are installed on military aircraft, every system is put through its paces. "Our products are found in the most sophisticated military aircraft. We've designed Microware's OS-9 into our critical avionics systems because of its reliability and functionality."

"We put every embedded OS-9 system to the test."

OS-9 and its comprehensive suite of real-time development tools provided a total solution for Systems Research Laboratories. Find out how Microware can put OS-9 to work for you. Call us today to order a FREE copy of the OS-9 Catalog (your complete guide to the OS-9 Operating System).

Call Microware Today!
1-800-475-9000
In California, call (408) 980-0201

MICROWARE SYSTEMS CORPORATION
1900 N. W. 114th Street • Des Moines, Iowa 50322
Phone: (515) 224-1929 • Fax: (515) 224-1352

Microware is a registered trademark of Microware Systems Corporation. OS-9 is a trademark of Microware Systems Corporation. All other brand or product names are trademarks or registered trademarks of their respective holders.
operations that would make up the pipeline in a RISC machine. With this much control, and with the atomic operations carefully defined to be nonoverlapping, the architecture virtually eliminates the possibility of resource contention within the CPU.

Thus the MISC CPU executes code as a series of tiny, direct-control operations fed in parallel to all the functional units. "You can think of the machine as running at the microcode level," suggests McKinney. Because the functional units are simple, flow-through devices, many of the register, gate and clock-skew delays encountered in RISC pipelines simply don't exist. This allows the MISC machine to operate at extremely high clock frequencies, and at least potentially to achieve far greater performance than CISC or RISC machines doing the same tasks on the same technology.

But there is also a clear disadvantage to the technique—it is memory-intensive with a vengeance. What in a RISC machine would be one 32-bit instruction may in the MISC machine balloon into several 128-bit instructions. Of course a good compiler will be able to pack portions of several different instructions into those few big words, so a one-to-one comparison is difficult. But Atmel marketing vice-president Jeff Katz admits, "Memory size requirements go up by a factor—something bigger than one and less than 10. But memory speed requirements aren't that great, and we have reasonably fast conventional SRAM caches and then a large pool of DRAM somewhere."

### Parallellism and emulation

One of the most unique things about the MISC architecture is that the CPU is designed to be an element in a massively parallel computer system. The processor chips can be used in arrays, connected by crossbar-like global switching chips, with what McKinney describes as "a revolutionary method for addressing global and local memory." One facet of the scheme is that the CPUs have no registers—all operands are stored in memory.

This means that an array of MISC CPUs would have two remarkable characteristics. First, all CPU hardware would be exposed to the compiler at the pipeline stage level. Second, all operands, including temporary results, would be exposed to all CPUs via the switching net. The combination of these two attributes makes possible a unique capability, according to McKinney: "We can do parallel scheduling at the instruction level."

In effect, the compiler can break a program down into CISC-level or even RISC-level instructions, then schedule different instructions to different CPUs in the system. In many cases, the compiler could even spread parts of a single CISC instruction across several CPUs. The power of this capability shows up quickly in an example.

"One thing we've done in simulations," McKinney says, "is to take foreign binaries, break them into atomic instructions and run them on our chip. One MISC chip can execute 80386 code 4.5 times faster than a 33-MHz 386 can."

### A range of promises

There are clearly several potential uses for the MISC machine. First, there is the application probably intended by the designers: massively parallel computers. Because of its extremely fine granularity and simple hardware, MISC parallel computers should be able to achieve both a higher parallel-performance multiplier and a higher operating frequency than those of most parallel architectures.

Second, and more intriguing for most designers, is the possible application to workstations. A MISC workstation could theoretically straddle the fence between IBM PC and RISC compatibility, executing binaries from both sources. Again, because of the compiler power and high clock frequency, the MISC CPU might well outrun both PC and RISC CPUs on their own code. And the workstation would be moderately scalable by simply adding more CPUs and recompiling. Users could expect nearly linear performance gains even on single-task systems.

But such promises are far from sure things. While MISC seems to be leading in the direction in which RISC and VLIW pointed, excellent architectures have failed to deliver the goods before. And any widespread acceptance of MISC is clearly predicated on continued erosion in memory costs. A PC five times faster than a 33-MHz 386 but with eight times the memory cost might not be a clear winner.

Finally, there are the issues that militate against the success of any new architecture: unfamiliarity, lack of tools and support, and lack of application code. Atmel will be working to overcome these. "Teraplex will originate the technical support for the chip, but we have time to get a strong organization in place by the time chips come out next year," says Atmel's Katz.

From Atmel's point of view, and from the perspective of design managers in the PC, workstation and server businesses, MISC represents far more than a fab agreement. Potentially, the new architecture could be the vanguard of the next generation in computing technology.
No matter which of these manufacturers’ CPUs you choose, passive backplane or motherboard, there’s an I-Bus enclosure that’s the right system package for your commercial or industrial environment.

Take a close look at an I-Bus enclosure. It’s designed for OEMs and system integrators:
- Scientifically developed cooling.
- Ease of service and maintainability.
- Thorough documentation.
- Safety approvals from UL, CSA and TUV.
- FCC Class A EMI/RFI.

Choose from a wide variety of models, from a compact 6-slot to a hefty 20-slot. Models that hold nine 5¼-inch drives. Rack mount, tabletop or floor-standing. Models for motherboards as well as passive backplanes—and segmented-backplane versions that can put 2, 3, 5, even 10 computers in a single enclosure.

But that’s only the beginning. We’ll tailor, modify or custom design an enclosure to your exact needs.

If you want, we’ll completely assemble and test your system (our boards and/or yours), and take it all the way to drop shipment to your customer.

We’re 100% dedicated to PC technologies, and dedicated to serve the OEM and Systems Integrator. Call today about the I-Bus T.O.P.S.™ (Total OEM Program Support) Plan—a complete life cycle support program that saves you time and cost in the design phase, and continuous support over the life of your system.

Call toll free 800-382-4229
Denser, faster FPGAs encroach further on masked gate arrays

Barbara Tuck, Senior Editor

In a market where a product can be a dinosaur 18 months after it's first shipped, design teams are being encouraged to explore alternative, cost-effective technologies to speed product development. Considering the limited number of users having the expertise to design masked gate arrays within a tight time schedule and budget, it's not surprising that the market for desktop-configurable field programmable gate arrays (FPGAs) is exploding. Indications are that the programmable parts are striking ever deeper into masked gate array territory.

Denser devices about to be shipped by Actel (Sunnyvale, CA) and Xilinx (San Jose, CA), along with the first FPGA device offered by Plessey Semiconductors (Scotts Valley, CA), are likely to fuel that activity. Advances in technology make this second generation of FPGAs an even more feasible design alternative to masked gate arrays, especially as prototype vehicles and for small production runs.

Actel confirmed last month that its in beta test with a new family of 1.2-µm CMOS nonvolatile FPGAs, to be shipped next quarter. Like earlier devices, the ACT 2 family is based on PLICE antifuse programming links and channeled gate array architecture. In comparison to the company's earlier devices, the new family's densest device, the A1280, is four times larger and has twice the speed (system-level performance up to 60 MHz) and twice the I/O capacity. The A1280 has 8,000 masked-gate-array-equivalent gates and 750,000 tiny PLICE antifuse elements.

Basic logic modules have been enhanced to accommodate functions that have up to seven inputs, and a new logic module optimized for configuring sequential macros accommodates a latch or flip-flop and/or many combinatorial macros of one to seven inputs. State machines with up to five five-input product terms require only two module delays with the enhanced architecture.

Actel has also increased routing resources by boosting the number of horizontal routing tracks per channel to 36 and vertical tracks per column to 15. To make performance more predictable, the vertical routing architecture has been modified to reduce from four to three the maximum number of antifuse elements required to make a connection. Speed-critical module-to-module connections involve only two antifuse elements.

Higher-density FPGAs of up to 16,000 equivalent gates are being developed by Actel and Hewlett-Packard in HP's 0.8-µm process. HP will use the FPGAs as prototype vehicles for its standard-cell designs. No estimate of availability has been given.

Gate-counting games

Formidable competition for Actel parts will continue to come from FPGA market leader Xilinx, also preparing to ship a new generation of programmable parts. Compared to earlier Xilinx parts, the XC4000 submicron CMOS Logic Cell Array family, to be available next month, has twice the density, twice the speed (60 to 70 MHz), plus on-chip data SRAM. The densest of the new RAM-based reprogrammable Logic Cell Arrays is 20,000 gates.

Actel counts its gates in such a way that the number of gates of an
When you must win!

For your "must-win" defense and aerospace programs, put the world’s leading supplier of MIL-SPEC VMEbus systems on your team. Ready-to-run VMEbus systems from DY 4 are selected overwhelmingly by system integrators for aerospace and defense programs world-wide.

DY 4 provides performance, reliability and cost-effectiveness through integration of a full range of open-system VMEbus products and services to military, ruggedized and commercial standards.

DY 4’s system solutions incorporate non-developmental item (NDI) products from the broadest product line in the business - CPUs... memories... communications controllers... analog I/O... high-performance graphics engines... chassis... Ada* foundation software and built-in-test (BIT) diagnostics.

DY 4 provides a comprehensive quality program to MIL-Q-9858A and fully compliant configuration management to MIL-STD-483; design procedures conform to MIL-STD-1521 with manufacturing according to MIL-I-48604 (quality control) and soldering to MIL-STD-2000 in an ESD-controlled environment.

Customer First, Quality Always

DY 4 Systems Inc.

Campbell, CA
Tel: (408) 377-9822
Fax: (408) 377-4725

Nashua, NH
Tel: (603)596-2400
Fax: (603)595-4343

Pennant Hills, Australia
Tel: +61-2-484-6314
Fax: +61-2-875-1665

Hannel, Denmark
Tel: +45-86-863824
Fax: +45-86-962075

21 Fitzgerald Road, Nepean, Ontario K2H 9H4 Tel: (613)596-9911 Fax: (613)596-0574

*Ada is a trademark of the United States Department of Defense

CIRCLE NO. 18
IN THE ERA OF MegaChip TECHNOLOGIES

YOUR DSP: ALL THERE

There is a big difference. Only Texas Instruments brings it all together for you in DSPs, from software to silicon... and we have 10,000 users to prove our point.
Designers are applying TI's single-chip TMS320 DSPs (digital signal processors) in more systems around the world than any other. In fact, leading manufacturers in most market segments — including telecommunications, computers and computer peripherals, automotive, industrial controls, consumer products, and military systems — use TMS320 DSPs. These designers choose our DSPs because they know there is a big difference between all there and almost. With TI, they know they are getting the most complete DSP solution in the business — (1) performance, (2) support, and (3) broad choice. These important factors are worth careful consideration as you evaluate DSPs:

- Yes 1. Am I assured of access to the top-performance devices in the field?
- No

Naturally, performance is a high priority for any DSP-based system. The TMS320 family consistently sets the performance standards for the industry. Among the newest additions are the highest performance fixed- and floating-point single-chip DSPs, both with clearly defined road maps for future performance upgrades. Multi-processing DSPs offer even higher performance.

- Yes 2. Is world-class support in place to help speed my design to market?
- No

Few if any DSP vendors equal the level of support that TI offers. Industry-standard high-level language optimizing compilers (ANSI C and Ada), HLL debuggers, the SPOX™ multitasking DSP operating system, and scan-based emulators provide you with a development environment similar to that traditionally enjoyed in general-purpose microprocessor design.

Low-cost evaluation modules allow you to accurately evaluate and benchmark a TMS320 processor for your application. Such leading-edge tools are only the beginning of our comprehensive support. Other TMS320 support includes:

- A hot line staffed with DSP personnel ready to answer your technical questions
- An on-line bulletin board service
- More than 2,000 pages of application notes and DSP code
- More than 100 third parties and consultants
- Hands-on workshops
- University program with more than 100 universities participating

- Yes 3. Is the choice of devices broad enough that I can closely match a DSP to my price/performance needs?
- No

Our TMS320 family spans five generations — more than 20 members offering a price/performance range from $4.00 to 40 MFLOPS. Your choice includes:

- EPROM DSPs that shorten your time to market
- DSPs optimized for specific applications
- Military versions
- Single-chip devices offering 40-MFLOPS performance
- Multiprocessing DSPs
- Low-cost DSP solutions for cost-sensitive applications
- Compatibility to protect your software investment

At TI, we have it all, and we are ready to help you put it all together.

Get your free three-volume TI DSP Applications Library; call 1-800-336-5236, ext. 3528
Or complete and mail the return card and we'll send you our three-volume TMS320 DSP Applications Library. If you prefer, we'll send you our TMS320 product overview and support brochure. We feel sure you will soon be one of the thousands around the world achieving design success with the leadership TMS320 family.
Actel FPGA would be equivalent to the number of gates of a masked gate array of the same gate count from LSI Logic (Milpitas, CA). Actel claims that architecture and routability differences between Actel and Xilinx parts make a 20,000-gate Xilinx device comparable to Actel's 8,000-gate device. But Chuck Fox, Xilinx director of IC marketing, counters that claim. "Though density is application-dependent," Fox says, "customers have gotten 20,000 gates out of the device."

Among enhancements to the Xilinx Logic Cell Arrays is an increase from five to nine combinatorial inputs for each configurable logic block. (Metal lines of programmable switching points and switching matrices connect logic blocks.) Two separate groups of four inputs each drive their own function generator, actually a small ROM lookup table. A third function generator can combine the outputs of the first two with the ninth input. Each trio of function generators can be programmed 32 billion different ways. Moreover, each four-input function generator can be configured as a two-bit adder with a built-in hidden carry that can be expanded to any length.

This fast carry logic can put two counter bits into each configurable logic block and run them at a clock rate of up to 50 MHz (for 16 bits), regardless of whether the counters are loadable. For a 16-bit loadable counter, that translates to three times the speed of XC3000 parts in half the number of logic blocks. Furthermore, the speed of the dedicated carry circuitry makes it possible for a 16-bit adder/accumulator, requiring eight configurable logic blocks, to have a combinatorial delay of only 20 ns. That's in contrast to 30 blocks and a 60-ns delay—or 41 blocks and 33 ns—for the same implementation in the earlier XC3000 family. Xilinx has also doubled the number of horizontal and vertical long lines that carry signals across the length or width of its Logic Cell Array.

Since the Logic Cell Arrays are based on a RAM process and all Xilinx circuits store their configurations in RAM, Xilinx has given users of the XC4000 family access to these distributed memories. The user determines whether configurable logic blocks are dedicated as RAM (organized in arrays of 32 × 1 bit or 16 × 2 bits) or as ROM-based logic. Read access time for the on-chip memory is the same as logic delay, about 5 ns, and write time is about 10 ns. This distributed RAM can be used for registered arrays of multiple accumulators, DMA counters, and FIFO buffers. A 32-byte FIFO, for instance, would use eight configurable logic blocks for storage, six for address counting, and one for arbitration.

While Actel promotes its FPGAs for prototyping and small-production runs, Xilinx targets a different customer, according to Lee Farrell, Xilinx vice-president of marketing. "Xilinx is in business to sell production volumes. We have customers buying thousands of Logic Cell Arrays a month—the per-unit cost is higher than a gate array, but there is no NRE. But if you prototype with one, it's not that easy to take it out and plug a gate array in. Customers have to ask themselves whether they want to redesign their previous project or go to work on their next design."

A new player
The already heated FPGA market has a new entry—Plessey Semiconductors—with its sea-of-gates Electrically Reconfigurable Arrays (ERAs). Like the Xilinx Logic Cell Arrays, they're RAM-based solutions. Plessey is now shipping the

The time is ripe for believing in FPGAs that don't involve resimulation and reiteration, not to mention endless test vectors.

1.4-µm 10,000-equivalent-gate 60100, and the company says that its three-layer-metal 1.4-µm process—with stacked vias and equal pitch on all metal layers—will later be used for a 40,000-gate part. Beyond that, Plessey plans to shrink the same architecture into a 1-µm process in 80,000 gates, and then down to 0.8 µm for up to 160,000 gates. Since the Plessey parts offer cell libraries compatible to the company's CMOS masked gate arrays, they may appeal to designers looking for an easy migration path.

The density of the Plessey parts is attributed to the granularity of the logic. Each cell in the matrix is programmable as a single NAND gate or latch. "Higher gate counts are possible with ERA technology," says Steve Brightfield, ERA market-
Radstone's 68-41 Freeflow+ multiple microprocessor board with truly independent microprocessors for data and I/O gives you next generation VME performance...Now!

- 68040 with 16 Mbytes of dual-ported memory for maximum data throughput via concurrent, uninterrupted microprocessor operation up to 40 MHz
- 68020 with 4 Mbytes of dual-ported memory controlling extensive high performance on-board I/O facilities—all operating independently
- Multiple independent external buses—VME, VSB & APEX
- Multiple independent local buses—processor and I/O
- High performance DMAs
- Intelligent, high performance Ethernet and SCSI/SCSI-2
- ...and much, much more.

Radstone's Freeflow+ architecture takes VME to new performance levels. And now it's available with 040 processing punch. It's the very latest in Radstone's long line of leading edge commercial real-time VME board level products.

Extend your VME lead...and investment
For details on how to supercharge your VME system with Radstone's Freeflow+, and extend your current investment in VME hardware and software, call or write. Do it now, because your system is worth it!
Each cell in the Plessey Electrically Reconfigurable Array matrix is programmable as a single NAND gate and has access to a number of input interconnects. For example, gate A can connect directly to gates B, C, D, E or F via the local interconnect. Each gate also has access to short-range and long-range vertical and horizontal bus resources for interconnecting macros and higher-level functions.

But the Xilinx reaction to Plessey's density claims is that the company is "making rather generous projections over time and confusing the market in doing so," says Fox. The fine-grained Plessey architecture may have a lot of gates, but the user will benefit from only about 30 percent of them, Fox claims. Plessey doesn't refute the claim that useful density will be limited to roughly one-third of the gates in its ERAs.

A feature unique to the ERAs that could be appealing to certain users is their ability to be partially or entirely reconfigured in-circuit. Even Xilinx's Fox admits that dynamic reconfigurability is an interesting technical feature, but adds the qualification, "If they can get it to work and anyone wants to use it, that is."

Designers exploring technology alternatives to masked gate arrays will no doubt be studying the new Actel, Xilinx and Plessey FPGAs very closely. The time is ripe for believing in a worthwhile design solution that doesn't involve resimulations and reiterations, not to mention endless test vectors, as well as NRE charges that are likely to be multiplied if you're not a veteran— and maybe even if you are. Agreement on a standard way to count gates, though, would very likely increase designers' faith in FPGAs. And the establishment of performance benchmarks would most likely boost that faith further. FPGAs have been around long enough to be taken seriously after all.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Actel
(408) 739-1010 Circle 204
LSI Logic
(408) 433-8000 Circle 205
Plessey Semiconductors
(408) 438-2900 Circle 206
Xilinx
(408) 559-7778 Circle 207

The best address for Siemens Semiconductors:
A. Wien
Tel. (0222) 71711-5661
B. Melbourne, Vic. 3121
Tel. (03) 425-7111
C. Bruxelles
Tel. (02) 336-2211
D. Sao Paulo-SP
Tel. (011) 893-2211
E. Mississauga L5T1P2
Tel. (416) 564-1995
F. Zurich
Tel. (01) 893-3111
G. Berlin 10
Tel. (030) 3939-1
H. Dusseldorf 1
Tel. (0211) 399-0
I. Frankfurt 1
Tel. (069) 797-0
J. Hamburg 1
Tel. (040) 286-99-0
K. Hannover 61
Tel. (0511) 877-0
L. Munich 80
Tel. (089) 9221-4391/4138
M. Nurnberg 1
Tel. (0911) 654-0
N. Stuttgart 1
Tel. (0711) 2076-0
O. Ballerup
Tel. (44) 774477
P. Madrid
Tel. (01) 555-4062
Q. Paris
Tel. (1) 4932-3810
R. Sarnbury on Thames
Tel. (0932) 752615
S. Amaoussio/Thessaloniki
Tel. (01) 6964-111
T. Hongkong
Tel. (852) 330322
U. Milano
Tel. (02) 6766-4241
V. Bombay 400018
Tel. (40) 38876
W. Dublin
Tel. (01) 302855
X. Tokyo 100
Tel. (03) 201-2401
Y. Osaka 5
Tel. (02) 563000
Z. Amsterdam
Tel. (02) 3333333
AA. Alfragide
Tel. (01) 4183311
AB. Buenos Aires
Tel. (01) 300411
AC. Taipei
Tel. (01) 5234700
AD. Seoul
Tel. (02) 275-6111
AE. Stockholm
Tel. (08) 728100
AF. Helsinki
Tel. (09) 305051
AG. Singapore 0513
Tel. (776) 0044
AH. Istanbul
Tel. (01) 1510990
AI. Iselin
Tel. (201) 906-4300 (Discrete)
AJ. Santa Clara
Tel. (408) 980-4500 (ICs)
AK. Cupertino
Tel. (408) 725-7919 (Opto)
AL. Johannesburg
Tel. (011) 407-4111

36 SEPTEMBER 1, 1990 COMPUTER DESIGN
Siemens has opened a whole new line of communication ICs which now makes it easier to successfully combine high-speed data transfer with high-level data-link control.

The Siemens High-Level Serial Communication Controller (HSCX) has all the features you need for a powerful communications system. The HSCX comes with a choice of one (SAB 82526) or two (SAB 82525) bi-directional channels, and has a storage capacity of up to 17 frames in its on-chip 64-Byte FIFOs. At a transfer speed of up to 6 Mbit/s, it supports a number of synchronous standardized protocols (HDLC, LAPB/LAPD, X.25, SDLC), and a greater number of proprietary protocols.

And by inserting data into programmable time slots automatically, the HSCX considerably lowers your CPU overhead, as well as reducing external glue logic. These features provide the potential for HSCX applications in a variety of fields, such as proprietary LAN controlling networks, assembly line LANs, fast diagnostic systems, and traffic systems, as well as standardized areas such as Switching Systems and ISDN (X.25, Terminal Adaptors, and Modems).

For easy access to the wide variety and complexity of synchronous data transfer, Siemens also provides a PC-based evaluation kit. The HSCX has already made a name for itself by providing the power needed to drive even the most complex communications systems. In fact, the biggest names in the industry already rely on the HSCX— with a great deal of success. The HSCX will be sourced also by AMD. Isn’t it amazing what you can accomplish with good communication skills?

If that goes down well and you want to find out more, contact your local Siemens office or just write to:

Europe:
Siemens AG, Infoservice HL 1575, Postfach 2348, D-8510 Fürth
USA:
Siemens Semiconductor Group, 2191 Laurelwood Road, Santa Clara, CA 95054 Quoting: „HSCX“

CIRCLE NO. 21
HOW TO TURN 040 WITHOUT LOSING A STEP.

FORCE '030
Turning 040 doesn’t mean you have to give up the code you lived by when you were 030. Although that’s what some manufacturers expect you to do.

But not FORCE. We guarantee that applications written for our 68030 VME boards will run on our 68040 boards. That’s because we’ve built compatibility into our 030 and 040 address maps and onboard device drivers.

In fact, no one makes it easier to move your software from 030 to 040. The competition can’t even come close. Just ask them. Then ask us. We’ll keep you from spending months writing new software drivers. So you can spend your time improving performance and functionality. Or getting to market months ahead of the competition.

What’s more, you can start today on your 040 applications. Just develop them on a FORCE 030 board. When you’re ready, we’ll upgrade you to the highest performance 040 board you can buy.

So you can speed up your software without missing a step.

Of course, we have all the tools you need to get started. Choose from the broadest range of real-time operating systems and kernels, including PDOS, OS-9, VxWorks, VRTX32 and pSOS+. We even give you VMEMROM, free of charge.

You can also take advantage of XRAY and the entire Microtec family of software tools. Including cross, native and embedded development environments.

Our performance advantage even extends to UNIX®. With the industry’s top-rated Unisoft UNIX 5.4.

Finally, you get the industry’s best-rated documentation, integration support, regional technical staff and a full one-year warranty.

Here’s your next step: call 1-800-BEST-VME ext. 40 for details on our 030 to 040 upgrade offer. Or fax a request to (408) 374-1146 for an immediate response.

Because turning 040 doesn’t have to slow you down.

FORCE
VME at its best.

FORCE Computers, Inc., 3165 Winchester Blvd., Campbell, CA 95008-6557, (408) 370-6300 ext. 40

CIRCLE NO. 22
Creative use of PLLs solves clock skew problem

Ron Wilson, Senior Editor

The mundane problem of getting clock signals to the synchronous chips in a computer seems like an implementation detail. But as clock periods shrink to a few tens of nanoseconds, clock skew allowance—added time in the machine cycle to make sure that all the clock signals have arrived at their destinations—is becoming a major limitation to system performance.

It may be possible to get a CMOS RISC CPU, cache memory subsystem and floating-point processor that all run at 40 MHz. But—as some design teams have found to their horror—if you have to wait 5 or 6 ns for all the various clock inputs to trigger, you may end up with a 25- or 30-MHz processor board. The degradation becomes even worse when critical parts are distributed across several boards and the clock is routed over a backplane.

Two semiconductor vendors—Motorola (Phoenix, AZ) and Gazelle Micrcircuits (Santa Clara, CA)—have announced low-skew clock distribution chips that can ease some of the more harrowing of these nightmares. The parts aren't based on fast, powerful drivers that try to overwhelm clock loads; that approach simply increases system noise problems. Instead, the two companies have used one of the fundamental properties of phase-locked loops (PLLs) to reproduce or manipulate clock signals with nearly zero skew.

Tracking the input clock

A sufficiently stable PLL can lock its output to the phase of an input signal with better than 1-ns accuracy. This idea can be applied directly to clock drivers—if the driver is a PLL, the device can have many clock outputs locked in phase to a single input clock. This is the principle used in the new parts from both companies.

Motorola's device, the MC88915, uses a 40- to 80-MHz CMOS PLL to accomplish its purpose. The device takes in a clock signal at TTL levels and reproduces its phase within a 1-μs window on five CMOS outputs. But the part has more tricks up its sleeve than just mimicking the input clock. Motorola uses the PLL's voltage-controlled oscillator (VCO) to drive a counter chain. By picking the feedback off the end of the chain, the VCO can run at twice the input frequency. This makes it possible for one of the chip's outputs to run at the VCO frequency—twice the input clock rate—while five other outputs reproduce the input frequency. For good measure, the chip also has an inverted output and a half-frequency output.

The frequency-doubling feature can be particularly useful in situations where a master clock has to run over a backplane. It would be hopeless to try to synchronize a system to a 40-MHz backplane clock. But with the new chip, you can distribute a 20-MHz clock and multiply it up to 40 MHz on each board in the system, with the phase of each 40-MHz local clock locked to the master within 1 μs or so.

Gazelle's concept is similar to Motorola's, but a big difference in pro-

Gazelle designers Gary Gouldsberry, standing, and Bob Burd examine the phase-shifting characteristics of Gazelle's PLL-based clock distribution chip (inset). It locks TTL-compatible clock outputs to a master signal, but with phase shifts programmable in 2-ns increments. The company claims the accuracy of the phase shift is typically ±100 ps.
Take a look at National’s new RS-485 quad transceiver.

The Industry's First and Only RS-485 Quad Transceiver Gets to All Points Faster.

National's new DS36950 sets the standard for multipoint bus transmission. It meets and exceeds RS-485, IPI, and SCSI standards, and is ideal for high-speed, parallel, multi-point, computer I/O bus applications.

In IPI systems, the DS36950 transmits information at speeds that sizzle, displaying data-transfer rates as high as 10 Megatransfers per second on a 13-ns signal transition time.

What's more, it has a typical driver propagation delay time of 13 ns, with guaranteed minimum and maximum propagation delay times that eliminate timing uncertainty across a parallel interface.

The DS36950 achieves higher speeds and consumes less power than previous multiple-chip solutions.

Stingy on Power.

Boasting a 50% improvement over prior options, the DS36950 consumes less than 20 mA per transceiver. Which makes it well suited for a variety of applications, including:
- Computers
- Telecommunications
- Workstations
- Laser printers
- Optical disk drives
- FAX machines
- Hard disk drives

We’re Driving the Standards.

National has long been a proactive player in setting today's standards. In fact, we participate in a number of committees, including SCSI (X3T9.2), IPI (X3T9.3), and RS-232/422/485 (EIA/T30.2).

Our portfolio of over 260 devices is the most comprehensive in the industry, with a wide range of bipolar and CMOS drivers, receivers, and transceivers. All of which are supported by our dedicated group of experienced product specialists.

For free samples and more information, call or write us today:
1-800-624-9613, Ext. 50. In Canada: 1-800-548-4529, Ext. 50. National Semiconductor Corporation, P.O. Box 7643, Mount Prospect, IL 60056-7643. For high-speed RS-485 multipoint transmission, the DS36950 has the look of a winner.
cess technology gives Gazelle's parts quite different features. Using a proprietary gallium-arsenide PLL based on the design in Gazelle's 1-GHz HotRod communications chip, the GaAs designers have been able to get outputs running as fast as 160 MHz at TTL levels, with better than 500-ps phase accuracy between clock input and any output.

The additional speed also gives Gazelle the freedom to play more games inside the chip, resulting in two parts with different feature sets.

The first part is a six-output clock frequency multiplier not unlike the Motorola part, except that by proper choice of feedback and programming pins, outputs can be anywhere from one-quarter to eight times the input frequency, all locked to the input within 0.5 ns.

Phase-shifting abilities

The second Gazelle part uses the fast internal circuitry not for a counter chain, but as a digital delay line. The result is an entirely unique capability—the ability to program a forward or backward phase shift on the outputs in precise 2-ns increments. The six outputs can be set to provide many different mixtures of phase relationships over a range of 6 ns in each direction from an input clock as fast as 60 MHz.

Thus, while one output pin is exactly tracking the input, another might be 2 ns ahead of the input, another 4 ns ahead, and one pin a full 6 ns ahead. As in the frequency-multiplying part, this device maintains clock-to-output alignment within 500 ps maximum, and 100 ps typical, of the requested phase shift.

"The part gives you the opportunity to manage the clock distribution problem across a board," says Gazelle product marketing engineer Jonathan Zierk. "You can use the phase-shifting ability of the chip to compensate for the loading on various clock paths and get close-to-simultaneous operation of paths with very different clock loads."

The potential to remove much of the layout iteration, hand-selection of parts, manual measuring and loading of individual clock lines on individual boards and other such black magic could be an enormous boon to system designers. If these chips can help, either by eliminating skews in the clock source or by actually putting compensating skews into the clock drivers, much of the battle in high-frequency CPU design will be won.
Unix Systems That Fit Your Image.

Mizar / Integrated Solutions' Optimum Systems match your application style.

Do Unix® systems reflect their developers? Or are developers shaped by their machines? With the Optimum™ Family of Unix products from Mizar / Integrated Solutions, you do the shaping, all according to your application needs and cost objectives.

Optimum Unix solutions range from pre-tested board and software kits to completely integrated systems. They’re the kind of products you can easily tailor to meet unique application requirements. Best of all, the Optimum Family provides all the features and performance of the finest Unix workstations, but without their restrictive packaging and limited upgradability.

Based on the VMEbus, the 68030, and a high-speed memory architecture, Optimum systems are true performers. And our Berkeley 4.3 Unix with NFS™ and X.11 Windows™ support provides the ideal environment for both development and deployment of Unix applications. You can even develop on Sun workstations for later transfer to Optimum application systems with little or no change in source code.

But Optimum’s capabilities don’t stop at the basics. Designed specifically for high performance Unix applications, the Optimum family offers special features such as the Transparent Remote File System, TRFS™ for file sharing and networking at twice the speed of TCP/IP over Ethernet™. For multiprocessor applications, our unique clustering approach allows you to integrate multiple Unix processors in a single VME chassis.

Finally, Optimum products are backed by the best warranty, factory service, and technical support programs in the business. The Optimum solution doesn’t just include hardware and software, but the personal attention you need to get your application running in record time.

If ordinary Unix products aren’t your style, the Optimum Family probably is. Call today for more information on how we can serve your Unix application needs.

1-800-635-0200

Mizar / Integrated Solutions
1419 Dunn Drive / Carrollton, Texas 75006
(214) 446-2664 / FAX (214) 242-5997

CIRCLE NO. 26
Get true no-wait-state performance in a 256K Fast Static RAM, with the famous reliability and performance that comes from Motorola’s pure CMOS technology.

To squeeze 15ns access times out of a 256K Fast Static, we had to go to the drawing board and rethink Fast Static design from the start. First, we eliminated the need for shortcut measures like Address Transition Detection (ATD). We replaced them in a design that incorporates several new memory innovations.

LOOK WHAT’S NEW.

As part of our redesigned Fast Static architecture, we radically increased the array subdivisions to 32 blocks (with 128 rows and 64 columns per block). We then added small signal techniques, pre-amps,
and current regulation throughout. The result is a 256K, pure CMOS Fast Static that keeps up with even the fastest 32-bit microprocessors.

Four versions of our 256Ks are available. The 64K x 4s and 256K x 1s are available with 15ns access times. The 32K x 8s and 32K x 9s both offer 17ns.

JUST TWO MORE OF MANY.

These new Fast Statics are just two of the many exciting products in Motorola’s complete line of memories—which includes Fast Static RAMs, one and four-megabit Dynamic RAMs, 256K and one-meg Slow Statics, and modules. For more information, complete and return the coupon, or contact your local Motorola sales office, or call us toll-free at 1-800-521-6274.
Industry group initiates object-oriented software standards

Tom Williams, Senior Editor

Interoperability of applications is a level of standardization that goes well beyond operating-system or protocol compatibility. It's the ability of one vendor's word processor to use the data created by another vendor's spreadsheet running under a different operating system—without having to resort to conversion routines, modular production of software, reuse of code or porting across many platforms. Interoperability is among the goals of the Object Management Group (Framingham, MA), a fast-growing association of companies formed to promote adoption of standards for object-oriented software technology.

OMG has produced its first document in what is hoped to be a comprehensive effort to standardize interfaces for object-oriented systems. OMG invites industry comment on the document, which defines an abstract object and reference model. "Application technology must be object-oriented to provide interoperability," says president Christopher Stone. "The promises of Unix, RPC (remote procedure calls) and other standards don't provide true interoperability of applications."

It's a rare but happy situation when a technology-standards effort starts to gather steam well before major players have committed substantial resources to producing and marketing proprietary versions of it. One need only think of the plethora of graphics or networking "standards" and the pains taken to coax vendors and users away from proprietary paths. "We're early enough in this technology for people to see that they can find a framework for cooperation without giving up competitive advantage," says OMG's vice-president of marketing, John Slitz. It seems to be true. OMG boasts over 80 members and is adding one new member a week.

Agreeing on terminology

OMG's efforts are aimed at defining an overall Object Management Architecture (OMA). It will bring object-oriented technology beyond its already-acknowledged usefulness in programming—modular design, inheritance and reusable code—to the broad world of networked architectures and global computing. As a first step, the OMG technical committee has developed a document describing an abstract object model and a reference model for an OMA. "You must have an abstract object concept," says Stone. "Everybody has to agree on what an object is, what requests are, how a common request mechanism is passed from one object to another and so on."

In the OMG object model, as in all object-oriented technologies, objects are defined as a state and a set of operations that can be performed on that state. These operations are called methods. Objects perform services that are requested by clients. A client sends a request to an object along with parameters for the requested operation. The object then performs the requested service using one or more of its associated methods and returns the results to the client. Clients can be other objects, a user acting through a user interface object or an application program. Requests specify the particular operation (method) they want performed and the parameters for that operation. In other object-oriented systems, such as Smalltalk, requests are known as messages. Requests are passed from clients to objects using a message format.

The OMG object model is somewhat more generalized than the classical object model, in which a request identifies an object and zero or more parameters (which may also be objects) upon which the object is to perform some action. In the OMG model, method selection can be based on multiple objects; the method—the operation to be performed—may be selected from any object named in the request, even if the object is contained in the request as a parameter. The OMG definition of an object model sets forth a set of definitions to be used with all OMG-compliant software, which will eliminate ambiguous terms.

Classifying discrete components

The next step, and the first basic specification offered by OMG, is a reference model that defines a classification of components within the OMA. These components are identi-

THE OMG REFERENCE MODEL

APPLICTION OBJECTS
WORD PROCESSOR
DOCUMENT PROCESSOR
SPREADSHEET
CASE TOOLS

COMMON FACILITIES
"KNOWBOTS"
DOCUMENT ARCHITECTURE
SPELLER
MAILER
TIME MANAGERS

OBJECT REQUEST BROKER

OBJECT SERVICES
DIRECTORY
AUTHENTICATION
SECURITY

OBJECT-ORIENTED
DATABASE

The OMG reference model links object-oriented applications and services via an object request broker. The broker can provide communications-naming services and protocols so applications can communicate with each other and other services on single and multiple platforms, whether they are the same, different, linked over networks, or run different operating systems.
Those endless compile-time coffee breaks are a thing of the past.

**Compiles Faster**
The Sierra C™ compiler gets your code into your target system 10 to 20 times faster than other high performance compiler packages. The dhrystone benchmark, on a 16 MHz PC AT® host, compiles, assembles, links and downloads to a 68020 target in less than 4 seconds.

**Generates Better Code**
Sierra C has resolved the paradox of fast compiles and optimized code. While compiling at blazing speeds, Sierra C generates faster and tighter code than any other optimizing compiler on the market today.

**Complete Development Toolset**
Sierra C is more than fast—it’s complete. It includes all the tools you need for cross-development, built to perform with unsurpassed efficiency. Along with Sierra C’s optimizing compiler, macro assembler, and linker/locator, you get a librarian, symbol table examination utilities, a high speed parallel download system and a multi-window source level debugger. Complementing the toolset is an extensive C runtime library supplied in both source and object form.

**Designed for Embedded Systems**
Sierra C conforms to the proposed ANSI C standard, supporting function prototypes and the important keywords `const` and `volatile`. Position independent, re-entrant, and ROMable code can be generated. Code can be optionally grouped into as many as 126 independently positionable sections. Assembly language can be inserted into your C program through the `asm` keyword extension. And the download utilities allow executable modules to be transferred directly into the target system or into a PROM programmer with optional even/odd/quad byte selection. The Sierra C toolset supports all members of the 68000 family including the new 68332. Sierra C is available now for PC AT and PS/2™ computers, DEC VAX® systems, Sun™ Workstations and other UNIX™ systems.

With Sierra C you get better products out faster. Call today for more information at 800•776•4888

6728 Evergreen Ave., Oakland, CA 94611 (415) 339-8200

CIRCLE NO. 27
Frustrated with microprocessor system debugging?

How the right preprocessor interface can simplify logic analysis.

Here's free help in making the connections.

Plug into our new series of application notes today. And learn how to save time and aggravation when you're debugging microprocessor systems and busses.

Find out how an HP preprocessor literally makes it a snap to connect your microprocessor to an HP logic analyzer. And see how completing your HP logic analysis system with a preprocessor will speed and simplify measurements and data analysis. You'll also discover the industry's broadest selection of preprocessors—over 60 models support more than 70 microprocessors and busses.

So call 1-800-752-0900 today. Ask for Ext. 1402 or mail the reply card and we'll send the application information you need from our FREE series of six industry-specific application notes.

There is a better way.
fied as major separable components of the total OMA. The document further characterizes the functions of each component and lays out the relationships between them and with the external environment. Finally, the document identifies the primary protocols and interfaces for accessing the components.

"We believe the software marketplace is on the wrong track, trying to do everything in layers—interface layer, data management layer and so on. We believe software should be classified as a series of discrete objects called object services," says Stone. As examples he cites database directory services, network-management services and user-interface services. These services have to be available for application-oriented objects such as spellers, mailers and time managers. "We're not going to tell Wordperfect how to write Wordperfect, but we're going to tell it how to talk to that speller it wants to use," he says.

The reference model for the OMA starts with a request broker component. The object request broker provides the mechanisms for objects to transparently make and receive requests and responses. The request broker will be able to operate over networks connecting different platforms and operating systems. It addresses the issues of request dispatch and delivery, parameter encoding, synchronization, exception handling and object name.

The object request broker doesn't impose constraints on how objects themselves are to accomplish their tasks. A request to "print layout 312 laser_plotter," for example, might be sent as a request to the object "layout 312" whose "print" method would then print layout 312 on "laser_plotter." Alternatively, the same request could go to the object laser_plotter, whose print method would access layout 312. Or the request broker itself could select a print method jointly owned by layout 312 and laser_plotter to accomplish the task. This ability to select a method from an object originally named as a parameter illustrates the flexibility of the OMG object model.

Other components

The other three major components of the OMA—object services, common facilities and application objects—interact via the request broker. Object services provides for the basis of object functionality—the logical structuring and physical storage of objects. It manages the creation, deletion and modification of object classes—categories that can be instantiated to create objects that have some shared initial behavior or characteristics. Object services also handles storage of objects and their components (data and methods).

Some examples of object services

### AN EFFICIENT C-COMPILER FOR YOUR 8051 PROJECT

- Optimizing compiler for tight, fast code.
- Configurable for all 8051 derivatives.
- For PC/XT/AT, PS/2 and compatibles.
- Produces object file containing full symbolic information for use with all popular emulators.
- Complies with the proposed ANSI standard.*
- Parameter passing identical to that of PL/M-51.
- SFR's and BIT's directly accessible from C.
- Variables can be placed in DATA, XDATA, IDATA, CODE and PDATA memory.
- Interrupt routines with register bank switching can be written directly in C.
- Comes complete with a macro assembler, linker, and librarian with SMALL, COMPACT and LARGE library models, with and without floating point.
- Datatypes: (signed / unsigned) char, int, long, float (32 bit IEEE) and bit.
- Can be linked with existing PL/M-51 and ASM-51 object modules.**
- Many library functions, including configurable input, output, and startup routines.
- Completely integrates with our simulator/debugger and target monitor into your development environment.

Call for more information and your FREE demo disk!

---

* Except where inconsistent with maximum 8051 efficiency.
** PL/M-51 and ASM-51 are trademarks of Intel Corp.
are object database management systems, query facilities and directory services. Regarding storage in general within the OMA, Stone notes that the whole idea is to be independent of a particular data structure. "A language might store data in its own format, but the idea is to define the interface to that format so that other languages and applications can get to the data," he says. OMG proposes that object services also be able to handle security and to define and enforce access control for objects.

The common facilities is an optional component of the OMA in that it can be used to aid developers of OMA-compliant applications by providing facilities called "knowbots" that are commonly used and shared by applications. The developer of a compliant CAD package, for instance, might want to take advantage of the common OMG help facility. Other common facilities could include spellers and thesauri, printing and spooling, interfaces to external systems and electronic mail facilities. Developers could also create subclasses to enrich any of these for their applications.

The application object component of the OMA defined in the reference model consists of all normal user applications that are OMA-compliant—that is, they conform to the interface specifications and can communicate with other objects and object services within a system. Not only applications that are specifically written to be OMA-compliant can fit into this category; existing applications can be fitted with an OMA-compliant wrapper to fit into the architecture. Some applications that provide a general type of service such as an ASCII text editor or a database lookup program might be able to migrate to the status of common facilities and be generally available to other applications.

Projects still ahead for the OMG include definition of an object-oriented applications interface, distributed object management over networks and different operating systems, and an interface to object-oriented databases. Stressing that the group isn't defining the types of objects but is concentrating on the interfaces, Stone says, "We're not going to build, sell or have anything to do with the code that implements these concepts. That allows the proprietary nature of the implementation to stay paramount and lets the basic business of vendors stay untouched by the standardization effort."
Optimize your 680x0 Application to its peak

...with Oasys Embedded/Cross Software Tools.

Reach the pinnacle of your development with Oasys Cross Tools

Oasys delivers full 680x0 Cross and Native development tool kits built around the industry standard Green Hills compilers.

The Green Hills 680x0 compiler's Dhrystone rating is 33% faster than Sun's native C compiler. Using the new procedural inlining optimization, the rating jumps to a staggering 80% improvement.

Advanced C, C++, FORTRAN and Pascal Language Support

- Full ANSI C XJ311 support with switch selectable K&R C support.
- A true C++ Compiler for cross development.
- FORTRAN 77 with VAX VMS and DoD MILSTD-1753 extensions.
- Pascal ISO Level 1 support.
- All compilers are inter-language callable.
- Native compilers are supported for 680x0, 88000, 80386 & i860 hosts.

Available Now!

Oasys tools are available on over 35 UNIX based workstations and systems including DEC (VMS/Ultrix), Sun, HP/Apollo, IBM (OS/2 and AIX), and DG. Call us for the complete list.

Other Cross Tool Kits include:

- 88000, 80386, i860 and Microsoft C.

Integrated 680x0 Cross Development Tool Kits

Green Hills 68000/10/20/30/40 Optimizing Cross Compilers (C, C++, Pascal, FORTRAN)
- Superior register allocation, inlining and loop unrolling techniques.
- Support for position independent code and data.
- 68881, 68882, 68332 support.
- ANSI C run-time source library included for cross development.

Oasys UDB Universal Debugger
- Source level remote debugger for embedded programming.
- Multi-targeted and multi-window (supports 680x0 and 88000 targets).
- Extensive macro language.
- Customize communications to your target.

Oasys 680x0 Assembler/Linker
- Macro Assembler, Linker, Librarian, Cross Reference and Symbol File Format Utilities.

Oasys 680x0 Simulator
- Invaluable for debugging software without target hardware.

Scale new heights with high performance tools from Oasys. Call us for detailed benchmark results.

CALL (617) 890-7889
FAX (617) 890-4644
The age-old competition between man and machine is often demonstrated in the world of CAD tools. Certainly in printed circuit board design, the debate about which is better, engineer or autorouter, has been waged for at least 20 years. And in the early days of autorouting, the human-designed board was almost always cleaner, more aesthetically pleasing and manufacturable, even if the autorouter was faster. But the newest autorouters and editors, several of which were unveiled at the recent Design Automation Conference, are combining speed with flexibility to win the confidence of even the most diehard designers.

"Autorouters generally have the reputation of increasing the cost of manufacturing the board," says Steve Chidester, product manager at Teradyne (Santa Clara, CA). "Traditionally, they use vias more liberally and don't use layers efficiently. Remember, autorouters can only do one trace at a time, then go back and rip up and retry. A human designer can constantly decide to change tactics for a more efficient layout."

Faced with this reputation of producing a speedy but sometimes inefficient tool for printed circuit board design, autorouter vendors are turning their attention to developing products that will rival the handmade products of an experienced designer, while maintaining all of the traditional speed advantages. The latest release of Teradyne's Vanguard PCB layout system, Version 5.1, includes an autorouter that posts a benchmark performance of routing a 400-equivalent-IC board to 100 percent completion in just 90 minutes. The router, called AutoTrak, addresses the inefficiency issue through a unique grid system, which accommodates any repeating grid pattern. Because the tool isn't restricted to traditional square grids, AutoTrak can create special grids to minimize unused layout paths for a more efficient board design.

AutoTrak's flexible grid selection not only makes more efficient use of board space; it also gives engineers a freer hand in selecting ICs for a particular application. "One of the complaints about autorouters in general, and gridded autorouters in particular, is that they put limitations on a design," says Chidester. "This is especially troublesome when a designer needs to use some surface-mount and analog devices, many of which have unusual pin spacings that don't fall in a traditional grid. The advantage there," Noreika says, "is that a user can control a design with a specified grid, but the system doesn't have to deal with a grid map. The user-defined grid points are purely a frame of reference."

Proponents of the gridless approach also boast about the ability of their routers to pack more components onto limited board real estate. The Freedom gridless router from Harris Scientific Calculations (Fishers, NY) is a clearance-based tool...
At Micron Technology, we offer a full line of leading-edge RAM components in speeds and packages for virtually any application.

But the memory business is more than just parts -- it's people.

That's why we offer a total commitment to service and support, and a team of engineers and technical support personnel that are the most experienced memory professionals in the industry.

Because in the memory business there's only one point of view that counts. Yours.

---

### We Approach the Memory Business from One Point of View... Yours.

---

### Component Product Family | Memory Size (MBit) | Pinout | Speed (ns) | Package | Special Features | Availability | Military Qualified
--- | --- | --- | --- | --- | --- | --- | ---
DRAMs | 1MEG | x1, x4, x16 | 70-120 | X X | X | Industry standard pin-out | 256K, 256K, Now; 1MEG, 2MEG, 2MEG
| 2MEG | x4 | 2MEG | x8 | 70-120 | X X | Industry standard pin-out | 256K, 256K, Now; 4MEG
| 4MEG | x8 | 1MEG, 2MEG, 4MEG | x16 | 15-45 | X | Industry standard pin-out with OE | 256K, 2MEG, Now; 4MEG
| 64K, 16K | x32 | 256K, 2MEG | x16 | 30-45 | X | Industry standard pin-out with OE | Now
| 256K, 128K, 64K, 16K | x32 | 256K, 2MEG | x16 | 30-45 | X | Industry standard pin-out with OE | Now

---

*Custom module and board-level product manufacturing services available.*
that addresses the complex pin and component architectures of tightly packed boards. The router lets designers place components anywhere on the board, and then it weaves a trace that can have an unlimited number of diagonal bends between the pads. Traces that can’t find an orthogonal path can be angled to hug objects along the route. An automatic cleanup feature reduces via count and eliminates hooks or loops to shorten trace lengths.

Though gridless routers seem to have the upper hand when the issue of flexibility is foremost, those partial to gridded routers claim that their tools are faster. “So far the gridless technology hasn’t beat a gridded router in a fair fight,” says Teradyne’s Chidester. “It’s important when comparing autorouters to make sure that both tools are working on the same design. Some board designs are more suited for gridless

and others for gridded routers. We feel that overall, our router wins more often than not.”

His claim is challenged, however, by Racal-Redac (Westford, MA). Racal’s router, dubbed Bloodhound, uses a proprietary algorithm to boost gridless routing performance to levels that rival gridded autorouters. “We believe that Bloodhound can match the performance of a gridded autorouter over the broad spectrum of design tasks,” says Keith Felton, technical marketing manager for CAD products at Racal-Redac. “And because our interactive editor uses the same algorithm as our autorouter, it allows users to reroute particular traces in a very high-technology bracket—fine-pitch, mixed-technology applications.”

Keeping control

The interactive editor is yet another feature that autorouter vendors are
NISSHO ELECTRONICS

AT/VME MM CPU
Improve Your System Architecture With A Solid Foundation

The NISSHO N5280/5380 Basic Building Block provides for:

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC/AT</td>
<td>All standard motherboard features including serial, parallel, keyboard, clock and floppy/hard disk interface</td>
</tr>
<tr>
<td>VMEbus</td>
<td>Both Master and Slave interfaces with complete slot-1 controller, a Dual-Ported battery backed SRAM, and 16 mailboxes with interrupts to provide an efficient interface for single and multiprocessor configurations</td>
</tr>
</tbody>
</table>
| MODULARITY | Two CPU selections:  
80286 20 MHz for speed  
80386SX for 32 bit addressing  
| | Three Dual-Ported SRAM options  
| | Four System DRAM capacities  
| | Five Video Interfaces - VGA, EGA, LCD, plasma, and EL panels |
| EFFICIENCY | With all options installed, only one 6U VMEbus slot and 20 watts required |
| SOFTWARE | Extensive support including configuration and driver utilities with source code to help get the N5280/5380 operating with the least amount of effort |
| ADD-ONS | Plug in the N7200 Modular Disk Memory with 40MBytes of hard disk, 1.44MBytes of floppy disk, and an SCSI host adapter capable of interfacing an additional six SCSI devices |

FOR A FREE 30 DAY EVALUATION
CALL 800-233-1837 – in California 714-261-8811

TIME TO MARKET IS THE KEY TO YOUR SUCCESS.
HP SoftBench: A software development environment with an integrated set of program development and integration platform tools.

HP AxDB Debugger: Displays microprocessor code, stack backtrace, and variables. Test coverage window shows statements not executed during test.

Interleaf Technical Publishing Software: A documentation software and management system that features integrated text and graphics.

Cadre Teamwork: A family of tools that implement system analysis and software design methodologies.

McCabe Test Tools: An automated software testing and reverse engineering application.

Best CA
Your software release dates are continually postponed. Defects are discovered late in your development process. And your team can’t find contemporary solutions to existing problems.

Hewlett-Packard has a better way.

With the HP CASEdge program and our software suppliers, we offer a broad selection of development tools for the software engineering industry. And a strong commitment to helping your team find, evaluate, and implement the right software engineering tools and best practices for the task at hand.

HP CASEdge solutions speed the automation of specification, design, implementation, debugging, and maintenance. And decrease development costs while getting your products to market faster.

For your next design project, choose the vendor with the best CASE scenario. Call HP today at 1-800-752-0900, Ext. 788R.

There is a better way.
touting to win over reluctant board designers. These tools, used after the autorouter has finished the design, allow users to either add traces that the autorouter couldn’t place, or to modify the board for manufacturing or testability reasons. Racal-Redac’s Visula Route Editor provides an interactive environment for the design engineer. The user simply traces the approximate path that he wants the route to go, and the editor will stitch in the route by pushing aside all obstacles, while observing all the design rules in the defined path. Trace by trace, the designer can switch back and forth from manual to semiautomatic routing. “The beauty of an interactive editor is that it gives the user the control of manual design combined with the power of an autorouter,” says Felton. “If, for example, the designer knows that some traces have to pass through specific points on the board, he can just specify them and the router will figure out how to get the trace to pass that way.”

In addition to the control that an editor gives an engineer, the tools can cut days or even weeks off the design cycle. The Advanced Dynam-
DESIGN AND DEVELOPMENT TOOLS

in 30 seconds or so."
The Mentor editor, like the one from Racal-Redac, lets the designer sketch the path of the trace to be routed and then makes the interconnect according to the design rules. The tool uses squeeze-through and shove-aside techniques to route the trace, and can work with either gridded or gridless designs. Though the interactive capabilities of both the Mentor and Racal-Redac editors are similar to other editors on the market, the way they handle trace placement is different. “Other interactive tools allow the user to place traces,” says Fred Smith, technical marketing engineer at Mentor, “but they first have to digitize all the points along the way. Ours simply looks at the design constraints and obstacles in the path and works around them. The result is almost instantaneous trace placement.”
The need for near-instantaneous results is at the heart of the increasing acceptance of the latest autorouters and interactive editors. “The challenge that autorouter vendors face is giving engineers a tool that will turn a design around quickly and not take a lot of time to learn,” says Jack Hendren, vice-president and general manager of the EDA division of Cadam (San Jose, CA). “Though many of the current design tools are good in the hands of a layout specialist, they can be confusing to an engineer who’s concerned primarily with board design and performance. The trick is to get an engineer to produce a basic design that’s manufacturable in the shortest amount of time. Some of our customers have only six weeks to design a product. That’s an extreme example, of course, but that’s where things are headed.”

If you thought Multibus 1 couldn’t handle complex tasks... Think Again!
From Robotics to CAD, Embedded Controllers to Host and Network Systems, MULTIBUS 1 by Zendex delivers Proven, Cost Effective Solutions that reach out and grab you!

The ZX-386/20 pictured here features 20MHz clock speed and on-board SCSI, supports up to 8MB of high-speed on-board dual-port RAM (or 16MB in PVAM), and has two 8/16-bit ISBX connectors. For Real-Time processing applications, Zendex’s TRU-32 mode turns MULTIBUS 1 into a screaming 32-bit system capable of addressing 256 MB of RAM, yet is fully compatible with MULTIBUS 1 products.

For more information on our complete family of MULTIBUS 1 products, call or write Zendex today!

The ALACRON AL860 Will Make Your Computer a PERSONAL SUPERCOMPUTER
Simply the Fastest Add-In Board for Your Computer
Now in VME!

- Intel i860 RISC microprocessor rated at 80MFLOPS at 40 MHz (66 MFLOPS at 33 MHz)
- 2 to 64 Mbytes of 0 wait state local memory
- Compatible with 80X86 AT bus or 6U VME machines
- Optional 120 Mbyte/sec bus allowing the interconnection of up to 30 boards with a peak throughput of 2.4 GigaFLOPS
- Optional SCSI and DT-Connect Interfaces
- DOS and UNIX interfaces
- C, Fortran, assembler and scientific subroutine library software available

6780 Sierra Court
Dublin, CA 94568
Phone: (415) 828-3000
FAX: (415) 828-1574

CIRCLE NO. 36
CIRCLE NO. 37

COMPUTER DESIGN SEPTEMBER 1, 1990 59
Fiber network supports distributed real-time systems

Tom Williams, Senior Editor

As applications put ever-increasing demands on real-time systems, there is a need to add hardware power in terms of multiple CPUs, as well as operating system services beyond those offered by most embedded kernels. But interprocessor communications, especially over networks, tends to muddy the rigid determinism often required by real-time applications.

Ethernet, for example, is typically nondeterministic because it uses collision detection and retry to resolve conflicts for the media. Thus there is a statistical probability that messages may conflict and have to be retried, and therefore the time needed to ultimately get on the network and transmit isn't predictable. Even processors that are communicating across a backplane can run into bus-contention problems that break down determinism.

The shared memory could also be described as reflective or replicated memory because the contents are exactly the same at each node. A write to any processor's shared memory space is automatically transmitted to the same address in every shared memory board on the network; and this is accomplished without any software overhead. The network electronics monitor the writes from their local CPU to their respective shared memories. Any write results in an automatic ring transmission.

SCRAMNet isn't a token-passing ring like FDDI; instead, it's a register-insertion ring in which the ring appears as a giant circular shift register. Nodes placing a message on the ring simply add the bits of their message to the bits that are being serially shifted around the ring.

Ethernet, for example, is typically nondeterministic because it uses collision detection and retry to resolve conflicts for the media. Thus there is a statistical probability that messages may conflict and have to be retried, and therefore the time needed to ultimately get on the network and transmit isn't predictable. Even processors that are communicating across a backplane can run into bus-contention problems that break down determinism. To be useful for difficult real-time applications, a network scheme must be fast and reliable, as well as offer rigidly predictable timing. To address the needs of distributed real-time systems, Systran (Dayton, OH) has developed a shared-memory network technology based on a fiber-optic waveguide media. Called SCRAMNet (Shared Common RAM Network), the scheme combines the best attributes of message-passing networks and shared-memory architectures for interprocessor communications. It eliminates costly software protocol overhead associated with most networks, and since it's a ring topology, it also eliminates uncertainties caused by contention. And it provides speed—a data rate of 150 Mbits/s, which is 50 percent faster than even FDDI (Fiber Distributed Data Interface).

How it works

The architecture consists of up to 256 computers connected via the fiber link. At each node there is a SCRAMNet interface board with the network interface electronics and from 8 kbytes to 2 Mbytes of shared memory.

The SCRAMNet node board. Each node board on the network contains exactly the same data, which eliminates the contention problems inherent in other multi-processor shared-memory schemes.

In a SCRAMNet node, the dual-port shared memory is mapped into the normal memory address space of a CPU on the network. The application's global variables are resolved so that they're stored in physical addresses on the SCRAMNet board. Each node board on the network contains exactly the same data, which eliminates the contention problems inherent in other multi-processor shared-memory schemes.
Some disk drive companies measure quality in hours.

We measure it in years.

With a never ending commitment to quality that goes beyond MTBF numbers. We back it up with a 5 year warranty on each of our disk drives, including 3.5-inch and 5.25-inch products with capacities ranging from 200-1600 Mbytes.

In fact, at HP, the pursuit of quality is reflected in everything we do. Like striving for continuous improvement in reliability at each stage of the production process, not just at the end. And consistently using reliability improvement tools like STRIFE testing and Design Defect Tracking to find and solve problems to their root cause.

Of course, our attention to quality will have a measured effect on your business. Like reducing your spare parts inventory and field support costs by two thirds.

For more information, call 1-800-752-0900, Ext. 1329 for an OEM evaluation package. Because at Hewlett-Packard, we don’t just prove reliability, we improve it.

There is a better way.
for having a single event simultaneously trigger multiple kinds of activities on different nodes.

**Deterministic timing**

Interruptions are passed on the network in the same way and at the same speed as data. On a 10-node ring, a new value will be available in the memory of all computers on the ring within 2.8 to 6 µs. The latency envelope increases with the number of nodes added to the ring, but it’s a strictly deterministic latency since there is no software protocol overhead or contention problem. The time represents application-to-application communications time, or the time for a variable on one computer to be available to the application code running on the farthest computer on the network.

Each node on the network introduces a fixed amount of latency—from 247 to 800 ns, depending on whether it’s active or it’s set to be passive and, therefore, merely passing data without writing it to its shared memory. But all latencies and ring access times are known and can be used in designing deterministic real-time applications. “We have formulas where you can compute deterministically the performance down to a microsecond, and usually down to a few nanoseconds, when a message will arrive,” Warden says.

To increase network efficiency, the SCRAMNet electronics include data-filtering logic that monitors writes to shared memory. Only those writes that produce a change in data are actually transmitted on the network. According to Warden, measurements in an aircraft flight-simulation application have shown that the data-filtering technique filtered out about 75 percent of the network traffic, increasing effective network bandwidth by 400 percent.

SCRAMNet controller boards are available for several popular buses, including Multibus II, VMEbus, Q-bus and Unibus. To make it possible for different CPUs to transparently use the network, the controllers include a byte-swapping feature. This allows them to handle the incompatibilities between big-endian and little-endian integer formats imposed by different CPU architectures. Little-endian is the format where the least-significant byte in a word is stored at the smaller address. Big-endian has the most-significant byte at the smaller address. All the system designer need do is set each board for the appropriate hardware translation to use any CPU on the network.

Call us:

**ALFCO AIR FILTRATION SPECIALISTS**

1000 CINDY LANE, CARPINTERIA, CA 93013  FAX (805) 684-3654  TEL. (805) 684-7651

CIRCLE NO. 39
CMC, world leader in VMEbus Ethernet products, has forged a second generation architecture worthy of our stature.

FXP, Full Throughput Architecture. The culmination of over five years’ experience and tens of thousands of installed nodes. The power behind the highest performance Ethernet network processors available—the CMC-130 series.

▲ A 20MHz 68020 processor with its own separate program and data memory processes more than 2,000 packets per second.

▲ 256KByte Video RAM as global dual-ported data buffer memory to move packets at full Ethernet and VMEbus data rates.

▲ LANCE™ Ethernet interface reliably handles back-to-back packets to provide full 10Mbits throughput.

▲ Autonomous DMA engine bursts data in block mode at up to 38MBytes/sec providing maximum efficiency to VMEbus host processors with minimal interrupt loading.

▲ CMC’s link level driver for the CMC-130 series supports UNIX® host-based protocols. CMC’s FDDI products also employ this same driver, allowing developers to use common applications for both Ethernet and FDDI networks.

CMC, the first supplier of intelligent VMEbus Ethernet interfaces, remains committed to supplying fully compliant on-board TCP/IP and OSI protocol suites that off-load the host.

The CMC-130 series is backed by a complete two year hardware warranty, as well as a comprehensive development environment, superior training and unmatched support.

To connect with the power of FXP and join the Ethernet performance vanguard, call today.

1-800-CMC-8023

CIRCLE NO. 40

Designed well. Built well. Rockwell.
Rockwell CMC
125 Cremona Drive, Santa Barbara, CA 93117
PHONE: 805/968-4262 1-800-CMC-8023
FAX: 805/968-6478 TELEX: 240876
The IBM RISC System/
Designing on any other workstation

Whatever you’re creating, you’ll sail into a whole new age with any of the four POWERstations in the RISC System/6000 family. Because POWER (Performance Optimization With Enhanced RISC) processing can give you performance you’ve probably only dreamed about:

- up to four instructions per machine cycle, 42 MIPS and 13 MFLOPS. Suddenly, complex designs don’t take long anymore.

The four RISC System/6000 POWERstations feature a range of graphics processors from grayscale to Supergraphics to satisfy any graphics demand. Great news for Power Seekers working on animation, scientific visualization, medical imaging and engineering solutions like CADAM, CAEDS™ and CATIA™.

And for electrical design automation, there’s IBM’s all new CBDS™ and an arsenal of over 60 EDA appli-
6000™ family. will seem downright primitive.

With every POWERstation, you can get an almost unimaginable palette of 16 million colors, which gives you 3D images so realistic, they fairly leap off the screen, with super sharp resolution of 1,280x1,024 pixels. And when it's time to call in the heavy artillery, the POWERstation 730 draws nearly one million 3D vectors per second. Like all POWERstations, it can come complete with its own graphics processor, freeing the POWER processor to rapidly create and analyze your designs. All at prices that won't sink anybody's budget.

So if you're tired of paddling upstream with yesterday's performance, call your IBM marketing representative or Business Partner to find out more about the RISC System/6000 family. For literature, call 1 800 IBM-6676, ext. 991.

Civilization never looked so good.

For the Power Seeker.

CIRCLE NO. 41
Small, reliable STD SBCs move into PC territory

Warren Andrews, Senior Editor

STD Bus, with and without the 32-bit extension, continues on a roll as demand surges for small, reliable PC compatibles. The latest round of STD Bus products reflects that demand—80286 and 80386 SX machines have entered the market, rivaling the best of the desktop units in performance while exceeding them in reliability, ruggedness and compact size. What's more, 386 DX and even 486 STD boards are on the drawing board— and in one case, already in the breadboard stage.

"Customers are looking for compact solutions to embedded control problems in both DOS and Unix environments," says Jim Eckford, director of marketing for Ziatech (San Luis Obispo, CA). According to Eckford, some customers are looking for a complete system in a small card cage with only a few slots, while others are looking for a single board they can embed in their products. Either way, customers are looking for smaller yet more powerful STD solutions," he says. "Size is turning out to be the most important feature of STD Bus."

As a result of the demand, an entire new family of STD products has been emerging over the past year, sporting high-performance processors, memory, and as much as- sorrted I/O as will fit on the small form-factor card. In addition, many of these boards provide hard and/or floppy disk interfaces, some kind of video port, some digital I/O, a keyboard interface and at least a serial or parallel port.

Kurt Priester, president of Computer Dynamics (Greer, SC), one of the many companies offering high-performance PC-compatible machines on STD, agrees with Eckford about the rising demand for small form-factor PC compatibles, but adds that "the other critical component in the formula is quality." Priester maintains that many PC applications fall from grace as the PCs prove unreliable.

"It's not uncommon," says Priester, "for companies to develop systems based on a conventional desktop PC only to have downtime wipe out all the gains made by automating a process. So many designers are turning to STD for the added reliability—the reduced size is simply an added bonus. With the latest generation of high-performance machines available on STD, there's no need to sacrifice performance or features to switch to STD."

WinSystems (Arlington, TX) is another of the STD makers that has been one of the leaders of the high-performance PC-compatible bandwagon. "The advanced PC chip sets provide the necessary functionality and space savings to allow complete PCs to reside on a single STD board," says Bob Burckle, WinSystems director of marketing. "The Chips and Technologies chip set that we use not only provides the housekeeping and peripheral functions for the PC but also provides clock signals to allow the processor to zip along at its top speed internally, while the backplane is allowed to operate at another speed. This means that the processor's performance isn't impaired by the relatively slow STD Bus, which isn't the case with some other solutions," he says.

Slight differences

Interestingly, the various approaches taken by STD vendors making PC compatibles differ only slightly. Computer Dynamics, for example, in its CPU-AT provides a 25-MHz 286-based board with up to 4 Mbytes of memory, and the company claims that the CPU-AT is 100 percent PC/AT compatible. In addition to the processor and memory, the board has room for a 256-kbit EPROM, two RS-232 ports, a printer port, a floppy disk controller, an IDE hard disk interface, a battery-backed real-time clock and CGA, EGA or VGA video. Furthermore, Priester claims that it's one of the few STD CPUs set up to drive flat-panel displays including LCD, plasma, electroluminescent and vacuum fluorescent.

The entire system, however, doesn't reside on only one card. The processor, memory, I/O ports and EPROM reside on one board, while the video, Winchester and floppy controllers reside on a daughtercard that plugs directly onto a connector on the host processor board. "This dual-board approach was taken for two reasons," says Priester. "First, there just isn't enough room on the processor board for the rest of the functions and the mother/daughterboard is a good way to make more room. Second, many customers simply want to embed the processor and memory functions with or without a card cage. The CPU-AT processor module permits that without the expense of including the disk and video interface functions."

"Right now, we're using the 286 processor because it offers equivalent—or better—performance than the 386 SX at a lower price," Priester says. "Unless the advanced memory features offered by the 386 SX are critical, there's no reason that I
FDDI.
Build with the power of FXP.

CMC, world leader in VMEbus Ethernet products, has forged a second generation architecture worthy of our stature.

FXP, Full Throughput Architecture. The culmination of over five years' experience and tens of thousands of installed nodes. The power behind the highest performance FDDI network processors available—the CMC-1000 series.

- A 25MHz Am29000™ RISC processor with its own separate program and data memory processes up to 30,000 packets per second.
- 512KByte Video RAM as global dual-ported data buffer memory to move packets at FDDI speeds and handle high VMEbus latency.
- Supernet™ FDDI chip set configured for dual- or single-attach operation coupled with high-speed 256KByte buffer memory provides full 100Mbps throughput.
- Autonomous DMA engine bursts data in block mode at up to 38MBytes/sec providing maximum efficiency to VMEbus host processors with minimal interrupt loading.
- Complete Station Management software fully complies with the latest ANSI X3T9.5 standards for maximum interoperability.
- CMC’s link level driver for the CMC-1000 series supports UNIX® host-based protocols. CMC’s Ethernet products also employ this same driver, allowing developers to use common applications for both Ethernet and FDDI networks.

CMC, the first supplier of intelligent VMEbus Ethernet interfaces, remains committed to supplying fully compliant on-board TCP/IP and OSI protocol suites that off-load the host.

The CMC-1000 series is backed by a complete two year hardware warranty, as well as a comprehensive development environment, superior training and unmatched support.

To connect with the power of FXP and join the FDDI performance vanguard, call today.

1-800-CMC-8023
CIRCLE NO. 42

Designed well. Built well. Rockwell.
Rockwell CMC
125 Cremora Drive, Santa Barbara, CA 93117
PHONE: 805/968-4262 1-800-CMC-8025
FAX: 805/968-6478 TELEX: 240876

FXP is a trademark of CMC. Am29000 and Supernet are trademarks of Advanced Micro Devices, Inc. UNIX is a registered trademark of AT&T. ©1990 CMC.
can think of to use the SX." But the 386 DX is a different story, according to Priester, and he expects his company to develop a 386 DX machine soon.

WinSystems also provides a high-performance 286-based machine with similar functions. And this company, unlike Computer Dynamics, offers a board using a 16- or 20-MHz 386 SX. WinSystems' 386 SX board allows for automatic switching between 8- and 16-bit transfers and, like other approaches, separates the disk and video interface from the main processor board. A specially modified Phoenix BIOS allows the board to boot off either disk or ROM.

STANDARD 32

Ziatech, not unexpectedly, used the company-developed STD 32 for its latest 386 CPU board. STD 32 has been on a popularity roller coaster since Ziatech first announced it almost a year ago. It still has only a limited following, and some supporters who had initially expressed a favorable response, such as Computer Dynamics' Priester, have recently displayed considerably less enthusiasm. Further, the STD Manufacturers Group appears to be no closer to endorsing the concept than it was six months ago.

Despite the ups and downs, Ziatech and a small group of vendors calling themselves Task Group 32 have gone ahead and finalized the specification, provided nonrecurring engineering expense monies for the manufacture of the connector, designated a connector manufacturer, and set up licensing rules. In addition, the group has cleared the use of the EISA specification and settled other legal issues that could have been obstacles. Still, reception to STD 32 has been cool at the STD vendor level due to what Priester describes as "political problems."

Though connectors and backplanes for STD 32 won't be available until October, Ziatech has been making its CPU board for some time. "You have to remember that STD 32 is fully compatible with all existing 8-bit backplanes and systems," says Eckford. Ziatech's 386 SX-based CPU approach is similar to Computer Dynamics' and WinSystems' in that it uses two boards: one for processor/memory and another for video and disk control.

Ziatech's processor/memory board is a full 32-bit 386 SX with 8 Mbytes of memory, a pair of serial ports, a parallel port, a keyboard interface and all the other features normally found on a CPU. A companion card includes the floppy disk and hard disk controllers and VGA port. "These two boards combined with a floppy disk drive and a 40- or 105-Mbyte Winchester make an attrac-

100 MFLOP ENGINE

Based on Motorola's 50 MFLOP 96002, Ariel's Dual DSP MM-96 blasts through real time signal processing, graphics, floating point number crunching and multimedia applications like nothing else.

The MM-96 hooks directly to frame grabber cards via its DT-Connect™ interface and to digital audio with Ariel's DSPnet™ multimaster bus.

Configurations for IBM AT compatibles are available up to 16 megabytes of memory and complete development software (including an optimizing C compiler, host drivers, and demo software).

Ariel provides the best applications support in the business via telephone, mail, fax, or our 24 hour DSP BBS.

The MM-96 is available now. Call for 96002 support on other platforms.

DT-Connect is a trademark of Data Translation, Inc. DSPnet is a trademark of Ariel Corporation.

©1990 Ariel Corporation.
NEW...Warrior-III

The ultimate subroutine machine.

The ultimate, the best. A board level array processor whose i860, and i960 combination make it the most megaflop friendly array processor available. It is a full three to six times faster than its predecessor the Warrior-II. The two internal processors are supported by either fast SRAM or cached DRAM memory. Coupled with a 160 Mbyte per second internal bus you've got a real screamer. 80 Mflops, 40 MIPS peak performance.

Single slot 6U and 9U VME
Supercomputing on a single slot board. Memory from 1/2 to 64 Mbytes. The board includes a VSB bus interface and an additional expansion port. SKY also offers standard I/O daughter cards such as a 32-bit parallel interface. Or if you like, you can customize your own interface. And, multiple Warriors can be used without special cabling.

Real DMA
The i960 executive controls a powerful DMA engine capable of addressing host memory and external devices. There is no tie up of the i860 to accomplish this. And, since internal interrupts don't affect the i860, you get more usable megaflops. Real horsepower to solve problems like image processing, signal processing or matrix manipulation.

Software support
Add to this built in source code compatibility with the Warrior-II library, advanced features like command chaining, user built command blocks, and tools to do custom routines. The result, the most competitive board level array processor on the market.

Want to find out more?
Circle the bingo, and we will send you more data or give us a call. We can have a SKY technical representative contact you immediately.

---

SKY Computers, Inc.
27 Industrial Ave.
Chelmsford, MA 01824
Tel. (508) 250-1920
FAX: (508) 250-0036
CIRCLE NO. 44
Looking ahead
Ziatech's existing package is only the tip of the iceberg, according to Eckford, who says his company realizes that board compactness is critical to many applications and is compacting its designs even further. Ziatech will soon unveil a 286-based card with even more I/O than existing cards. To squeeze in the additional functionality, the company is taking advantage of its recently developed ASIC I/O chip designed to provide high-density, high-current digital I/O.

The 286 board is expected to boast 48 digital I/O points in addition to memory, serial and parallel I/O. "The digital I/O chip we developed is just the first of many we plan to develop to increase functionality on the postcard-sized STD form factor," says Eckford. "Even though the chip was used in a few current products and will be incorporated into several emerging products, it was really a test-bed for our ASIC strategy, and we expect to be developing more custom chips."

While STD vendors are looking to compact more functions on their boards, they also have an eye toward boosting performance. Computer Dynamics and WinSystems are running 286-based machines at 20 and 25 MHz, and WinSystems and Ziatech are running 386 SX boards at 16 and 20 MHz. Computer Dynamics, as mentioned, is planning to develop a high-speed 386 DX machine soon, while Ziatech may well jump the gun and offer a 486 machine in the not-too-distant future. "Right now, it's too early to tell whether—or when—a 486 STD product will emerge," says Eckford, "but we have a breadboard of a full 486 EISA machine already completed. Since STD 32 operates on a subset of the EISA specification, an STD 32/EISA design could become a reality in a relatively short time."

And some vendors that are looking to stretch the performance envelope are also looking to put STD/PC power in customers' hands at increasingly lower prices. "WinSystems has just announced a new low-priced CPU for those embedded applications calling for moderate PC performance at a moderate price," says Burckle. Based on an 80188 processor, the WinSystems board is priced under $200.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Computer Dynamics
(803) 877-8700 .................................................. Circle 225
WinSystems
(817) 261-1801 .................................................. Circle 226
Ziatech
(805) 541-0488 .................................................. Circle 227
NOW! IMAGE PROCESSING

SO FLEXIBLE,

YOU RUN THE SHOW.

Matrox has redefined imaging for the 1990's. The revolutionary IMAGE Series delivers peak hardware power and lets you scale the boardset to your application. The most advanced semiconductors and 12 custom gate arrays are combined to provide a major breakthrough in performance, capability, packaging and price.

The IMAGE Series brings you color acquisition, real-time processing, 1280 x 1024 display resolution, powerful graphics and... spectacular price/performance numbers in an integrated product line. Input device interfaces, reconfigurable image memories and an optional 1000 MIPS programmable pipelined processor communicate over the high-speed 30 MHz IMAGE Bus.

IMAGE Series: Powerful, Modular, Scalable.
Let's talk about the details.

Matrox is a registered trademark of Matrox Electronic Systems Ltd. In Canada: (514) 685-2630

1-800-361-4903

CD-IMAGE 9/1/90

matrox

THE LEADER IN VIDEO MICROTECHNOLOGY
“Simply the best... by Design”

“We're new, and new companies must offer better solutions”

Super High Performance Backplane
- Full VME Specification
- 10 Layer Stripline Construction
- Virtually Zero Cross Talk
- Controlled Impedance
- Noise Reduction

New Enclosure Design
- Aluminum Construction
- Easy to Access
- Direct Flow Cooling

Call 1-800-628-4095

Graham Electronic Manufacturing Inc,
109 State Pl, Escondido, CA 92025,
(619) 747-9177 FAX (619) 747-9326
DSP chips stalk industrial buses

Ripe for new roles, DSP chips are slowly making their way onto VME and Multibus boards. But system designers are tentative about the prospects.

Warren Andrews
Senior Editor

Not too many years ago, when the first single-chip digital signal processing devices became available, they were heralded as the second coming of the microprocessor. Now, several years later, the blush seems to have paled somewhat even though the latest generation of floating-point chips has recently become available. Though having found a home in many high-volume niches, these chips still have failed to realize their anticipated use. The board business has followed a similar trajectory. Despite a growing number of product offerings on personal computer and industrial buses, DSP boards remain more of a laboratory curiosity than the backbone of industrial automation and control systems.

Why? “There are a lot of reasons,” says Cimarron Boozer, industry marketing manager for Sky Computers (Chelmsford, MA), one of the leaders in industrial DSP boards. “A main one is that there are a lot of designers who prefer to roll their own DSP boards to suit a particular application,” he says. “The business for DSP is largely fragmented, calling for a lot of different and specialized designs.”

But more important, there seem to be other obstacles. DSP is still relatively new and system designers are somewhat tentative about jumping into the unknown. Astute observers point out that the term “signal processing” may itself account for some designer reticence. Signal processing has traditionally been the domain (no pun intended) of analog designers who turned to digital techniques to solve what are essentially analog (signal) problems. Therefore, the high-powered mathematical techniques available as part of DSP technology are most often found solving typical signal processing/conditioning chores such as switching from a frequency to a time domain, modifying the result and swapping back to the frequency domain or vice versa.

But the capabilities of DSPs and the techniques and algorithms they employ extend beyond those tasks normally associated with analog signal processing. Yet few designers have taken advantage of these capabilities. Instead, designers have walked around DSP solutions, finding more conventional solutions to DSP-like problems.
DSP ON BUSES

THE PENTEK 4283 PROCESSOR BOARD

Aside from the fact that the concept of signal processing might intimidate designers, there is also some confusion as to what DSP is, compared with array processing or simply specialized accelerators (see "Choosing the right accelerator technology," p 75). The idea of DSP has developed such a narrow focus that these other names have been appended to basically the same functions and capabilities used in signal processors but with, perhaps, a somewhat wider scope.

History intervenes

Another factor hindering the advancement of DSP techniques into other areas of processing is the traditional development and programming environment that has surrounded DSP. To understand that environment, it's important to look at DSP with some historical perspective. DSP functions are highly iterative manipulations crunching through relatively small amounts of code very fast, and many times over. In any look at price/performance, the emphasis in DSP has always been on performance. As a result, DSP programs have traditionally been written in assembly code to fit into the relatively small on-chip memory that DSP chips provide and to speed execution.

Thus, many of the development tools for the DSP chips have evolved independent of, and totally different from, traditional system design tools. Such tools include everything from compilers and debuggers and assemblers to in-circuit emulation devices. The maxim was, DSP designers aren't system designers, so there's no need for DSP designers to operate in the Unix or real-time operating system world. Consequently, development environments tended to focus on the individual chip rather than on the system.

But as system designers' demands change, so do DSP approaches. And though chip makers such as AT&T (Murray Hill, NJ), Texas Instruments (Dallas, TX), Motorola (Austin, TX), Analog Devices (Norwood, MA) and others recognize the needs of system designers, there has been little movement to integrate DSP into nonsignal applications.

Even at the board level, where tools are more readily available and hardware designs well polished, "most of the applications are in conventional signal-processing applications, such as speech processing, radar, medical imaging, sonar and communications," says Rodger Hosking, vice-president of Pentek (Rockleigh, NJ), maker of both VME and Multibus DSP boards.

One approach

While many of the offerings of DSP hardware are conventional boards operating within the confines of a host system bus, there is a growing tendency toward using mezzanine or daughterboards. Two of the most distinctive of these offerings are from Io (Tucson, AZ) and Pentek.

Io's daughterboard, the MathCOP2 floating-point coprocessor, is a full-sized 6U VME board that plugs into a standard VMEbus slot in a card cage next to an Io CPU card. The MathCOP2 daughterboard, though plugged into the host P1 connector, draws only power and ground from the host system and is connected directly to the adjacent CPU board. Therefore, the board uses no VMEbus bandwidth and occupies only a single VME slot.

Io's MathCOP2 is based on the 2100 floating-point chip set from Bipolar Integrated Technology (Beaverton, OR) and is designed to operate at better than 30 MFlops. It consists of a multiply/divide component and an adder/Boolean component. Both of these are connected to a four-ported register file providing sixty-four 32-bit operating registers. In addition, there is a local SRAM that can hold up to 64,000 32-bit words of data. Program instructions for the coprocessor reside in a separate microprogram memory, which has capacity for 2,048 80-bit instructions.

Because the board uses two parallel floating-point processors—one for multiply, divide and square root and the other to add, subtract and perform data conversions and Boolean operations—complex operations can be handled with single commands.

The addition of program storage space on the board is as much responsible for its performance as the native speed of the BIT parts. According to Tom Sargent, Io's president, the performance of a Motorola 68881 math coprocessor, combined with a 68020/030 processor as the system host, limits the math speed by the rate at which commands can be passed from the host processor to the coprocessor. But being able to download a sequence of instructions into the board's program memory...
Choosing the right accelerator technology

With RISC chips doubling in performance every 18 to 24 months, workstations have made enormous strides in technical computing power. But despite these advances, workstations are still a far cry from the supercomputing performance that engineering and scientific users often need for their applications.

When combined with the new class of third-party accelerator products, however, workstations can speed up many technical applications to near-supercomputing levels. But it requires matching the right application with the right accelerator product. Unfortunately for end users, accelerator products come in many guises these days, provoking much confusion and frustration.

There are three types of technologies that are capable of achieving double-and triple-digit Mips and MFlops performance on the desktop: application accelerators, array processors and digital signal processors. Understanding how they each work will help end users avoid making misguided purchasing decisions.

Application accelerators

Application accelerators are ideal for such applications as computational chemistry, molecular engineering, finite element analysis, computational fluid dynamics, modeling, computer-aided design, simulation and financial analysis. Unfortunately, there's a lot of confusion about what constitutes an application accelerator. The term has been used loosely to market everything from add-on simulation hardware to faster memory boards.

Sky Computers defines application accelerators as a specific technology that transparently accelerates numerically intensive applications without requiring modification to the source code. The technology is a general-purpose solution for working with all types of numeric data—both integer and 32- and 64-bit floating-point—and the architecture is balanced to accommodate both scalar and vector processing.

Application accelerators serve as coprocessors that work in parallel with the host computer. If users have complex programs that use a variety of data types organized as scalars or vectors, or if users are concerned about accelerating more than one type of application, then application accelerators are the most efficient, cost-effective solution.

They are supported by a set of programming tools and software, including vectorizing Fortran and C compilers, debugging tools, libraries of often-used routines, simulators and profilers. But users must ensure that the accelerator they select supports their operating system calls. If it doesn’t, their programs won’t run transparently, and users must develop their own system interface code or do “work-arounds.”

For this reason, many accelerators are available for Unix machines. The Unix operating system calls use established standards, and if vendors support them, they can truly call their products transparent application accelerators.

Array processors

Array processors are best suited for applications involving repetitive arithmetic operations on large data sets or manipulation of floating-point data arranged in vectors, or arrays. Examples of such applications include medical image processing, real-time 3-D graphics, geophysical analysis, automated test, and radar and sonar signal processing.

Array processors accelerate applications by pumping multiple array elements through a highly optimized processing pipeline.

Users of array processors often modify their programs to take advantage of special subroutine libraries, typically vector and matrix routines. Array processors are optimized to do some tasks well, such as fast Fourier transforms and vector operations.

These processors are supported by a library of vector and matrix routines callable from high-level programming languages such as C or Fortran. In operation, the application executes on the host computer and passes data and commands to the array processor. Array processors aren’t good at programs that can’t easily use subroutine calls, or applications that are scalar in nature.

Array processors offer users the benefit of having ultimate control over their applications. They can control such functions as I/O, dataflow and arithmetic processing. Of course, more effort is required to develop applications for array processors than for application accelerators.

Digital signal processors

For applications dealing with signal processing—radar, sonar, speech/voice processing and real-time control, for example—digital signal processors are a popular solution for increasing application speed. These processors accept large quantities, and often continuous streams, of data. DSP applications typically have small memory requirements because of small algorithms and because applications often perform data reduction.

The architecture of DSPs is optimized in favor of the specialized range of algorithms used in signal processing, such as finite impulse response filters. Software includes a library of signal-processing routines that execute on-board. It also includes host routines that allow a program executing on the host computer to communicate with the board.

Traditional DSPs have been fixed-point processors. This allowed a fairly low cost chip to be used in embedded systems. The drawback was that algorithms that needed floating-point capabilities had to emulate floating-point computations.

Some of the newest DSPs, however, work with 32-bit floating-point data, so users can now program their applications using 32-bit floating-point arithmetic. The 32-bit precision is more than adequate for most DSP applications that involve 12- or 16-bit input data.

In general, for an application accelerator, array processor or DSP to be successful, it should meet one basic criteria: a workstation equipped with one of these products should run a numerically intensive application at least five times faster than a workstation lacking such a product. And on certain types of numeric processing, a 10- to 20-times performance improvement should be achievable.

Bruce Rusch, BSEE, president and chief executive officer, Sky Computers
DSP ON BUSES

eliminates this type of overhead. It allows the coprocessor to fetch the instructions for itself automatically, freeing the host CPU to manage the data flow. The board is capable of fetching 20 Mips—many times the rate a host processor could supply them.

Mixing the buses

While I0 has taken its full-sized daughterboard approach, Pentek has adopted a totally different tack, stealing some of its Multibus II TMS320C30 Mix daughterboard technology for adoption on VME. Pentek’s Multibus II entry, based on Intel’s Mix (Modular Interface Ex-

the limited space in a VMEbus card cage, three Mix modules plus the VMEbus baseboard occupy four slots,” says Hosking.

Other Multibus solutions

Pentek’s Mix approach is one of the few DSP solutions available on—or for—Multibus II. One of the few other solutions—and one of the first, in fact—comes from McDonnell Douglas (St. Louis, MO). “This Multibus II DSP board,” says senior lab engineer Brian Leger, “was designed early on in the life of Multibus II.” Since then, the board has continually been updated from the initial 32020 version, to the 320C25 and the soon-to-be-introduced 320C26 version.

The board was designed to synthesize aircraft sounds for the company’s flight simulator. In addition, the board synthesizes special pilot signal tones as well as speech synthesis and analysis. The updated version, says Leger, allows for about three times the on-board RAM, increasing the 16-bit-wide memory from 0.5 to 1.5 kwords. This will allow a monitor to be written for the chips’ serial ports. Each of the boards uses four 320C25s now and will share the same complement of C26s. The only other major Multibus II offering comes from Micro Industries (Westerville, OH), which McDonnell has licensed to make the C25 board.

Most target VME

By far, the greatest number of DSP solutions appearing on industrial buses are emerging on VME. According to the 1990 VME Compatible Products Directory, 18 different manufacturers report making DSP VMEbus products. Five of those make products based on TI’s 320 family of chips, eight use Motorola’s 56000, and six are using some other DSP chip or chip set, including AT&T’s DSP16 and DSP32C, Analog Devices’ AD2100, BIT’s 2100 chip set or other solution.

Sky Computers offers a complete line of VMEbus-based products for straight DSP applications, array processing and application acceleration, according to Boozer. Sky’s latest product is the third generation in its family of 320-based products. Boasting a pair of 320C30 processors, Sky’s Challenger-C30 provides up to 66 MFlops and 32 Mips.

One of Sky’s first customers—and
The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face. Interphase delivers those solutions.

**PROVEN FDDI SPEED AND INTELLIGENCE**

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

**TOKEN-RING RESULTS**

The V/TOKEN-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

**ETHERNET CHOICES**

Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.

**GET YOUR NETWORKING NOW**

No matter what your networking need—FDDI, Token-Ring or Ethernet—Interphase is ready to provide the solution. For more information call today:

**(214) 919-9000**
DSP on Buses

The parallel port—which can be thought of as a fully programmable high-speed local bus—can be used to daisy-chain multiple boards together or to interface with other high-speed devices such as A-D or D-A converters.

The parallel port—or ports, more often—is a fixture on almost all of the commercially available DSP boards. Obviously, the processor is capable of operating on data far faster than it can be transferred over the host system bus and/or stored in local memory. Furthermore, in many typical applications, multiple processes are going on simultaneously, with one processor feeding the results of its calculation to the next and so on down the line.

It’s interesting that there is little commonality between the external propriety ports of various boards. A board being developed by Loughborough Sound Images (Loughborough, UK), which also sports a pair of 320C30s, uses two very fast private buses, according to Bill Meschach, consulting engineer at the company. Meschach says the company looked carefully at other alternatives, including secondary buses such as VSB and ‘standard’ mezzanine buses, but found that none could provide the type of performance required.

Loughborough Sound has developed a broad family of DSP boards on both VME and PC buses using the Analog Devices, TI and Motorola DSP chips. Spectrum Signal Processing (Waltham, MA) markets Loughborough’s products in North America.

Megafloppage

Local buses take on added significance when tying DSPs together on a single board. While boards based on multiple 320C30s are starting to approach 60 MFlops and beyond, the real performance winner is a VMEbus board from AT&T. The board was designed as a multi-purpose development platform to provide raw processing power for analog interface applications and software tools, according to Jim Snyder, member of the technical staff at the Murray Hill signal-processing research group.

The 6Ux160 VMEbus card combines two “clusters” of three 50-MHz DSP32C processors, achieving an unparalleled 150 MFlops. And while Snyder takes justifiable pride in the performance of the AT&T board, he explains that the “megafloppage” claims by themselves aren’t what’s most important.

What really counts, says Snyder, and what designers are looking for, is a system that can take a signal in the front end, do some serious processing and send it back out the other end in as close to real time as possible. This frequently takes the form of taking information in and doing some kind of transformation on the front end—for example, converting from one standard domain, such as frequency, to another, such as time. The signal is then processed according to some set of routines and then transformed and sent out.

Transformation can, for example, take the form of a fast Fourier transform at the front end and an inverse FFT at the other end.

AT&T’s VME board, says Snyder, is well equipped to do exactly that. Similar to other high-performance DSP cards, it has a high-speed port on each node, and a bus and memory interconnecting the two clusters of DSPs. The board provides a real-time data path on a serial link to all the DSP32Cs in the system.

Each “cluster” of processors comprises two DSP32C5E processors and one DSP32C. The two processors differ in that the 5E has no external memory-accessing capability. Between the two clusters is up
The Multibus II product line has changed.

We've dramatically reduced your costs and added dozens of products. And that's great news when your designs call for more than a PC.

Today, our Multibus II system with a 386" CPU, disk, tape, and 4MB of RAM is priced at just $9,995.

And the costs of our Multibus II single board computers are down as much as 47%.

Now you can build the Multibus II discipline right into your system for the price of VME or EISA. Multibus II's new MPI bus interface chip is perfect for building simple analog, digital, or serial interface boards. It costs just $40 in quantities over 100.

The Multibus II product line has expanded, too. In the last year alone, we've added over a dozen I/O and CPU board products. And you can choose from the more than 500 Multibus II products on the market, including 150 full-size Multibus II boards.

Need help migrating from VME? Our single-slot VME-to-Multibus II adapters will give you a jump on switching your custom VME boards to Multibus II.

To view the entire expanse of Multibus II products—from over 100 vendors—call Intel at (800) 548-4725, Dept. AA60. Ask for a free copy of the 1990 Multibus II Product Directory.

So don't delay. Call now, and start a change for the better.
to 4 Mbytes of DRAM, which is accessible to either cluster as well as to the host VMEbus. Each cluster also has its own 256 kbytes of memory, and each processor has 8 kbytes of internal memory.

The need for tools
As each new generation of processor emerges and is harnessed in some board-level implementation, successive boards will continue to leapfrog its precursor in performance. But designers need tools to effectively utilize that performance. "The challenge to the board maker is to provide better packaging, make the product even easier to use, and provide the software tools necessary to let a designer solve a problem," says Boozer.

The basic tools to implement a filter, FFT or other function are provided by the chip makers. But the rest of the pieces to the software puzzle—integration with an operating system such as SPOX, interface to utility routines and documentation—is lacking. "These are the types of things—the value added—that Sky provides with its hardware platform," Boozer says.

Sky provides full DSP support for Sun-3 and Sun-4 workstations running SunOS. The software consists of host utility routines, C30 usage-support routines, a multiboard debugger, Sun device driver and the SPOX DSP operating system. The SunOS driver supports up to 16 simultaneously active dual-processor C30 cards. Programs can be written in T1's 320 C and can include assembly-language statements for faster execution. For fine-tuned applications, the entire program can be written in the C30 assembly language. The board uses T1's standard tools to compile, assemble and link programs.

Others have gone even further in providing a development environment. AT&T, for example, has an extensive library of software routines for its DSP32C, but has supplemented them with a variety of other tools including a source-code debugger and a tool called DSPX, which provides library functions in C and provides for direct connection between the DSP function and a Unix-based operating system.
Most likely, if you need SNA compatibility, you’ll buy the software source code from one company and hardware from another. Then you’ll spend several months desperately working out the integration.

Or worse, you’ll design it from scratch.

Systech knows you’ve got better things to do with your time. So we’ve created a way to cut down that lengthy process. With OneStep™.

OneStep is a complete SNA/DCP board package. Which makes it the quickest and easiest off-the-shelf solution for IBM communication. In fact, with our help, the OneStep can be up-and-running in just five days.

To make this unique integration work, we teamed up with the most reputable and experienced company in IBM compatibility around—Systems Strategies, Inc. With their superb emulation software and Systech’s modular design, OneStep gives you the wide-area links you need for VME and Multibus systems. What’s more, the OneStep takes a load off your CPU. That way, you have more power and improved system performance overall.

Systems Strategies, Inc’s extensive variety of popular protocols includes SNA 3270, RJE and LU6.2, BSC 3270 and RJE, Plus, X.25 and QLLC. All thoroughly tested and successfully ported to Systech’s hardware.

Along with easy installation, the OneStep will keep your up-front costs down. And its modularity makes it easy to maintain and upgrade.

Most importantly, with the experience and expertise of Systech and Systems Strategies, Inc., you’ll be in step with the latest software and hardware developments. And you’ll always be OneStep ahead of the competition.

For a demonstration or more information, call Systech at (619) 453-8970. Or write: Systech Corp., 6465 Nancy Ridge Dr., San Diego, CA 92121.
To See What a UniFLEX Real-Time Operating System Has to Offer...

...Just Open a Window

Then get ready to be amazed. Because UniFLEX® is the most complete solution available for real-time embedded systems.

It all begins with X Windows, a graphical user interface that features window managers and terminal emulators. And Motif™, the most powerful X-based development environment for graphics applications.

Then you'll find the highest level of UNIX® compatibility in any real-time system. Bringing immediate access to a growing source of UNIX programs. And programmers.

For networking, UniFLEX features the ease of NFS™, plus all TCP/IP networking utilities and a complete C library of BSD socket functions and rpc routines.

And when you need multiprocessing capability, UniFLEX is unsurpassed. Dynamically balanced systems are available for applications requiring the power of up to sixteen closely-coupled processors.

UniFLEX saves time as well. Because it's not only fast, it's self-hosting. You design and debug in one system without flopping between host and target. And targets can even be modified right in the field.

After nine years, UniFLEX has been honed to perfection. With over forty device drivers available off-the-shelf, supporting a wide range of peripheral devices. And it's available on most VMEbus single board computers such as Motorola®, Force and Ironies. Not to mention Macintosh®.

So if you're looking for the most complete real-time operating system, call us at 1-800-486-1000. Then just open a window. And be amazed at what UniFLEX has to offer.
16-bit MCUs diversify to survive

Seeking to secure their niche in the gap between cheap and powerful, 16-bit architectures take distinct approaches to meeting application demands.

Ron Wilson
Senior Editor

Like species struggling against a harsh environment, 16-bit microcontroller families are seeking out niches where they can survive and prosper. In the process, the chip architectures are diverging from each other, increasingly reflecting their differing origins. Design managers must be aware of these differences if they're going to find the right chip for their application.

"It's amazing how each of these 16-bit chips fits into a different niche," says Nicholas Andrews, president of real-time kernel vendor Byte-BOS Integrated Systems (San Francisco, CA). "Each one has a different blend of cost, power consumption, memory size and peripheral support."

Many of the characteristics of a particular 16-bit architecture follow directly from the vendor's original concept of the market. The earliest 16-bit MCUs, for instance, were point products, designed for—and often with—a particular customer for a particular product. These chip families have grown by elaborating on the original design.

Other families grew out of vendors' notions of product migration. Some predicted that as code grew larger and functions grew more complex, there would be a migration from 8- to 16-bit parts. Hence they concluded that 16-bit architectures should be supersets of popular 8-bit architectures. Other vendors expected just the opposite—that increasing integration would cause a migration from 16-bit and 32-bit microprocessors into single-chippers. These vendors naturally favored chips that resembled 16-bit board-level computers.

Still other vendors attempted to derive an architecture from the design tools and concepts they expected customers to use. They produced designs that emphasized the needs of high-level languages. Each of the four approaches has produced a distinct class of parts, with distinct strengths and weaknesses in a particular application.

The point solutions
The first vendor to find a volume market for 16-bit microcontrollers was Intel (Chandler, AZ) with its 8096 MCU. In the joint development of the part, Intel established a pattern of architectural choices that would be followed, perhaps unknowingly, by several other vendors.
16-BIT MCUs

"The 8096 was designed along with the participation of an automotive industry customer," remembers Intel product manager Lee Davidson. "As in later 16-bit parts, the design emphasized the ability to capture an event, set up an event, perform data conversion and do fast arithmetic."

Intel, already dominant in 8-bit microcontrollers, had to face the fact that its 8-bit architectures simply couldn’t be stretched to achieve the performance needed by the application. So the company started with a clean sheet of paper. "We chose to go for performance rather than compatibility," says Davidson.

The result of Intel’s efforts was an architecture characterized by fast 16-bit arithmetic, a register-to-register instruction set with a large on-chip register file, and semiautonomous peripheral devices—such as analog-to-digital converters, capture registers and pulse-width modulators (PWMs)—to handle the most demanding types of I/O transactions without CPU intervention.

At the time, virtually all embedded-control tasks were programmed in assembler, and very few designs approached 64 kbytes in size. These assumptions found their way into the 8096 architecture as well. In sum, Intel produced a compact, inexpensive part—by 16-bit microprocessor standards—that could be hand-coded to produce very high calculating speed and could rely on new, complex I/O modules.

In contrast, the HPC emphasized tight, very fast assembly code in what was then a big 64-kbyte address space. Unlike the 8096, which addresses all of its on-chip RAM as registers, the HPC uses a more-conventional small register file.

After initial successes in the applications for which they were created, the Intel and National chips began to branch out. "The HPC is now used in engine control and printers," Ahrons says. The 8096 and its slightly expanded, considerably faster offspring, the 80C196, have spread from automotive to industrial and consumer applications. "Just about every 16-bit MCU has the same peripheral functions and speed," says Davidson. "The difference is how they’re optimized."

Moving up from 8-bit

As Intel and National were demonstrating the validity of the 16-bit MCU concept, other vendors were beginning to look at the market from a different point of view, and with the advantage of more recent CMOS processes. These companies saw the 16-bit opportunity not in isolation, but as an extension of the 8-bit applications they were already servicing. Not unreasonably, the chip designers concluded that the best 16-bit product would be a straightforward extension of successful 8-bit architectures.

The first of these companies to move was Mitsubishi (Sunnyvale, CA). By modeling its 7700-series MCUs on the existing 7400-series 8-bit parts, the vendor aimed at the needs of migrating customers. "We see two kinds of customers," says Ike Saeed, Mitsubishi marketing manager. "Some want to move from 8-bit parts just because they’ve run out of memory space. These people tend to want the same kinds of instructions and peripherals they..."
InterTools Products

Intermetrics' C cross development tools will help you clear the hurdles, so you can create a fully integrated environment that can deliver fast, efficient code for any host-target configuration you choose.

The Intermetrics state-of-the-art cross compilers, assemblers and utilities are built to work together as a team. Whether you're using a Sun, Apollo, DEC, HP or IBM system, targeted to run on a 680x0, 80x86, V Series, DSP96002, or Am29000 microprocessor, we are the single vendor that can help you get your development project across the finish line!

Our Source Level Debugger, XDB, works like a champion with our new low cost ROM Monitor, and with our new hardware simulation board, as well as with most in-circuit emulators.

Our technical support department will help you keep your development environment up and running by providing toll-free telephone assistance, free software updates and reduced rates for new releases.

Intermetrics' C cross development tools are the top tools in their class—call us to see how they run!

1-800-356-3594

in Massachusetts or Canada (617) 661-0072

Intermetrics

Intermetrics, Inc. • 733 Concord Avenue • Cambridge, Massachusetts 02138-1002

CIRCLE NO. 53
Philips, believing that users of 68000-based boards are looking for chip-level solutions, has been evolving the old CPU into a microcontroller for some time. The latest edition is the 93C110, a 68000 core with on-chip memory and peripherals.

have now. Others—in motor control and energy management, for example—have run out of time. They need more speed. These people want both more powerful instructions and more sophisticated peripherals to meet their timing requirements."

Mitsubishi took the logical steps to meet these needs. Starting from the 7400 family, the company decided to preserve the very low power dissipation that characterized the older products. Next they began to expand the part, enlarging the address space to 16 Mbytes, addressable in 64-kbyte pages. Then they began enriching the instruction set.

There were obvious changes necessary, like more addressing modes to deal with what would clearly be a memory-intensive machine. Mitsubishi created a total of 38. Additional new instructions were necessary for 16-bit arithmetic, helping out with floating-point, and so forth. But many of the new instructions were created for a specific issue that had come up since the design of the 8096: C. While it probably wouldn't be fair to say the 7700 series was designed to be a C machine, many of the 104 instructions (the 7400 series has 63) are there to support high-level language constructs.

The combination of low power, rich instruction set and large memory space has given the 7700 a unique spot in the 16-bit MCU business. Saeed believes the part will only expand its scope in the future. "We're moving in two directions—first, toward higher performance, with 25-MHz parts that carry general-purpose peripherals. Second, we're approaching some areas that require specific peripheral configurations—areas like motor control, printer control, hard disks and automotive. One new part, for instance, will have DSP hardware to accelerate servo loops. Another will carry an on-chip SCSI controller that will run as fast as 3 Mbytes/s asynchr

"Some customers move from 8-bit parts because they've run out of memory. Others have run out of time."

—ike Saeed, Mitsubishi

stance, will have DSP hardware to accelerate servo loops. Another will carry an on-chip SCSI controller that will run as fast as 3 Mbytes/s asynchronous."

An old friend resurfaces

Another powerful 8-bit player, NEC (Mountain View, CA), has taken a similar approach to the 16-bit arena, but with a more-familiar architecture: that of the Z80. The recently much-touted NEC K series contains the 8-bit K2, 8-bit-internal/16-bit-external K3 and the full 16-bit K6 MCUs with cores that are direct descendants of the venerable Z80 microprocessor.

NEC's belief seems to have been not so much that people wanted to migrate from the Z80 to a more powerful machine, but that the Z80 architecture gave them the tools they needed to address 16-bit issues. For instance, as NEC senior product marketing engineer Marc Birnkrant explains, "The architecture is optimized for multitasking—an important issue in big control systems. By taking the multiple register bank concept (from the Z80) and expanding it, we are able to do extremely fast context switches." The K6 takes the concept to something of an extreme, providing 16 register banks and some hardware task-management instructions as well.

Like Mitsubishi, NEC expanded its instruction set to support the greater needs of 16-bit applications. Full 16-bit math operations, more registers per bank, and elimination of some of the Z80's arcane addressing restrictions all helped. And the underlying hardware became more complex as well, with a prefetch queue and—in the K6—the ability to look ahead and prefetch the targets of branch instructions.

Along with this more powerful—and presumably busier—CPU comes a problem. How do you keep the wonderful CPU from being completely absorbed in servicing interrupts from the wonderful peripherals? The answer chosen by NEC, and later by Intel for a recent 80C196 model, is a hardware datamoving engine that operates autonomously from the CPU.

In NEC's case, the device is virtually a processor itself. In the more-advanced family members, the Peripheral Management Unit can not only perform DMA-like data transfers, but can also filter the data on the way through, performing comparisons and Boolean operations. Vahid Ordoubadian, an NEC senior field applications engineer, points out that these capabilities can be used for tasks that would otherwise have to get high-priority CPU time, like searching for immediate commands in a stream of incoming data.

Shrinking the old standard

While Mitsubishi and NEC have looked to 8-bit architectures for a core to expand, Philips Components (Sunnyvale, CA) has been looking in just the opposite direction. "We saw that 16-bit MCUs were trying to solve problems that had formerly been handled by 16-bit microproces-
Choosing the right MCU—a real-time O/S vendor’s view

A unique viewpoint for comparing 16-bit is MCUs that of Nicholas Andrews, president of real-time kernel vendor ByteBOS (San Francisco, CA). In porting his C-based multitasking operating system, Andrews is asking microcontrollers to do things everybody knows the little chips can’t do: support an on-chip kernel with formal task management, run compiled code, and execute portable applications software.

Consequently, Andrews has had to produce small, efficient versions of his BOS kernel for a variety of 8-and 16-bit controllers. This process has given him a good look at the hardware decisions, instruction-set choices and design toolsets that characterize major 16-bit families.

One important issue for Andrews is memory space. The first question here is whether the operating system and the application tasks can fit in the part’s internal memory. A few years ago, the answer would have been an obvious “no,” but this is changing. “Some of the latest versions of the Mitsubishi 7700 have 32 kbytes of EPROM and lots of RAM space,” says Andrews. “At that level, you can fit the operating system and a big application into the on-chip memory, and have a single-chip system.”

Beyond the physical memory on the chip, Andrews is concerned about the total address space of the device, and how it is organized. As an example he points out, “The Intel 80196 family has excellent peripherals and a fine instruction set, but it’s limited to 64 kbytes each for code and data. This almost makes the chip a niche product for people whose code will fit into 64 kbytes.” Address spaces of other microcontrollers range from 1 Mbyte for the Hitachi H8 and H16 architectures up to 16 Mbytes for the 7700.

Organization of the address space can also be an issue. Most single-chippers use a segmented address space, presumably to keep the instructions compact. But segmentation imposes its own problems. “If you compare two CPUs of similar performance, maybe the 16-MHz Intel 80C186 and the Motorola 68332 would be head-to-head,” he says. “But there’s about 30 percent more work involved to support the segmented address space model of the 186.”

Peripheral matters matter
It’s obvious that memory is a critical resource for an operating system. But at first glance one would think on-chip peripherals—things like timers and analog-to-digital converters—would be purely an applications issue. Not so, in at least one case, according to Andrews.

“One of the things you need to implement a multitasking operating system is a heartbeat timer: a piece of hardware to mark off the basic time interval for task control. Almost all controllers have at least one timer available that I can use for that, but the implementation varies from chip to chip.

“On the 68332,” Andrews adds, “you have these very sophisticated timers in the timer processing unit, but you also have a separate programmable interrupt timer that’s just right for the heartbeat timer job. The Motorola people seem to have anticipated the problem and solved it. The 7700 may be more typical—it has eight general-purpose timers, and I use one of them, meaning it’s not available to the application.”

The most difficult situation, according to Andrews, comes up on the 80C196 family. Here, there are only two timers, and if the application requires both of them—which frequently happens—the heartbeat timer ends up being tied to a multiple of some clock frequency used by the application. In addition, the timers lack an auto-reload register, so the operating system must calculate a correction to load into the timer in compensation for the time lost in recognizing the timer interrupt and reloading the device.

Instruction issues
The instruction-set architecture of the microcontroller can also be an important issue for the operating system vendor, for two different reasons. First, a good port depends on a good compiler, which in turn depends on the quality of the chip’s instruction set. Second, critical parts of BOS are written in assembly code for performance reasons. This forces Andrews to deal with the ease-of-coding issue for a chip as well.

Andrews cites the 80196 in particular for the quality of its instructions. “Finally, a good, orthogonal instruction set on an Intel machine,” he comments wryly. “Not surprisingly, architectures borrowed from the microprocessor world also rate well for Andrews’ needs. “I just can’t say enough about the 68332 architecture. There are a lot of tools, and you get really tight C code—and about the best context switch of any microcontroller. The 68332 took the fewest instructions of any chip to implement the BOS kernel—sometimes you can do in one instruction what it would take other machines eight instructions to do.”

At the opposite end of his list is the 7700. “The instruction set is very rich, but it’s weak in bit-manipulation instructions and not entirely orthogonal,” he complains. “That makes the chip very difficult to program in assembler.

Fortunately, Mitsubishi’s C compiler does a good job of making up for the instruction set,” he continues. “For instance, you have to set a control bit in the CPU to determine whether the next instruction operates on a byte or a word. The compiler manages to look through the code and minimize the amount of thrashing it has to do on this control bit. So you end up with reasonably efficient code.”

The issue of compiler quality raises the more general question of tool availability. Since the 16-bit parts aren’t yet widely used, they can lack the range of third-party development tools that an 8051 or 68HC11 user might expect.

“One of the drawbacks of the 7700 right now it that Mitsubishi is the only source of tools,” Andrews says. “But so far, the company’s support has been great, and I understand there are more tools on the way for the chip.”

There seems to be a good correlation between the age of an architecture and the volume of tool support. The 8096 family, for example, has the oldest mainline 16-bit controller architecture. It also boasts excellent tool support from both Intel and third parties.

Yet Andrews sees one trend that could break up this state of affairs. “Motorola sells a $700 development system for the 68332 that gives you an execution target plus emulation capability. The tools are really inexpensive and very good. There is virtually no cost to get into this chip. As the chips get more powerful, this sort of development tool, using the controller itself, could become a trend.” For the software developer on a limited capital budget, that could be as big a consideration as any of the others.
You might not be able to tell from the feature list, but NEC's new entry into the 16-bit fray—the µPD78312—is based on the Z80 architecture. A vastly improved instruction set, legions of registers and a powerful DMA engine put the chip in a different class from its ancestor.

---

From a clean sheet

Despite the appeal of arguments that customers of 16-bit MCUs want to work with a familiar architecture, some vendors think that the needs of this market are so unique that they must be met with a fresh start. Among these is Siemens (Santa Clara, CA), whose 80C166 MCU has the distinctions of being the first European 16-bit MCU architecture and the first CMOS MCU to be second-sourced—by SGS-Thomson (Phoenix, AZ).

"The chip was designed with two goals: short interrupt latency and high instruction throughput," says Ash Ahluwalia, senior product specialist at Siemens. The creators of the part achieved these goals by applying some of the latest RISC-ish thinking from the microprocessor world to the design of their MCU core.

The resulting architecture takes ideas from many sources. For instance, the chip uses a branch cache. Like Sparc—and the 8096—the device treats on-chip RAM as banks of registers. It can switch between any of the sixty-four 16-register banks in a single 100-ns machine cycle and do a multiply in less than 1 µs. Also like many RISC machines, most instructions are executed in a single cycle, via a four-stage pipelined execution unit. "But unlike many 32-bit machines, the pipeline has been designed so that it can be flushed elegantly," says product marketing manager Mike Rampelberg.

An important point about the 80C166 is that throughout the design, the architects knew that the chip would be programmed primarily in high-level languages. In fact a compiler team developed the MCU's C compiler while the silicon folk worked on the chip. This close coupling led to such hardware features as a 16-Mbyte address space and the ability to pass parameters through overlapping register windows. On the software side, the team worked made possible inclusion in the C compiler of commands that exploit...
The Microtec Research XRAY Debugger opens a new window to the world of debugging. With XRAY's state-of-the-art technology, you can debug fully optimized C programs.

No longer will you debug non-optimized programs only to find that the optimized version does not work. The Microtec Research XRAY Debugger is designed specifically to support non-intrusive debugging of optimized code. And XRAY doesn't add a single byte to your executable program.

The XRAY Debugger offers a complete set of features for today's demanding software professional:

- Multiple windows for convenient display of source code, program variables, breakpoints, execution state, and commands
- Complete set of breakpoint commands for simple and complex breakpoints
- Full display of user variables in their declared type
- Powerful macro language for use in user-defined commands, custom windows, and automatic testing scripts
- Comprehensive set of execution environments including software simulation, hardware emulation, real-time operating systems, and in-circuit monitors
- On-line help

XRAY: The standard by which other debuggers are measured.

The Microtec Research XRAY Debugger and compiler family create a complete software development package. Learn more about the XRAY Debugger.

Call now. 800-950-5554.

Don't delay. We'll rush you the latest technical information about our feature-packed window-oriented debugger.

<table>
<thead>
<tr>
<th>XRAY COMPATIBILITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOSTS</td>
</tr>
<tr>
<td>IBM PC</td>
</tr>
<tr>
<td>Sun</td>
</tr>
<tr>
<td>HP</td>
</tr>
<tr>
<td>Apollo</td>
</tr>
<tr>
<td>DEC</td>
</tr>
</tbody>
</table>

Creators of the XRAY development environment.
2350 Mission College Blvd. Santa Clara, CA 95054 408-980-1300
London 0256-57-55-1 Munich 089-609-6020 Tokyo 03-597-9000 New England 603-880-4484

CIRCLE NO. 54
the chip's fast context switching, and C support for an on-chip cycle-stealing data moving engine called the Peripheral Event Controller.

With its fast computation and context switching and excellent linkage to C, the 80C166 should do a fine job of delivering its latent performance to C-language programmers. But perhaps the ultimate effort in this regard has been made by another vendor, Harris (Melbourne, FL), whose RTX MCU

pointed Harris. The part, which can use its four buses to simultaneously perform stack, computational and I/O operations, has become an important ingredient in Harris's embedded computing box, both as an ASIC cell and as several flavors of standard products.

### Covering all the bases

The 16-bit world, then, covers a wide range of architectural ideas. Some architectures have grown out of the family was originally designed specifically to execute Forth.

"Originally the RTX architecture was one of the few ever intended for direct execution of a high-level language," says David Williams, RTX market development manager. "But when Harris looked at acquiring the technology, we saw not just a Forth machine, but a very fast general-purpose stack architecture, implemented in a very small—about 4,000-gate—core.

"We knew that stack architectures were well suited to executing code from many different language sources. And because stack machines inherently have very little context—no pipelines, no caches and no queues—they are very easy to use in demanding event-driven environments. Also, we knew that a core this size could be just what we needed—a powerful 16-bit MCU that could be an element in our ASIC cell library."

The RTX apparently hasn't disap-

The Motorola 68331, a stripped-down version of the vendor's 68332, offers the basic concept—a 32-bit CPU core in a microcontroller format—without the 332's frills. Reduced peripheral complement and aggressive pricing could put the 331 in direct competition with conventional 16-bit MCUs.

concept of hand-crafted code and application-specific peripherals in an anything-for-speed design. Other parts have been blended from a combination of older architectures and newer ideas. Still other designs have come out of entirely fresh thinking about fast execution of high-level-language code in a multitasking environment.

The one major 8-bit player that has remained on the sidelines of this entire debate has been Motorola (Austin, TX). With its externally 8-bit 68HC11 family and its full 32-bit 68332 family, the company had bracketed the cost/performance range of 16-bit MCUs without ever actually entering the 16-bit waters. Now that is changing as well. In a series of steps begun last month, Motorola will unveil its midrange series of steps begun last month, Motorola will unveil its midrange.

Initially, Motorola has shown an upgraded 68HC11, sporting improved speed and memory size, and an on-chip memory manager for greater-than-64-byte address range. "This part will compete head-on against 80C96-class 16-bit MCUs," boasts Motorola director of marketing Steve Marsh.

This month, the company will boost its efforts to promote the 68000 architecture for MCUs by introducing price cuts for the existing 68332 and rolling out an ever lower-cost subset of the big part: the 68331. The new device is intended to offer the 68000 architecture and the sophisticated peripheral environment of the 332 at a price competitive with high-end 16-bit parts.

The end of the unveiling will happen next month, with the announcement of Motorola's long-awaited true 16-bit MCU. The company won't release architectural details yet, but Marsh is clear about the philosophy behind the chip. "It's our perception that in the migration to more powerful MCUs, 32 bits is the right place to change instruction-set architectures. And 16 bits isn't the right place to make people change."

This sequence of announcements seems to put Motorola firmly in almost everyone's camp. The vendor is supporting the notion of evolution from 8-bit architectures. And it's offering a complex 32-bit architecture originally intended for use with high-level languages and operating systems. Motorola's message—and perhaps the best overall conclusion about the 16-bit parts—is that each approach has its own validity for a particular set of application needs. None is all-powerful, and none is obsolete.

---

**MOTOROLA's NO-FRILLS 68331**

- CPU32
- General Purpose Timer
- Queued Serial Module
- Chip Selects
- System Integration Module
- External Bus

---

**For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.**

<table>
<thead>
<tr>
<th>Company</th>
<th>Phone Number</th>
<th>Circle Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte-BOS Integrated Systems</td>
<td>(415) 543-3626</td>
<td>209</td>
</tr>
<tr>
<td>Harris Semiconductor</td>
<td>(407) 724-7000</td>
<td>210</td>
</tr>
<tr>
<td>Intel</td>
<td>(602) 554-8080</td>
<td>211</td>
</tr>
<tr>
<td>Motorola</td>
<td>(512) 851-2000</td>
<td>212</td>
</tr>
<tr>
<td>Mitsubishi</td>
<td>(408) 730-5900</td>
<td>213</td>
</tr>
<tr>
<td>NEC</td>
<td>(415) 965-6000</td>
<td>214</td>
</tr>
<tr>
<td>National Semiconductor</td>
<td>(408) 721-5000</td>
<td>215</td>
</tr>
<tr>
<td>SGS-Thomson</td>
<td>(602) 861-6100</td>
<td>216</td>
</tr>
<tr>
<td>Siemens</td>
<td>(408) 980-4518</td>
<td>217</td>
</tr>
<tr>
<td>Signetics</td>
<td>(408) 951-2000</td>
<td>218</td>
</tr>
</tbody>
</table>

---

**90 SEPTEMBER 1, 1990 COMPUTER DESIGN**
The Motorola Computer Group invites you to become their newest boardmember.
Take Advantage Of Board-Level Partner
Once you've seen what Motorola brings to the table, we think you'll agree it's everything you need. Like the most complete line of VME products, services and engineering support available anywhere. Award-winning quality. Competitive pricing. All from the company that pioneered VME technology, and whose product line ranges from ICs to boards to full systems. And includes everything in between.

You decide exactly what you need from our more than 100 VME products at every level of price and performance. From CPU boards, like our new '040-based MVME165, to memory boards, to communications boards. And the industry's widest assortment of development tools, software resources, and technical support.

A partnership with Motorola not only helps you control costs, but even more importantly, speeds your time to market. Our products include more functionality with a higher level of integration to accelerate your development efforts. And because of Six Sigma quality control you can be assured that our products will work right out of the box. It all adds up to the fact that getting you to market sooner is a promise only a company with the resources of Motorola can make good on.

Every Motorola product includes a built-in migration path, so your future product cycles are assured. Such as providing a way to upgrade from the 68020 to the 68030 to the 68040, or from a 68000 CISC board to an 88000 RISC board with a simple re-compile. Wherever you're headed, Motorola is going to be there.

And we'll support you during the entire development process. Every board in our product line includes a full suite of board diagnostics available in both a run-time and a source package. This degree of flexibility also extends to our nationwide customer service programs, which run the gamut from total on-site maintenance to self-maintenance support packages.

For more information, call us today at 1-800-624-8999, ext. 230. Once you discover the advantages of a partnership with Motorola, you'll see that it's no ordinary board-level decision. It could ensure the future of your company.

At Motorola, Openness Is Standard Procedure

These days, openness has become something of a buzz word, and everybody seems to have a different idea on what is and isn't "open." To us, it's no big mystery. Openness means open architectures, open software, open networking. And open standards like UNIX, as indicated by our role in founding open. It means we're open to helping solve problems with your point of view in mind, not just ours. And it's been that way ever since we helped introduce VME back in 1982.

That's why Motorola is committed to supporting official and de facto industry standards, interoperable computing between multiple vendors, and non-proprietary open system architectures. It's why we created VMEexec to facilitate the interoperability of different real-time software modules within a common UNIX environment. And it's why we support virtually every networking protocol, including XNS, TCP/IP, DECnet, MAP/TOP/OSI, SNA, BSC, X.400, and X.25.

This philosophy of openness is the same reason we offer as many VME boards, products and services as we do. It's to our mutual benefit, and after all, isn't that what partnerships are for?
How much can Design-for-Test reduce the need for testing?

Jon Gabay
Contributing Editor

Making a design functional and making it producible have been two different tasks. Now, test standards, tools and embedded circuitry move them closer together—and into designers' hands.

The test issue has plagued engineering ever since the cave man who invented the club accidentally knocked himself out to prove to the tribe that it worked. Many engineering firms are still knocking themselves out to tackle the tough testability problems of today's more advanced and sophisticated designs.

Unfortunately, when a design task is given to an engineer or an engineering team, the foremost concern on their minds is to get a functional implementation of the specific tasks implemented. Testability of functional verification and system-level verification is often not even considered when an engineer sits down to design a circuit, subassembly, assembly or system.

What complicates matters even more is that on large designs, many engineers may be simultaneously working on different sections. In this case, even if each individual engineer has a test philosophy in mind, merging them together later to obtain a system-level test strategy (either for functional verification or fault analysis during debug or production repair) can be a formidable task.

Engineers typically design, debug and implement first, then work on a test strategy. When test philosophy is imposed, it will usually involve another iteration through the design loop. Later, a system-level test philosophy may cause each engineer to iterate yet once again. This is time-consuming, redundant and an ineffective solution to satisfy today's time-to-market demands.

The overburdened engineer

The double-edged sword caused by design automation has left the engineer responsible for yet even more. Since schematics can be captured and edited rather quickly, schematic capture is part of his or her dance card. Likewise, since simulation technology is advanced to a usable point, these tasks are added. Although simulation has taken a bite out of breadboarding, a prototype isn't uncommon—again, something the engineer oversees.

What's more, today's designs are often pushing the limitations of blind printed circuit board designs. The higher clock rates, more functionally dense systems, and mixed analog and digital designs require the engineer to take an active part in the layout of the printed circuit board, instead of merely handing off a schematic to a department or service. On top of all that, the engineer must be responsible for some form of documentation.

The engineer is tied up even longer when test constraints are imposed after board layout. At larger companies, which often have dedicated test engineers on staff, the test engineer is usually given a black-box approach to work with, meaning that his or her expertise is injected after the functional portion of the design is in place.

What complicates matters even more is that with many of today's designs, including embedded microprocessors and microcontrollers, software testing for effectiveness, performance and bullet proofing adds even more stress.

The ideal approach

Ideally, test strategy should be mapped out at the time of product conception and definition. This test strategy will vary greatly from company to company, depending on what test and testability tools they have in place. Further, this test strategy will vary within the same company for each project.

Also in this ideal environment, test engineers work side by side with design engineers, software pro-
grammers and printed circuit board designers. This permits test features to be incorporated at the time of implementation rather than later adding components that may affect critical delay paths or already tight printed circuit boards. A software guru working with the group can also make recommendations as to how to make the hardware implementation more efficient for operation and test.

A design engineer may, for example, have to write to a latch a series of bytes that control the gating and transfers of register-level data. While from the hardware engineer's point of view, any bits of the latch can be assigned as any of the control signals, the programmer may require bit placement in a non-random sequence to make masking, state checking and I/O easier from the software point of view. This same philosophy applies when the test engineer and the software engineer work together, since often the most efficient approach is to combine built-in self-test coding with external testing.

While many people may be involved in the loop, it's still the hardware engineer who is ultimately
Engineers typically design, debug and implement first, then work on a test strategy, causing many design iterations. Unnecessary design iterations could be eliminated by mapping out a test strategy during product conception and definition. In that approach, test engineers would work side by side with design engineers, software programmers and printed circuit board designers, incorporating test features at the time of implementation rather than adding components later on that may affect critical delay paths or already tight printed circuit boards.

… responsible for a design that can be tested. As a result, the designer's choice of parts greatly affects the outcome. Unfortunately, a global test standard isn't yet in place, and each different chip may have its own proprietary test interface, or none at all. What's more, every different kind of device carries its own set of problems associated with testing and design-for-testability within a system-level environment. The simplest is glue logic.

Discrete-function TTL, SSI- and MSI-level functions have no built-in test incorporated on-chip. This means an engineer must physically connect key signals to some form of decoder or multiplexer to observe critical signals within the system. For the most part, glue logic chips are pretty reliable, but a failed NAND gate in a 300-IC board can still be a bear to troubleshoot.

One solution is to take advantage of specialized discrete-function chips that incorporate a test standard. Texas Instruments (Dallas, TX) offers the Scope family of cells as part of its standard-cell library. For discrete implementation, and for designs that need to adapt for scan-path technology, TI also offers octal I/O devices that are compatible with the JTAG (Joint Test Action Group) standard. These devices can be added into scan chains to cover signals and devices not implementing a scan-type test capability. To round off its offering, TI also provides a PC-based development tool called Asset, which helps familiarize, implement and test circuits using the JTAG devices.

Programmable logic devices have gained much popularity and widespread use. But PLDs pose greater quality-control problems than do standard parts, and therefore require a more involved test strategy. With PLDs, more faults are likely to occur and more defects are possible. Testing for only stuck-at-0 and stuck-at-1 faults and intact fuse faults will uncover some faults, but won't uncover many sources of PLD-related board and system failures.

Fault coverage depends on defining all possible defects for a device and then determining what portion of those faults are detectable through testing. Because PLDs can have so many different types of faults, engineers pick a sample of
No Limits.

No Compromises.

No Substitutes.

When you want your FPGA and PLD designs to be smaller, faster and more testable, Data I/O®’s software and hardware development tools never say no.

No Limits. Only Data I/O gives you unlimited device choices. We support every device manufacturer, technology, and architecture. And we’re always first with support for the latest devices. Our close relationships with the semiconductor manufacturers help us anticipate technology trends, ensuring that support is ready when you are.

No Compromises. You’ll never have to compromise your FPGA and PLD designs because of tool limitations. Our software and hardware products take advantage of the latest technologies, giving you the most powerful design, verification, test, and programming capabilities available.

No Substitutes. Only Data I/O offers a full range of development tools for advanced devices. Whether you’re designing an FPGA or PLD, designing for PLD testability or programming the latest device, Data I/O gives you the best support. Make us prove it.

Call now and qualify for your FREE Evaluation Package. 1-800-247-5700

The Personal Silicon Experts

© 1990 Data I/O Corporation
defects and measure the detection rates on those sample faults.

In reality, though, what matters is how the measured coverage corresponds to the yield at the next test stage. If, for example, the measured fault coverage at the component test stage is very high, then any defects found at the board- or system-level test stages should be traceable to steps occurring after component programming and testing.

Another concern about PLDs that's not a factor with other logic parts is that programmed functionality may be living in a one-time-programmable part or an erasable/reprogrammable part. One-time-programmable parts can't be tested in any incoming inspectional test barrage. Even EPROM-based parts take too much time to program, test and erase enough times to thoroughly verify that part. So only EEPROM- and RAM-based parts can provide some level of incoming assurance before production.

Because PLDs have limited incoming inspection testability, fault grading—the process of evaluating and selecting test vectors for the testing process—is important. When fault-grading tests for PLDs, test designers should include fuse-related faults, particularly faults on blown fuses. Fuse faults are critical because fuses make up most of the physical area on the chip itself. Therefore, most defects appear on fuses.

If a fuse that should be blown is intact, the resulting device behavior can act in a nondeterministic way and can cause symptoms that don't necessarily point to the PLD itself. Consider, for example, a combinatorial circuit that factors in an unused pin as a result of a partially blown fuse, or a fuse that is intact that shouldn't be. If that unused pin is floating, the resulting failure can be intermittent, the worst type of problem to find.

This effect is especially important with the newer architectured PLDs and FPGAs. With so many fuses (or antifuses or EPROM or EEPROM cells), programmable clocks can change polarity, glitch, or acquire enables; macrocells can change types, polarities and functions; product-term sharing can be combined or increase; state machines can lock up, insert new states or skip vital stages; and combinatorial elements can become memory elements.

Generally speaking, the more sophisticated the PLD architecture, the more baffling the blown fuse fault can be.

Tools to the rescue

Tools from companies like Data I/O (Redmond, WA) and Anvil Software (Nashua, NH) help detect fuse faults early in the process. "It's important for an engineer doing the design to take time to account for proper and full test-vector coverage, or nightmares and headaches can follow long after the engineer thinks the design is completed," says Stephen King, product marketing manager from Data I/O. "In addition to proper test coverage, it's important to understand how the test coverage is determined, as well as how the programmer will apply these test vectors."

The following fuse faults can be detected.

"It's important for an engineer doing the design to take time to account for proper and full test-vector coverage."

—Stephen King, Data I/O

1) Pin-level faults, including stuck-at faults on all input and output pins of the chip. In-circuit-board testers for standard parts can test for pin faults. Also, properly developed test vectors after programming can detect this.

2) Logic faults, including stuck-at faults on all internal gates, input pins, output pins, column drivers into the fuse array, product term AND gates, OR gates, master and slave latches in flip-flops, three-state enables, set and reset lines, clock lines, and gates inside macrocells. Gates inside macrocells include feedback and output multiplexers, which are faulted at the gate level.

3) Junction faults, including stuck-at faults on each input to each gate. Junction faults differ from logic faults whenever a gate has more than one fanout. That's because a junction fault affects just one or more fanouts, whereas a logic fault affects all its fanouts. The MIL-454 standard primarily addresses junction faults in component fault grading, including PLDs.

4) Intact fuses that are faulted as blown. Each fuse in the fuse array that is supposed to be intact is faulted as though it were blown. This is the same as sticking the fuse junction to a 1 in programmable AND array devices or faulting the input junctions to the product-term AND gates high.

5) Blown fuses that are faulted as intact. Each fuse in the fuse array that is supposed to be blown is faulted as though it were intact. This is the same as causing a short between a column in the fuse array and a product-term line.

Testing semicustom

More than any other form of technology, semicustom silicon in the form of gate arrays, standard cells and silicon compilers has been responsible for pushing testability as a philosophy. If these risky and expensive designs don't work to specification, the engineers have some explaining to do.

In the early days of gate array and standard-cell designs, functionality was fully the driving force. Test vectors verified functionality and didn't trace faulty symptoms back to specific problem areas. Tools and architectural strategies weren't automatically built into the process. As a result, larger companies, and even astute smaller companies, solved the device-testability problem in various and clever ways.

If I/O wasn't the problem, and if test speeds became an issue, parallel dedicated test lines were implemented. In that approach, a proprietary parallel port gave access to whatever internal nodes needed stimulating or observing. In a fashion similar to a microprocessor peripheral chip, each device was addressed, tested and evaluated. But this was inefficient for several reasons.

First, this adds another parallel bus to the circuit board, which may already be tight for space. Also, a proprietary protocol and hardware structure must be implemented in each device. This adds a lot of development time and cost and requires specialized test equipment.

Scan technology is an umbrella term for all the serial protocols and architectures used within a device (or family of devices) to implement
Marketing
OEM Peripherals?

AMONG ICC ATTENDEES,
COMPUTER DESIGN IS #1

During 1989, Dataquest/ICC asked attendees at each OEM Peripherals Invitational Computer Conference to name the publications they read.

THE #1 CHOICE IS
COMPUTER DESIGN.

But that shouldn't be a surprise. After all, COMPUTER DESIGN is 100% design & development qualified, 70% engineering management and has more than 70,000 specifiers of memory/storage equipment & systems, and 82,000 specifiers of terminals and other output/input equipment.

If you're marketing peripherals to important OEM specifiers, we should be your #1 advertising buy. Call any of us for more information.

Thanks and good selling.
some form of stimulus and response pertinent to the inner workings of that device (or system). Scan technology is desirable because it provides a window into each device, but requires only a few signals (usually four) to route between devices. Outgrowths of scan technology have diverged into many approaches, the simplest being boundary scan and the most complex being full scan.

Boundary scan is the cheapest and simplest scan approach and introduces the smallest penalties for device performance. Boundary scan involves taking control of all I/O pins, applying test vectors and observing results. Conceptually, a large shift register encompasses the periphery of the ASIC and, when put in test mode, engineers shift in the applied levels for test, and shift out the results via a test access port, which usually consists of four wires (data in, data out, clock and mode). In this way, each ASIC (or device incorporating this test structure) can be effectively isolated and verified.

Boundary scan is increasingly becoming standard practice. The JTAG approach has been gaining interest among the IEEE-P1149 Test Standards Committee, Department of Defense and industry as a workable test solution for device and system-level testing. (See “JTAG testability takes on today’s system-test demands,” p 101.) As a result, many semiconductor houses are adopting JTAG support for ASIC customers and providing JTAG-compatible cells or macros.

The problem with this approach, however, is that since only I/O signals are sent and received to and from the devices, test times can be too slow. Consider, for example, a standard ASIC that may implement some type of RAM or FIFO, as well as some other multiregistered and/or pipelined function. Testing memory will require vectors for each location (or each row, if the memory is laid out cleverly), each register, each level in the pipeline and so on. It may take between several hundred and several thousand cycles to see the results of the applied vectors—not an efficient production-line solution.

On the other end of the spectrum is full-scan test, which involves placing a stimulus tap (usually a multiplexer) on every internal driving signal, and a response tap is placed on every internally driven signal. This approach is faster and more efficient than boundary scan and permits 100 percent controllability and observability.
JTAG testability takes on today’s system-test demands

Advanced technologies are playing havoc with efficient testing of today’s more-powerful system designs. Such developments as submicron processes, tighter package pin pitches, and advanced surface-mount technology stymie the accuracy of traditional test and measurement tools.

But help is at hand. Systems houses can look to JTAG testability for an efficient, up-front test methodology. Test circuitry that conforms to the JTAG IEEE-1149.1 standard test interface and boundary-scan architecture is being implemented in ASICs and other chips to ease board testing.

The key features of the JTAG IEEE-1149.1 standard are a four-wire test bus and boundary scan. Each JTAG-compatible IC has four added pins: two for control (test mode select and test clock) and two for moving serial data in and out of the chip (test data in and test data out). The JTAG architecture includes a test access port for controlling the instruction and data registers. The boundary-scan data register includes a boundary-scan cell at each pin except for the power and ground pins.

During normal operation, the boundary-scan cells are transparent. But in test mode, the cells are linked together to form a serial shift register, thus allowing systems designers to control and observe data at the test data pins.

Hierarchical testability

Systems houses are finding that by taking the JTAG route, they can leverage hierarchical testability for higher-quality systems at a reduced cost. This is accomplished because a consistent, structured test approach is used throughout the product life cycle. Test vectors, for example, can be reused throughout the process, from design to manufacturing to field repair and maintenance.

Texas Instruments (Dallas, TX) is the first chip maker to play its JTAG hand, and is promoting the concept of hierarchical testability. Included are special test ICs, ASIC test cells, test controllers, IEEE-1149.1-compatible standard parts, and a computer-aided test-scan-based diagnostic tool. To TI, hierarchical testability means placing control and observation structures into devices for all test and integration levels from ICs to systems. And the heart of TI’s hierarchical testability strategy is the JTAG four-wire test bus.

TI pioneered three types of JTAG controllable devices, and they are members of the company’s product family named Scope (System Controllability and Observability Partitioning Environment). Scope octals, the first type, are standard bus-oriented devices with a JTAG interface that serve to create board partitions and add in-circuit testing around VLSI chips, like microprocessors. Scope ASIC cells, the second type, are used in customer-designed ASICs for 1149.1 compatibility plus access to built-in self-test (BIST). Third, new TI application processors such as the TMS320C50 are 1149.1-compatible.

The scan-test octals (the devices with the BCT prefix) in the application illustrated below execute such BIST operations as pseudorandom pattern generation and parallel signature analysis. These devices give designers a free hand at isolating specific circuitry within an assembled module, board or system. Through this isolation, engineers can debug circuits, components and connectors without manually probing them. The octals’ test capabilities can also be used to test adjacent devices lacking test structures.

As part of its JTAG commitment, TI recently introduced Asset (Advanced Support System for Emulation and Test). A member of the Scope product line, Asset is a scan-based diagnostic tool for design debugging and hardware testing. IEEE-1149.1 products should continue to gain acceptance. Such products make sense in light of the poor efficiency that’s associated with conventional test methods.

Glenn Woppman, BSIE, product marketing manager, Design Automation Div, Texas Instruments
The newest system through space-time.

The AMP Z-Pack Interconnection System is a scalable, high-density board-to-board/cable-to-board system for nanosecond and subnanosecond applications, in 2 mm and .100" grid sizes to accommodate global packaging requirements.

The fastest members use stripline technology, introducing reference planes between pin columns to retain maximum pin counts in a controlled impedance interface.

The design advantages are immediate: Z-Pack .100" stripline connectors accommodate 250 ps edge rates with no sacrifice in signal density: four rows = 40 lines per inch.

High-temp materials for SMT compatibility.
Twin-beam receptacles, 2 mm wipe.
Sequenced mating up to four levels.
2 mm versions accommodate two traces between lands.
Stripline versions isolate pin columns for 50 ohm interface.
Reliable compliant-pin versions available.
Space: 40 lines/inch.
Time: 250 ps.

2 mm stripline versions (500 ps) require just one pin row for reference, and open pin field versions in both centerlines handle 1.8 ns rise-times with a 3:1 signal/ground ratio. Standard spacing minimizes board redesign, and system modules stack end-to-end with no loss of signal positions, offering true form/performance scalability in Futurebus-like applications.

For more information on the Z-Pack Interconnection System, call our Product Information Center at 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

For advanced design and manufacturing of complete characterized multilayer backplane systems, contact AMP Packaging Systems, Inc., P.O. Box 9044, Austin, Texas 78766, (512) 244-5100.

CIRCLE NO. 58
structure, which is almost always proprietary for each company. Most important, though, is the performance penalty. Every signal is delayed either because it’s driving through an extra level of logic, or because it’s being driven by a signal, which has to drive an extra load.

A middle-of-the-road partial-scan approach seems to be the most beneficial in terms of device performance, silicon overhead and test effectiveness. With partial scan, a boundary scan can still apply test vectors and monitor responses. In addition, other scan paths can test generators (ATPGs), which produce test vectors that strive to provide total coverage of a design. Test vectors from ATPGs and from other sources are then fault-graded to determine the efficiency of the test vectors regarding how many nodes are accessible and observable.

Fault grading, the process of determining the test coverage, is expressed as a rough percentage of how much of the circuit is stimulatable and observable with a set of test vectors. There are two types of fault graders: probabilistic and deterministic. Oki Semiconductor has implemented a built-in test structure that permits control and observability independent of functional logic and causes no performance penalty. The company’s scan-test flip-flops differ from standard flip-flops in that they have two additional pins—scan data and scan clock—to control the scan-test logic. Oki claims that implementing the same amount of logic discretely would add 77 percent overhead to the size of the chip. The truth table is for a scan-test D flip-flop with SET and RESET.

\[ \begin{array}{cccccccc}
  D & C & SD & SC & RN & SN & QA & QN \\
  H & L & X & H & H & H & H & L \\
  L & L & X & H & H & H & H & L \\
  X & L & X & H & H & QA(1-1) & QN(1-1) & \\
  H & X & H & L & H & H & H & L \\
  X & H & L & L & L & H & H & H \\
  X & H & X & L & L & H & L & H \\
  X & L & X & L & L & L & L & L \\
  X & L & X & X & X & X & # & # \\
\end{array} \]

NOTES: **"** TRANSITION FROM *TO *" PROHIBITED
# PROHIBITED

those problem areas that test vectors either can’t, or take too long to, reach. This can provide fast production test with reasonable observability and controllability. More important, it allows engineers to take advantage of the many test-pattern generator and fault-grading tools already available.

**Tools meet the challenges**

Many advances in tools have helped ease the burden of analyzing a device’s testability. Now commonplace are automated test vector probabilistic fault grading is a fast but inexact method that involves statistically extracted results obtained from applying a limited set of vectors. It’s useful for getting a quick feel for how good a set of test vectors are at exercising and testing the entire device.

Deterministic fault grading is the exhaustive search for coverage of each node as a result of the test vectors. This approach provides an exact number of testable and non-testable circuit elements but takes a lot of computer time.

Fault simulation is the umbrella term for applying an exhaustive barrage of test patterns to a device to characterize its failure behaviors. Although limited to the assumption that only one failure will occur at any one time, fault simulation lets engineers work backward from a faulty part to determine the cause.

The problem with fault simulation is that it, too, is very compute-intensive. An entire simulation run must be performed for every combination of stuck-at-0 and stuck-at-1 logic states at every node. Concurrent fault simulators speed things up by permitting more than one stuck-at fault to be analyzed in one simulation pass, providing that the stuck-at signals don’t interfere with the observable output from each fault. Even so, fault simulation will take time—more time than most are willing to spend.

**Improving the design**

Design tools such as the Design Advisor from NCR (Fort Collins, CO) and the Design Consultant from Triimeter (Pittsburg, PA) are striving to make the source of the problem better for the process. By improving the design, everything else should improve. These tools, based on expert-system technology, analyze a design and make recommendations on how to increase testability by improving the design structurally without altering it functionally. In addition, these tools can make recommendations on how to increase performance without sacrificing functionality.

Another solution comes from Integrated CMOS Systems (Sunnyvale, CA), which provides a standard-cell library with a twist. In ICS’s library, every cell implements a proprietary architecture through which it provides and builds a testable scan path automatically and transparently to the designer, without introducing delay penalties. “A proprietary architecture automatically implements scan-test paths with no delay penalties to every function in a design, including storage elements,” says Stephen McMinn, vice-president of marketing and sales at ICS.

“We guarantee 99.5 percent minimum fault coverage, and our ATPGs handle the testability task transparently to the designer.” There is still a small penalty in silicon overhead. Typically, though, a 300-pin ASIC can be fully testable at sort time using only 14 pins.
Is your emulator giving you the whole picture?

MICE-V-486.
33MHz Emulation.
Real features.
Real-time.

Without real-time emulation you never know how your product will perform until it has to. Traditional in-circuit emulators slow your target to collect, display or reprogram. Or even stop emulation (or your target) to load complex triggers. When your emulator can't show you what's actually happening you risk missing a bug that will sneak from your prototype to the finished product.

MICE-V-486 lets you see it all.

▼ Real-time emulation to 33MHz.
▼ Complex, sequential triggers, loaded without slowing the emulator or target.
▼ Access to the fully qualified trace buffer during full-speed emulation.
▼ High level language debug.
▼ Probe kits for 386, SX, 376 and 286 support.

Most in-circuit emulators require partially or completely functional hardware to operate correctly. MICE-V-486 has a unique Isolation Mode™, requiring only a working clock signal. Logic analyzer taps are conveniently located to give you access to critical timing information. MICE-V-486 provides absolutely the fastest method for debugging non-functional 486-based hardware.

Microtek also has real-time emulators and source-level debuggers for 68000, -020, -030 and 80C186.

So, stop wasting development time because your emulator isn't real-time. Call us, and get your product to market fast.

MICROTEK
The Leader In Development Systems Technology.™
Design synthesis tools are starting to flaunt their testability features as well as their design prowess. Newer design compiler tools from Synopsys (Mountain View, CA) and Recal-Redac's ASIC Product Group (Westford, MA), among others, not only generate functional logic but also (transparently to the engineer) make that functional logic testable and automatically provide test vectors with around 99 percent coverage. Since overall, synthesized designs take up to 30 percent less silicon real estate than do gate and macro-level manually produced designs, the addition of another 30 percent to make a design fully testable brings the design close to parity with the silicon real estate of a manual design.

The Silcsyn tool from Recal-Redac (formerly Sile Technologies) provides a register-transfer-level scan capability that lets designers specify the allowable sequential depths of circuits. Silcsyn is an outgrowth of the MacPitts silicon compiler project from the Massachusetts Institute of Technology. The MacPitts compiler was perhaps the first truly behavioral silicon compiler, but its silicon implementation was inefficient. "We have stripped away the silicon-specific aspects of the tool and instead map it into libraries from specific silicon vendors from the proprietary design language notation, VHDL or EDIF netlist source file," says Paul Lindemann, director of marketing of Recal-Redac's ASIC Product Group. "The resulting tool automates design-for-test constraints and provides a flexible input and output mechanism for integrating into a design environment."

The Synopsys Logic Compiler accepts Boolean equations or netlists as inputs and provides synthesis and minimization based on rules for cell mapping, timing, and area constraints specified by the engineer. Synopsys also recently announced Test Compiler, which automatically removes redundant logic from a design, inserts scan elements, connects scan chains, optimizes the design for speed and area and then generates and compacts (by up to 40 percent) test vectors for up to 100 percent of the single stuck-at faults in a circuit.

Another product gaining headway is the Test Design Expert (TDX) from ExperTest (Mountain View, CA). TDX automatically generates test vectors from the same high-level descriptive language used to synthesize the logic. "By incorporating a concurrent fault simulator, TDX gains an advantage in speed over fault simulators, which test one fault at a time," says Ghulam Nurie, director of product marketing. "TDX also speeds up the task by using a proprietary heuristic algorithm linked to a knowledge base of test information." Valid Logic Systems (San Jose, CA), ViewLogic Systems (Marlboro, MA) and Test System Strategies Inc (Beaverton, OR) have announced support for ExperTest.

There is, however, some resistance to design synthesis from hard-core hardware designers who don't want to become programmers. An HDL or high-level language is just that, a language, and the task of hardware design is transformed into a programmer's task. Furthermore, although known states can be described, random or glitched conditions from power-up can create unknown states in sequencers, which can cause a locked condition in an indeterminate state. Designers must therefore design what they don't want as well as what they do.

Nevertheless, HDLs are quickly becoming commonplace. Most CAE vendors already have in place some form of VHDL support and are moving toward tying design synthesis, simulation and testability into one easy-to-digest pill.

Architectural enhancements

While steps are being taken to make testability easier to deal with on the design front, another approach being considered is the integration of testability into the basic fiber of the device before it becomes personalized by metal interconnect.

An approach for architectural modification that solves the design-for-testability issue comes from Oki Semiconductor (Sunnyvale, CA),
Guess where business goes shopping and win $10,000 spending money.

Here's your chance to prove you're a marketing genius and win $10,000 in the bargain.

We asked 9,823 business and professional executives what sources they find most useful in providing information about the products and services they buy for their companies. You can win our $10,000 jackpot by simply ranking the sources from 1 to 13 in the order that you think our survey respondents ranked them.

We'll tell you what came in second to get you started: It might surprise some people, but trade shows finished #2.

And we'll give you a hint about who's #1. It's the selling medium that:
• Speaks the business and professional buyer's language.
• Provides an environment with built-in credibility.
• Is loaded with helpful information about product and industry developments.

Now just get the rest of the answers right and you could win plenty of cash to go on a personal shopping spree.

Good luck.
DESIGN-FOR-TEST

CROSSCHECK'S EMBEDDED MATRIX

The Embedded Matrix from CrossCheck Technology provides built-in observability throughout the array. This streamlines and reduces silicon overhead in test design, since very little additional logic is necessary to be able to fully observe a function at the gate level.

which has implemented a built-in test structure that results in zero degradation in performance, according to the company.

Oki's MSM10T000 family of sea-of-gates arrays features dedicated locations of hand-crafted sequential blocks used solely for the implementation of scan-test flip-flops. This provides test resources that designers and tools can take advantage of without the silicon overhead associated with dedicated logic for scan implementation.

Oki claims that implementing the same amount of logic discretely would add 77 percent overhead to the size of the chip. What's more, since the test structure is architectured directly into the silicon, test pattern generators can generate 95 percent coverage in a matter of hours as opposed to days or more. Designers must still make sure that all devices with internal feedback are patched into the scan logic. They must also make sure that no race conditions exist, and they must add external signal lines for the scan clocks if internally generated clocks are used.

Another solution, from CrossCheck Technology (San Jose, CA), includes two elements: a patented on-chip test structure, and software tools that let designers take advantage of this unique architecture. "The patented structure includes a grid matrix embedded within the array, which transparently provides a large number of observable points," says Michael Carroll, vice-president of marketing at CrossCheck. "Typically, this structure adds roughly 10 percent silicon area overhead to the actual die, but allows the designer to observe gate-level behavior of actual devices for verification and debug." Since the test structure is part of the uncommitted array, it's necessary to fab these uncommitted arrays with the embedded test structure so that the test grid becomes a standard feature of the ASIC vendor's product.

Designers use the same conventional design approach and CAE tools as before, including libraries and simulation models. Timing is unaffected since the embedded test structure provides observability without degradation of signal. Once they're satisfied with the functionality and timing of a design, designers can then run the CrossCheck tools, which automatically generate test patterns with exceptionally high fault coverage as much as 50 times faster than conventional test pattern generators can.

So far, LSI Logic (Milpitas, CA) and Fujitsu Microelectronics (Santa Clara, CA) have licensed CrossCheck's technology and provide this approach to ASIC customers. Harris Semiconductor (Melbourne, FL) and the Advanced Device Center of Raytheon (Mountain View, CA) have also licensed this technology and are supporting it as part of their own design systems.

Simulation vectors

Designers of standard-cell and silicon-compiler ASICs have some special concerns when testability is an issue. Since a designer is designing at a larger functional-block level, the actual gate-level representations of these macro functions won't be available. It therefore becomes imperative that the silicon vendor provide designers with simulation vectors and a patch capability to a scan path or other test structure within the device. Since these macrocells are already characterized, simulation and timing models should exist for each standard cell and should be generated by each silicon-compiler module.

One approach for designers who need to design ultra-reliable devices is to add reconfigurable redundancies. Although this will drastically add to the silicon overhead associated with a specific design, this approach isn't that far-fetched for tactical and survivable designs.

One recent example of such an undertaking came from Motorola (Austin, TX) and TRW Electronics Component Group (La Jolla, CA), which jointly developed the first multimillion-device chip. Although not yet available to the general public, the groundwork has proved successful for future fabrication of highly dense ICs. The 0.5-µm CPUAX SuperChip has successfully been fabricated and tested for military applications.

Containing 4 million discrete devices, the SuperChip is touted as being the fastest floating-point processor yet, capable of performing two hundred 32-bit MFlops.

The most interesting feature of the CPUAX is its ability to repair itself, even during operations. Internal functional macrocells are reduc-
SCSI Data Acquisition from Analogic/CDA

**DASM-FGM**

SCSI Monochrome Frame Grabber

The DASM-FGM is a SCSI compatible, 8-bit grey scale video frame grabber for real-time digital image acquisition and display. The DASM-FGM acquires real-time video data, transfers image data to and from the host, and displays the data in monochrome or RGB pseudo-color. The DASM-FGM appears to the host as a RAMdisk connected to a host SCSI port.

The DASM-FGM captures, extracts and digitizes luminance information of input video data at a rate of up to 30 image frames per second. Up to 8 Mb of memory is available for storage of images at variable resolutions and frame sizes. The unit is packaged to fit into a standard 5 ¼” half-height peripheral bay, and uses power from the standard peripheral power connector designed for SCSI disk drives. Multiple DASM’s (7) can be connected to the same SCSI bus, and up to three cameras can be connected to each DASM-FGM.

**Applications**
- Manufacturing Inspection & Control
- Desk-top Publishing
- Security & Surveillance
- Military & Defense Imaging
- Robotics
- Optical Microscopy
- Busless Workstation Interface

**DASM-FGM Technical Specifications**
- 640 x 480 8-bit monochrome
- NTSC, PAL, RS170
- Video capture: 30 frames/s
- Three analog inputs
- Composite sync detection
- RGB & composite video out
- 256 x 8 input lookup table
- 256 x 24 output lookup table
- ALU for output operations
- 256K - 8 Mb RAMdisk memory
- 1 - 32 frame buffers (640x480x8)
- SCSI interface: 4 Mb/s
- 5 ¼ ” half-height form factor
- Standard disk drive power
- 17 watts
- Optional standalone enclosures
- On-board control processor
- Two 256 x 8 FIFO line buffers

**Hosts**
- DEC
- SUN
- APPLE
- IBM
- WANG
- Concurrent
- Motorola
- Other: any host w/SCSI

For further information, contact: Richard Steele
Analogic Corporation/CDA Division
8 Centennial Drive, Peabody, MA 01960-7987
Tel: (508) 977-3830, (800) 237-1011, Telex 681-7438
Fax: (508) 977-9220

Trademarks used from various companies.
dant internally and are capable of being switched in and out if an internal fault is detected. A powerful housekeeping system separates working from nonworking macrocells and disconnects the nonworking ones. The spares are then automatically patched in, even while the device is in the middle of an operation.

Of the 142 macrocells in the CPUAX, only 61 must be functional for complete operation. In device terms, of the 4 million devices on the chip, 1.7 million must function. Commercial successors to the SuperChip could find use in a wide variety of applications where the high speed, relatively low power, and reliability are necessary, such as advanced CAD/CAE, medical diagnosis, critical plant controls and ultracomplex imaging.

Although quite an accomplishment on its own, this Phase 2 VHSIC success is only the start. The design team plans to eventually build chips 150 times more dense.

**Board testability**

While ASIC testability continues to make inroads, life for design engineers gets real tricky at the board and system level. Printed circuit boards are shrinking in size, increasing in functional density and using more and more surface-mount components. Although the components may not be pushing limits of technology, the reduced spacings may mean that test points and access points to important signals and buses is getting harder and harder to do.

Take, for example, a typical microcontroller application where a 40-pin DIP lives with a 28- or 32-pin DIP RAM and ROM, a 20- or 24-pin DIP PAL, and other assorted DIP components. The 100-mil lead spacing leaves room for test probes, jumper clips, test headers (for buses and groups of signals) and so on.

When that same design is implemented using surface-mount components, the 25- and 50-mil spacings don’t easily allow test clips and probes to effectively look at one signal. What’s more, accidentally shorting two signals together while probing is easier to do on a surface-mount board, and if that happens to blow a chip, it becomes increasingly more difficult to perform rework when surface mount is utilized. Another concern is that tight and dense boards often require more than two layers. Blind and buried vias leave no access to signals.

Given these concerns, yet another responsibility is cast toward the design engineer to assure that adequate test points are left on the printed circuit board that will permit full-function and diagnostic capabilities for debug, production troubleshooting and repair operations. This concern becomes increasingly more important with smaller circuit boards, but also will be of prime concern when the industry starts moving toward multichip modules (MCMs), which will isolate the inner workings of a design even more from the engineer’s probing touch. In addition, bed-of-nails test approaches will be increasingly infeasible for verifying board or substrate continuity.

Fortunately, the boundary-scan test strategy works around this. As mentioned, boundary scan lets a compact (usually four-pin) bus serve as the master to a device’s I/O lines. As such, boundary-scan devices can be used on a printed circuit board, or MCM for that matter, which will allow engineers to test for continuity between signal points. By driving one set of outputs and verifying that the driven signal is present on all the associated inputs, continuity as well as a device’s inner workings can be verified.

This approach does have a few drawbacks, however. A board or MCM must be populated with devices to be able to perform this active test. And power must be applied to the circuit since each boundary-scan element must be alive. This means that some shorts could possibly damage components or crash the test bus.

Nevertheless, scan-compatible standard components are emerging to provide engineers with this option. For example, Bipolar Integrated Technology (Beaverton, OR) has incorporated a scan bus into its 64-bit B3130 floating-point processor, which has more than 55,000 ECL logic gates. The scan bus permits a test sequence to drive I/O and test internal functions. Packaged in a 395-pin pin grid array, the B3130 dissipates 24 W of power and features synchronous and asynchronous output enables for output ports and status flags.

**The test manufacturer’s view**

Tester manufacturers are obviously part of the driving force for test standards and implementation techniques. "If all board networks are accessible to traditional fixturing, a full bed-of-nails in-circuit approach may be used, which provides certain advantages," says Peter
High Data Flow Requirements Clouding Your VMEbus Design?

break through!

with Ironics high-throughput solutions!

Selecting a high-performance CPU may be the easiest part of your VMEbus design. But how do you overcome the real bottlenecks to system performance—getting data in and out, across, and between chassis?—not to mention the headaches in the design process itself.

Ironics can help you burrow through the high-data-flow haze... not only with hot CPUs, but with a complete line of bottleneck busting boards.

HIGH-THROUGHPUT SOLUTIONS FOR REAL-TIME BOTTLENECKS

High Speed DMA Daughter Boards
- 92 MBytes/sec, sustained, real-time I/O data rates directly into processor memory
- Designed for the Ironics family of RISC processors

Parallel I/O Daughter Board
- Data rates up to 38 MBytes/sec
- Designed for use with Ironics Full Speed Data Transporter

HIGH-THROUGHPUT SOLUTIONS FOR VMEBUS CONGESTION

Full Speed Data Transporter
- Block transfer rates up to 32 MBytes/sec across VMEbus
- Optimized for Ironics RISC and CISC processor boards

VSB Daughter Boards
- Alternate path for high speed data transfers between CPU, Memory and I/O boards
- Designed for the Ironics family of RISC and CISC processors

HIGH-THROUGHPUT SOLUTIONS FOR INTERCHASSIS DATA TRANSFERS

Multiprocessor PipeLine
- 20-30 MBytes/sec, sustained, inter-chassis transfer rates
- Multiple system link for VMEbus chassis and/or VME compatible SUN Workstations

High Speed DMA Daughter Boards
- 92 MBytes/sec transfers between processor boards or VMEbus chassis
- Designed for the Ironics family of RISC processors

HIGH-PRODUCTIVITY SOLUTIONS FOR REAL-TIME DEVELOPMENT

CASEworks/RT
- Integration Toolkit
- High Level Debugger
- Application Simulator
- Real Time Kernels
- VXWorks
- pSOS, pSOS+
- OS9
- VRTX
- The most complete, highly integrated, and flexible Real Time tool set

For more information on Ironics’ Hot Processor Boards, High Speed I/O Boards, High-Throughput Data Transfer products, Real-Time Target Systems, and High Productivity Development environments, contact:

Ironics Incorporated
790 Cascadilla Street
Ithaca, New York 1486

phone: 867-271-4660
fax: 867-272-5767
telex: 785742

©1990 Ironics, Inc.
Hansen, applications manager at Teradyne (Boston, MA), “All shorts testing can be done with no power applied to the board, thus saving some components that may be damaged if powered up with a fault. Further, test patterns with 100 percent fault coverage can be easily generated using this approach since all connections are compatible with the netlist.”

But Teradyne is also supporting scan continuity testing. The test stimulus applied by automatic test equipment is captured by scan input cells while the stimulus shifted into boundary-scan output cells is monitored by automatic test equipment. By avoiding the core logic of devices under test, vectors are simplified and continuity can be verified quickly.

For applications where some elements are scannable and some are not, a mixed approach may be the answer. Here, scannable elements are tested exclusively through scan techniques, and fixturing for the test fixture is aimed at verifying the nonscannable elements. While this still requires some nails for a fixture, the nail count is significantly reduced.

Another technique is to cluster the physical implementation of a function so that it’s testable as an entire function. A bit of forethought is required here, since some discretely implemented scan logic often must be designed into a function to guarantee controllability and observability of some key verifying signals. But this technique does let even simpler testers perform detailed testing, since larger blocks are being verified with fewer vectors.

The technique that requires the most up-front engineering effort is to use scan exclusively to test the entire functionality of a board or system. Unless partial or full scan is employed, this can be more time-consuming than just using boundary-scan techniques. What’s more, many devices won’t incorporate the scan logic on-chip, meaning that discrete scan elements must be added to the circuit.

This does offer some advantages, though. Since scan test requires only a few signal lines to verify a device, testers can get smaller, even though the number of vectors applied is usually deeper. Furthermore, the entire tester operation is, for the most part, synchronous to the scan clock. This, coupled with the fact that the testers can be smaller and less sophisticated, means that simultaneous gang testing is possible since the entire tester will be synchronously transmitting, receiving and comparing.

Teradyne isn’t alone in pursuing these new test techniques. Makers of high-end testers such as GenRad (Concord, MA) and LTX (San Jose, CA), as well as makers of mid-level ASIC verifiers and testers such as Integrated Measurement Systems (Beaverton, OR), Hilevel Technology (Irvine, CA), ASIX Systems (Fremont, CA) and Tektronix (Beaverton, OR) are moving toward more up-front engineered strategic test philosophies.

One example is the collaboration between Motorola and Schlumberger Technologies ATE Division (San Jose, CA), which together created the Typhoon architecture.

The Typhoon supports scan-data rates up to 40 MHz and internal built-in self-test (BIST) rates to 800 MHz. Up to 4 Gbytes of local memory can feed its 64 high-speed and 1,024 broadside scan channels of this tester for CMOS, BiCMOS and bipolar devices. “The philosophy behind Typhoon is that only 10 percent of the time available from a tester is needed to do ac parametric testing, and the cost premium for a tester with the ac parametric capabilities was 70 percent,” says David Karpenske, vice-president of strategic products at Schlumberger.

“By eliminating parametric test features and going with ‘at-speed’ testing using BIST, up to 800-MHz parametrics can be performed.”

—David Karpenske, Schlumberger

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.
Get the Facts

When evaluating RISC processors for embedded applications, you need real benchmark data from independent sources. The R3001 Performance Comparison Report is a collection of the original third-party data used in the graph below.

Benchmark Your Code

Of course, we know that published data can’t give you all the information. You’d prefer to perform benchmarks for your specific application, and our six technology centers are equipped to do just that — bring us your code and we’ll run your benchmarks!

You Can Count On Us

IDT offers a full array of complementary high-performance system building blocks for all your applications. Contact us today and get the facts: an R3001 Data Pak and R3001 Performance Comparison Report.

IDT Corporate Marketing
P.O. Box 58015
3236 Scott Blvd.
Santa Clara, CA 95052-8015

(800) 345-7015
FAX: 408-492-8454

CIRCLE NO. 63

When cost-effective performance counts

Embedded RISC

REAL-TIME PERFORMANCE

<table>
<thead>
<tr>
<th>Processor</th>
<th>Clock Rate</th>
<th>Interrupt Response</th>
<th>Context Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel 80486</td>
<td>12.5-33MHz</td>
<td>Fair</td>
<td>?</td>
</tr>
<tr>
<td>IDT R3001</td>
<td>12.5-33MHz</td>
<td>Fast</td>
<td>10µs</td>
</tr>
<tr>
<td>AMD 29000</td>
<td>12.5-33MHz</td>
<td>Fair</td>
<td>29µs</td>
</tr>
</tbody>
</table>

DEVELOPMENT TOOLS

<table>
<thead>
<tr>
<th>Feature</th>
<th>Intel 80486</th>
<th>IDT R3001</th>
<th>AMD 29000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Native Platform</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>IBM PC Tools</td>
<td>Yes</td>
<td>Intel</td>
<td>Yes</td>
</tr>
<tr>
<td>In-circuit Emulation</td>
<td>$960</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Simulation Tools</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Evaluation Board</td>
<td>No</td>
<td>VxWorks</td>
<td>No</td>
</tr>
<tr>
<td>CPU Modules</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SOFTWARE SUPPORT

<table>
<thead>
<tr>
<th>Compiler</th>
<th>Intel 80486</th>
<th>IDT R3001</th>
<th>AMD 29000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Robust Compilers</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RTOS</td>
<td></td>
<td>C. EXECUTIVE</td>
<td>VRTX, C. EXECUTIVE</td>
</tr>
</tbody>
</table>


RISCcontroller is a trademark of Integrated Device Technology
More and more...

Advertisers are investing in Computer Design Magazine’s unique readership

ADVERTISING GROWTH - FIRST SIX MONTHS 1990

Changes in Percent*

Changes in Pages*

* These figures include magazine editions only of Computer Design and EDN

Source: MMS Rome Reports

Our Magazine Edition’s 70% engineering management, 100% design & development qualified circulation is causing more and more advertisers to take a new look at where electronics OEM marketers are placing their ad dollars. In these leaner, tougher times, they are turning to COMPUTER DESIGN to deliver their message, promote their products and boost their sales to today’s computer/micro-processor-based OEMs.
## 1991 Computer Design Magazine Edition

### UPCOMING ISSUES

<table>
<thead>
<tr>
<th>MONTH</th>
<th>SPECIAL REPORT</th>
<th>TECHNOLOGY FOCUS</th>
<th>PRODUCT FOCUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>January 1</td>
<td>30th Anniversary Issue — The evolution of electronics into computers</td>
<td>FDDI ICs — Ron Wilson</td>
<td>Logic analyzers</td>
</tr>
<tr>
<td></td>
<td>COMPUTER DESIGN editors</td>
<td>Design capture — Mike Donlin</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>February 1</td>
<td>Workstation buses</td>
<td>Mixed CMOS, ECL &amp; BICMOS — Barbara Tuck</td>
<td>High-speed D-A converters</td>
</tr>
<tr>
<td>Buscon Systems/USA</td>
<td>Warren Andrews</td>
<td>LAN controllers ICs — Ron Wilson</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>March 1</td>
<td>Fuzzy logic in embedded control</td>
<td>Static RAMs</td>
<td>Emulators</td>
</tr>
<tr>
<td></td>
<td>Tom Williams</td>
<td>Designing ASICs for testability — Barbara Tuck</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>April 1</td>
<td>PCB layout tools</td>
<td>High-level design languages — Mike Donlin</td>
<td>Op amps</td>
</tr>
<tr>
<td>Electro</td>
<td>Mike Donlin</td>
<td>Object-oriented programming — Tom Williams</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>May 1</td>
<td>Superfast processors</td>
<td>Communication with standard buses — Warren Andrews</td>
<td></td>
</tr>
<tr>
<td>CICC Comdex</td>
<td>Ron Wilson</td>
<td>Disk controller ICs — Ron Wilson</td>
<td>Multibus CPU boards</td>
</tr>
<tr>
<td>June 1</td>
<td>Design synthesis</td>
<td>Mezzanine buses — Warren Andrews</td>
<td>DRAMs</td>
</tr>
<tr>
<td>DAC</td>
<td>Barbara Tuck</td>
<td>Device modeling — Mike Donlin</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>July 1</td>
<td>CASE for real-time Programming</td>
<td>CAD frameworks — Mike Donlin</td>
<td>Device programmers</td>
</tr>
<tr>
<td></td>
<td>Tom Williams</td>
<td>RISC in real-time — Tom Williams</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>August 1</td>
<td>Mixed-signal ASICs</td>
<td>Display controller ICs — Ron Wilson</td>
<td></td>
</tr>
<tr>
<td>Siggraph</td>
<td>Barbara Tuck</td>
<td>Software-management tools — Tom Williams</td>
<td></td>
</tr>
<tr>
<td>September 1</td>
<td>Enhanced-performance standard buses</td>
<td>Accelerators to boost standard-bus performance — Warren Andrews</td>
<td>Flash EPROMs</td>
</tr>
<tr>
<td>Buscon Systems/USA ESC</td>
<td>Warren Andrews</td>
<td>High-resolution A-D converters — Ron Wilson</td>
<td>Jeff Child</td>
</tr>
<tr>
<td>October 1</td>
<td>32-bit microcontrollers</td>
<td>Fast PLDs — Barbara Tuck</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ron Wilson</td>
<td>RISC-based CPU boards — Warren Andrews</td>
<td></td>
</tr>
<tr>
<td>November 1</td>
<td>System simulation and verification</td>
<td>High-density ASIC packaging — Jeff Child</td>
<td>STD CPU boards</td>
</tr>
<tr>
<td>Wescoson ITC</td>
<td>Mike Donlin</td>
<td>Multiprocessing in real-time — Tom Williams</td>
<td></td>
</tr>
<tr>
<td>December 1</td>
<td>Migrating PLDs to full ASICs</td>
<td>Accelerators to boost standard-bus performance — Warren Andrews</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Barbara Tuck</td>
<td>8- and 16-bit microcontrollers — Ron Wilson</td>
<td></td>
</tr>
</tbody>
</table>
Time will be the true currency of the 90s. As competitive pressures accelerate the need for you to stay current with advancing technologies becomes paramount. Trade shows have the unique ability to leverage your time as you seek new technical information and strive to establish a competitive advantage for your company. For a complete guide to surface mount technology in the 90s visit SMTCON West at the Santa Clara Convention Center.
The 2,400-bit/s modem is entrenched as the standard in data communications. And though users have long recognized that higher-speed modems reduce time and communication charges, it’s widely agreed that the 2,400-bit/s modem won’t become outdated as quickly as the slower devices that came before it. When the 1,200-bit/s modem came along, for instance, it quickly replaced its 300-bit/s predecessor. Similarly, the advent of the 2,400-bit/s modem swiftly pushed the 1,200-bit/s modem aside.

But now, in the day of 2,400-bit/s modems, performance enhancement standards have emerged that are giving the 2,400-bit/s modem ICs a new lease on life. Among those standards gaining wide acceptance are Microcom Networking Protocol (MNP) Class 4 and V.42 for error correction and MNP Class 5 and V.42bis for data compression.

Because these standards let modems exchange data at greater throughputs, they’re satisfying users’ demands for speed without the need to create a whole new hardware platform. Support for error correction and data compression can be provided right in the firmware. Manufacturers of 2,400-bit/s modem chip sets are integrating these features into their latest designs.

This feature-driven trend has altered the modem IC market. “By offering features like MNP 5, board designers are able to provide a broader product line. They can offer both a low end and a high end by incorporating different combinations of features,” says Shyam Dujari, senior marketing manager of Exar (San Jose, CA). This flexibility has inspired modem IC manufacturers to add more and more features to their products. Some have even gone beyond traditional data modem functions and added fax capabilities.

Although modem chip set manufacturers are integrating more new features into their designs, they’re still preserving ties to earlier standards, including the venerable Bell 103 standard for 300-bit/s transmission. By having 300-bit/s support, a modem can be configured to shift down to a lower speed if it encounters a bad phone line. Besides, it seems almost no one in the modem industry wants to be the first not to offer Bell 103 compatibility.

**Blending modems and fax**

The most recent trend among modem IC manufacturers is to combine data modem and fax functions in the same chip set. Sierra Semiconductor (San Jose, CA) makes Sendfax, a line of modem solutions that adds send-only fax capabilities. Sierra’s SC11046 single-chip device adds 4,800-bit/s Group 3 fax capability to a full-duplex, Hayes-compatible, V.22bis, 2,400-bit/s modem. An external controller performs all the handshaking functions, including fax-call setup conforming to the CCITT T.30 standard.

Sierra has found a range of situations in which a send-only fax capability is sufficient. It allows laptop users in the field, for instance, to use any local fax machine as a printer. In the corporate environment, send-only fax capability lets PC users transmit faxes without having to first print out a document and then wait to gain access to a fax machine. Sendfax implementation is simple, so it isn’t much added cost. It involves only a modification to the analog front end and to the code. For all its added market value, it’s a relatively inexpensive feature to add, according to Sierra.

Exar has taken the next step in the integration of fax and data modem functions with its combined fax/data modem in the form of a two-chip set. The XR-2900 serves as a modem data pump for both 9,600-bit/s V.29 fax and 2,400-bit/s V.22bis data communications requirements. The XR-2900 also supports two other fax and three other data modem standards. This wide range makes the device compatible with MNP options and the proposed V.42/V.42bis compression/correction standard.

The 2900 is made up of a mainly analog front end and a digital back end. In the analog chip, Exar has packed the analog line filtration and amplifiers required for fax use, a 10-bit receive analog-to-digital converter, a 9-bit transmit digital-to-analog converter, a clock phased-locked loop and some interface circuitry. The digital chip includes the signal processing and transform circuitry.

**Standards breathe new life into 2,400-bit/s modem ICs**

Jeffrey Child, Associate Editor

Exar’s XR-2900 chip set integrates a 2,400-bit/s V.22bis data modem with 9,600-bit/s Group 3 send/receive fax capabilities. With analog and DSP circuitry partitioned into a two-chip set, OEMs can combine the XR-2900 with an external controller and memory to form a complete data/fax modem.
<table>
<thead>
<tr>
<th>Model</th>
<th>Full compatibility</th>
<th>CCITT compatibility</th>
<th>UART on-chip</th>
<th>AT command set</th>
<th>Interfaces</th>
<th>Power consumption (mW)</th>
<th>Packaging</th>
<th>Price/Quantity</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dallas Semiconductor</strong></td>
<td>4350 S Beltwood Pkwy, Dallas, TX 75244 (214) 450-0400</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DS2244T</td>
<td>212A, 103</td>
<td>V.22bis</td>
<td>N</td>
<td>Y</td>
<td>S</td>
<td>200</td>
<td>SIMM 3.5x0.85x0.375 in.</td>
<td>$781,000</td>
<td>Full-function µC with modem, capable of embedded control and data storage</td>
</tr>
<tr>
<td>DS2245</td>
<td>212A, 103</td>
<td>V.22bis</td>
<td>Y</td>
<td>Y</td>
<td>P</td>
<td>250</td>
<td>SIMM 3.5x0.85x0.375 in.</td>
<td>$781,000</td>
<td>FCC part 68 reg. when used with DS2249 DAA</td>
</tr>
<tr>
<td>DS2246</td>
<td>212A, 103</td>
<td>V.22bis</td>
<td>Y</td>
<td>Y</td>
<td>P</td>
<td>250</td>
<td>SIMM</td>
<td>$781,000</td>
<td>MNP5, error correction</td>
</tr>
<tr>
<td><strong>Exar</strong></td>
<td>2222 Qume Dr, PO Box 49007, San Jose, CA 95161-9007 (408) 434-6400</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2900</td>
<td>212A, 103</td>
<td>V.21 channel 2, V.22, V.22bis, V.27ter, V.29, V.42, V.42bis</td>
<td>N</td>
<td>Y</td>
<td>S, P</td>
<td>500</td>
<td>DIP, PLCC, QFP</td>
<td>$27.33/10,000</td>
<td>MNP2-5, AT command set, TR29, T.30 provided</td>
</tr>
<tr>
<td>2400</td>
<td>212A, 103</td>
<td>V.22, V.22bis, V.42, V.42bis</td>
<td>N</td>
<td>Y</td>
<td>S, P</td>
<td>400</td>
<td>DIP, PLCC, QFP</td>
<td>$18.51/10,000</td>
<td>MNP2-5, Exar AT command set provided, V.21/V.23 also supported</td>
</tr>
<tr>
<td><strong>Intel</strong></td>
<td>1900 Prairie City Rd, FM2-18, Folsom, CA 95630 (916) 351-5133</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>89C024XE</td>
<td>212A, 103</td>
<td>V.21, V.22A/B, V.22bis</td>
<td>N</td>
<td>Y</td>
<td>S</td>
<td>385</td>
<td>28-pin PDIP, 28-pin, 68-pin PLCC</td>
<td>$26/10,000</td>
<td>2 chips, CHMOS, MNP software available</td>
</tr>
<tr>
<td>89C024LT</td>
<td>212A, 103</td>
<td>V.21, V.22A/B, V.22bis</td>
<td>N</td>
<td>Y</td>
<td>S</td>
<td>400</td>
<td>28-pin PDIP, 28-pin, 68-pin PLCC</td>
<td>$26/10,000</td>
<td>CHMOS, 2 chips in 3 in.², sleep and resume modes</td>
</tr>
<tr>
<td>89024</td>
<td>212A, 103</td>
<td>V.21, V.22A/B, V.22bis, N</td>
<td>N</td>
<td>S</td>
<td>S</td>
<td>1.5W</td>
<td>28-pin PDIP, 28-pin, 68-pin PLCC</td>
<td>$16/10,000</td>
<td>2-chip solution</td>
</tr>
<tr>
<td><strong>NEC Electronics</strong></td>
<td>401 Ellis St, Mountain View, CA 94043 (415) 960-6000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>µPD77810</td>
<td>—</td>
<td>—</td>
<td>Y</td>
<td>—</td>
<td>—</td>
<td>68-pin PLCC</td>
<td>—</td>
<td>—</td>
<td>Flexible, user programmable, use any front end and gain variable amp, guard-tone generator, 8-bit A-D, D-A converters used w/77811, does modulation and tone generation/detection</td>
</tr>
<tr>
<td>µPD77811</td>
<td>—</td>
<td>—</td>
<td>Y</td>
<td>—</td>
<td>—</td>
<td>44-pin PLCC</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>µPD77812</td>
<td>—</td>
<td>—</td>
<td>Y</td>
<td>—</td>
<td>—</td>
<td>68-pin PLCC, 74-pin QFP</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td><strong>Oki Semiconductor</strong></td>
<td>785 N Mary Ave, Sunnyvale, CA 94086-2909 (408) 720-1900</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MSM6994-01FEP</td>
<td>212, 202, 103</td>
<td>V.21, V.22, V.22bis, V.23, V.27, V.29, V.32</td>
<td>N</td>
<td>N</td>
<td>S</td>
<td>150</td>
<td>64-pin mini-DIP, 64-pin FP, 68-pin PLCC</td>
<td>$20/50,000</td>
<td>Meant for use with DSP chip, band limit filtering, carrier detection, AGC, call progress</td>
</tr>
<tr>
<td><strong>Rockwell Comm Systems, Digital Comm Div</strong></td>
<td>4311 Jamboree Rd, Newport Beach, CA 92658 (714) 833-6849</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RC224AT</td>
<td>212A, 103</td>
<td>V.22, V.22bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>300</td>
<td>68-pin PLCC</td>
<td>$24/10,000</td>
<td>Single complete modem</td>
</tr>
<tr>
<td>RC2324AC</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.42, V.42bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>650</td>
<td>68-pin PLCC</td>
<td>$35/10,000</td>
<td>2-chip integrated quad modem with MNP2-5</td>
</tr>
<tr>
<td>RC2324DP/1</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.23</td>
<td>—</td>
<td>—</td>
<td>S, P</td>
<td>500</td>
<td>68-pin PLCC</td>
<td>$26.50/10,000</td>
<td>Single-device quad modem data pump, HDLC framing</td>
</tr>
<tr>
<td>RC9624AT</td>
<td>212A, 103</td>
<td>V.21 channel 2, V.22, V.22bis, V.27ter, V.29</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>300</td>
<td>68-pin PLCC</td>
<td>—</td>
<td>2-chip set; 9,600-bit/s send/receive G3 fax</td>
</tr>
<tr>
<td><strong>SGS-Thomson</strong></td>
<td>1000 E Bell, Phoenix, AZ 85022 (602) 867-6100</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TS75C25</td>
<td>212, 103</td>
<td>V.21, V.22, V.22bis, V.23</td>
<td>N</td>
<td>N</td>
<td>P</td>
<td>700</td>
<td>1x48 DIP, 1x40 DIP, 1x52 PLCC, 1x44 DIP</td>
<td>$18/10,000</td>
<td>2 chips, CMOS</td>
</tr>
<tr>
<td><strong>Sharp Digital Information Products</strong></td>
<td>16841 Armstrong Ave, Irvine, CA 92714 (714) 261-6224</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-4810S</td>
<td>212A, 103</td>
<td>V.22A/B, V.22bis</td>
<td>N</td>
<td>N</td>
<td>S</td>
<td>500</td>
<td>64-pin QFP</td>
<td>$34/1,000</td>
<td>2 chips; CMOS; 4,800-bit/s full-duplex mode; V54 test modes</td>
</tr>
</tbody>
</table>

118 SEPTEMBER 1, 1990 COMPUTER DESIGN
<table>
<thead>
<tr>
<th>Model</th>
<th>Bill compatibility</th>
<th>COM port compatibility</th>
<th>UART on-chip</th>
<th>AT command set</th>
<th>Power consumption (mW)</th>
<th>Packaging</th>
<th>Price/Quantity</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SK0611</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>330</td>
<td>DIP, PLCC</td>
<td>$18/10,000 basic modem</td>
</tr>
<tr>
<td>SK423</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis</td>
<td>Y</td>
<td>Y</td>
<td>P</td>
<td>260</td>
<td>DIP, PLCC</td>
<td>$21/10,000 5-V supply, power down, laptop modem</td>
</tr>
<tr>
<td>SK2491</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.42bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>270</td>
<td>DIP, PLCC</td>
<td>$25/10,000 5-V supply, power down, MNPS5/V</td>
</tr>
<tr>
<td>SK2691</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.42bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>310</td>
<td>DIP, PLCC</td>
<td>$26/10,000 MNPS5</td>
</tr>
<tr>
<td>SK4611</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.27ter</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>280</td>
<td>DIP, PLCC</td>
<td>$20/10,000 basic Sendfax 48 modem</td>
</tr>
<tr>
<td>SK4721</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.27ter, V.29</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>260</td>
<td>DIP, PLCC</td>
<td>$22/10,000 5-V supply, laptop Sendfax</td>
</tr>
<tr>
<td>SK5474</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.27ter, V.29</td>
<td>Y</td>
<td>Y</td>
<td>P</td>
<td>260</td>
<td>DIP, PLCC</td>
<td>$32/10,000 5-V supply, power down, smallest footprint, low parts count, pocket Sendfax, 2 chips</td>
</tr>
<tr>
<td>SK5475</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.27ter, V.29</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>270</td>
<td>DIP, PLCC</td>
<td>$34/10,000 5-V supply, power down, smallest footprint, low parts count, laptop Sendfax, 2 chips</td>
</tr>
<tr>
<td>SK5491</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.27ter, V.29, V.42, V.42bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>720</td>
<td>DIP, PLCC</td>
<td>$33/10,000 power down: 2.400-bits data modem w/ send/receive fax modem</td>
</tr>
<tr>
<td>SQ2496</td>
<td>212A, 103</td>
<td>V.21, V.22, V.22bis, V.27ter, V.29, V.42, V.42bis</td>
<td>Y</td>
<td>Y</td>
<td>S, P</td>
<td>750</td>
<td>DIP, PLCC</td>
<td>$40/10,000 power down: MNPS5/42bis data modem w/ send/receive fax modem</td>
</tr>
</tbody>
</table>

**Sierra Semiconductor** 2075 N Capitol Ave, San Jose, CA 95132 (408) 263-9300

**Silicon Systems** 14351 Myford Rd, Tustin, CA 92680 (714) 731-7110

**United Microelectronics** 3350 Scott Blvd, Bldg 48 & 49, Santa Clara, CA 95054 (408) 727-9589

**Xecom** 374 Turquoise St, Milpitas, CA 95035 (408) 945-6640

**Comments**
PRODUCT FOCUS/Modem ICs

INTEGRATED CIRCUITS

necessary to go between the converter inputs or outputs and a microcontroller interface.

Separating modem functions
Modem IC manufacturers are also differentiating their products by the way they partition modem functions. While some manufacturers combine a data pump and a controller in a set, others use an analog front end and a digital signal processor.

Typical of the latter partitioning style is the T75C25, a V.22bis modem chip set from SGS-Thompson (Phoenix, AZ), consisting of a preprogrammed CMOS DSP plus an analog front end. Together these devices form a modem that can operate at up to 2,400 bit/s, full duplex. The DSP implements the signal processing necessary to send and receive data, plus utilities such as call-progress tone detection and tone generation. The analog front end incorporates the circuits required for programmable gain control, clock generation and signal filtering. Because the T75C25 uses a preprogrammed DSP, it can be customized simply by modifying software.

Although 2,400-bit/s modems won't be outdated overnight, the next jump in speed for modem designs will come—probably at 9,600 baud.

RC2324AC from Rockwell International (Newport Beach, CA) integrates the V.42bis data compression algorithm into its chip set. Modems using V.42bis can achieve up to 9,600 bit/s of data throughput. In addition to V.42bis, the RC2324AC has MNP 4 and V.42 error correction and MNP 5 data compression built into its firmware. This CMOS chip set offers adaptive equalization, which lets the modem automatically compensate for telephone line distortions.

The digital domain
Although 2,400-bit/s modem won't be outdated overnight, the next jump in speed for modem designs will come eventually—probably at 9,600 baud. In fact, there are products today that support V.32, the protocol for 9,600-bit/s operation. But to achieve this next jump in speed requires a technology significantly different from traditional analog approaches.

Using this new technology is the MSM6994, the latest offering from Oki Semiconductor (Sunnyvale, CA). It's unique among modem devices in that it operates in the digital domain rather than the analog. The MSM6994 supports up to eight standards including V.32 and fax standards. It's a front-end processor chip designed to operate with a general-purpose DSP. Separate transmit and receive functions are integrated in this device. At the heart of the MSM6994 is a 5-Mips DSP core providing band-limiting filtering, carrier-detecting and automatic gain control with call-progress tone detection. The chip also contains A-D and D-A converters that replace the switch-capacitor filter usually used in modem front ends.

"When you're doing 9,600 baud, you can't use switch-capacitor filtering," says Jerry Gora, technical marketing engineer at Oki. Switch-capacitor filtering has a lot of phase delay problems. To build a device equivalent to the MSM6994 in the analog domain, says Gora, would require four stages of op-amps and many discrete components. Since the MSM6994 does its processing in the digital domain, it can maintain phase-coherency on all the filters.

Targeting laptops
The laptop arena also demands special features from 2,400-bit/s modem ICs. Whether designed into the motherboard or into an external socket, the total modem circuit in a laptop must be as small as possible while drawing low power. Laptop modems also should support the power-down capability popular in laptops.

With these requirements in mind, Intel (Santa Clara, CA) has created the 89C024LT. Specifically targeted for laptop designs, the 2,400-bit/s 89C024LT consumes 400 mW in normal operation and 5 mW in standby mode. The chip set conforms to MNP classes 1 through 5 while supporting the sleep and resume modes found in most laptops. Controlled by the 89C026LT microcontroller through a high-speed serial data link, the 89C027 analog front end handles the complex filtering functions required by the modem. The 68-pin 89C026LT also performs DSP, call monitoring, and Hayes-compatible command-set and user-interface functions.

Another modem solution for laptop configurations is the 75D2240 chip set from Silicon Systems (Tustin, CA). The set includes the main 73K224L modem chip and the 73D600 microcontroller. Combined, these chips offer an AT command interpreter compatible with the Hayes 2400 Smartmodem command set. The modem operates from a single 5-V supply and requires only 125 mW of power, 30 mW in sleep mode. The chip set also offers dual-tone multifrequency dialing, automatic speed detect and terminal autobaud.
A World of Choice

When it comes to mass storage needs, your choice is clear: Ricoh optical disc drives. From WORM and rewritable to bare drive and entire library units or subsystems, Ricoh offers a world of choice. Each drive boasts quality you can trust to safeguard vital information. The kind of quality that comes from over 50 years of know-how in optics and image processing, in such products as cameras, copiers, facsimiles, telepress, laserprinters and scanners. Now you know why Ricoh is the world’s leading supplier of 5-1/4" optical disc drives. For more information, call 1 (800) 955-FILE.

1. RH5500/5-1/4" REMOVABLE CARTRIDGE HARD DISK DRIVE
2. RS-9100H/5-1/4" HALF-HEIGHT WORM SUBSYSTEM
3. RO-5030EII/REWRITABLE OPTICAL DISK DRIVE
4. RJ-5330E/MAGNETO-OPTICAL DISK LIBRARY UNIT

BEST FOR QUALITY.
UNMATCHED FOR SERVICE.

RICOH CORPORATION (File Products Division) 5150 El Camino Real, M/S D-20, Los Altos, Ca 94022 U.S.A Phone: 415-962-0443 Fax: 415-962-0441
RICOH CORPORATION (Eastern Region Office) 59 Stiles Road, Suite 102, Salem, NH 03079 Phone: 603-893-0547 Fax: 603-893-4162

CIRCLE NO. 66
VMEbus accelerator board offers 1.3M fuzzy-rule evaluations/s

Designed for either Unix-based fuzzy-processing applications or stand-alone applications, the FCA10VME is a four-processor parallel fuzzy-processing VME board from Togai InfraLogic. The board provides four of Togai’s custom FC110 digital fuzzy processors (DFPs) arranged to run in flexible combinations, allowing up to 1.3 million fuzzy-rule evaluations/s. Up to 64 boards may be used in the same computer system for a total of 256 fuzzy processors operating in parallel.

The message-passing facilities integral to the FC110 DFP allow each processor independent communication to the host computer system. By using these message-passing features and coupling the processors at the software level, users can create many different architectures for parallel-processing systems without changing the hardware. This lets researchers experiment with disjoint, systolic, mesh, hypercube and hypertorus architectures all in the same development platform.

The vital organs of the board are the four DFPs, each operating at 20 MHz. At this speed, each DFP performs as a 10-Mips fuzzy-computing node. With 128 kbytes of knowledge-based memory exclusive to each node, each processor has uninhibited access to its own knowledge base. In addition, there are 256 bytes of shared variable space between each FC110 and the host computer. This memory is used for passing messages, commands and data between the node and the host computer. With all four processors active, the FCA10VME board provides up to 40 Mips of fuzzy-computing power.

Making optimum use of available memory, the logical addressing on the card is configured to minimize the physical address space. Requiring only 256 kbytes of physical address space in a VME system, the 512 kbytes of knowledge-based memory is switched into physical memory 128 kbytes at a time. This lets the host switch the knowledge-based memory of a node into the physical address space of the system, download the knowledge base, and then switch to the next node.

The availability of each node is key to the board’s performance, letting the DFPs be used in flexible combinations. Because of this, they aren’t switched like the knowledge-based memory; they’re mapped into physical memory so there’s no unnecessary overhead when accessing them. The control and status registers are also permanently mapped into the physical memory.

The FCA10VME is supported by two major software development tools. The TILShell is a graphical tool for creating and modifying expert systems, including ones that will run on the FCA10VME. The FC110 Development System includes a compiler, an assembler and a linker. The compiler and assembler produce relocatable object modules. These modules are combined by the linker to produce load images for the FC110 processors and to create C interface code for the expert system.

Unix-based or stand-alone uses

Built to be easily integrated into existing VME systems, the FCA10VME requires different interface methods depending on the type of operating system used. The interface depends on whether a “protected” operating system such as Unix is used. A protected operating system is one which blocks an application process from accessing arbitrary memory locations.

When operating in a protected operating system, an application program wishing to access the FCA10VME board must do so via a device driver. For use under Sun O/S Version 4.0.1, the board is supplied with C source code for a simple Unix device driver.

In a stand-alone application a program can access the FCA10VME’s fuzzy processors in a more direct manner: by just reading and writing to locations in the VME address space.

The FCA10VME fits in a single 6U form factor. Hardware jumpers are provided to allow both nonprivileged and supervisor access, letting the FCA10VME function as a generally available embedded peripheral or a system-regulated resource. Available now, the board is priced at $4,500.

-- Jeff Child

Togai InfraLogic
30 Corporate Pk, Suite 107
Irvine, CA 92714
(714) 975-8522
Circle 359
Great connections! Bridge, Router and LAN/WAN Gateway on one VMEbus board.

- Two Ethernet Ports (TSVME 551E).
- Six X.25 Ports, with rates up to T1 and CEPT 2.048 Mbits/sec (TSVME 551X).
- Token Ring (IEEE 802.5), with Source Router chip support (TSVME 551T).
- Multiprocessor Triple-Bus™ architecture crunches protocol stacks up to 3 times faster.
- Unique DMA design provides VMEbus data block transfer rates in excess of 20MB/sec.


Themis’ “open systems” strategy puts Bridge, Router and Gateway functions on one VMEbus board. The TSVME 551-Triple-Bus™ means performance.
The TSVME 551-Triple-Bus and proprietary high-performance DMA engine make possible simultaneous data transfers between:
1. 68020 MPU and 512 Kbytes of local memory,
2. DMA data buffer and VMEbus,
3. Communications controller module and 1 Mbyte of shared memory.

Step up to the Themis TSVME 551-. It’s multiprocessing, multi-port and supports multiple network technologies. All on one VMEbus platform.

Free Technology Report.

Call (415) 734-0870, fax (415) 734-0873, or in Europe, 33.1.69.86.15.25, fax 33.1.64.46.45.50.

At Themis, we’re making the open systems promise a reality.
NEW PRODUCT HIGHLIGHTS

COMPUTERS AND SUBSYSTEMS

68040-based VMEbus board features intelligent I/O subsystem

The 68-41, the latest 68040-based VMEbus single-board computer (SBC) from Radstone Technology, provides multiple microprocessors and dual-ported memories for high-performance real-time applications. A key factor to the 68-41’s performance is its on-board intelligent I/O subsystem, responsible for avoiding I/O bottlenecks. Such bottlenecks can seriously hinder the processing strength of multifeatured VME SBCs such as the 68-41, with its multiple local and external buses and various I/O interfaces. To ensure optimum processing power and the free flow of data, the I/O subsystem lets the board operate at full performance even when all its local and external interfaces are in use.

At the heart of the board is the 68040 microprocessor, with up to 16 Mbytes of multiport DRAM. Offering cache-burst-mode support, this DRAM is closely coupled with the 40-MHz 68040. The board’s I/O subsystem handles data flow, letting the 68040 work without interruption.

A dedicated 68020 processor, combined with up to 4 Mbytes of I/O memory, forms the core of the 68-41’s I/O subsystem. Working with the gateway controller and datapath ASICs, the 68020 initiates DMA-type movements that handle data flow between the 68040 and I/O areas. This eliminates I/O bottlenecks and allows maximum data throughput. An intelligent SCSI containing an internal SCSI processor, on-chip 32-byte FIFO, a built-in DMA controller and SCSI-2 capability is part of this subsystem.

Besides SCSI, the 68-41 also provides additional external interfaces to communicate with the outside world through both serial I/O and a high-performance Ethernet interface. Serial I/O on the card moves through four RS-232C/422/485 serial ports. These may be configured for either synchronous or asynchronous operation. Additional I/O support is available through the board’s 32-bit interface, letting users add standard or custom modules depending on their requirements.

The on-board Ethernet interface is built around an Advanced Micro Devices 79C900. It provides LAN support and includes an on-chip 48-byte FIFO and a 32-bit DMA controller. The interface also provides advanced buffer management and is compatible with both Ethernet 2.0 and IEEE-802.3 10Base5 specifications.

To allow maximum data throughput along user-selectable data paths, the board features two high-performance bus interfaces. First is a 32-bit VMEbus, implemented by the VIC068 interface with the aid of a 40-Mbyte/s DMA controller. The other bus interface is the 32-bit VME subsystem bus (VSB), which offloads the data traffic from the main VMEbus. The VSB has a complete 32-bit multimaster interface plus its own DMA controller. The 68-41 is priced starting at $6,995.

—Jeff Child

Radstone Technology
20 Craig Rd
Montvale, NJ 07645
(800) 386-2738
Circle 360
New DR11W Enhancements Solve VMEbus Interface Problems...

The new DR11W-A from VMIC is an enhanced version of our standard DR11W VMEbus interface which has been a standard product for over 5 years.

Our DR11W interface family is the most mature DR11W compatible product line in the VMEbus industry with hundreds of installations throughout the world. This installed base means that VMIC customers are assured a trouble free systems integration effort. This lowers your risk and virtually guarantees a highly reliable and maintenance free operation. This fact alone solves a big problem. Now look at the high performance features of VMIC's new and enhanced DR11W-A that will solve the rest of your problems:

- Two Year Warranty
- 24 Hour Customer Service Hotline
- 32-Bit Addressing
- 32-Bit VMEbus Data Transfers
- Watchdog Timers Prevent Transfer Lock-out on VMEbus and Cables
- Byte & Word Swapping
- Provides Data Loopback Tests Through Cable on Single Board
- Provides Interface from VMEbus to DEC, Concurrent/Masscomp, Prime, Sun Micro-systems, Alliant, Data General, Harris Night Hawk, IBM PC/AT, Motorola Delta Series, Silicon Graphics, and other VMEbus-based host processors
- Provides Interface with High Resolution Graphic Terminals such as Raster Technologies, Megatek, Chromatics and others.

Now Available for Immediate Shipment and Backed by a 100% Satisfaction Guarantee. Call Our TOLL-FREE Hotline Today!

- Front Panel Fail LED
- Supports Off-Line Built-In-Test Plus Single Board Loopback Testing (with Test Cable)
- Meets VMEbus Spec. C.1 - Compatible Address Pipelining
- Fully Programmable Operation (Includes Selection of 16/32 Bit Transfer, Burst Mode, etc.)
- Fully Programmable Interrupt Levels and Vectors
- Software Compatible with VMIC's DR11W and DR11W-485 Boards
- Two VMIVME-DR11W-As form VMEbus-to-VMEbus Link
- Unix System V.3 Driver available

CALL NOW TOLL-FREE:

1-800-322-3616

VMIC

VME MICROSYSTEMS INTERNATIONAL CORPORATION

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
(205)880-0444 FAX(205)882-0859

VMIC products are internationally represented by Distributors throughout the world. Call or FAX VMIC for complete information.

CIRCLE NO. 69
Wind River Systems has announced a greatly extended version of the VxWorks real-time development and run-time system. Offering a completely rewritten kernel, enhanced connectivity, debugging and X Window System support, VxWorks 5.0 supports the 680X0 family of processors, the Sparc architecture and the 80960, and runs on a wide variety of Unix and VMS host platforms.

The rewrite of the Wind River kernel has resulted in greatly reduced latency and context switch times, according to the company. The interrupt lock/unlock sequence, for instance, formerly 10 to 15 µs, has been reduced to 2 to 3 µs. In addition, context switching has been optimized for a constant time, regardless of the number of tasks.

Enhanced floating-point emulation has been added to the kernel. In addition to run-time libraries that support software emulation of floating-point operations in systems without math coprocessors, VxWorks supports floating-point processor functions. Floating-point registers are saved as part of a task's context. This support is optional.

Enhanced communication

Intertask communication in the kernel has been enriched by adding two more types of semaphores: counting and priority-inheritance semaphores. Counting semaphores are like basic binary semaphores except that they keep track of how many times a semaphore is given. This makes them useful for guarding resources with multiple copies.

Priority-inheritance semaphores eliminate situations in which a high-priority task block is waiting for a semaphore held by a lower-priority task. The higher-priority task could wait an indeterminate amount of time while the lower-priority task is preempted by other tasks. Priority inheritance lets a task temporarily inherit the highest priority of tasks waiting for its semaphore.

VxWorks has traditionally included integrated networking. The new version includes the latest Tahoe release 4.0 of 4.3 BSD Unix Transmission Control Protocol/Internet Protocol for Ethernet. In addition, VxWorks 5.0 supports network connections between CPUs on a backplane and the serial line interface protocol.

In terms of higher-level communications protocols, VxWorks 5.0 has upgraded its remote procedure calls (RPC) to version 4.0. RPC allows Unix or VxWorks processes to invoke procedures executed on remote CPUs on the network. The addition of the ftp file protocol allows two-way access of VxWorks processes to Unix files, and remote Unix or VxWorks access to VxWorks files.

Various options available

New compiler and debugger options are also available. VxWorks 5.0 now supports the GNU C compiler, called gcc, distributed by the Free Software Foundation (Cambridge, MA). The code produced by the compiler is so compact that all VxWorks system source code (except for host executables) is compiled with gcc. The native compilers of host systems will still be supported. VxGDB, a new source-level debugger, is also offered. And finally, Wind River offers an optional support package for X Windows, version 11, called windX. WindX lets real-time processes open windows for input and output and display graphics that can be used to design graphical user interfaces for real-time systems.

The price for a single-user development license is $19,000, which includes the VxGDB debugger. The windX X Window System client-side developer's kit option is priced at $5,000.

—Tom Williams
Now! Up to 120,000 usable gates in a three-layer metal array.

Toshiba's 1-micron CMOS gate arrays provide the capability for a whole system-on-a-chip with gate delays of 0.4 ns.

Toshiba's TC150G series of 1.0 micron CMOS gate arrays pack up to 120,000 usable gates on a 172K master. The series uses our proven architecture combined with triple-layer wiring technology that makes highly efficient use of silicon.

The TC150G series is supported by a compatible library of more than 900 macrocells and over 150 macrofunctions. Our design environment covers the full CAD tool spectrum which includes high-level description language; design capture; design simulation; synthesis/design optimization ... and more! The Toshiba design environment is compatible with all major EWS including AIDA, Cadence, Dazix, HP, IKOS, Mentor, Synopsys, VALID, Verilog and Viewlogic.

Where design economy is a priority, Toshiba offers high pin-count plastic flat packs as a surface mount alternative to PGAs for many applications.

The series is available in 14 master array sizes ranging from 1,400 usable gates to 120,000, or up to 40,000 in plastic. And, you can depend on Toshiba to meet virtually any production quantity your business demands.

<table>
<thead>
<tr>
<th>SERIES</th>
<th>2-LAYER METAL</th>
<th>3-LAYER METAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC140G</td>
<td>2,300 TO 172,000</td>
<td>2,300 TO 172,000</td>
</tr>
<tr>
<td>TC150G</td>
<td>1,400 TO 120,000</td>
<td>1,400 TO 120,000</td>
</tr>
<tr>
<td>GATES</td>
<td>1,000 TO 68,000</td>
<td>1,400 TO 120,000</td>
</tr>
<tr>
<td>GATE LENGTH</td>
<td>1.0µm (drawn)</td>
<td>1.0µm (drawn)</td>
</tr>
<tr>
<td>GATE SPEED</td>
<td>0.4 ns</td>
<td>0.4 ns</td>
</tr>
<tr>
<td>OUTPUT DRIVE</td>
<td>up to 24 ma.</td>
<td>up to 24 ma.</td>
</tr>
<tr>
<td>PART NUMBERS</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>SECOND SOURCE</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>AVAILABILITY</td>
<td>NOW</td>
<td>NOW</td>
</tr>
</tbody>
</table>

There are five Toshiba design centers around the U.S. and one in Ottawa, Canada to help you. For technical literature, call 1-800-888-0848, extension 517 today. Service is our key component.

In Touch with Tomorrow

TOSHIBA

© 1990 Toshiba America Electronic Components, Inc.
New version of Abel tailored to device-independent, top-down design

Abel-4, the latest version of Data I/O's Abel Design Software, brings a host of features to designers of field-programmable gate arrays (FPGAs) and programmable logic devices (PLDs). The software is a major departure from previous versions because of the addition of Abel-HDL, a new hardware description language that lets designs be entered and verified with little or no concern for the target device architecture.

"We're answering the needs of the customer who wants the freedom to classes of programmable devices. Designers can, therefore, choose the detail level required for the application. Abel-HDL also supports a variety of behavioral input methods including high-level equations, state diagrams and truth tables.

The Abel-4 package contains an integrated design environment that features a windows-based interactive user interface, enhanced FPGA device support, intelligent device selection, and the first generic fitters for the recently announced Open-dialogue box or keyword), as well as an auto-update capability that tracks the design and processes only the necessary portions. All messages and error notifications are interactively reported, and all interface features can be accessed either through windows, or from the command line.

SmartPart, an intelligent device-selection capability, automatically generates a list of candidate devices for every design (from a database containing over 6,000 parts) by comparing requirements with device resources. Without any changes, designs can then be tried in multiple device architectures to achieve full optimization. User-definable criteria include device technology, speed, manufacturer and price, all of which can be prioritized according to design requirements. Fields can therefore be set to determine company-specific parameters such as "in stock" or "company qualified."

Simulation before selection

The tool can also perform design- and device-level simulation before device selection—another departure from previous versions. The simulation provides multiple forms of feedback including tabular and waveform formats. Device-level simulation allows full verification before programming and verifies that the design properly fits into the targeted device. This includes full debugging of every fuse, node and pin.

Abel-4 contains four fitters: one for traditional programmable logic and field-programmable logic architectures (this supports 150 device architectures); one for the Altera EP1800; one for the Altera MAX 5032 and 5016; and one for the Cypress programmable sequencers 330, 331 and 332. Data I/O and device vendors will add more device fitters in the future.

Abel-4 is available now and is priced at $1,995 for the MS-DOS version. The software is also available for Sun-3 and Sparcstation at $2,695, and for VAX/VMS workstations at $4,115.

—Mike Donlin
Discover the quality voice processing products, superior service, and unparalleled distribution system of InnoVoice.

Innovative voice processing I/O boards from InnoVoice utilize our patented compression technology. The boards provide high quality voice/music capture and reproduction at low bit rates, giving you the building blocks to develop high performance systems at competitive system costs.

Innovative, Quality Products

**OctaLink™**
- 8 Channel Single Slot Voice I/O board;
- Unique architecture and flexible interface board provide improved functionality and efficient slot utilization;
- Supports industry-standard software;
- Applications include Interactive Voice Response, Voice Mail/Messaging and Automated Attendant.

**StereoLink™**
- 2 Channel Stereo Card;
- High quality voice/music for PC based multi-media presentations;
- Selectable storage rates provide sound quality from AM to near CD levels using only a fraction of conventional CD memory.

**SpeechLink™**
- 1 Channel Voice Card;
- Applications include Voice over E-mail, Digital Dictation and Annotation of Complex Graphics or Text.

Nationwide Service and Support

InnoVoice provides pre-sales support, applications and engineering assistance, and post-sales support. We back all this up with the best warranty in the industry, three full years! In addition to serving our customers via our 800 telephone service, all InnoVoice products are now available through a major electronics distributor, at no additional cost! With offices in over 60 locations throughout the U.S. and Canada, we'll get you what you need, when you need it.

Our mission is to provide total customer satisfaction. We believe that by being responsive to your needs, we can provide better products, better service and better delivery than anyone else.

Call InnoVoice today. Let us show you what "A New Perspective in Voice Processing" can mean to your bottom line.

"Innovative Voice Solutions"
10700 Parkridge Boulevard
Reston, Virginia 22091
800-347-6007

© 1990 Extrema Systems International Corporation
A division of Extrema Systems International Corporation
CIRCLE NO. 71
Open simulation system eases design of mixed-signal ASICs and ICs

A new mixed-signal simulation system from the Analog Division of Cadence Design Systems, the Analog Artist, is tightly tied into a front-to-back-end toolset. Mixed-signal designers can access design-entry, simulation, physical-design and verification tools through the Analog Artist design system, which is integrated within the Cadence Design Framework architecture. Customers who prefer an alternate simulator can use an open simulation socket to integrate additional tools within the environment.

The new mixed-signal tool combines the simulation cores of Verilog-XL and Cadence-Spice. A schematic-entry system supports Verilog and Cadence-Spice primitives, as well as Verilog behavioral models. The system highlights analog and digital partitioning, with visual feedback on the schematic of actual simulation configuration. There are no constraints on mixing analog and digital blocks in a hierarchy. Users can switch the level of a block model for critical-path simulation. Netlists for Verilog and Cadence-Spice are automatically generated.

Design simplified

A mixed analog/digital display system lets users view analog and digital waveforms in the same window and displays them on the same horizontal strip plots. It also displays full transient, parametric and statistical analog waveforms.

To ease both top-down and bottom-up design, the multilevel mixed-signal simulator lets users model each section of the design at the optimum level of detail. Users can simulate logic designs from stochastic, architectural, gate, switch and RTL levels through Verilog-XL and circuits through Cadence-Spice for all combinations of mixed-signal designs and processes.

Cadence-Spice supports the use of high-level macromodels as well as transistor models. When systems-level libraries become available, the Analog Artist Mixed-Signal Simulator will be able to do analog and digital systems design.

Interactive simulation control lets mixed-signal designers stop, interactively probe a schematic and continue without needing restart the simulation. Simulation results can be back-annotated directly to the schematic. Users can manipulate simulation outputs to create new variables through a video keypad and a calculator.

Although the database of the Analog Artist Mixed-Signal Simulator can handle 1 million or more transistors, the present release of Cadence-Spice has a computational limit of about 2,500 devices. With circuits larger than that, designers will encounter excessive simulation run times, or may suffer convergence difficulties.

The Analog Artist Mixed-Signal Simulation Interface is priced at $10,000 per license and requires the Analog Artist Design System (which includes Cadence-Spice), starting at $30,000 per seat, and the Verilog simulator at $25,000 per seat. The Analog Artist supports Sun, Apollo and DEC workstations.

—Barbara Tuck

THE ANALOG ARTIST

Trademark Information

UNIX is a registered trademark of AT&T Bell Laboratories.
PAL is a registered trademark of Advanced Micro Devices, Inc.
SMART-POWER is a registered trademark of Nartron Corp.
CDA and BurstRAM are trademarks of Motorola Inc.
If OEM sales are part of your business, Systems/USA is THE place to be.

Systems/USA is the OEM computer technology exposition for systems design and integration—the only show dedicated to the OEM computer technology market.

Systems/USA is the place to showcase products and expand OEM business, or find the solutions to systems design and integration requirements.

- **Technology Conference** will consist of a “hands-on” forum of nine separate tracks spanning three full days addressing these important categories:
  - High-Performance ICs
  - Power Sources
  - Input Technology
  - Buses & Boards
  - Output Technology
  - Government Defense
  - Software Development
  - Display Technology
  - Storage Technology

- **Exhibits** will coincide directly with the topics being addressed within the technology program.

- **New Product Announcements** will be a key feature of the show, providing exhibiting companies the opportunity to showcase their products and meet one-on-one with interested parties.

- **Management Issues Conference** will focus on business developments within the systems integration industry as told by the industry’s leaders.

**Systems/USA Conference & Exposition**

SYSTEMS/USA-West

February 11-13, 1991
Anaheim Convention Center
Anaheim, California

For simple solutions to complex problems... Systems/USA

For FREE registration and more information, call (800) 873-1177 ext. 300.

Sponsored by the

American Electronics Association

5201 Great America Parkway, Santa Clara, CA 95054

CIRCLE NO. 72
C&T, Opti develop low-cost cache solutions for 386 chip sets

The expanding market demand in the PC arena is pulling cache technology not just onto PC motherboards, but into chip sets as well. For some time, Chips and Technologies has offered its high-end Peak chip set with a built-in two-way set-associative cache controller. But most cache solutions have depended on either proprietary controllers designed by the systems vendor or on separate controller ICs.

Now, in conjunction with its announcement of a 33-MHz version of the original Peak chip set, Chips has also unveiled a new version of the three-chip high-end product. The Peak/DM is essentially identical to the 33-MHz Peak set and includes all the usual modern chip set features: 128-Mbyte memory space, 4-Mbit DRAM support and so forth. But as the name suggests, the new set uses a direct-mapped, rather than a two-way set-associative, cache controller.

Chips is exploiting this fact to take a bit of the cost out of the chip set. The simpler circuitry of the DM permits the company to offer the set for $153 (1,000s) for the 33-MHz parts, compared to $189 (1,000s) for the full Peak set at the same speed. Production volumes for both sets are expected this month.

Expanding the market downward

Meanwhile, Opti, a young Chips spin-off, is aiming even lower with its latest product. Opti has gained some fame by selling single-chip AT bus 486 and 386 DX solutions with on-board cache control. Now the company is introducing the first single-chip 386 SX parts with integral cache control.

“So far, vendors have just been gluing a 16-bit interface onto their existing page-interleave DX chip set and calling it an SX product,” says Opti vice-president of marketing and sales Raj Jaswa. “We took it as a challenge to come up with a product specifically engineered for the SX and able to compete against both page-interleave and cache-based sets at a reasonable cost.”

Except for the single-chip partitioning, the Opti sets have many features in common with the Peak/DM—not surprising, since many of the Opti founders were involved in the design of previous Chips products. The new chips, for example, support 4-Mbit DRAMs.

The essence of Opti’s strategy in the excruciatingly cost-competitive SX market is to find a set of memory architecture compromises that will beat existing page-interleave chips on cost/performance. This is a trick, since the Opti sets must bear the added cost of cache SRAMs.

Opti’s solution is a pair of single-chip parts with direct-map cache controllers. The high-end part, the 82C281, supports caches up to 128 kbytes and has a write buffer to slightly improve overall memory performance. This device is priced at $35 (10,000s). This should yield a system cost, after adding a peripheral controller, cache and tag SRAMs and TTL buffers, lower than that of a standard SX chip set with an external cache controller.

The low-end chip, the 82C282, leaves out the write buffer but is otherwise identical. Priced at $24.50 (10,000s), the part is intended to give system performance much better than that of page-interleaved systems, but at a very comparable system cost. Volume shipments for both sets should begin this month.

—Ron Wilson

Chips and Technologies
3050 Zanker Rd
San Jose, CA 95134
(408) 434-0600
Circle 353

Opti
2700 Augustine Dr, #165
Santa Clara, CA 95054
(408) 980-8178
Circle 354
What's the best kept secret in the VME industry?

The Calmos VME chipset from Newbridge Microsystems.

The Calmos™ VME chipset has been in military and commercial production for over two years. With full compliance to industry standards, it provides high performance and flexibility for the future through a pin-for-pin compatible migration path to VME-64.

This unique VME chipset offers a versatile, complete solution. It can be used as a two chip set for a full VMEBus interface or as a single chip with external address and data bypass.

Complete compatibility with the IEEE 1014/VMEBus Rev C Interface ensures that all VMEBus signals are terminated, and all VMEBus Recommendations and Functional Modules, including master/slave interface, are implemented. The Calmos VME chipset also supports all cycle types and addressing modes.

The powerful Local Bus Interface provides compatibility with the industry standard 68020/030 protocol, and includes a 3 source Arbiter/Requester, Interrupt Controller (local and VMEBus), and Watchdog, Tick and Baud Rate Timers.

In addition, the Calmos VME chipset features BiMode Bus Isolation mode for system fault isolation, Auto ID and Auto SYSCON for jumper free design, plus 32 location monitors.

Part of the Newbridge Microsystems complete open bus product line extending all the way to Futurebus+, the Calmos VME chipset delivers the features you need today to build high-performance systems now and in the future!
Controller expands palette for color LCDs

Now that the first laptop-sized color LCDs are moving out of the research lab and into the hands of OEMs, designers are starting to look around for color LCD controller chips. And after they wire up a controller, the designers are discovering a limitation of the new displays: most existing panels have a repertoire of only eight colors. Even the latest active-matrix displays only manage 512 colors—enough for business applications, but inadequate for image-rendering or multimedia applications.

Enter Cirrus Logic, the folks who brought you 64-shade gray scale on a supposedly two-tone monochrome display. With its new CL-GD6340 LCD interface controller, the company offers a palette of several thousand discernible colors on existing LCD panels.

The chip goes between a conventional VGA controller chip and a color panel, essentially replacing the RAMDAC that would be there in a CRT-based system. Taking in the red, green, blue and sync signals from the VGA, the chip produces the unique vertical and horizontal clocks and pixel values needed by the panel. The 6340 also provides the power sequencing necessary to power up, power down and idle the panel without frying it—a delicate business with the active-matrix displays.

But the chip's real claim to fame is its color rendering—the ability to offer users 256 colors from a several-thousand-color palette in VGA mode 13. Three different techniques are used in combination to create the colors, according to Cirrus product marketing manager Mark Singer.

"The techniques are similar to what we do for gray scale on monochrome displays," Singer says. "But the active-matrix panels are much faster—everything is more critical." First, Singer says, the controller manipulates the duty cycle of the cells on the panel to obtain variations in apparent brightness. Second, as the pixels are flashing off and on, the controller can change the colors to create the appearance of different hues.

The third technique takes advantage of the fact that in VGA mode 13, each logical pixel comprises four physical pixels. So the controller can create stipple patterns—different colors in adjacent pixels of the four-pixel group—to achieve additional effects. The chip combines the techniques in a proprietary algorithm that's entirely transparent to the display software—the hardware just looks like a RAMDAC with a very large color palette.

The new chip will be sampled in the fourth quarter in a 100-pin quad flat pack. Sample price will be $68 each (100s).

—Ron Wilson

Cirrus Logic
1463 Centre Pointe Dr
Milpitas, CA 95035
(408) 945-8300
Circle 355
If you haven't registered to attend Surface Mount '90 in Boston, it's time. There are only a few weeks left to register for the leading surface mount exposition and conference with over 30 outstanding technical sessions and over 300 exhibit booths.

Call 800-223-7126 or 617-232-3976 today

We'll send you a complete show and conference preview or, if you call before August 17, we'll register you right over the phone.

Time is running out...
If you're serious about surface mount, it's time to register for Surface Mount '90.

Surface Mount '90 is the only surface mount exposition and conference co-owned and produced by the Surface Mount Technology Association (SMTA) and Miller Freeman Expositions.
In the nether reaches of high-precision radio-secure-channel communications, radar receivers and radio test instrumentation—digital techniques are gradually displacing analog circuitry. Already the relatively slow operations such as signal detection, windowing and spectral analysis have migrated into programmable digital signal processors or into dedicated fast Fourier transform chips, convolvers or whatever. Decimation in time and signal filtering functions have been taken over by digital filter chips. Now Plessey Semiconductors is offering another step in the process: a combination of phase accumulator, digital synthesizer and in-phase/quadrature (I/Q) splitting circuitry in a single package.

Running at sine/cosine synthesis speeds as fast as 20 Msamples/s and with resolution of .001 Hz, the PDSP16350 permits well-funded developers of precision digital receivers to go directly from digitized intermediate frequency to digital I and Q components ready for filtering and message extraction. The PDSP16350 starts out with a 34-bit phase accumulator, which drives a cordic processor. The processor generates sine and cosine waveforms with 16-bit resolution. The digital waveforms are, in turn, fed to a pair of 16-bit multipliers where the sine and cosine components can be applied to an incoming signal. The resulting pair of product waveforms is then fed to the chip outputs.

There's sufficient flexibility built into the part to permit its use in AM, FM or PM environments, according to Plessey. It can serve as a signal generator, modulator or demodulator. Combined with other Plessey DSP building blocks such as dual FIR filters, FFT and Pythagorean processors, or convolvers, it can form the basis of a very compact high-resolution digital radio system. The CMOS PDSP16350 comes in a single in-package, dual-FM or PM environments, according to Plessey. It can serve as a signal generator, modulator or demodulator. Combined with other Plessey DSP building blocks such as dual FIR filters, FFT and Pythagorean processors, or convolvers, it can form the basis of a very compact high-resolution digital radio system. The CMOS PDSP16350 comes in an 84-pin pin grid array package and is available in production quantities for $395 each (1,000s). A 132-pin ceramic quad flat pack version will be available in the fourth quarter.
THE ROAD TO INNOVATIVE SOLUTIONS

BUSCON/90-EAST™
OCTOBER 16-18, 1990
ROYAL PLAZA TRADE CENTER
MARLBOROUGH, MASSACHUSETTS

FOR MORE INFORMATION CALL (800) 243-3238
IN CONNECTICUT CALL (203) 852-0500

CIRCLE NO. 78
VME64™ from Performance Technologies—The only Bus designed for the Autobahn

In 1989 Performance Technologies introduced VME64 and established a new standard for high speed VMEbus performance. Products based on this standard, which is now included in the VMEbus Rev D spec, are in-stock NOW at Performance Technologies.

Model PT-VME240 DRAM memory. The fastest memory configuration available for the VMEbus. Transfer rates to 48 MBytes/sec. (32 bit) and 96 MBytes/sec. (VME64) rates.

Model PT-VME940 VME Crate-to-Crate networking. Transfer rates to 30 MBytes/sec. between VME chassis and up to 60 MBytes/sec. on VME.

Model PT-VME140 Single Board 68030 CPU. The first product using the PT-VMSI VME64 bus interface ASICs.

For detailed specifications Call: (716) 586-6727 Fax: (716) 586-6707

The BUS Stops Here for innovative VMEbus solutions

Performance Technologies Incorporated
435 W. Commercial St.
E. Rochester, NY 14445 U.S.A.

*Using the PT-VME240 memory VME64 is a trademark of Performance Technologies, Inc.

NEW PRODUCT HIGHLIGHTS

INTEGRATED CIRCUITS

RAMDAC supports multiple windows with different color maps

A new true-color window RAMDAC allows applications with different color map requirements to run in multiple windows on one screen. Normally, the color map information loaded in a RAMDAC's lookup tables determines the color map for the entire display screen. But high-performance workstations often need to display a 24-bit true color imaging applications in one window, for example, while at the same time running another window with only 16 colors, or with 256 colors.

To address this problem, Brooktree has announced the Bt463 CMOS window RAMDAC. The Bt463 is designed for high-performance graphics workstations and requires a 32-bit-deep frame buffer. The basic pixel word size is 28 bits, with 24 bits for color information (up to 8 bits each for red, green and blue) and 4 bits for graphic overlay. In addition, each word contains a 4-bit window-type field that's the key to changing color maps on a window-by-window basis.

The Bt463 has three 528 x 8-bit color lookup tables each for red, green and blue. But these lookup tables can be partitioned to contain up to 16 different color maps, depending on the size of color map selected. The 4-bit window-type field that comes in with the pixel word determines which color map the pixel data accesses.

The window-type field in the pixel word addresses a 16 x 24-bit RAM array, called the window-type table, so at any one time one could theoretically have 16 (4 bits of address) types of windows. Each 24-bit window-type word in the array is divided into seven fields that determine the attributes of the window. If only 4-bit color planes (12 bits of color) are to be used, for instance, the upper 4 bits of color data in each plane can be moved down in the word via the shift field, and the rest of the pixel can be discarded. Another field specifies the number of active planes for pixel data, and another the location of overlay data, which can be anywhere in the 24-bit pixel word. And the start-address field specifies the beginning of the physical address of each individual color map within the 528 x 8-bit lookup table.

Applications request color maps in the lookup tables on initialization. They also assign window-type words to the window-type array. Then they include the 4-bit address of their type word with the pixel data they store in the frame buffer. As each pixel comes in, its color map is automatically selected based on the window-type information that's associated with it. So color maps are actually selected on a pixel-by-pixel basis. As users size a window, they merely change the boundaries of frame buffer addresses where the pixel data for that window's application is stored; there's no need to change any value in the RAMDAC.

The Bt463 will be available in three speed versions: 110, 135 and 170 MHz. It comes in a 169-pin PGA package. Availability is scheduled for fourth quarter of 1990. Pricing for the 135-MHz part is projected to be $317 (100s).

—Tom Williams

Brooktree
9950 Barnes Canyon Rd
San Diego, CA 92121
(619) 452-7680

Circle 357
The Best Collection of Peripherals Ever Assembled Have Joined The ICC World Tour

Invitational Computer Conferences (ICC) collects the world’s best suppliers for an event you won’t want to miss. At a nearby location, you’ll see the latest in technology exclusively for computer peripherals.

See what today’s products offer through hands-on demonstrations...learn what tomorrow’s products will be. Attend technology seminars that give you expert answers to your peripherals questions. Take part in panel discussions and debates on current technology and business issues. Explore all your options so you can make your peripherals decisions.

Make plans now to attend. Watch for your invitation or call for additional facts and details on how you can receive an invitation.

For almost two decades, the ICCs have specialized in bringing the latest computer technologies to you, for your evaluation.

With the research expertise from our parent company, Dataquest, we have the support of the world’s leading computer analysts at each stop on the ICC tour.

Call for your OEM Peripherals invitation, Dataquest/ICC, U.S. TEL: (714)957-0171, FAX: (714)957-0903 EUROPE/UK TEL: (0895)835050, FAX: (0895)835260/1/2

CIRCLE NO. 80
**Positions Wanted Ads**

Free 1" ad to subscribers seeking full-time employment. Just include 50 words of copy and your subscription label. We'll run your ad in 2 consecutive issues.

Available to non-subscribers or consultants/companies at $125 per column inch. Mail your position wanted ad to:

**Computer Design**

**The First Magazine of System Design, Development and Integration**

Positions Wanted
One Technology Park Dr
PO Box 990
Westford, MA 01886

---


**Senior Mechanical Design Engineer**. 20+ years systems, mechanism and component design, including 7+ years technical manager. Computer to medical diagnostics packaging. Injection molding to die casting to machined components and sheet metal. Permanent or temporary. Will travel or relocate. Vick Vickroy (209) 832-0255 P.O. Box 1929, Tracy, CA 95378.


**Senior Hardware/Software Systems Engineer/Integrator**. 25 years experience. MSE in SysEng & CS. BSEE. Proposal development, system simulation/studies, R&D, requirements, design, test, training, support, and maintenance along with system/software development methodologies and standards. David Roggendorff, 2601 Evergreen, Huntsville, AL 35801-2816 or 205-539-0055 for resume.

**Data Communications Expert**—7 years experience. Field service, technical support and management experience. Stat muxes, protocol converters, interfaces, standards, LANs, PCs, modems, T1, TDMs, switched 56, DDS, CSUs. Interested in Portland/Vancouver, WA area. Possible Field Service Mgr., Technical Support, Product Management. Call (503) 981-1302 for resume/references.

**Senior Hardware/Software Systems Engineer**. 20 years experience. Analog & Logic design, systems integration. Self test. Automatic test equipment. ATP's, TRD's, FME's. Software documentation. Basic, 8086, 8085, Assembler, and C. Programmable controllers. Design of interface fixtures, power supplies. Full time or full contract. Willing to relocate. Resume on request. 22 Bellvidere Ave., Jersey City, NJ 07304; (201) 434-8604.

---

**Purchasing/Materials Management Director.** Twelve+ years experience in close cooperation with MIS, Engineering, and Design personnel in effecting cost savings in the procurement of high technology systems and components. QA and VA given top priority. R. Coughlin, 120 Dorset Dr., Buffalo, NY 14223.

**BSEE MBA/Entrepreneur** seeks to fully use my talents in a growing company covering product development, production, marketing, service or sales. Commercial ship control systems, telephone, and electronics background. Contact: Harry P.O. Box 675, Nutley, NJ 07110; (201) 667-1329.
SYSTEM SHOWCASE

Reach over 100,000 qualified engineers and engineering managers with System Showcase advertising. Rates start at $765. For more information call Sue Nawoichik at (800) 225-0556 or (508) 392-2194.

COLOR, GRAY SCALE & BINARY IMAGE COMPRESSION

OITIPAC is an extremely flexible image compression system providing both lossless and controlled quality modes. It is currently implemented as an add-in card for PC/AT compatibles and also as a software only version for DOS.

STANDARDS: JPEG (ANSI X3L2.8) for color & gray scale images and CCITT Group 3 and 4 binary images.

SPEED: the new OPTIPAC-ISA Model B can compress/decompress full screen images in less than a second.

Optivision, Inc.
1-800-552-8934
Davis, CA
Fax: (916) 756-1309

8051 SUPERMARKET

Complete line of 25 single board computers. Fully supports over 100 variants of 8051 micro-controller family, including 537, 532, 751, 732, 492, 451, 535, DS5000 and many more. Available software includes 8052 BASIC, BASIC compiler, FRANKLIN C, and 8051 assembler. Six Footprints ranging from 1" x 4" to PC/AT long slot. Expansion bus with simultaneous multi-channel communications. Optional floating-point. Boards may be stacked or backplane mounted. Custom/CAD service at reasonable rates. Quick turn on 8051-based designs.

MODULAR MICRO CONTROLS
109 S. Water St. Northfield, MN 55057
Phone (507) 645-8315
Fax (507) 645-4342

CIRCLE NO. 177

CIRCLE NO. 178

X.25
SDLC
QLLC
HDLC
ADCCP
PAD

• C source code
• ROM-able
• Full porting provided
• No OS required

GCOM, Inc.
41 E. University
Champaign IL 61820
(217) 352-4266

Specialists in Computer Communications
FAX 217-352-2215

CIRCLE NO. 180

CIRCLE NO. 181

RAM CARD APPLICATIONS

MS-DOS compatible, serial and parallel RAM CARDRIVE. Installable software drivers and format programs to make a RAM card "look like" an MS-DOS formatted drive. Compatible with XT, AT, PS/2, Zenith, Compaq and others.

PAMCO ELECTRONICS INC.
377 Carowinds Blvd.
Fort Mill, SC 29715
1-800-255-6265
(803) 548-6740

CIRCLE NO. 182

CIRCLE NO. 183

CIRCLE NO. 184

COMPUTER DESIGN SEPTEMBER 1, 1990 141
Stop Blasting ROMs

PROMCEO emulates 8 bit ROMs from 2716-27450, or 16-bit ROMs 27C1024 or 2CC404. (require emulating other ROMs. Non-JEDEC ROMs require custom cable.) Sophisticated LoadICE™ Host Software downloads, uploads and edits ROM contents, supports MS-DOS, UNIX, MAC & VMS. Software sources are included. **Bi-directional Serial link, abandons to 57600 bauds 1 sec in 2 sec**. **Bi-directional Parallels port (option)-loads 1 Mbit in 4 sec**. Emulate up to 2 ROMs per unit, daisy-chain up to 256 ROMs from one port! **New! Analysis Interface** (option) implements a ROM-based UART for sophisticated debugging.

Free Demo Disk of OrCAD
PC Board Layout Tools
OrCAD, makers of the world's best known schematic capture product, offers OrCAD/PCB II. This affordable package includes everything needed for laying out printed circuit boards as big as 32" x 32" and 16 levels deep. $1495 buys utilities, printer/ploter drivers, autorouting abilities, optimization and much more. Call OrCAD at (503) 690-9881.

CIRCLE NO. 185

IT'S IN THE CARDS ...
More Leads, More Action, More Sales

Our readers are proven buyers of:
- Computer Systems
- Systems Boards
- Integrated Circuits
- Design Development Equipment
- Memory Storage Equipment
- Software
- Terminal Input-Output Equipment
- Communications Equipment
- Components
- Test Equipment

Smart buyers depend on COMPUTER DESIGN DIRECT ACTION CARDS

Call Sue Nawoichik: at 800-225-0556 or 508-392-2194

CIRCLE NO. 188

Data I/O Programming Tools

50% OFF
280 Set Programmer plus PROMlink PC File Management Software just $995*

- Set/gang programming with the 8-socket 2808
- Supports E/EPROMs up to 512K
- Easy PC control with PROMlink™ software
- FREE: one-year Data I/O® warranty

Call now for a **FREE 15-day trial** with no obligation to purchase; **and receive a FREE tutorial on programming today's device technologies.**

1-800-247-5700

CIRCLE NO. 189

GENERATE QUALITY SALES LEADS WITH LOW COST ADVERTISING

System Showcase advertising generates leads without hurting your ad budget. For as little as $765.00 per insertion your advertising message reaches over 100,000 computer systems designers, developers and integrators — each a key decision maker responsible for purchasing your products. Just send a glossy photo and approximately 60 words of copy. We do the rest... at no production charge. If no photo, 100 words of copy accepted. Two and four color available at nominal charge.

CIRCLE NO. 190

ELECTRONIC DESIGN SERVICES

- Initial concept through prototype and production
- Design of advanced digital and analog electronics
- Approved programmable gate array design center
- Real - time embedded software - DSP code
- 7000 square foot facility with fully equipped labs
- 12 year track record of successful product designs
- Designs are warranted Defect Free Forever

CIRCLE NO. 192

CIRCLE NO. 193
**Low Cost Logic Simulator**

**DLsim™ Digital Logic Simulator**
- Event driven, nine state functional and timing simulation
- 16,000 gate capability without additional memory
- Direct support from JEDEC files for PLDs and GALs
- Compatible with HDL or IC/ICD schematics files
- Runs on IBM PC/XT/AT or compatible
- Interactive logic viewer (EGA/VGA or Hercules)
- Supports HP Laser or EPSON dot-matrix printers
- Includes TTL, ALS and CMOS libraries with source
- No copy protection
- Complete package only $495

CADSim Technologies
525 Melbourne Ct., Newbury Park, CA 91320
(805) 499-8653

**C for the 8051**

**Expanded with 1/0 and interrupt handling.**

Eratosthenes Sieve Program from BYTE (1/83)

Benchmark Results - Sample program:

Responsive engineers and engineering available for rent. 100,000 direct mail managers. Key decision makers, by name, product design, purchase influence or geographic areas. Proven winner for books, hardware, software, testing instruments and many other offers.

For more information call Deanna at PennWell Lists, Advanced Technology Group:
800-962-4669 or 918-831-9551

**C for the 8051 Compare:**

Benchmark Results—Sample program: Eratosthenes Sieve Program from BYTE (1/83), expanded with I/O and interrupt handling.

<table>
<thead>
<tr>
<th><strong>FRANKLIN SOFTWARE</strong></th>
<th><strong>Archimedes</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>C-51 v2.1</td>
<td>MCC51 v1.2</td>
</tr>
<tr>
<td></td>
<td>IOC51 v2.20A</td>
</tr>
</tbody>
</table>

- Linkage time 6 sec
- Execution time 0.88 sec
- Total code size 1720 bytes
- Compilation time 17 sec
- Sieve module size 541 bytes

CIRCLE NO. 200

**CIRCLE NO. 199**

**DOS IN EPROM**

FREE We'll include a free copy of the pocket-sized XT-XT Handbook by Chooser and Foster with each PromKit if you mention this ad when you order. Of course, the $9.95 value is also available by itself. Or buy five or more for only $5.00 each.

**CIRCLE NO. 198**

**CIRCLE NO. 197**

**CIRCLE NO. 195**

**Don't Get Gapped!**

High infrared current can destroy your sensitive VAX CPUs and peripherals in less than time it takes to flip a switch.

**THE SOLUTION?**

Power up with Z-LINE TPC 115-10 MTD™ the smallest power distribution and control system available. POWER UP WITH --- ---

Our proprietary Multiple Time Delay™ circuitry sequences your power-up to protect your systems from the spikes and surges, EMI & RFI, that destroy your hardware and erase your data. And our remote on/off and emergency shutdown gives the power control back to you.

All Puluzzi Engineering MTD™ controllers are compatible with DEC and UPS systems.

DON'T WAIT UNTIL IT HAPPENS, CALL TODAY!

PULZZI ENGINEERING, INC.
3260 S. Susan Street, Santa Ana, CA 92704-6665
(714) 540-4229 FAX (714) 641-9062

**CIRCLE NO. 196**

**DISTRIBUTOR INQUIRIES ARE WELCOME!**

ADVANCED DIGITAL MACHINES LTD.
550 Parkside Drive, Waterloo Ontario N2L 5V4, Canada Tel./Fax: (519) 888-6811

**CIRCLE NO. 194**

**TARGET COMPUTER DESIGN SUBSCRIBERS BY MAIL!**

COMPUTER DESIGN subscriber list available for rent! 100,000 direct mail responsive engineers and engineering managers. Key decision makers, by name, at business addresses. Target by job function, company type, design management, product design, purchase influence or geographic areas. Proven winner for books, subscriptions, technical reports, seminars, conferences, tools, components, catalogs, hardware, software, testing instruments and many other offers.

For more information call Deanna at PennWell Lists, Advanced Technology Group:
800-962-4669 or 918-831-9551

**C for the 8051**

**Compare:**

<table>
<thead>
<tr>
<th><strong>Franklin Software</strong></th>
<th><strong>Archimedes</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>C-51 v2.1</td>
<td>MCC51 v1.2</td>
</tr>
<tr>
<td></td>
<td>IOC51 v2.20A</td>
</tr>
</tbody>
</table>

- Linkage time 6 sec
- Execution time 0.88 sec
- Total code size 1720 bytes
- Compilation time 17 sec
- Sieve module size 541 bytes

Call now for your free DEMO disk.

**FRANKLIN SOFTWARE, INC.**

888 Saratoga Ave. #2 • San Jose, CA 95129
(408) 296-8051 • FAX (408) 296-8061

**Synopsis:**

- Multibus™ AT COMPATIBLE SBC

Multibus™ is now PCA/AT™ compatible with MAT-286 which includes all of the functions of a 10 MHz AT motherboard, plus 3 serial ports, a parallel port, two SBX interfaces, 10 28-pin EPROM sockets, and up to 4M of parity checked, dual ported DRAM. A daughter card, MATxSYS80, adds EGA, floppy, and SCSI interfaces.

**Single Board Solutions, Inc.**

20045 Stevens Creek Blvd., Cupertino, CA 95014
(408) 253-0250

Multibus™ Intel Corp. PCA/AT™ IBM

**CIRCLE NO. 200**

**CIRCLE NO. 197**

**Industrial Computers**

Pro-Log's line of STD Bus board level products are ideal for low power, high noise immunity and varying temperature range applications. Their reliable, high speed processing is ideal for use in manufacturing automation and industrial control. A variety of expansions and options enables the system to meet individual application specifications.

**Pro-Log Corporation**

800-538-9570

2555 Garden Road
Monterey, CA 93940

**CIRCLE NO. 176**

**COMPUTER DESIGN SEPTEMBER 1, 1990**

143
SBE...At the Core of WAN Interface Solutions

The SBE VCOM-4 Multiprotocol Communications Controller...today's high-performance, cost effective WAN interface. For price-performance in a single VMEbus communications controller, nothing equals the new SBE VCOM-4.

This exclusive SBE card features four full-duplex, independently programmable serial channels. Yet, it takes up only one VMEbus slot and provides twice the throughput of conventional boards. A complete implementation of X.25 is available ported to the VCOM-4, which speeds your product to market.

The result: an unmatched WAN interface for VME-based hosts, front-end processors, and data/voice networking systems, including:

- Two channels at T1 speeds.
- All four channels can operate with sustained throughput at speeds up to 768 Kbps, interfacing to fractional T1 services or 56/64 Kbps lines.
- Each communications channel can be independently configured to support HDLC, SDLC, Bisync, Async.

Turn to SBE and the VCOM-4 for the core of your VMEbus WAN product design application. For fast action, contact SBE, Inc., 2400 Bisso Lane, Concord, CA 94520, or call 1-800-347-C OMM.

CIRCLE NO. 81
You'll want to keep tabs on these.

To make that easier, we'll send you our new Data Book if you call the toll-free number below. You'll get 1344 pages of hard data on our high performance parts, support tools, quality programs, military programs, and packaging options. You'll get thorough descriptions of all our SRAMs, PROMs, EPLDs, FIFOs, LOGIC, SPARC Microprocessors, SRAM Modules, BiCMOS, and ECL parts.

An idea book for high performance designers, our 1990 Data Book can be yours for a fast, free call.

Data Book Hotline: 1-800-952-6300.*
Ask for Dept. C116.

*1-800-387-7599 in Canada, 020 2-672-2220 in Europe. ©1990 Cypress Semiconductor. 3901 North First Street, San Jose, CA 95134. Phone (408) 943-2600, Telex: 821032 CYPRESS SN J UD, TWX: 910-997-0753. MAX is a trademark of Altera Corporation.