Sharing design data through networking

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Why talk SCSI with Ciprico? To start with, we're the only vendor with a complete line of high-performance SCSI host bus adapters for Multibus® I, VMEbus, and Multibus II. Each board was designed to optimize performance with its system bus. And consider our experience. Ciprico has over 50,000 boards installed worldwide. Our design expertise provides you with the highest possible performance at the lowest possible price.

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In the time it takes other graphics engines to draw a few lines...

Texas Instruments TMS 34010 (2%)

AMD Am95C60 (17%)

Hitachi HD63484 (20%)

Intel 82786 (25%)

GeoCad perspective drawing courtesy of Rudolph Horowitz and Associates, Architects.
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Sparc wins and loses

Although endorsements for the popular Sparc RISC chip from Sun Microsystems (Mountain View, CA) continue to be announced, the chip may also be about to lose some significant support.

Rumors are circulating that AT&T (Morristown, NJ) is reconsidering its earlier commitment to Sparc and will turn instead to Motorola's 88000 as its core processor for future Unix System V-based computers. The Sun/AT&T agreement, signed last January, created a furor among Unix licensees that eventually resulted in the formation of the Open Software Foundation (OSF). Apparently, the agreement was also viewed within AT&T as a threat to the company's longstanding relationship with Motorola. AT&T uses Motorola's 68000 family of processors in its 3B line of minicomputers. Meanwhile, Sun's plans to establish a group of highly competitive vendors for Sparc has taken several more steps forward. Following the announcement in August of a second-source agreement between previous Sparc licensee Cypress Semiconductor (San Jose, CA) and Texas Instruments (Dallas, TX), Fujitsu Microelectronics (San Jose, CA) and Prisma (Colorado Springs, CO) have made announcements of their own. Fujitsu has announced production release of its 15-Mips, second-generation S-25 Sparc CPU. Implemented in the company's 1.2-micron CMOS process, the chip will run at 25 MHz.

Separately, supercomputer design house Prisma announced plans to implement Sparc in gallium-arsenide MSI. The company reportedly plans to use logic chips from Gigabit Logic (Newbury Park, CA) to build a Sparc CPU system capable of 250-MHz operation and a peak execution speed of 250 Mips. Shipment is scheduled for late 1989. —John Mayer and Ron Wilson

A RISC solution takes wing

At the Buscon/88-East show earlier this month, a group of vendors unveiled what's touted to be the first complete real-time and general-purpose development system and execution environment for a RISC processor: namely, Sparc from Sun Microsystems (Mountain View, CA). Cooperative development efforts among Fujitsu Microelectronics (Santa Clara, CA), Mizar (Carrollton, TX), Sun Microsystems (Mountain View, CA) and Wind River Systems (Emeryville, CA) have yielded their first fruit. The real-time computer server and a hybrid development system combines a Sun Unix environment and a Sparc real-time subsystem within a single enclosure. "Anyone who wants to do a real-time application with Sparc will now have all the hardware, software, development tools, and other support he needs," says Joe Ramunni, Mizar president and CEO. —David Lieberman

Digital paper drives poised to boost optical storage

Mass storage peripherals using inexpensive, flexible "digital paper"—actually a Mylar substrate coated with photoactive polymer dye—are set to compete heavily in the optical storage arena. According to a report by Venture Development Corp (Natick, MA), Bernoulli Optical Systems (Boulder, CO), a subsidiary of Ionmega (Roy, UT), is readying disk drives using digital paper, and Creo Products (Burnaby, BC, Canada) will use the paper in tape drives.

Digital paper disks can be accessed in around 40 ms, according to Robert Perera, director of research and development for Bernoulli. This access time, faster than that of rigid optical disks, is possible because the flexible media can be stabilized at the focal point of the laser head. Because the head needs no focusing mechanism and can be lighter than other optical heads, they can be positioned faster. Storage capacities on the order of 1 Gbyte on a 5½-in. disk are expected.

The digital-paper-based tape drive under development by Creo is expected to boast 1,000 Gbytes per reel. Fabio Arcuri, market research analyst at VDC, calculates that a 2,900-ft reel of digital paper tape would have the capacity of a 20-ft optical disk—with sequential access, of course. —Tom Williams

DEC to purchase new RISC chip for Unix workstation

Digital Equipment Corp (Maynard, MA) has finally gone public with its long-rumored agreement to purchase RISC microprocessors from MIPS Computer (Sunnyvale, CA). DEC will use the MIPS processor in a line of Unix workstations. The move is apparently a counterstroke against the success of Sun Microsystems (Mountain View, CA) in penetrating the decade-old VAX/VMS hegemony over engineering computing. Previous DEC attempts to fight against Sun and Apollo workstations with its proprietary MicroVAX architecture have seen only limited success. Under the agreement, DEC will take an equity position in closely held MIPS that could reach as much as 20 percent of the company. —Ron Wilson

The PS/2 clone countdown

There are 30 days left until Comdex '88 convenes in Las Vegas, and the odds are excellent, according to well-placed sources, that somewhere between a half and a full dozen computer vendors will introduce their first PS/2 clones at the show, joining the three vendors who have already taken the plunge.

Even more board, system and peripheral vendors may use the show to preannounce PS/2-compatible products, unless the recent announcement of the EISA (Extended Industry Standard Architecture) alternative to IBM's Micro Channel architecture moves them to continue to keep their PS/2-compatible prototypes under wraps. Should the EISA indeed contribute to the already widespread uncertainty about the advisability of supporting the PS/2, expect to see a slew of "EISA-compatible" banners gracing the wealth of new AT-compatible products certain to appear at the show. Then, of course, there will be those who hedge their bets by supporting both the Micro Channel and the EISA. —David Lieberman

(continued on page 10)
OEM superminis tackle real-time applications

Thanks to a cell-based application-specific IC processor, a new family of high-performance computers from Modcomp (Fort Lauderdale, FL) can tackle real-time applications without the need for additional front-end processors. The ASIC processor provides over 10 Mips to give the series the ability to address the computational speed requirements of real-time systems. Additional computational power is available using an optional hardware floating-point accelerator.

The company uses an advanced 299-lead ceramic pin grid array to handle the main processor chip, which packs over 220,000 transistors (54,000 gates) and was developed in conjunction with VLSI Technology (San Jose, CA). Cache and memory-management handling for the machines is provided through ASICs, while interrupt handling and I/O throughput are managed with additional ASIC components as well as standard ICs. Introduction of this yet-to-be-named series of computers is slated for Autotake next month.—Sydney Shapiro

DEC submits XUI user interface tools to OSF

Digital Equipment Corp (Maynard, MA) has formally submitted its XUI user interface technology in response to the Open Software Foundation’s request for graphical user interface technology. All technologies submitted must conform to the X Window System, Version 11, which was developed at the Massachusetts Institute of Technology (Cambridge, MA).

Designed to run on any hardware platform, the XUI programming environment consists of a toolkit, a style guide, a window manager, a session property manager and associated documentation. With XUI, programmers can design a graphical user interface with icons, scroll bars, and pull-down menus for their programs. DEC designed the technology to provide a single application program interface for systems supporting the X Window standard and to eliminate the problems associated with multiple operating system environments.—Mike Donlin

PC-based system uses CD-ROMs to automate component selection

A PC-based system gives engineers access to technical specifications and manufacturer’s data sheets for ICs and discrete semiconductors. Called Cahners CAPS (Computer Aided Product Selection) by Cahners Information Services (Newton, MA), the system stores text and graphics images of over 400,000 devices from more than 250 companies worldwide on a set of CD-ROMs.

CAPS installs on a subscriber-provided IBM PC AT or compatible and consists of a four-disc CD-ROM reader, a high-resolution full-page monitor and a mouse. Data base updates are issued to subscribers at 90-day intervals and include information on new components, manufacturers’ revisions and cross-reference part numbers. A one-year subscription, including hardware, costs $7,950.—Mike Donlin

Whither the Micro Channel?

Is IBM slowly abandoning the Micro Channel? Just a few weeks after introducing a new PC based on the older AT bus, and just one week after IBM’s major PC rivals banded together to endorse an extended version of the older bus architecture, reports are circulating that IBM is working on yet another PC not built around the Micro Channel.

The new system reportedly uses Intel’s new 80386SX processor, a stripped-down version of the popular 80386 with a 16-bit data path. If not indicative of any erosion of IBM’s support for the Micro Channel, the “new/old” PCs just may reflect the company’s reassessment of its decision to quickly abandon the older AT architecture after introducing the Micro Channel-based products.—John Mayer

Quarter-inch tape vendors fight back against DAT

For those tempted to exchange their familiar ½-in. cartridge tape drives for one of the latest wrinkles in magnetic storage—the computer-oriented variety of digital audio tape (DAT)—the ¼-in. industry suggests another solution: stick with what you have. Since many designers have become enamored of the very high capacities possible with DAT, the Quarter-Inch Cartridge (QIC) standards committee will push its products beyond the current 320-Mbyte frontier into the 1.3-Gbyte capacity range by 1990 and to as much as 4 Gbytes by 1993. “This natural migration path will all be based on the use of reliable, widely accepted DC600-class cartridges,” says Sam Thompson, committee chairman, “and the resultant product class will have capacities equal to new, competing technologies such as DAT, while achieving faster transfer rates.”

—David Lieberman

EDIF interface boosts CAE system independence

Designers can now transfer schematics and net lists between multivendor application-specific IC design-automation tools by using a software interface from Synopsys (Mountain View, CA). The interface allows automatic EDIF (Electronic Design Interchange Format) net-list-to-schematic translation in either direction between the company’s Design Compiler and standard EDIF-compatible files available from most major CAE vendors. Although EDIF has been around since 1983, true compatibility between systems has been hindered by differences in each system’s design data. The Synopsys interfaces tackles that problem by extracting the design from its source representation and then regenerating it into an EDIF description in the context of the target system.—John Mayer
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Crucial issues buried in the noise

This year's presidential campaign has been marked by so much mudslinging, negative campaigning and evasion that even the few positive proposals made by the campaigners have been lost in the noise. Bush's day-care plan, for example, was ridiculed into oblivion, and Dukakis's college-financing proposal seems to have evaporated like a morning fog. At a time when the United States is challenged by determined, hard-working and ruthless competitors throughout the world, how can two such crucial issues—one, our ability to utilize every potential member of the work force who wants to work, and two, our ability to create a more knowledgeable and skilled work force by opening the doors to everyone who wants a college education—be so brusquely pushed aside? It boggles the mind, to use a tired, but true, cliche.

The United States has an enormously underutilized resource in its female population. Despite all of the gains that have been made over the last 20 years or so, there's still a long way to go before women have a fair shot at all of the jobs—and everything that goes with them—that are open to men. You only have to look at the number of women in science and engineering to see that this is so. Maleness or fatherhood is never an obstacle to a good job, or good pay, or rapid advancement or a rewarding career, but femaleness, and especially motherhood, still is. The time has long since passed for us to remove this last barrier. Many of our competitors, even those in which women are still second-class citizens in every way, provide better day care than the United States does. The options are many, and a tax credit is only one of those that should be—no, must be—explored.

Male or female, the route to a good job, good pay, rapid advancement or a rewarding career is a dead end for most without a college education. But getting a college education today means having parents who are well-off—nothing short of wealthy, it seems—or who are self-sacrificing, or who are poor enough to have their children qualify for assistance in one form or another. A lot of youngsters who are smart, hard-working and deserving of an education are simply left out. A simple solution to this vexing problem is to have the individuals who will benefit from a college education over their lifetimes pay for that education over their lifetimes. According to Dukakis's proposal (which was nothing new, by the way), an eighth of a percent tax for every thousand dollars borrowed for a college education—maybe we should say "invested" in a college education—would do the trick. What's that, compared to the extra quarter of a million dollars, more or less, that a college education is worth over a lifetime?
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**SHARP'S NEW HIGH-SPEED CMOS SRAMs**

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>ORGANIZATION</th>
<th>ACCESS TIME</th>
<th>AVAILABILITY</th>
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<tr>
<td>LH52252</td>
<td>64k x 4</td>
<td>35 ns/45 ns/55 ns</td>
<td>Immediate</td>
</tr>
<tr>
<td>LH52259</td>
<td>32k x 9</td>
<td>35 ns/45 ns/55 ns</td>
<td>3Q 1988</td>
</tr>
<tr>
<td>LH52251</td>
<td>256k x 1</td>
<td>35 ns/45 ns/55 ns</td>
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<td>LH52256</td>
<td>32k x 8</td>
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<td>LH5261</td>
<td>64k x 1</td>
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<td>1Q 1989</td>
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<tr>
<td>LH5262</td>
<td>16k x 4</td>
<td>25 ns/35 ns</td>
<td>4Q 1988</td>
</tr>
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This issue's cover...

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Chip set tackles laptop design issues, offers flat-panel VGA control

Tom Williams, Western Managing Editor

Declaring laptop computer systems as “the wave of the future,” Chips and Technologies (San Jose, CA) has developed a core logic chip set specially tailored to laptop computers’ needs for power savings, tight integration and design flexibility. Called Leap (for Low-Power, Enhanced AT Portable), the chip set is accompanied by a single-chip flat-panel Video Graphics Array (VGA) graphics display controller. The chips are designed to provide the basis for systems built around the Intel 80286 at 12, 16 and 20 MHz, and around the 80386SX at 16 or 20 MHz. The 80386SX, a full 32-bit 80386 that uses a 16-bit external bus, allows considerable interconnect and board space savings in portable systems.

Chips and Technologies designed the Leap chip set with the assumption that the distinction between desktop and laptop systems will blur in terms of functionality. “In order for laptop systems to really take off, there will have to be a lot of the desktop features embedded that you can take with you,” says Ahmet Alpdemir, systems logic product manager. In addition, customers are demanding other features—such as security, power savings and the ability to interface to ROM cartridges—that are unique to laptops.

The Leap chip set, also designated the CS8223 chip set, consists of a bus and memory controller, an address/data buffer chip with bus conversion logic, an 82C206 integrated peripheral chip, an 82C636 power control unit, an 82C609 multifunction controller/data separator and an 82C455 VGA/LCD controller.

Many of Leap’s features are programmable—and these are the ones that OEM system designers will use to to make cost/performance trade-off decisions and to customize designs. One of the main avenues for product differentiation, according to Alpdemir, will be by means of the basic I/O system (BIOS). “Every motherboard is going to be different from OEM to OEM,” he says. An OEM system designer may decide, for instance, to program in different wait states based on the selected memory speed, or he may want even more security features than are already implemented by the chip set. Or the designer may choose to give the user control over setting certain para-

Chip set provides a shadow RAM capability, which lets the BIOS be loaded into system RAM from the EPROM on boot-up. The BIOS is then executed from the faster system RAM. The designer also has the option of storing system and display BIOS in the same EPROM.

Meeting needs of laptop users

Since laptops contain sensitive information, users want them made safe from unauthorized access. Chips and Technologies dealt with the security issue by building in an interface to EEPROM that allows storage of two passwords. The user enters one of the passwords, and the factory preprograms the other. The preprogrammed password overrides the user password; therefore, a user who forgets his or her password can take the machine back to the dealer to regain access to it.

Users also want a laptop that can run on battery for eight to 10 hours, according to Alpdemir. Power-saving features of the Leap chip set concentrate on two main areas: shutting or slowing down the CPU clock, and monitoring peripherals that consume large amounts of power and shutting them down if no activity is detected in a given time period. For the 80C286, the 82C241 system controller provides a sleep mode that stops the CPU clock while the application is waiting for an external event. While the system is in sleep mode, interrupts are still processed normally. Each time an interrupt is serviced, the sleep mode checks to see if some specified event has occurred. If it has, the application takes over; if not, the system goes back to sleep.

For CMOS processors that can’t be completely shut down, their operating frequency can be slowed down to one-sixteenth the operating frequency of the processor clock. This can be combined with the use of slow-refresh dynamic RAMs, for which the refresh cycle can be expanded from 4 to 64 ms for added power savings.

Slow-refresh DRAMS come into play when using the Leap suspend/resume capability. The designer can configure a BIOS to set the machine into standby mode when the power is turned off. In standby mode, operation is suspended and the contents of registers are saved either to battery-
backed CMOS RAM or to disk—again at the designer's option. Battery-backed slow-refresh DRAMs can be used to keep the application alive while consuming less power. When power is turned on, the contents of the machine's registers are restored to the CPU and configuration registers, and the application resumes.

One big consumer of power in any system is the disk drive. Several peripheral manufacturers, seeing the potential in the laptop market, are designing devices with power monitoring and conservation features. The 3½-in. CP-3022 20-Mbyte Winchester drive from Conner Peripherals (San Jose, CA), for example, can be programmed to shut down the other power-hungry devices—especially backlit LCD displays—in the system and shut them down after a predetermined time-out. Here again, time-outs for certain devices can be set by the OEM in the BIOS, and/or a range of time-out options can be made available to the user.

The advent of ROM cards and modules that can be plugged in or removed by the user has made customizing systems and applications easy and affordable and is a natural for laptops. "All of our customers asked for direct access to ROM modules," says Alpdemir. ROM modules can come in many forms, such as chips that plug into the mother board, or as credit-card-sized modules such as the ITT Cannon (Fountain Valley, CA).

Although a great deal of this will be done in hardware, an even greater degree of product differentiation will probably come through innovations in the BIOS that will take advantage of high-performance levels and options using a common silicon platform. Chips and Technologies' goal in developing the Leap chip set, according to Alpdemir, was to offer OEMs a wide range of possibilities for configuring systems and targeting price/performance levels and options that ensure a minimum user-selectable contrast between any adjacent gray scales on the screen. Thus, no matter how the initial gray-level-to-color map is set up, the actual display will be automatically adjusted so that it's readable.

Chips and Technologies' Leap chip set is helping create a new generation of true laptops that are small, power-stingy and highly functional. The chip set integrates CPU, AT bus control functions, memory control logic and specific features into six VLSI CMOS devices.

The Leap control logic supports EMS 4.0 with four 1-Mbyte on-chip page registers, and Chips and Technologies also supplies a software driver to use the extended memory option to accommodate ROM modules or system memory beyond the 640-kbyte DOS limit. But for optimal multitasking of the kind that will be required to support OS/2, at least 64 registers are needed.

**Flat-panel VGA control**

Probably the biggest barrier to a wide acceptance of laptop computers is the quality of their displays. While there have been steady improvements in readability, until now there hasn't been a large-format LCD display that's truly readable in a wide range of viewing angles and lighting conditions.

"This year, however, all the major Japanese LCD manufacturers will be presenting neutralized twisted nematic (NTN) displays that will finally have "page white" display quality. And they'll be capable of up to 16 levels of gray scale and will have a screen resolution of 640×480 pixels, making them compatible with the VGA standard from IBM."

"What we're seeing is the influence of increasing display resolution coinciding with the software standard," says Keith Angelo, product manager of graphics operations at Chips and Technologies. The company claims that the pairing of the 82C455 flat-panel VGA controller with the Leap chip set creates the first controller chip to offer VGA support for LCD, plasma, electroluminescent and CRT displays.

Since even the NTN LCD displays are monochrome, the chip must be able to map the 16 gray-scale levels of an NTN panel to the 16 colors specified by VGA. This is done by an on-chip algorithm called Smartmap that ensures a minimum user-selectable contrast between any adjacent gray scales on the screen. Thus, no matter how the initial gray-level-to-color map is set up, the actual display will be automatically adjusted so that it's readable.

Chips and Technologies' goal in developing the Leap chip set, according to Alpdemir, was to offer OEMs a wide range of possibilities for configuring systems and targeting price/performance levels and options using a common silicon platform. Although a great deal of this will be done in hardware, an even greater degree of product differentiation will probably come through innovations in the BIOS that will take advantage of Leap's programmable options.

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**LEAP-BASED LAPTOP SYSTEM**

Chips and Technologies' Leap chip set is helping create a new generation of true laptops that are small, power-stingy and highly functional. The chip set integrates CPU, AT bus control functions, memory control logic and specific features into six VLSI CMOS devices.
DSP-based microcontrollers blaze new trails into real-time computing

Warren Andrews, Contributing Editor

The traditional role of the microcontroller is changing from performing relatively slow, standalone functions to handling high-speed, real-time, or close-to-real-time activities. And while semiconductor manufacturers are scrambling to boost the performance and bus width of more conventional controllers, industry demands—particularly in terms of algorithm complexity—are outrunning their efforts. In response, a new breed of microcontroller is emerging that's replacing the conventional processor core with a high-performance digital signal processor. And while such parts may take sockets from traditional microcontrollers, their speed and flexibility will undoubtedly let them replace analog subsystems as well as underpin entirely new applications.

The first of this new-generation device comes from Microchip Technology (Chandler, AZ), the wholly owned spin-off of General Instrument's semiconductor group (Hicksville, NY). The chip was designed by Microchip under a license from Texas Instruments (Houston, TX) and is being manufactured and marketed by both companies. The DSC320C14 is a single-chip device in which the core of a TI 320C10 DSP is surrounded with I/O and peripheral circuits. The new controller offers a 160-ns instruction time that, when combined with its ability to execute multiplication operations in one instruction cycle, results in a peak performance of 6.4 Mips—five to 10 times that of conventional 16-bit microcontrollers.

The new architecture represents a revolutionary change in the way engineers look at control functions—many of whom continue to use analog circuitry because the DSP horsepower hasn't been available, according to Rahul Sud, vice-president of marketing for Microchip. Because the 320C14 can execute single-cycle multiplications, it can perform many advanced control algorithms, such as adaptive control, Kalman filtering and those for state controllers in real time, says Ajay Padgaonkar, design engineering manager.

Other DSP makers follow suit

Though the Microchip/TI DSP controller is the first of its kind to hit the market, expect to see a host of similar products surface in coming months. Fujitsu Microelectronics (Santa Clara, CA), for example, recently introduced a 24-bit floating-point DSP chip aimed at cost-sensitive applications. Fujitsu is positioning the device as a DSP microcontroller even though it lacks most of the peripheral and I/O functions of the 32C14, according to John Reimer, the company's manager of microcomputer and communications products. Because the company positions the chip as a controller, Reimer hopes that designers will begin to consider using DSPs rather than more conventional microcontrollers such as

**THE DSC320C14 ARCHITECTURE**

Microchip Technology's 320C14 single-chip digital signal processor controller includes a TI 320C10 core DSP and a number of I/O and peripheral functions. These include 16 bidirectional I/O ports; four 16-bit incrementing timers; a compare module including four 4-x16-bit first-in, first-outs; a capture module with six pulse-width modulation output channels; a serial port that performs either synchronously or asynchronously and offers a codec (coder-decoder) mode to support standard digital telephone rates; and an interrupt controller.
The combination of a DSP CPU's power with a microcontroller's I/O and peripheral functions has opened up a host of new applications.

Closed-loop control
One of the more promising applications for the DSP controller is in closed-loop control, where a feedback loop is used to improve control accuracy by compensating for system characteristics. Traditionally, these compensation loops have been built using analog circuitry. If digital techniques are used, the control loops are generally implemented using second-order finite impulse response (FIR) and infinite impulse response (IIR) filters. These digital approaches bring higher reliability, noise immunity and flexibility to such applications. But these complex digital filters require computationally intensive sum-of-products calculations and traditionally have been poor performers, too expensive, or both.

Conventional microcontrollers lack the hardware arithmetic capability and are unable to compute such filter algorithms in anywhere near real time. Instead, they rely on approximate values obtained by accessing lookup tables, which results in an inflexible system that often lacks the necessary accuracy. DSP chips have the computational capability but, until now, have lacked the I/O and peripheral functionality for cost-effective implementation. Systems built from conventional single-chip DSPs are burdened with so much extra glue logic that their implementable prescalers to divide the clock by 1, 4 or 16. Included are a watchdog timer with programmable time-out; a pair of general-purpose timers that can be configured to produce one 40-bit timer with a resolution of 160 ns and a maximum duration to two days; and a baud-rate generator.

The watchdog timer provides a number of functions. To prevent accidental resetting of the timer, it's nonwritable. To assure glitch-free operation, the programmable time-out period is stored in a double-buffered period register, and to simplify the creation of an independent "warm restart" mechanism, the timer makes its overflow signal available on one of the chip's pins, which can also be tied directly to the reset input.

Direct control over external actuators such as valves, relays and indicators is managed by the 32C014's 16 software-configurable latched I/O lines. A data-direction register determines whether a given line is used as an input or output. A second 16-bit register stores the status of each line. Individual bits can be set or reset using bit-set or bit-clear functions without having to use read-modify-write operations. In addition, the input lines can be grouped so that an interrupt is generated when the value of the input lines matches a preset value stored in an I/O buffer.

A timer-based event manager comprising a capture system, comparator and a pair of timers handles high-resolution edge detection and enables direct, continuous control of power devices, transducers and motors. The capture system offers 160-ns edge detection and provides a direct optical encoder interface for performing functions such as determining motor speed and resolving shaft position. The capture system monitors the chip's four capture pins with one 4 x 16-bit first-in, first-out dedicated to each pin for storing the timer value associated with a pin transition. The event manager's two timers can be used as a time reference.

The compare system produces pulses on six of the chip's output pins. The pulse width is determined by one of the timer values and a programmed value stored in a compare register. The compare registers constantly compare their value with the
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timer value and hold data until it's rewritten with a different value. When the value in a compare register matches the timer, the compare subsystem generates a pulse and feeds it to a set of six action registers. Bits in the action registers determine if the compare pulses will set, reset or toggle the compare pins, or generate compare interrupts.

The compare system's six outputs can be converted to high-speed pulse-width modulation outputs by setting a control bit. The outputs produce pulses as small as 40 ns at a frequency of up to 3 MHz, thus providing a 10-bit resolution at 25 kHz or 8-bit resolution at 100 kHz.

The future of DSP controllers

Looking a step or so ahead, it seems natural evolution for DSP cores to become cells in many semicustom vendors' libraries, just as the 6502, COPS800, 8051 and other microcontroller architectures have been merged into cell libraries. At least for this generation and maybe the next, however, this may not prove to be a practical solution because of the die area occupied by the DSP function. The DSP function measures about 110 mils on a side—considerably larger than most conventional library cells. But with rapidly shrinking geometries and process refinements, the DSP core's size may cease to be an obstacle to its semicustom status.

SOFTWARE

Unix gains edge over OS/2 by running DOS applications

Tom Williams, Western Managing Editor

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he race is on between Unix and OS/2, and Unix has a head start. Why? As OS/2 and Unix start to compete side by side for acceptance in the commercial, business sector, Unix stands ready at the starting gate with a rich multitask environment and established applications. And now, Unix is gaining an extra boost as the capability emerges to easily run DOS applications from a Unix environment on a wide variety of hardware platforms. In addition, Unix may pull a clear distance ahead of OS/2 with the added push from recent developments aimed at improving the user interface via the X Window standard, combined with the efforts of the Open Software Foundation (OSF) to provide a common operating environment spanning many major hardware vendors.

Unix will likely move from its traditionally perceived role as an operating system for engineers and scientists into a new role as an operating system for the business environment that can support single- and multiuser productivity applications. And that's precisely the environment for which OS/2 has been targeted. This migration of Unix into the office will become possible when and if a commonly understood user interface emerges to shield the nontechnical user from having to deal directly with the actual workings of the operating system.

Although Unix hasn't yet achieved an acceptable level of user comfort, it still has a leg up over the yet-to-be-fully-real OS/2: there's a larger number of applications than currently exist for OS/2, and now with the ability to run existing DOS applications from a Unix environment, that advantage will take a quantum leap.

Efforts to provide access to DOS applications from the Unix environment have been spurred by the emergence of workstations based on high-performance, 20- to 25-MHz versions of the Intel 80386 32-bit CPU. Such workstations are in a performance class with Motorola 68000-based workstations running Unix that are now used for CAE/CAD/CAM and scientific work.

The 80386 also brings a link into a universe of applications that have become widely accepted in the business community. What has heretofore been lacking, however, is an operating system that can fully utilize the 80386's potential. What users have really needed—and what DOS doesn't provide—is a truly multitasking operating system that can directly address large memory arrays. But at the same time, users also need access to the vast number of quality application programs and the civilized user interface they have come to ex-

"The last thing a software vendor wants is to have his 'pride and joy' run in Unix and run terribly," says Colin Hunter, president of Hunter Systems. To ease the translation of DOS programs so that they run efficiently under Unix, Hunter Systems has developed a set of tools for both software vendors and hardware OEMs.
SOFTWARE

pect under DOS.
The development of OS/2 was ostensibly aimed at that goal. But with OS/2 lagging and genuine standards efforts afoot in the Unix community, software developers are taking a wait-and-see attitude before investing in developing OS/2 applications. Meanwhile, some companies have developed ways to bring existing DOS applications into the Unix environment, thus making Unix an even more attractive option as a powerful, multitasking operating system.

Bringing DOS into the fold

There are basically two ways to get applications written for DOS to run under Unix: emulate a DOS environment under Unix and run the applications unmodified, or translate each program so that it runs efficiently in the Unix milieu. Both of these approaches are being pursued. Insignia Solutions (Sunnyvale, CA) and The Santa Cruz Operation (Santa Cruz, CA) are taking different tacks at emulating a DOS environment, while Hunter Systems (Mountain View, CA) has developed a set of tools to ease the task of translating DOS programs to run like "well-behaved" Unix applications.

Insignia Solutions has created a complete software emulation of a PC. Called SoftPC, it's "a total emulation of a PC, including 8088, peripheral chips, DMA, timers and graphics," according to Henry Nash, vice-president of engineering. Versions of SoftPC are available for the 68000 family, MIPS Computer Systems' reduced-instruction-set processors, the Motorola 88000, and the Intergraph Clipper processor. SoftPC is also available for manufacturers to bundle with their systems.

A similar approach is used by The Santa Cruz Operation (SCO) with its VP/ix product, which runs under the company's Xenix version of Unix on the 80386. VP/ix is limited to the 80386 because it takes advantage of the 80386's ability to support a mode that will run a hardware version of the 8088 instruction set. So VP/ix supports an emulation of the PC DOS environment under Unix but, unlike SoftPC, doesn't have to emulate the instruction set. VP/ix, however, doesn't have SoftPC's portability to other processors. Both SoftPC and SCO's approach requires somewhat less memory because the instruction set is in hardware and, therefore, SCO doesn't have to emulate the machine instructions in software.

The performance of VP/ix is tied directly to the speed of the 80386 processor being used. For SoftPC, performance is also tied to the processor, but will vary greatly depending on the particular processor, architecture and the number of users and/or tasks on a multiuser system. A single-user 68020 running at 16 MHz, for example, will yield a SoftPC performance roughly equivalent to that of a basic IBM PC XT, according to Insignia's Nash. With higher performance systems, he says, "You can get close to the performance of an AT." In addition, he says, as code is refined and made more efficient, performance will improve.

Easing the translation task

"The last thing a software vendor wants is to have his 'pride and joy' run in Unix and run terribly," says Colin Hunter, president of Hunter Systems. "Most DOS software ven-

SC0 XENIX WITH VPI/IX EXTENSION

The Santa Cruz Operation's solution to emulating a DOS environment under Unix, VP/ix runs under the company's Xenix version of Unix and uses the 80386's support of the 8088 instruction set to set up multiple virtual DOS environments. Users can load and run DOS applications without modification, but can also share DOS and Xenix data files.

VP/ix can share files with Unix.

Emulating an entire machine's logic as well as an operating system requires a certain amount of overhead. And in a multiuser environment, each user running a DOS application has his or her own DOS machine emulation. Nash estimates that a SoftPC emulation requires about 1 Mbyte of memory plus 640 kbytes for the DOS system memory.
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of a front-end that reads an executable DOS program—directly as supplied by the manufacturer—and a back-end that generates instructions for the target processor. The resulting code is then linked to a run-time package to run under Unix. Thus, the user doesn’t need access to source code to perform the translation.

The front-end of the binary compiler reads the DOS program and a .KEY file that has been generated by the global analyzer. The .KEY file contains information needed by the compiler to help it regenerate the application in a form that will make it run efficiently under Unix. The .KEY file contains a complete analysis of the program, including flow graphs, information on registers and flags needed by the XDOS compiler.

In the course of generating the .KEY file, the analyzer may encounter sections of code it can’t handle automatically. Anomalies may include sections of code that alter themselves or I/O routines that aren’t efficient in a Unix environment. In the case of such ambiguous code, an engineer is needed to interactively input data to complete the .KEY file.

One example cited by Hunter where an interactive input would be useful is in a keyboard input routine. Many DOS programs are written for single-user, single-task machines. Thus, a program might go into a tight loop, polling the keyboard and looking for character input. In a multitasking, multiuser system, this represents a waste of CPU resources. A keyboard interrupt routine is more appropriate, because it simply waits for an interrupt to tell it that it has input rather than tying up the CPU.

Hunter Systems’ strategy is to make the analyzer portion of XDOS primarily available to software manufacturers. They could then produce .KEY files to go with the Unix versions of their DOS software products. The binary compiler would mainly be used by hardware OEMs to bundle with their systems.

Dealing with graphics

Lest the situation sound too rosy, none of the three companies mentioned has come up with a totally satisfactory way to transform the IBM standard graphics operations into something that looks like the DOS application’s graphics output on the myriad of display devices used by Unix-based systems—including dumb terminals. The reason is that graphics and user interface standards in the Unix world are still in a state of flux.

Of the three products, Insignia’s SoftPC comes the closest to “DOS-like” graphics because the PC emulation also emulates the graphics silicon. The present graphics emulation is limited to the Color Graphics Adapter hardware, which has a resolution of only 320 x 200 pixels, but emulations are in the works for emulation of the Enhanced Graphics Adapter (EGA) with 640 x 350 pixels and the Video Graphics Array (VGA) at 640 x 480 pixels. The output of the SoftPC graphics emulation must, of course, then be adapted to whatever Unix drivers and display hardware are being used on the target system.

Insignia also has a standard X Window version 11 implementation of SoftPC for Unix machines that standardize on the X Window system. DOS graphics output from a VP/ix has an advantage in that many 80386-based systems use IBM-type graphics controllers—primarily EGA and VGA—and therefore can handle the graphics directly. Since VP/ix isn’t specific only to the 80386, but also to Xenix, DOS graphics output can run in full-screen mode in SCO’s Xenix window environment.

XDOS comes in two versions: a “vanilla” character mode version and a graphics-oriented version. Porting the graphics version requires more effort, and the hardware integrator must pay attention to all the details of a given display environment to be able to adapt it. Hunter says he is encouraged, however, by the growing popularity of window-oriented user interface systems, both in the DOS and in the Unix worlds. “We can easily map a Microsoft Windows application onto X Window,” Hunter says.

Given the fact that Unix appears to be getting its act together, proponents of Unix as an alternative to OS/2 have been becoming bolder in their pronouncements. Not least among these are the suppliers of bridges to DOS applications.

What if one should be tempted to ask the heretical question, Does the world even need OS/2? “That’s a good question,” says Insignia’s Nash. “We’re taking a wait-and-see attitude.” Hunter Systems’ Hunter is more definite. His answer: “No.”

A global analyzer and a binary compiler are the two major components of Hunter Systems’ XDOS system. The global analyzer (a) reads an application .EXE file and generates a .KEY file containing the parameters needed to convert the program structure to work with Unix. Any items the analyzer can’t deal with automatically are stored in the .ANOM file. An engineer then resolves those problems and enters any customization input via the .ASD file. The XDOS binary compiler (b) runs on the target hardware. It reads the software vendor’s standard .EXE file along with the final version of the .KEY file, and the target processor-specific back-end produces a native binary file that’s linked to the target machine’s run-time package.
Development tools enhance real-time Ada support

Richard Goering, Senior Editor

Developers of embedded software for military systems have two critical needs—real-time programming support and the Ada programming language. To provide the best of both, Ready Systems (Sunnyvale, CA) this month is introducing a target-environment Ada simulator, a complete Ada operating system, and various Ada-specific enhancements to its Computer Aided Real-Time Development tools (CARDtools).

Of these, the most significant introduction appears to be RTAda-Sim, which Ready Systems claims to be the first run-time Ada simulator. This software simulator lets users test Ada programs written for 68020 targets without having to use an actual target or I/O devices. Available on VAX/VMS and Sun/Unix hosts, RTAda-Sim provides a re-creation of the environment, simulating the I/O devices, clock, run-time system and operating system.

Of the many existing software simulators, few provide a run-time simulation of target I/O devices. In RTAda-Sim, these devices are described through a simple form that specifies the I/O behavior in terms of direction (input or output), timing and data.

"The real bottom line is that RT-Ada-Sim lets you run Ada code unchanged," says Rich Blomseth, Ready Systems product manager. To test Ada code on a host today, users normally have to change any code dealing with the target I/O devices. Yet the complexity of I/O is one of the most difficult aspects of real-time programming, and I/O code may be the part of the program that needs testing the most. Simulating the target environment lets this I/O code be tested without modification.

RTAda-Sim includes a source-level debugger that displays the source code, allows breakpoints on the Ada source line and permits single stepping by Ada source statements. The source code displayed and executed by the debugger is the same code that will run on the target system, including operating system calls and I/O device handlers. When users are ready to move to the target, they can use Ready Systems' Artscope, a multitasking debugger that lets the target system run at full speed.

**Building an operating system**

RTAda-Sim works with RTAda/OS, an extensible real-time operating system introduced this month by Ready Systems. RTAda/OS includes ARTX, a real-time Ada kernel based on Ready Systems' VRTX kernel. "We added three additional products to build the kernel into a full operating system," explains Blomseth. These modular products include RTAda-I/O, which provides a file system; RTAda-MP, which supports shared-memory multiprocessing; and RTAda-Net, which supports LAN multiprocessing.

"The big deal with RTAda-I/O is that it provides a complete, hierarchical file system for the run-time target," says Blomseth. "Typically you have only a very simple file system for the target." In addition, RTAda-I/O supports disk and stream I/O in the target environment. RTAda-MP supports architectures that plug multiple processors into one bus, while RTAda-Net provides networking between processors using TCP/IP (Transmission Control Protocol/Internet Protocol).

**New CARDtools**

To round out its offerings, Ready Systems has added several Ada enhancements to its CARDTools, including structured analysis, structured design and real-time performance verification. One addition is an Ada Program Design Language (PDL). The Ada PDL includes Ada-specific keywords and structured support for Ada tasking constructs.

The Ada Code Builder generates Ada code frames from PDL descriptions. A code frame is an Ada package declaration that can be automatically compiled into Ada source code. It includes a header, and procedure and type declarations.

To support the documentation that's required from government contractors, Ready Systems has released a DOD-STD-2167A document generator. This standard, updated from the previous 2167 standard, defines the types of documentation that must be included with embedded software. Ready Systems has also announced a requirements traceability tool that lets users keep track of contractual obligations and ensure that these requirements are met when the software design is complete. The traceability tool also ensures that changes to the design don't violate the original specification.

**SUPPORT FOR REAL-TIME ADA DEVELOPMENT**

Ready Systems has enhanced its support for real-time Ada development with a number of capabilities. Areas of enhancement include CARDtools, which provide structured analysis and design; the RTAda development environment, which now provides a target-environment simulator; and RTAda/OS, a new operating system that builds on Ready Systems' ARTX kernel.
Off-the-shelf in-circuit programmers cut costs, ease firmware updates

Richard Goering, Senior Editor

By programming devices such as EPROMs after they're loaded onto printed circuit boards, in-circuit programming tools can save production costs and ease firmware updates. But in-circuit programming is both customized and expensive. And, until now, it has been used almost exclusively in certain high-reliability military applications. This month, however, Data I/O (Redmond, WA) is taking first aim at the commercial marketplace by introducing what it claims to be the industry's first off-the-shelf in-circuit programmer.

The company's Boardsite 4100 and 4400 programmers are portable units hosted by the IBM PC. They include a do-it-yourself interface kit that lets users connect their printed circuit boards to the programmer by constructing a simple wire-wrap board. The Boardsite units also provide software that lets users define a board profile, which describes the printed circuit board's characteristics to the programmer.

A traditional custom-built system, in contrast to a portable unit, includes a physical interface and a board profile that's developed by the programmer vendor. Costs are typically $40,000 to $50,000, and a new cost is incurred every time the board is changed. The Boardsite programmers start at $9,500.

Multiple benefits
In Data I/O's missionary effort to bring in-circuit programming to the commercial world, the big selling point is going to be cost savings during production. In-circuit programming involves fewer production steps because users don't have to program each device individually, label each part, and then store each part before assembly. Instead, the entire board is assembled, and then it's programmed as a unit.

"Not only have some steps been eliminated, but you're dealing with whole boards rather than parts," says Randall Lutz, product manager at Data I/O.

In addition, inventory control is simpler with in-circuit programming because it isn't necessary to maintain separate supplies of individually programmed parts. Firmware updates are also much easier because users won't have to remove devices from the board, erase and reprogram each part individually, and load them back onto the board. With in-circuit programming, the entire board can be erased and then reprogrammed as a unit.

In-circuit programming also eliminates sockets, which is a big plus for some users. Sockets are often placed on boards so that devices can be removed for firmware updates. But sockets take up real estate, and they cost money. "For example, if you're talking 15 parts to a board, at anywhere from 50¢ to $1 for a socket, and 10,000 to 20,000 boards a year, it adds up," explains Lutz.

Despite its advantages, in-circuit programming isn't the answer for all types of programmable devices or all kinds of designs. It's primarily beneficial for MOS EPROMs and EEPROMs. The Boardsite programmers can support certain other MOS devices as well, such as microprocessors, microcontrollers and programmable logic devices. Bipolar PROMs generally aren't programmed in-circuit because they require that voltages be raised to levels that could possibly damage adjacent TTL circuitry.

In-circuit programming is seldom practical for complex PLDs because it would complicate logic verification. "You can't verify the test vectors very easily unless you've done some fancy footwork in order to get the sig-

The Boardsite programmer from Data I/O is the first off-the-shelf programmer for in-circuit programming. According to product marketing manager Randall Lutz, board manufacturers can save production costs and simplify firmware updates by programming devices such as EPROMs after they're loaded into boards.
Placing decoupling capacitors on the $V_{cc}$ and $V_{pp}$ lines is recommended.

**Creating a board profile**

In-circuit programming requires that the designer describe the board's characteristics to the programmer. This is done with a piece of software called the board profile, and in the past it's been created from an assembly language program. The Boardsite programmers let users create a board profile by answering questions in a menu format. Users provide such data as bus width, device architecture, address and data assignments, and types of MOS devices mounted on the board.

Building a physical interface to the board that's being programmed is much like constructing a simple breadboard. The Boardsite programmers come with a do-it-yourself kit that includes some prepunched boards. "It used to be hard to build an interface, but we put a lot of the logic you need inside the programmer," says Lutz. "Eighty to 90 percent of the applications need only wires and connectors. You don't need to put active components on the interface."

Because Boardsite lets users program several boards simultaneously, it includes isolation circuitry. This buffer circuitry isolates the boards from one another, so that, in the case of a catastrophic failure, only one board will be affected.

The Boardsite 4100 is a single-board programmer that can be expanded to program up to eight boards. The Boardsite 4400 programs from four to 32 boards at a time. Both are now available as benchtop or portable models, and both connect to any IBM PC or compatible over a high-speed expansion bus.

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**Printed circuit board component libraries deliver consistency and accuracy**

Richard Goering, Senior Editor

One aspect of printed circuit board CAE/CAD that most engineers despise is the creation and maintenance of component libraries. Those library headaches might soon be eliminated, however, by a new company formed to provide component libraries, Sedco (Scotts Valley, CA), which is now forging agreements with printed circuit board CAD vendors.

Sedco provides component libraries representing 28 data books with over 20,000 components. Each of Sedco's DesignLib libraries includes a schematic symbol for every component in a single data book, along with a physical outline of every package type in the data book. The libraries also include all the gate- and pin-swapping information necessary for automatic placement and routing. So far, DesignLib libraries are available for design systems from Computervision, Mentor Graphics, OrCAD, Personal CAD Systems, Racal-Redac, Zuken and IBM.

Following an OEM agreement with Zuken (San Jose, CA), Sedco signed an OEM agreement this month in which DesignLib will be sold with IBM's CBDS printed circuit board CAD system. About six more OEM agreements are in the works, according to Sedco president Frank Summers. Also this month, Systems Effectiveness Associates (Norwood, MA) signed a joint marketing agreement in which Sedco will provide component libraries for SEA's thermal- and reliability-analysis programs. Until now, the absence of libraries has prevented many designers from using these programs.

**Will users pay?**

Printed circuit board CAE/CAD vendors already provide component libraries, but the cost of creating and maintaining them can be significant. Sedco's libraries are priced competitively, and the company hopes to attract new customers with its comprehensive library offerings.

"Creating and maintaining component libraries can be a big problem for printed circuit board CAD users," according to Frank Summers, president of Sedco. "Some users we've talked to say creating and maintaining libraries takes one-third to one-half of their time," he says. To help ease the engineer's task, Sedco provides component libraries that include complete data books and implement a number of accuracy checks.
TECHNOLOGY UPDATES

DESIGN AND DEVELOPMENT TOOLS

libraries as part of their product lines, but these libraries are far from complete. Rather, vendors select the most common components and then group them by technology. A given vendor might offer, for example, 500 of the most widely used TTL parts from Texas Instruments (Austin, TX). One DesignLib, in comparison, covers the entire TI TTL volume 2 data book and can be updated along with the data book.

Accuracy is another selling point for the Sedco approach. Not only is data entry from a data book error prone, but the data books themselves are often found to be inaccurate. Sedco implements an exhaustive series of checks to ensure library accuracy.

"We will not knowingly pass along an error to a customer," vows Summers. "We fixed 600 errors in the Texas Instruments TTL volume 2 data book alone."

The question now facing Sedco is whether users are willing to pay for this accuracy and completeness. After all, printed circuit board CAD vendors don't charge an additional fee for libraries, so they're essentially free. For IBM PC-based systems, Sedco leases its DesignLib libraries for $125 per seat per year for schematic or layout. For workstation-based systems, a complete schematic and layout library leases for $1,000 per seat per year.

If CAD users need to manually create even a small number of symbols per year, the cost may be worth it. It takes several hours of an engineer's time just to create a simple component definition, exclusive of test and documentation costs, according to Summers. "Some users we've talked to say creating and maintaining libraries takes one-third to one-half of their time," he says.

Schematics and layout

The schematic symbols provided by Sedco can be displayed in either the ANSI Y32.14 or IEEE-91 standards. But all of the libraries are compliant with the IEEE-91 standard, which is mandatory for defense contractors.

"There can't be a vanilla file that handles all data structures from all vendors."

—Frank Summers, Sedco

To guarantee consistency between the two different types of symbols, Sedco has developed a symbology that ensures all connection points are the same. Either ANSI or IEEE symbols can thus be plotted from the same library.

The layout symbol includes all pin numbers and names that are in the schematic view. Because there may be small variations in package size, it also includes minimum, maximum and nominal dimensions for each package. Finally, component height information is included in the layout symbol, letting the libraries be used for any of the three-dimensional mechanical tools that check for clearance and fit inside enclosures.

Sedco libraries also identify functionally equivalent pins, allowing automatic placement and routing programs to swap pins. This information may be included with schematic or layout views, depending on the system. In the future, Sedco intends to add parameters for such characteristics as pin-to-pin timing, thermal properties, weight and mass, and power dissipation. These parameters will be used in SEA's thermal analysis, in addition to stress and vibration analysis.

To get the library into a printed circuit board CAE/CAD system, Sedco compiles ASCII files according to the CAD vendor's format requirements. If the vendor uses a binary data format, for example, the library data is then compiled into that format. Once read into the system, the Sedco libraries appear exactly like any other library that comes with the system, and users can modify symbols and add part numbers if permitted by the system.

Making EDIF work

Users should remember that each Sedco library is targeted to a specific printed circuit board CAD system. "There can't be a vanilla file that handles all data structures from all vendors," explains Summers. Issuing a library in the Electronic Design Interchange Format (EDIF) won't help, according to Summers, because EDIF is aimed at file transfers between systems. EDIF doesn't let Sedco take advantage of those data structures that might be specific to one vendor.

But Sedco's approach could let EDIF translation take place at a higher level. If two systems have Sedco libraries, a component can be translated by simply referencing its name, orientation and location. One of the big problems with EDIF today is that it's difficult to move library data from one system to another. If Sedco libraries someday become common, then library portability will also become less of a problem.

Sedco's printed circuit board component libraries provide three types of information. Schematic symbols (left) are compliant with the IEEE-91 specification. Gate and pin swapping information (center) notates functionally equivalent pins for automatic placement and routing. Package size and configuration (right) is provided for printed circuit board layout.
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Multiprocessing cache bus turns to AT bus for I/O

David Lieberman, Senior Editor

Perhaps the most interesting sidelights on IBM's AT bus are the clever ways designers work around its inadequacies, especially those involved in 80386-based AT-compatible systems—such as 16-bit transfers, relatively low bandwidth, relatively inefficient DMA, and clumsy multимastering capabilities. A new multituser computer architecture called ATtack, developed by Corollary (Irvine, CA), gets around these inadequacies by relegating the AT bus to the position of I/O bus for a main system bus. The main bus of the ATtack architecture—the C (for cache) bus—has all the facilities that the AT bus lacks for building high-performance multiprocessor systems—and it even has some facilities that are lacking in the more powerful industrial buses.

Using an industry-standard bus as an I/O channel is linked to a proprietary system bus whose specifics are closely guarded secrets. Corollary, in contrast, is working on cooperative ventures to bring the architecture to market and won't be building its own ATtack machine. "We're going out of our way to be the first computer company to resist the temptation to actually build a computer," says company president George White.

Flexibility key to system

Simultaneous with the ATtack announcement, Zenith Data Systems (Glenview, IL) announced that its ATtack-based prototype workgroup and networking platform has been at beta sites since April. "This architecture is an ideal platform for Xenix/Unix applications, which can best tap the multiuser, multitasking capabilities of this new technology," explains John Frank, Zenith president. "The key to the system is flexibility. By using industry-standard components, operating systems and an open architecture, it allows expansion and upgrading as workgroup needs evolve and microcomputer technology advances."

Corollary is having "serious discussions" with three other vendors of personal computer systems, according to White.

The base components

The base components of an ATtack system are two to six 80386-based CPU boards, each with a healthy 64 kbytes of cache and support for an 80387 coprocessor; a SVID-compliant (Unix System V Interface Definition), binary-compatible extension of the Xenix 386 operating system from The Santa Cruz Operation (Santa Cruz, CA); up to four memory boards, each with from 4 to 16 Mbytes of memory for a potential maximum of 64 Mbytes of pipelined, error-corrected memory; the 32-bit, 64-Mbyte/s synchronous C bus; a "bridge" board that links the C and AT buses; and the AT I/O bus with whatever boards the system requires. The ATtack CPUs and memory boards reside only on the C bus, and the AT boards only on the AT bus, while the bridge CPU board resides on both buses, linking the two. The C bus owes its speed in part to a 16-MHz clock rate, compared to the 10-MHz clock rate of NuBus and Multibus II. "Parts have gotten faster since these two buses were first defined," White explains. "We're also willing to live with a 12-in. bus, instead of the 20-in. bus that might be specified for a Multibus II or NuBus system."

The speed and efficiency of the C bus also depend on a block-transfer
mode that, while optional on several other buses, is the only mode of transfer on the C bus, except for certain utility operations. "There's no such thing as going out to read a byte out of C bus memory," says Corollary's White. "Every transfer is of four sequential 32-bit words." The C bus, CPU caches and system memory are all geared toward this mode of operation. The C bus also has built-in cache coherency protocols, a feature shared by only the Futurebus among the industry-standard buses. For the sake of bus efficiency, a copyback caching scheme is used.

The new bus also features a fair arbitration scheme to prevent bus hogging and overlapped arbitration to avoid unnecessary idling. "Everybody says their buses are 'optimized for multiprocessing,' but C bus was built specifically to be a multiprocessing bus, and it's not particularly good at anything else," White says.

The ATtack caching scheme yields an overall 96 percent hit rate, according to White. "We've used a diagnostic program that attempts to pathologically cause the cache to miss a lot," he says. "When we run it on a five-CPU system, we wind up using about half the bus bandwidth. With a real benchmark running spreadsheets, data bases and a large variety of other application programs, the traffic is between 17 and 20 percent of bandwidth."

This suggests, of course, that the ATtack scheme could be expanded beyond its stated six-CPU limit, which White confirms. "We designed the system for 10 CPUs, although we've only built one with six CPUs so far," he says. "But we're looking at a midrange multiuser platform and aren't trying to compete with Sequent Computer Systems."

In an ATtack system, the C bus can be implemented on the same backplane as the AT bus, on a separate backplane or, conceivably, on a ribbon cable across the top of the boards. As far as running application code is concerned, ATtack is a completely symmetrical multiprocessor system, although its multiprocessing architecture is invisible to the application. Each CPU runs an identical copy of the extended Xenix kernel, and the system work load is transparently

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distributed among system CPUs as they fetch jobs from a common run list residing in system memory. But since the bridge CPU is the only CPU with direct access to the AT bus, it's the only C bus CPU able to run certain system code, such as the driver routines for an AT disk controller board. The bridge board also contains a memory-mapping function that gives AT boards a 16-Mbyte window on system memory that may, nevertheless, reside virtually anywhere in C bus memory space.

For connection to the outside world, ATtack has four 230-kbaud synchronous serial ports that link to a Corollary eight-port terminal concentrator. In this configuration, each ATtack CPU can link to 32 external serial devices. Other configurations are possible as well. White cites one interested vendor that considered replacing the ports with a small computer system interface (SCSI) chip set in order to bring disk data directly into the C bus without first going through the AT bus. "There's no hard technical information on what the benefit of this might be," explains White, "but perhaps disk traffic can create an AT bus bottleneck in some systems."

The ATtack architecture seems to have both the power and flexibility to help carry the AT bus standard well into the future. Zenith's platform, which is the first announced system to be built around the architecture, demonstrates some of the possible variations. Built around a passive backplane, the as-yet-unnamed Zenith machine implements a combination 8-16-32-bit I/O bus called the Superset bus instead of an AT bus. This permits the use of both 8-bit XT and 16-bit AT boards, as well as boards with a full 32-bit interface. The machine also features a fault-tolerant power supply—complementing the fault-tolerance capabilities of a multiprocessor system—and removable disk drives that satisfy archival or security requirements.

Hybrid board scheme bridges optical and electrical circuitry

David Lieberman, Senior Editor

Someday, prognosticators say, as the increasing speed and density of computer circuitry forces electrical technology to give way to the optical alternative, photons will replace electrons as the data carriers of necessity. In these days of pre-optical computing, however, two electrical engineers have developed a method for bringing the benefits of optical interconnection to electronic circuitry: the Optobuss electrical/optical interconnection system.

Developed and patented by William Batina, president, and Lamar Gipson, vice-president, of Optobus Technology (Miami, FL), the Optobuss system consists of an optical network embedded within a printed circuit board, an edge-card connector that accommodates both electrical and optical media, and a unique chip-carrier design that bridges the electrical and optical worlds. Although no Optobuss components or systems have actually been built, nor have its basic concepts been tested, the Optobuss system suggests some interesting possibilities for designers who are finding themselves at a dead end with conventional printed circuit board technology.

"The Optobuss system was developed as an offshoot of our research into starting a contract manufacturing company for circuit board assembly," says Batina. "We observed many industry problems with interconnecting high-speed, high-pin-count chips by means of increasingly finer printed circuit board traces with smaller spaces in between. With finer lines and closer spacing, the capacitance goes way up, which slows transmission down, and there's a greater potential for crosstalk between signal lines."

Accomplishing reliable inspection of very dense boards is also a dilemma, according to Batina.

In the Optobuss scheme, a board's data bus(es), address bus(es) and control lines are all implemented via optical fibers, rather than traditional copper traces, within a printed circuit board. Electrical traces are provided on or within the printed cir-

THE OPTOBUSS EDGE-CARD CONNECTOR

The Optobuss edge-card connector secures both electrical and optical media to a printed circuit board for distribution of optical and electrical signals as the application requires. Internal and external optical fibers mate within the connector body. Tensioned finger tabs connected to the ribbon cable mate with electrical traces on the printed circuit board.
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cuit board basically for power and ground, and wire is used for commu-
nications within each chip carrier. It’s also possible to install additional electrical highways for other functions.

Because of the inherently greater speed and bandwidth of optical transmission, says Batina, “One optical fiber may be able to substitute for an entire 16- or 32-bit data bus. In an address bus, the lower-order bits move very rapidly and the higher-order bits sometimes move more slowly, so you might want to use an individual fiber for each lower-order bit but multiple any of the higher-order bits into a single fiber.”

Fiber optic transmission also offers the familiar benefits of immunity to electromagnetic interference, electromagnetic pulses and electronic countermeasures.

**The Optobuss configuration**

The Optobuss solderless chip carrier, pressfit into a printed circuit board mating hole, consists of an opaque, molded ceramic substrate, transparent plastic side walls and an integral beam splitter. Three dice—a phototransistor, a function chip (such as a microprocessor or a memory chip) and a phototransmitter—are epoxied to the substrate and interconnected via wire bonding. Batina predicts that future ICs will incorporate the functions of all three dice into a single die.

In operation, a light pulse traveling down an optical fiber enters the Optobuss carrier through one side and hits the beam splitter, which deflects some portion of the light to the phototransistor. The phototransistor then converts the optical signal to an electrical signal that’s conducted to the function chip. Electrical signals that are output by the function IC are conducted to the phototransmitter for conversion to an optical signal that’s transmitted to the beam splitter, which then deflects it into the optical pathway.

Electrical signals output by the phototransistor can also be conducted directly to the phototransmitter for optical conversion and transmission, if so required. As an option, optical fibers can be used to focus and project the light entering or exiting the chip carrier. In addition, a pair of carriers can be sandwiched around a single beam splitter to create a bidirectional optical network.

A variation on the basic Optobuss interconnect scheme provides a novel approach to multiboard computer design: the vertical-optical interconnect. Built with a transparent top and bottom, the chip carrier could be used to transmit signals perpendicular to the plane of a printed circuit board to communicate with other boards stacked above or below it. According to the intent of the Optobuss scheme, the multiple stacked printed circuit boards would be separated by thermally conductive plates that act as heat sinks, and holes would be drilled through the plates to let optical signals be projected from board to board throughout the stack.

By offering both thermal management and a very high-speed board-to-board interconnect, the Optobuss stacked printed circuit board scheme is a perfect medium for developing gallium arsenide-based systems today, says Batina. A stacked printed circuit board system also would result in an extremely rugged design.

**From concept to finished product**

Right now, Optobuss is only a concept. Transforming it into a real-world product means problems and expense. It’s uncertain, for one thing, whether common optical fiber could withstand the high-temperature, high-pressure processing used with common printed circuit board materials. Molded printed circuit boards made of plastic or some other material would probably be most appropriate for the Optobuss scheme, according to Batina. Also, since the optical fibers must be bent to route an optical pathway wherever one is needed, he says, “The glass optical fibers we’re all familiar with aren’t necessarily the right transmission media for Optobuss.”

The Optobuss system also would require extremely tight manufactur-
ing tolerances. One reason for this would be to ensure proper alignment between the deflecting surfaces of the beam splitter and the optical fibers on either side, and between the splitter and photodiode. Also, the Optobuss system's potential for using dual electrical/optical highways, optional lenses in various locations, both sin-

Nonetheless, Batina views Optobuss as a relatively simple system. "You've got to take a close look at some recent high-performance boards," he says. "They've got 24 layers these days. That in itself creates an absolute layout nightmare, not to mention what happens in debug, test and inspection."

THE OPTOBUSS CHIP CARRIER

The Optobuss chip carrier has transparent side walls that let light pulses enter and exit. A phototransistor die converts the optical signal to an electrical signal for the chip; a phototransmitter die translates the chip's electrical output into an optical signal. If fashioned with transparent top and/or bottom walls, the carrier would also allow the implementation of interboard optical pathways.

gle and multimode fibers, uni- and bi-directional pathways, and a range of other possibilities could quickly tempt the designer into unnecessarily complex implementations. Then, too, the more complex the Optobuss design, the less tolerance it might have to minor imperfections in the actual implementation. On the other hand, however, if properly done, an Optobuss design could conceivably exploit complexity to create an implementation that's very tolerant of system faults.

Managing signal timing in Optobuss wouldn't be an easy feat either, because of its built-in redundancy. Since a light pulse entering the chip carrier is only partially deflected by the beam splitter, an attenuated version of the signal passes through to the next chip in the optical pathway, creating the potential for contention problems. Then, too, if the electrical signal output by the phototransmitter is conducted to the phototransmitter as well as to the function chip, another version of the signal enters the optical pathway.

Another potential problem with Optobuss is that optical-to-electrical and electrical-to-optical conversions within the chip carrier would introduce a certain amount of delay, albeit trivial compared to the overall speedup. Also, if parallel data is serialized for transmission over a single fiber, this would inject a degree of delay. Furthermore, the light lost because of this partial deflection could become a problem. "It might become significant if you're trying to communicate over several kilometers," Batina admits, "but for several inches or centimeters, it probably won't be a problem." It's also possible, he adds, to construct a half-silver-type mirror splitter that would deflect virtually all the light that hits it.

Mixed response to Optobuss

Industry spokespersons have expressed mixed reactions regarding the Optobuss scheme. Chuck Richardson, director of the Surface Mount Technology Association and vice-president of manufacturing at Micro Industries (Westerville, OH), sees some appeal in the scheme. "We've been hearing about all kinds of wild things being done with printed circuit boards lately, including a scheme to place components in pre-cut grooves," he says. Like the mating holes for Optobuss chip carriers, these grooves are intended to simplify the placement and alignment of fine-pitch devices, a procedure that, according to Richardson, tends to be "very critical, difficult and expensive. I wonder about the yield and, hence, the cost associated with Optobuss boards, considering the difficulties we now have with printed circuit board houses dealing with pretty straightforward things."

Michael Hayward, president of Hybricon (Ayer, MA), thinks the notion of an optical interconnect between boards is somewhat premature, although he mentions that some companies have successfully used optical transmission to interconnect backplanes in different chasses. "The market for optical transmission of signals was supposed to take off for about 15 to 18 years now, but it hasn't," he says. "It may make sense for very specific applications where it would allow the size of the equipment to be materially reduced, but otherwise it would require deviation from existing bus standards, so there would be no open-market boards available for it. Even if it offers significant advantages, such a scheme will take a long time to take off."

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AI techniques enter the realm of conventional languages

Artificial intelligence techniques promise to provide the built-in cleverness needed to run the complex systems of the future. But most system developers have been frustrated by the difficulties of implementing these techniques. Coding AI in conventional languages such as C or Ada is, to say the least, arduous. Although AI-oriented languages, of which the best known are Lisp and Prolog, offer much simpler programming for AI functions, they also have discouraging faults. Code execution is slow with these languages, and demands for memory are extensive.

Although Lisp and Prolog vendors initially considered their products to be superior replacements for conventional languages, users haven’t been drawn to these languages as vehicles for developing complete software systems for large applications. Instead, most Lisp and Prolog vendors and users now stress the ability to embed intelligent modules, developed in these languages, within conventionally coded systems. Restriction of Lisp and Prolog to narrower use has been further defined by developers of AI tools, who have discovered that, despite the difficulties, it can often be worth the effort to use conventional languages to implement AI functions.

If a workable strategy to extend the use of Lisp and Prolog beyond the present limited group of devotees exists, it probably lies in encouraging the development of AI modules, written in these AI-oriented languages, which can be linked into conventionally coded systems. “We recognize that Prolog isn’t a universal language. It won’t solve all applications problems, but Prolog-coded routines can be useful in many applications systems,” says Johnathan Grayson, a member of the technical staff at Expert Systems International (Philadelphia, PA).

In the future, according to David Bowen, manager of Prolog technology at Quintus Computer Systems (Mountain View, CA), the Prolog language will have to synchronize more closely with conventional software tools because users are becoming more interested in adding Prolog subroutines to conventional language programs than in doing complete applications in Prolog. At present, C can be called from Quintus Prolog, and there’s an interprocess library package that lets a running Prolog process be called by a separate C process. There’s still no general mechanism for calling Quintus Prolog...
The ProWindows display from Quintus aids users of Quintus Prolog during software development. The application flow diagram (upper left) can be altered by using display buttons that call for help information, load new diagram scripts, add nodes and change connections between them. The Object Registry Browser window displays defined lists of existing objects, while the Available Classes window displays a scrollable list of available classes. Users can both send and receive messages about these objects through the Dialog window (lower right).

The Main window of this development display from Arity lists a game program written in Prolog. (Output can also be displayed through this window.) Execution of the program is shown in the box labeled Towers of Hanoi. Working on a line of code in the Debugger window, the user has popped up a command box through which that portion of the code is being re-executed. From the menu bar below the screen title, users can select function keys to pull down additional windows for editing, reading in files, adjusting the size of existing windows or working with DOS.
"Interfaces to other languages are becoming increasingly important," says Richard Gabriel, chief technical officer at Lucid (Menlo Park, CA). Gabriel notes that C, Pascal and Fortran are all being used in conjunction with Lisp, and that many Lucid Common Lisp users are now embedding AI functions within conventional software. To make this worthwhile, users must be able to call into and out of Lisp to the other language with little or no penalty in time and effort.

"Initially, Lisp provided inadequate means for interfacing to other languages," admits Gabriel. The company then developed a data-structure description language that describes foreign data structures in a declarative way. This lets Lucid Common Lisp construct and recognize such data structures. These structures are known to the Lisp garbage collector, which is a routine that makes memory available by clearing out infrequently used material.

The interface between the languages doesn’t create objects that will be discarded by the garbage collector. C and other procedural languages have stack frame formats that are radically different from that of Lisp. Lucid’s approach lets Lisp and foreign language stack formats coexist. Lucid software also ensures that Lisp-style interrupts can be correctly processed by C code. Since C and Lisp must share the same address space, Lucid Common Lisp understands malloc and other C procedures for allocating storage.

The ability to move easily between a declarative AI language such as Prolog or Lisp and conventional procedural languages, combined with the ability to prepare linkable AI language modules, is the wave of the future, according to Gabriel. This approach lets developers use AI techniques in conventional software systems without making a large commitment to AI technology, since AI segments can be imported into existing or planned systems.

Effective prototyping tools
If Lisp and Prolog can extend their usefulness by serving as tools for developing embedded AI, system developers will become more familiar with these languages and may discover that they also have virtues as prototyping tools.

One of the problems with development of large systems is that conventional software preparation, and modification to meet changing requirements, can take a very long time. To speed the process, many developers now write a preliminary prototype program as soon as the fundamental languages used to develop expert system tools. But amid the excessive growth of expert systems technology, and the less-optimistic recent expectations, there’s been a subtle but broad move away from AI in favor of conventional languages, such as C and Pascal.

As Citrenbaum sees it, this trend is based on the fact that the AI user community is moving out of the research labs and into real-world applications. He points out that most conventional languages have recursive functionality and other basic features needed for expert system development. Whether the language

| Space station system troubleshoots with embedded AI |

A good example of embedded intelligence is the Mission Information Data Analysis System (Midas) for a planned U.S. space station, according to Ronald Citrenbaum, chairman of Abacus Programming (Van Nuys, CA). Midas takes in telemetry data and monitors for fault summary messages coming from space. The system’s objective is to let users identify, locate and solve problems as they arise.

When an expert system like the one in Midas interfaces with traditional data-retrieval facilities, it’s possible for users to make their queries in terms of their problems, without having to know where or how the stored data is organized. In response to a query about a malfunctioning subsystem, for example, Midas might reply that there are three probable areas of trouble. The user could then choose one of those areas, and Midas would display any data from that area that wasn’t within normal ranges. Midas would also comment on the current behavior of the system, compared to its expected behavior, and on related problems that had been encountered in the past. This kind of interactive troubleshooting, based on a large data base, is comparable to discussing problems with another person.

In a conventional data base configuration, there might be an operating system, a data-management system such as R-Base and application programs written in C. The application programs would call material from the data base and, if outside expertise was needed, a user interface would handle the interaction. With embedded intelligence, expert system software emulates the human expert in guiding the work of the overall system. A protocol interface is used to link the expert system to the applications code and the data-management system.

The Abacus Programming expert software for Midas resides on personal computers and is written in Pascal. Information on components and black boxes is stored in a 30,000-record data-tape data base. The Pascal programs interface with an R-Base relational data base, which controls the data-tape data base. Associated with the R-Base is a large program, written in Arity Prolog, which provides information about the meaning of the data. Midas users key in questions directed to mission problems. The AI embedded in the system translates this user input into a query through R-Base to find relevant data, and then displays the results through the Pascal software.

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**AI LANGUAGES**

is Lisp, Prolog, C, Pascal or Ada, it can be used to develop reusable AI subroutines. During the next few years, Citrenbaum expects to see many Ada-based tools developed for AI applications.

Nexpert Object, an expert system development tool from Digital Equipment Corp (Marlboro, MA), for example, is written in C for VAX systems. Other similar expert system development tools, including the S.1 from Teknowledge (Palo Alto, CA), KES from Software Architecture and Engineering (Arlington, VA) and Rulemaster from Radian (Austin, TX), are also written in conventional code. Now that expert system techniques have become well defined, the needed modules can be readily coded in conventional languages. While it’s true that such modules can be built more rapidly in Lisp or Prolog, they will run more slowly.

In fact, vendors of AI-oriented languages make no bones about their slowness and even willingly offer speed estimates. Allegro Common Lisp from Coral Software (Cambridge, MA) is about half as fast as C, according to Andrew Shalit, software engineer. Shalit says that Lisp slowness can be particularly evident when run-time libraries are used, since storage paging tends to be inefficient. Quintus’ Bowen estimates that a typical Quintus Prolog application will run about four times slower than the same application written in C. He notes that execution speed

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**We recognize that Prolog isn’t a universal language.**

—Johnathan Grayson, Expert Systems International

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of Prolog code, when symbolic information is being manipulated, now runs about half as fast as C. This fourfold slowdown is due to the fact that Prolog is even slower for arithmetic computations. Lisp or Prolog vendors seem unable to predict when, if ever, Lisp and Prolog code will run as fast as equivalent C code. Meanwhile, since user choices of one version versus another of these AI-oriented languages is still mainly influenced by speed, vendors are striving to improve these codes to optimize their speeds.

**Optimizing AI speeds**

About a year ago, Arity found some mistakes in the traditional model it had used for Prolog compilation, known as a Warren abstract machine. Since then, a new Arity compilation model has been developed that analyzes Prolog code in unique ways. Arity Prolog is much faster in execution than competitive versions of Prolog, according to Gabriel.

Prolog code consists of clauses within predicates (procedures). During compilation, indexing is performed to find the desired clause. Traditionally, when a clause is compiled, a lot of time is spent optimizing the head of the clause, or the material before the “if” in the clause. The body of the clause is then compiled as a series of calls. The new Arity compilers take a more powerful approach, which considers the entire clause and the entire predicate when making optimization decisions. Arity also uses optimizations that deal with calls to predicates. With this broader view, additional worthwhile optimizations come into play.

New optimization techniques developed for Allegro Common Lisp RISC versions, from Franz (Alameda, CA), also take a broader view of the source code. The intermediate code form used in the RISC compilers lets optimizations be performed based on data-flow analysis. Instruction scheduling implements optimizations that take advantage of delays after branch instructions. When users declare that numbers are floating-point, special floating-point optimizations are invoked by the compiler.

AI vendors are also offering users added control over optimization. For example, in GC Lisp from Gold Hill (Cambridge, MA), there’s a proclamation statement that lets users specify degrees (one to four) of speed and code-size optimization, as well as optimization safety. Typically, when code is first being developed, safety is set high, so errors will be readily caught for debugging. Once the code is developed and debugged, optimization safety can be set lower to generate faster, more efficient code. Users can hope that no added bugs will be
introduced by this setting. Users of Allegro Common Lisp can set the compiler for maximum run-time error checking and for speed, with settings from one to three for each. Users can also decide which compiler functions will be invoked or bypassed by different settings.

If the user throws the right switch, the Lucid Common Lisp compiler can report on which optimizations could and could not be done. Such information can be valuable to developers seeking to improve their code. Lucid is working to further improve this capability, according to Gabriel.

Vendors are also striving to find ways to limit Lisp's appetite for memory, mostly by reducing the number of Lisp language functions kept in memory. The undesirable side effect, however, is sometimes slower execution. Another approach to limiting this need for memory is to use shared dynamic libraries of Lisp software, similar to those provided by Unix. Techniques are being developed at Lucid to link together Lisp and conventional code segments for these libraries. Since few libraries for Lucid Common Lisp have been produced, the development process includes recoding Lisp code segments into library-usable formats.

If Lisp and Prolog can capture the allegiance of a large number of developers who wish to incorporate AI modules in larger, conventionally coded systems, these languages have a promising future. Programming and maintenance of existing programs in these languages seem to call for less effort than do conventional languages. Undoubtedly, Lisp and Prolog seem to be superior vehicles for developing AI implementations. But until the drawbacks of sluggish execution and significant memory demands are overcome, prospective users will continue to be diverted from investing in these AI-oriented languages and will postpone their use of AI techniques.
Sharing design data through networking

Bill Harding, Contributing Editor

Engineering managers find that the benefits of CAE/CAD networks are more clear-cut than the implementation as they work to link diverse sets of computing resources.

With engineering work groups communicating via yellow Ethernet cables, twisted-pair phone lines, fiber-optic cables, satellite links and floppy disk "walknets," engineering networks occupy a position equal to engineering computers. A network populated with compatible workstations and compute servers supplied by a single vendor and that runs compatible CAE/CAD software seldom presents any networking problems to its users. The problems arise when incompatible computing machines running incompatible CAE/CAD software from a number of vendors attempt to coexist on the same network. Of course, such a situation would be avoided if the network were planned before workstations or software were acquired.

But no network, it seems, has ever been planned. Virtually all network users and all CAE, workstation and network vendors share the same opinion: networks evolve. And they evolve using a wide variety of computing resources—from mainframes to minicomputers to personal computers to engineering workstations to special-purpose computers. A network grows by adding to existing resources, not by discarding anything that's already in place. Although starting over would be much easier from a technical point of view, doing so would be impractical.

Since engineering managers constantly face the question of how to expand existing resources or how to bring divergent resources together, the status of networking today must be examined, with special focus placed on the options open to the engineering manager who must expand or enhance an engineering network.

I The evolution of networks

The evolution of computer capability and the plunging prices of computing power are major influences on today's networks, reversing the computer-to-user ratio that existed in the late 1970s and early 1980s. The earliest networks could be characterized as one computer with many users; a single mainframe or large minicomputer served a number of users who accessed the system via interactive terminals. The arrival of low-cost PCs and powerful engineering workstations resulted in a trend toward one computer with one user. Today, with special-purpose computers and compute servers on the network, the typical network has many computers for each user.

As networks moved from one stage to the next, however, users weren't willing to give up what they already had in place. The one-computer/many-users environment of the early 1980s usually consisted of time-shared, interactive applications running on IBM mainframes or DEC VAX computers, accessed through individual user terminals. Sometimes the network would contain both IBM and DEC computers, with occasional large Crays, loosely coupled via remote job entry or SNA.

When powerful engineering workstations came onto the scene in the mid-1980s, the tendency of the engineering community was to add workstations and PCs to the existing time-share environment. But engineers weren't willing to give up their mainframe capability. They knew how it worked, they trusted it, and all of their applications were there. New applications could go on the workstations and old ones could eventually migrate there, but the mainframes would stay in place.

To paraphrase Parkinson's Law, designs will grow to fill the capacity allocated to their creation. Today's huge designs have taxed the capacity of engineering workstations, which has led to the introduction of special-purpose computers and very power-
ful compute servers. But these compute servers and special-purpose computers probably come from different vendors; thus, the software tools aren't compatible. In addition, more engineers must work on the same design and access the same data, which creates a need for better communication between systems. So networks filled with mainframes, workstations, PCs, compute servers and special-purpose computers bring us to the one-user/many-computers ratio that we see today.

**Deciding on functions**

When faced with networking options, you must ask yourself what you want from your network. Do you want that great design team in Europe to work with your local team on some new projects? Do you want to send fully simulated designs to a plant in Asia for fabrication? Do you want all the engineers in your local design group to have access to the engineering department's new simulation accelerator and file servers? Whatever your reasons, they probably boil down to two things: communications and resource sharing.

Communications involves everything from passing a message via electronic mail to transmitting a cus-
CAE/CAD NETWORKS

tom chip design from a design center to a foundry's fabrication facility. Designs can pass from one engineering workstation to another over an engineering department's local network, or they can be sent around the world through a hierarchy of networks.

Resource sharing, on the other hand, is more likely to be a localized function. Compute servers and special-purpose computers tend to be departmental rather than company-wide resources. Local cluster file servers may be used to store files on large disks in one central location, allowing for easy backup but maintaining fast and simple access for those who need the files.

Most engineering networks today use Ethernet for the physical process of moving bits and bytes, and Transmission Control Protocol/Internet Protocol (TCP/IP) to control that movement. While Ethernet's capabilities are improving and Ethernet is retaining compatibility from version to version, the same isn't true for the software protocols.

Ethernet standards are controlled by the IEEE 802.3 standards committee. Over the years, that committee has defined a series of standards, ranging from the ubiquitous yellow cable that implements 10BASE5 Thick Cable Ethernet, to 1BASE5 StarLAN. All of the standards have a bandwidth of 10 Mbits/s, except StarLAN, which has a bandwidth of only 1 Mbit/s.

StarLAN received much notice because it can carry Ethernet communications over unshielded twisted-pair telephone lines, according to Rich Brand and Balakrishnan, National Semiconductor (Santa Clara, CA) delegates on the IEEE 802.3 committee. Since most companies have extra twisted pairs in their phone systems, Ethernet can be run over phone lines without pulling expensive yellow cable. After all, the 10BASE5 Thick Cable costs upwards of $1.50/ft, but twisted pair is effectively free since it already exists.

But StarLAN's 1-Mbit/s bandwidth limitation, and the need for an expensive bridge to connect a StarLAN network to any 10-Mbit/s Ethernet backbone, is cooling that enthusiasm. Studies have shown that maximum usage of an Ethernet network with a 10-Mbit/s bandwidth is typically in the 30 to 40 percent range. Thus, a 10-Mbit/s network is unlikely to experience an overload condition; a 1-Mbit/s network, however, is in a constant overload condition.

A proposed standard—10BASET—for a 10-Mbit/s Ethernet protocol that will work over unshielded twisted-pair current is before the 802.3 committee. 10BASET is getting a lot of attention, even in preliminary committee meetings, according to Brand and Balakrishnan, because it can run over the same unshielded twisted-pair phone lines as StarLAN, but at a 10-Mbit/s rate. And, with a 10-Mbit/s bandwidth, it requires a much less expensive connection to 10BASE5 backbone networks.

Another standard—10BASEF—is being proposed for connecting Ethernet to fiberoptic networks. The proposed implementation of the standard, for which IEEE approval is still about two years away, would let users upgrade it to the 100-Mbit/s Fiber Distributed Data Interface (FDDI) methodology. However, since the controller board at each node costs about $200,000, FDDI can be quite expensive.

Ethernet vs. token ring

Ethernet, however, isn't the only game in town. IBM offers Token Ring, and Apol (Santa Clara, CA) offers Domain, also a ring network. Rings offer advantages over Ethernet, particularly when network usage gets very high.

Ethernet is a contention-based network; every node has equal access to the network at all times, according to Wes Hilton, manager of integration products at Computervision (Bedford, MA). If two nodes try to transmit at the same time, a collision occurs. When network usage exceeds about 75 percent, the node that wins the randomizing routine to get out of sync, and try again. This can cause problems, notes Hilton, but only when network usage exceeds about 75 percent, and most engineering applications don't reach that level.

Collisions can occur on token-ring networks, since only one node can ever attempt to transmit at one time. In this type of network, a token is passed around the ring. If a node wants to transmit, it takes the token, thereby preventing other nodes from also transmitting. If it doesn't want to transmit, the node passes the token to the next node.

Response times are more predictable in a token-ring network than in an Ethernet network, making the token-ring adaptable to applications where response time is critical. A token-ring network, however, is more sensitive to system failures within the network, since the failure of one system could break the ring. Ethernet networks, on the other hand, are much more sensitive to system failures within the network, since the failure of one system could break the ring.

Early networks grouped users around a single computer in a timeshare environment. Workstations and personal computers brought engineering power to the individual engineer's desk. Networking today lets a single user have access to a wide range of computers.

"OSI is supposedly a standard, but it's not here yet."

—Bob Davis, Excelan
Networking: a glossary of terms

The networking world has a language all its own, with heavy use of acronyms and abbreviations. The following are some of the more common terms.

**Backbone** The primary organizational network that ties systems and other networks together.

**BSD** Berkeley Software Distribution. Networking protocols developed at the University of California at Berkeley for use with Unix.

**Bridge** A hardware link that connects two similar networks, such as two Ethernet networks.

**Ethernet** Defines the Physical (Layer 1) and Data Link (Layer 2) levels of the OSI Reference Model (see OSI Reference Model).

**FDI** Fiber Distributed Data Interface. Fiberoptics LAN standard that operates at 100 Mbits/s.

**Frame** The Ethernet communications "packet" that moves information across the physical link from one Ethernet node to another.

**FTAM** File Transfer, Access and Management. The OSI standard for multivendor file access and transfer. It competes with NFS (Sun's Network File System), which is the equivalent de facto standard under TCP/IP.

**Gateway** A hardware link that connects two dissimilar networks, such as connecting Ethernet to IBM's SNA.

**ISO** International Standards Organization. The international organization that's defining the OSI standards for multivendor networking.


**MAP** Manufacturing Automation Protocol. Specifies networking protocols for manufacturing; a subset of OSI protocols.

**Network** The physical link and control software that lets data be transferred between systems.

**WAN** Wide area network. A network that connects systems over long distances. Distances can be a few miles or thousands of miles. With satellite links, WANs frequently provide worldwide communications.

**LAN** Local area network. A network that operates over relatively short distances (typically no more than two or three miles), linking systems within the same building or in nearby buildings.

**SAN** Small area network. Generally limited to short-range (tens of meters) special-purpose communications functions, such as process-control systems and real-time applications.

**Network manager** A "traffic cop" that handles the flow of data within a network.

**NFS** Network File System. A method developed by Sun Microsystems for organizing and managing file transfer over a network. Currently adopted by well over 100 computer vendors.

**OSI Reference Model** A seven-layer communications protocol model proposed by the ISO; sometimes referred to as the ISO/OSI Reference Model (OSI stands for open system interconnection).

**Layer 7: Applications Layer** Provides the interface between applications programs and the network.

**Layer 6: Presentation Layer** A translation function that converts messages from a native format to an international standard format for transmission, and from the international standard to the native format upon reception.

**Layer 5: Session Layer** Establishes communications paths between systems and terminates them upon completion of transmissions.

**Layer 4: Transport Layer** Provides reliable data flow between sender and receiver. This layer corresponds to the Transmission Control Protocol (TCP) function in the TCP/IP methodology.

**Layer 3: Network Layer** Accepts packets (or frames) of data from the Transport Layer and routes them to their destination over all necessary links and intermediate systems as necessary. In the receiving system, this layer simply passes packets to the Transport Layer. Layer 3 corresponds to the Internet Protocol (IP) level in the TCP/IP methodology.

**Layer 2: Data Link Layer** The interface between hardware and software layers. This is a hardware layer that formats packets for transmission and ensures that they're properly received at the other end. In the receiving node, the Data Link checks packet address fields to see if the local node should receive the packet.

**Layer 1: Physical Layer** The actual connection to the transmission medium, handling the transmission and reception of raw bits across the medium.

**RJE** Remote Job Entry (or Execution).

**SNA** Systems Network Architecture. IBM's proprietary networking format.

**TCP/IP** Transmission Control Protocol/Internet Protocol. The de facto standard for communicating via Ethernet, corresponding to Layers 3 and 4 of the OSI Reference Model.

**Token Ring** Endorsed by IBM, it's emerging as the de facto standard for networking PCs.

**TOP** Technical/Office Protocol. A subset of OSI protocols, similar to MAP, for engineering and office applications.

**UUCP** Unix-to-Unix Communications Protocol. Commonly used for electronic mail within the Unix community, including universities on public networks.

**X.25** A standard adopted by the ISO for wide area networking, as opposed to local area networking. It involves layers 1, 2 and 3 of the OSI model.

**X.400** A standard adopted by the ISO for electronic mail handling over a multivendor network.
The IEEE 802.3 standards committee has defined the following four Ethernet standards:

**10BASE5** Known as Thick Cable Ethernet. 10 Mbits/s, baseband, 500-m range. Can be identified by the yellow Ethernet cable.

**10BASE2** Known as Thin Cable Ethernet (or Cheapernet). 10 Mbits/s, baseband, 200 m. Runs on a 50-Ω shielded cable. Its major attraction is its lower-cost cable, about 104/ft (compared to about $1.50/ft for Thick Cable).

**10BROAD36** 10 Mbits/s, broadband, 3,600 m. Provides much longer range than both 10BASE5 and 10BASE2 and will run on any broadband cable plan.

**1BASE5** Known as StarLAN. 1 Mbit/s, baseband, 500 m. Twisted pair. Networking 10-Mbit/s Ethernet with 1-Mbit/s StarLAN requires an expensive bridge. StarLAN is losing its luster with the pending approval of the 10BASET standard.

The following aren't yet IEEE 802.3 standards but are under development by the IEEE 802.3 standards committee:

**10BASET** 10 Mbit/s, baseband, twisted pair. The majority of the 802.3 committee work is going on here. This standard, once developed, will allow 10-Mbit/s Ethernet over existing telephone wires. Since it's 10 Mbit/s, it can work with a 10BASE5 backbone without an expensive bridge. It should be ready for design in six to nine months, with the official IEEE stamp of approval in 18 months.

**10BASEF** 10 Mbit/s, baseband, fiberoptics. This proposed standard is in the early stages of development, and it will be about 12 to 18 months before design efforts can be started, and over two years before IEEE approval. There's some controversy revolving around passive hub architecture vs. active hub architecture. The cable plan for 10BASEF could be used for the higher performance Fiber Distributed Data Interface so that users who need even higher performance could upgrade in the future.

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**IEEE 802.3 Ethernet physical standards**

The backbone of a typical network implementing the 802.3 Ethernet standard is the 10BASE, or Thick Cable, standard. Workstations connect to the backbone via a repeater and to each other using 10BASE twisted-pair phone lines. Shared peripherals connect to the backbone via a repeater and to each other via 10BASE2 Thin Ethernet.

Source: National Semiconductor

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The whole purpose of networking is to let systems communicate and share resources. At the physical level, systems can be connected to form networks, similar networks can be connected by bridges, and significantly different networks can be joined by gateways.

Since the early 1980s, TCP/IP has been the de facto standard for communicating over heterogeneous Ethernet networks. First introduced in the 1970s by the Department of Defense, TCP/IP gained commercial acceptance when it was incorporated into the Unix 4.2 BSD kernel in 1982, and later when 4.2 BSD linked TCP/IP with Ethernet. Since then, TCP/IP has grown in strength.

In 1984, before TCP/IP became popular, the International Standards Organization (ISO) proposed a seven-layer protocol called the ISO/OSI (open systems interconnection) Reference Model. The OSI model addressed many of the issues that plagued networks at the time of its early definition. A hot issue in the networking community today concerns the migration to the OSI standard from TCP/IP.

Bob Davis, product-line manager at Excelan (San Jose, CA), for one, questions such a migration. "OSI is supposedly a standard, but it's not here yet," he says. "TCP/IP is the least common denominator when trying heterogeneous networks together; it's a de facto standard; it's here now; it's mature; and it's rapidly filling all of the gaps that OSI supposedly addresses."

One OSI strength is its File Transfer, Access and Management (FTAM) facility, through which it addresses file access across a network. FTAM has specifications that are better, particularly in the area of electronic mail, than those of the Network File System (NFS), the equivalent de facto standard in the TCP/IP and Unix worlds. NFS, which was developed by Sun Microsystems (Mountain View, CA), has been around for several years, however, and is constantly being improved.

So, while some of OSI's features appear to be somewhat better than those of TCP/IP, it's unlikely that OSI will soon replace TCP/IP, if ever.
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The question, according to Davis, shouldn't be one of replacing TCP/IP with OSI, but of running both at the same time on the same network.

Excelan's strategy is to run both on the same network by providing controllers that automatically and transparently determine whether a command or message uses the OSI protocol or the TCP/IP protocol. Excelan customers can replace TCP/IP with OSI, or both protocols can continue to run on the same network.

"The network is the computer"

Network vendors and workstation vendors have recognized the movement to heterogeneous networks and have developed their networking strategies and products accordingly.

"The network is the computer," states Sun Microsystems in a trademarked phrase. To support this contention, Sun developed the Open Systems Network (OSN) philosophy, designed not only to let diverse systems work together in a single network, but to also make the entire network look like a single computer to the user. OSN is made up of two parts: open network computing (ONC) and a network/extendible window system called X.11/NeWS, which is a merging of Sun's NeWS windowing system and Version 11 of the X Window System.

ONC is designed to address three networking problems: resource access, application design and development, and network administration. Through a layered process, ONC lets users access any network resources, from simple files to special-purpose computers, as if the resources were resident on the user's local computer.

At the top of the ONC hierarchy is the applications level. One such application is Sun's NFS, which is rapidly becoming a standard in its own right. NFS provides the ability to access files anywhere in the system and to let different computers share files. Vendors also may develop applications at this level.

Just below the application level is a remote procedure call (RPC) facility, which accesses remote resources and executes portions of an application on another network system.

Below the RPC level is a parameter translation level called XDR (external data representation). At this level, data can be passed between machines that use different data representation formats.

The second part of OSN, X.11/NeWS, can be distributed anywhere on the network, since it's independent of operating systems, hardware and screen resolution. Sun's aim is to make X.11/NeWS a network resource, just like a piece of network hardware.

The last piece of the puzzle

Hewlett-Packard's Colorado Networks Division (Fort Collins, CO) bases its Advancenet on the idea that a network starts with a mainframe, possibly a minicomputer, and some PCs in place. "When you add engineering workstations to the network, you must first ensure that the existing network is still functional," says Dave Morse, HP's engineering solutions manager. "You must provide file-transfer capability to move files back and forth, and you must provide a terminal emulation mode to maintain access to the applications on the mainframe."

One motivation for moving out of the time-share environment, according to Morse, is to take advantage of the competition in the computer market. Adopting a networking scheme that's vendor-specific defeats that purpose, he says, so users should stick to standards that let them take advantage of the most cost-effective engineering solutions available.

Advancenet supports what HP considers to be the dominant standards in networking: the OSI Reference Model and IBM's SNA. It supports both the original Ethernet and the more recent IEEE 802.3 specification at Layers 1 and 2 of the OSI Reference Model. Advancenet also includes HP StarLAN and HP StarLAN 10 for LANs; IEEE 802.4 for ARPA (the Department of Defense's Advanced Research Projects Agency) and MAP (Manufacturing Automation Protocol) networks; and the HP Private Packet Network, which is based on the X.25 standard.

Like HP, Apollo focuses on the fact that networking is considered only after all the other pieces are in place. "Networking is the last frontier of

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**Sun Microsystems' Open Systems Network (OSN) supports a heterogeneous network** (a). It works on the premise that a network must build on any existing installation and be compatible with future installations. Major components of OSN (b) include Sun's open network computing (ONC) and a window system, X.11/NeWS, which is a merging of X Window System Version 11 and Sun's NeWS.
Distributed fault simulation elicits supercomputer performance from CAE network

Networks of CAE workstations aren't limited to the tasks originally envisioned for them. They can also be used as loosely coupled parallel processors that can cost effectively reduce the run time of compute-intensive operations.

Accurate fault simulation is one operation that can benefit from such parallel-processing schemes and is therefore contributing to an industry trend toward more effective use of network resources. Verifault-XL, the latest fault-simulation product from Gateway Design Automation (Westford, MA), for example, can run on networks of standard workstations, achieving an almost linear reduction in processing time as network workstations are added.

Designers use fault simulation to determine the efficacy of sets of test patterns that they've developed using a logic simulator. The test patterns, if proven adequate, can then be used in manufacturing and field-service test equipment. Unfortunately, large numbers of circuit nodes (and hence potential faults) coupled with the large numbers of test patterns necessary to exercise the nodes can make fault-simulation execution quite slow.

Random fault sampling

Statistical fault-simulation schemes can quickly provide a rough indication of the effectiveness of a set of test patterns. Verifault-XL, for instance, includes a random fault-sampling feature that lets users simulate only a small percentage of the total number of possible faults. Obtaining full confidence in a test-pattern set, however, requires an accurate, deterministic fault simulation.

To perform such a simulation, a fault simulator must be able to simulate a stuck fault (that is, a permanent logic 1, 0, or for MOS circuits, open condition) at each circuit node. The total time required for fault simulation is dominated by the "F x T x P" time, where F is the total number of faults to be simulated, P is the total number of patterns, and T is the average time required to simulate a faulty machine for each pattern.

For circuits of even moderate gate count, fault simulation, therefore, is computationally intensive. One 6,600-gate circuit evaluated by Gateway exhibited 23,741 faults. Achieving 68 percent fault coverage of this circuit required 104 test patterns.

Hardware accelerators have provided one means of speeding up accurate, deterministic fault simulation, but to use them, you must buy expensive, dedicated equipment. In contrast, if you use an existing network of general-purpose workstations to run a distributed fault-simulation package, the hardware is essentially free because fault simulation can run on the network at night.

Parallel-processing tasks

The operation of Verifault-XL illustrates how networked workstations can accomplish parallel-processing tasks. Verifault-XL lets multiple workstations work in parallel on a single simulation. For logic circuits of 1,000 gates or more, adding additional workstations results in a nearly linear reduction in run time despite the overhead associated with interprocessor communication.

To run Verifault-XL on a network, the user interfaces with a parent processor, which serves as the user's single point of entry and exit. The parent processor (which may be any workstation in the network) accesses the circuit model and stimulus vectors for the circuit to be simulated. Next, the parent passes circuit information on to several children processors, designated by the user.

Each processor (including the parent) then performs fault simulation on the entire circuit for a unique, nonoverlapping subset of the total fault set. This step essentially divides the dominant F x T x P time by the number of workstations available for distributed processing. The time spent modeling and post-processing and the total time spent simulating a good machine for each pattern also add to the total fault-simulation time.

When each processor finishes its simulation, it returns summary information to the parent, which merges the simulation data from all processors into a results file. The user gets supercomputer performance from a network of standard workstations.

Prabhu Goel, PhD, president, Gateway Design Automation

computing," says Bob Chiras, networking marketing manager at Apollo. "We get to the user last, after most of the computing decisions that have made, so we have the least influence on the user's environment. The networking vendor's job is to coexist with the decisions already made and to make the user's investments in connectivity correct."

Apollo's networking offerings span the full range of commonly used protocols and network configurations, including Ethernet 802.3 and the Apollo Domain ring.

For application development, Apollo's Network Computing System considers the engineering workstation the integration point, or unifying technology, for network computing. It provides the foundation for a heterogeneous network that supports distributed applications and services across one network or a group of interconnected networks.

The networking goal of Digital Equipment Corp (Maynard, MA) is to
Networking innovations maximize CAE/CAD performance

The growing need to proliferate CAE/CAD resources among as many engineers as possible has driven the demand for affordable desktop workstations. At the same time, CAE/CAD applications' hunger for computer performance is greater than that of almost any other class of software, and the graphics- and compute-intensive nature of CAE/CAD is continuing to increase. These factors have pushed computer hardware to its performance limits. Through networking innovations, however, the CAE/CAD environment can reach effective performance levels at the right price.

"Networking innovations" refers to the creation of a cost-effective CAE/CAD environment that satisfies the computer-performance requirements of the different stages of the design cycle. Digital simulation requires the highest CPU (or Mips) performance. Design capture and CAD applications require the maximum level of graphics performance. And analog simulation and printed circuit board routing require very high floating-point performance (Flops). Because no one affordable workstation can meet all of these CAE/CAD requirements, the compute environment must consist of a variety of resources linked transparently via a network.

One method on which to model a networked CAE/CAD environment is the desktop/server approach—the approach taken by Daisy Systems (Mountain View, CA). Graphics-intensive activities such as schematic capture, simulation analysis and printed circuit board design are supported on the desktop computer. CPU-intensive and floating-point-intensive activities are allocated to specialized resources shared over the network, such as hardware accelerators and high-Mips servers, respectively. This approach provides the individual engineer with low-cost, dedicated computer power on the desktop as well as access to more expensive computer resources that are shared with other design team members.

To give the engineer the ability to interact with the accelerator or server as if the applications were running on the desktop workstation, Daisy has developed a specialized communication protocol called Inter-Process Communication (IPC). Because it's optimized for the CAE/CAD environment, IPC provides a high level of functionality.

IPC is a Session Layer protocol (Layer 5 in the OSI model), optimized to establish cooperation between applications running on Daisy workstations and those running on accelerators and servers. IPC runs on the industry-standard Transmission Control Protocol (TCP). Daisy's IPC protocol is used typically by engineers sitting at a workstation running a digital simulation on a Megalogician or Gigalogician accelerator. The accelerator implements the actual simulation algorithm in microcode at speeds greater than those of general-purpose computers. With the IPC protocol establishing and maintaining a link between the accelerator and the desktop workstation, the engineer can interact with the simulation in real time with little thought that the simulation is being carried out elsewhere.

IPC also supports Daisy's analog simulation engine, DSpace, which requires strong floating-point performance. DSpace performs best on the Sun-4-based XL Server or on a VAX. For engineers running DSpace on a VAX, IPC maintains the link between the engine and the graphics interface running on the engineer's desktop.

Because of its transparency, many of the engineers who use IPC may not even realize it. But the benefits of such a communications protocol are evident. It offloads CPU-intensive tasks such as analog or digital simulations to powerful network resources, yet maintains interactivity. This reduces the CPU load on the local workstations, which minimizes cost per seat. Powerful resources are easily accessible to the entire network, which maximizes their availability and cost effectiveness.

Kevin Woods, BSEE, product manager, workstation marketing, Daisy Systems

move everyone to OSI. As a means to this end, the company announced in August its enterprise-wide networking product line. These products are designed to help integrate networks and computers throughout an organization. DEC recommends that networks be organized with local VAX clusters serving individual engineering groups, with the local cluster connected to a backbone Ethernet cable for companywide networking, an approach DEC's enterprise-wide products support.

The new product line includes communications servers, networking software and gateways that connect dissimilar networks. The DEC MicroServer is a MicroVAX II-based server that provides four times the performance of DEC's previous server. The DECrouter 2000 software connects DECnet users to high-speed telephone lines. The X25router 2000 software gives DECnet users access to wide area networks using the X.25 protocol. And the SDV11 is a high-speed synchronous interface that provides two lines that run different applications, as well as providing access to networks using the DECnet, X.25 or SNA protocols.

Supporting OSI is DEC's VAX FTAM software, which complies with ISO/OSI Reference Model specifications. Since OSI isn't yet an industry standard, DEC also supports numerous de facto standards, including TCP/IP and Ethernet.

CAE vendors provide support

Most CAE vendors prefer to let their workstation vendors or independent networking vendors provide networking hardware and software, while they develop applications that will run on those networks.

Daisy Systems (Mountain View, CA) believes that networking has three functions in the engineering environment: meeting engineering performance needs, tying members of a design team together, and tying the engineering environment to the corporate environment.

Performance needs refer to those tasks that can't be handled on the engineer's PC or engineering workstation. Such tasks would include long simulation runs, IC or printed circuit board layout, centralized file storage, and shared peripherals such as plotters and printers. Daisy's applications tend to support interactive design on the engineer's desk and batch-mode applications on servers.
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CIRCLE NO. 17
How do networks get started? The answers are as varied as the companies that use them. The examination of three networking examples illustrates the influences on network decisions.

The first example involves a giant manufacturing company that had to merge two product lines. The second involves a consulting company, but gave up consulting to pursue the design and manufacture of supermicrocomputers. The company's engineering network consists of six Apple Macintosh computers, six IBM PC ATs, a Sun workstation and an Apollo workstation. As one might surmise, the network evolved rather than was planned, but it gets the job done.

"As a consulting company, our objective was to produce thorough reports for our clients," says Douglas McTavish, vice-president and one of the founders of Clustrix. "We chose the Apple Macintosh for its text processing, spreadsheet and graphics capabilities."

When Clustrix undertook the design of its first product, it had to select design tools and the computers to run them, since few such tools run on the Macintosh. The Clustrix design philosophy, based on mainframe computer design techniques, played a major part in how those selections were made. Among these is the company's method for creating and entering designs into the design data base.

"We develop our ASIC designs as a set of equations that we enter directly into the design data base," says McTavish. "ASICs constitute about 90 percent of our design effort."

Since the ASIC design files are equations that are created and edited using commercially available text editors rather than graphics editors, it wasn't necessary to have a large number of graphics workstations. Clustrix added ATs as individual engineering stations because of their greater compatibility with available engineering tools. The company chose a suite of design automation tools from Silvar-Lisco (Menlo Park, CA), thus dictating that workstations capable of running simulators and printed circuit board design tools be part of the design environment. A Sun workstation was added to run the simulators, and an Apollo workstation was added for printed circuit board design.

The Macintoshes are connected by Apple Talk; all other machines are connected by Ethernet, with a bridge between the two. Designers can run simulations by logging onto the Sun workstation via the network and run the simulations from either a Macintosh or a PC. When it's time to move an ASIC design from the local environment to a foundry for final simulation and fabrication, the move is accomplished via magnetic tape rather than by a network link.

Networking the networks

The network at National Semiconductor (Santa Clara, CA) is what one would expect: individual engineering groups using a variety of engineering workstations are networked together within their own groups and may be supported by local NAS mainframes (National Advanced Systems' IBM-compatible computers) or VAX minicomputers. Protocols such as TCP/IP (Transmission Control Protocol/Internet Protocol) and DECnet are used to link various computers.

Local clusters are connected to the company's backbone network, which links various National facilities throughout the world. In addition, gateways provide links from the backbone into public networks.

When National acquired Fairchild Semiconductor last year, Roy McGuffin, director of design automation at National's ASIC Division, was faced with a problem: National's ASIC design network had to be merged with Fairchild's network. In addition, National's customers, using a variety of design automation tools, had to be able to work with the National foundry for the production of their ASIC designs.

National's system was based on NAS mainframes, and the Fairchild system, FairCAD, was based on VAX VMS. Both systems worked but were somewhat inflexible in how they interfaced to customers' design tools. So National decided not to simply merge the two networks. Instead the company developed DA4, a design environment that's more compatible with customer design environments and that takes advantage of existing workstation and networking standards.

According to McGuffin, the most important thing that National did was to base DA4 on existing standards, in particular on the Electronic Data Interchange Format (EDIF) standard. An EDIF "backplane" is the key to integrating diverse systems and design tools. All of the customer design tools and National design center tools plug into one side of the EDIF backplane, and the National foundry tools plug into the other side.

A design may be created and a net list generated on any CAE workstation, as long as it can produce a net list in EDIF 2.0 format. The EDIF net list then becomes the universal language for accessing all National simulation, layout and verification functions.

The giant influence

General Motors has a somewhat different problem: standardizing the way outside contractors work for GM. GM has approximately 90,000 approved subcontractors, and they produce about 80 percent of every new GM automotive design.

GM's problem is one that every engineer manages: compatibility of information. GM decided, therefore, to implement a program, called the C-3 Data Pipeline, that will provide "art to part" consistency of data generation, data transmission and data interpretation. When implemented, outside contractors will be required to provide their design inputs in an electronic format that's compatible with the C-3 Data Pipeline and therefore compatible with other design and fabrication tools. GM estimates that it will spend hundreds of millions of dollars implementing this program over the next five years.

The C-3 Pipeline is both a very large design network and a design philosophy. Cadam (Burbank, CA), a major supplier of mechanical and printed circuit board design software to GM, was selected as a strategic partner to help implement the program.

"The C-3 Data Pipeline doesn't mandate anything that we hadn't already planned," says David Brazier, director of CIM marketing at Cadam. "The whole philosophy is to apply standards that already exist in order to achieve greater compatibility and portability."
The latter two network functions relate to communications: communications among design team members working on elements of the same task, and communications between design teams and other departments such as MIS and manufacturing.

Cadnetix (Boulder, CO), like most vendors, usually integrates its CAE/CAD tools with existing customer engineering environments. But the company believes that customers have to change how they do their job. The mere act of integrating CAE/CAD tools into an engineering department should cause changes. The problem is getting both the customer and the CAE vendor to understand what those changes are.

When integrating into an existing environment, Cadnetix usually deals with the MIS department, since new computers will be hooking into the companywide network. Cadnetix provides turnkey systems with its software on Sun workstations and incorporates Sun networking tools, including NFS for file access and XDR for data compatibility.

Cadnetix has found that integrating the engineering environment into the overall corporate network runs into more political resistance than technical problems. Companies demand that paper be moved when a design is handed to manufacturing.

Electronic mail may be a first step to corporatewide networking. But MIS managers are reluctant to give nonprofessionals—that is, non-MIS professionals—access to the corporate mainframes. The managers wonder, "Will those engineers do weird things with my systems?"

But political resistance isn't the only problem. There are ample technical problems within the engineering network itself, according to William Loesch, president of Ikos Systems (Sunnyvale, CA). Ikos provides high-performance simulators, including hardware simulation accelerators, for incorporation as a special-purpose computer on a client's engineering network. The Ikos system must integrate into the client's network because Ikos doesn't offer the front-end products.

The physical process of moving bits and bytes around in a network isn't a problem, according to Loesch. Ethernet does that quite well. The problem is being able to do something with the information once it arrives at its destination.

The difficulty is caused by the way different computer architectures handle data internally, Loesch explains. A "byte-swapping" problem results, not from data in pure binary or pure ASCII, but from mixed binary and ASCII files. Since a schematic is often a mixed ASCII/binary file, with graphics information in binary and text in ASCII, a schematic started on one workstation may cause problems if edited on a different architecture, even though the applications software is from the same vendor.

Where to from here?

It looks like networks will be with us for quite some time, although the transmission media may change. Ten-Mbit/s twisted-pair Ethernet networks are probably less than two years away. Fiberoptic networks, while expensive today, will probably follow the path of all other technological advances and come down in price. And perhaps a future network will consist of portable workstations connected by cellular telephones or even satellites.

Will we solve the problems of moving information between diverse systems in a meaningful manner? The answer may lie in the recent movements toward cooperation among electronic CAE/CAD companies. The Electronic Design Interchange Format (EDIF) finally works and is being supported by several CAE vendors. And the CAD Framework Initiative (CFI) announced at the 1988 Design Automation Conference could solve many data-interchange problems.

The best advice to the engineering manager, however, is stick with the standards that exist today. You can always find a networking technology that may be somewhat better than the one everyone else is using, but what happens when you can't exploit your own network because no one supports the technology you've chosen? As one network user puts it, "Beware of the vendor who wants to control the universe!" Like it or not, networking is one area where it pays to follow the crowd.

Special-purpose and general-purpose compute servers extend the capabilities of an engineering network. In some cases, the compute server connects directly to the network. Some special-purpose computers, such as the Ikos simulator, attach to the network through an intermediate workstation.

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Caching designs eliminate wait states to relieve bottlenecks

Alternative approaches to cache architectures present a range of trade-offs in cost, performance and complexity.

Richard Gregory, BScEE

The demands that today’s high-speed processors place on main memory can’t be economically met without severe price/performance trade-offs. Designers have had to either use dynamic memory and insert wait states in CPU memory accesses or use high-performance static memory and pay a premium price. There is, however, a third alternative: A relatively small static memory cache can be added to dynamic memory to allow high average read-access bandwidth with relatively little extra cost.

By exploiting the repetitive and sequential nature of software execution and database manipulation, caching enables a small amount of very fast static memory to improve the perceived performance of sluggish dynamic memory. Memory systems incorporating cache devices can eliminate wait states for over 90 percent of all accesses and can do so at a fraction of the cost of equivalent high-speed static memory. The resulting increase in memory access bandwidth is particularly important in real-time systems, multiuser/multitasking systems, database manipulation, multiprocessor systems and any application that’s memory-intensive and time-critical.

Because cache systems increase bandwidth so efficiently, they’ve become very much in vogue. Various manufacturers provide processors with on-chip caches, chip sets to implement full off-chip caches, and cache boards that “turbo boost” existing memory systems. And one standardized bus, Futurebus, includes provision to exploit all cache features. Each variation on the cache

Richard Gregory is technical director at Ovation Systems (Great Milton, Oxfordshire, UK).
CACHING DESIGNS

theme presents its own cost, performance and complexity trade-offs. Cache systems increase the effective speed of main memory by providing the CPU with a copy of the most frequently used data more quickly. If more data is prefetched than requested, cache memory can be further enhanced and can provide a very high hit rate to sequential accesses.

Cache systems consist of a cachetag RAM and an associated data RAM. The cache-tag RAM contains records of addresses accessed on previous cycles together with validation bits indicating that a valid cache entry has been made. The data RAM contains the corresponding data associated with those addresses. When subsequent addresses match a validated cache-tag entry, a cache hit is indicated. The main memory is then bypassed and the corresponding data retrieved from the cache data RAM.

Software properties

Because most software routines spend considerable time in loops repeatedly executed from the same memory location, it’s very likely that program data will be found in the cache from previous passes through the loop. Cache systems exploit this property to provide high hit rates for program data accesses. A 32-kbyte cache will typically contain program data for 70 percent of accesses, yielding a 70 percent hit rate and, thus, a 30 percent miss rate.

Because programs typically operate sequentially, the cache miss rate can be reduced by prefetching multiple data words from main memory and entering them into cache. Also, by expanding the data width—or line length—of prefetched data, the miss rate is reduced in almost direct relation. Memory systems designed with a wide line length thus give very high hit rates.

Since most software loops and subroutines typically reside within less than 1 or 2 kbytes of memory, cache memory doesn’t have to be particularly large to produce noticeable improvements. The 68020/68030 CPUs from Motorola (Tempe, AZ), for example, have only 256 bytes of cache memory yet achieve significant performance enhancements over similar CPUs without caches. Increasing the cache size will improve the hit rate, but for most applications a cache size of around 16 to 32 kbytes will produce the optimum cost/performance ratio.

Prefetch program data fetches also benefit from cache memory. Variables used within software routines may be accessed repeatedly with a high probability of being provided from cache. Similarly, data base manipulation will typically concentrate on relatively small parts of a data base, and these will mostly be contained in the cache. But a simple cache memory is unlikely to dramatically benefit systems in which large amounts of data must be written into main memory without being read back, or if the memory accesses are unlikely to be to sequential or repeated locations.

Direct vs. associative mapping

There are a number of ways in which a cache can maintain a store of the addresses and corresponding data of the most commonly used memory locations. Each storage method differs in how the cache-tag entries relate, or map, to the address space that they serve.

Associative mapping stores cachetag entries in the order in which they last occurred, with the records stacked in a specialized first-in, first-out (FIFO) memory. This method provides very efficient mapping since it maintains a complete record of all the most recently accessed memory locations. It’s difficult, however, to implement on a large scale because all the cache-tag entries in the FIFO must be checked to determine whether they match any subsequent cycles. This checking can be done in VLSI circuitry, but it can’t provide for many entries because a dedicated comparator must be attached to every cache-tag location to determine whether any of the cache-tag locations have hit.

Unlike associative mapping, direct mapping allows the use of static RAM devices to hold the records of the addresses that are most commonly accessed. Direct mapping is thus easier to implement. The records aren’t stored strictly in order of occurrence, but in locations that have a direct relationship to the address in main memory.

With direct mapping, lower-order address lines are used to retrieve a record of the higher-order addresses of previous cycles from high-speed static memory. If this record matches the present higher-order addresses and the validation bit is asserted, the cache tag indicates a cache hit. Data is then retrieved from the cache data RAM in preference to the main memory. If the addresses don’t match or the validation bit isn’t set, a cache miss is indicated and a new cache entry is made, consisting of the present address and data storage methods differ in how the cache-tag entries relate, or map, to the address space they serve.

Address and data storage methods differ in how the cache-tag entries relate, or map, to the address space they serve.

With direct mapping, conventional static RAM can be used to hold the records of the addresses most commonly accessed. Although not quite as efficient as associative mapping, direct mapping requires just one comparator to check the retrieved cache tag.

DIRECT MAPPING

<table>
<thead>
<tr>
<th>CACHE TAG RAM</th>
<th>DATA RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>RECORDS OF PREVIOUS HIGHER-ORDER ADDRESS</td>
<td>CORRESPONDING DATA</td>
</tr>
<tr>
<td>CURRENT LOWER-ORDER ADDRESS POINTER</td>
<td>DATA DRIVEN ONTO BUS ON HIT</td>
</tr>
<tr>
<td>VALIDATION BITS</td>
<td>BUFFER</td>
</tr>
<tr>
<td>CURRENT HIGHER-ORDER ADDRESS</td>
<td>DATA FROM CACHE</td>
</tr>
<tr>
<td>COMPARE</td>
<td>HIT</td>
</tr>
<tr>
<td>MAIN MEMORY DISABLED</td>
<td></td>
</tr>
</tbody>
</table>
Evaluating cache performance

Of the many factors that affect the performance increase attained by attaching a cache to a system, the most important are the characteristics of the actual application. Nevertheless, it's possible to perform a theoretical analysis of different caching techniques in a few simple steps.

First, look at the cache miss rate for various cache sizes and prefetched data-line lengths for a direct-mapped system. Note that the miss rate drops dramatically with an increase in line length. A line length that's wider than the processor bus will provide enhanced cache hit rates because of the sequential nature of most CPU activity. In fact, read hit rates approaching 95 percent can be achieved through line lengths of eight times the CPU bus width.

Next, compare the cache miss rates of the various mapping methods, here expressed as a ratio of the direct-mapped method. To determine the actual miss rate of a nondirect-mapped system, find the miss rate (from first table) for a direct-mapped system and multiply it by the relevant cache-mapping-type ratio (from second table).

The resulting miss rate applies to read cycles only. If the cache uses a copyback scheme or includes a write-cycle buffer, all write cycles may be regarded as cache hits. Assuming that 80 percent of memory cycles are read cycles, the overall miss rate may be reduced by 0.8. If the system is a writethrough cache, all write cycles are analogous to a cache miss in that the cache has to go to main memory, so 0.20 should be subtracted from the hit rate.

The miss rate of a particular cache implementation may be translated into a figure for total system improvement by determining the resultant hit rate, which equals 1 minus the miss rate, and considering the improvement in cycle time on a cache hit compared to a cache miss (see equation above). A cache hit will normally provide the minimum cycle period from the CPU. The cache miss cycle period depends on the main memory used.

A direct-mapped, writethrough caching system with 8-byte entries and a 4-byte line length removes three wait states for a cache hit in a 68020-based system. (The 68020 has a minimum memory access cycle length of three clock periods. Any further clock periods required to meet the memory access time are referred to as wait states.) The system, therefore, provides a 52 percent increase in total performance.

<table>
<thead>
<tr>
<th>CACHE SIZE AND LINE LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Entries</td>
</tr>
<tr>
<td>2k</td>
</tr>
<tr>
<td>4k</td>
</tr>
<tr>
<td>8k</td>
</tr>
<tr>
<td>16k</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CACHE TYPE ADJUSTMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache Types</td>
</tr>
<tr>
<td>direct-mapped</td>
</tr>
<tr>
<td>two-way set-associative</td>
</tr>
<tr>
<td>four-way set-associative</td>
</tr>
<tr>
<td>eight-way set-associative</td>
</tr>
<tr>
<td>fully associative</td>
</tr>
</tbody>
</table>

higher-order addresses, an asserted validation bit and the current data.

Direct mapping replaces cache entries on accesses to addresses that are multiples of the lower-order address range. This isn't quite as efficient as associative mapping, which replaces entries as on a least recently used basis. However, since most software operates serially, direct-mapped systems perform almost as well as associative systems. What's more, direct mapping has the considerable advantages of requiring just one comparator to check the retrieved cache-tag record and of using conventional SRAM. Direct-mapped caches of larger capacity thus may be constructed without extra cost or complexity.

A hybrid approach

Set-associative mapping is a hybrid of the direct-mapped and associative methods and is normally used as an efficient way of expanding a direct-mapped system. Set-associative systems contain multiple banks of direct-mapped caches that are dynamically allocated on a least recently used basis, effectively providing a stack of direct-mapped caches.

A set-associative cache that has 2^s banks of direct-mapped caches is referred to as £-way set-associative. Increasing the cache size by set-associative mapping gives greater hit rates than increasing the depth of a direct-mapped system. For this reason, many high-performance caching devices and systems adopt set-associative caching as a compromise between complexity and performance.

Performance Improvement = \[ \frac{\text{Cache Miss Cycle Period} \times \text{Miss Rate}}{\text{Cache Hit Cycle Period} \times \text{Hit Rate}} \]
**CACHING DESIGNS**

All of these cache-tag methods need a mechanism for invalidating cache records either on power up or when it’s clear that the cache entry is no longer a valid copy of the main memory. This mechanism is implemented as a validation bit attached to the cache-tag RAM and is included in the address comparison when determining whether a hit has occurred. Also, since many locations in a system address map may be uncacheable—including status latches, I/O devices and devices that require regular access—cache systems must provide mechanisms to exclude these locations from being entered in the cache.

**Dealing with write cycles**

In addition to the various mapping methods, cache systems may deal with write cycles by adopting one of two schemes: writethrough or copyback. Writethrough systems provide the best balance of performance and economy. In performing write cycles, writethrough systems provide mechanisms to exclude these locations from being entered in the cache. Writethrough caches don’t affect the performance of write cycles, but since processors typically spend only 20 percent of their time performing write cycles, writethrough systems provide the best balance of performance and economy.

Copyback systems are the more complex of the two alternatives, providing a cache for write cycles as well as for read cycles. The copyback cache accumulates write cycles, transferring the data through to the main memory either when space is required in the cache for new entries, or to ensure that cache coherency is maintained when the cache has the only valid copy of data that another processor requires. Copyback systems will thus make the main memory appear to contain only valid data; the actual data in main memory will be incomplete until all the cache data has been copied back into it.

Copyback systems offer optimum performance, but they’re highly complex. Copyback systems are most valuable when multiprocessors communicate via shared memory over a common bus. A copyback cache lets each processor maintain its own local copy of the global data, considerably reducing the traffic over the common bus. Protocols must be established for guaranteeing that data modified by any processor and retained within its cache is redistributed when other processors access the same location.

**A bus solution**

Futurebus, which was designed to let powerful cache systems be implemented within a standard bus structure, provides protocols that guarantee the redistribution of this data. The only fully standardized system to offer these facilities, Futurebus lets simple writethrough systems coexist with full copyback systems.

The Futurebus caching scheme adds a new dimension to multiprocessor cache systems. Multiple CPU cards, each with its own cache, may access shared global memory over Futurebus. Each cache may retain the only valid copy of pieces of data or one of multiple copies. Subsequent accesses to that data from any other processor will access the relevant cache and not necessarily the main memory. The global memory map thus becomes physically distributed among the separate cache systems, yet always appears as linear centralized global memory to all participating processors. Futurebus need only transfer data for write cycles and cache misses—a fraction of the data traffic otherwise required.

To allow full, coherent copyback operation, Futurebus defines states that are attached to every cache entry to indicate whether that entry is modified, owned, exclusive, shared or invalid. Futurebus further defines the rules that manipulate these states to maintain coherency. Once suitable VLSI devices become available, the Futurebus caching scheme will hold great promise for multiprocessor systems operating on a common data base.

**Keeping the cache coherent**

A cache system works by providing a local image of part of main memory. That image must be accurately maintained: It must be kept coherent. A caching system must operate within a set of rules that ensures that all entries are updated to reflect the true state of main memory. This procedure is straightforward when all accesses to the main memory share a common access port and, hence, share the cache facilities. This happens in single-processor designs in which only one device is using the memory. It is also true of multiprocessor systems in which the cache is positioned between the common global bus and the memory. Cache coherency proves difficult when the main memory may be updated independently of the cache from a secondary port or independent bus. Although the main memory could be updated, the cache would
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still contain the old, now invalid, data. This could be the case when each processor in a multiprocessor system has its own cache independent of the global bus where the shared memory resides, or when the main memory is actively dual-ported between two independent buses.

One solution to ensure cache coherency is to provide a mechanism to update or invalidate individual cache entries when the corresponding main memory locations are modified by a second processor or from another port. This is called bus watching, or snooping. As an alternative, cache coherency through dual-ported memory may be maintained by suitable software handshaking. The processors sharing memory would arrange that no block of memory would be used while a device is actively modifying that block. When a processor needs to use a new memory block, it would clear all previous cache entries to guarantee that no stale data remains.

**On-chip caches**

Processors with on-chip caches create potential cache coherency problems if the main memory is dual-ported to other devices. When the on-chip cache is used solely for program data fetches, the dual-ported memory isn’t usually a problem because program data isn’t normally dynamically altered. It becomes a problem, however, when dynamically changing data is shared between two devices. Multiple processors with on-chip caches will have difficulty communicating and coordinating actions when they don’t recognize all of the changes in shared memory. Most processors with on-chip cache rely on the software handshaking solution to this problem, but some processors provide hardware hooks that let off-chip bus-watching hardware invalidate internal cache entries. Processors could conceivably also be designed with bus-watching hardware on-chip.

On-chip caches improve system performance significantly, but they’re hungry for silicon real estate. These caches are, therefore, typically quite small: 256 bytes for the 68020/68030 and 512 bytes for the NS32532 from National Semiconductor (Santa Clara, CA), for example. Some high-performance processors use pipelined architectures that let a data fetch from an internal cache overlap accesses to off-chip devices. On-chip caching thus allows concurrency of data fetching, reducing the bottleneck of getting data on- and off-chip.

The NS32532, for example, provides hardware hooks to let an off-chip bus watcher invalidate on-chip cache. The 68030 allows burst filling of its cache, exploiting the relatively high access bandwidth of DRAM page and nibble modes, with which sequential data may be retrieved within a single, extended memory cycle. And the 29000 from Advanced

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### CACHING DESIGNS

Micro Devices (Austin, TX) uses its cache to fill its instruction pipeline when a branch is made out of a sequential program flow. Off-chip caches, on the other hand, allow even greater performance increases. With an off-chip cache, the cache system can be more precisely tailored to specific applications, but at the expense of extra chip count and complexity.

These external caches range enormously in their degree of integration. All contain a cache-tag RAM of varying mapping types, some contain the logic to control a separate off-chip data RAM, some provide an on-chip data RAM, and some include bus-snooping circuitry, parity protection or even memory-management units. Generally, the more highly integrated devices are targeted at specific processors and offer very high hit rates.

The current use of cache systems bridges the gap between high-performance processors and low-cost memory, allowing the transmutation of lumbering DRAM into nimble SRAM. With the present trend toward parallel processing, caching schemes relieve the shared memory access bottleneck and so let conventional processor elements operate efficiently in multiprocessor systems.

---

### Table: Microprocessors with on-chip caches

<table>
<thead>
<tr>
<th>Processor</th>
<th>Manufacturer</th>
<th>Cache Size (Bytes)</th>
<th>Mapping Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>68020</td>
<td>Motorola</td>
<td>256 program</td>
<td>direct-mapped</td>
<td></td>
</tr>
<tr>
<td>68030</td>
<td>Motorola</td>
<td>256 program 256 data</td>
<td>direct-mapped</td>
<td>on-chip MMU</td>
</tr>
<tr>
<td>29000</td>
<td>Advanced Micro Devices</td>
<td>512 program</td>
<td>two-way set-associative</td>
<td>cache branches out of sequential program flow</td>
</tr>
<tr>
<td>32532</td>
<td>National Semiconductor</td>
<td>512 program 1,024 data</td>
<td>two-way set-associative</td>
<td>on-chip MMU</td>
</tr>
<tr>
<td>Clipper</td>
<td>Intergraph</td>
<td>4k program 4k data</td>
<td>two-way set-associative</td>
<td>chip set</td>
</tr>
</tbody>
</table>

Microprocessors that have their own on-chip caches improve system performance significantly. Some use pipelined architectures to overlap data fetches from internal cache with accesses to off-chip devices.
Higher speeds, CMOS designs drive flash A-D converter developments

John H. Mayer, Senior Associate Editor

As digital signal processing systems move beyond strictly military applications and into the imaging and consumer markets, the demand is building for high-performance flash analog-to-digital converters capable of digitizing analog signals at increasingly faster rates. Vendors of high-performance DSPs are finding that the success of their processors is as dependent on the availability and cost of comparable high-performance front-ends as it is on processor performance.

“We’re finally getting to the point where the whole DSP arena is getting out of the military domain,” says John Hull, marketing manager for data-conversion products at Integrated Device Technology (Santa Clara, CA). “There’s finally enough of a base of knowledge, the components are understood well enough, and the prices have come down to where it’s really worthwhile to use these DSPs in consumer applications.”

The market is responding with a growing array of monolithic and hybrid bipolar flash A-D converters capable of delivering sampling rates of up to 300 Msamples/s at 8 bits and 50 Msamples/s at 10 bits. In addition, vendors such as GE (Santa Clara, CA), IDT, Micro Power (Santa Clara, CA) and Datel (Mansfield, MA) are delivering CMOS parts boasting power consumption a fraction of their higher speed bipolar cousins. Continuing improvements in CMOS processes are pushing these 8-bit devices up to 30 MHz and higher. At the same time, data-converter designers are finding ways to add support functions ranging from references and drivers to clamping circuits and sampling amplifiers.

Business prospects for the flash A-D converter market look attractive enough to support a growing number of manufacturers. A few years ago, TRW (La Jolla, CA) led the industry as the sole major supplier. Its multisourced TDC1048 set the industry standard for 8-bit flash A-D converters. But with market analysts such as Venture Development (Natick, MA) projecting average annual growth rates in the 15 percent range over the next five years, the flash A-D converter market is becoming increasingly crowded. As the accompanying table demonstrates, about 20 vendors (some didn’t respond to our survey) offer significant product lines ranging in resolution from 4 to 10 bits.

Ten-bit flash A-D converters

TRW still leads the industry in the race for the highest resolution flash A-D converter. The company’s TDC1020 is the only 10-bit monolithic flash design in volume production. Packed into a 64-pin dual in-line package, the TDC1020 offers a significantly more compact and less power-hungry solution than board-level alternatives. A commercial version of the TDC1020 is available, with a military model to be introduced later this year.

The other company to announce a 10-bit flash A-D converter is Honeywell (Colorado Springs, CO). The 50-MHz HADC77600 has already been designed into one military system, according to a spokesperson from the company’s Signal Processing Technologies Group. Like many high-resolution flash A-D converters, the device adds a sparkel code detection circuit to prevent erroneous outputs.

Announced over a year ago and not yet available in production quantities, the HADC77600 has already gone through one redesign. The initial version of the part added a linear preamplifier with differential inputs and outputs placed between each pair of input-signal lines to the chip’s comparators. Honeywell added the preamp because there weren’t any buffer amplifiers capable of driving the converter’s input, according to a company spokesperson. The revised, simplified design will eliminate the preamp in favor of an off-chip track-and-hold amp recently developed by Addacon (Greensboro, NC). Addacon offers the track-and-hold separately, but will eventually bundle the 30-MHz circuit in a module with the converter.

Video applications dominate

The product lines of most suppliers center around 8-bit parts targeted for TV video systems—by far the largest application for flash A-D converters. Determining the speed leader is a difficult, almost futile task. Spesman-
<table>
<thead>
<tr>
<th>Device</th>
<th>Resolution (bits)</th>
<th>Sample Rate (Mamples/s)</th>
<th>Power Dissipation (mW)</th>
<th>Input Bandwidth (MHz)</th>
<th>Packaging</th>
<th>Price (000s)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Devices</td>
<td>PO Box 9106, Norwood, MA 02062 (617) 329-4700</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Circle 100</td>
</tr>
<tr>
<td>AD9002</td>
<td>8</td>
<td>150</td>
<td>750</td>
<td>115</td>
<td>DIP, LCC</td>
<td>$90</td>
<td>single supply, ECL output</td>
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<tr>
<td>AD9000</td>
<td>6</td>
<td>77</td>
<td>675</td>
<td>20</td>
<td>DIP, LCC</td>
<td>$40</td>
<td>overflow bit, bipolar input</td>
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<td>100</td>
<td>1,500</td>
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<td>metal DIP</td>
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<td>955</td>
<td>180</td>
<td>DIP, LCC</td>
<td>$70</td>
<td>TTL comp.</td>
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<td>$175</td>
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<td>Brooktree</td>
<td>9950 Barnes Canyon Rd, San Diego, CA 92121 (619) 452-7580</td>
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<td>Circle 101</td>
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<td>Datel</td>
<td>11 Cabot Blvd, Mansfield, MA 02048 (508) 339-3000</td>
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<td>ADC-207</td>
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<td>Fujitsu Microelectronics</td>
<td>3545 N First St, San Jose, CA 95134 (408) 922-9000</td>
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<td>22-pin DIP</td>
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<td>0.2% linearity, TTL output</td>
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<td>GE Solid State/Intersil</td>
<td>2450 Walsh Ave, Santa Clara, CA 95051 (408) 996-5000</td>
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<td>5</td>
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<td>CMOS/SOS</td>
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<td>Hitachi America</td>
<td>2210 O'Toole Ave, San Jose, CA 95131 (408) 435-8300</td>
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<td>DIP</td>
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<td>7</td>
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<td>bipolar, three-state output w/ latch</td>
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<td>HA19213</td>
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<td>250</td>
<td>5</td>
<td>DIP, SM (MSP)</td>
<td>$9.70</td>
<td>bipolar, TTL or CMOS comp.</td>
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Key: * single piece price; C= ceramic; comp.= compatible; DIP= dual in-line package; DNL= differential nonlinearity; EDC= error detection and correction; INL= integral nonlinearity; LSB= least significant bit; LCC= leadless chip carrier; MSP= mini square pack; P= plastic; PLCC= plastic leaded chip carrier; S/H= sample and hold; SM= surface mount; SO= small outline; SOS= sapphire-on-silicon; T & H= track and hold
## PRODUCT FOCUS/Flash A-D Converters

<table>
<thead>
<tr>
<th>Device</th>
<th>Resolution (bips)</th>
<th>Sample Rate (Msamples/s)</th>
<th>Power Dissipation (mW)</th>
<th>Input Bandwidth (MHz)</th>
<th>Packaging</th>
<th>Price (100s)</th>
<th>Comments</th>
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<tbody>
<tr>
<td><strong>Hitachi America</strong></td>
<td>2210 O'Toole Ave, San Jose, CA 95131 (408) 435-8300</td>
<td>Circle 105</td>
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<td>HA19211A</td>
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<td>—</td>
<td>DIP</td>
<td>$4.25</td>
<td>bipolar</td>
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<td><strong>Integrated Device Technology</strong></td>
<td>3236 Scott Blvd, PO Box 58015, Santa Clara, CA 95052 (408) 727-6116</td>
<td>Circle 106</td>
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<td>IDT75C48</td>
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<td>$21.50</td>
<td>CMOS, comp. w/TRW 1048, includes EDC</td>
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<td>28-pin CDIP, LCC, SO</td>
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<td>CMOS, tristate output, overflow output</td>
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<tr>
<td><strong>Maxim Integrated Products</strong></td>
<td>120 San Gabriel Dr, Sunnyvale CA 94086 (408) 737-7600</td>
<td>Circle 107</td>
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<td>ADC0820</td>
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<td>25</td>
<td>12.7 kHz</td>
<td>DIP, SO, PLCC</td>
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<td>CMOS, half-flash, w/ T &amp; H, 1.4-µs conversion</td>
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<td>±2.5-Ref, T &amp; H, eight input channels</td>
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<td><strong>Micro Power Systems</strong></td>
<td>3151 Jay St, Santa Clara, CA 95054 (408) 727-5350</td>
<td>Circle 108</td>
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<td>MP7690</td>
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<td>400</td>
<td>50</td>
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<td>MP7684</td>
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<td><strong>Motorola Semiconductor Products</strong></td>
<td>7402 S Price Rd, PR360, Tempe, AZ 85282 (602) 897-3872</td>
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<td>2900 Semiconductor Dr, PO Box 58090, Santa Clara, CA 95051 (408) 721-5000</td>
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<td>Device</td>
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<td>Sample Rate (Msample/s)</td>
<td>Power Dissipation (mW)</td>
<td>Input Bandwidth (MHz)</td>
<td>Packaging</td>
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<td>401 Ellis St, Mountain View, CA 94039 (415) 960-6000</td>
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<td>Plessey Semiconductors</td>
<td>1500 Green Hills Rd, Scotts Valley, CA 95066 (408) 438-2900</td>
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<td>ECL, ±1/2 or ±1/8 LSB</td>
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<td>100</td>
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<td>ECL output, on-chip encoding</td>
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<td>Samsung Semiconductor</td>
<td>3725 N First St, San Jose, CA 95134 (408) 434-5400</td>
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<tr>
<td>KSV3100AN-7/8</td>
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<td>1,200</td>
<td>50</td>
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<td>flash A-D &amp; D-A, A-D 7 or 8 bits, on-chip $V_{ref}$ gen., input preamp</td>
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<td>40-pin DIP</td>
<td>$24/$32/$48</td>
<td>A-D only, on-chip $V_{ref}$ gen., input preamp, input clamping circuit</td>
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<td>KSV3208AN</td>
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<td>50</td>
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<tr>
<td>Siemens Semiconductor Group, IC Div</td>
<td>2191 Laurelwood Rd, Santa Clara, CA 95054 (408) 980-4577</td>
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<td>SDA8010</td>
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<td>250</td>
<td>40-pin C DIP</td>
<td>$168</td>
<td>five effective bits at 150-MHz full-scale input, output demultiplexer</td>
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<td>Signal Processing Technologies</td>
<td>1150 E Cheyenne Mtn Blvd, Colorado Spgs, CO 80906 (719) 540-3900</td>
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<td>monolithic, preamp comparator design, quarter-point ref. ladder taps</td>
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<td>70</td>
<td>PGA</td>
<td>$795*</td>
<td>monolithic, preamp, eighth-point ref. ladder taps</td>
</tr>
<tr>
<td>Signetics</td>
<td>811 E Arques Ave, Sunnyvale, CA 94088 (408) 991-2000</td>
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<td>TDA8703</td>
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<td>40</td>
<td>300</td>
<td>19.5</td>
<td>24-pin DIP</td>
<td>$15</td>
<td>low power, input buffer amp, +5V only</td>
</tr>
<tr>
<td>Sipex, Hybrid Systems Div</td>
<td>22 Linnell Cir, Billerica, MA 01821 (508) 667-8700</td>
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<td>HS1068</td>
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<td>13</td>
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<td>25</td>
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<td>hermetic 42-pin pkg</td>
<td>—</td>
<td>dual-channel hybrid, two 8-bit A-Ds, two buffer amps/channel, $V_{ref}$</td>
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PRODUCT FOCUS/Flash A-D Converters

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<tr>
<th>Device</th>
<th>Resolution (bits)</th>
<th>Sample Rate (Megasamples)</th>
<th>Power Dissipation (mW)</th>
<th>Input Bandwidth (MHz)</th>
<th>Packaging</th>
<th>Price ($100s)</th>
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<tr>
<td>Tektronix</td>
<td>PO Box 500, Beaverton, OR 97077 (800) 835-9433</td>
<td></td>
<td></td>
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<tr>
<td>TKAD20C</td>
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<td>250</td>
<td>5,000</td>
<td>125</td>
<td>84-pin ceramic</td>
<td>$850</td>
<td>on-board T &amp; H, selectable demultiplexed output</td>
</tr>
<tr>
<td>TRW LSI Products</td>
<td>PO Box 2472, La Jolla, CA 92038 (619) 457-1000</td>
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<td>68-contact CC</td>
<td>$290</td>
<td>monolithic, comm. or hi-rel. test, ECL output</td>
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</table>

ship, as always, is a problem. Also, newer, faster parts emerge every few months. But if one had to select the speed leaders among 8-bit flash A-D converters, they would no doubt include the AD770 from Analog Devices (Norwood, MA), the TKAD20C from Tektronix (Portland, OR), the SDA8200 from Siemens (Santa Clara, CA), and the CXA1076 and CXA1176 from Sony (Cypress, CA).

For pure 8-bit accuracy, the TKAD20C from Tektronix offers the best, albeit one of the most expensive, solutions. At high speeds, A-D converters are typically limited by their ability to track and capture the incoming signal. Many designers handle this problem by placing a separate track-and-hold amplifier in front of the device. The TKAD20C, however, was the first commercial A-D converter to include an on-board track-and-hold circuit.
Unlike many competitors, the TKAD20C was designed from the ground up as a two-chip device. The resulting tight interface between the A-D converter and the track-and-hold amplifier helps the part achieve a 250-M-sample/s conversion rate and an impressive accuracy of 7 effective bits at 125 MHz. Selectable demultiplexed outputs let designers easily conform the part to a variety of applications. Though the AD770 from Analog Devices can’t quite match the performance of the Tektronix part, it delivers an 8-bit output at 200 Msamples/s with a 250-MHz full-power bandwidth. The converter also sells at roughly one-quarter the price of the Tektronix part. For radio frequency applications, the analog input range can be unipolar or bipolar and can be set any to any span within ±2 V.

An interesting price/performance trade-off is offered by the Siemens SDA8200. The 6-bit, 300-MHz A-D converter is the first monolithic flash converter to digitize a 150-MHz input signal with an effective resolution of 5 bits. In addition, the 6-bit part only requires 63 comparators to reach its performance level, in contrast to the 255 comparators required for an 8-bit part. Chip size is small, and power dissipation is a scant 1,800 mW. Like its competitors, the SDA8200 adds overflow outputs so designers can cascade two or more parts to achieve 7-bit resolution. A user-selectable demultiplexer splits the output signal through two parallel output streams at half the sampling rate.

**CMOS speeds accelerate**

Although bipolar flash A-D converters still provide the highest performing solutions, CMOS devices continue to edge closer to their bipolar competitors. If a designer doesn’t require flash A-D converters at top speeds, CMOS parts offer compact, precise solutions at significant power savings. “For the 20-MHz and under region, there’s very little argument in favor of bipolar, and most of it in favor of CMOS,” says Walter Borlase, Micro Power Systems’ director of standard products.

Micro Power Systems offers monolithic CMOS A-D converters up to 20 MHz with full-power bandwidths in excess of 50 MHz. The Micro Power parts operate from a single supply and provide a reference voltage of 0 to 2 V. “Most of the devices on the market right now are built almost strictly for television, so you get a 2-Vpp,” says Borlase. “We’ll actually give you 0 to 5 V.” Other vendors are pushing CMOS parts beyond 20 MHz. This summer, IDT unveiled its IDT75C58, a 30-MHz 8-bit CMOS chip. The device features a unique on-chip error detection and correction (EDC) circuit that guarantees no missing codes over all temperature and voltage extremes. “A lot of our competitors’ converters will get so hot you might not be able to put it into a normal package,” he says. “It would be well-nigh-impossible to put the amount of added circuitry that we included on this EDC on a bipolar flash A-to-D.”

Despite these apparent advantages, most vendors agree that as CMOS parts move to bipolar speeds, the dividends CMOS offers evaporate. Bipolar converters dissipate the same power whether running at 1 or 20 MHz, while CMOS power usage increases with speed. “It’s a myth that CMOS parts are low-power,” says Karlak. “The reality is that at higher speeds, they’re going to approach bipolar power.” Micro Power’s Borlase agrees. “If you take a CMOS machine and start to run it at very high clock rates, you suddenly find that the power consumption goes up as well because you have all the capacitance to charge.”

Still, CMOS designs, or perhaps BiCMOS designs, should offer designers an opportunity to add a number of interesting support functions on-chip. Some of the first add-ons will probably be input buffer amplifiers and significant digital interfaces designed to simplify use of the part. Eventually, the flash A-D converter market will most likely see increasingly application-specific products with inputs and outputs designed to meet specific application needs.
E²/DIGITAL/ANALOG. COMBINATION Y
To be perfectly honest, we didn’t invent the concept that says high integration equals high profit. But as you can see from the application diagram on this page, we definitely perfected it. With our Triple Technology™, a process that allows you to combine E², digital, and analog functions on the same chip. And, create higher levels of integration than ever before.

In this case, our customer’s last product was a medical instrument the size of a paperback, with 70 different components. By combining a sophisticated 8-bit controller, RAM, ROM, A/D converter, and 256 bytes of EEPROM on the same chip, we helped them shrink the same instrument to the size of a matchbox. And cut the costs just as dramatically.

As a result, they have a product that sets new standards for the industry. And for their shareholders. And by working closely with their designers, we were able to create this one-chip solution with standard cells from our library. In fact, our customer only had to design about 200 gates of logic using our standard digital cells.

Turnaround time from code to first silicon was only 18 weeks. And because of our development tools and mixed-mode simulation (MIXsim™), the first prototypes worked.

Of course, this is only one example. With 250 digital, 50 analog, and over 20 EEPROM cells in our library, we can create literally thousands of combinations. Including Analog/E², E²/Digital, Analog/Digital, and E²/Analog/Digital. For every application you can imagine. And we can execute them all in high performance CMOS.

So, no matter what you’re designing, call or write for our complete library card. And we’ll show you a combination you can always bank on. Your ideas and our technology.
Macintosh II floating-point coprocessor performs 20 MFlops

The MC3200NU single-slot processor card for the Macintosh II is aimed at 32-bit floating-point-intensive applications. The board, which can be master or slave in the system, is a 20-MFlops, 10-Mips coprocessor that executes computation-intensive vector and scalar operations for applications such as simulation, modeling, signal processing, image processing and postscript. Programmable in C, Fortran, assembler and microcode, the coprocessor is supported by the Macintosh Programmer's Workshop, which provides the development environment.

The board is based on Weitek's XL-5032 reduced-instruction-set processor chip set, which includes the WTL-3132 32-bit floating-point unit. The three-chip set is supported by up to 8 Mbytes of two-way interleaved memory on a 40-Mbyte/s internal bus. Mastership capability lets the board transfer data independent of the host anywhere in the 4-Gbyte address space of the NuBus. Available software includes an extensive collection of microcoded algorithms such as the fast Fourier transform (FFT) as well as other signal processing algorithms. The 8 Mbytes of memory let the user load a complete program and run the application independent of the host. A 2-Mbyte system will sell for $10,000, hardware only. The Fortran and C development environment is available for $8,500.

Z280 STD Bus board expands to 128 kbytes

Featuring the speed and architectural improvements of the Zilog Z820, the Z280STD is a single-board computer for the STD Bus. It will run all current Z80 applications, including CP/M. On-board cache is incorporated by the microprocessor, as well as 24-bit address space, memory management and protection, and hardware multiply/divide. Up to 128 kbytes of ROM or battery-backed RAM can be included in any mix on the board, which comes with 20 bits of parallel I/O standard and three RS-232 ports. A total of eight counters/timers are included for real-time, multitasking process control applications. Price for the single-board computer is $395.

Computer Design Solutions
PO Box 127
Statesville, NC 28677
Circle number 122

Single-board computer consumes 3 W

The Quark/PC+ single-board computer boasts a complete IBM-compatible CPU with on-board video and disk controllers on a 4-x-6-in. card, and consumes 3 W. Up to 768 kbytes of dynamic RAM is available on the board, as well as a small computer system interface host adapter, a floppy disk controller, a video/LCD controller, three serial ports, a parallel port, a reset switch and a battery-backed real-time clock. All I/O is provided through a 96-pin Eurocard connector, while access to the PC bus is by a user-specified 64-pin header or 62-pin male edge connector. An on-board legal basic I/O system lets the board boot any version of PC or MS-DOS as well as run most conventional PC software packages. Prices start at $325.

Megatel Computer
174 Turbine Dr.
Weston, ON M9L 2S2, Canada
Circle number 123

Controller functions reside on AT-class mother board

A small-footprint, IBM PC AT-compatible computer, the ARC ProTurbo uses VLSI chips for I/O, video and disk controller functions. The system runs under either the MS-DOS or OS/2 operating system, with keyboard- or software-selectable
clock speeds of 8 or 12 MHz. Basic configuration includes 1 Mbyte of RAM expandable to 16 Mbytes, a 1.2-Mbyte 5¼-in. floppy disk drive, a keyboard and a 150-W power supply. System expansion is provided through five full-sized expansion slots, four of them 16 bits and one 8 bits. An 80287 numeric coprocessor is optional. The basic system is priced at $1,995.

American Research
1101 Monterey Pass Rd
Monterey Park, CA 91754
Circle number 124

68020 VMEbus SBCs use mezzanines for expansion

A pair of VMEbus controller/single-board computer products are specifically designed to allow user expansions via plug-in mezzanine modules. The 68020-based boards are identical except in the area of on-board memory. The PT-VME118 provides 1 Mbyte of dual-ported RAM, expandable to 2 Mbytes, without parity. The PT-VME120 offers a fixed 1 Mbyte of dual-ported dynamic RAM with parity protection. Both models' memory runs at 16-MHz zero-wait-state clock speeds. Other features include a seven-level VMEbus interrupt handler, two 32 JEDEC sockets for local RAM/ROM and an optimized VME interface. Most options on the modules are configured via a software menu through an RS-232C terminal with all software-defined user information stored in a dedicated 1-kbit EEPROM. The PT-VME118 is priced at $1,600, while the PT-VME120 costs $1,840.

Performance Technologies
435 W Commercial St
Rochester, NY 14445
Circle number 125

80386 mother board doubles AT’s speed

Based on the Intel 80386 microprocessor, the 386 Motherboard/AT improves the performance of an IBM PC AT by 2½ times by upgrading a 6- or 8-MHz AT to 16-MHz 386 speed. The board, which will also work with AT compatibles, uses the Award 386 basic I/O system, comes with four 16-bit and four 8-bit I/O slots, has a 32-bit RAM extension connector, and can be expanded with up to 12 Mbytes of RAM. A 16-MHz 387 math coprocessor is available for math-intensive applications. With 1 Mbyte of memory, the board is priced at $1,595.

Hauppauge Computer Works
175 Commerce Dr
Hauppauge, NY 11788
Circle number 126

2.5 Gigabytes Unattended Backup

Digi-Data’s GIGASTORE™ provides 2.5 Gigabytes of data storage on a single T-120 VHS video cartridge. That permits backup of your largest disk drive on off-hours without an operator. Utilizing true read-after-write coupled with very powerful error correction, GIGASTORE gives you an unsurpassed error rate of 1 in 10^23 bits. In addition, you get a high speed search capability not available in most 9-track drives. GIGASTORE can be provided with an interface for DEC computers, such as VAX and Micro Vax, for operation under VMS. It is also available with an IBM PC interface, operating under MS/DOS.

Call Digi-Data, an organization with a 25 year history of manufacturing quality tape drives, at (301) 498-0200.

DIGI-DATA CORPORATION
8580 Dorsey Run Road
Jessup, MD 20794-9990
(301) 498-0200
Telex 87-580

CIRCLE NO. 22
COMPUTER DESIGN OCTOBER 15, 1988 83
NEW PRODUCT HIGHLIGHTS

DATA ACQUISITION AND CONTROL

Analog-to-digital 
I/O board speeds 
to 1 Msample/s

Featuring an on-board 12-bit analog- 
to-digital converter with a maximum 
sampling rate of 1 Msample/s, the 
DAS-50 is a four-channel I/O board 
for IBM PCs, PC XT, PC AT and 
compatibles. A series of samples (or 
Trace) may be triggered via software 
commands, an external trigger or a 
voltage-level input.

Since direct memory access isn’t 
possible at 1 million conversions/s, lo- 
cal on-board data storage is provided. 
Up to 1 Mword of memory may be 
configured by using up to four banks 
of 256k x 1-bit dynamic RAMs. By us- 
ing 16 consecutive locations in I/O 
address space that can be set to start 
at any base I/O address, the board 
takes up no memory address space, 
requires no on-board initializing 
basic I/O system and can be installed 
regardless of the I/O address usage of 
other peripherals.

Five software programmable, uni- 
polar or bipolar input ranges are 
available, and maximum linearity 
error is only 1 least-significant bit 
guaranteed over the full input range. 
The selection and control of all fea- 
tures are accomplished through the 
computer keyboard or a mouse, with 
utility software provided as a device 
driver, letting programs be written 
in any upper-level language. Prices 
start at $1,999.

GW Instruments
35 Medford St
Somerville, MA 02143

Circle number 128

Data-acquisition products 
target Macintosh II and SE

The MacAdios II Data Acquisition 
System consists of a multifunction 
analog and digital I/O board set that 
plugs into one of the Macintosh II or 
SE expansion slots, a variety of sig- 
nal-conditioning daughter boards, 
and software for data acquisition 
and control. Optional Labtech Notebook 
software provides user-definable con- 
trol and display setups and param- 
eters; real-time mathematical, statis- 
tical and signal-processing calcula-
tions; triggering; monitoring; control 
functions; and data replay. The soft- 
ware transfers acquired and reduced 
data to spreadsheets, scientific graph- 
ics worksheets and other Macintosh 
programs for further data analysis 
and display.

GW Instruments
35 Medford St
Somerville, MA 02143

Circle number 128

Industrial process control 
software runs on PCs

A factory automation software pack- 
age for industrial process control, 
the L/T Control System is designed 
for use on IBM PCs or compatibles 
equipped with the manufacturer’s 
data acquisition and control hard- 
ware. The boards plug into PC expan- 
sion slots; have software-selectable 
ranges or autorange; are self-calib- 
rating with diagnostics available on 
command; and feature a low-noise in-
tegrating converter that can take up 
to 10,000 samples/s. Graphical real-
time animated data displays are of- 
fered, as well as high-resolution plots, 
on/off control, and alarm loops. Addi-
tional set-up commands include data 
logging, real-time operator interfaces 
and on-line analysis. The package is 
priced at $2,995.

Strawberry Tree Computers
160 S Wolfe Rd
Sunnyvale, CA 94086

Circle number 129

Controller allows data 
aquisition on Bitbus

The RTP7411/70 serial controller 
provides an interface between Bitbus 
and the manufacturer's RTP family 
of analog, digital and special-func- 
tion I/O data-acquisition hardware 
and software products. The board
### DATA ACQUISITION AND CONTROL

Consists of a standard Bitbus core, a hardware interface to the RTP bus, an RS-232 serial channel and a firmware package that converts Bitbus to RTP signals. All programs and data are stored in a 32-kbyte, battery-backed CMOS RAM. Rates of up to 375 kbits/s are supported.

**Computer Products**
2900 Gateway Dr
Pompano Beach, FL 33069

*Circle number 130*

### VMEbus boards feature 16-bit A-D resolution

The DT1492 series of analog and digital I/O boards features single-board operation with up to 16 bits of analog-to-digital resolution and 16 lines of digital I/O. High-speed simultaneous analog input and output operations are supported via 512 kbytes of memory, allowing A-D throughput speeds of up to 750 kHz. Gap-free continuous performance operation assures data integrity, while automatic sampling of any input or output sequence is possible at any gain. Optional simultaneous sample-and-hold A-D can acquire up to four channels within 10 ns. The series consists of nine models with a variety of options. Prices start at $2,195.

**Data Translation**
100 Locke Dr
Marlboro, MA 01752

*Circle number 131*

### DESIGN AND DEVELOPMENT TOOLS

**Emulator boasts zero wait states at 16 MHz**

An in-circuit emulator for Intel's 80C186/80C188, the ES 1800 runs with zero wait states at 16 MHz. An I/O overlay capability is featured that lets the emulator exercise I/O service routines without target hardware. The device also lets the user see the entire peripheral control block on one screen and make register changes without the large number of register dumps and writes normally required.

Complementing the emulator is the Validate/Soft-Scope source-level debugger. It features a powerful command set, real-time trace displayed in source-level statements, machine instructions and bus cycles with easy access to high-level language data structures and arrays. The Event Monitor System is included, providing state-machine capabilities for triggering, breakpoint and emulation control. The system lets an engineer control emulation by breaking on any combination of address, data status, pass counter and logic state fields. An event or combination of events, defined by logic statements, can be used to break emulation, trace software sequences and count or trigger outputs. Prices start at $11,000.

**Applied Microsystems**
5020 148th Ave, NE
Redmond, WA 98073

*Circle number 132*

**X Window System coupled to DOS, Unix workstations**

The X Window System Version 11 (X11) lets Hewlett-Packard's MS-DOS and Unix workstations access X-based applications in a multivendor, networked environment. Based on a client/server architecture, the system lets clients, or X-based applications, make requests for resources (display, keyboard, mouse or other input devices) from the server. Software developers have the choice of building a user interface for their applications based on HP's X Widgets, designing their own widgets, or using a combination of the two. With these tools, developers can use pop-up menus, panels, scroll bars and a variety of other widgets to construct the desired user interface. Prices range from $495 to $4,500 depending on the host system.

**Hewlett-Packard**
19310 Pruneridge Ave
Cupertino, CA 95014

*Circle number 133*

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*Free information—Richard Crowe, M.D. (Harvard); President, Columbia Pacific University, Department 3E50, 1415 Third Street, San Rafael, CA 94901. Toll free: (800) 227-0119; California: (800) 552-5522 or (415) 458-1650.*

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**COMPUTER DESIGN** OCTOBER 15, 1988 85
Logics analyzer increases debugging performance

A logic analyzer that can rapidly identify problem areas in microprocessor and logic designs, the K115 offers the power of two independent analyzers in one package. The general-purpose state/timing section provides 64 input channels and eight levels of trace control triggering at resolutions of 50 ns. The high-resolution section provides eight additional channels with resolution to 10 ns, with four channels user configurable to 5 ns. Other features include noise margin analysis to identify signals not making full logic-level swings, histogram analysis for program execution overviews, disassembly for detailed program tracking and mixed radix display formats.

Floppy disk controllers support XT's, AT's and PS/2s

The ACC 3200 series of single-chip floppy disk controllers for IBM PC XT, PC AT and Personal System/2 Models 30, 50, 60, 80 and compatible systems directly controls up to four diskette drives. Each VLSI device is manufactured with 1.5-micron CMOS technology and incorporates all functions of a floppy disk controller in one 68-pin plastic leaded chip carrier to save space in system designs. Prices are from $10 to $20.

Routing program designs surface-mount devices

A gridless software program for automatically routing ultra-high-density circuits, the Flex Router is based on algorithms designed for surface-mount technology. The software runs on the manufacturer's CR 3000 electrical CAE/CAD/CAM system and allows exact routing from the center of the surface-mount device pad or off-grid routing between pads. Capabilities for bus routing, general signal routing and ground routing are also provided. The design tool allows special routing of connectors, including autorouting of edge connectors, and features user-selectable routing angles as well as rip-up and reroute capabilities.

Twelve-bit multiplying D-A converter hosts on-chip amplifier

A 12-bit, four-quadrant multiplying digital-to-analog converter, the AD-7845 includes an on-chip output amplifier. The monolithic device combines high-speed digital logic and linear circuitry in a 0.3-in. Skinny dual in-line package (DIP) to reduce chip count while displacing half the space of traditional 24-pin double-width DIP devices.

External connections permit configuration for either unipolar or bipolar operation, as a programmable-gain amplifier or a programmable current source. Gain ranging and offsetting are provided via three matched internal application resistors, while TTL- or CMOS-compatible inputs drive the 12-bit latch, controlled by standard signals, allowing connection to the 16-bit bus interface through direct unbuffered operation. Guaranteed monotonic over the full operating temperature range, the device allows a maximum of ±1 least-significant bit (LSB) differential nonlinearity and ±2-mV zero-code offset error. The on-chip amplifier and feedback resistor perform current-to-voltage conversion with accuracy within ±1 LSB. Delivering a ±10-V swing into a 2-ohm load, the internally compensated output amplifier settles to 0.01 percent full-scale range in under 5 µs. In quantities of 100, prices for the D-A converter start at $7.40.
EDC circuit detects memory errors in 16 ns

The Am29C660 error detection and correction (EDC) circuit, a high-speed CMOS device, detects all single-, double- and some triple-bit errors in each single memory word. The 32-bit circuit corrects all single-bit errors, including hard errors caused by permanent physical device failure as well as soft transient errors by using a modified Hamming Code algorithm and generated check bits. The highest performance version has a 16-ns maximum delay for error detection and a 24-ns maximum delay for error correction. In 5,000-piece quantities, the chip is available in a 68-pin plastic leaded chip carrier for $42 and in a 68-pin grid array the chip is priced at $44.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94088
Circle number 138

64-kbit SRAM yields 10-ns access time

Arranged as 64k x 1 bit, the IDT-10490 is a BiCMOS ECL I/O static RAM with a 10-ns access time. The chip consumes only 120 mA of power and offers ECL-100K compatibility, which keeps logic levels constant through temperature and power-supply fluctuations. The device is available in 22-pin, 300-mil wide cerdip as well as in plastic dual in-line packages. In 100-unit quantities, the chip is priced at $88.50.

Integrated Device Technology
3236 Scott Blvd
Santa Clara, CA 95052
Circle number 139

Chip set emulates PS/2

A chip set is available that lets users emulate the IBM Personal System/2 Model 30, reduces non-memory chip count and improves system speed by 25 percent, according to the manufacturer. The three-chip set consists of the VL82C031 System Controller, the VL82C032 I/O Controller and the three-chip set is priced at $92.60, while the VGA chip is $38.60.

VL82C033 Disk Controller and Data Separator. In conjunction with the set, a Video Graphics Array (VGA) device is available that provides high-resolution graphics normally reserved for PS/2 Model 50 and higher. In quantities of 1,000, the

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8375 S River Pkwy
Tempe, AZ 85284
Circle number 140

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So, use this publication's bingo card to send for your free demo disk of the only network analyzer you'll ever need: LANWatch.

Runs on IBM PCs, PS/2s and compatibles under DOS 2.0 or later, with Western Digital, 3Com, MICO/Meridian, Proteon and other interfaces.

CIRCLE NO. 23
COMPUTER DESIGN OCTOBER 15, 1988 87
NEW PRODUCT HIGHLIGHTS

MAJOR SYSTEM COMPONENTS

VMEbus monolithic backplane features low-capacitive loading

Two 21-slot monolithic backplanes, the 024-139 and the 024-239, are designed for critical 32-bit applications and VMEbus speed. The six-layer design of the backplanes, with 3-oz power and ground planes, keeps ground shifts and noise potentials to a minimum. In addition, in-board termination contributes to reduced propagation times for the forward and reflected signals.

The optimized geometry design achieves clean transmission of bus signals with low crosstalk and features low-capacitive loading to ensure minimum propagation delays on VME interface circuits. The 024-239 differs from the 024-139 in that the J2 section has extra rows of ground pins to provide shielding between signal lines in I/O cables, which are connected to the A and C rows of each J2 connector.

Each backplane comes in three versions (designated -01, -02 and -03), differing in the types of connectors by which power is brought into the backplane. Customized models are also available. The price of the backplane is $1,150.

Industrial terminals comply with NEMA 4X specifications

Based on a high-resolution, 640×400-pixel electroluminescent display, the Model CV-10 solid-state terminal is built to the National Electrical Manufacturers Association 4X specification. The display is less than 4 in. in depth, weighs less than 6 lb and can withstand water, dust and dirt found in harsh industrial environments. Enclosed in polystyrene, the device can also tolerate electrical noise, magnetic fields and vibration, but doesn’t require any cooling fans or filters. The terminal comes with its own text and graphics support, which can produce 80-character×25-line text, 40-character×12-line double high/wide text and complete bit-mapped graphics. A touch-screen feature is optional. In 100-piece quantities, the unit is priced at $1,795.

Switcher series ranges from 40 to 150 W

Intended for low-power applications such as personal and mainframe computers and other microprocessor-based environments, the Gold Line series of switching power supplies offers outputs ranging from 40 to 150 W. These open-frame, dual-input units offer minimum efficiencies of 60 percent and are designed to meet MIL-STD-801D vibration/shock specifications. The switchers are capable of operating on dual-input voltages of either 90 to 132 V or 180 to 264 V ac, user-selectable through a jumperwire adjustment. All models feature built-in EMI filtering to prevent noise feedback onto the power line, reverse voltage protection, and overcurrent protection on the +5-V main output. Prices start at $60.

Power supplies plug to VMEbus systems

A family of plug-in dedicated power supplies for systems using VMEbus architecture, the NCR series features a TTL-compatible open-collector signal that verifies in-spec performance within 500 ms after power-on. Remote control is accomplished by using a 2.4-Vdc TTL signal as the ENABLE, and an open-collector signal as the DISABLE. While the standard models are usually adequate, factory customization is available to comply with special conditions. Three dc outputs are standard.

Emerald Computers
7324 SW Durham Rd
Portland, OR 97224

Hybricon
12 Willows Rd
Ayer, MA 01432

Sola
1717 Busse Rd
Elk Grove Village, IL 60007

NCR Power Systems
3200 Lake Emma Rd
Lake Mary, FL 32746
**SOFTWARE**

I **Software package brings parallel processing to Ada**

An implementation of Ada designed to run on the manufacturer's multiprocessor system, the Encore Parallel Ada Software Package allows multiple servicing of run-time requests in parallel. The software emphasizes the locking of data structures in the run-time rather than in critical code sections, allowing concurrent access to run-time services by multiple Ada tasks.

Multiple processes are preforked at execution start and are then dynamically available during program execution. Re-using these processes by assigning them to queued Ada tasks awaiting execution reduces the overhead involved in concurrent processing of these tasks.

The number of processes assigned to Ada task execution may be matched to the number of available processors and to the computational needs of others on the system. These optimizations, as well as the process scheduling strategy, are selectable by run-time parameters and don't require recompilation or relinking of the application.

A complete set of tools for compilation, program generation, library management, debugging and source code control are included. Prices for the package start at $20,000 for commercial users and $7,500 for educational users.

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<th>Encore Computer</th>
<th>257 Cedar Hill St</th>
<th>Marlboro, MA 01752</th>
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II **Ada compiler offers C performance**

The Tartan Ada compiler boasts benchmark performance competitive with optimizing C compilers. Code generated with the software for the Hennessey benchmark programs executed faster than the equivalent code generated by the Sun-3 C compiler in seven out of 10 programs. Tested both internally and at external beta sites, the compiler has completed the required government on-site testing for validation under ACVC version 1.9. The product line includes VAX-VMS and Sun-3 Ada compilers, and a VMS-hosted cross compiler to the MIL-STD-1750A.

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<th>461 Melwood Ave</th>
<th>Pittsburgh, PA 15213</th>
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| 68000 C compiler targets ROMable applications |

An optimizing Compiler for Motorola 68000 family systems, Crosscode C generates ROMable code for all 68000 family members, including the 68020 and the 68881 floating-point processor. Compiler output code is split into five independent memory sections that can be assigned into ROM or RAM as the user requires. Position-independent code can also be selected. Small and large models can be chosen for any target processor, with small models using 16-bit offsets for tighter code, while large models allow unlimited code and data sizes. Special facilities on the compiler let users locate their C code in memory. Prices start at $1,595.00. The library automatically detects which coprocessors (Weitek MW1167, Intel 80387 or 80287) are present at run time. If more than one is available, the math chip that will optimize performance is selected. The software supports arrays of up to 4 Gbytes and can access the entire protected mode address space of the 80386. The practical limit on array sizes is determined by the physical memory available in the computer. The price is $250.

| 80386 protected mode |

A library of one- and two-dimensional fast Fourier transform (FFT) and digital signal processing (DSP) algorithms, the NDP/FFT library is callable from the manufacturer's 80386 protected mode C and Fortran compilers, NDP C-386 and NDP Fortran-386. The library automatically detects which coprocessors (Weitek mW1167, Intel 80387 or 80287) are present at run time. If more than one is available, the math chip that will optimize performance is selected. The software supports arrays of up to 4 Gbytes and can access the entire protected mode address space of the 80386. The practical limit on array sizes is determined by the physical memory available in the computer. The price is $250.

| Micro Way | PO Box 79 | Kingston, MA 02364 | Circle number 149 |

III **Trademark Information**

UNIX is a registered trademark of AT&T Bell Laboratories. PAL and PALASM are registered trademarks of Monolithic Memories Inc. GEOMETRY ENGINE is a trademark of Silicon Graphics Inc. 386, 386SX, 376, Intel386, iRMK, iRMX, and ICE are trademarks of Intel.
### PRODUCT BRIEFS

#### Fast-settling FET-input op amp
The AD845 FET-input op amp features a typical settling time of 350 ns to 0.1% (for a 10-V step) into a 500-Ω/100-pF load. Starts at $9.50. **Analog Devices** [Circle 150]

#### Workstation for harsh environments
The RT-60 Unix workstation is designed for military and harsh industrial environments and provides approximately 5 Mips. Starts at $46,000. **RTG** [Circle 151]

#### Monolithic SRAMs
Using a four-transistor CMOS design, the DPS92256 32k×8-bit SRAM features low-operating power (50 mA max), TTL compatibility and access times as fast as 85 ns. Starts at $30. **Dense-Pac Microsystems** [Circle 152]

#### 21-in. gray-scale monitor for Mac II
Designed for use with the Macintosh II, the Silverview is a 21-in. gray-scale monitor capable of displaying from 2 to 256 shades of gray. Starts at $1,999. **Sigma Designs** [Circle 153]

#### 12-bit A-D converter
The ADC12B is a 12-bit dual-slope integrating A-D converter. The cell offers a nonlinearity specification of ±1 count as well as common-mode rejection ratio of 80 dB. **Sierra Semiconductor** [Circle 154]

#### PAL chip eases timing problems
The PAL2216 allows communication between two system components that aren't synchronized to a common clock. It has six edge-activated programmable flip-flops. Starts at $13.95. **Advanced Micro Devices** [Circle 155]

#### Disk subsystems for Sun
Designed for new and existing VMEbus Sun workstations, the CoDisk series of disk subsystems offers capacities from 330 Mbytes to 1.2 Gbytes in stand-alone cabinets. The disks are controlled by a proprietary 32-bit disk controller that takes a single slot in the Sun system. **Cosystems** [Circle 156]

#### Monochrome monitor
The GreyScale Bundle model RS9503 for PS/2s consists of a 14-in. flat-screen monitor and an Orchid VGA card. $545. **Relisys** [Circle 157]

#### Parallel/serial converter
The Mali Card matches parallel and serial data transmissions. Parameters can be set dynamically or with DIP switches. **Cartron** [Circle 158]

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**WHY SAFECON?**

Competition in the electronic device market is so intense that design turnaround time is becoming a major factor in the success or failure of a product. Thus, the popularity of ASICs (application specific integrated circuits) and design strategies that promise fast turn times for nearly-custom logic.

At the same time, the newest chips are increasingly complex and their performance depends more and more on efficient firmware. The information provided by vendors on how to use their chips is spotty and not always accurate. As end products become more sophisticated, firmware programming has become an increasingly large portion of the product development cycle.

Software components can provide a piece of the firmware solution. In some cases, these provide a leap forward in the development cycle. Standard software components provide continuity from project to project. But they must be well understood or they just add to the confusion.

The same difficulty lies in the use of high-level languages. Certainly, a programmer writes more code, faster, when using LISP, Pascal, or ADA, but compilers distance the programmer from the hardware—a serious limitation that must also be understood, especially for real-time applications.

Thus SAFECON, the new Software and Firmware Engineering Conference. SAFECON is the first forum to address these problem areas and provide applications knowledge on a highly-focused basis.

**WHO WILL ATTEND?**

The SAFECON attendee is a software engineer who generally selects the software and tools with little or no input from management.

At SAFECON, the attendee will get an in-depth education in the latest programming techniques, tools, and ways to use them in daily work. We call this "next-day education"—what is taught at SAFECON today can be used tomorrow. The emphasis is on practical knowledge, not abstract theory. Moreover, SAFECON gives the attendee enough information to make an intelligent selection of processors, support chips, software and development tools for his or her specific application.

Attendees will be drawn from Original Equipment Manufacturers (OEMs) that manufacture board and system-level products based on high-performance microprocessor technology.

Similarly, designers of peripheral devices, such as input/output devices, storage systems, communication products and consumer products ranging from blenders to televisions, will find SAFECON an ideal refresher on the latest real-time programming methods and the application of the latest controller technology.

**WHO SHOULD EXHIBIT AND WHY?**

The SAFECON exhibition and technical conference is an ideal forum for chip manufacturers and vendors of software-development tools (such as compilers, assemblers, CASE systems, software components and in-circuit emulation equipment).

SAFECON, with its technical program tightly coupled to the equipment exhibited, provides a unique one-on-one, in-person forum to meet quality attendees in an unhurried atmosphere. You'll meet developers specifically interested in software/firmware programming requirements related to high-end microprocessors.

**Seminar/Session Topics:** Understanding the new chips (Intel, Motorola, National, AMD, etc.), including bus structures, instruction sets, memory management, interrupt structure; Leveraging processor performance (registers, burst-made read/write operations to reduce bandwidth); Maintaining software quality (change control, testing); Multi-processing, peer processors) and more . . .

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The 1.5GHz MB810 discrete logic series and 1.0GHz MB1600 and MB1700 master slice series are designed for use in high-speed test equipment, instrumentation and general logic applications. And they're conventionally packaged in 16-pin cerdip and ceramic flat packs to provide performance at a lower cost.

What's more, you don't have to worry about compatibility, either. Because the MB880 and MB810 discrete logic series, and the MB1600, MB1700 and MB1800 master slice array series are logic-level compatible with ECL 10K and 10KH series.

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MX-3 6 Channel TDM Multiplexer $389.95. Features include: EIA RS-232 or CCITT V.24 interface—speeds up to 19200 bps—no modem needed up to 5000 ft—completely transparent to data format—DTED/IDCE switch selectable on each channel—composite link test for diagnostic—built-in lightning protection. Bo-Sherrel Co., Inc., 36133 Niles Blvd., Fremont, CA 94536 or phone (415) 792-0354.

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COMPUTER DESIGN OCTOBER 15, 1988 95
Control Data establishes separate disk drive group

In an effort to improve its marketing flexibility and ability to respond to customer needs, Control Data (Minneapolis, MN) is establishing its highly successful Data Storage Products Group as a stand-alone subsidiary operating under the moniker Imprimis Technology. Lawrence Perlman, Data Storage Group vice-president, will head Imprimis.

After a difficult few years in the mid-1980s, the Data Storage Group under Perlman has assumed a strong position in the disk drive industry with an array of high-capacity, fast-access 8.5¼ and 3½-in. Winchester drives. With its independent status, the new subsidiary will be free to seek strategic alliances, joint ventures and partnerships in the fast-moving disk drive industry and to sell a minority interest of its stock to the public.

Motorola and Cherry agree to exchange bipolar technologies

Motorola Semiconductor Products Sector (Phoenix, AZ) and Cherry Semiconductor (East Greenwich, RI) have agreed to collaborate to achieve compatibility in manufacturing processes for selected high-volume, bipolar linear ICs. Each company will have the technical capability to alternate source certain bipolar ICs designed by the other. The agreement will effectively offer better service to customers who require alternate supply sources for bipolar devices.

Mathematical application tools made for RISC

Customers wanting floating-point capabilities for the AM29000 32-bit RISC microprocessor from Advanced Micro Devices (Sunnyvale, CA) won't have to buy an accelerator chip or write extra code, thanks to an agreement between AMD and Quantitative Technology Corp (Beaverton, OR). Under the terms of the agreement, QTC will develop trap handlers to implement IEEE standard instructions that emulate all the functions of a floating-point processor chip in software. The trap handlers are best suited for systems with limited floating-point requirements, such as various embedded controller designs, spreadsheets, low-end workstations or simple statistics programs.

Space station contract targets gate arrays

International Microcircuits (Santa Clara, CA) has been awarded $8.75 million in production contracts for military-standard applications in defense, outer space and other high-reliability environments. Production quantities of the manufacturer's sub-micron gate arrays are being delivered to Rockwell International's Avionics Division (Cedar Rapids, IA) for use in the Navstar Global Positioning Satellite. In addition, Canadian Marconi (Montreal, Quebec), Singer's Kearfott Division (Wayne, NJ) and Magnavox Marine Division (Fort Wayne, IN) are receiving the gate arrays for use in NASA's space station project as well as other defense applications.

Apollo announces Portable Software Group

In what seems to be an industry first, Apollo Computer (Chelmsford, MA) has announced that it will offer object-code versions of its software to competing vendors. The newly formed Portable Software Group will open up three Apollo products to other users and vendors: the industry-standard Network Computing System, the Open Dialogue object-oriented interface creation system and the Network License Server, which provides for the concurrent usage licensing of software applications. Apollo's move seems to be an attempt to gain strength in the Open Software Foundation while positioning its software products as industry standards.
The Integrated PADS-Superstation™ is a new and powerful PC-Based Design Station that allows the Engineer or Circuit Designer to perform the entire design sequence from cradle-to-grave. Every decision required in the design effort, from Logic Capture to Printed Circuit Design, to 100% Connection Routing, to checking, to generating Manufacturing Aids, is made by the responsible engineer and implemented on a single, fully integrated CAE/CAD SUPERSTATION!

LOGIC CAPTURE

The PADS-CAE system maximizes Logic Capture automation, while allowing the engineer to concentrate on the design task. This high degree of automation results from the use of a new type of database: A Design-Oriented-Database. All drawing sheets of the design are simultaneously available - not merely a single sheet, as with most other Logic Capture systems.

Among the many advantages of this new database are Automatic (hands-off) entry of Reference Designation, gate and pin data, on-line real time data checking across all drawing sheets, rapid paging from sheet-to-sheet, and instantly available (no batching) Annotation Lists to both PADS-PCB and other board CAD systems using FUTURE.NET™.

The most tedious and error-prone phase of Engineering Documentation, i.e., Engineering Change Order (ECO), is easy with PADS. ECOs generated in either the Schematic, or the Board database are used to automatically (hands-off) update the corresponding database.

BOARD DESIGN

PADS-PCB is today's most popular board CAD System and is the heart of the Superstation. PADS-PCB has revolutionized Printed Circuit Board CAD expectations by demonstrating an alternative to today's $100,000 Work Stations. Thousands of designers, engineers, and Board Design Centers use PADS-PCB - and for good reasons: 1 mil resolution, 30 layers, large board (over 400 14 pin ICs per board), complete SMD support, fine line (1, 2 & 3 tracks between IC pins), both Analog & Digital capability, fast Air Gap & Data checking, Gate & Pin swapping, dynamic rubber banding, rats' nest display, interactive and auto placement, interactive & auto routing, and all required Manufacturing Aids (CAM).

PADS-PCB is tightly coupled, both to and from PADS-CAE, and from other Logic Capture systems using FutureNet™.

100% COMPLETION AUTOROUTING

The most demanding phase of board design is routing the connections; approximately 70% of the board design effort is spent in this time consuming, labor-intensive task. Every Designer and Engineer's dream is to have a 100% completion autorouter, and PADS-Superrouter™ brings this capability to the Superstation™.

Here's how it works: the Designer places the components on the board, selects the "Route" command, and the SUPERROUTER takes over, routing around the clock, hour after hour, performing this tedious task to completion, or near completion, while the Designer is involved in other tasks. It's that easy! PADS-Superrouter allows the designer to set up a routing strategy based upon the requirements of each board. A costed Maze Search algorithm, using obstacle hugging on a 10, 20, 25 or 50 mil grid, and up to 12 simultaneous layers attempts to achieve 100% completion. A Rip-up-and-Retry Algorithm is used to obtain this objective.

Following routing, an Ease-of-Manufacturing Optimizer prepares the board for maximizing the manufacturing yield. Bends and curves put in by obstacle hugging are removed, closely spaced tracks are unpacked, corners are made at 45°, and all possible Vias are removed. The results equal or exceed that of the most experienced board designer.

LOW PRICE

While the performance and functionality of the PADS-SUPERROUTER is equal to any Workstation at any price, its price is competitive with the very low cost PC-based CAD systems. The price has been structured to allow every engineer in the organization to have his/her own personal SUPERSTATION™.

EVALUATION PACKAGE

So that you can appreciate the impact the PADS-Superstation™ will have in your organization, we have created a Superstation Evaluation Package. It is available at no cost to qualified engineers and designers. Please call our Sales Department at (800) 255-7814; Inside Mass. (508) 486-9521.
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this LAN was made from yours and ours.

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