NEW!
from out of the West...

WESPERGROUP
DIMENSION SERIES

DEC COMPATIBLE CONTROLLERS

The Wespergroup Dimension series expands twofold in three dimensions. Wespergroup introduces six exciting new additions to the tape and disk dimension series:
THE TAPE DIMENSION Q-BUS COUPLERS TDQ-I AND TDQ-II. These couplers easily support the new tri-density "formatted tape drives" both in Start/Stop or Streaming modes. The TDQ-I supports Pertec interface tape drives, while the TDQ-II supports high speed Pertec, STC, and Telex interface tape drives using a 64K byte data buffer. Both couplers emulate the DEC TSV05.

THE DISK DIMENSION DEC UNIBUS CONTROLLERS DD-I AND DD-II. These controllers sustain up to four industry standard SMD interface disk drives. The DD-II handles up to two megabyte/second data transfer rate of the new SMD interface disk drives. The DD-I and DD-II emulate DEC RM02/03, RM05, and RP06 disk drives.

THE TAPE DIMENSION DEC UNIBUS COUPLERS TD-III AND TD-IV. These couplers support the new "formatted tape drives" with either STC, Telex or Pertec interfaces in Start/Stop or Streaming modes. The TD-IV includes a 64K byte multi-stage data buffer to upgrade the efficiency of the Streaming Drive in the write mode. Both couplers emulate the DEC TS II drives.

Call or write today for the complete Wespergroup catalog. WESPERGROUP, Div. of WESPERCORP (USA), 14321 New Myford Road, Tustin, CA 92680, Tel: (714) 730-6250, Cable WESPER, TWX 910-595-1775, Telex 4724629. (Germany) GmbH, Tel: 089 982420. (U.K.) Tel: (44) 0276-20934.

DEC, Unibus and Q-Bus are registered trademarks of Digital Equipment Corporation.
Model 6455 Cartridge Tape System

Loaded with Features —
Loaded with Benefits.

Kennedy products have always provided innovative new features. And these features have always provided added benefits and convenience for the user. For instance, our Model 6455 offers these features and benefits:

**Feature:** Start/Stop Operation
**Benefit:** Drive can emulate a ½" tape drive by providing the ability to perform selective file back-ups, file-restructuring, journaling and software updates. The drive is effectively a ½" Tape Drive in a smaller package.

**Feature:** Hard Read Error Spec. of 1 in 10^11 bits.
**Benefit:** Best data reliability of any tape cartridge drive. Gives the user confidence in the integrity of the back-up medium.

**Feature:** On-board Diagnostics
**Benefit:** Drive can be tested off-line with no test equipment required. Use of S.A. also lowers the MTTR.

**Feature:** Cartridge Jam Protection
**Benefit:** Protects the cartridge from damage if cartridge jams. This is accomplished by sensing a current surge and then disabling the motor, thus insuring that the cartridge will not be damaged.

**Feature:** High Density Recording
**Benefit:** Storage capacity of 23 MB on a single cartridge.

**Feature:** Optional industry standard ½" tape interface.
**Benefit:** Operates with existing tape couplers and software. The drive operates as though it were a ½" tape drive without having to modify existing hardware or software.

By now you can see what we’re driving at. Model 6455 is full of unique features and benefits for you. For the complete story, write or call us today.

KENNEDY
An Allegheny International Company
1600 Shamrock Ave., Monrovia, CA 91016
(818) 357-8831 • FT TELEX 472-0116 KENNEDY
TWX 310-472-0116 KENNEDY

KENNEDY • QUALITY • COUNT ON IT
CIRCLE 2
MDB’S 32-BIT UNIX SYSTEM IS WAITING FOR YOU

You’ve asked for a 32-bit computer system with unlimited expansion capabilities... one that is low-cost and compact yet powerful enough for multi-user, multi-tasking requirements.

So we created the MDB Micro/32 an MC68000** based system with 512KB memory (expandable to 4MB). This powerful system combines MDB’s REGULUS*** with the incredible expansion capability of our place Q-Bus**** repertoire of peripheral controllers... as well as our interfaces/multiplexors for all communication modes, protocols and disciplines.

The result: speed, power and versatility of systems design you can’t get anywhere else!

REGULUS is MDB’s UNIX... the most advanced and powerful version in the world. Featuring user source compatibility with UNIX V6, 7, and System III, REGULUS offers complete support of all UNIX kernel features, multi-key B-tree ISAM and VAX/PDP-11**** cross support, and a host of operating systems and command functions not available in any other UNIX.

We speak your language too. Under REGULUS you can also have BASIC, FORTRAN, COBOL, PASCAL and DIBOL, in addition to most other popular compilers, utilities and special software packages.

Best of all, you don’t have to wait. It’s all available now. Call us today for complete information.

*UNIX is a Trademark of Bell Laboratories. **MC68000 is a registered Trademark of Motorola, Inc. ***REGULUS is a Trademark of Alcyon. ****Q-Bus, VAX PDP-11 are Trademarks of Digital Equipment Corporation
French private branch exchange enters U.S. market

Although it is fashionable to expound on the "upcoming next generation" of equipment (see staff report, p 149), some companies are content to nibble away at a "real" market by offering equipment of a "before-the-next" generation caliber. For example, Jistel of Stamford, Conn has introduced a family of analog and digital private branch exchanges (PBXs) with which the company hopes to capture a 4- to 6-percent share of the U.S. market by 1987. (Jistel is a division of JS of America Inc, which in turn is a subsidiary of Jeumont-Schneider of Puteaux, France.) The U.S. PBX market—40 percent of that worldwide—is relatively free of the restrictions imposed in European countries. Also, the breakup of the Bell Telephone System offers an even more lucrative target for competitive companies.

Two analog voice-only systems available this quarter are time division multiplex switches using pulse amplitude modulation techniques. Jistel 95 has a capacity for 16 trunk lines and can accommodate 80 stations, while the Jistel 200 handles 32 trunk lines and 208 stations. Both products have been in use in France and other European countries for several years, but are reconfigured to adhere to U.S. FCC regulations and to match U.S. PBX competitive features. Two digital products, the 150 and 500, to be available in the last quarter of 1984, will be able to route both voice and data at a 56-kbit/s rate.

"Concept-processing" workstation links to powerful computing

For the most part, array-based schemes favored for developing artificial intelligence, robotics, vision systems, and signal processing applications have been ideas in search of a practical development tool. To that end, Analogic Corp (Wakefield, Mass) has created its APL Machine, which turns an unmodified IBM PC into a programmer's workstation fronting its 10-MFLOPS, 32-bit AP500 array processor. Under a Unix-derived operating system, the PC runs the International Standards Organization-validated APL written on its own or outside hardware. The APL interpreter runs in the 12.5-MHz, 16/32-bit micro control processor; primitive functions and operators of APL reside in pipeline microcode. In addition, the company provides Unix-like shells that incorporate non-APL code for applications using compiled or assembled code.

Macintosh or Granny Smith?

The high stakes personal computer game gets yet another raise in the form of Apple's long-awaited Macintosh. By spurning the pack and IBM PC compatibility, Apple is clearly drawing a line in the dirt. The 68000-based machine will have a Lisa-like operating environment such that Macintosh programs will run on the Lisa but not vice versa. The machine should also give a big boost to acceptance of the 3½-in. floppy disk that Hewlett-Packard is already using in its PC-compatible model 150. Apple is emphasizing support for independent software developers, and at the price of $2495, Macintosh (if it makes it in the initial post-introduction phase), should give the competition a real run for the money. The basic price includes a word processing program (MacWrite) and a graphics package (MacPaint). Apple has also introduced three new models of Lisa: Lisa 2, 2/5, and 2/10, all software compatible with the Macintosh.

Seeq to produce high endurance EEROM

One million write cycles per byte is to be the new standard for electrically erasable ROMs produced by Seeq Technology (San Jose, Calif). The 5516A, a 16-Kbit (2-K x 8) EEROM, will hopefully encourage more design-in by designers wary of write limitations in EEROMs. The part has an onchip timer and a write cycle time of 10 ms. Seeq offers the million-write version as a high endurance version of its existing 2816A. Future products will include high endurance versions of existing parts as well as yet unannounced million-write EEROMs and other ICs incorporating the high endurance "Q cell" technology onchip.
Motorola completes CMOS RAM tests for VHSIC program

Engineers at Motorola Semiconductor (Phoenix, Ariz) have completed tests on a 4-port silicon-gate CMOS RAM as part of phase I for the Department of Defense's very high speed integrated circuit (VHSIC) program. The 4-Kbit chip is believed to be the first bulk CMOS part manufactured using Motorola's 1.25-µm HCMOS design rules. In operation, the RAM can have two independent addresses read out while two other independent addresses are being written into it, all using a single 25-MHz clock. The part is slated for an electronic warfare application for which Motorola's VHSIC partner, TRW Inc (Redondo Beach, Calif), is supplying the brassboard. The memory IC is functionally compatible with TRW's triple-diffused bipolar parts, with both types of circuits operating off a 3.3-V power supply. With 12 transistors/memory cell, the 290- x 313-mil memory chip contains a total of 59,700 transistors. This translates to a functional throughput rate (FTR) of $10^{11}$ gate•Hz/cm$^2$ which, in turn, requires 300 mW of power to dissipate. The next challenge for Motorola engineers is to build a 6-Kbit CMOS gate array chip that will also be compatible with the other chips on TRW's brassboard. (Sperry Corp is a third member of the program team.)

IBM PC backs Unix

IBM Information Systems Group (Rye Brook, NY) has announced its flavor of Unix for the IBM PC. Known as the personal computer interactive executive system (PC/IX), the operating system implements a superset of Unix System III with an interactive full-screen editor. The minimum configuration needed is 256 Kbytes of RAM, a single 320-Kbyte floppy disk drive, and a 10-Mbyte rigid disk drive. The Unix port was done by Interactive Systems (Santa Monica, Calif). It will be ready for release at the beginning of April.

Industrial computer slides in processing capability

Departing from the traditional shared logic approach of single CPU systems, Indocomp, Inc's (Drayton Plains, Mich) IMP-68000 depends on independent processors. Each processor runs its own operating system and executes its own application programs. This prevents one processor crash from affecting other running processes. Slide-in processor boards (all front accessible) consist of a standard processor section and a customized I/O section. Current I/O sections include both digital and analog boards as well as a development board with predrilled holes and a large wirewrap area.

TI and Fujitsu to alternate source bipolar, CMOS arrays

At a still-unannounced future date, Texas Instruments (Dallas, Tex) will supply gate array products based on design and fabrication information from Fujitsu Ltd (Santa Clara, Calif). This alternate-source agreement between the American and Japanese semiconductor giants covers both bipolar and CMOS devices. Specifically, these will be bipolar Schottky TTL arrays with 1.9-ns delays in densities ranging from 240 to 1100 gates; and H-series and VH-series CMOS arrays in densities from 440 to 8000 gates. Both TI and Fujitsu have proprietary computer aided design systems and design languages. To aid customers, each company will provide the means to accept circuit descriptions written in the other's language and convert them to produce guaranteed compatible parts. The companies emphasize that Fujitsu is giving TI parameters for producing compatible designs rather than actual process technology.
send me your 16-page brochure detailing BULK SEMI. Please call me to discuss my application.

Title

Company

Address

City State Zip

Telephone

Minicomputer

WHAT'S THE BIG IDEA?

☐ Send me your 16-page brochure detailing BULK SEMI.

☐ Please call me to discuss my application.

Name __________________________ Title __________________________

Company __________________________

Address __________________________

City __________________________ State __________ Zip __________

Telephone __________________________

Minicomputer __________________________

CIRCLE 4
System technology

27 Interface:  
Thirty-two bit system designers face decision time

49 Software:  
Local area networks proliferate while standards lag

56 Integrated circuits:  
Chip finds degree of similarity between strings

64 Data communications:  
Terminals move to X.25 transparent to host

System design

73 Microprocessors/microcomputers: Triple-bus architecture gains speed, versatility  
_by Dave Cane and Steve Mullen_—Both problems and opportunities lurk for designers of realtime minicomputer systems. A three-pronged approach attacks the problems inherent to single-bus architecture.

89 Data conversion: How vocabulary is generated determines speech quality  
_by Michael W. Hutchins and Lee Dusek_—Synthetic speech vocabulary can be generated by analyzing natural speech or by artificial construction from phonetic parts, with differing results.

105 Computers: Array processor achieves 100 MFLOPS  
_by Robert Hausman and Phil Cannon_—Parallel architecture and fast hardware team up with a resident operating system to speed data flow and minimize host communication.

121 Computers: Using an efficient microarchitecture achieves goals  
_by Kenneth Burns and David M. Burns_—Careful microarchitecture planning enables design engineers to achieve dual goals of low cost and high performance in a 32-bit computer.

137 Microprocessors/microcomputers: Motor control system design hinges on processor delays  
_by Manuel R. Cereijo_—Microprocessors are a boon to motor-speed controllers, but certain limitations of the devices must be accounted for in system designs.
This month's data communications report includes many of the same local network topics discussed here a year ago. A few new choices and some extra flavored ingredients for the established entrees, however, add spice to the computer designer's menu. With digital PBXs giving LANs a run for their money, and LSI chips making the final choice between the two ever so difficult, the engineer will have to study this year's menu carefully before making the "right" selections. Bon appetit!

This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

System components

243 Transputer—a programmable component that gives micros a new name
246 Graphics system functionality swells with million addressable points
246 Low cost plotter combines graphics command set and offline operation
248 Laser-based optical disk drive stores 1 million bytes
248 Open architecture characterizes programmable handheld computer
250 Compact station engineers hierarchical VLSI design system
250 Condensing architecture makes small system perform big
252 Winchester/floppy controller rules over diverse disk selections
252 Portable operating system easily adapts to specific microcomputers
259 Data communications
260 Interface
262 Test & measurement
264 Memory systems
265 Peripherals
267 Microprocessors/microcomputers
268 Data conversion
270 Development systems
274 Integrated circuits
275 Software
278 Interconnection & packaging
280 Computers
282 System elements
289 Control & automation
291 Power sources & protection

Departments

3 Up front
11 Editorial
17 Letters to the editor
294 Calendar
297 Literature
300 Designer's bookcase
303 System showcase
306 Advertisers' index
315 Reader inquiry card
315 Change of address card

Editorial reviewer
for part of this issue:
D. Iuster, Sr
You'll never get trapped into dead-end designs with
Here's more proof that nobody does more to extend the life of your 8-bit designs than Zilog. Because now you can increase 8-bit Z80* performance up to 6 MHz with the high-speed Z80B CPU and its family of peripherals. You can join the hundreds of design engineers that have already tested this claim with winning results. Or wonder...

Is there something here they know that you don't?

Like the fact that the Z80B CPU has the same 158 instruction set and the elegant registers and interrupts that you're used to working with, but runs them 50 percent faster than the Z80A chip?

That the Z80B processor is completely software compatible with the rest of the Z80 family, permitting you to upgrade to higher performance without getting trapped into software redevelopment? That software compatibility also means you can use the Z80B device in co-processing and/or multi-processing environments along side our other Z80 processors?

And consider the fact that you can surround our Z80B CPU's with a complete family of Z8400 and Z8500 peripherals and really boost system performance. They help you keep your parts and space requirements to a minimum and increase system throughput because we build more functions into every device. The peripherals include a PIO, a CTC, an SIO, an SCC, an FIO, an FIFO, a CIO, and a UPC.

For complete specifications and applications data on the Z80B and peripherals, fill out the coupon and mail to: Zilog, Inc., Components Tech. Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008. Or call our TOLL FREE Literature Hot Line at 800-272-6560. For information on Zilog's other components, call (408) 370-8000.

Z80 is a registered trademark of Zilog, Inc.

☐ I'd like more information at this time.
☐ Please have a salesman contact me.

Name:
Title:
Company:
Address:
City         State         Zip
Phone

Z80B/Peripherals
Hitachi introduces the new standard in Hi-Resolution. That standard is embodied in our new HM-4619 RGB Color Monitor.

The HM-4619 delivers flicker-free images with 1280 x 1024 resolution at 60 Hz. Hitachi tube technology leadership has created a new in-line gun delivering high brightness with sharper focus. All of this is enhanced by our Digital Dynamic Convergence™ of 0.1/0.3 mm.

The Hitachi line of RGB Color Monitors is rapidly becoming the clear choice of OEM's throughout the world. We feel our new, top of the line, HM-4619 is the unit which will set the standard by which all other color monitors will be judged.

- New In-Line Gun with Hi-Brightness and Sharp Focus
- 1280 x 1024 Resolution at 60 Hz
- 0.1/0.3 mm Misconvergence
- 100 MHz Video Bandwidth
- Compact Design
- Cost Effective State of the Art Technology Plus the Strength of Hitachi Worldwide Support

Hitachi America, Ltd.
59 Route 17S, Allendale, NJ 07401
(201) 625-8000
3540 Arden Road, Hayward, CA 94545
(415) 763-9400
Hitachi Europe Ltd. 10th Floor
London Wall, London EC2A 2AS
(01) 606-7831
Hitachi Denki Canada Ltd. 65 Melford Drive
Scarborough, Ontario, Canada M1B 2S6
(416) 299-5800

H-I?-Hitachi America, Ltd.
computer graphic courtesy of METHEUS Corporation, Hillsboro, Oregon

CIRCLE 6
THE COMPUTER ILLITERACY THREAT

Many years ago, we knew a fellow who sold encyclopedias. His selling technique was brutal but quite effective. Usually, he would work low income neighborhoods, going from door to door. If the prospects had children, he would ask if they wanted their kids to grow up as poor and uneducated as their parents. Except in those cases where the door slammed in his face, it was then surprisingly easy for him to convince the concerned parents that the purchase of a set of encyclopedias on an easy payment plan virtually guaranteed that their kids would become prosperous geniuses.

Today, unfortunately, many personal computers are being sold in a similar fashion. Now we are starting to read and hear a lot about “computer literacy” without which, it is said, our children will not be able to survive in an increasingly competitive and computerized world. Yet, although many people talk about computer literacy, nobody ever bothers to define it. Therefore, we are not sure whether it means the ability to play a fair game of Pac-Man, or the ability to write device drivers in assembly code. Either way, however, the skill does not seem to have any particular relevance to survival in tomorrow’s business world.

Computer system designers know that, by the time today’s schoolchildren join the workforce, a business computer will be no more difficult to use than a typewriter or telephone. Tomorrow’s computer users will not have to worry about the subtle quirks of operating systems, just as today’s users do not have to get Cobol programs keypunched onto decks of cards. Yet, the public seems to have been brainwashed by the computer literacy argument that has been pounded home by repeated TV commercials. People today ask engineers not whether they should buy a personal computer, but only which one to buy.

In a few years, it is very possible that personal computers will provide convenient educational workstations at which children can learn, draw, write, and calculate. So far, however, most educational software is so abysmal that a computer is a needlessly expensive replacement for a conventional blackboard and textbooks.

Apart from maintaining the financial health of computer companies, therefore, we see no urgent need to accelerate the introduction of personal computers into the school or home. Certainly, we see no overwhelming national benefit in such proposed legislation as HR701—a bill introduced by Congressman Fortney Stark of California—which would give computer makers a double tax write-off for donating their computers to schools. If we as engineers push too vigorously for such legislation—in the misguided hope that it will aid the computer industry—we may find that we have lost our professional credibility when the fad has passed and unused personal computers are littered around like Rubik’s Cubes or Pet Rocks. Yes, computers should have a bright future in business, the classroom, and the home—but not if we kill the industry with premature and excessive hype.

Michael Elphick
Editor in Chief
Write or call for a free Sunnyvale poster and all the facts on our memories.
If you’re looking for the world’s fastest MOS static RAMs, don’t look in Holland. Searching for the world’s fastest bipolar PROMs? Forget Texas or Arizona. And you won’t find the world’s fastest EPROMs anywhere near Mt. Fuji. They’re all right here in Sunnyvale. At Advanced Micro Devices.

**Everything we make is fast. Including the Am27256, the world’s fastest 256K EPROM.**

The Am27256 is 170ns fast. It’s the only EPROM quick enough to keep up with a 10MHz MPU without a wait state. And we’ve got the 40ns Am27S43A, the world’s fastest 32K bipolar PROM. And the 35ns Am2167, the world’s fastest 16K static RAM.

With leading-edge parts like these, it’s no wonder memories account for half our total sales. And our other products are just as hot. Controllers. Bipolar and MOS microprocessors. Communications circuits. Signal processors. We’ve got ‘em all, and then some.

And every single chip meets or exceeds the International Standard of Quality.

Next time your design demands high performance memories, or any high-performance parts, look us up. We put high performance on the map.

---

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088
For direct factory response call (408) 749-5000. Outside California, call toll free (800) 538-8450, ext. 5000.

CIRCLE 7
MORE STORAGE FOR LESS

DEC USERS

LSI-11 COMPATIBLE

EMULATION RK06/RK07
42MB Winchester/Floppy (8") $6995.00
70MB Winchester/Floppy (8") $7495.00
140MB Winchester/Floppy (8") $9995.00

EMULATION RL02
10MB Winchester/Floppy (8") $4995.00
20MB Version Add $500.00

ALL SYSTEMS CONTAIN 2MB OF FLOPPY BACKUP

MORE MEMORY ON A SINGLE CARD THEN ANY OTHER MANUFACTURER

512KB TO 2MB QBUS ERROR DETECTING AND CORRECTING MEMORY

CALL FOR MORE DETAILS!

OFFERING QUALITY WITH AFFORDABLE PRICING

Chrislin Industries, Inc.
31352 Via Colinas • Westlake Village, CA 91362 • 213-991-2254
TWX 910-494-1253 (CHRISLIN WKGV)
RK06, RK07, RL02, QBUS, DEC, LSI-11 are trademarks of Digital Equipment Corporation.

CIRCLE 8

FREE PUBLICATIONS

Use the handy order form in the tax package to obtain free IRS publications on over 90 different tax topics.

A PUBLIC SERVICE MESSAGE FROM THE INTERNAL REVENUE SERVICE

COMPUTER DESIGN

Editor in Chief, Michael Elphick
Managing Editor, Sydney F. Shapiro
Senior Editors, John Bond Peg Killmon
Senior Associate Editor, Deb Hightberger
Associate Editor, Malinda E. Banash
Chief Copy Editor, Leslie Ann Wheeler
Copy Editors, Helen McElwee Lauren A. Stickler Jack Vaughan

New York Field Office
Senior Editor, Nicolas Mokhoff
Special Features Editor, Harvey J. Hindin
230 Park Ave, Suite 907, New York, NY 10169,
Tel: 212/986-4310

Western Field Offices
Managing Editor, Tom Williams
540 Weddel Dr, Suite 8, Sunnyvale, CA 94086,
Tel: 408/745-0715
Field Editor, Sam Bassett
1714 Stockton St, San Francisco, CA 94133
Tel: 415/398-7151
Field Editor, Joseph A. Aseo
331 Freeway Center Bldg, 3605 Long Beach Blvd, Long Beach, CA 90807,
Tel: 213/426-1172

Publisher, Gene Pritchard
Marketing Director, Robert A. Billhimer
Circulation Director, Robert P. Dromgoole
Production Assistant, Philip Korn
Design Coordinator, Lou Ann Morin
Technical Art, Designline

PennWell PUBLISHING COMPANY
Advanced Technology Group
119 Russell Street, Littleton, MA 01460
Tel: 617/486-9501

H. Mason Fackert, Group Vice President
Saul B. Dinman, Editorial Director
David C. Ciommo, Controller
Steve Fedor, Promotion Director
Linda G. Clark, Marketing Services/PR Manager
Linda M. Wright, Production Director
Wanda Holt, Data Services Manager
Pat Armstrong, Administrative Services Manager
It's just not fair
to claim that TEMPLATE® is the
best graphics software available.
Our competition's already
discouraged.

And we like competition. We really do. It's just that it's difficult, if not
impossible, to find graphics software as efficient and functional as
TEMPLATE. Try as you might. TEMPLATE is the hands-down winner. With
true device-independence and intelligence, total graphics functionality
for CAD, scientific analysis, seismic work, process control, molecular modell­ing, and a host of other applications.

In almost any environment, whether it's batch or
interactive, 2D or 3D, TEMPLATE wins. Benchmark
tests prove it. TEMPLATE, besides being a true 3D
graphics package for 32-bit or larger computers, features
powerful commands that provide matchless produc­tivity. TEMPLATE makes optimal use of available com­puter resources, giving you fast, efficient computer
graphics program execution. And it supports over 125
graphics devices, from dumb termi­
als to sophisticated systems.

We also provide on-site installation and training,
continuous updates, a regular flow of new device
drivers, and ongoing documentation. What's more,
we back you up with a telephone hotline so
TEMPLATE software specialists can provide help
if you need it.

But let's be fair. If you're look­
ing for graphics software, call our competitors first. Find
out what they have to say about theirs. Then call us,
and find out why TEMPLATE really has no competition.

And why the competi­tion
has been so discouraged
for so long.

CIRCLE 9
Like DEC's.

$8,845 system price*

256 KB minimum... up to 4 MB!

8-quad slot Q-BUS card cage

Supports RT-11, RSTS, RSX-11M-PLUS, UNIX, and TSX-PLUS

Two fans in card cage area (vs. one in Micro/PDP-11)

RL02-compatible 5½" Winchester disk; 10 MB, 20 MB, or 40 MB capability

Cartridge tape capability

Media and software compatibility with DEC's RX02 8" floppy (vs. Micro/PDP-11's non-compatible 5½" floppy)

1.0 MB floppy disk back-up (vs. 2 x 400 KB for Micro/PDP-11)

Only better.

You can buy DEC's Micro/PDP-11 with its impressive array of features... or you can get Dataram's A22—an LSI-11/23 based minicomputer that gives you a whole lot more... for a lot less dollars! Like an 8" RX02-compatible floppy, 40 MB 5½" Winchester and ¼" cartridge tape capability. And two fans that provide push-pull air flow in the card cage area.

For more information, forward this coupon to us, or, for faster response, call (609) 799-0071.

☐ Send information. ☐ Contact me immediately.

Name

Company

Address

City  State  Zip  Phone

Dataram Corporation, Princeton Road, Cranbury, NJ 08512

CD284

*$8,845 is single-quantity domestic price for A22 with LSI-11/23, 256 KB, 10 MB Winchester and RX02-compatible 8" floppy.

DEC, LSI-11, Micro/PDP, PDP, RSTS, RSX, and RT-11 are trademarks of Digital Equipment Corporation.

TSX-PLUS is a trademark of S&H computer systems, inc.

UNIX is a trademark of Bell Laboratories.

Dataram Corporation  □ Princeton Road  □ Cranbury, New Jersey 08512  □ Tel: 609-799-0071  □ TWX: 510-685-2542
Identifying management differences

This is written in response to your editorial (Oct 4, 1983) entitled “Wa Versus the Gunslingers.” I believe that you identified the main point of management style differences. American managers seem to love a crisis where they can fumble or manage their way through it. Japanese managers consider a crisis, any crisis, a management failure. Simple, isn’t it? But what a difference.

Eugene S. Redner
Digital Equipment Corp
146 Main St
Maynard, MA 01754

Another look at the IEEE

Congratulations on the Nov 1983 editorial “Democratizing the IEEE.” I am sure that Mr Elphick has done the IEEE and the profession a great service by airing some of our dirty laundry in public. Perhaps this will lead to less dirty laundry.

The editorial was of special interest to us in Rochester, because Malcolm "Mac" Drummond is a Rochestrian, and is active in local Section activities. With your kind permission, I would like to reprint your editorial in The Rochester Engineer. It is a monthly publication of the Rochester Engineering Society, and carries several pages of IEEE news, as well as news from other member engineering societies. The total circulation is, I believe, in excess of 3000, including about 1400 IEEE members.

I hope that you are able to continue to present, on occasion, an unsanitized view of the IEEE. The only other unbiased source of information on IEEE doings seems to be EE Times.

Jacob Z. Schanker
IEEE, Rochester Section
65 Crandon Way
Rochester, NY 14618

I just got to the Nov 1983 IEEE editorial. I hope you voted for Irwin Feerst and also sent his committee a contribution. Perhaps your editorial and others will help get IEEE back on track, but I doubt it. I quit several years ago and haven’t had any second thoughts.

Jonathan A. Titus
The Blacksburg Group, Inc
PO Box 242
Blacksburg, VA 24060

The Nov 1983 editorial, “Democratizing the IEEE,” was terse and to the point. Simply put, the IEEE does not support the group that supports it—the working engineer.

Your identification of Edward J. Doyle (IEEE’s former VP for Professional Activities) as of Dec 31, 1983) as the villain in the RCA pension dispute was correct. And in the furor surrounding the “return home” clause of the pending immigration bill (which would require that all foreign graduates of American colleges return home for at least two years) you were also correct. So long as this important position is selected by IEEE’s Board of Directors and not elected by the membership, there is little hope that the VP for Professional Activities will reflect the wishes of the membership.

For this reason, we are sponsoring an amendment to IEEE’s constitution that would make this position an elective one. Interested readers may obtain a copy of the petition form by writing to the undersigned.

Irwin Feerst
Committee of Concerned EEs
PO Box 19
Massapequa Park, NY 11762

A different look at the IEEE

The perennial gadfly, Irwin Feerst, has received so much unwarranted press coverage, the effect is nauseating. The Nov 1983 issue of Computer Design carries another of his unsubstantiated diatribes. Not only that, Mr Michael Elphick, editor in chief, joins him in belittling IEEE procedures and policies. I expect more mature journalism. IEEE is by no means perfect, but as many times as Irwin Feerst has run and been rejected by the majority of its members, he and Michael Elphick ought to be getting the message. While Mr Elphick may have a valid point in the case of Mr Lewis and Mr Drummond, he cannot be trusted if he associates himself with Mr Feerst. Computer Design ought to be able to do better.

Jens J. Jonsson
Brigham Young University
Electrical Engineering Science Dept
Provo, UT 84602

The Nov 1983 editorial, “Democratizing the IEEE” is in tune with the loud noise exerted by the street people who are always fortified by "coke" and weeds. Legislation requiring alien engineering students to return home upon graduation is a pathetic political attempt to rectify inexorable economic facts. The logic behind it is equivalent to saying that we had better ship Einstein back to Germany, because he is competing unfairly with Americans.

Legislating import quotas for computers, autos, and engineers is simply a frank admission of mediocrity. It is untenable in a free market. Trying to "democratize" IEEE will have no effect whatsoever. Your editorial efforts will be more appreciated if you will stick to developing better guidelines for computer design.

Frederick Marich
Amdahl Corp
110 Seville Way
San Mateo, CA 94402

In my editorial, I never took a position either for or against a return-home clause for foreign engineering students. I merely proposed that the IEEE should be responsive to the wishes of the majority of its members. In the absence of a formal referendum, we still do not know the majority position on this issue. Apparently, the IEEE’s Professional Activities Committee changed its position without consulting the membership. This indecisiveness undermined the credibility of any position the IEEE might adopt and also forced the resignation of an energetic volunteer worker. If the IEEE persists in taking positions on major issues without polling the membership, its leadership must take full responsibility for their actions. This makes them fair game for editorial comment and for criticism from people like Irwin Feerst who suspect they are motivated by narrow corporate and academic interests.

Michael Elphick
Editor in Chief

(continued on page 20)
CONTROL DATA:
AFTER 25 YEARS,
STILL THE LEADER IN
THE PERFORMING ARTS.

Designing peripherals with exceptional performance is as much an art as a science. We know. We’ve been doing it since 1962. From the beginning, we’ve been dedicated to giving you solutions to on-line and back-up storage needs. Example: the Storage Module Drive (SMD) we introduced became the industry standard for removable media disk drives. The SMD is just one of the high-performance products that helped make us the world’s leading independent supplier of storage peripherals.

We’re still adding star performers to our product family. The LARK with a combined 50 Mbytes of fixed and removable media. The WREN high-performance 5-1/4” winchester drive. The Sentinel 1/4” cartridge streaming tape drive and the RSD that provides 80 Mbytes of removable media in a unit one-half the size of the original SMD.

Today there are more than 35 different products designed to help you meet any storage or back-up requirement, with maximum reliability and low cost of ownership built right in.

There’s more—the direct support that Control Data offers. We can deliver maintenance on everything we make. So wherever your customers are, Control Data peripherals can be counted on for less downtime and more productivity than unsupported products. Our spare parts programs help ensure that your reputation for excellent service with your customers is backed to the hilt, 24 hours a day, 365 days a year. In the United States and around the globe.

Add to this the commitment to research, to development and to manufacturing quality that a corporation the size of Control Data contributes, and you’re looking at precisely the kind of performance that makes our OEM peripherals top-rated in independent preference studies year after year.

Every performance needs a program. We’ll send you one free: our new 48-page OEM products catalog. Write OEM Product Sales, Control Data Corporation, P.O. Box 0, HQN08H, Minneapolis, MN 55440.

CIRCLE 12
Marketing chip sets

I find it necessary to elaborate on a statement made in Joseph Aseo's article, "Processors Divorced from Peripherals with Separate 1/O Bus" (Nov 1983, p 64). The statement "NCR Corp also showed an interest in marketing chip sets" is somewhat ambiguous. NCR Corp was one of the earliest promoters of the SCSI standard, as appreciable marketplace advantages would be available with the creation of this SCSI "universal bus with generic commands" standard. In fact, NCR Corp's Microelectronics Div was the first semiconductor manufacturer to bring a commercially available SCSI protocol controller packaged in a 48-pin DIP to the OEM marketplace.

The NCR 5385 SCSI protocol controller, supporting the 1.5-Mbyte/s data transfer rate and arbitration, was first released in Electronic Design (Apr 1983). Since then, the device has been available directly from NCR's Microelectronics Div Colorado Springs facility, as well as through distribution. As you can see, not only is NCR Corp interested in marketing this standard device, we are actively pursuing it.

Michael B. Burchman
NCR Corp
Microelectronics Div
1635 Aeroplaza Dr
Colorado Springs, CO 80916

Forth is core of CATS-1 system

In the report by Nic Mokhoff, entitled "Artificial Intelligence Systems Make Their Mark" (Nov 1983, p 33), Lisp is described as the core language in expert systems. The accompanying photograph identifies the CATS-1 system for locomotive repair as an example of an expert system. The CATS-1 system was programmed in Forth. For references, see the article by Harold E. Johnson and Piero P. Bonissone, "Expert System for Diesel Electric Locomotive Repair," The Journal of Forth Application and Research, vol 1, no. 1, Sept 1983.

Harvey Glass
University of South Florida
College of Engineering
Tampa, FL 33620

The article "Artificial Intelligence Systems Make Their Mark" (Nov 1983, p 33) conveys two misconceptions. First, the expert system used in the CATS-1 system of General Electric was actually implemented in Forth and not Lisp, as the article implies. Nowhere in the article is it mentioned that any environment other than Lisp is suitable for artificial intelligence, whereas in fact many other environments are used. The Japanese, for instance, are scheduled to use Prolog.

Secondly, a consequence of the first misconception is the impression that the best machines for development work in artificial intelligence are optimized for Lisp. Since expert systems are very small when implemented in Forth, and since Forth is implemented on more different machines than any other high level language, there is a good chance that the particular machine already available to the knowledge engineers will probably be cheaper to configure for artificial intelligence (in time and money) than a new dedicated Lisp processor. In fact, Lisp itself has been implemented in Forth, and could still be used if necessary.

Paul Thomas
Inner Access Corp
PO Box 888
Belmont, CA 94002

Updating specifications

As a communicator for Gould CSD, I am constantly working with our development and product planning people to keep abreast of changes in our product line. It is not easy. We work in an industry where specifications and performance figures are constantly being revised upward as a result of enhancements in hardware and software. Therefore, I can understand how difficult it is to keep up with the specifications for multiple vendors when doing a report like "Superminis: Changing Direction for the Future," by Peg Killmon (Nov 1983, p 167). For the record, however, I would like to correct some factual errors in the report.

First, in recent benchmark tests, the Gould Concept 32/87 computer performed 5.6 million Whetstone instructions per second (MIPS). This is a significant improvement over the 4-MIPS level indicated in the report, and was achieved using our new Fortran compiler and Multiply Accelerator.

Also, the report implied that the 4-MIPS performance level was achieved using "dual processing units." This is not true. The 5.6-MIPS performance was achieved by the Concept 32/8750 computer, a single processor. The Concept 8780, which features our unique CPU/IPC combination, is capable of performing 10 MIPS. This represents an 80-percent improvement over a single CPU configuration.

Another part of the report states that the 75-ns cycle time of 100-K ECL logic is a mature technology, it is still viable and will continue to be so for years to come.

Joe Barcheski
Gould Inc
SEL Computer Systems Div
6901 W Sunrise Blvd
Fort Lauderdale, FL 33310-9148

Speaking out for Forth

I am a user of Forth and as such would like to reply to John D. Stanley's letter about the flaws of the Forth language (Sept 1983). Certainly one cannot deny that Forth is slower than well-written assembly language code. As one who has written many thousands of lines of assembly code I would be the first to admit this. But, I don't agree that this represents a weakness of Forth.

The point is that Forth is not assembly language but a higher level language of admirable speed and compactness. Not only is it faster than many other higher level languages, but it also produces more compact code than assembly language for complex programs.

Forth can support user defined interrupt handling. Bryte-Forth is an implementation currently available for the Intel 8031 microcontroller that not only allows interrupt handlers defined in Forth or machine code but also supports runtime reassignment of handlers, systems time/date, fully buffered interrupt driven serial I/O, user defined error handling, and self-starting, ROM-resident user applications. What more could a real-time application programmer need?

On the subject of readability, I contend that "unreadable" programs can be (and are) written in any higher level language or assembly language. Readability is influenced most by the ability of the programmer and the experience of the reader. Well-written Forth is very readable because of the ability to build a problem-oriented vocabulary of mnemonic words or phrases.

Forth is a fine language. Those just learning should read a good book on the concepts and programming techniques of the Forth language.

Christopher K. Johnson
Bryte Computers, Inc
PO Box 46
Augusta, ME 04330
NS32032

The First True 32-Bit Microprocessor to Become Reality.
NS32032

The first commercially available microprocessor to feature:

1. Full 32-bit architecture
2. Full 32-bit internal implementation
3. Full 32-bit data bus to memory
The industry’s consensus: with the introduction of the NS32032, the NS16000™ microprocessor family has become the foundation for the next generation of high-performance, low-cost computers.

Any software developed for the 32-bit NS32032 will run just as well on the 16-bit NS16032 or the 8-bit NS08032, and vice-versa. And it will also run on future NS16000 32-bit CPUs. Consider this absolute downward-upward object code compatibility in contrast to the upward-only compatibility of other microprocessor families, which will make their 16-bit processors obsolete when they add 32-bit processors to their product line.

The NS16000 microprocessor family already includes peripherals compatible with its CPUs, and each is in full production: the NS16201 Timing Control Unit (TCU), the NS16202 Interrupt Control Unit (ICU), the NS16081 Floating Point Unit (FPU), and the NS16082 Memory Management Unit (MMU). Since the FPU and MMU interfaces are almost entirely invisible to NS16000 programs, the decision to include or omit floating point or memory management hardware (for cost/performance reasons) will not affect NS16000-based systems’ software compatibility.

The billions of bytes of existing mainframe software can now be easily ported to run on NS16000-based systems. The NS16000 family’s mainframe-in-silicon architecture (designed specifically to support high level language programming), its full high-speed floating point arithmetic capability, its integral support for Demand Paged Virtual Memory, and the NS32032’s 32-bit data bus to memory combine to make this possible for the first time.

Elegance, you see, is everything.

Think about it.
The only limits on NS16000-based applications are those of the imagination.

The full 32-bit architecture of the NS32032 (shared by all NS16000-family CPUs) sets no bounds to programmers' productivity or creativity.

No other processor family—micro, mini, or mainframe—has an architecture designed to fully support the use of high level languages, with a structure and behavior corresponding directly to the objects and operations of HLLs.

Its powerful features:
- A compactly encoded, completely symmetrical, two-address instruction set.
- Thirteen addressing modes (many not found in other microprocessors) designed for the kinds of accesses compilers generate.
- Indexing automatically scaled to argument size (1, 2, 4, or 8 bytes), applicable to any addressing mode.
- Instructions to implement high level language constructs such as case statements, loops, and calls, as well as bit-field and string manipulation.
- A fully integrated floating point instruction set, supported by hardware.

The 32-bit architecture of the NS32032 (like that of the other NS16000 CPUs) is fully implemented, without exception or restriction.

Simply stated, physical limitations in processing or packaging technology have not constrained internal implementation. All NS16000 CPUs have a full 32-bit Arithmetic Logic Unit (ALU), a full 32-bit register set, and a full 32-bit internal data bus to the input/output control block.

The value of such elegant implementation? An example: competitive microprocessors take eight to twenty internal steps to execute the expression evaluation "A = A * X + Ai," commonly used in high-performance technical and scientific applications.

The NS32032 takes four.

The NS32032's full 32-bit data bus to memory increases memory bus bandwidth—and thus the speed at which data can be transferred.

In simple systems (CPU and memory), the NS32032's ability to access a full 32 bits of external data dramatically increases the rate at which instructions and data are processed, while leaving bus time available for system peripherals.

Because it requires less than 50% of the available bus bandwidth in standard applications, the NS32032 is also ideally suited to complex multi-processor systems, DMA transfers, and high-speed graphics.

In the NS16000 family of CPUs, the primary feature that distinguishes one processor from another is the width of the data bus to memory.

The fact that the NS08032 and the NS16032, with their 8-bit and 16-bit data buses, share identical 32-bit architecture and 32-bit implementation with the NS32032 means that it is now possible to develop 8- and 16-bit systems with all the benefits of 32-bit software performance. The same software can now be implemented on all the systems within a product family, an enormous benefit to programmers and systems designers.

Future 32-bit CPUs planned for the NS16000 family will feature improved performance—bettering the NS32032's 1 MIPS tenfold by 1988—yet these future CPUs will also be compatible. This clear migration path guarantees the preservation of your initial software investment while providing for significant enhancement in your product line.

No other family of microprocessors shows such foresight or foresight.

TYPICAL EXECUTION TIMES (in µs at 10MHz)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Register-to-Register</th>
<th>Memory-to-Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mov Byte</td>
<td>0.3</td>
<td>1.7</td>
</tr>
<tr>
<td>Word</td>
<td>0.3</td>
<td>2.5</td>
</tr>
<tr>
<td>Dbl.word</td>
<td>0.3</td>
<td>4.2</td>
</tr>
<tr>
<td>Add Byte</td>
<td>0.4</td>
<td>2.0</td>
</tr>
<tr>
<td>Word</td>
<td>0.4</td>
<td>3.2</td>
</tr>
<tr>
<td>Dbl.word</td>
<td>0.4</td>
<td>4.7</td>
</tr>
<tr>
<td>Mul Byte</td>
<td>3.8</td>
<td>4.3</td>
</tr>
<tr>
<td>Word</td>
<td>5.4</td>
<td>7.0</td>
</tr>
<tr>
<td>Dbl.word</td>
<td>8.6</td>
<td>12.0</td>
</tr>
</tbody>
</table>

Additional reasons why the NS16000 family now leads in microprocessor design-wins:

1. Hardware development can begin immediately. All three CPUs are available right now. So are all the necessary peripherals in the family.
2. Software development can begin immediately. Appropriate evaluation tools, and both resident- and cross-support packages, are available now, as is an extensive list of third-party software.

Our SYS16™—a multi-user, multi-tasking development system—incorporates the complete family of NS16000 chips (CPU, TCU, ICU, FPU, and MMU), and therefore gives up to eight programmers a true, native environment to work in.

GENIX™, a product of our software engineering group, is the first microprocessor operating system capable of implementing Demand Paged Virtual Memory.

The NS16000 microprocessor family.
Adapted from the Berkeley 4.1 bsd version of UNIX, it has been elegantly tailored to optimize the NS16000 architecture. (We also offer source code under license for GENIX and its utilities.) Together, the SYS16 and GENIX demonstrate that the NS16000 microprocessor family makes the best "UNIX engine" on the market today.

For customers with VAX-11™ systems under UNIX, our GCS™ (GENIX Cross Software) contains the C compiler and other NS16000 tools from the SYS16. For VAX-11 systems running the VMS™ operating system, our NSX-16™ cross software provides full NS16000 family support.

To help complete your development cycle simply and quickly, all of our development tools provide support for our easy-to-work-with ISE/16™. An elegant development tool in its own right, the ISE/16 allows real-time evaluation of the NS16000 chips, for testing and debugging hardware and software in your own hardware environment, and requires no target-system modification.

3. Every resource imaginable to help you get your NS16000-based application to market first is available now. We are totally committed—with in-house hardware, software, and systems expertise; with service, documentation, and customer training. We are backing the NS16000 microprocessor family to a degree unparalleled in the history of the semiconductor industry.

But then, there has never been anything like the NS16000 microprocessor family before.

NS16000
Elegance is everything.

See it.
The NS16000 microprocessor family will be on exhibition at Uniforum and Electro.

Talk with us.
Please call the National Sales Representative nearest you for more information, and the answers to your questions.
Ask to meet with one of our Field Applications Engineers, too. Or, circle the number below.

Read about it.
For more information, please request a copy of NS16000: The Specifics of 32-Bit Architecture. And for practical experience, ask for a copy of NS16000 Training, detailed information on available courses.

NS16000: The Specifics of 32-Bit Architecture
NS16000 Training

VAX and VMS are trademarks of Digital Equipment Corporation. UNIX is a trademark of Bell Laboratories. NS16000, SYS16, GENIX, GCS, NSX/16, and ISE/16 are trademarks of National Semiconductor Corporation.
For tough image processing problems like pixel rotation, image reconstruction, or hidden line removal from wire frame models, Mini-MAP gets results in seconds, not hours. Attach a Mini-MAP to a PDP-11 or VAX UNIBUS and you have an interactive number cruncher that is ideal for image processing, CAD/CAM, solid modeling, medical imaging, and animation.

Shared memory simplifies programming and provides the unprecedented throughput necessary for truly interactive image processing of complex algorithms. 32-bit DEC floating point arithmetic, along with 7 MFLOPS of number crunching power, ensures that accurate results are available quickly.

A scientific subroutine library of over 225 FORTRAN callable routines including an expanding selection of image processing algorithms is available for Mini-MAP. For optimum performance, high-level FORTRAN control languages are provided for both the host and Mini-MAP.

Memory is expandable up to 16 MBytes. Configurations include a four-board set with DEC-type backplane or fully packaged systems.

System integrators are finding Mini-MAP is the most cost-effective number crunching solution for image manipulation. Write for information or call toll free 1 800 325-3110 for fast action.

- 32-bit floating point precision
- Compiler/Assembler/Linker/Debugger
- 225 FORTRAN callable arithmetic routines
- Up to 16 MBytes of memory
- 1024 x 1024 2-D real FFT in 8.8 seconds
- 1280 x 1024 4-color image rotation (Raster Scan Storage Format) in 27.5 seconds.

DEC, PDP-11, VAX, and UNIBUS are trademarks of Digital Equipment Corp. Mini-MAP is a trademark of CSPI

CSPI
THE ARRAY PROCESSORS
40 Linnell Circle, Billerica, Massachusetts 01821 • 617/272-6020 • TWX: 710-347-0176
CIRCLE 14
Thirty-two bit system designers face decision time

Computer system designers and system integrators producing leading edge equipment in the next five years will often opt for powerful 32-bit microprocessors, or 32-bit microprocessor-based boards and systems. They must hook these chips, boards, and boxes together with a 32-bit bus if they want to take full advantage of 32-bit machine functionality.

Designers can choose an open system bus, whose specifiers will cooperate with other firms to generate industry support in the form of interface, driver, and other chips needed to run a bus. Third-party firms will also produce single- and multi-board computers, software, memory, peripheral driver boards, and the like, for open buses.

Today, there are two major open bus choices—the Multibus II from Intel (Hillsboro, Ore) and the Versa Module Europa (VME) bus from the Motorola (Phoenix, Ariz), Signetics (Sunnyvale, Calif), Mostek (Carrollton, Tex) troika. In addition, there is the NuBus from Texas Instruments (Dallas, Tex), a 32-bit bus from Digital Equipment Corp (Maynard, Mass) and a 32-bit bus standard from the IEEE.

To help make an intelligent decision as to which bus to choose for a computer system's lifetime, designers should be cognizant of major and minor differences between the buses. It is equally important to be aware of how they evolved into their present form, and what they can be expected to offer from both the technical and marketing points of view. Finally, designers understand that a bus is really a local network in a small geographical area. As such, like any local network, it can be designed much like an implementation of the International Standards Organization (ISO) seven-layer model for computer communications—the Open Systems Interconnection (OSI) model.

Significantly, the Multibus II specification addresses not only the usual layers 1 and 2 of this model (the physical and data link layers), but also parts of the higher, software-based layers. In contrast, the VMEbus confines itself to implementing the first two layers in the bus with the higher layers taken care of by microprocessor operating system software. Of
Designers face decision time
(continued from page 27)

Fig 2 The five different buses designed by Intel to form Multibus II can be configured in various ways. They include a parallel system bus, a local memory bus, a serial bus for message passing, and two buses adapted from Multibus I. These I/O buses handle DMA and I/O expansion.

course, the different approaches have advantages and disadvantages.

Multibus II, (riding on the bustrails of the successful Multibus I for 8- and 16-bit processors), and the VMEbus are the main contenders for new 32-bit products. Their specifications have been published, and their backers and advocates are making a major marketing effort. Given the 8- and 16-bit history of these buses, industry support is likely to follow.

Both the Multibus II and the VMEbus have made their start toward implementation and the development of complementary products. VME has had a head start and has been specified as a 32-bit bus since 1981. For example, members of its backing troika have announced sample availability for certain bus chips. Vendors making VME-based, 32-bit boards have also been able to make prototypes for some time with 16-bit processors.

The Multibus II enjoys the support of Hewlett-Packard (Palo Alto, Calif) Siemens (West Germany) Tektronix (Beaverton, Ore) and Advanced Micro Devices (Sunnyvale, Calif) as well as a host of other companies. For its part, VME has been blessed by Philips Gloeilampenfabrieken in The Netherlands (Signetics' parent firm), France's Thompson-CSF, and its own list of major and minor companies.

The gut issue for computer system designers is not who approves what bus or the size of a supporting consortium. It is what they can do with the bus for the product they have in mind, and when. This designer point of view assumes that the competing buses are backed by reputable firms that will support them with a sufficiently varied line of products—clearly the case for both Multibus II and the VME.

Projections of market share, endorsements, and the like, while useful in showing designers that there is a sound economic base for the bus, are not primary concerns. Competing giants will divide the market in some way and no one will be stuck with an unsupported bus unless one of the contenders happens to fail badly.

In reality, both buses can be expected to find support from hundreds of vendors and designed into numerous products. This is already the case for the Multibus I, Intel's 8- and 16-bit bus. Not so popular in this regard—at least according to the third-party vendor catalogs issued by IronOak Corp (La Jolla, Calif), the VMEbus is rapidly gaining market share. This gain may accelerate as Motorola's 68000 microprocessor family, for which the VME is ideal, gets onstream.

The question of which processor designers choose in the first place (or are locked into by tradition or software) is a major one for both the Multibus II and VMEbuses. Designers who opt for the Motorola 68000 or Intel 80X86 family will probably not make a detailed investigation into bus specifications. Bus functionality at least for the next few years of microcomputer products, will remain about the same.

So, many designers will pick the bus associated with the manufacturer of the processor they have chosen and assume they best support each other.

Erstwhile computer system designers need a comparison of the basic specifications of the Multibus II and VMEbuses to determine whether one can be rejected out of hand (Fig 1). A detailed comparison of bus specifications determines more sophisticated rejection criteria. Any one of the specifications can eliminate a bus from further consideration—e.g., multiplexing or asynchronous behavior.

Some users find the plug-and-socket connector in the VMEbus (introduced in Nov 1981 as an 8-, 16-, or 32-bit data width bus) to be more reliable than the Multibus I's edge connector. In any case, Intel has come up with a Deutsche Institut für Normung (DIN) plug-and-socket connector for the Multibus II design (introduced at the Las Vegas Comdex show in Nov 1983), so connector reliability is not an issue.

Intel's Multibus II offering comprises five, "software configurable," connectable buses. The fastest bus is a 32-bit wide, synchronous communications, 10-MHz bandwidth system bus that links single-board computers, microprocessors, memory, I/O, and other components. The system bus can handle a theoretical maximum of 40 Mbytes/s in a burst mode.

The second new Multibus II offering is a local bus extension designed to hook local memory to a microprocessor. It runs at 12 MHz.
for up to 64 Mbytes of memory that must be accessed by a microprocessor without contention problems.

The third member of the bus quintet passes messages between software processes in a serial mode at 2 MHz. This bus member and the 32-bit parallel system bus have what Intel says is the "same interface for VLSI chips," thereby making them software compatible.

The last two Multibus II parts are a multichannel DMA bus for I/O and an I/O expansion bus that have been adopted from the Multibus I. Fig 2 illustrates how the five different buses function in a computer system.

Because of the large amount of software that has been written for the Multibus I devices, continuing software compatibility with the Multibus II is an Intel goal. For Multibus II project manager Frank J. Costa of Intel’s Hillsboro, Ore facility, such software compatibility "is a matter of writing new device drivers," a chore he does not think is too difficult—at least for Multibus I software porting to Multibus II. However, designers are pressed for time, and Black points out that it will take a year for Intel to have Multibus II products on the market. "In contrast," says Black, "VME customers can start work with VMEbus and Multibus II are rather small points. Neither bus stands out above the other."

According to Black, the products available for each bus are the primary considerations. Designers are pressed for time, and Black points out that it will take a year for Intel to have Multibus II products on the market. "In contrast," says Black, "VME customers can start work with 16-bit VME boards now, and the software will run on 32-bit versions since the 68000 family software is upward compatible."

As might be expected, Intel has a similar point of view for its microprocessors and buses. However, Black says that the upper ISO layer-like software, (eg, message space mapping), that Intel features on its Multibus II is not supported by the present Intel Multibus I hardware or user groups last Nov, the Motorola, Signetics, and Mostek troika announced additional buses for the VME architecture. These include a high speed memory expansion bus (the VMX bus), and a self-arbitrating high speed serial bus that can be used in the existing VME bus, as seen in Fig 3.

As mentioned, Motorola’s buses use ISO layers 1 and 2 only. For Motorola, system software functions that correspond to higher ISO software layers are best handled in software that rides on the microprocessor operating system, not in the bus specification. Once the software is well defined, it will be implemented in hardware. In any case, system software considerations are being worked on by both Intel and Motorola.

The details of the VME and Multibus II bus designs in Fig 1 and the bus specifications are best understood by specialists. For Motorola’s John A. Black, Jr, manager of systems and technology at the firm’s Tempe, Ariz operation, this means that bus-pickers will have chosen a bus from the company that makes the processor they prefer. "Moreover," he adds, "most bus details concerning ISO layers 1 and 2 that are talked about to help make a distinction between VME and Multibus II are rather small points. Neither bus stands out above the other."

According to Black, the products available for each bus are the primary considerations. Designers are pressed for time, and Black points out that it will take a year for Intel to have Multibus II products on the market. "In contrast," says Black, "VME customers can start work with 16-bit VME boards now, and the software will run on 32-bit versions since the 68000 family software is upward compatible."

As might be expected, Intel has a similar point of view for its microprocessors and buses. However, Black says that the upper ISO layer-like software, (eg, message space mapping), that Intel features on its Multibus II is not supported by the present Intel Multibus I hardware or

---

**Fig 3** In its latest version, Motorola’s VMEbus is no longer a single, multifunction parallel bus that is configured to do all system chores. It has two partners: the VMSbus handles serial chores like message passing; and the VMXbus connects CPUs to local memory or other devices.
Designing with Tektronix Microprocessor Development systems are in color.

Color makes Tektronix design tools the industry's easiest to use. With our Colorkey+ user interface, you spot errors faster and work more efficiently.

Why the competition is green with envy.

Because, not only were we the first to bring color to microprocessor development, but we also have unmatched chip support... including emulation for the Z80, 8085, NSC800, 80186, 68008, 68010 and 30 more.

And our wide selection of design tools lets you fit the solution to your environment, whether you need our own proven system for one to eight users, or our...
microprocessors? the way you look at us.

software to turn your VAX™ into a powerful development system. **We speak your language.** Pascal and C, of course. But we also understand your application. And we can configure a system to help you take your design from start to finish.

Call your Tektronix Sales Engineer and ask about the innovations we've made in microprocessor development.

Look at Us Now!

Call 1-800-547-1512

VAX is a registered trademark of Digital Equipment Corp.

Circle 173 for Literature
Circle 174 for Sales Contact
Designers face decision time  
(continued from page 29)

What's Nu?

Although the 32-bit, 10-MHz synchronous NuBus is not being promoted by TI with the same intensity as the VME and Multibus II buses, it has nevertheless been proposed by TI to the IEEE 896 committee for consideration as the basis for a 32-bit synchronous bus standard. It is also being used in a TI-developed technical workstation introduced in Jan 1984.

According to George P. White, who is both the 896.2's coordinator, synchronous version task group, and TI's Nu Machine development manager, NuBus was originally developed by MIT for workstation research in artificial intelligence, networking, and office automation. Western Digital licensed it from MIT and TI took over the license from Western.

NuBus is designed to be as processor-independent as possible, White says, since MIT, Western, and TI have no specific processor interest. For example, the artificial intelligence workstation known as the Lisp Machine from LISP Machines, Inc (Culver City, Calif) has a four-board, bit-sliced, microcoded MSI processor that operates on a NuBus.

While TI would "like to see industry standard boards based on the NuBus", and it has converters, (eg, to hook up NuBus cards to Multibus I cards), it has "not yet decided to what extent it will try" to accomplish this goal. Current TI activities include, for example, rewriting of the NuBus specification to make it more user-friendly. In addition, TI designers are looking into certain system aspects of the bus and how they could be hardware- or software-implemented.

"NuBus is designed to implement layers 1 and 2 of the ISO model," White reports, noting that this helps in keeping it processor-independent since "the more ISO levels 3 through 7 (or parts of them) are implemented in bus specifications, the more the bus is tied to system architecture and the more processor dependent it is."

For its part, Motorola, points out that part of the VME specifications can be found in Multibus II.

Clearly, both buses will be well supported as their backers fight hard for the dominant share of what they perceive is a large market for 32-bit microcomputers. In fact, Hughes notes that pragmatic engineers, confused over which bus to use for their new designs, could probably choose either and do well.

"But, that's today," he adds. "The real question is which bus will be around a few years from now and which will be supported by a wide variety of sources."

For Hunter, the distinction between buses is more a question of which microprocessor family computer designers are going to use. Supporters of both buses claim that different microprocessors can be accommodated. However, Hunter says there is no question that the VMEbus is designed to work best with Motorola's 68000 family and the Multibus II with Intel's 80X86 designs.

And there, Hunter claims, is an important difference for designers.

Other engineers and marketers at the firms involved said that both buses could accommodate all common processors but it was a matter of how many glue chips would be needed, what software modifications would have to be made, and whether any throughput problems would arise. All agree that the issues are complex and best addressed on a case-by-case basis.

VME partisans feel that an asynchronous bus is better suited for a variety of processors since it is not locked to a fixed clock frequency.

Other observers feel that Intel's Multibus II, because it includes some upper-ISO level software, fixes certain system design details, thereby making it more processor-dependent. Such dependency would be for the 80X86 family, which can be expected to be the first to implement the ISO-based software.

Asynchronous or synchronous?

Although the synchronous Multibus II bus makes provision for different device speeds by interfacing and translating them to its 10 MHz, there are more timing constraints than with an asynchronous bus. However, Intel's John Beaston, product marketing manager, points out that bus interface chips can accommodate a variety of speeds with no trouble. Furthermore, they can do this at little incremental cost in their VLSI versions, which will perform many other chores. He says there are also speed translator chips all over the VMEbus even though it is asynchronous.

(continued on page 34)
Designing with the 68000, 68008 or 68010? Call us.
Tektronix Microprocessor Development Systems support you from your first line of code clear to your last line of debug, in Assembly, C or Pascal. Our systems match your environment, too—from one to eight users. And we can even harness the power of your VAX™ computer and turn it into a powerful microprocessor development system.
If you’re working with the 68000, 68008 or 68010, call your Tektronix Sales Engineer. And find out why Tek is leading the pack in microprocessor development.

Tektronix Microprocessor Development Systems.

Look at Us Now!
Call 1-800-547-1512

™ VAX is a registered trademark of Digital Equipment Corporation, Inc.

Circle 175 for Literature
Circle 176 for Sales Contact
Designers face decision time
(continued from page 32)

A matter of diplomacy

In what might be called bus diplomacy, Paul Borrill, Research Fellow at University College in London, England is chairing the IEEE's P896 committee. The committee is charged with setting a standard for an asynchronous, 32-bit bus known as the Futurebus. Borrill's committee works closely with P896.2, an IEEE P896 group handling a synchronous, 32-bit bus standard (headed by another bus diplomat, Task Group Coordinator George White at TI's digital systems operation in Irvine, Calif).

According to Borrill, the work of the 896 committee is complete as far as the asynchronous bus is concerned and its documents are out for public comment after some five years of work. "Several companies are prototyping to this specification even though they have their own bus," Borrill notes, mentioning Tektronix. In contrast, much remains to be done on 896.2, which only recently started its work.

Intel will introduce its Multibus II specification for consideration as the 896.2 standard (or as an 896.2 implementation) at the Feb 1984 Compcon meeting in San Francisco. TI's 32-bit NuBus (out of Western Digital and MIT and already presented to P896), belongs in 896.2's domain, as does Digital Equipment Corp's new 32-bit bus. "Multibus II is being proposed as a basis for 896.2," Borrill says, adding that the IEEE bus committee goal is to reduce the number of buses available, not increase them.

As far as the asynchronous VMEbus is concerned [it conforms to IEEE specification in P1014], Borrill says it has a simplier bus interface implementation and a simpler system implementation for single and multiple processors and is very well optimized for its applications. The VMEbus follows the traditions of the Multibus I, the Motorola Exorcsor bus in that it is asynchronous and non-multiplexed, and the STD bus, Borrill says, adding that it provides more features and a higher performance than both of them. "Its performance is even better now that it has secondary buses on which to put communication overhead traffic. This will be of great help in a multiprocessor environment where all buses have bandwidth problems."

Borrill's reflections on various IEEE committee efforts to standardize buses shed interesting light on some VME versus Multibus II controversy. The 896 committee consensus was that the most processor-independent bus was asynchronous. On the other hand, the question of whether asynchronous or synchronous buses are better for high performance takes on "the tone of a religious argument with passionate believers on both sides." As far as the original intent of the committee is concerned, Borrill says that the intended application of Futurebus is high end, fault-tolerant systems, while 896.2's application is medium-range, 32-bit markets.

Yet to come from the 896 committee are specifications (for both synchronous and asynchronous buses) that define how to take care of software chores in the next layer of the 896 architecture. These include specification of identical address mapping on both buses, specification of identical error control methods, and specification of the same method of accessing the bus with a higher level protocol, such as a message passing protocol. These specifications will move software transparently between any asynchronous or synchronous bus without changing a line of code.

Bus specification accomplished so far for the 896 committee is equivalent to the physical and data-link layers (layers 1 and 2) of the ISO seven-layer model for computer communications. DIN connectors and Eurocard boards are equivalent to layer 1 and the bus communication protocol is equivalent to layer 2. Now the committee would like to consider implementing higher level communication-oriented protocols that can be built into the bus interface. For its part, Intel, with its message passing and error detection schemes in the Multibus II specification, has already taken a step toward implementing some higher level ISO functionality in the bus itself.

The 68000 and 80X86 families are said to work with either an asynchronous or synchronous design. Asynchronous is more flexible, Hunter says, adding that the 80X86 family functions best with a synchronous bus. Intel's Hughes and Beaston disagree, each noting that Intel's processors work well with the asynchronous Multibus I and are being designed onto VMEbuses by third-party vendors.

While the asynchronous versus synchronous question rages, there are more mundane considerations in bus design. For example, Intel's opting for a longer Eurocard (220 mm instead of the VMEbus 160 mm) for its board may be a short-term advantage but a long-term disadvantage. Today's designers may need the room but, as chip integration technology improves, and more functions are crammed onchip, less board space may be needed. On the other hand, it may be that additional space will be needed both today and tomorrow as more functions are put on a board. Indeed, TI's NuBus board is 60 mm longer than Intel's—the next step in the Eurocard standard.

More to the story

There is more to bus design than how to take care of ISO levels 1 and 2 (or higher). Rick Main, the VMEbus manufacturer's group secretary, manager of microsystems engineering at Signetics, and designer of both Intel- and Motorola-chip-based computer boards and systems has found that the practical hardware and software problems of

(continued on page 36)
Designing with a 1750A processor? Call us.
For development support for your 1750A compliant processor, you need Tektronix. No matter what your implementation—chip, bit slice, or single-board processor—Tektronix lets you develop software and hardware that fit together. And you can integrate the software right on the target processor, so you can test it where it lives.

Using another microprocessor? Take a look at Tek. We support over 30 chips, including both 8-bit and 16-bit processors. And we have systems that fit your design environment, from our proven hardware for one to eight users, to our software that turns your VAX™ into a powerful development system.

Call your Tektronix engineer and find out why Tek’s support stands alone.

Tektronix Microprocessor Development Systems.

Call 1-800-547-1512

™ VAX is a registered trademark of Digital Equipment Corporation.
Designers face decision time
(continued from page 34)

In the wings

While the VME and Multibus II buses are the major contenders right now for 32-bit bus honors, they are not without competitors in the long run. Digital Equipment Corp is working on a 32-bit bus design that will hook up machines based on its PDP/11-70 minicomputers into a distributed, realtime multiprocessor network. Philips and Intel have such designs in prototype form but DEC has wired systems together and is working feverishly on developing software to make them run with all the DEC applications.

Called variously the bi-bus (for bus interface bus), the enhanced Q-bus, and the Q-32 bus, DEC's bus will help DEC minicomputers compete with the microcomputer and supermicrocomputers whose functionality has been migrating up into the traditional minicomputer area. In short, DEC, pressured by the increasing power of micros, has increased mini capability, but it will soon directly counterattack the micro world with its 32-bit bus mini-based system.

The new bus will not hurt the sales of DEC's computer boards, which have made a strong industry mark. Moreover, if DEC opts for an open bus with all its specifications made public, it may well compete with Intel and Motorola for third-party vendor support—as may TI if it decides to push its NuBus.

The choice between the VME and Multibus II will be easier as both Motorola and Intel further define the system functions mentioned and how they are implemented. On the other hand, DEC could complicate matters with its impending 32-bit bus if it is indeed different. According to IEEE's Borriull, DEC's bus is "far more radical in design concept than the Multibus II."

making real, bus-based computer systems have general applicability. According to Main, both the VME and Multibus II user groups and the written bus specifications deal with these practical issues.

First, there is the problem of the internal design and operating environment of the boards that vendors furnish for bus connections. Some design and environmental standards would be useful. Main also notes that power distribution, electrical noise, and thermal problems must also be solved in practical computer systems. It would be helpful if the bus specification provided guidance. This is especially true now that standard buses and standard boards mean there are more nonexpert computer system designers.

Then, there is the software problem. With readily available industry-standard languages, operating systems, compilers, and the like for realtime, multitasking, and multiuser applications, designing one's own software is unnecessary except for highly specialized applications. The real problem is integrating software with hardware—especially when both are developed by different vendors who are not in contact with each other.

According to Main, some of these software/hardware integration problems can be addressed by appropriate system specifications. For example, if a bus has standard I/O driver interfaces, board vendors can supply software drivers with their boards and users can integrate these drivers into their operating systems. This allows modular replacement or reconfiguration of systems but without the operating system impact.

Bus manufacturers and bus standards can bring about software standards for coprocessor chips for floating point algorithms. And, as operating systems are standardized, standards will follow for assembly language commands to create software tasks, wake-up tasks, send messages, and more. Once standardized, these algorithms can be implemented in faster hardware that plays well with a particular bus design. Both Motorola and Intel promise VLSI to help reach these goals.

Software must also work with hardware to perform such chores as power-fail recovery and automatic operating system configuration to fit the hardware on which it is running. Main says these are ambitious chores for any bus but at the very least, "guidelines can be established if not full-fledged specifications for getting the job done." Some of this material is under review by both Motorola and Intel, and Intel has gone so far as to specify (in Multibus II) ways to accomplish several of the important tasks.

A look at system issues

System issues separate the Multibus II from the VMEbus since the VMEbus (combined with the VMX and VMS buses) functions in a way similar to Multibus II—at least for the next few years. In fact, both Motorola and Intel feel that 32-bit data paths are just part of the increased functionality needed by 32-bit systems, and system attributes like ease of use, reliability, and multiprocessing capability are equally important.

As far as ease of use is concerned, Intel's Beaston says that the Multibus II specification makes it software configurable compared to the hardware-configurable VMEbus. He notes that many of the jumpers and spikes on a Multibus II board are eliminated, since starting addresses, interrupt vectors from memory, and the like are more readily handled by Multibus II.

Motorola's Black disagrees, pointing out that auto-configuration or automatic system generation are but one part of the different bus design philosophies of Intel and Motorola. Motorola is working on a system specification to be released in mid-1984. The document will address system software modularization and its hardware module implementation, including such factors as automatic configuration.

This specification will respect the separation and independence of the upper-ISO layers. Unlike the Intel approach, it will not specify how parts of the layers should be implemented by the bus specification. According to Black, Motorola believes that system software implementation is
Turn your VAX™ computer into a powerful microprocessor development system.

Tektronix software. The same powerful tools that set the standard for high-level programming on Tek's 8500 series of microprocessor development systems are now available for use on your VAX. Get the sophistication of Pascal and C Language Development Systems (LANDS). Plus real-time emulation and debug when you integrate Tek's 8540 emulation unit to your system. Add 4105 Color Graphics terminals to access Colorkey+, Tek's single-key interactive user interface. All fully integrated with VAX-specific communications software.

Support from the first line of source code to the last line of debug.

Call your Tektronix sales engineer. With your VAX, we'll help you create a system that suits your engineering environment, and show you how Tek and your VAX have met the challenge of microprocessor software design.

Tektronix Microprocessor Development Systems.

Call 1-800-547-1512

***VAX is a registered trademark of Digital Equipment Corporation.**
Designers face decision time (continued from page 36)

best done by system designers to suit their own needs. This means using the operating system, not the bus, as a foundation.

"Software configuration is flexible but costly in board real estate and board performance," Black says. "Moreover," he adds, "it's hard to do halfway with some done by the operating system and some by hand. It also needs operating system intelligence resources and memory; our experience shows it's not something customers are inclined to pay for."

Beaston also claims that remote diagnostics are more readily handled by Multibus II. For example, having the interconnect address space in the bus specification to allow designers to identify boards by their physical position in the backplane facilitates implementation of the diagnostics facility. Motorola's view is that such a use is best built on top of the designer option (today in software, tomorrow in hardware) and not into the bus specification with a predefined method and addresses.

As far as comparative bus reliability is concerned, there is the matter of error detection. Multibus II has a nonoptional feature that allows parity checks for error detection on data transfers so that a processor has an indication that something is amiss, and can abort or retry if necessary. Multibus II is also designed to allow the detection of operational errors. For example, a request for a 32-bit read on an 8-bit I/O line will cause an error indication, which will cause several other operational errors. These chores are taken care of by the Multibus II protocol.

There are several other reliability considerations. For one, Multibus II data samples are said to be taken to so that they have less noise sensitivity than VME samples. Beaston claims that the connector pinout is better designed than that of the VME since the different signal groups are shielded from one another. In addition, there are more ground lines for better noise performance as well as more power pins. Finally, there is less crosstalk since the pins are multiplexed and fewer lines are switched at once.

Black has a different point of view regarding relative bus reliability. He again points out that Intel is forcing a procedure on computer designers by insisting they use parity checks and pay the board space and speed penalty. Parity found on VME memory boards is a valid concept for memory but is not valid for bus drivers. Unlike RAMs, they are not likely to break down before the system mean time before failure (MTBF) calls for a system breakdown.

The VME approach to error diagnosis is to handle it in the microcomputer operating system where the operating system software handles all possible system errors and communicates with the system hardware to take care of them. In contrast, Multibus II handles some errors in its bus specification and would have to handle others in the operating system. In Black's view, this is an improper partitioning of operating system functions.

For Black, Beaston's comments about Multibus II's superiority in noise behavior, crosstalk, and pinout are not relevant, given today's advanced backplane technologies and multilayer boards. "There are no edge-sensitive noise, high frequency grounding, or shielding problems with the VMEbus," he says.

Lots of processors

Perhaps most important from the point of view of future designs for a multiprocessing environment, Beaston says that Intel's Multibus II is better designed for many processors than the VMEbus.

Normally, when a multiprocessor computer system shares memory, its processors must work with overlapping memory space. If there are more than two processors, there are likely to be address aliasing problems for the multiprocessor's operating system to manage. The microprocessor has contention and pointer manipulation chores to handle and can do nothing else when it is so occupied. The Multibus II philosophy is to take care of part of the support for multiprocessor data sharing in the bus interface hardware. For example, an 8-bit 8088 can

(continued on page 40)
The Alps Advantage in switches:

1,000,000,000 switches is more than just a whole lot of switches! It's a record of customer acceptance that has made us the world's leading manufacturer of electro-mechanical switches. We've been making them since 1948, with a very special kind of skill and commitment, dedicated to producing the most innovative, highest quality switches possible. In addition to making a far greater number of switches than any other company, we also make more types of switches, divided into 8 basic categories: push, slide, lever, rotary, power, flex, communication and digital switches...a staggering product line that includes thousands of different styles, models and variations.

Series SGK digital DIP switches. Very small DIP switches, with some very big Alps Advantages: exclusive twin-split contact design with super-smooth wiping action; 2-position circuit with a choice of 2, 3, 4, 5, 6, 7, 8 or 10-poles; ultrasonic sealing to eliminate flux penetration and silver migration problems; removable tape seal or protective cover to allow washing; ultra-low-profile, only 4.9 mm height; all in the perfect package for automatic insertion machines!

Total application versatility. If your application needs a switch, you can count on the Alps Advantage to meet your need — just write or call today.

One-billion switches per year, including 24 new models of ultra-low-profile DIP switches designed for automatic insertion.

ALPS ELECTRIC (USA), INC.
100 N. Centre Ave., Rockville Centre, NY 11570
Phone 516-766-3436 • TWX 510-221-6747

CIRCLE 19
Designers face decision time (continued from page 38)

control message passing in a 32-bit wide burst transfer interface.

Such a procedure is not possible with the VMEbus, which does not have a mechanism in its specification to do it, Beaston says. He adds that the VMEbus would require a separate address space in the bus specification to take care of message passing in the bus interface hardware and it cannot be added.

The VME manages data sharing by means of pointer passing on its VMS serial bus. According to Beaston, this is inferior to the Multibus II's approach because its 32-bit parallel bus would pass a 32-bit pointer in one clock cycle (32 times faster than the serial bus) even if their speeds were the same—and the parallel bus is much faster.

For Motorola's Black, the VME has unsurpassed multiprocessing capabilities. "All multiprocessing systems need, and will do, message passing, and the VMEbus has a memory map for messages," he says, adding that the real question is where in the system you define the mapping. According to the VME system plan, the VMEbus will pass messages over either its serial or parallel buses under control of the microprocessor, not the bus.

The VMEbus's realtime executive in its operating system takes care of all message passing with what is known as “address modifier codes.” In contrast, Intel has divided message passing so it is partially handled by the bus specification and partially by operating system software. All Multibus II has done so far, Black maintains, is define a message space—a separate page of memory—and specify some registers without saying what goes in them.

According to Black there are no inherent limitations to the multiprocessing capability of the VMEbus which might make it inferior in any way to the Multibus II. He goes on to say that the number of processors that can be handled is a function of the application, and such factors as bus arbitration efficiency.

The two bus arbitration schemes are basically equivalent, Black says.

As both buses have the same number of backplane slots, both arbitration schemes will accept a processor board in each slot, and bus arbitration (even though the VMEbus is marginally faster) is not a major factor since both buses arbitrate concurrently with bus activity.

The only remaining factor is how fast designers can move data through the bus and, as Black puts it, both are subject to the same laws of physics. For real world block transfers using real memory and other components designers can buy, not theorize about, the buses have equivalent throughput for block transfers, Black says. He adds that the VMEbus can do twice the transfers of a Multibus II for a single-cycle access because it is not multiplexed.

—Harvey J. Hindin, Special Features Editor
“When SSI/MSI isn’t enough, and gate arrays are too much, the logical choice is a short circuit.”

— Napoleone Cavlan
Director of New Product Development,
Bipolar Memory Division
"Signetics short circuits. Simple logic says it’s time to take a shortcut."

Take the shortcut! More than 60 SSI/MSI devices have been replaced by six Signetics short circuits. Even with a smaller board, there’s still plenty of room for other part types.

We know all about the expanse of SSI/MSI. And the expense of gate arrays. Because we sell plenty of both.

But we also bridge the gap between them with IFL (Integrated Fuse Logic), otherwise known as short circuits. That means you can have customized logic. Without the custom prices or lead times.

IFL takes user-programmable logic far beyond programmable read only memory and programmable array logic circuits. It provides a high level of integration. Flexibility. And ease of use. All this adds up to dramatically lower parts count. Improved reliability. Lower inventory costs. And shorter design cycles. Just for starters.

Programming is quick and easy, too. IFL devices are made up of logic elements joined by a selectable interconnect system. All connections and macro functions are completely programmable.

If you can write a Boolean equation, you’re home free. Just define your system in terms of the equation and enter it at a CRT terminal for downloading to your PROM programmer. Blow the fuses, and your logic circuit is ready. As simply and quickly as that.

"They blow everything else right out of the water."

No matter what other devices you stack up against our IFL circuits, there’s no contest.

Compared to TTL, they can cut your PC board size and pin count often by as much as 90%, and make the system more reliable in the process.

Compared to gate arrays, IFL circuits give you shorter development cycles, since it takes about 30 seconds to program one of our parts versus 6 to 8 weeks to make a gate array mask. They also give you lower initial cost, less design risk, and off-the-shelf availability.

Our IFL circuits can even give you programmable output levels. The most useable P-terms per output. The most inputs and outputs. And the most straightforward programming of any logic device in the industry. Complete with programmable AND and programmable OR arrays in the same device.

These circuits are among the most complex LSI products made today. But they’re manufactured on the same bipolar fab line which recently demonstrated 54 ppm mechanical and 0 ppm electrical AOQ (Average Outgoing Quality) — an industry low.

We’re applying this knowhow to our IFL. So you can be sure of the same high quality standards.

"You won’t believe all the things they can do."

They’re so flexible, you can get everything you need from just three basic IFL circuits: our simple Field Programmable Gate Array (FPGA), Field Programmable Logic Array (FPLA) and Field Programmable Logic Sequencer (FPLS). All of which come in 20, 24, and 28-pin packages.

By stocking that basic inventory alone, you can program your own devices to perform an amazing variety of functions.

With just the 82S151 FPGA, for instance, you can get memory mapping, fault monitoring, address decoding for peripheral selection, and random gating functions.

You can use our 82S153 FPLA in CRT display systems, code conversion, microprogramming, character generation, data secu-
rity encoding, frequency synthesis, interfacing, and random logic replacement.

And then there's our 82S159 Field Programmable Logic Sequencer, the newest member of our FPLS family. It can replace more than two dozen small and medium-scale TTL logic circuits, and also directly replace the 16R8 circuit.

Its exceptionally broad flexibility makes this FPLS ideal for a wider-than-ever range of functions. Including synchronous up/down counters, shift registers, random sequential logic, bidirectional data buffers, priority encoders/registers and bus arbiters.

"We'll help you take the best possible shortcut." We've developed a number of comprehensive aids that explain the advantages of short circuits. Including descriptive product application notes. A complete new Data Manual. Software brochure. And even a colorful wall chart with individual product summaries and analyses of the various approaches to user-programmable logic.

We give you all kinds of one-to-one help, too. From IFL seminars to programming support from our distributors, and direct support from our Field Application Engineers nationwide.

So no matter what you need, we're ready to help. But however you decide to get into short circuits, we think you should do it soon. Because IFL is such a logical choice that it's bound to give someone a big jump on their competition. And that someone might as well be you.

I'd like a short course on short circuits. Send me more facts.

Name: __________________________
Title: __________________________
Company: ________________________
Division: ________________________
Address: _________________________
City: _____________________________
State/Zip: ________________________
Phone: ___________________________

Mail to:
Signetics Corporation, MS 2527,
811 E. Arques, P.O. Box 3409,
Sunnyvale, CA 94088-3409
What is Z...ing? Z...ing is a philosophy that we at ZAX maintain about technology and its application. We realize that our customers need more than just the best technology... they need our concern of how that technology will be utilized now as well as in the future. That’s why our emulators more than meet today’s needs for development and will remain the state-of-art for your future requirements.

**ZAX EMULATORS + YOUR COMPUTER = A COMPLETE MICROPROCESSOR DEVELOPMENT SYSTEM**

From IBM’s PC to Digital’s VAX, ZAX now gives you the ability to form a complete development system using your computer... the ZAX In-circuit Emulator and interface software package makes this possible.

For the IBM PC, three special software packages utilize: the standard MSDOS™ operating system, Digital Research Programmers Utilities with Symbolic Debugging, or an Intel compatible Assembler/Linker Loader with Symbolic Debugging. ZAX also has standard packages for CP/M 86™ with Symbolic Debugging.

ZAX has an answer for mainframe computers with simple uploading and downloading of object files.

Development system owners benefit by downloading programs to ZAX Emulators... this cost efficient feature frees your system for further software development. This enables you to use ZAX Emulators for software debugging and system integration, permitting total control over your future development needs.

If Zmaximum flexibility at a minimum investment makes sense for your future, hook-up with the company that can give you more Z...ing...ZAX!

For further information please contact ZAX.
The World's Most Elegant Microprocessor Family Has its Own UNIX™ Operating System.

Introducing GENIX, the best operating system for the NS16000™ microprocessor family, from the company that knows the chip best.

Impressive mainframe architecture and sophisticated high level language support characterize the NS16000 microprocessor family.

Software development tools function very effectively in this advanced environment.

The custom match of GENIX with the NS16000 architecture is an obvious benefit. Besides providing all the proven benefits of the Berkeley 4.1 bsd version of UNIX—such as multiprogramming, a hierarchical file structure, and over 200 powerful utilities—GENIX adds value. GENIX supports true Demand Paged Virtual Memory and floating point operation. High level languages are also supported by an optimized C compiler and an optional, powerful Pascal compiler.

Of course, support for the full range of NS16000 advanced components is provided: CPUs, Memory Management Unit, Floating Point Unit, Interrupt Control Unit, and Timing Control Unit. These components, combined with GENIX, provide an unbeatable integrated microcomputer solution. GENIX runs on the SYS16 Development System and is also available now in source code, under license, for NS16000-based systems.

Expect more from the future.

The long-term success of a system depends upon its ability to expand. The clear migration path of fully implemented 32-bit architecture throughout the NS16000 microprocessor family means innovation never equals obsolescence. The NS16000 family brings the benefits of 32-bit architecture to 8, 16 and 32-bit systems to protect and optimize your system and software investments. Future 32-bit CPUs will also be compatible.

And there's more. Our UNIX expertise is already being applied to the implementation of Berkeley 4.2 for added technical and networking capabilities. The generic port of UNIX System V is also underway.

NS16000
Elegance is everything.

See it.

See the NS16000 family, featuring GENIX on the SYS16 on exhibition at Electro, or call your local Field Applications Engineer for a demonstration.

Talk with us.

Call the National Sales Engineer near you for more information and the answers to your questions. Ask to meet with one of our Field Applications Engineers to discuss your specific application.

Read about it.

For more complete details request the GENIX Summary.

CIRCLE 23

NS16000 and GENIX are trademarks of National Semiconductor Corporation. UNIX is a trademark of AT&T Bell Laboratories.

National Semiconductor
MICROCOMPUTER SYSTEMS DIVISION
Try to imagine a real-time operating system flexible enough to handle hundreds of different applications.
Without any modification.
Our VRTX* microprocessor operating system can do just that. Over 200 diverse applications, from navigating aircraft to controlling disks, to playing video games, have been successfully implemented around VRTX. All without tweaking a single bit of VRTX code.
A good thing, too.
Because our VRTX operating system is delivered in 4K bytes of ROM. Which naturally makes tweaking a little impractical.
But it does make VRTX the most bug-free operating system you'll ever use. And the easiest one you'll ever install.
In fact, we wouldn't be surprised if you saved six to 12 months of development time using VRTX.

But protecting our 100,000 hours of debugging and testing really led us to seal VRTX in silicon. And prevent even accidental modifications from introducing new bugs. So now we know, no matter how successful we get, we'll never get spoiled.

For a free VRTX evaluation package (including timings for system calls and interrupts) contact us with the details of your application, including the microprocessors you're using: Z8000, Z80, MC68000 or 8086 family. Write Hunter & Ready, Inc., 445 Sherman Avenue, Palo Alto, California 94306. Or call (415) 326-2950.

HUNTER & READY
Operating systems in silicon.
© 1983 Hunter & Ready, Inc.
Local area networks proliferate while standards lag

Since VLSI devices and interfaces to support them have appeared, local area networks (LANs) have been multiplying like rabbits. The advantages of connecting relatively cheap workstations to expensive file servers and graphics peripherals are obvious, as is the need to connect to mainframes with superior computing power and database structures.

The problem, however, is that individual hardware and software vendors have gone haring off in separate directions. Each provides relatively easy interconnection between users of their particular products, but no simple way of transferring data or programs to other systems.

The resulting incompatibilities, like the chaos of floppy disk formats, are a disservice to the industry and the consumer. The real and pressing need, at all levels of the computer industry, is for a free flow of data and information among all levels of machines and users.

Purely commercial concerns—locking users into a particular hardware/software combination—will prove counterproductive in the long run. Telecommunication managers are already beginning to see that a 10-Mbyte/s Ethernet link, with expensive cables, interface hardware, and installation, is not much good if the machines at either end of the link cannot understand one another.

Creating a local network interface is a fairly straightforward technical problem that can usually be solved relatively quick. Standards, on the other hand, are a political problem involving a large number of people and the reconciliation of conflicting points of view. Technology, as usual, is outrunning the political process.

Considering implementations

DR Soft/Net, from Digital Research, Inc (Pacific Grove, Calif), implements the session and transport layers of the International Standards Organization (ISO) interconnect standard. It is basically a distributed file-serving mechanism that allows various machines running Digital Research operating systems to share data files and use remote peripherals.

Its strength is in its modularity. Each function is a self-contained routine that other functions access via strictly defined interfaces. Data and service requests are passed between modules in a standard and easily understood way. Thus, details (continued on page 50)
are effectively hidden and design effort can be concentrated on the job at hand.

Implementation of this modularity (which has received much academic attention over the last 20 years) is Digital Research’s technical contribution to the computer field. By putting all hardware interfaces into one module, basic I/O system (BIOS), file handling in another, basic disk operating system (BDOS), and a simplified user interface, console command processor (CCP) in another, Digital Research has created a flexible operating system. This system has made writing relatively inexpensive application programs feasible and quick.

Soft/Net continues the tradition of modularity, and was designed to make it easy for manufacturers to configure for particular hardware. The strictly logical component, network disk operating system (NDS) is provided in both 8-bit (8080/280) and 16-bit (8086) versions. Hardware connections network I/O system (NDS) are presently available for Ethernet and Arcnet, with documentation available for adapting to other transmission media.

File sharing, password protection, record and file locking, and remote peripheral use are all supported by Soft/Net. The first release of Soft/Net will be as part of Concurrent CP/M-86 next month. This package will allow remote operations to go on in the background, while other programs are running.

However, the weakness of modularity is that the user is dependent on the functions that the vendor has chosen to include. CP/M has been criticized for allowing only four I/O devices apart from the disks—a Teletype (CON:), tape reader (RDR:), a punch (PUN:), and a line printer (LPT:). Each of these four logical devices can be dynamically connected to any one of 12 device drivers, but the choices are not many. Nonstandard peripherals must often be driven directly from the application program, defeating the concept of modularity.

In providing the NDS for Soft/Net, and the Graphic I/O System (GOS) for the recently introduced graphics system, the company has begun to address this weakness. Given the company’s announcement that development work is now being done in the C language, further modular extensions of the basic operating system can be expected. High level source code will also make possible, for better or worse, porting to new processors. CP/M-68K (for Motorola’s 68000) is already available, and rumors about an implementation for the 16032/32032 are circulating.

A technical problem with the CP/M file structure is that it is flat, consisting of a single list of files with 8-character names and 3-character
extensions. Hierarchical files (eg, PC-DOS 2.0 and Unix) can probably be expected in the future, especially since Digital Research has been chosen to complete the Unix implementation for Intel’s 286 processor. With the simultaneous increase in capacity and decline in price of mass storage (eg, 100 Mbytes on a 5¼-in. Winchester) the hierarchical file structure, in one form or another, should become the standard for 16-bit and larger systems.

Unix to PC networking
Distributed processing, using the most widespread, commercially available desktop microcomputer, is the goal of an Ethernet-based Unix network recently announced by Plexus Computers, Inc (Santa Clara, Calif) and LanTech Systems (Dallas, Tex). The network lets users of the IBM PC take advantage of Unix files, utilities, and multiuser capabilities.

LanTech’s uNETix, a single-user Unix-compatible operating system for the PC, includes software interfaces to Plexus’ network operating system (NOS). Together with a standard Ethernet interface board, the system turns the PC into a very intelligent distributed workstation with access to the resources of a supermicrocomputer. It is available 90 days ARO for $250 from LanTech.

Modularity is built into Unix, although the granularity is different than in CP/M. All data is treated as a character stream—a one-dimensional series of bytes. Programs accept streams through their standard input, process them, and emit them from the standard output. This approach facilitates the creation of software tools. These small, well-understood, and tested programs can be strung together easily to do any job needed.

It also makes a hierarchical file structure imperative, to keep the hundreds of small tools from cluttering the programmer’s “workbench.”

Strictly defined and adhered to, a character stream approach also imposes time and space penalties on applications, such as data bases, which use two- (or more) dimensional data structures. Transferring a large data array byte by byte can be a long process.

Vendors like Plexus are working to make a distributed Unix environment a viable competitor to IBM’s 3270/SNA network connections to and between mainframes. While it is undoubtedly a good environment for programmers to work in, Unix has been described as being “user-hostile.” The face it presents to the casual user is both cryptic and confusing.

While IBM’s batch-processing interface may leave much to be desired, particularly in the realm of job control language, there are a

(continued on page 52)

World-Class Components Update:

RELAYS

Fujitsu Gives You The Most Technologically Advanced And Comprehensive Line Of Relays In The World.

When it comes to PC-board-type relays—electromechanical, mercury-wetted, reed—nobody can touch Fujitsu for quality and reliability, performance and sophistication.

Fujitsu technology produces relays no other company can. Such as the world’s smallest electromechanical relay, the FBR-20. Fujitsu provides relays with such outstanding size-to-performance characteristics that major automobile makers use them in state of the art keyless door systems, voice electronics and other applications.

When the problem demands a mercury-wetted solution, Fujitsu offers the finest made. A relay that features a reliability rate many times better than the competition. And proven performance that’s tested to 20 billion operations.

Fujitsu relays are UL recognized and CSA certified. Because the line is so complete, there is a Fujitsu relay for nearly every application—such as process control, telecommunications, automotive, automatic test equipment. Or if you have a specific design problem, Fujitsu can customize a solution with its wealth of technological experience and resources.

For years, Fujitsu has been on the leading edge in developing breakthrough, problem-solving technology. Offering companies, worldwide, uncompromising quality and reliability—the result of Fujitsu’s insistence on controlling, in house, every aspect of the design and manufacturing process. And delivering—with the highest level of service and absolutely competitive prices.

Find out more about World-Class Relays from Fujitsu. Contact your value added Fujitsu Distributor or Fujitsu directly.

World-Class Components
Part of Tomorrow’s Technology

Component Division Fujitsu America, Inc.
918 Sherwood Drive, Lake Bluff, IL 60044
(312) 295-2610 Telex: 206196 TWX: 910-651-2559

FUJITSU

World-Class Components
Part of Tomorrow’s Technology

CIRCLE 182
LANS proliferate
(continued from page 51)

host of productivity tools, text editors, and utilities (eg, SPF) are available from both IBM and independent vendors. These tools and interfaces, called shells in Unix, are being developed, and even exist in full form at some installations. However, they are not generally available to the business user.

More specifically, this uNETIX-Ethernet combination competes directly for board and disk space with IBM's recent PC/3270 (for communications) and PC/370 (for executing mainframe software in the PC) products. Neither system makes provision for communicating with the other—except, perhaps, by writing data to the PC disk, and rebooting with the other operating system to read it. This is, however, an inherently slow and clumsy process. In the absence of formal standards and user demands for compatibility, manufacturers will continue to create technical solutions that cause intercommunication problems.

Unveiling a new "standard"

Billing it as "The standard in network software," SofTech Micro systems (San Diego, Calif) has introduced Liaison, a networking implementation of the UCSD p-System. Liaison includes a limited multiprocessing operating system ($750 to $4000, depending on number of users), a disk server ($150) to manage files for remote users, a print server ($150), and a tool kit ($200) to help develop Liaison systems.

The system is presently available for the Apple IIE, IBM PC, TI Professional, and Corvus Concept computers. It communicates via the Corvus Omninet LAN. Implementations for other computer systems and other LANS are slated to become available later this year.

An intriguing, and somewhat lamentable, feature of the system is the Liaison Monitor, which allows the independent seller of the system to limit the number of simultaneous users. This is justified in SofTech's literature as a way for software developers to ensure profits by charging different prices for the same program, according to the number of users. While the goal of networking and communications is to increase productivity by making data and programs more widely available, profitability is generally the motivating force behind business. But this seems like a step backwards—the same thing can be accomplished cheaper with a single program on a single disk that will only run on a single machine (eg, VisiCalc on the Apple).

While the UCSD p-System has a wealth of tools, a Pascal that cures most of the standard language deficiencies and a large, vocal, and active programmer community, it is by no means a standard or "universal" operating system. Standards are created by the general consensus of large numbers of vendors and users. Despite the fact that the majority of p-System users have bought it from Apple Computer Inc (Cupertino, Calif), and not SofTech, the latter shows a certain lack of interest or awareness that anyone else exists in the data processing world.

Technically expert users feel that Liaison is an excellent solution to networking between machines running the p-System. It addresses the needs of a multi-user system very well, providing for interchange of data and program source and object files, as well as the file-locking and password protection necessary to keep a multi-user system secure. It is modular, and provides services at all seven levels of the ISO interconnection model.

It does not, however, make direct provision for communication with other systems which are not running Liaison, whether they are non-Liaison p-Systems or others. Some of this lack can be charged to the vendor; but a greater percentage must be charged to the whole industry and user community worldwide, in delaying the implementation of clear interconnect standards and translation protocols.

—Sam Bassett, Field Editor

Window worlds open to independent programmers

The open applications environment and the desktop metaphor are common concepts among the newer 16-bit operating system user interfaces. Notable among these are the Lisa by Apple Computer, the Windows system by Microsoft, and VisiOn by VisiCorp. The desktop metaphor uses windows, icons, menus, and a mouse to select actions and is obviously meant to make the systems appealing to those who are not totally familiar with computers. The open application environment, however, has two purposes: to allow the user to select and run applications from different software vendors, and to encourage independent software vendors (ISVs) to write applications for the window environments.

To this end, Apple Computer (Cupertino, Calif), Microsoft (Belle vue, Wash), and VisiCorp (San Jose, Calif), have come up with ISV programming aids and support. They have also specifically designed their operating environments to make it easy to adapt independently produced applications programs to their computers. Such ISV support has appeared in the form of "tool kits" for adapting to the world of windows and as porting aids for adapting existing programs to the new environment.

Porting existing software from other systems can be done in two ways. In some cases, programs can be recompiled and adapted to a subset of the window environment. In other cases, an application must run in a window which simply emulates a standard alphanumeric terminal. The programmer may (continued on page 54)
First we brought you the Ω400 Display Controller, with 1024 x 768 resolution, 8-bit planes and one million pixels/second vector drawing speed. This innovation introduced state-of-the-art color graphics performance from a single circuit board, providing OEMs with the ultimate in reliability, flexibility and price.

Now, Metheus has moved even further ahead with the Ω500, first of a new generation of color graphic display controllers.

Ω500: New standards in resolution, refresh and ergonomics. Still on a single board.

The Ω500 Display Controller sets a new standard in graphics display ergonomics, bringing you brighter, crisper images and truly flicker-free displays. It has the highest resolution available, 1280 x 1024 at 60Hz non-interlaced refresh, the rate needed to drive the latest 100MHz monitors.

Ω500's bit-slice processor supports drawing speeds ranging from 1.5 million to 120 million pixels per second.

And, once again, Metheus' advanced graphics technology is neatly packaged on a single board for exceptional reliability and efficiency. On-board signature analysis circuitry and extensive self-testing capability ensure consistent, dependable operation and fast diagnosis of any malfunction.

A Writeable Control Store (WCS) feature allows OEMs to customize the controller's instruction set for a wide range of specialized customer applications.

The Ω500 is software compatible with Ω400. And, both are supported by Metheus' Axia™ Graphics Package, built around the ACM SIGGRAPH CORE and designed to speed and simplify your application software development.

Let Metheus put you a generation ahead of your competitors.

Both the Ω400 and Ω500 are available as display controller or integrated graphics subsystem incorporating a high resolution monitor. And both are available for immediate delivery in quantity.

If color graphics are a part of your product's future, you owe it to yourself and your customers to talk to Metheus today.
Window worlds
(continued from page 52)

The machine-dependent interface, VisiHost, connects the VisiOn environment to the host operating system. Applications written by VisiCorp, as well as those by ISVs, run consistently in the VisiOn world sharing user interface and data.

later have the option of rewriting routines in the ported application to make it work more closely with the world of windows, but at least the existing software investment is preserved in the new environment.

The Apple Lisa system has a tool called QuickPort, which enables applications written in Basic-Plus, Cobol, or Pascal to be quickly moved to the Lisa Desktop. Such applications readily make use of complementing screen features. They will have their own menu, window, icon, and stationery pad, as well as be able to utilize Lisa's scrolling and printing interfaces. Thus, although the Lisa uses an object-oriented programming approach, nonobject-oriented programs can be written for it and can interact with the user in a Lisa-like manner.

For programs that have been developed in a Unix-only environment, Lisa runs the Microsoft Xenix and the UniSoft UniPlus+ versions of Unix. In the Unix environment, the Lisa user-interface features are not available. The "window" occupies the entire screen and emulates a 24 x 80 alphanumeric terminal. Unix programs can thereby be ported to Lisa, or Lisa can be used as a development station for Unix programs running on other systems.

One main difference exists between the Lisa world and the window systems offered by VisiCorp and Microsoft. Lisa is a hardware environment with its own operating system, while the latter two represent extensions to existing operating systems. Microsoft's Windows is an extension of its own MS-DOS operating system. VisiCorp's VisiOn interfaces to other 16-bit operating systems via a machine-dependent VisiHost/operating system interface. Microsoft does provide the ability for a window to emulate a VT-52 type terminal for straight alphanumeric I/O. But, applications that write directly to hardware, bypassing MS-DOS, will not run in a window. Here, in contrast to Lisa, the portability issue involves porting the program to the MS-DOS environment rather than to a hardware system. Unix-only programs would obviously not run under MS-DOS. On the other hand, Microsoft provides language bindings to six languages that give them access to the standard features of Windows when compiled under MS-DOS.

Program development
In all three approaches, applications are able to take full advantage of user-interface features when they are written specifically for that environment, and all three companies provide tools for the ISV to do that. Each of the three, however, has a somewhat different focus. Apple is primarily a hardware manufacturer with its own operating system. Microsoft has concentrated primarily on the MS-DOS operating system running on a wide variety of machines. VisiCorp has focused mainly on consistent application software that runs in a number of operating systems. The three companies are also aware that they cannot service the full demand for applications, and hence the importance of the ISV.

Apple provides a development environment called the Workshop that consists of a Lisa machine, the ToolKit/32 package, which includes the Generic Application, QuickDraw graphics, and an object-oriented extension of Pascal called Clascal. The Generic Application can start software development using all of Lisa's standard user-interface features, including cut/paste integration, scrolling, menu handling, and window management. Since applications are built using ToolKit/32, all programs written with it will have a consistent user interface.

Programming with Clascal on the Workshop takes an object-oriented approach where the user describes characteristics and interactions of objects, such as windows, which comprise the application. The Generic Application contains a library of object descriptions (windows, documents, commands, etc). The developer has only to describe the objects needed to make up a specific application and the characteristics that might make a given object distinct. Syntax is very close to that of Pascal.

VisiCorp's approach with VisiOn is first to interface the VisiOn environment to a given operating system environment. Applications are then built on top of VisiOn using VisiC, a dialect of the C language, and C extensions (eg, the menu compiler, the help compiler, and the forms compiler) to create the user interface. These compilers turn C-like code into the menus and screens that make up the window interface of VisiOn.

(continued on page 56)
Options up to 1.0 MIPS.

Expandable to 4M bytes ECC RAM.

Multi-user: supports up to 28 serial ports.

For $9,326.63* Computer-Automation's implementation of Bell Laboratories' UNIX, using dataCASE/5 and the Series 5 computer, delivers mainframe performance in an attractive desktop package. This highly expandable, packaged system offers OEMs and Volume End Users an exceptionally efficient cost per user ratio. And we have the benchmark tests and the price tag to prove it.

Call us, toll free (800) 556-1234, Ext. 25.
In California, call (800) 441-2345, Ext. 25.

UNIX is a trademark of Bell Laboratories.
*For OEM quantities, not including UNIX software license fee.
Window worlds
(continued from page 54)

With these tools, the program developer can create a standard interface between the user and all products that run under VisiOn. The interface, called Basic Interaction Techniques (BITS), includes a mouse input, forms input, and multimedia (combined mouse and text) input. Interaction with devices is via VisiOps which provides high level services between the C program and the VisiHost/operating system interface. VisiCorp provides its ISV toolkit in the form of packages that run in the Digital Equipment VAX Unix environment or on a 68000-based Unix system.

In the world of Microsoft Windows, the system takes responsibility for screen management, data exchange, and device independence. There is an icon editor to allow the ISV to create unique icons for the application which are then displayed as available in the windows display.

For communicating with external devices, primarily bit-mapped displays or other output devices, the programmer can write in terms of a graphics device interface (GDI) which provides primitives for an "abstract device." Hardware OEMs will assume responsibility for providing physical device drivers that interface to the GDI on systems running windows. Thus, any program written for Windows will run on the devices supported by any system running Windows.

Microsoft has also provided a way for programs from different vendors—written using the ISV toolkit—to exchange data. Applications from Microsoft itself will use the Symbolic Link (SYLK) data interchange protocol. However, the toolkit also allows data to be passed between applications in uninterpreted binary or in ASCII form. Programs would have to find and agree on a protocol before they could share data.

One effect of the open application trend may be the emergence of a standard for the human interface. By not withholding interface tools from ISVs, the major companies are not only encouraging vendors to write software for their systems, but are also encouraging the use of ready-made tools. These tools will provide users with a familiar way to interact with the new generation of applications.

—Tom Williams,
West Coast Managing Editor

Integrated Circuits

Chip finds degree of similarity between strings

Adaptive pattern recognition techniques have to date been mostly software systems that try to deal with information based on inexact, inaccurate, or incomplete data. One of the main problems has been determining the degree of similarity between strings. That function—computing similarity—has now been placed on a silicon chip called the PF474 microcircuit by Proximity Devices Corp.

The Proximity Filter PF474 performs extremely fast serial string comparisons and computes a degree of similarity for each. This comparison is expressed as a 32-bit binary fraction. Two totally dissimilar strings will yield a zero, while two exactly matching strings will produce a one. In computing the degree of similarity, the PF474 uses a set of parameters that are stored in onchip RAM. The 16 best matches are then stored in the ranker section of the chip, which also contains flags to locate the 16 next best matches, and so on. The Proximity computer section and the ranker operate in a pipelined mode so that neither need slow down the other in order to complete an operation.

Software comparison algorithms have yielded computation times that are proportional to the square of the number of characters in the string. With the PF474, however, the comparison time is linear with the length of the string, provided data is supplied at the chip's full input rate. This can be quite fast, since the PF474 is mapped into memory address space and has a DMA capability of up to 2 Mbytes/s. Thus, 8-character (byte) strings can be compared at a rate of 49,600 comparisons/s, while 127-byte strings run at 3870 comparisons/s.

The PF474 normally operates by taking a query string, for which parameters of similarity have been loaded into its parameter RAM, and rapidly searching through a long list of comparison strings in a data base. It is thereby possible to perform an exhaustive search in an acceptable amount of time without having to limit the search space and risk missing some similar strings.

To the system, the PF474 looks like a 1024-byte address range that is partitioned into four 256-byte sections: control, parameter, string, and ranker. The chip also contains the special purpose Proximity computer core which calculates the comparisons. The string section is further divided into two 128-byte sections to hold the query string and the string currently being compared to it. Since a string must be terminated by a null character, strings of up to 127 bytes in length can be processed.

The Proximity computer uses the 256 values stored in the parameter RAM section to compute the similarity. The fact that the parameters are stored in RAM means that they can be set and altered by the user, or even dynamically by a running program. This is quite important because the same kinds of parameters that work for English might not work as well for French or proper names, and a signal-processing application might require different parameters altogether. The three
FROM GENERAL CABLE FIBER OPTICS

Cables for all installation environments, to meet your specific transmission requirements. General Cable has been involved in fiber optics for over a decade. In 1976 we manufactured the cable used in the world's first fiber optic system for commercial telephone service. Today, we provide fiber optic cables for all applications—from telephony to data communications.

GenGuide® SINGLE MODE CABLES
Provide system engineers with a readily expandable transmission network. Expandable, by simply upgrading terminal equipment. GenGuide Single Mode cables are available with a variety of protective sheaths for duct, aerial and direct buried installations.

GenGuide MULTIMODE CABLES
Available with fiber types to meet end-use attenuation, bandwidth and light source coupling requirements. Cable designs include those for intra-building use, patching terminal equipment and outside plant installation.

FIELD AND ENGINEERING SERVICES
Complement the GenGuide fiber optic cable line. Whether you want us to supervise your installation, provide training in splicing and measurement or recommend the proper ancillary equipment, General Cable has the experience and knowledge you need.

For more information about our line of GenGuide Optical Fiber Cable write: GENERAL CABLE COMPANY FIBER OPTICS DIVISION 160 Fieldcrest Avenue, Edison, NJ 08818 or call: (201) 225-4780

GenGuide® is a registered trademark of General Cable Company A Unit of The Penn Central Corporation
In their search for innovative IC designs, here's why telecom equipment and systems manufacturers come to SSI.

- It's the company who produced the industry's first fully integrated Dual Tone Multiple Frequency (DTMF) receiver.
- It's the company who has developed switched capacitor filter technology to its present state-of-the-art.
- It's the company with the capability to produce analog or digital circuits—or both—on the same chip.

In their search for production credibility, here's why the telecom leaders also come to SSI.

- It's the company with the industry's newest and most efficient wafer fab for production at optimum yields.
- It's the company with both Bipolar and CMOS multi-process capability in the same wafer fabrication facility.
- It's the company with the proven track record of ramping up its production on the industry's most popular Touch-Tone® receiver to keep pace with an exploding market.

And here's why those telecom companies looking for a competitive edge come to SSI.

- It's the one company they can rely on for their "Applications Specific ICs"—from SSI's standard or semicustom products, or to full-custom specifications.

For an overview of Silicon Systems' DTMF's, Modems, Speech Synthesizers, and Switched Capacitor Filter Arrays, send for the new SSI Telecom Brochure.

Silicon Systems incorporated,
14351 Myford Rd., Tustin, CA 92680
(714) 731-7110, Ext. 575.

*Touch-Tone is a registered trademark of AT&T.
The SSI 201 DTMF receiver is the industry-standard one-chip solution for many telecom applications. It detects a selectable group of 12 or 16 digits, with no front-end filtering required. And its innovative design eliminates the need for all external components except a 3.58 MHz crystal and an inexpensive resistor.

The SSI 202 incorporates the features of the SSI 201 in a low-cost, 18-pin, plastic package. This lower cost unit also dissipates lower power and operates on 5 volts, making it compatible for use with microprocessors and suitable for consumer electronics. An additional "early detect" feature is provided in the SSI 203, the newest unit in SSI's growing line of Touch-Tone circuits.

To find out more about the industry's First Family of DTMF receivers, contact: Silicon Systems, 14351 Myford Road, Tustin, CA 92680, (714) 731-7110 Ext. 575.

*Touch-Tone is a registered trademark of AT&T

In the PF474 architecture, four major blocks, string space, control, parameter tables, and ranker, appear to the system as memory address ranges and can be directly addressed. The Proximity computer generates 32-bit binary fractions that are used by the ranker to establish the list of 16 best matches.

The parameters stored in each byte are weight, compensation, and bias.

Weight is a direct reflection of the importance of a character in the string, and can vary in value from 0 to 7 (3 bits). For example, in comparing English words, less weight would be assigned to vowels than to consonants and different consonants might have different weights according to the similarity or difference of the sounds they make. A weight of 0 would be almost ignored, but it would affect the similarity since it occupies a position in the string.

The bias parameter tells if a character is more important near the beginning or near the end of the string. Bias can range from a value of −2 to +1. For instance, if all characters had a negative bias, the computer would assign more importance to similarity near the beginning of the word than near the end.

Compensation considers the dissimilarity between two characters and whether a word contains a given character or not, or whether a given character is in the same position in both words. The compensation value of unmatched characters is cumulative in a comparison. Setting a high compensation parameter will make the comparison more tolerant of dropped characters.

This type of pattern recognition therefore necessitates two main (continued on page 60)
Advanced Multibus Products

Powerful 68000
SBC, Graphics
Complete Software
Development Tools

Featuring a 10MHz 68000 processor, a high performance Multibus™ graphics controller and add-on memory. The board level products of Forward Technology combine low price to keep your systems cost down, and high performance to keep your customer satisfied.

Single Board Computer... FT-68X
- 10MHz MC68000
- 2 level MMU
- 256 KB No Wait State Memory
- Dual Port DMA
- 8 MB Addressability

Fast, High-resolution Graphics... FT-1024
- 1024 by 1024 by 1 frame buffer
- Bit-map organized in (X,Y) coordinates
- Simultaneous access to 4 different graphical objects
- On-board “raster OP” implementation
- One 16-bit update executed each microsecond

Large-capacity Add-on Memory... FT-768
- Add-on memory for FT-68X
- Single board
- 768 KB of no wait state RAM
- Supported by FT-68X DMA

XENIX™ Operating System
- FORTRAN 77, C, PASCAL, APL, and BASIC language support for multiple users.

Forward Technology products for forward looking OEMs. Send today for full information.
2175 Marlin Ave., Santa Clara, CA 95050.
(408) 988-2378

Western Regional Office (213)541-0166
Eastern Regional Office (617)890-6131

*Multibus is a registered trademark of Intel Corp
*XENIX is a registered trademark of Microsoft Corp

CIRCLE 30

SYSTEM TECHNOLOGY/INTEGRATED CIRCUITS

Chip compares strings
(continued from page 59)

Each of the 256 parameter bytes is divided into three fields as shown for compensation (0 to 7), bias (-2 to +1), and weight (0 to 7) attributes for each character in the strings being compared. Different combinations of parameters can set widely varying criteria for similarity.

... (continued on page 64)
CONFIDENCE BUILDERS

- Designed with the clearance/creepage spacing and hi-pot ratings required to meet IEC 380 and VDE 0806
- Input filter conforms to VDE 0871/6.78 and FCC 20780 Part 15, Subpart J
- Complies with UL 478 and CSA C22.2 154
- Quality control according to MIL-I-45208
- Holdup time of 20 ms
- Efficiencies of 70 to 80%, dependent on output voltage
- User-selectable 115/230 VAC dual input
- Overvoltage protection standard
- Overload protection standard
- Short-circuit protection standard
- AC transient suppression
- Logic inhibit on many models
- Remote or local sensing on most models
- Cover included with all models

20 Single Output Switchers, from 5 to 24 V and 2.5 to 60 A

50 W

180 W

288 W

120 W

384 W

POWER/MATE
THE PACESETTER IN SWITCHING POWER SUPPLIES

POWER/MATE CO.
514 South River Street, Hackensack, NJ 07601-6697 • (201) 440-3100 • TX: 710-990-5023
10951 Coventry Place, Santa Ana, CA 92705-2315 • (213) 793-4070 • TX: 910-588-3285

CIRCLE 31
If you’re manufacturing a product with an ergonomically designed keyboard, you need one of these three Stackpole advantages!
Actually, there are a lot more advantages to Stackpole keyboards. Start with the confidence you can have in the keyboard because it was made by Stackpole. We had built our reputation for high-quality components long before the age of the computer.

But as a manufacturer of products with keyboards, knowing that the quality of the keyboard is critical to the quality of your product, you should know about these three Stackpole advantages.

The KS-200E—Mechanical Technology

In the KS-200E, Stackpole has combined the newer discipline of human engineering with its tradition of engineering components to work well and last longer. The result—a full-travel, ergonomically designed, highly reliable keyboard that projects quality where the fingers meet the machine. The KS-200E meets the most recent DIN requirements.

The built-in reliability of the KS-200E begins with the sturdy monolithic housing that assures keycap alignment and reduces cost by reducing inventory. Then there are the patented twin bifurcated contacts; that’s four points of contact that assure reliable operation over the KS-200E’s rated life of fifty million cycles.

And—unlike many keyboards—the KS-200E is field repairable. In a matter of minutes.

The KS-200E is available just as you need it—as discrete switches or arrays assembled with or without keycaps, or assembled and soldered to a PC board with or without electronic encoding to fit your specifications. So that we can be an important part of your solution without creating any problems.

The KS-500E Membrane Keyboard

The KS-500E shows just how good a membrane keyboard can be. Full travel. Ergonomically designed to the latest DIN requirements. Engineered into a monolithic housing that eliminates keyswitch alignment problems. It has a lot in common with its cousin—the KS-200E.

And because the screened circuit traces and contacts are laminated between two pieces of polyester, the KS-500E is protected against spills and other environmental contaminants.

The metal backplate gives built-in EMI/RFI protection.

If your design calls for a membrane keyboard—one that works well from the first touch and will continue to work well over its rated life of 20,000,000 cycles—ask about the KS-500E. It’s available in a wide selection of two-shot keycaps, a variety of colors and finishes and in either low profile or ultra-low profile.

Stackpole Development Services

We know that in your business, one size—or style or array—does not fit all. That’s the reason we put a very experienced staff of applications engineers at your disposal.

Along with the experience, the talent and the proven ability to meet manufacturers’ specifications and engineers’ hopes, our development services bring you Stackpole’s testing facilities, our custom manufacturing capabilities—and the same thing you get with every Stackpole keyboard—Stackpole quality.

So if the KS-200E or the KS-500E looks like just the keyboard for your product, call us. And if they don’t fit, call us anyway. We can build you one—either domestically or at our Far East facility.
Terminals move to X.25 transparent to host

Local and remote terminal users move freely between Digital Equipment's VAX-11 computers and packet-switched networks with a frontend communication processor from Advanced Computer Communications. The IF-11/X.25 Plus handles any necessary packet assembly and disassembly (PAD) called for in the X.25 specification, as well as necessary terminal protocols, without host intervention. The host services each terminal in a normal time-sharing fashion, regardless of where it is physically located.

Such transparency results from the ability to emulate a terminal multiplexer, such as the DH-11. Few modifications to existing software drivers are needed. Furthermore, the host computer cannot distinguish between attached and remote terminals. The controller hides its ability to operate in one of two modes: access by remote terminals only, or in access by attached and remote terminals.

Remote terminal access is the most straightforward of the two modes, since the 32 data ports dedicated on the host computer handle just incoming calls. Local terminals require additional hardware support since they can initiate X.25 conversations as well as converse with the host system. As a result, the IF-11/X.25 Plus allocates one of the 32 channels for each attached terminal, with the remaining channels free to support remote terminals.

Under either hardware configuration, remote users initiate a terminal session by placing a call to the desired network node. Packet switched networks typically use dialup lines for these incoming calls, with RS-232 serial communications used as the physical link. Implementation of the high level data link (HDLC) protocol at the transport layer (ISO layer 2) ensures error-free data transmission. Messages are transmitted across the network at 56 kbits/s. Incoming calls can either choose a specific port address (1 to 32) or allow the controller to assign the lowest port address available.

In addition to routing incoming calls to the appropriate port address, the controller handles PAD functions. The data link established at layer 2 is divided into 32 logical channels. These channels identify individual user conversations that have been combined for transmission over a single trunk line in the packet network.

Packets also contain session and presentation-dependent information such as baud rate and terminal characteristics (ISO layers 5 and 6) enabling the user to communicate effectively with the remote host. Moreover, the IF-11/X.25 Plus translates these parameters (which are set forth in the X.3 and X.28 specifications) into specific terminal protocols (eg, VT100). If necessary, users can reconfigure a remote network node with parameters defined in the X.29 specification.

Besides handling incoming calls, the IF-11/X.25 Plus also provides a means for local users to send packets to remote network nodes. Terminal line expansion boards link as many as 32 users (in groups of eight) to the controller, although the host computer cannot tell the difference. All ASCII terminal functions are available to each user. In fact, terminal communications can occur at a rate as fast as 9600 bits/s.

Only when the user enters a special character sequence does the controller come into play. The user, in effect, disconnects from the host and further terminal communications are routed to the controller for action. Special PAD commands are then used to connect an X.25 data network, as well as to move back to local mode for further interaction with the host computer. Users need not log off the host system at all to enter the PAD mode.

The IF-11/X.25 Plus occupies a double hex-width Unibus slot on any PDP-11 or VAX-11 minicomputer running RSX-11, VMS, or Unix operating systems. The device driver is included in the $9000 single-unit price; each optional terminal expansion board is priced at $3000.

Advanced Computer Communications, 720 Santa Barbara St, Santa Barbara, CA, 93101. Circle 241
AST Research, the leader in IBM PC enhancement products, brightens your micro/mainframe communications picture with a full palette of economical, integrated hardware/software masterpieces. With AST Products, you can emulate IBM terminals or create PC-based Local Area Networks.

**AST improves your office operating cost picture.**

AST communications products give your IBM PC the flexibility to act as a terminal for your host system or as a stand-alone computer for smaller tasks. Your PC won't bog down the mainframe with unnecessary small jobs and local computing on the PC eliminates phone line charges too. Get the power of a mainframe when you need it and personal computer convenience right at your fingertips.

**Applications solutions that are strokes of genius.**

AST keeps pace with your ever-changing applications requirements with reliable, high quality, cost effective communications products. AST products provide support for Bisync and SNA/SDLC communications protocols as well as networking multiple PCs for sharing resources.

**Choose AST products — by the numbers.**

These AST communications packages are currently available:

1. AST-SNA™ emulates a 3274/3276 controller and 3278 or 3279 display terminal using SDLC protocol.
2. AST-BSC™ emulates 2770 batch RJE and remote 3270 display terminals using 3270 Bisync protocol.
3. AST-PCOX™ allows your PC to connect to an IBM 3274/3276 cluster controller via coax cable and emulates a 3278 or 3279 display terminal.
4. AST-3780™ emulates 2770, 2780, 3741, and 3780 RJE workstations using Bisync protocol.
5. AST-5251™ emulates a 5251 Model 12 remote workstation connected to an IBM System 34, 36 or 38.
6. PCnet™ is the first Local Area Network designed specifically for the IBM PC or XT and the PC-DOS 1.1 or 2.0 operating system.
7. CC-232™ is a user-programmable dual-port card capable of communicating in Async, Bisync, SDLC, or HDLC protocols.

Discover how well AST can fill in your micro/mainframe communications picture. For descriptive data sheets, write or call: AST Research Inc., 2121 Alton Ave., Irvine, CA 92714. (714) 863-1333. TWX: 295370ASTRUR

---

**CIRCLE 34**

**AST RESEARCH INC.**

**Number One Add-Ons For IBM PC.**

IBM in a registered trademark of International Business Machines Corporation. PCnet is a registered trademark of Orchid Technology Inc. AST is a product developed by AST Research, Inc., and Wiltron Systems, Inc. AST-3270 is a product developed by AST Research, Inc., and Software Systems, Inc., of Jefferson City, MO. PCnet is a product developed by CU Inc.
Make your 212A modem
for half the cost.

Your Design Problems are Over
Now available to you are the LSI circuits and software know-how needed for your own design and implementation of an operational Bell 212A compatible modem—all from one experienced source, Exar.

Exar Delivers the Solution
First, you get high technology, quality IC's that form the heart of a 212A modem. The XR2123 CMOS Modular/Demodulator provides the 1200 BPS PSK function, the XR14412 modem system performs the 300 BPS FSK modulation/demodulation function required for the 212A compatibility and the XR2120 switched capacitor filter, also CMOS technology provides the 1200 and 300 BPS filtering requirements for the modem.

But, Exar does not stop there. In order to implement these devices into a compatible Bell 212A modem, we have devised a simple and cost-effective trouble-free way to evaluate them in a system. Exar can provide you with a modem evaluation kit including these three devices, along with all the necessary supporting components, PC board, schematic and operating instructions to minimize your design task.

Cut Costs, Reduce Space, Improve Reliability
By getting our IC's along with our know-how you make sure your modem will be right. With our LSI components, you get a modem for about half the money you would normally spend for a finished board and reliability is improved because our LSI circuits reduce the number of necessary parts and the space to house them.

More Modem Solutions
Exar provides modem solutions for a wide variety of applications, from telephone communications compatible with Bell and CCITT standards to high-speed transmission over twisted-pair wires. Modern types available include Bell Standard 103 (300 BPS FSK), 202 (1200 BPS FSK), and 212A circuits as well as CCITT compatible V.21 (300 BPS FSK), V.22 (1200 BPS FSK), V.23 (1200/75 BPS FSK) and V.26 (2400 BPS PSK). To round out a complete design Exar provides RS-232 line drivers and receivers for interfacing and a wide range of op amps to perform amplification and signal conditioning functions.

212A Compatible Modem
The Solution is Available Now
Just send the coupon below or give us a call. You'll get everything you need, including our compilation of modem design and technical data, called the Modem Data Book. So let Exar get your modem design going. Send us the coupon today.

Help me make my modem!
☐ Send me the Exar Modem Data Book.
☐ Also, send me more information about the Modern Design Kit.

Name ____________________________
Title ____________________________
Company _________________________
Dept./Div. _________________________
Address __________________________
City _____________________________
State __ Zip __
Phone (____) _____ Ext. __
Application _______________________

750 Palomar Avenue
Sunnyvale, CA 94088
Tel. (408) 732-7970 TWX 910-339-9233
For telecommunications, industrial, medical and military IC applications...

EXAR

CIRCLE 35
Fujitsu believes deserves love.

See us at Interface '84, March 12-15. Booth #786-790.

The world's first 14.4 kilobit modem card; superior reliability in a compact package. 9,600 bps & 4,800 bps core modems and stand-alone modems also available.
That's why Fujitsu now offers the world's first 14,400 bit per second modem card, along with companion 9,600 bps and 4,800 bps core modems. All three single PC boards employ custom digital signal processors. And from a standpoint of versatility, the units are compatible with any type of equipment.

By offering your customers the fastest, most reliable, and economical modem, you're not only offering state-of-the-art technology, but a product that is backed by a world leader in the telecommunications and computer industry.

We also realize that diversity sells your products and increases your profits. So, Fujitsu not only offers core modems, but also offers a full line of stand-alone modems.

Fujitsu modems meet the future head on. And that's the kind of fast talk you deserve.
"Backup claims"

Low Cost
Small Size
High Capacity
Innovative

Operator Control
Interchangeable
Performance
Standards
were too confusing.
Then I called Cipher.

Whether you need a ½" tape drive compatible with streaming or start/stop software, we have your solution with our Microstreamer® or CacheTape™.

Or whether you need a ¼" cartridge tape drive compatible with OIC or floppy disk standards, we have your solution with our 540 or FloppyTape™.

The next time you find backup confusing, call the leader. No matter what your system requirements are, we have the tape drive that meets your backup needs. Call or write us today for a free product brochure.

Cipher Data Products, Inc.
10225 Willow Creek Road, P.O. Box 85170
San Diego, California 92138
Telephone (619) 578-9100, TWX: 910-335-1251

European subsidiaries in:
United Kingdom (phone: 0276-682912),
West Germany (phone: 089-807001/02),
France (phone: 1-668-87-87)

CIRCLE 37
We can’t keep it quiet any longer!

Occam is the language for today’s microprocessors

Today’s microprocessor systems are growing up. New boundaries in performance and functionality are being called for and met.

But software tools are falling behind. Assembler programming is woefully inadequate. Traditional high level languages—Pascal, C—leave critical portions of the systems to low level languages. And new languages like Ada are too complex for serious consideration.

Where can systems designers turn? Occam.

Occam is a new language created just for system design and implementation. With the ability to describe concurrency and message passing built right into the language at the lowest level, all aspects of a system can be designed and programmed in occam. From interrupt handling to signal processing to screen editors to artificial intelligence. And it’s available for the iAPX86 and MC68000 families of microprocessors now.

With the Occam Programming System, INMOS provides the optimum environment for the creation of occam systems for these microprocessors. An intelligent editor understands the language. Source-level debugging lets you investigate the behavior of your program in terms of the program you have written. There’s even a word processor package.

Together with the abilities of the language, these features will significantly reduce your development time and risks.

Even more, occam equips you for the future. As increased performance requirements move you into multiprocessor systems, your software is already written. Occam programs may be configured to run on one, many or even hundreds of connected processors. And you’ll also be ready to take advantage of the massive increase in performance that INMOS’ transputers—a family of 16 and 32 bit VLSI devices integrating processor, memory and communications onto one chip—will offer.

We have a complete set of evaluation and development tools available for occam. Send today for informative literature pack which describes occam, the Occam Evaluation Kit, the Occam Programming System and the transputer.

For immediate response call us at (303) 630-4363, or write:
Occam, P.O. Box 16000, Colorado Springs, CO 80935. We’ll take care of the rest.
TRIPLE-BUS ARCHITECTURE GAINS SPEED, VERSATILITY

Both problems and opportunities lurk for designers of realtime minicomputer systems. A three-pronged approach attacks the problems inherent to single-bus architectures.

by Dave Cane and Steve Mullen

In traditional minicomputer architecture, a single high speed internal bus transfers digital data throughout the system. However, the problems inherent to this design can be overcome with an alternative, multiple-bus architecture. Using multiple industry standard processors with multiple industry standard buses, the MC-500's 32-bit architecture distributes data acquisition, computation, and graphics tasks among several very high performance processors.

The main system CPU uses a proprietary bus to connect the VLSI processors to system memory. A high performance Intel Multibus (IEEE 796) supports a data acquisition and control processor (DA/CP), up to four independent graphics processors (IGPs), and system peripherals. An enhanced STD bus—controlled by the DA/CP module—provides efficient data acquisition and control.

This triple-bus design, the core of the system architecture (Fig 1), provides a flexible structure that anticipates future system enhancements with technological advances in microprocessors, memory, mass storage peripherals, communication devices, and realtime interfaces.

Cumulative bandwidth in triple-bus structure

Since the primary design goal was to provide a one million sample/s analog acquisition rate, the bus that supports the A-D converter—the STD bus—must operate at 2 Mbytes/s. Operating at this speed, however, requires a 4-Mbyte/s transfer rate since the Multibus needs twice the bandwidth of the STD bus. This is necessary because, in analog throughput-to-disk applications, data must travel over the Multibus twice.

At first glance, it appears that the Multibus bandwidth will allow this rate. If a bus runs near capacity, however, bus latency problems may surface. Long latencies slow data transfer and generally make data acquisition/control performance highly unpredictable. Since the Multibus must also carry data traffic from system peripherals during data acquisition, it is loaded at 80 percent capacity. Thus, the Multibus transfer rate was designed at 6 Mbytes/s.

Dave Cane is a hardware development manager at Masscomp, 543 Great Rd, Littleton, MA 01460, where he is responsible for hardware design. He holds an MSEE and a BSEE from the Massachusetts Institute of Technology, Cambridge, Mass.

Steve Mullen is an end user marketing manager at Masscomp. He holds a BA from Lawrence University and a PhD from the University of Minnesota.
Primarily, the proprietary MC-500 bus serves as the CPU to memory connection. To allow the Motorola 68000 to operate at maximum speed, this bus is specified to transfer data at up to 8 Mbytes/s.

One 68010 and one 68000 microprocessor make up the MC-500 VLSI virtual memory CPU. A 4-Kbyte instruction and data cache are used to raise the microprocessors' speed. Memory management control supports up to 16 Mbytes of virtual memory space in a demand-page format.

Memory is mapped in 4-Kbyte pages. A 4096-entry address translation table maps virtual to physical addresses. A 1024-entry RAM-based address translation buffer operates as a cache for the full translation table, thereby improving performance. The CPU's 68000 processor handles memory management and address translation buffer "misses" (Fig 2).

The MC-500 bus connects the CPU to physical memory (storage capacity ranges from 0.5 to 6 Mbytes). The fastest bus in the system, it transfers blocks of data at up to 8 Mbytes/s. It also supports the optional Masscomp floating point and array processors.

Providing the CPU with a dedicated high speed bus avoids the time that would be lost on CPU/Multibus access arbitration if memory were placed on the Multibus. In addition, the 68000 processor uses an unusual handshake process—it notifies a bus that it will strobe data a full cycle before actually transferring that data. The Multibus protocol, however, is designed to move data almost simultaneously upon request. This causes the bus (as well as the processor) to be idle while it waits. The triple-bus design eliminates this bus wait state.

Finally, the system design is most effective when multiple main CPUs are integrated into a system. Rather than a multiple CPU architecture where the CPUs must share multiport memory access, each CPU has its own physical memory connected by an MC-500 bus (Fig 3).

**CPU/Multibus connection**

Using the industry standard Multibus (IEEE 796) allows the peripheral controllers, the data communication devices, and the data acquisition interfaces that exist for this bus to be attached to the system. Connected to the MC-500 bus through a Multibus adapter, the Multibus supports a DA/CP,
OB68K/VME1™

12.5MHz 68000/VME SINGLE BOARD COMPUTER

GENERAL DESCRIPTION
The OB68K/VME 1 is an extremely powerful, complete stand alone microcomputer board that is functionally interfaced to the double height (6U) VME bus and is fully compatible with the VME bus standard by way of the P1 connector.

FEATURES
- Powerful 12.5MHz 68000R12 16/32 Bit CPU
- 8 pairs of 28 pin sockets for ROM/RAM.
  - ROM 2732, 2764, 27128 or 27256 (Maximum of 7-pairs may be used, at least one pair required).
  - RAM 2K × 8 or 8K × 8 static (Maximum of 7-pairs may be used, at least one pair required).
- User selectable access time on (DTACK) RAM and ROM
- Directly addresses 16M-bytes.
- Offboard I/O space 64K bytes (short Address Modifier code)
- (7) Prioritized - BUS or AUTOVECTORED Prioritized Interrupts (One Non-Maskable)
- (2) RS-232C Serial Ports utilizing one 68681 DUART
- (2) 8 bit Parallel I/O Ports with two control lines utilizing one 68230 P1/T.
- (1) 16-bit Timer/Counter (in 68681)
- (1) 24-bit Timer/Counter (in 68230)
- VME Bus Compatible (Rev. B)
- All external I/O connections available through user defined pins on P2 connector.
- System controller functions are supported. They consist of:
  (1) 8-level Prioritized bus arbiter (68452)
  (1) 16-MHz system clock
  (1) Power-on Reset Generator
  (1) Manual Reset Generator
  (1) System watch dog timer
- All system controller functions may be inhibited for Multi-Master System use if desired.
- Two year limited warranty.

FOR MORE INFORMATION ABOUT THE OB68K/VME1 SEND $10 FOR A DETAILED TECHNICAL MANUAL.
Contact Sue Cochran, Sales Manager

OMNIBYTE CORPORATION
245 W. Roosevelt Rd.
West Chicago, IL 60185
(312) 231-6880
Intl. Telex: 210070 MAGEX UR

Quality, Reliability, Performance
as many as four IGPs, each incorporating a 68000 processor; multiple disk and tape drives; terminals; printers; plotters; and network communication via RS-232 and Ethernet. The Multibus adapter enables 32-bit block transfers, providing a bus bandwidth of up to 6 Mbytes/s.

Historically, the Multibus evolved from a 1-Mbyte, 20-bit address version to a 16-Mbyte, 24-bit address configuration. Putting both types of boards on a system creates a DMA address problem. A second DMA problem results because peripheral memory buffers are not continuous for virtual memory systems. Therefore, DMA controllers cannot handle transfers that cross page boundaries.

To solve these problems, the design incorporates an I/O map in the CPU/Multibus adapter. A 1024-entry RAM, the I/O map converts the logical address from a DMA memory reference to the appropriate physical address. The operating system sets up this map before initiating the mass storage transfer. Once set up, contiguous addresses produced by a peripheral are mapped to noncontiguous physical pages.

A private line added in the Multibus P2 connector causes the I/O map to be bypassed when asserted; ordinary Multibus devices do not assert this line. When one CPU uses the Multibus to communicate to another CPU’s memory, mapping is not necessary because the first CPU has already performed a virtual-to-physical translation.

A Multibus protocol defines a busy line, a set of address lines, and a strobe line. The bus also specifies address setup time and address hold time, as well as XACK (slave acknowledges on a read that it put data on the bus, and that it has removed data from the bus on a write). This Multibus protocol carries addresses made on bracket strobes, giving devices time to decode their own assert and deassert addresses. The 68000 has a similar protocol.

Unfortunately, comparing the 68000 timing specification to the Multibus timing specification shows that available address time for the 68000 after completion of its address strobe is not long enough to match the Multibus signal timing pattern. Therefore, to guarantee that 68000 strobes meet the Multibus setup for proper access, system designers have provided an address latch on that patch when the 68000 is bus master performing a read/write over the Multibus.

Finally, designers had to address the deadlock problem in the CPU/Multibus interconnection (ie, the CPU has to request and obtain Multibus time for a reference to memory). This eliminates the benefits of the high speed MC-500 bus. If, however,

**When one CPU uses the Multibus to communicate to another CPU’s memory, mapping is unnecessary.**

the CPU references a location that is not in local memory, the request must be made on the Multibus. If, at the same time, a peripheral also requests and wins the Multibus, a stalemate exists. The peripheral will not give up the Multibus until it receives its handshake from memory. To obtain that handshake, it must use the MC-500 bus to access memory.

Although the CPU could hold the high speed bus while waiting to obtain the Multibus, this condition is avoided by logic, external to the 68010. This causes the CPU to temporarily withdraw its request. The peripheral can then enter its memory cycle to transfer data. Once the transfer is complete, the Multibus is free for access by the CPU. Using external logic rather than the deadlock avoidance mechanism built into the 68010, allows the 68010’s full instruction set to be used. Using the 68010’s deadlock function makes a critical 68010 instruction (the test and set instruction) unavailable in this case, because it does not function appropriately when the chip itself breaks a deadlock.

**Multibus block transfer mode**

The 32-bit block transfer mode on the Multibus follows the MC-500 high speed bus protocol. Mid-cycle, the master flips address line A1 to command the other half of the longword. In a read, the slave senses the A1 flip and switches its data to the other word within the long-word. In a write, the master changes A1 and the write data simultaneously.
We were going to compare Vectrix graphics to IBM’s. Unfortunately, there is no comparison.

 Vectrix VX/XT Graphics

For the demanding professional, it’s not fair to compare Vectrix’s VX/XT color card set with IBM’s own. Our 512 colors (out of a palette of 4,096) vs. their 16. Our beautiful 672 x 480 pixels vs. their not-quite-precise 640 x 200. Plus the logical, easy to use Vectrix command system. There’s really no comparison.

But the IBM PC XT does other things well — like provide a wealth of outstanding software. That’s the reason we made sure the Vectrix VX/XT two-board set runs all the software that runs with IBM’s color card (except in low resolution mode, which even IBM doesn’t support). Options include a Siggraph core library, 4010 emulation package, Plot-10 compatible library and the amazingly versatile Vectrix paint program. Get everything the IBM PC XT has to offer.

Plus incomparably better graphics. The Vectrix VX/XT color card set for the IBM PC XT or the IBM PC with expansion chassis. See for yourself — call us toll-free at 1-800-334-8181. Vectrix Corporation, 2606 Branchwood Dr. Greensboro, NC 27408. Telex 574417.
Sensing the $A_1$ change, the slave obtains the data and does the write.

To differentiate this special mode, the design designates another unused line from the P2 connector as "block mode." An ordinary Multibus device will not select this mode; however, it can be used by a special device such as the DA/CP.

As part of its definition, the Multibus's protocol has a clock edge. While bus exchanges (arbitration determining bus master) happen on clock edges, the clock edge becomes irrelevant during address strobes, $XACK$, and data transfers, which are just asynchronous handshakes.

In block mode, the clock again becomes relevant. The slave must assert $XACK$ on the clock edge. When the master flips $A_1$, it must be on the clock edge, and when the slave swaps the data, it again must be on the clock edge. This reduces the time involved (and wasted) in round-trip handshakes. By following an agreed upon protocol, which occurs on clock edges, the transfer process gains considerable speed.

The burden of flipping $A_1$ always rests on the host. Once $XACK$ is asserted, the master can wait an arbitrary number of cycles before flipping $A_1$; this means that it can accept data at any rate. The burden of handling the second word rests on the slave because there is no handshake on the second part of the transfer. Once $A_1$ flips, the slave must handle the data.

**Multibus/STD+ bus connection**

The large number of data acquisition interfaces available on the STD bus led to the decision to equip the system with a STD bus. While the simplest approach to providing the system with a STD bus would have been to incorporate another bus adapter, this would have required the 68000/68010 CPU to supply all STD device control. Results would have decreased Bell Labs' Unix System III performance when there were high levels of data acquisition activity, and less predictable data acquisition performance. A separate processor avoids these problems and makes the connection between Multibus and STD bus devices.

Making this connection, DA/CP is a programmable, DMA controller based on an 8-MIPS bipolar bit-slice processor, which executes each instruction in 125 ns (Fig 4). The DA/CP also contains 1024 locations of 40-bit storage for the control software, 256 locations of 24-bit temporary data storage, two 16-element first in, first out (FIFO) buffers, and one 64-element FIFO.

These components allow devices connected to the STD+ bus to input or output data to buffers within an application program. Designed as an enhanced industry standard, the STD+ bus combines two, nine-slot STD buses side by side. These buses share address lines, but have separate data paths and read/write control lines.

Most Z80-compatible 8-bit STD boards plug into the STD+ bus; however, the data transfer rate for these devices is limited to a maximum of 1 Mbytes/s. Several STD+ Masscomp interfaces transfer at rates twice as high as those of normal STD boards; therefore, they plug into two slots. Since data transfer happens over two separate byte-wide pathways, the STD+ bus moves data in and out of the system at up to 2 Mbytes/s (see the Panel). When an application program wants to perform realtime data I/O, it makes a request to the interface handlers resident in DA/CP program memory. The DA/CP uses these routines to manipulate the STD+ bus interfaces. Since the DA/CP performs 24-bit arithmetic, it can command simple data reduction and data-dependent realtime decisions.

For example, the DA/CP could acquire 100,000 samples before or after an analog trigger or threshold event.

Priority-interrupt logic in the DA/CP allows it to respond to interrupts generated by up to ten interfaces on the STD+ bus. This simple interrupt structure, added to the DA/CP's fixed instruction duration, makes data acquisition highly stable and predictable.

The DA/CP was designed as a Multibus peripheral. To ensure that Multibus DMA and interrupt latencies do not affect DA/CP performance, all time critical data is passed to and from the Multibus via hardware FIFO registers. The DA/CP is able
metamorphosis
dramatically transforms your designs into high performance ECL/TTL logic arrays.

Like metamorphosis in nature, we're dramatically transforming logic and board designs into semicustom, ECL/TTL logic arrays that stretch the imagination ... that advance the state of the art in military systems, communications, test, instrumentation, computer systems and peripherals.

If you need sub-nanosecond performance ... ECL speeds at LSTTL power ... ECL, TTL, or mixed I/O ... up front design flexibility with engineer-to-engineer support ... full CAD capability and the highest functionality macro library available ... Mil. Spec. 883C ... a source with fully integrated wafer fabrication, assembly and test ... up to 95% utilization with auto place/route ... six to eight week prototype turnaround ... and fast reliable delivery of production quantities ... Call us. Let us prove that we can dramatically convert your designs into high performance logic arrays ... it's what we call AMCC metamorphosis.

Ask about our newest product ... our Q1500 Series with 120 I/Os, 1700 gates, ECL, TTL or mixed I/O, and high functionality macros ... and get data sheets on the other members of our logic array family.

<table>
<thead>
<tr>
<th>AMCC ECL/TTL GATE ARRAYS</th>
<th>Equivalent Gates</th>
<th>Typ. Gate Delay (nS)</th>
<th>Typ. Power (W)</th>
<th>I/Os</th>
<th>Gate Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>QH1500A</td>
<td>1700</td>
<td>.9</td>
<td>2.8</td>
<td>120</td>
<td>95%</td>
</tr>
<tr>
<td>Q1500A</td>
<td>1500</td>
<td>.9</td>
<td>2.5</td>
<td>84</td>
<td>95%</td>
</tr>
<tr>
<td>H700</td>
<td>1000</td>
<td>.9</td>
<td>2.0</td>
<td>76</td>
<td>85%</td>
</tr>
<tr>
<td>Q710</td>
<td>500</td>
<td>.9</td>
<td>1.2</td>
<td>56</td>
<td>85%</td>
</tr>
<tr>
<td>Q720</td>
<td>250</td>
<td>.9</td>
<td>.6</td>
<td>36</td>
<td>85%</td>
</tr>
</tbody>
</table>

Get all the facts:
Call or write for information on our line of logic arrays and our capabilities. Write: Applied Micro Circuits Corporation, 5502 Oberlin Drive, San Diego, California 92121. Telephone: (619) 450-9333. TWX/Telex: 910-337-1136.

Nature's metamorphosis ...
dramatically transforms a caterpillar using its eight pairs of legs to crawl along a leaf ... into an incredible, winged butterfly.

CIRCLE 41
STD+ bus compatibility

Using the STD bus as the basis of the STD+ bus is relatively straightforward. However, several STD+ characteristics require explanation.

For example, the DA/CP does not issue an INTAK* signal in response to interrupts. An interrupt from a STD bus module must be cleared by a read/write operation to a STD address recognized by that module. An interrupt should be cleared on the leading edge of a read/write operation. This allows the interrupt to clear out of the DA/CP interrupt register before the DA/CP code again enables interrupt service.

The most efficient way to handle this is to have the interrupt service action (i.e., a register read operation) clear the interrupt. A status register with an error and a done flag is desirable. The error flag should show when data have been lost because the DA/CP responded too slowly to interrupts. The done flag is the same as the interrupt signal. The DA/CP uses it to distinguish between two modules asserting the same interrupt. A module with more than one interrupt function should have a done bit for each function in the status register.

In addition, the DA/CP does not issue an MCSYNC* signal (sometimes used to synchronize interrupts). A device may assert interrupts asynchronously, or it may use the CLOCK* signal to assert them.

Read/write timings for the STD+ bus are equivalent to those provided by a 4-MHz Z80 processor (see the Fig). But, pins 35, 37, 38, 39, 40, 41, 42, 43, 46, 48, 50, 51, and 52 are not supported. These lines are held at ground. Pins 55 and 56 carry 15V and −15 V, respectively.

STD Address

DA/CP Clock

Address

Memory Request

Read

Write

STD Address

Write

Write

125 ns

STD Address

Write

STDATA

Write

125 ns

DA/CP Clock

Address

Memory Request

Read

Write

STD Address

Write

Write

125 ns

DA/CP Clock

Address

I/O Request

Read

Write

I/O Read/Write

STD Bus Timing

A write request is composed of a 24-bit address, followed by a 16- or 32-bit data word; a read request is a 24-bit address. These requests pass through a 64-bit FIFO to the Multibus interface logic. The 16- or 32-bit data obtained from the MC-500's CPU memory pass through a 16-element FIFO back to the DA/CP. Thus, these FIFOs effectively isolate the DA/CP from the Multibus’s inherent DMA latencies.

The DA/CP can issue Multibus interrupt requests; these are also passed through the 64-element FIFO to synchronize them with read/write requests. However, when they emerge from this FIFO, interrupt requests pass through a second 16-element FIFO. This prevents data transfers from being held back by Multibus interrupt latencies. Data transfers on the Multibus use the special 32-bit block mode gained through the CPU/Multibus adapter.

Design features allow the MC-500 system to acquire analog signals with 12-bit resolution at an aggregate rate of one million samples/s. This can be done with negligible effect on computation and graphics task performance.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 701 Average 702 Low 703
KONTRON Logic Analyzer/Slave Emulator

Your Most Powerful Micro Development Tools Have Been Combined

Now you can have timing and state logic analysis, slave in-circuit emulation, and full software development capability in one powerful, economical system. And, KONTRON's new Logic Analyzer/Slave Emulator (LASER) system can be configured to match your needs. With 32-, 48-, or 64-channel logic analysis to 100 MHz. With built-in dual 5¼” disk drives. With disassemblers, microprocessor interface, and slave emulation for all popular 8- and 16-bit chips. And, with all of the software development tools and ease-of-use features of the KONTRON/FutureData 2300 Series development system at your command, running under CP/M®*. With the flexible LASER system, you can reduce your investment in new development tools by as much as 50 percent. If you already own a 2300 Series system, expand its logic analysis capability with a software-compatible LASER. Or, if you own a KLA Series Logic Analyzer, expand its use by adding an ASCII keyboard, software development tools, and in-circuit emulation. LASER can even be interfaced to Intel, Motorola, HP, Tektronix, or other development systems. Complete your capabilities with one of KONTRON's desktop or portable PROM programmers.

Get all the facts and figures on these synergistic cost-reducing solutions to your hardware/software development/debugging needs. Call our 24-hour toll-free number (800) 227-8834... or drop us a line.

*CP/M is a registered trademark of Digital Research, Inc.
Powerful new computer graphic systems, in the hands of imaginative designers, are changing the world we live in. Automobiles, buildings, bridges and aircraft are just some of the applications for computer-aided engineering.

High resolution raster graphic CAD/CAM systems are the most versatile of these new tools, and Conrac's new Model 7300 is the color monitor designed specifically for those systems. Over 1000 non-interlaced lines of resolution (65 kHz scan rate, 60 Hz refresh) and a pixel rise time of less than 5 nanoseconds, gives you a completely flicker-free display with clarity and realism you've never seen before. Operators will enjoy working comfortably with this monitor all day long. The 7300 has permanent convergence and quiet operation—because it doesn't need a cooling fan.
AVAILABLE TODAY.

Computer graphic systems will soon be as common as typewriters in the business and industrial world. Conrac, the leading name in video monitors for over 37 years, will be a part of those systems. Conrac has sales offices and service centers located in principal cities across the country—with more on the way.

Find out more about the advanced concept new Conrac 7300. Use the Reader Service number or call Marketing Communications at (213) 966-3511.

Contact Conrac Division for a full color reproduction of this illustration which is suitable for framing.

CIRCLE 43
PC Circular Connector

Need to eliminate shock hazards

Require durable, custom-spec, EMI/RFI tested cable

Must be compatible with all IEEE 802 networks

Jack-Jack adaptor required for splices

Need frequency range from 0-11 GHz

Terminate with type N

Need cable-end terminator for system impedance balance

PC Fibre Optic Connector

Plastic D-Subminiature Connector

©1983 Allied Corp
For you, anything.


When it comes to meeting the rigid interconnection requirements of business equipment, there's hardly anything we won't do. Because at Amphenol, we know that the best design is often a custom design.

The data must get through.

Every day your design parameters get tougher. Amphenol’s Design Group has tackled and solved many of the problems you face in data communications interconnection. Our design selection includes an impressive variety of high performance connectors and interconnect systems. In fact, we’ve probably already developed a solution close to what you need.

Mainframes to games. And beyond.

The LANS connector is but one example of our solution capability. There are many more:

To eliminate interface wiring from a PC board to a cabinet mounted connector, we added printed circuit contacts to a standard circular connector. The connector plugs directly into the PC board and has an attractive exterior finish.

For CATV, we developed a modular eight-channel fibre optic connector that mounts directly on a PC board. It takes the place of eight separate optical connectors with less space and complexity—but no loss in performance.

We developed a low-cost, all plastic D-subminiature to meet the need for reliable connections in video games and home computers. The connector, with selectively-plated, pre-aligned and stiffened contacts, snaps easily into a PC board and withstands rugged use.

We designed a computer peripheral interconnect harness using shielded planar four-conductor coax cable. Two additional stress members in the jacketing accommodate 360° rotational stress.

We’ve developed several low-cost solutions to EMI/RFI control in business equipment. We added a full range of filter functions to our industry standard 57 Series ribbon connectors. We coated a plastic backshell with nickel and dimpled the plug shell of a D-subminiature for RS-232C/RS-449 applications. Amphenol can help with Docket 20780.

An energy saving device.

Early involvement with the Amphenol Design Group can save you a lot of engineering energy. Whether your needs call for a standard, modified or fully custom connector design, call Amphenol for the answer. Your solution may be as close as your phone.

Call the Amphenol Design Line
1-800-323-7299

CIRCLE 44

Amphenol Products

An Allied Company

Amphenol Products world headquarters: Oak Brook, IL 60521

Make the Amphenol Connection
NEPCON WEST Booth 2251
Anaheim, CA Feb. 28-Mar. 1

Planar Coax Interconnect Harness
Filtered Ribbon Connectors
Shielded D-Subminiature Connector
They look like anyone else's 12-bit CMOS DACs. But we made them twice as accurate.
Analog's LC²MOS DACs. The first DACs to combine CMOS low power with extraordinary accuracy.

If you want low power dissipation and better accuracy than ever before in a 12-bit monolithic D/A converter, only a DAC built with our exclusive Linear-Compatible CMOS (LC²MOS) technology will do.

Thanks to LC²MOS, our new AD7240 and AD7548 also deliver remarkable improvements in speed, packing density, and board reliability, while significantly reducing device capacitance. And they’re so tightly spec’d that there’s never a need to recalibrate.

Check out the AD7240. With total unadjusted error of 1½ LSB max over temperature, it beats other CMOS DACs by upwards of 500%! And its 18 pins carry an outstanding array of features—single supply operation, high-speed voltage settling (to 0.01% in 550ns), and superb differential nonlinearity.

And our AD7548 is just as extraordinary. The gain error is only 3 LSB max over temperature—twice as precise as the closest competitor! And there are more good things in the AD7548’s small 20-pin package, including 8-bit bus compatibility, guaranteed monotonicity, selectable data format, and both +5V and +12V to +15V supply operation.

So if all CMOS DACs look the same to you, take a closer look at Analog Devices' LC²MOS DACs. For the eye-opening details on the AD7240 and AD7548, just call Steve Miller or Stanley Domanski today at (617) 935-5565. Or write Analog Devices, P.O. Box 280, Norwood, MA 02062.
<table>
<thead>
<tr>
<th>SOFTWARE NOW AVAILABLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. UniFLEX™ Operating System</td>
</tr>
<tr>
<td>2. BASIC</td>
</tr>
<tr>
<td>3. COBOL</td>
</tr>
<tr>
<td>4. FORTRAN</td>
</tr>
<tr>
<td>5. 68000 Relocating Assembler</td>
</tr>
<tr>
<td>6. 68000 Linking Loader</td>
</tr>
<tr>
<td>7. Sort/Merge</td>
</tr>
<tr>
<td>8. Editor</td>
</tr>
<tr>
<td>9. Advanced Spooler</td>
</tr>
<tr>
<td>10. BASIC Precompiler</td>
</tr>
<tr>
<td>11. Floating Point Package</td>
</tr>
<tr>
<td>Scientific Functions Package</td>
</tr>
<tr>
<td>12. Utilities</td>
</tr>
</tbody>
</table>

UNIX is a trademark of Bell Laboratories. UniFLEX and The Masterminds of Advanced Systems Software are trademarks of Technical Systems Consultants, Inc.
How Vocabulary Is Generated Determines Speech Quality

Synthetic speech vocabulary can be generated by analyzing natural speech or by artificial construction from phonetic parts, with differing results.

By Michael W. Hutchins and Lee Dusek

Computer games and even appliances can easily add speech output with low cost speech synthesizer chips. Without a vocabulary, however, chips are mute. Words, phrases, and sentences in the vocabulary must be clearly understood, and if required, the sound should be natural and pleasant, not mechanically monotonic.

A vocabulary can be assembled from written text by means of artificial phonetic approximations, or from real speech (Fig 1). For large vocabularies exceeding several hundred words, artificial constructive/synthesis word and phrase generation appears attractive because vocabulary size in a given language is virtually limitless. However, its artificial source in phonetic speech parts—like sets of phonemes and allophones—makes it difficult to get an understandable, natural sound.

Real speech as a vocabulary source generally produces the highest quality results and, at least for small vocabularies, the lowest cost system. This approach involves collecting words, phrases, and sentences from speakers having the desired voice characteristics; converting this analog data to digital form; analyzing the speech content into spectral coefficients; and encoding these components into a suitable format, such as linear predictive coding (LPC) for storage in a ROM (Fig 2).

Because the analysis/synthesis method derives its vocabulary from actual human speech, the final speech synthesizing resembles real speech more closely in inflection, emotion, and intelligibility. Conversely, speech synthesized by the constructive/synthesis method—piecemeal approximations from text—generally sounds less natural. With this artificial approach, sound variations that depend on an utterance’s context (ie, what sounds precede and follow it, and where within the word, phrase, or sentence the utterance appears) are difficult to generate accurately.

Using spectral coefficients

Whether the natural speech analysis/synthesis or the artificial constructive/synthesis method is used, spectral coefficients are involved. Entire words or phrases in most current synthetic speech systems are analyzed into spectral components in the former case, or built up from selected component sets in the latter case.

Constructive synthesis can be based on phonemes, diphones, demisyllables, or morphs. Of these, phonemes are usually employed in modern speech synthesis. Phonemes emphasize an alphabet-like simplicity. Accordingly, American English can be created from just 40 to 50 (of about 90 total) phonemes. This is accomplished by following an appropriate set of rules requiring a minimal amount of memory storage space.

Michael W. Hutchins is product engineer for the Speech Products Dept, at Texas Instruments, PO Box 1443, MS 6418, Houston, TX 77099. Mr Hutchins received his BS in biology and BA in psychology from the University of California at Irvine.

Lee Dusek is substrategy manager for the Speech Products Dept at Texas Instruments, Houston. She has been involved with the use of speech processing algorithms on minicomputer and microprocessor-based systems. Ms Dusek holds a BS in math from Longwood College and an MS in Math and an MSISE from Ohio State University.
Phonemes include speech characteristics like voicing and manner. Any voiced sound, including a voiced phoneme, is produced with vibrating vocal cords. In English, voiced phonemes include all the vowels and 11 consonants. Eight other consonants produce unvoiced phonemes. Articulation depends on the way sounds are modulated by the lips, tongue, and teeth: full closure produces a stop, or plosive sound or phoneme; partial closure produces a fricative.

**Allophones needed**

Phonemes alone are not enough to characterize speech so that reconstituted synthetic speech can be made to sound nearly natural.

In constructive synthesis, deciding which collection of speech components to use requires a closer look at speech sounds. There may be hundreds of minor variations between sounds that are categorized roughly as the same. For example, the /P/ sound in “pin” is aspirated, that is, followed by a puff of air. The /P/ sound in “spin” is not aspirated. Sounds that are slightly different but generally perceived as the same are the phonemes of a language. Subsets of phonemes that change slightly depending on the context or environment in which the sounds appear are called allophones. Thus, the unaspirated /P/ sound in “spin” and the aspirated /P/ sound of “pin” are different allophones of the same phoneme, /P/, and represent the sound more accurately than the phoneme. In order to preserve this linguistic accuracy, the TI text-to-speech system uses allophone stringing to form words and phrases.

Allophones are more fundamental than most other linguistic components, except morphs. About 130 allophonic sound characteristics can provide the needed variations for all the phonemes.
How to avoid Capitol Punishment.

Now there's a code of silence in Washington. It's called FCC Docket 20780. And the Cannon® Shielded/Shrouded D Series of subminiature connectors helps manufacturers meet all its stringent EMI/RFI requirements, while helping to maintain the integrity of the entire shielded system.

Our shield is crimped to the cable to maximize shielding effectiveness and provide a low-impedance path to the ground. The shroud/plastic backshell protects the equipment from ESD (Electro Static Discharge) and isolates the user from ground potentials that may exist on the shield. Plastic strain-relief members are provided to prevent cable pullout. The center-latched version is available in configurations of 9, 15, 25 and 37 contacts.

Cannon's quality D Subminiature Transverse Monolith Filter connectors reduce EMI/RFI noise. The addition of the transverse monolith filter expands the overall shielding versatility of the D Subminiature without adding to the overall dimensions of the connectors.

And these Cannon connectors are available in contact arrangements of 9, 15, 25 and 37, with a wide range of capacitances and cutoff frequencies offered.

The Shielded/Shrouded D and Transverse Monolith Filter Series connectors from ITT Cannon. The best way to give FCC Docket 20780 the silent treatment.

For more information on Transverse Monolith Filter Connectors, contact Phoenix Division, ITT Cannon, 2801 Air Lane, Phoenix, AZ 85034. Telephone: (602) 275-4792.

Or for more information on the D Subminiature Shielded/Shrouded D Series, contact Commercial/Industrial products, ITT Cannon, a Division of ITT Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. Telephone: (714) 964-7400. For the local sales office nearest you, call toll-free: (800) 845-7000.

CANNON ITT
The Global Connection
Consequently, in order to preserve linguistic accuracy, Texas Instruments’ text-to-speech system utilizes allophone stringing to form the words and phrases.

Allophones provide many of the subtle variations each English phoneme can encompass, and allophone rules can select each variation in an appropriate relationship to the utterance’s context. Although much better than a pure phonemic approach, the allophonic help is not perfect. Some speech systems, such as Lingua and Mitalk, use a more complex morph approach for still higher quality speech.

However, there are drawbacks to a morph system. While a good quality set of 128 allophones (set sizes can range from 80 to 500) can be stored with its 650 rules in less than 10 Kbytes of memory, a typical high quality morph system needs about 600 Kbytes of memory for at least 12,000 of its speech parts. Even with a relatively small number of allophones, most of the stress and intonation, rising and falling inflections, and other speech patterns that convey much of the information when speaking, can still be handled effectively. The speech, however, is still somewhat unnatural.

In a great many applications, this is not a serious problem. For more natural speech, perhaps for a different use, an allophone set can be tailored to that application. Speech can be used in many different places. For example, an automated banking facility must use a clear and pleasant sounding voice, while the owner of a video game arcade may prefer a distorted mechanical sounding voice. Each, accordingly, would be best served by a different set.

Although not perfect, the allophone approach is still a good compromise among many factors. These include vocabulary size, memory storage requirements, versatility and flexibility, hardware and software complexity, cost, and quality.

An allophonic system lends itself to translation from American English text with a reasonably-sized set of rules. Input text from an ASCII keyboard can be automatically converted into allophones. TI’s text-to-allophone rules are an enhanced version of work done at the U.S. Naval Research Laboratory. For instance, rules have been added to the basic navy list to ensure that word-ending allophones properly terminate appropriate words. Longer words stress the monosyllables before voiced consonants, and unstressed vowels are used before suffixes such as “er,” “ely,” and “es” (after t and d).

The resulting rules can then string allophones that are 97 percent correct on only one pass for the 2000 most common American English words. (Accuracy, however, drops to about 92 percent when word usage frequency is measured.)

**LPC forms the basis**

Whether words to be synthetically spoken are from text or from natural speech, these words must be coded for use with a digital speech synthesizer chip. LPC is a particularly effective form of compressed speech digital data. While all the allophones and essential rules needed to construct 200 words use only 10 Kbytes of memory, the equivalent custom vocabulary would require 16 Kbytes of memory. Moreover, the system data rate must be a higher 1200 bits/s than the allophonic 400 to 600 bits/s to convey speech at a real-time rate.

The speech synthesizer chip, driven by LPC speech data, is essentially an electronic, digital signal processor model of the human vocal tract [Fig 3(a)]. The p-channel MOS (PMOS) device consists of a 10-stage time-varying digital lattice filter...
WHAT MAKES OUR 32 BIT WORKSTATION DIFFERENT?

- 16032 microprocessor
- Demand paged virtual memory
- Hardware floating point
- Industry standard 32 bit VMEbus

If you're looking for the power of a VAX™ at the price of a 68000, our Consultant is the system for you. It is the first microcomputer with the power to run mainframe programs.

The PVS™ operating system has all the popular features of UNIX™ plus real time capabilities, record locking and dynamically installable device drivers. Fortran 77, Pascal and C are available.

For less than $18,000 (qty. one), the Consultant includes 512K memory, high resolution (768 x 624) B&W graphics and a 10 megabyte cartridge disk drive. Memory is expandable to 3 megabytes and disk storage to 70 megabytes within the desktop enclosure.

Always one step ahead of your needs, the Consultant will have the 32032, color graphics, multi-processor capability and more languages later this year.
and associated control logic [Fig 3(b)]. Its source is an internal digital excitation function when producing voiced sounds, and a digital white-noise generator when delivering unvoiced sounds. Because the synthesizer has 10 stages, the vocal tract parameters, or LPC data supplied to it, are designated LPC-10.

Voiced sounds are coded for energy levels and pitch and for 10 so-called filter reflection coefficients (K1 through KPV10), according to Table 1. Together, the chip receives 247 levels of data coded with 49 bits (plus an extra bit for a repeat operation) for each 25 ms of operation, called a frame.

The synthesized speech output consists of 10 bits output every 125 µs and are converted to an analog signal of up to 1.5 mA (with a resolution of 5.9 µA). This is more than sufficient to drive a power audio amplifier. The 7 low order bits determine the magnitude of the analog output level. The MSB of the 10-bit word is the sign bit, which, when combined with the next two bits, is used to force the output driver to full on or full off.

Although the LPC-10 parameter input to the synthesizer needs 50 bits to describe them, the commands to the synthesizer are minimal—just six operational commands make up the total (Table 2). Thus, a synthesizer chip needs minimal control from a host processor (typically less than 1 percent). The host passes commands only to initiate specific activities and does not involve itself in carrying out the speech producing activity. Thus, the host selects data for the desired word, phrase, or sentence by locating its starting address; passes a command, such as speak external; and sends the required data from memory.

**Synthesizer chip handles both speech sources**

Both the constructive/synthesis method of stringing allophones together from a library by given rules, and the analysis/synthesis method of analyzing natural speech, end up in LPC-10 form. For this reason, the TMS5220C synthesizer chip can work with data derived from either source. However, when derived from a natural source, with a relatively low cost development system, the user has more complete control over speaker, dialect, inflection, and other speech characteristics, including language. Moreover, it is even possible for sound effects to be analyzed and synthesized from natural sources.

Analysis/synthesis is language independent; constructive/synthesis is not. The latter requires a completely different set of allophones and rules for each language or even for each dialect. Dialect is a complicating factor in reproducing speech sounds from the multilingual areas of Europe and Asia. This may be overcome, however, by using a common multilingual subset of allophones with only the language-specific allophones added to reduce total memory requirements.

To help in applying the analysis/synthesis approach, TI’s Dallas speech laboratory has recorded speakers so that potential users can make selections. Then a selected person can be brought in to record the actual words wanted, or customers can bring in their own speakers, or previously recorded speech. In either case, TI can make an analysis and provide the results in LPC-10 on almost any memory device or combination of devices.

Unless customers want to develop their own inhouse capabilities, analysis/synthesis allows easy access to an outside agency. Working together, customer personnel and TI speech analysis experts can often reduce vocabulary size substantially by using generic words. Such words cover a variety of situations, yet are specific enough when combined to avoid ambiguity. In this way, storage requirements can be minimized in the final system, and many phrases and sentences can often be strung together with selections from these words. This is especially true where the quality of emotion and intonation are not important, as in a learning aid such as TI Speak-and-Spell.

### TABLE 1

**Parameter Coding**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Levels</th>
<th>Code bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy</td>
<td>15 *</td>
<td>4</td>
</tr>
<tr>
<td>pitch</td>
<td>64</td>
<td>6</td>
</tr>
<tr>
<td>K1</td>
<td>32</td>
<td>5</td>
</tr>
<tr>
<td>K2</td>
<td>32</td>
<td>5</td>
</tr>
<tr>
<td>K3</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>K4</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>K5</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>K6</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>K7</td>
<td>16</td>
<td>4</td>
</tr>
<tr>
<td>K8</td>
<td>8</td>
<td>3</td>
</tr>
<tr>
<td>K9</td>
<td>8</td>
<td>3</td>
</tr>
<tr>
<td>K10</td>
<td>8</td>
<td>3</td>
</tr>
</tbody>
</table>

*Energy = 1111 is the stop code

### TABLE 2

**Synthesizer Commands**

<table>
<thead>
<tr>
<th>Data Bus Command Code (D0-D7)*</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>X000XXXX</td>
<td>NOP (No operation)</td>
</tr>
<tr>
<td>X001XXXX</td>
<td>Read byte</td>
</tr>
<tr>
<td>X010XXXX</td>
<td>NOP (No operation)</td>
</tr>
<tr>
<td>X110XXXX</td>
<td>Speak external</td>
</tr>
<tr>
<td>X011XXXX</td>
<td>Read and branch</td>
</tr>
<tr>
<td>X100AAAA</td>
<td>Load address</td>
</tr>
<tr>
<td>X101XXXX</td>
<td>Speak</td>
</tr>
<tr>
<td>X111XXXX</td>
<td>Reset</td>
</tr>
</tbody>
</table>

*A = Address
X = Don’t care
WE SOLVE PROBLEMS!

Meet some of our new problem solvers.

High performance, innovative design data displays in 5", 7", 9", 12", 15" and 5" x 9" screen sizes, for system designers like you. And they're all available in integrated (neck-mounted), chassis or kit versions.

Using these basic displays, our engineers become your engineers! They custom design a display for your specific application, meeting your particular system design requirements.

Scanning frequencies to 32 KHz and more. Up to 1200 line resolution. TTL or composite video. 120 or 240V AC, or 12 or 24V DC. Give us your specifications and we'll solve all your display problems. And we'll deliver on time, when you want them.

Audiotronics has been solving problems for over 25 years, designing hundreds of custom data displays for important customers, large and small. Call today. Turn our engineers loose with your display system problems.

North Hollywood
California 91605
(213) 781-6700
In another similar but more complex application, TI programmed a huge Mandarin alphabet keyboard with about 1260 characters on it to echo back individual words and other text characters as they were entered. Even for English, checking keyed-in material by listening to words fed back on earphones would be a great aid in reducing errors. A selection of just 500 of the most common words could be quite adequate for most such applications.

With the TMS5220C synthesizer chip and a custom ROM (one, for instance, made up of several TMS6100 voice synthesis 128-K x 1 ROMs), ROM addressing can be handled automatically without involving the host processor except to provide the synthesizer with a starting address (Fig 4). Until the utterance is completed, the processor is not involved except for possibly checking the synthesizer's status register. This behavior is similar to a built-in DMA system.

The TMS5220C has an onchip 16-byte first in, first out (FIFO) buffer that can hold two full frames of speech (about 50 ms when operated at a nominal system-clock of 160 kHz). When the FIFO's contents fall to less than 8 bytes, the synthesizer can generate an interrupt or set a polling level for the host computer to indicate that more data is needed.

For a vocabulary of several thousand words, a single TMS5220C synthesizer chip can access up to 16 TMS6100 ROMS to provide approximately 30 minutes of continuous speech without repeating any of the stored words.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 704 Average 705 Low 706
Extraordinary is the best word we could find to describe the new Epson family of 3½" and 5¼" floppy disk drives. Because there is nothing ordinary about them.

The 3½" drives, for instance, feature two-sided capacities up to 1MB. And some draw so little power they can operate on batteries.

The half-height 5¼" drives offer capacities from 500KB to 1.6MB and access times down to 3 msec. And the one-third height 5¼" drive is the industry's slimmest.

But that's only part of the story. What really makes them extraordinary is the fact that they're Epson drives. Designed and built by the people who have made "quality in quantity" their trademark around the world.

That means they're designed and engineered with such state-of-the-art features as noise and RF shielding, ultra-high precision head positioning and loading, perfect disk centering, reduced power consumption and heat generation. But, even more importantly, it means they're manufactured by the people who have established the lowest rejection rate in the industry. When you buy Epson, you buy confidence.

If you'd like more information about the extraordinary Epson family of floppy drives and how they can solve your storage problems, write or call us today.

SW Region (714) 250-0111 • NW Region (408) 985-8828
SE Region (404) 458-9666 • NE Region (617) 245-6007
CENTRAL Region (815) 338-5610

CIRCLE 51
Motorola presents the without the price that
A computer to develop a computer.

We designed it that way, using the most powerful MPU yet devised, the MC68010. Plus, the most advanced VMEsystem architecture and optimized modular structures and support. The result is the most versatile, most flexible, multi-purpose microcomputer personality you can integrate into your life.

If you’re an OEM wanting a complete hardware/software development station, VME/10 exceeds demands of the target system itself.

If you’re a system integrator, it’s a front-end processor for large scientific, engineering, lab and industrial needs.

If you need a complete micro “engine,” VME/10 easily converts to dedicated, turnkey applications.

In a world of colorless compromise and concession, VME/10 is the new benchmark in the crowd. At a price that’s nearly PC-competitive.

VME/10 can be its own target.

VME/10 can be all or part of the same system it helped design … and where other micros are optimized for one specific end use, VME/10 is configurable to your function, with slots for up to nine additional modules for custom-tailoring.

And you’ll find VME/10 virtually obsolescence-proof.

Complete Software Support

Drawing on VMEmodules™ and I/Omodules™ for instant, functional implementation, its eminence and stature is ensured through IEEE P1014/VMEbus standardization and growing vendor support. Over 60 vendors offer VMEbus-compatible products.

VMEbus. A global success.

VMEbus architecture is thoroughly documented, widely adopted and recognized as an emerging international 8-to-32-bit standard. You can enhance it even more with the I/O Channel which increases the speed of multiprocessor systems by relieving VMEbus from servicing local peripherals … significantly valuable in I/O-intensive systems.

Mainframe memory & management.

The new, powerful MC68010 keyboard with 16 user-programmable keys, numerical keypad and all the ergonomics.

Top support. Bottom line.

From initial technical orientation and seminars to our toll-free service hotline, you’ll get total VME/10 answers and support. We are committed to regular software updating, on-site installation and repair, third-party support and comprehensive documentation.

The bottom line says it all. Because you can acquire VME/10 WITH DEVELOPMENT SOFTWARE FOR LESS THAN $10,000 … not much more than some personals trying to be professionals.

Write Motorola Semiconductor Products, Inc. P.O. Box 20912. Phoenix, AZ 85036.

MOTOROLA INC.

TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

Please send me more VME/10™ information.

165CD020084

Name __________________________
Title _________________________
Call me: ( ) __________________
Company ______________________
Address _______________________
City __________________________ State ______ ZIP ________
Introducing the K105. No other logic analyzer is so easy to use.

Logic analyzers have always been a bit complicated. Perhaps even intimidating to the occasional user. No more.

When you sit down at our new K105 logic analyzer, the first thing you'll notice is that big, friendly red HELP button. Press it. You'll begin to feel better immediately.

You see, we wrote the book on logic analyzers. And now the book is in the machine. So when you press the button, you display easy-to-understand, step-by-step operating instructions right across the bottom of the screen. While the data from the operation you're performing remains on the screen.

And if you're still in trouble, just press again. The HELP button and an adjacent SHIFT button call up a HELP MENU and 28 pages of detailed instructions on every analyzer function.

We'll say it again. No other logic analyzer is so easy to use.

Modular design accommodates application changes.

The K105 isn't just easy to use. It's accommodating, too. By simply swapping boards, you can configure several different logic analyzers.

For instance, you can select up to 64 20 MHz channels in 32-channel increments for microprocessor analysis. Up to 16 100 MHz channels in 8-channel increments for hardware analysis. Or combine them to a maximum of 72 channels for software/hardware integration tasks.

And there's more. You can add a dual 5 1/4" floppy disk drive (IBM CP/M 86™ compatible) to store up to 70 setups or data files. While providing data portability and post-processing capabilities.

Disassemblers and Trace Control™ speed software debugging.

It's a lot easier to debug software when you can get your system's microprocessor to speak assembly language mnemonics rather than object code. And our disassembly modules for the 68000, 8086, 8088, 8080, 8085A and Z80®B do just that.

And with the K105's 8 levels of Trace Control at 20 MHz, you can isolate and capture widely-separated slices of program flow to pinpoint failure causes...in a fraction of the time it would take with a conventional triggering scheme.

Two-analyzers-in-one enhances software/hardware integration.

When you're integrating hardware and software, the K105 is two analyzers in one. Just combine the 20 MHz and 100 MHz options to look at both state and timing. For trouble-shooting multi-processor systems, you can even monitor both processors and capture the asynchronous data between the two.

And the K105 offers a fast 5 ns glitch capture capability to pinpoint hard-to-find random problems.

Plus high-speed sampling for hardware analysis.

For high-speed sampling, you can configure the K105 with up to 16 100 MHz...
channels. Our unique automatic noise margin analysis feature enables you to verify specified system thresholds on as many as 16 channels simultaneously.

And design verification is simplified by a "don't care memory" that allows you to selectively mask out memory portions so you can compare only those portions you want to see.

**Uncompromising dedication to high performance.**

The Gould philosophy dictates that every instrument we make be the best for the job it's designed to do.

The K105, with its unsurpassed ease-of-operation and modular flexibility to perform a wide range of analysis tasks, is evidence of that dedication.

For detailed application notes or a demonstration, write Gould, Inc., Design & Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050-1279.

For fastest response, call toll-free: Nationwide (800) 538-9320; In California (800) 662-9231 or (408) 988-6800.

The K105 offers you two levels of HELP at the press of a button. The first displays step-by-step operating instructions across the bottom of the analyzer screen. The second brings a menu to the screen, allowing you to select more detailed help from an integral 28-page manual.

Clearly the Best.
INTRODUCING THE BEST THING NEXT TO THE TOWER.

Introducing Tower™ Annex.
It's a mass storage add-on that transforms the original Tower into the even more powerful Tower Complex. With up to 228MB. Plus streaming tape.

Now Tower 1632 by itself has always been a formidable rival for the minicomputer. With as much as 2MB of ECC memory. Plenty of mass storage. Industry standard flexibility.

Our operating system derived from UNIX* for maximum portability. And full communications capability for both peer level and host networking.

So if you’re a minicomputer OEM, the Tower Complex may really have you worried. But we have the answer to your problem.

Instead of losing out as our competitor, why not become a winner again—by becoming a Tower OEM? Towers and Tower Complexes are substituting for minicomputers everywhere else—why not in your product line as well?

You’ll have better performance, reliability and profits. Because nothing stands up to Tower 1632. Except Tower Annex. Call us at 1-800-222-1235 to learn more.

BUILT FOR SYSTEMS BUILDERS.
TOWER 1632.


*UNIX is a trademark of Bell Laboratories.
SUPER SIX, THE FIRST 6MHz S-100 SINGLE BOARD COMPUTER TO SUPPORT BANKED CP/M™ 3.0

SUPER SIX FEATURES:

- 128 KB of Bank — selectable RAM
- 6 MHz, Z-80B CPU
- DMA Controller
- 6 MHz, Z-80B DART (2 Serial RS-232 Ports)
- 6 MHz, Z-80B PIO (2 Parallel Ports)
- 6 MHz, Z-80B CTC (Clock Timer)
- Double/Single Density Floppy Disk Controller — Supports 8" and 5-1/4"
  Drives Simultaneously
- 2/4 KB of Monitor EPROM
- S-100, IEEE 696 Compatible

SUPER SIX & CP/M™ 3.0 A PERFECT MATCH

Advanced Digital has found the perfect match to its powerful, high-speed SUPER SIX single board computer. It’s Digital Research’s new CP/M 3.0. Because of SUPER SIX’s 128 KB of RAM, it is the only S-100 board to support CP/M 3.0 in the banked mode; or run CP/M 2.2 with 64 KB of extra buffer.

SUPER SIX & TurboDOS™ ANOTHER PERFECT MATCH

When you combine the TurboDOS multi-user operating system with the 6 MHz SUPER SIX, you’ll find your system running 1-1/2 times faster than

before. Add the 4 MHz or 6 MHz SUPER SLAVE™ processor board(s) and you will have the fastest multi-user, multi-processor system available today.

See the SUPER SIX at your quality computer dealer or contact:

ADVANCED DIGITAL CORPORATION
5432 Production Dr., Huntington Beach, CA 92649
Phone: (714) 891-4004
Telex: 678401 TAB IRIN
ARRAY PROCESSOR ACHIEVES 100 MFLOPS

Parallel architecture and fast hardware team up with a resident operating system to speed data flow and minimize host communication.

by Robert Hausman and Phil Cannon

Until recently, a gap of roughly an order of magnitude has existed between the computation rate of supercomputers (e.g., the CDC Cyber 205 and the Cray machines) and that of the fastest array processors. An affordable machine that approaches the speed of today's supercomputers is needed to solve the increasingly complex problems in seismic exploration, image processing, simulation, and signal processing. Computation requirements in seismic exploration, for example, have progressed from those involving two-dimensional arrays to three-dimensional ones. To obtain results in an acceptable time, throughput must be much faster than what existing mid-sized array processors provide, and at costs below the several million dollar price tags of supercomputers.

With a 100-mega floating point operation per second (MFLOPS) maximum internal computation rate, the ST-100 array processor addresses this need by combining fast parallel processors, a large onboard memory, and parallel programming techniques. The array processor's design incorporates several hardware improvements. An 8-Mword main memory allows block transfer of large scale computation routines (processes) from host to array processor together with the large data arrays that will undergo operation. A multichannel I/O subsystem provides high speed communication with the host computer and with dedicated peripherals. A separate parallel processor controls internal movement of data. All parallel hardware elements operate in time-overlapped fashion under direction of a control processor.

The large scale computation routines are written in a higher level array processor control language. This allows the user to develop processes for execution on the array using a Fortran-like language. Another significant innovation relative to conventional array processors is an operating system that coordinates simultaneous execution of various programming levels on the parallel hardware elements.

This combination of hardware and software results in computation speed rivaling that of multimillion
dollar supercomputers. Parallel support hardware and multilevel programming permit attainment of a high percentage of the arithmetic unit's 100-MFLOPS maximum.

Like other array processors, the ST-100 operates in conjunction with a host mini or mainframe computer and attaches physically to the host like any other peripheral device (Fig 1). Note, however, that this array processor can be shared by more than one host and that it can have its own peripheral devices.

Logically, the array processor acts as an extension of the host processor, executing computation-intensive application routines called processes. Properly speaking, three levels of application software execute on the host/ST-100 system. At the top is a host Fortran application program. This program calls large scale computation processes running on the ST-100 which in turn call macros (i.e., assembly language arithmetic or data movement routines).

Parallel hardware speeds throughput

The block diagram in Fig 2 shows the major additions that differentiate the ST-100 hardware from that of mid-sized array processors. The components inside the dotted line represent a large array processor. The speed of the floating point arithmetic unit with its five parallel computation elements is up to eight times that of the fastest predecessors. All blocks outside of the dotted line have been added to aid data flow. To better illustrate the interrelation of the major hardware elements, the ST-100 block diagram is repeated in Fig 3, emphasizing data and control flows.

The I/O subsystem block consists of as many as eight parallel I/O processors, seven device interface adapters, and a DMA channel. Through this block flows all data and control communication between the array processor and the outside world.

One of the parallel I/O processors is dedicated to internal system control while the others are connected through interface adapters to host computers or to array processor peripherals. The interface adapters match the hardware characteristics of the external devices to those of the array processor. Each I/O processor is capable of operating at rates up to 12.5 Mbytes/s with a maximum multiplexed channel rate of 25 Mbytes/s to/from the main memory. The DMA channel can transfer data at rates up to 100 Mbytes/s.

The control processor (CP) has been added to the conventional array processor architecture to coordinate the many parallel elements of the ST-100. To do this, it uses its own operating system, the array processor monitor (APM). This operating system runs on the CP and supervises the execution of application programs in the various elements. The application processes execute on the CP.

All activities of the ST-100 are scheduled by the CP. It initiates and synchronizes program loading and execution for all of the ST-100's other processors. Hardware design permits the queuing of commands to both the storage move processor (SMP) and arithmetic control processor (ACP) so that their functions can be both synchronized and time overlapped.

The CP is built using two Motorola 68000 microprocessors, clocked at 80 ns. They share a 192-Kbyte memory with each processor also having a nonshared 32-Kbyte memory. Cycle time for the memory is 120 ns. One of the microprocessors executes the APM operating system and controls the I/O subsystem, the maintenance terminal, dead start, and the other microprocessor. The second microprocessor executes array processor application processes. To accomplish this, it communicates with the main memory, the SMP, and the ACP.

A large main memory (up to 8 million 32-bit words) allows complete application processes to be transferred from the host to the array processor as single blocks. In previous designs, such a task would have been broken down into multiple transfers of smaller computation routines. In addition, return of intermediate results would have been necessary, all with attendant host overhead. Memory size also permits storing of multiple application processes for sequential execution. The marked reduction in time-consuming host/array processor communication enhances computation throughput substantially.

Three 32-bit wide main memory ports are assigned respectively to the data I/O channels, a DMA channel, and the data cache. The data I/O port operates at 25 Mbytes/s, while the DMA and data cache ports operate at 100 Mbytes/s. The eight-way
DIGI-PAD® WORKS WHERE YOU WORK

DIGI-PAD digitizer tablets perform in the real world. They won't quit over spilled coffee! They are unaffected by dirt, graphite, moisture, or perspiration on the tablet. And DIGI-PADS are insensitive to acoustic noise, magnets, vibration, or pressure. In fact, DIGI-PADS will work in almost any environment you will. That's because they use our reliable absolute electromagnetic sensing technology. And GTCO is the largest producer of digitizers using electromagnetic technology.

Most other digitizers are not as tolerant as a DIGI-PAD. So make sure that the digitizer you choose won't fail or require adjustments because of heavy use or environmental factors.

DIGI-PADS are designed for years of silent, maintenance free operation. You will find the DIGI-PAD comfortable to work with because the stylus generates no heat or acoustic noise. And there's no need for special handling of magnetic storage media because GTCO digitizers will not erase floppy diskettes.

DIGI-PADS are available in sizes from 6" x 6" to 42" x 60", all using the same patented electromagnetic technology. They have been field proven in military, industrial, technical, business, and educational environments. DIGI-PAD is compatible with nearly all computers, from PC to mainframe. Most models are in stock for quick delivery and all comply with pertinent EMI and safety standards.

Choose a digitizer tablet that's willing to work where you work. Choose DIGI-PAD from GTCO (pronounced Gee Tee Co). Call one of our digitizer specialists today at (301) 279-9550.

GTCO Corporation
1055 First Street, Rockville, Md 20850
(301) 279-9550 Telex 898471
interleaving of 320-ns access time memory devices allows a complete 32-bit word transfer every 40 ns. An extra 7 bits per word provide single-error correction and double-error detection.

The data cache provides fast access working memory for the floating point arithmetic unit. It consists of three physical noninterleaved banks each containing 16 Kwords of 32-bits each. Each bank has address space available to allow expansion to 65 Kwords per bank. The CP can divide each bank into two logical sections and assign any of the six possible logical sections to either the SMP or the ACP. Three accesses to the cache memory by the ACP and one by the SMP can be made in every 40-ns machine cycle.

**Parallel processing advances execution**

The SMP executes macros loaded into it by the CP. These macros control data movement between ST-100 main memory and the data cache. The SMP can perform complex address generation for both memories as well as on-the-fly data format conversion between them. Since it operates in parallel with the other processors, data movement can be time overlapped with floating point computation and control program execution. Upon completion of its assigned task, the SMP issues an interrupt to the CP.

An 80-bit wide control word allows the three ALUs within the SMP to run in parallel. A 32-bit ALU performs 32-bit main memory address generation and can also perform auxiliary 32-bit integer computation. A 16-bit ALU can address any of three data cache banks as well as control bank selection. A second 16-bit ALU provides loop control for the two address generation ALUs. The SMP also controls conversion between the various data formats that may be stored in main memory and the ST-100's internal formats (i.e., two's complement 32-bit integer and 32-bit floating point). A three-stage, pipelined conversion unit reformats data during transfers between main memory and the data cache.

The arithmetic section controls and executes the application computations on array data. It contains two parts: an ACP and a floating point computation subsystem. The ACP is a microprogrammed device, which contains three ALUs that generate addresses to and from the data cache plus a fourth for loop control. It has its own 4-Kword x 128-bit micro instruction memory; address space permits an increase to 16 Kwords. The 128-bit wide control word permits parallel performance of four integer ALU operations, four floating point arithmetic operations, one test-and-branch operation, and three memory references during each 40-ns clock cycle. The ACP also controls a crossbar switch between the data cache and the floating point computation subsystem. This switch enables a process or other macro to treat the three banks in the data cache as logical rather than physical banks so that they can be assigned to the three address generators in any order.

Thus, the ACP can move data logically about in the cache for different calculations without time-consuming physical movement. Within the floating point computation subsystem, a data interchange
How the Plastics Fanatics lower the ceiling on housing costs.

When tight deadlines and tighter profit margins put the pinch on you and your electronic enclosure costs, no one can help ease the squeeze quite like an American Hoechst service technician. Here's why.

First, he's part of an experienced team of specialists that has worked closely with the electronics industry in developing a total family of American Hoechst V-O polystyrenes to solve a wide range of enclosure design and processing problems.

He also knows what it takes to fill your complete needs when it comes to modified, high impact polystyrenes that will give you the durability, heat and creep resistance, color stability and finish characteristics you need—without costly overengineering! He's familiar, too, with all the ins and outs of agency classifications including U.L., IEC, CSA, VDE and others.

Why not give the American Hoechst Plastics Fanatics an opportunity to show you what they can do to help bring your electronic enclosure in on target in terms of time, costs and performance. Circle the reader service number and we'll mail you our free V-O polystyrene brochure and a special design evaluation form. American Hoechst, 289 North Main Street, Leominster, MA 01453.

We're the Plastics Fanatics.

American Hoechst Corporation

HDPE/Polystyrene/EPS/UHMW Polymer

Hoechst

CIRCLE 57
unit maintains an orderly flow of operands between the data cache and the parallel arithmetic elements. It universally distributes the operands between the individual arithmetic elements without having to return intermediate results to the data cache.

Two adders, two multipliers, and a divide/square root unit comprise the floating point computation elements. The adders and multipliers are three-step pipelines executing at 25-MHz (40-ns) clock rates. The divide/square root unit requires 13 clock periods for a complete calculation. With the four adders and multipliers in operation, the arithmetic unit’s computation rate is 100 MFLOPS.

### Processes reduce communication overhead

Three distinct levels of application software execute on the host/ST-100 system. The top level is the user’s Fortran application program, which executes on the host. For traditional array processors, this application program would call array processor computation routines (e.g., vector arithmetic, matrix operations, transforms, and filters). Such an approach requires time-consuming host/array processor communication at the beginning and end of each individual computation. While such communication overhead may be tolerable in an intermediate speed array processor, it would severely degrade potential throughput in a machine with an arithmetic unit capable of 100 MFLOPS for certain types of algorithms.

To overcome the communication bottleneck, the ST-100 has added an intermediate application software level called a process. A process can be thought of as a very large application routine which can be called by the host Fortran application program. It encompasses many computation subroutines to accomplish a sizable portion of a total application program (e.g., a three-dimensional migration in a seismic exploration program).

A process consists of general purpose control code that executes on the ST-100 control processor plus specialized instructions (macros) for execution on the SMP and ACP. Multiple processes and their associated data can be stored in the array processor’s large main memory and executed sequentially as shown in Fig 4.

Other major blocks of ST-100 software are production (executive) software, which is discussed separately below, and maintenance software. Maintenance software consists of idle loop reliability tests that run automatically during any ST-100 idle time, a user confidence test routine that can be called by the application program, and various diagnostic programs. The first two are designed to report on array processor usability; the diagnostic programs aid in fault isolation.

To overcome communication bottlenecks, the ST-100 has added an intermediate application software level called a process.

Two major blocks of software aid the user in coding the application processes discussed above. The first, is the array processor control language (APCL). It is the software counterpart to the parallel elements which make up ST-100 hardware. This higher level language is used to generate the
HOW TO BOARD THE MULTIBUS WITH BETTER MEMORIES

A guided tour of superior Multibus memories from the folks who know the route best. Plessey Microsystems.

Making the Multibus all that it can be requires memories that do more than just meet the specs. That's where Plessey Microsystems comes in. We can help you board the Multibus with much better memories. For example:

1/2 Mbyte Dynamic EDC Multibus Memories. Our PSM 512A gives you 512K x 8 bit dynamic memory on a single board to save slots in your system... low power consumption to save operating dollars... EDC to save your data! Single bit error detection and correction assures complete data integrity. Our options let you tailor the interrupt system to your system's needs. Standard features include on-board circuitry for all refresh functions, 8MHz optimization, byte/word control, selectable address ranges, start-up error override and a lot more.

1/2 Mbyte Dynamic Parity Multibus Memories. The Plessey PSM 512P gives you all of the features and options of the 512A with the exception of EDC. With the 512P, parity single bit error detection protects your system from undetected RAM errors. At a cost even less than our EDC memory.

Non-Volatile Multibus Memories. The new PSM 6663 non-volatile memory with interrupting real-time clock/calendar and on-board battery back-up offers capacity ranges from 16K fast static RAM to 1 Mbyte of EPROM with 256K bytes of RAM/EPROM mix.

Multibus... the Plessey Way. All Plessey Multibus memories are produced to the most demanding specs... tested on equipment so advanced that it reveals flaws which go unnoticed on other devices... double sourced by Plessey both here and abroad... priced with boards of less-than-Plessey quality... and guaranteed for a full year.

Board your Multibus with better memories. From Plessey Microsystems. For details, call or write Plessey Microsystems, Inc., One Blue Hill Plaza, Pearl River, NY 10965. (914) 735-4661. Or toll-free (800) 368-2738.

PLESSEY MICROSYSTEMS
The Plus in Your System.
program that will control process execution. The APCL compiler executes on the host to produce a process object module that will run on the ST-100 control processor. It also produces a Fortran host process subroutine (HPS), which can be linked to the host Fortran application program. The ST-100 linker combines the process object module with the called SMP and ACP macros to form a process load module suitable for execution on the array processor. When the host application program calls the process for execution, the HPS module provides the necessary interface to load the process module into the array processor.

APCL is a subset of ANSI Fortran 77 with statements added to control the architectural features unique to the ST-100, such as the hierarchical memory structure. The language also supports service requests to the array processor monitor via subroutine calls. The Macro Assembler is used to write macros for execution on the ACP and the SMP. A meta-assembler concept allows the same assembler to serve both processors. Assembler output includes a source listing with errors and cross references, object code for the target processors, and information to define the relationship between cache memory banks. APCL uses the cache memory relationship in order to determine the crossbar switching control.

**Library supports custom macro development**

Development software also includes a linker, a debugger to aid in macro debugging, a host-resident simulator (for the SMP and ACP) to aid in macro development, an application support library, and library maintenance facilities. The application support library is a set of macros for performing commonly used storage move and arithmetic control functions. The types of standard macros contained in the library are indicated in the Table. Custom macros can be developed by the user and readily added to the library. The macro level development software is provided for the user to create application specific macros (instructions) to be added to the applications support library.

Production software consists of the array processor executive (APX) and the array processor monitor (APM). These software blocks link the host computer and the array processor for execution of ST-100 processes. The APX interprets a set of Fortran-callable subroutines that interface the user application program to the array processor. It is bound and linked to the application program and executes within the context of the user's address space. APX subroutines enable the user to request array processor resources, define main memory arrays, control data movement to and from the array processor, and release array processor resources.

**Resident operating system coordinates operations**

The array processor's multiple parallel hardware elements function concurrently. Thus, an operating system is needed to control and coordinate their operation. The APM runs on the CP and oversees all of the activities within the ST-100. It communicates with multiple hosts through the I/O subsystem. This mechanism allows the APM to control data transmission between host computers and array processor main memory and to supervise main memory allocation and protection.

Execution of the multiple processes stored in main memory is scheduled on a priority basis. The APM loads a new process into the CP memory as soon as space becomes available. Execution of the new process is initiated by the APM upon completion of the currently executing process. When an application partition is released by the user, the APM returns accounting information to the host.

Turning to array processor application software, the user's fundamental concern is process development. All process development takes place on the host computer. This results in two blocks of code—a process load module which will execute on the array processor, and an application load module (ie, HPS), which will execute on the host. The top level of application software is a Fortran application program, which will execute on the host computer. This application is developed using standard host Fortran development software.

An APCL process is logically divided into a declaration section and an executable section. Process statements, Memory statements (main memory, cache memory, and local memory), and Data statements make up the declarations section. Process statements identify processes and list arguments being passed between the host and the process. The executable section contains Assignment statements as well as Call, Continue, Do, Goto, arithmetic If, logical If, Return, and End statements. These statements have their normal Fortran meaning. Assignment statements compute the results of arithmetic expressions and store them in local memory locations. Call statements initiate the execution of SMP and ACP macros or of service

### Standard macro types

<table>
<thead>
<tr>
<th>Storage move macros</th>
<th>Arithmetic macros</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moving data between main memory and data cache with format conversion</td>
<td>General vector arithmetic (real and complex)</td>
</tr>
<tr>
<td>Performing integer and logical operations on data in main memory or data cache</td>
<td>Vector-to-scalar arithmetic</td>
</tr>
<tr>
<td></td>
<td>Vector logical operations</td>
</tr>
<tr>
<td></td>
<td>Matrix operations</td>
</tr>
<tr>
<td></td>
<td>Transform operations</td>
</tr>
<tr>
<td></td>
<td>Filtering operations</td>
</tr>
</tbody>
</table>
requests. Return and End statements transfer control to the host application program. To code processes the user also needs an understanding of functions executed by the application library macros and of data cache mapping.

All process development takes place on the host computer.

Main memory statements allocate storage of array data in main memory. Local memory statements assign space in local memory (memory contained within the control processor) for scalar variables to be used in controlling process execution. Data statements assign initial values to local memory variables. Cache memory statements allocate space for data in the six logical sections of the data cache discussed earlier. Using the STsync service request, a process can assign any combination of the six cache sections to the SMP and to the ACP. This allows the programmer to direct the SMP and ACP macros to simultaneously operate on the data cache. Calls are issued by the APCL coded process to SMP and ACP macros. Using these calls, the user is able to control the sequence of operations performed on application data.

To be debugged and executed, an ST-100 process must be called by a Fortran Call statement in the host application program. Specifically, the call is issued to an HPS. An HPS in turn directs loading of the process load module into the array processor and execution of the process via the APX. The HPS object module is generated automatically by the APCL compiler during compilation of the process object module. It remains, however, for users to link the HPS with their application programs, forming a complete application load module for execution on the host.
Storage and backup problems on your QBus?
SABRE™ has a sharp solution.

SABRE™ is a cut above anything on the market. It's a new concept in high-capacity, high-performance mass storage. A 5½" Winchester/cartridge disk package for use with operating systems that run on DEC LSI-11 through 11/23+ microcomputers. SABRE's an innovative, RL02 software transparent storage alternative that puts 41.6 Mbytes on-line and delivers balanced backup through a versatile, removable cartridge disk. All in a compact, rack-mountable package.

**Standard interfaces/transparent software.**

SABRE hits the mark for reliable, high-speed, low-cost storage with convenient, efficient backup. Its UC01 host adapter plugs into any single-quad width QBus slot, and provides the Small Computer System Interface (SCSI) system-level bus for SABRE and up to five additional I/O devices. Through exact RL02 emulation, SABRE runs existing operating and diagnostic software as is. With logical RL02 images on both the fixed and removable media drives, volume backup is a snap.

**Hard disk backup performance.**

The ruggedized cartridge drive provides hard disk backup performance and reliability. Many times faster than either floppies or tape, it also provides the versatility to handle program entry, data storage and can function as a system disk. Overall, the 5½" Winchester/cartridge disk combination gives system-level performance which exceeds multiple RL02's in many applications.

**Efficient system packaging.**

Space-saving SABRE is 5½" high, slips into any standard 19" Retma enclosure and comes complete with power supply, host adapter and connecting cables. It needs one-eighth the space and draws one-quarter of the power of four RL02's. Further, SABRE slashes hardware and installation costs by eliminating the need for a separate system bootstrap, bus terminator and clock control board.

For more information on SABRE or any of the high-quality Emulex communications, disk, tape and packaged subsystem products, call toll-free (800) 854-7112. In California (714) 662-5600.

**SABRE's Features**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>Compact 5½&quot; height x 19&quot; width package contains 31.2 MB (3x RL02) 5½&quot; Winchester disk and 10.4 MB (1x RL02) removable 8&quot; cartridge disk.</td>
</tr>
<tr>
<td>Capacity</td>
<td>Equivalent to four (4) DEC RL02's.</td>
</tr>
<tr>
<td>Speed</td>
<td>Overall performance significantly increased over tape and floppies, especially in throughput and backup time.</td>
</tr>
<tr>
<td>Transparency</td>
<td>Runs standard RL02 diagnostics and operating software.</td>
</tr>
<tr>
<td>Flexibility</td>
<td>Removable cartridge disk; SCSI Bus interface allows up to five (5) I/O devices; single-board host adapter.</td>
</tr>
<tr>
<td>Reliability/Durability</td>
<td>Winchester technology; ruggedized cartridge disk construction; shock mounts; hermetically sealed HDA for protection against contamination.</td>
</tr>
<tr>
<td>Price/Performance</td>
<td>Lower cost per box and per MB in virtually all applications.</td>
</tr>
</tbody>
</table>

GSA Contract #: GSOOK8401SS575 "SABRE is a trademark of Emulex Corporation. DEC, LSI and QBus are trademarks of Digital Equipment Corporation.
Since we first entered the Winchester market two years ago, we've accomplished many things our competition claimed were impossible.

It was impossible, they said, for a floppy disk company to make a significant dent in the highly competitive Winchester market.

We've not only made a dent, we're the second-largest company in the business, and we have the capacity in place to be first.

It was impossible to expand our production capacity from 0 to 60,000 drives a month practically overnight. But we did it.

It was impossible to sell Winchesters at such a low cost. But last year our 500 series drives were introduced at under $500, 30% under then-standard industry costs. And since then, we've led the industry to ever-lower costs on full and half-height drives.

It was impossible to produce and ship high-performance plated media drives in high volume at prices lower than most vendors are charging for oxide media drives. One of our competitors backed away from plated media because they couldn't buy enough of it to build drives in efficient quantities.

We solved that problem by building our

own plated media factory dedicated to plated media production in high volume. Because we make our own, our costs are low and we are independent of outside vendors for supply.

It was impossible for a start-up company to produce and ship a broad line of products: full and half-height drives, open and closed-loop, from 6.4 to 50 MB. But we've done it. With the help of one of the industry's best-funded R&D programs. And with our steady supply of plated media, we will soon be offering 5¼" drives that push Winchester technology to the limits of its capacity. In high volume. At prices that are pure Tandon.

Impossible?
For our competition, yes.
But not for the Tandon Winchester Company.

TANDON WINCHESTER COMPANY.

Tandon
THE MOST SUCCESSFUL DRIVE COMPANIES YOU EVER HEARD OF.
OUR NEW 2Kx8 STATIC RAM IS TWICE AS FAST AS ANY OTHER BYTE-WIDE. HITTING SPEEDS TO 45ns.

Toshiba has the world's fastest 2K x 8 Static RAM. With speeds as fast as 45ns and other byte-wide units with power consumption as low as 1µA, your range of design options just got twice as wide as before.

Our new TMM2018D provides both high-speed and low-power features with an access time of 45ns. This, along with high density, explains why they're rapidly displacing bipolar devices.

All our high-speed NMOS and CMOS 2K x 8's are designed for maximum compatibility with microprocessor bus structures.

In fact, ours were the first 16K CMOS RAMs on the market. We designed them for a maximum 1µA standby current.

Operating from a single 5V power supply, our byte-wide RAMs are available in a 24-pin package, DIP (.300" or .600"), flat pack and a variety of other configurations.
If you’re designing cache memory, high-speed storage, hand-helds and other high-density memory applications, write for more information to Toshiba America, Inc., 2441 Michelle Drive, Tustin, CA 92680, (714) 730-5000. Or call your local distributor or sales representative.

Toshiba America broke the speed limit so there’ll be fewer design limitations for you.

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Type</th>
<th>Access Time (Max)</th>
<th>Operating Current (Max)</th>
<th>Standby Current (Max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016P</td>
<td>NMOS</td>
<td>150ns</td>
<td>100mA</td>
<td>15mA</td>
</tr>
<tr>
<td>2016P-2</td>
<td>NMOS</td>
<td>100ns</td>
<td>120mA</td>
<td>15mA</td>
</tr>
<tr>
<td>2016P-4</td>
<td>NMOS</td>
<td>140ns</td>
<td>120mA</td>
<td>15mA</td>
</tr>
<tr>
<td>2016AP-9</td>
<td>NMOS</td>
<td>90ns</td>
<td>80mA</td>
<td>7mA</td>
</tr>
<tr>
<td>2016AP-10</td>
<td>NMOS</td>
<td>120ns</td>
<td>65mA</td>
<td>7mA</td>
</tr>
<tr>
<td>2016AP-12</td>
<td>NMOS</td>
<td>50ns</td>
<td>65mA</td>
<td>7mA</td>
</tr>
<tr>
<td>2016AP-18</td>
<td>NMOS</td>
<td>45ns</td>
<td>65mA</td>
<td>7mA</td>
</tr>
<tr>
<td>201ID-45</td>
<td>NMOS</td>
<td>45ns</td>
<td>120mA</td>
<td>20mA</td>
</tr>
<tr>
<td>2010D-55</td>
<td>NMOS</td>
<td>55ns</td>
<td>120mA</td>
<td>20mA</td>
</tr>
<tr>
<td>5516P</td>
<td>CMOS</td>
<td>250ns</td>
<td>55mA</td>
<td>30µA</td>
</tr>
<tr>
<td>5516P-2</td>
<td>CMOS</td>
<td>200ns</td>
<td>55mA</td>
<td>30µA</td>
</tr>
<tr>
<td>5516PL</td>
<td>CMOS</td>
<td>280ns</td>
<td>55mA</td>
<td>30µA</td>
</tr>
<tr>
<td>557BP</td>
<td>CMOS</td>
<td>280ns</td>
<td>25mA</td>
<td>1mA</td>
</tr>
<tr>
<td>557BP-2</td>
<td>CMOS</td>
<td>200ns</td>
<td>25mA</td>
<td>1mA</td>
</tr>
<tr>
<td>557BPL</td>
<td>CMOS</td>
<td>200ns</td>
<td>25mA</td>
<td>1mA</td>
</tr>
<tr>
<td>5518BP</td>
<td>CMOS</td>
<td>200ns</td>
<td>25mA</td>
<td>1mA</td>
</tr>
</tbody>
</table>

*A also available in a .300" wide package — Part No. 2015-XX.
**Available only in a .300" wide package.
Meet the newest member of our Datatest family. The Datatest II Plus is a complete lightweight test set that offers all the powerful capabilities of the Datatest II...and more.

Here's the PLUS!

**Simultaneous 17 function BERT test**
- Counts bit errors, bits received, block errors, blocks received, error free seconds, errored seconds, sync losses, time outs, parity errors, framing errors, and BCC errors. Also displays on-line transmit and receive data, summarizes test set-up and enables a multifunction timer. In addition, it calculates both bit and block error rates, simultaneously.

**Optional X.25 Diagnostics/Monitoring/Statistics**
- Emulate and test all 3 levels, send and receive calls, frame and packet level mnemonic decoding, calculate average size of data packets, system throughput per logical channel number and much more.

**Additional features:**
- User definable flow control
- Interactive keyboard functions
- CRC/BCC calculation
- Permanent storage for all user messages and set-ups
- 25 function timer
- Rechargeable battery operation
- Echo function
- 4094 character trap
- DTE test function
- 16 user messages
- Alarm
- Parity error measurement
- Optional input/output package provides downline loading, printer output functions, memory pacs, and much more
- Optional SNA/SDLC package
- Weighs only two lbs., 90 in³

Call or write today for more information.

$2195.

**THE NEW DATATEST II PLUS**

THE ULTIMATE FIELD SERVICE TEST SET!

NAVTEL
FOR THE TESTING TIMES
TELEPHONE 1-416-669-9918
A division of **ATCO**
CIRCLE 63
USING AN EFFICIENT MICROARCHITECTURE ACHIEVES GOALS

Careful microarchitecture planning enables design engineers to achieve dual goals of low cost and high performance in a 32-bit computer.

by Kenneth Burns and David M. Burns

A computer's architectural specification defines that machine on a functional level. As technology advances, the machine itself may change. But as long as it maintains the required relationship between input and output, it can be said to adhere to the architectural specification.

New generations of machines with the same architecture acquire different levels of price and performance by adding or deleting such performance accelerators as pipelining or cache. To help in the development of new models along the price/performance curve, design engineers use a software tool called a hardware simulator. By simulating the runtime environment of the proposed machine, designers can determine if the incremental performance gain is worth the additional hardware cost.

A machine's microarchitecture design requires similar trade-offs. An increase in microcode speed and flexibility usually means a commitment to a more costly design. Thus, the microarchitect's task is to design a microcode structure based on the proposed hardware design. This allows the machine to be positioned at its targeted level on the price/performance curve. A perfectly horizontal microword exists when every control line in the machine is associated with a bit in the microcode word. Once conceptualized, this initiates the design process. This structure offers the maximum amount of parallelism, and hence speed, which is available with a proposed set of hardware resources.

In reality, trade-offs are inevitable, since the hardware limits the amount of parallel processing possible within the machine. As the design process continues, the microcode structure moves toward a more vertical implementation. This means that a narrower microword can be used, resulting in a lower implementation cost.

Data General's recently introduced Eclipse MV/4000 system is a low cost, high performance implementation of the same MV architecture on which the Eclipse MV/8000 system is based. Although it was unnecessary to redesign a new functional instruction set, engineers faced several design challenges during the machine's development. An initial constraint was that the entire CPU be contained on only two boards. This required the development of a highly efficient and flexible microarchitecture that produced optimum algorithm execution speeds.

The MV/4000 CPU (Fig 1) is a version of the company's 32-bit MV/family architecture. Although it has the functional ability of the higher performance
MV/8000, the CPU board count was reduced from eight to two boards. This was made possible by using VLSI, gate array, and high speed Schottky technology, and by the definition of a highly compact and efficient microarchitecture.

The system control unit (SCU) in Fig 2 contains the instruction prefetcher, microsequencer and its associated control store, memory control, and clock generation logic. The instruction prefetcher consists of a three-level pipe that allows overlapped fetch and execution of instructions. The prefetch unit also generates the displacements used in memory reference address calculations. These displacements, together with the instruction predecode gate array and macroinstruction decode PROMs, form a starting microcode address that is sent to the microsequencer.

The microsequencer determines the order in which the vertical control store words are accessed and subsequently executed. A 9-bit field in the currently executing vertical microword determines the selection of the proper horizontal control word. At power-up time, and before the soft vertical control store has been loaded from system media, the microsequencer addresses a NOVA instruction set that is contained in kernel PROM. Using the 110 instructions contained in this kernel, the vertical control RAM is loaded with the full MV instruction set, and control is transferred to it.

Additional SCU logic performs error checking and correction on all memory accesses, and controls main memory refreshing. Hardware referenced and modified bits for each physical page are used by the AOS/VS operating system to support its page replacement algorithm.

How the system processing unit functions

The system processing unit (SPU) of Fig 3 performs all arithmetic and logical operations, both high and low speed I/O, and translates 32-bit logical addresses to physical memory addresses. Within it, a 32-bit ALU is responsible for all data manipulation. It contains eight 4-bit-slice ALU chips that are cascaded together to give full 32-bit capability. A separate nibble shifter allows for efficient data alignment. The ALU also contains the microcode visible register set (GR0 to GR7), user visible accumulators, wide stack pointer, and macro program counter (PC).

Data General's two standard I/O buses are implemented on the MV/4000. The low speed Eclipse data channel transfers data at 1.5 Mbytes/s, while the high speed burst multiplexer channel (BMC) performs block transfers at the rate of 5 Mbytes/s.

To implement full 32-bit virtual capabilities, the SPU contains logic that translates the 32-bit logical address to a 22-bit physical address. Using this address, the CPU can directly access the entire 8 Mbytes of physical memory.

To form the physical address, the logical address is taken from the ALU output (YBUS) and placed in the logical address register (LAR). This address is
Fig 2 The MV/4000 system control unit performs instruction prefetch, microsequencing, memory control, and clock generation.

Fig 3 The MV/4000 system processing unit performs arithmetic and logical operations, I/O and address translation.
<table>
<thead>
<tr>
<th>µseg step</th>
<th>PRA</th>
<th>PRB</th>
<th>µaddress</th>
<th>Predecode register, NIR</th>
<th>DISPHI</th>
<th>DISPLO</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>WADD</td>
<td>WSUB</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>WADD</td>
<td>WSUB</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>WADD</td>
<td>WADD</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>LWLDA</td>
<td>DISPO to 15</td>
<td></td>
<td>WADD</td>
<td>WSUB</td>
<td>WSUB</td>
</tr>
<tr>
<td>5</td>
<td>LWLDA</td>
<td>DISPO to 15</td>
<td></td>
<td>WADD</td>
<td>WSUB</td>
<td>WSUB</td>
</tr>
<tr>
<td>6</td>
<td>LWLDA</td>
<td>DISPO to 15</td>
<td></td>
<td>WADD</td>
<td>WSUB</td>
<td>WSUB</td>
</tr>
<tr>
<td>7</td>
<td>DISP16 to 31</td>
<td>WMOV</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>DISP16 to 31</td>
<td>WMOV</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>-</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>-</td>
<td>-</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>-</td>
<td>-</td>
<td></td>
<td>WADD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig 4 This instruction prefetch example shows the logical stepping of the prefetcher (not individual microcycles).

then translated by using information stored in the scratchpad’s (SPAD) address translation cache. The user has the option of specifying a special “physical” mode, in which case no translation will take place.

**Surveying pipeline stages**

The MV/4000 prefetcher is implemented as a three-stage pipeline that allows instruction prefetching, decoding, and execution to occur in parallel. The PC prefetch logic on the SPU (Fig 3) initiates a double word (32-bit) read from memory that is transferred via the memory data bus to the prefetch A (PRA) and prefetch B (PRB) 16-bit registers. This is the first stage of the pipeline.

In the second stage of the pipeline, the next instruction register (NIR) is loaded with the next 16-bit instruction opcode to be executed. This may come from either PRA or PRB, depending on the previous instruction sequence. At the same time, this opcode passes through the instruction predecode gate array, the output of which is stored in the predecode register (PR). This gate array uses the 16-bit opcode to produce an address for the macroinstruction decode PROMs.

The decode PROMs output a starting microcode address for the macroinstruction. This is placed on the alternate address (ALT) bus and driven to the microsequencer. In addition, the PROMs produce instruction specific decode information that is loaded into the extended instruction register (XIR) during the third stage of the pipeline. To maximize pipeline throughput, displacement data from the first stage of the pipeline is transferred to the displacement latches during stage two. This enables the prefetcher to request additional data.

Instruction execution occurs during stage three of the pipeline. The instruction register (IR) is loaded with the instruction opcode saved in NIR, while XIRs accept additional decode PROM information. The following example illustrates the execution of the instruction sequence:

- **WADD** Adds two 32-bit accumulators together
- **WSUB** Subtracts one 32-bit accumulator from another
- **LWLDA** Loads a 32-bit accumulator from the memory location specified by the 32-bit logical displacement
- **WMOV** Moves one 32-bit accumulator to another

These instructions are stored in memory as shown below:

```
<32 bits->
```

```
WADD  WSUB
LWLDA  DISPO to 15
DISP16 to 31  WMOV
```

They are prefetched, decoded, and executed, as shown in Fig 4. The following steps describe the logical movement of instructions through the prefetch pipeline.

Begin in step 1 (Fig 4) by prefetching the double word containing the WADD and WSUB opcodes and loading it into PRA and PRB. In step 2, the WADD opcode is passed through the instruction predecode gate array. This generates a unique 9-bit address that is saved in the PR where it will be used to access the macroinstruction decode PROMs. The WADD opcode is also loaded into NIR at this time. During step 3, the starting microaddress of the WADD instruction (produced by the decode PROMs) is placed on the ALT bus and then sent to the microsequencer, thereby allowing WADD execution to begin in the next cycle.

Step 4 (Fig 4) shows how all three stages of the prefetch pipeline can advance simultaneously. Here, the IR is loaded with the WADD opcode,
How it blasts through software BOTTLENECKS

How would you like to have a picture that identifies a software bottleneck? A picture taken as your software executes in real time? Via a measurement that is completely nonintrusive? Well now you can do all that. Via a low-cost subsystem for HP's 64000 Logic Development System called the 64310A Software Performance Analyzer.

But that's not all this powerful new software tool can do for you. It gives you a perspective on software like the one shown to help you characterize software through benchmarks of processors, operating systems, algorithms, application programs, etc. It provides data for intelligent hardware/software design trade-off decisions. It gives you new insight into software debugging, revealing interaction problems difficult or impossible to spot with other techniques. And it can put a spotlight on software inefficiencies that rob your system of performance and add extra cost.

Six different perspectives on software in action

Consider your own software projects. What problems could you solve with these six measurement modes?

1. *Memory activity* measurements, which show how your memory resources are being utilized. 2. *Program activity*, giving you a direct measure of time or occurrences required by specific software modules. 3. *Module duration*, showing execution time distribution of a specific software module as it reacts to internal and external stimuli. 4. *Module usage*, a measure of module demand. 5. *Inter-module duration*, the distribution of times from the exit of one module to the entry of another. 6. *Intermodule linkage*, the number of direct transfers between specific module pairs.

Individually, in combination, and interactively with emulation and logic analysis, these measurements give you tremendous new insight into software activity resulting in higher performance software with less development time.

High-level commands and histogram displays spell simplicity

This is an analyzer software engineers and programmers will feel at home with. That's because of its high-level symbolic interface that lets you define measurements and view results in familiar software terms using module names and variable names directly from the program being executed. Histogram displays of all measurements give you an intuitive feel for software activity. And statistical measurements and displays provide confidence level and error tolerance information.

Every lab should have at least one software performance analyzer

Consider this. The 64310A, costing just $3400*, can be added as a plug-in board. Many engineers who have used this analyzer report a factor of two or better improvement in software performance with very little effort. Few analysis tools offer so much for so little.

For more information, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

*U.S.A. list price only.
while the XIR receives the instruction specific decode PROM information for WADD execution. At the same time, the WSUB opcode in PRB is driven through the instruction predecode gate array and loaded into the predecode register. The WSUB opcode in PRB advances to the next stage of the pipe and is saved in NIR. The prefetch logic, having detected that the WADD and WSUB opcodes are no longer needed in PRA and PRB, now proceeds to load the next double word from memory. This double word fetch is initiated by the SCU which starts the PC prefetch logic on the SPU (see Fig 3).

Microcode assists in this task by indicating to the prefetcher, via the instruction prefetcher GO (IPGO) random (Fig 5), when the currently executing instruction will be completed. Upon completion, the pipeline will advance, and since both PRA and PRB are free at this time, they will be loaded with the double word prefetched from memory. This double word contains the LWLDA opcode and its upper 16 bits of address displacement.

The starting microaddress for the WSUB is generated in step 5 and is sent via the ALT bus to the microsequencer. Since WSUB is now executing, and its opcode has advanced to the IR, the predecode register and NIR are free to accept the LWLDA information in step 6.

To allow the lower 16 bits of the LWLDA displacement (DISP16 to 31) to be fetched, the upper portion of the displacement (DISP0 to 15) is saved in the DISPHI latch during step 7. This permits the double word containing DISP16 to 31 and the WMOV opcode to be loaded into PRA and PRB. The full 32-bit displacement of the LWLDA will be formed in the next step when DISP16 to 31 is loaded into the DISPLO latch. The instruction prefetch logic detects this, and proceeds to drive the starting microaddress for the LWLDA over the ALT bus.

The LWLDA instruction executes in step 8. To maximize prefetch piping, the displacement is only guaranteed to be valid during the first cycle of the instruction. This enables DISPHI and DISPLO to be

---

Note: \( \mu F1 \) is always bits 0, 1, 2 and parity is in 31 even if not shown.

<table>
<thead>
<tr>
<th>( \mu F1 )</th>
<th>( \mu F2 )</th>
<th>Test</th>
<th>AA</th>
<th>PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>horizontal</td>
<td>COND PA</td>
<td>horizontal</td>
<td>UNCOND AA</td>
<td>horizontal</td>
</tr>
<tr>
<td>horizontal</td>
<td>horizontal</td>
<td>horizontal</td>
<td>UNCOND</td>
<td>horizontal</td>
</tr>
<tr>
<td>horizontal</td>
<td>horizontal</td>
<td>horizontal</td>
<td>NEXT</td>
<td>horizontal</td>
</tr>
<tr>
<td>horizontal</td>
<td>horizontal</td>
<td>horizontal</td>
<td>UNCOND PA</td>
<td>horizontal</td>
</tr>
<tr>
<td>horizontal</td>
<td>horizontal</td>
<td>horizontal</td>
<td>COND GOTO</td>
<td>VONLY</td>
</tr>
</tbody>
</table>

| AREG | AREG | SPAD 8 |
| BREG | BREG | Constant |
| I | I | |
| OP | MEM | DBUS |
| C | I | |
| CARRY | 1 | |
| NIBSC | ALUOP | 1 |
| I | SRC | |
| I | G | |

SPAD ADDR 8
Constant 8
AREG 1
AREG 2
AREG 3
BREG 1
BREG 2
BREG 3
ALUOP 1
MEM 1
DBUS 1
ALUD 1
CARRY 1
CARRY 2
BIN 1
NIBSC 1
ALUS 1
SCU Control
IPGO

Vertical only defaults:
a) YBUS = ALU
b) SPAD address control = address translation unit (ATU)
c) SPAD operation = read
d) NIBSC = align_d
e) SPAD address = ATU

Fig 5 A vertical field example shows vertical formats and usage.
The HDS-400 is the most versatile emulation system available for Motorola's 68000 series microprocessor. And now you can rent this system from Leasametric, the foremost renter of quality electronic test equipment.

Speed, simplicity and power. The HDS-400 runs up to 12.5 MHz clock speed, the fastest today. And it performs real-time emulation and analysis at clock speeds up to 10 MHz with no wait states. So you can gauge your prototype's true performance.

This emulation system is unique. It can download both the target system code and the debugging system from either the Motorola EXORmacs Development System, DEC VAX or Motorola VME/10 as hosts. The HDS-400 can serve as a fully functional substitute for the MPU in your target system. And its analysis commands are straightforward, so you can rapidly debug and integrate your target system.

But this simplicity and power is further enhanced by the Bus State Analyzer module that is also available for rent from Leasametric. With it you can gather data by continuous trace mode, sequential trigger mode and window trigger mode. Plus generate performance histograms that provide a clear picture of system performance efficiency.

Rent the best from the best. Rent the HDS-400 from Leasametric and you get equipment that has been rigorously tested and fully calibrated. It arrives ready to work. Complete with operator's manual and all accessories.

Our service is famous in the industry. We'll ship your order immediately and be there if you need us. If a system problem occurs, we'll take immediate action. With timely on-line diagnostics, on-site service or replacement.

Call Leasametric and stretch your cash. Our rental charges are much smaller than the capital outlays of buying. Rent what you need. Or lease it. Or rent with option to buy. We'll tailor a package that fits your needs.

Rent and you pay for equipment that's being used, not sitting on a shelf somewhere. Real-time emulation at the right price. And Leasametric has thousands of other quality items for rent. We'd be pleased to tell you more—and to send our latest catalogue. Call us at 800-227-1817. In Europe, call Leasametric GmbH, Eching/Munich (089) 3192007.

Rent the best name in the business from the best name in the business.
used in the next cycle in the event of back to back 32-bit memory reference instructions. Steps 9, 10, and 11, show the WM0V instruction as it advances through the instruction decode and execution stages of the pipeline.

**Microinstruction flow**

The MV/4000’s microcode architecture was designed to allow the greatest degree of flexibility, and reduce the necessary control store width to allow a two-board implementation. Algorithmic speed was among the primary concerns of the microword architects. The chosen architecture takes into account the most common microcode operations, allowing them to be performed in one cycle.

To initiate the actual execution of a macroinstruction, a starting microcode address is driven from the prefetcher to the microsequencer via the ALT bus. Once there, it passes through the micro direct bus input multiplexer and enters the microprogram control unit. This address is then used to access vertical control store RAM, the output of which is registered in the vertical instruction register (VIR). Because a vertical microinstruction is associated with every microcycle, subsequent microaddresses for the executing macroinstruction are generated by the next address control (NAC) field contained within the vertical microinstruction.

The NAC field allows for conditional and unconditional sequencing. Conditional microsequencer functions are based on the results of a test selected by the vertical microword. On the other hand, unconditional operations will always be performed. Examples of microsequencer operations include jumps, subroutine calls and returns, 16-way calls, advancing to the next microaddress (NEXT), microstack push, and microstack pop. Many of these functions use the 16-level microstack because microaddresses can be saved on it.

The microword architecture selected for the MV/4000 consists of both vertical and horizontal control store (Fig 6). The power and flexibility of this architecture is due to the large amount of interaction between the two.

**Vertical control store**

Each vertical microword, except for the vertical only format, can specify any 1 of 512 horizontal microwords. The selected horizontal may in turn specify that certain bits of the vertical microword be used as control during the microcycle. In addition to selecting the horizontal, the vertical microword performs other functions such as determining which microsequencer operation is to be performed, supplying 1 of 128 possible test conditions, and supplying an absolute microaddress field. Thus, the microcoder logically sees the execution of a very powerful “functional” microword on every machine cycle. This functional microword consists of a combination of the selected horizontal along with certain vertical fields (vertical modifiers) specified by the horizontal.

The MV/4000 contains 16-K x 32 bits of vertical control store, thereby requiring a 14-bit address field for full access capability. In order to use fewer vertical bits to specify an address, microcode is broken into 256-word pages, requiring only an 8-bit page address (PA) for operations within the same page. The 6 page bits, maintained by the microsequencer, specify which of the 64 pages is currently being accessed. To change the current page of execution, a microsequencer format containing the full 14-bit address (AA) must be selected. Fig 5 shows all possibilities of vertical field usage.

The vertical control word is only 32 bits wide. Of these bits, 7 bits select the microsequencer function ($\mu F1$ and $\mu F2$), 1 bit is for parity (#), and 9 bits select 1 of the 512 horizontal control words, leaving 15 bits of vertical microword free to specify control. These 15 free bits are often required to specify a TEST and NEXT PA, or to select a constant.

The horizontal can fill a field in one of two ways. It can specify the value for the field directly, or it can indicate which vertical control word bits will be used to control the field. Several of the fields have more than one possible vertical source. For example, Fig 5 shows that the ALU B register source (BREG) may come from one of three possible places in the vertical microword. BREG1 uses the vertical bits 3 to 6, BREG2 bits 7 to 10, and BREG3 bits 18 to 21, as the value for BREG. This 4-bit BREG value is used to select one of 16 possible microcode visible registers from the ALU register file. The horizontal may also specify that the BREG value must come directly
WHO ELSE COULD FIT 520MB,
20 YEARS OF EXPERIENCE
AND A $6 BILLION COMPANY
INTO A 9” DISK DRIVE?

features 520 megabytes (unformatted) of storage capacity, a 15 millisecond average access time and

8” drive that NEC customers have been using for the past three years.

We know what systems builders need. We build systems too.

That gives us an edge over other drive companies. Because it gives us a special insight into the needs of a systems builder.

The D2300 is extremely compact. At just 8½” wide, two drives can be mounted in a single 19-inch rack for a storage capacity in excess of one gigabyte.

For the name of your nearest NEC representative, call 1-800-343-4418 (In Massachusetts, call 617-264-8635). You'll discover why more and more systems builders are saying “NEC and me.”

WHO ELSE COULD FIT 520MB,
20 YEARS OF EXPERIENCE
AND A $6 BILLION COMPANY
INTO A 9” DISK DRIVE?

520 MB, SIZED FOR TODAY'S SMALLER SUPERMINIS.

Who else but NEC?

NEC has been pioneering advancements in electronics for almost 85 years. And developing disk drives since their beginning, back in 1959.

Today we're a $6 billion company. And one of the leading disk drive manufacturers in the world.

Introducing our new 9” drive.
It's not only big, it's super fast.

Our latest drive achievement, the NEC D2300,

data transfer rate of 1.859 megabytes per second.

Behind our new 520 MB drive is a field-tested technology.
The technology of the D2300 is evolutionary. It is based on our successful 402 MB plated media

520 MB, SIZED FOR TODAY'S SMALLER SUPERMINIS.

IF YOU'RE READY FOR OUR NEW 9” DRIVE, WE'RE READY TO SHIP.

NEC AND ME

NEC Information Systems, Inc.
1414 Mass. Ave.
Boxborough, MA 01719

CIRCLE 66
from its own HREG field instead of using one of the three previously mentioned vertical fields. The horizontal's ability to select the control of a field from one of several vertical sources increases the microarchitecture's flexibility.

The final BREG select value is generated by the currently executing vertical microinstruction which selects 1 of 512 possible horizontals. The BREG field of the selected horizontal is then used to control the BREG MUX. This multiplexer allows one of four possible 4-bit BREG sources (horizontal HREG value, V18 to 21, V7 to 10, or V3 to 6) to be chosen as the ALU B register address. The selected 32-bit register is then used as the input to the ALU's B side.

Specific vertical bits can often be used to control more than one portion of the machine. For example, Fig 5 shows that vertical bits 18 to 21 can be used to specify an ALU B source (BREG), DBUS control, ALU destination (DES), and ALU carry input (C), or nibble shifter control (NIBSC). One of the constraints placed on the microcoder is that it must be aware of all possible combinations of vertical fields allowed. In most cases this can be overcome by permitting the horizontal to be the source for some of the control. This is not always possible, however, due to the limited number of horizontals.

Although control sourcing several fields from the same vertical bits may seem a constraint, it actually allows more combinations of fields to be specified than would be possible if these bits were only used to control a single field. To take advantage of this "microfield multiplexing" capability, the majority of horizontals were designed to be as general as possible. This means that they choose to use a large number of vertical modifiers, enabling a small group or horizontals to handle most operations.

**Examining vertical field usage**

Another way of controlling the machine is called vertical only. This method does not require a horizontal to be specified, thus allowing 9 more bits of vertical control. Vertical only is used whenever the next microaddress can be derived from the current microsequencer state. Examples include situations where control proceeds directly to the next microaddress, and operations such as popping the microstack on microcode subroutine returns. The vertical only word is designed to be the most general word available to the microcoder. It allows for complete control of the ALU and memory. Associated with the vertical only field are several default values for fields not specified by the vertical only microword.

To further illustrate vertical field usage we will examine all microsequencer functions that have an impact on BREG selection (see Fig 5). If µF1 contains the NEXT encoding, then vertical bits 3 to 21 are all free to be selected by various fields in the horizontal. This means that the horizontal may select either BREG1, BREG2, or BREG3. Of course, the horizontal is always free to specify BREG directly through the use of its HREG field.

When a conditional microsequencer function is specified that does not require an address field (see Fig 5, COND), then vertical bits 14 to 21 become available. Such a case is the conditional return operation where the desired address has been previously stored on the microstack. This allows the use of vertical bits 18 to 21 (BREG3) or HREG from the horizontal to specify BREG.

UNCOND PA is an unconditional microsequencer operation that specifies a microcode address. This format allows vertical bits 7 to 10 (BREG2) to be used for BREG specification. The horizontal HREG field is also available.

If a conditional goto (COND GOTO) is coded into the µF1 field, then only vertical bits 3 to 6 (BREG1) are available for selection by the horizontal. Vertical bits 7 to 10 (BREG2) and 18 to 21 (BREG3) cannot be chosen because these fields are occupied by TEST and PA, respectively. Again, the HREG field of the horizontal may also be used as the BREG value.

An unconditional subroutine call must use the UNCOND AA format to specify a new 15-bit microaddress (AA). This means that no vertical bits are available to specify BREG, leaving only the HREG field of the horizontal to supply the BREG value. If a horizontal is not needed, the vertical only (VONLY) format may directly select BREG from vertical bits 3 to 6.

The MV/4000 microcode is written in a high level register transfer language developed solely for the microassembler. In contrast, the MV/4000 uses a free form input to its microassembler that enables the microcoder to input high level language statements that are logically equivalent to the desired hardware function. Since unused fields need not be specified, the chances of programming error are reduced while microprogrammer productivity is increased.

---

**Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.**

- High 710
- Average 711
- Low 712
UDS gives 212 users three ways to go!

212A — Today's most popular modem. UDS offers a fully Bell-compatible unit with complete local and remote test capability. Select 0-300 or 1200 bps for full-duplex asynchronous communication. The UDS 212A is FCC certified for direct connection to the dial-up telephone network, and available in multi-channel, rack-mounted configuration.

SINGLE UNIT PRICE $595

212 LP — Compatible with 212As at the 1200 bps, full-duplex asynchronous communication rate. No power supply or AC connection required; the 212 LP derives its operating power directly from the telephone line. Ideal for applications requiring 212A capability at 1200 bps only. The 212 LP is direct-connect certified.

SINGLE UNIT PRICE $445

212A/D — Identical to the 212A, with automatic dialing capability added! The unit stores and dials up to five 30-digit numbers. CRT menu prompting, single-stroke commands and automatic test capabilities are provided. The 212A/D is direct-connect certified.

SINGLE UNIT PRICE $645

Universal Data Systems

5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/837-8100; TWX 810-726-2100

DISTRICT OFFICES:
- Old Bridge, NJ, 201/251-9090
- Blue Bell, PA, 215/643-2336
- Atlanta, 404/988-2715
- Glenview, IL, 312/998-8190
- Columbus, OH, 614/985-3025
- Boston, 617/875-8868
- Richardson, TX, 214/680-0002
- Englewood, CO, 303/694-6043
- Houston, 713/988-5506
- Tustin, CA, 714/669-8001
- Mountain View, CA, 415/969-3323

CIRCLE 67
SIMPLE SHIELDING SOLUTION.

**AMP shielded ribbon cable connectors.**
**EMC retrofit, without board redesign.**

Now designers facing FCC Docket 20780 requirements have two ways to go.

Redesign your pc boards to accommodate shielded headers.

Or keep your present board design and headers, and use AMP shielded ribbon cable connectors.

On the board, a one-piece metal shield snaps onto the universal header you’re using. At the cable, a specially-sized AMP-LATCH connector with metal shell crimps to the cable shield. No soldering is required.

And the cable half fits the board half perfectly.

AMP has other shielding solutions, too, including shielded subminiature Ds (that fit existing metal-shell headers) and even a shielded feed-through assembly for ribbon cable passing through a panel cutout.

All ways to help you turn redesign time into new-design time. All ways to get you back to the business of productivity.

From AMP.

---

For complete details, call the AMP-LATCH Information Desk at (717) 780-4400. AMP Incorporated, Harrisburg, PA 17105.

**AMP means productivity.**

---

**AMP Facts**

**Shielded AMP- LATCH Connectors**
- Full 360° termination, multiple point-piercing contacts suitable for foil and mesh type shields.
- Snap-on plastic cover provides strain relief.

**Subminiature D Connectors**
- Mates with existing metal-body subminiature D headers.
- Metal shield fits over standard AMP subminiature D cable connector.

**Standard AMP-LATCH Connectors**
Styles, shapes and configurations to fill any need.

AMP and AMP-LATCH are trademarks of AMP incorporated.
Computers designed for the office environment are in for a shock!

Here's a shocking fact: when someone sets a computer down on a desk, the disk drive inside can be subjected to a pulse shock as high as 30 g's. Obviously, if the disk drive (or any other component in your system) can't handle that kind of shock, your system runs the risk of breaking down under rather ordinary conditions—like every time there's an office shuffle and people move their computers.

What follows is some technical information on how we handle the problem in our high performance 5¼-inch Winchester disk drives.

Shock and vibration: twin problems

Shock, and the closely related problem of vibration, have come under intense study at ATASI Corporation, and for good reason: both can cause loss of data. A severe pulse shock can cause a
drive’s head to “slap” against the disk, removing a “divot” of oxide material, along with the data written there. Severe vibration can cause the head to overshoot or undershoot a track, so that the head can’t find the data it’s seeking. In addition, vibration can fatigue components over time, and perhaps lead to premature failure.

**Double shock isolation**

In order to sustain high shock loads, the ATASI design incorporates a unique dual system for shock and vibration isolation. Like most disk drives, ATASI drives have isolators between the frame and the head/disk assembly bowl. In addition, ATASI’s proprietary design includes elastomere isolators inside the bowl, between the bowl and baseplate on which the head/disk assembly is mounted. A foam pad with high damping properties, also located between the baseplate and the bowl, further protects the head/disk assembly from vibration.

The grommets ATASI uses for isolators are far from ordinary. To handle both pulse shocks and vibration effectively—to avoid a declining spring rate with displacement while maintaining adequate damping properties—ATASI tested 330 different options before making a choice. These tests involved the use of a laboratory shaker as well as computer models.

ATASI’s double isolation system more than protects its drives—and the data they store—from the shocks of the office environment.

**Beyond the shock/vibration problem**

Shock and vibration engineering is only one of a number of ways ATASI achieves such a high level of data integrity. ATASI drives also feature dedicated “landing zones.” Upon powerdown—intentional or emergency—the back e.m.f. of the motor is used to position the carriage over data-free landing zones. A carriage lock then mechanically holds the carriage in place, protecting the data field from any head contact.

**The ATASI White Paper**

At ATASI, we are proud of the quality we build into every drive we make, and we encourage clients to test our products rigorously. To help, we have prepared a White Paper on shock and vibration for systems integrators. It discusses test methods and the interpretation of test data in detail.

If you are a systems integrator, contact ATASI Corporation now to receive your ATASI White Paper. Corporate headquarters: 2075 Zanker Road, San Jose, CA 95131, (408) 995-0335; Eastern region: (617) 890-3890; Southwest region: (714) 432-0757.

---

**Performance Specifications**

<table>
<thead>
<tr>
<th>Model No.</th>
<th>3033</th>
<th>3046</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td>33 MB</td>
<td>46 MB</td>
</tr>
<tr>
<td>Access Time (Avg.)</td>
<td>30 ms</td>
<td>30 ms</td>
</tr>
<tr>
<td>Data Rate</td>
<td>5 Mbits</td>
<td>5 Mbits</td>
</tr>
<tr>
<td>Interface</td>
<td>ST 506</td>
<td>ST 506</td>
</tr>
</tbody>
</table>

Available in high volume today.

<table>
<thead>
<tr>
<th>Model No.</th>
<th>3065</th>
<th>3075</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td>65 MB</td>
<td>75 MB</td>
</tr>
<tr>
<td>Access Time (Avg.)</td>
<td>24 ms</td>
<td>24 ms</td>
</tr>
<tr>
<td>Data Rate</td>
<td>5 Mbits</td>
<td>5 Mbits</td>
</tr>
<tr>
<td>Interface</td>
<td>ST 506</td>
<td>ST 506</td>
</tr>
</tbody>
</table>

Never before has anyone put so much into something so small. The WY-50 gives you big terminal features without occupying your entire work-space. This took revolutionary design. Design a lot of people couldn't accomplish for the price. But we did.

In fact, the WY-50 introduces a new standard for low-cost terminals. You get a compact, full-featured design that meets the most advanced European ergonomic standards. 30% more viewing area than standard screens. And a price tag as small as they come.

The WY-50 sells for only $695.00.

FEATURES:
- 14" screen.
- 80/132 column format.
- Soft-set up mode.
- High resolution characters.
- Low-profile keyboard.
- Industry compatible.
- Only $695.00.

For more information on the revolutionary design, outstanding features and unique good looks of the new WY-50, contact WYSE and we'll send you a brochure filled with everything you need to know. The WY-50. The full-featured terminal with the small price.

WYSE TECHNOLOGY 3040 N. First St., San Jose, CA 95134, 408/946-3075, TLX 910-338-2251, Outside CA call toll-free, 800/421-1058, in So. CA 213/340-2013.
MOTOR CONTROL
SYSTEM DESIGN HINGES ON PROCESSOR DELAYS

Microprocessors are a boon to motor-speed controllers, but certain limitations of the devices must be accounted for in system designs.

by Manuel R. Cereijo

Although microprocessor-based control systems are quickly overtaking analog controllers, designers must understand that using a microprocessor does not remedy all design problems. In fact, in realtime systems, time delays in microprocessor execution can significantly affect system response. For example, in digital motor-speed control applications, execution speed can be relatively slow, putting an inherent upper limit on the sampling rate. Another limitation of a microprocessor is finite word length. If a processor handles only 8 bits, resolution is limited to 256 discrete outputs.

Before undertaking the design of a complex system such as a digital motor-speed controller, a prudent designer should be aware of the types of problems usually encountered. In the matter of time delays, two factors stand out. The first is long delays; if they are too lengthy, there is insufficient time to carry out the computations necessary to execute the control algorithm. The second is the adverse effect that delays have on the stability of closed-loop systems.

Time delays resulting from microprocessor computation can be identified by analyzing both the program in the control routine and any sub-

---

Manuel R. Cereijo is associate dean for the College of Technology, School of Engineering, at Florida International University, Tamiami Campus, Miami, FL 33199. Dr Cereijo holds a DSC from Universidad Central, Cuba, and an MSEE from the Georgia Institute of Technology.
control algorithm can take anywhere from 2 to 5 ms to execute completely. Obviously, execution time varies according to the processor and the program. A designer must come up with a good estimate of the minimum and maximum delay times for the system. Such information is available in the microprocessor's user manual, and this allows a designer to calculate the total number of machine states to execute a program, or to determine the time required to reach a specific point in any computation performed by the program.

From analog to digital
As a first step toward designing a digital motor-speed controller, it is helpful to examine the fundamental principles of its analog counterpart. A basic analog motor-speed control system is shown in Fig 1, and in this case, assume that the motor is a fractional-horsepower dc servo motor.

The reference input voltage to the system is variable—0 to -15 V—and is provided by a potentiometer. This voltage is an analog representation of the motor's desired speed. The reference voltage is fed through a resistor into an operational amplifier connected in the voltage-summing mode. A second input to the amplifier is in the form of a negative feedback signal that is proportional to the motor's speed. This feedback signal comes from a tachometer, or other type of speed-to-voltage transducer.

Due to the subtractive nature of the negative-feedback signal, the system is stable. The output voltage of the operational amplifier, called the error signal, is the difference between the reference and feedback voltages and drives the servo amplifier unit in Fig 1. In addition, the output of the servo amplifier drives the servo motor to the desired speed. A third input to the operational amplifier summing-network, the gain-control potentiometer, is provided to increase the system's sensitivity and power transfer.

The servo motor is powered by a transistor amplifier within the servo amplifier unit. Current can be supplied to either the field or armature windings of the motor, but the most accurate control results from an armature connection. The tachometer or tachogenerator connected to the motor shaft generates a voltage proportional to the speed of the shaft multiplied by a tachometer constant. In this case, the constant is determined experimentally and equals 2.55 V/1000 rpm. Thus, when the motor shaft spins at 1000 rpm, the tachometer generates 2.55 V. This voltage is subtracted from the reference voltage at the summing junction.

An analog system of this type can be adapted to digital control techniques by digitizing the voltage variations and writing the feedback loop in software. Digitizing the control voltages involves the design of a control interface whose software is available in a number of different forms. The software's function is to successively compare the feedback and reference signals and generate a compensation signal to the motor-drive circuitry.

If the control system is simple, machine language programming may be adequate. However, a user should be aware that problems can arise in writing and debugging the program, and that modifications to the program can be difficult. In most cases, it is wiser to rely on high level language (Basic, Pascal, etc) programming since it permits more attention to be given to control operations rather than causing concern about the information flow in the processor's registers and internal memory.

Converting voltage values
To digitize control-system feedback signals, an A-D converter of the type shown in Fig 2 is used. The converter, a Teledyne 8703, is a dual-slope type. A low logic-level on the Enable input line activates the device and a positive-going pulse on the Initiate Conversion line starts A-D conversions. The analog input voltage to be converted is applied to the 8703's Vin line.

<table>
<thead>
<tr>
<th>Task</th>
<th>Time required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floating point addition</td>
<td>18.5 to 202.5 µs</td>
</tr>
<tr>
<td>Floating point multiplication</td>
<td>63.5 to 446.0 µs</td>
</tr>
<tr>
<td>Floating point to fixed point conversion</td>
<td>25.0 to 109.0 µs</td>
</tr>
</tbody>
</table>
The converter contains a zero-adjust terminal that connects through a fixed resistor to a potentiometer. This permits a user to adjust the converter output to 0 V when a 0-V signal is present at the analog input. The I_{Bias} input serves to establish the bias current for the converter's internal circuitry. With a reference voltage of −15 V and a 750 kΩ current-limiting resistor, the maximum current that can be drawn by the chip during a conversion is a −20 µA. The eight output lines of the converter connect to the control system data bus, which feeds, in turn, into a system I/O port.

Fig 3 illustrates the control system's (D-A) conversion system, centered around the DAC-100 D-A chip. Internally, the DAC-100 has a series of current switches that are activated by data on the data bus. The current switches are connected to a highly accurate and stable R2R resistor ladder network. It is this internal resistor network that forms the basis of D-A conversions. A potentiometer connected between −15 V and the converter's full-scale adjust terminals permits a user to obtain a 0-V output for an all-logic 0 input.

The converter's output feeds into an AD 118A operational amplifier. This device is chosen for its accuracy, response, and fast slew-rate characteristics. Slew rate, in particular, is important because the input to the amplifier often changes at a fast rate. For the 118A, the slew rate is 6 V/µs—the output signal switches at a rate of 6 V in 1 µs. The
amplifier also provides excellent thermal stability. Another trimming adjustment is included on the amplifier to allow the output signal of the D-A system to be set to 0 V when the input to the system is found to be 0 V.

A second AD118A is included to invert the output of the first operational amplifier. All resistors in the system should be metal-film types having ±1 percent tolerance to ensure high accuracy, thermal stability, and low noise generation.

**A complete speed controller**

The schematic diagram of Fig 4 shows a complete microprocessor-based speed control system whose computing element is a Motorola M6800 8-bit microprocessor. The M6800 is not shown in Fig 4, but its interface device, the MC6820, is shown connecting to both the A-D and D-A converter subsystems of Figs 2 and 3 respectively. As an I/O port, the MC6820 peripheral interface adapter (PIA) interfaces the system data bus to the buses of both the A-D and D-A converters. The PIA is activated through a series of control signals sent by the microprocessor. Note that the summing amplifier and servo amplifier circuitry is the same as that of Fig 1.

The reference signal to the controller comes from an external source such as a keyboard. However, the feedback signal is available at the output of the A-D converter. The system software controls the subtraction of these two signals, and when the result is zero, the desired speed of the motor is attained and the system is under control.

The system of Fig 4 is very basic and can be varied in many ways. For example, it can be modified to include reversible speed control and even position control. Such modifications involve changes to the hardware and an efficient program written with high level software.
The CalComp line of electrostatic plotters.

You already know CalComp as the leader in pen plotters. Now, we've taken our reputation for reliability, commitment and support, and placed it on our complete line of electrostatic plotters.

CalComp's line of electrostatics gives you a choice of 11", 22" and 36" plotter/printers. Each is perfect for plot previewing at an affordable price, and is ideal for mapping, business charts, graphics and a wide range of other applications. And by using clear mylar media, you can also produce finished-quality drawings.

To make it as easy as possible for electrostatics and pen plotters to work together, CalComp also offers a family of 95X controllers. These unique and versatile controllers can drive up to eight electrostatic plotters with a pen plotter, freeing your host computer for more cost-efficient tasks.

Let CalComp's sales representatives and graphic consultants find the right electrostatic to fit your needs. Write us now, because we're placing our reputation on the line—for you.

CalComp, 2411 West La Palma Ave., P.O. Box 3250, Anaheim, California 92803. Or call (800) 556-1234, ext. 156. In California call (800) 441-2345, ext. 156.
It's a wonder anything ever gets finished. Fortunately, it doesn't have to be that way. Even though you're developing a complex system, the system development can be simple. And timely.

With development tools from Intel. The most complete, fully-integrated set of hardware and software development tools in the industry.

You can work in a variety of high level languages — PL/M, Pascal, FORTRAN or C — from the very beginning. And our tools will keep you at that high level where you're most productive.

Take our PSCOPE debugger. It lets you detect and patch all program errors at the source level in your choice of PL/M, Pascal, or FORTRAN. Then you recompile just once.

Same for our LINK utility.

It allows someone to work in Pascal and someone else to work in PL/M, and then makes short work of the integration.

Very slick. But you're also going to love SVCS and MAKE.

SVCS stands for Software Version Control System and it functions as a data base manager that automatically logs who makes changes, when, and why.

Then our MAKE utility automatically finds the correct versions of each module, automati-
cally recompiles those modules that need it, and produces the complete, correct system. Automatically, of course.

Which brings us to PICE, our Integrated Instrumentation and In-Circuit Emulation System. PICE uses the same high level human interface as PSCOPE, so you don't have to learn a new one. It also emulates at full speed, real time, to eliminate any tricky little timing problems. And of course, it supports every processor in the iAPX86 family.

We also have a variety of Intellec Development Systems for them to plug into.

Not to mention the best in project management and control, our Network Development System, NDS II, allows you to share resources and communicate throughout the process. What’s more, these tools are available at the same time as the silicon they were made for. Engineering assistance and training workshops are available as well. As is a lot more information.

Just call (800) 538-1876. In California, (800) 672-1833. Or write Intel, Lit Dept L-8, 3065 Bowers Ave., Santa Clara, CA 95050.

But do it soon. Whoever finishes first wins. Everybody else just finishes.
Quality means more when it comes from Fujitsu.
You get the latest Winchester disk drive technology. A total vertically integrated manufacturing operation. And a solid reputation built on more than 15 years experience.

Our broad base of customers have come to rely on this level of quality over the years. Quality that's exclusively Fujitsu.

For more information contact the Fujitsu America Sales Office nearest you. Northwest: (408) 988-8100, East Coast: (617) 229-6310, Southwest: (714) 558-8757, Europe: 44-1/493-1138.

<table>
<thead>
<tr>
<th></th>
<th>A 14-INCH</th>
<th>B 10½-INCH</th>
<th>C 8-INCH</th>
<th>D 8-INCH</th>
<th>E 5½-INCH</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAPACITY (M Bytes)</td>
<td>84 / 168 / 336</td>
<td>474</td>
<td>48 / 84 / 168</td>
<td>24 / 48</td>
<td>7 / 13 / 20 / 27</td>
</tr>
<tr>
<td>AVG.POSITIONING TIME (ms)</td>
<td>27</td>
<td>18</td>
<td>20</td>
<td>70</td>
<td>83</td>
</tr>
<tr>
<td>TRANSFER RATE (K Bytes/s)</td>
<td>1,012</td>
<td>1,859</td>
<td>1,229</td>
<td>593 / 1,200*</td>
<td>625</td>
</tr>
<tr>
<td>INTERFACE</td>
<td>SMD</td>
<td>Modified SMD</td>
<td>SMD</td>
<td>SA4000</td>
<td>ST506/SA4000</td>
</tr>
<tr>
<td>POSITIONING METHOD</td>
<td>Rotary Voice-Coil</td>
<td>Rotary Voice-Coil</td>
<td>Rotary Voice-Coil</td>
<td>Buffered Stepper</td>
<td>Buffered Stepper</td>
</tr>
</tbody>
</table>

*48 M Bytes Configuration available only in 1200 K Bytes/s
Special report on data communications

147 Introduction

149 Networks expand as PBXs get smarter
by Nicolas Mokhoff—Local area networks integrate with private branch exchanges as data acquires a new partner in voice.

175 Standardizing upper-level network protocols
by David Berry—Data communication networks will communicate more efficiently once standards are defined for the upper-level layers of the International Standards Organization seven-layer model.

191 PBX-based LANS: lower cost per terminal connection
by Henry Wurzburg and Steve Kelley—Universal digital loop transceiver chip set offers attractive alternative to coaxial and fiber optic based local area network.

203 A simple gateway for odd networks
by Joonees K. Chay, Jeff Seltzer, and Naseer Siddique—Ethertnets talk to token-bus baseband networks via a gateway implemented with LSI chips.

215 Controller and micro team up for smart Ethernet node
by James A. Fontaine—The LANCE chip adapts 16-bit power of micro to form a true Ethernet connection.

231 Establishing the micro-to-mainframe connection
by Dan Erlin—The 3270 emulator accommodates coaxial link with RS-232 serial data on the same card.
The General Electric 3000 family of printers has become an industry leading product. But now, this popular printer series has a new name, because the Data Communication Products Department of GE is now an independently owned company called Genicom.

At Genicom today, we offer the same complete line of printers we offered while a part of General Electric. We have the same facilities, the same nationwide service network, and the same corps of experienced employees... only the name has changed.

Above all, Genicom offers you the same reliable product quality you've come to expect from us over the years. Our Genicom 3000 printers feature outstanding performance for end-users as well as superior flexibility for many OEM's, distributors, retailers and dealers. There are 3000 models with speeds from 40 to over 400 cps. Single or dual mode printing. Type quality from EDP to NLQ. Multi-color printing. Graphics. Selectable type fonts, American craftsmanship and more. There are even 3000 family printers for personal computers... ideal for business needs.

We're proud of the excellent brand reputation we established under General Electric. But now we're going to make a new name for ourselves by bringing you more innovations, and more of the reliable quality you've always found in each of our products.


For the solution to your printing needs call TOLL FREE 1-800-437-7468
SPECIAL REPORT ON DATA COMMUNICATIONS

To switch or not to switch, that is this year's choice for the computer designer. Is a digital private branch exchange (PBX) really needed to switch data and voice throughout a facility, or does a local area network (LAN) suffice for today's communication needs? The answer, of course, depends on the individual need. More and more applications require communication of both high speed data and digital voice and, in some cases, even digitized video. These applications necessitate handling a large amount of data and currently are being wooed by both LAN and PBX vendors, each of whom claim to provide the "total" solution to short-distance communication needs.

A good amount of this short-haul communication technology is being geared for offices where some kind of PBX already routes telephone traffic. Now that switching technology has graduated its third generation, a new breed of voice/data digital PBXs—the fourth generation—is starting to be launched to effectively compete with LANS for office applications.

This special report examines the technology behind the upcoming fourth-generation PBXs while highlighting the major trade-offs among various media access contention schemes used by major vendors, including IBM and AT&T Information Systems. In addition, the report details a typical fourth-generation digital PBX to reveal a natural merging of LAN technology in a PBX configuration. Finally, the report reviews the latest trends in LAN developments.

Five articles that are variations on the PBX/LAN theme complement the report. The engineers of four established semiconductor companies and a startup venture present the scope of state-of-the-art developments. David Berry of Advanced Micro Devices reviews standards for protocols needed to communicate between different terminals that use the Open Systems Interconnection (OSI) model. He reviews the ongoing protocol standardization efforts of various organizations for the upper levels of the OSI model.

Two authors from Motorola, Henry Wurzburg and Steve Kelley, show how a digital PBX can be transformed into a LAN by using a universal digital loop chip set. The allotted 64-kbit/s data rate adequately meets the effective 40-kbit/s data rate of current LANS when these are fully loaded, and does so at a lower cost per connection, according to the two authors. Signetics' three authors—Joonees Chay, Jeff Seltzer, and Naseer Siddique—propose to link Ethernets that use a CSMA/CD contention scheme with token-bus networks that use a token to get on the bus. Their gateway controller chip set, in theory, allows Ethernet-based offices to talk to realtime response token-bus LANS in factories.

As more Ethernets are installed and more users gain access to Ethernet media, more intelligence must be added to the nodes to contend with the added data congestion. Mostek's James A. Fontaine offers a solution to the congestion problem that combines a 16-bit microcomputer with an Ethernet controller chip to form a smart node.

Local intelligence by itself can be a self-defeating goal if the processed information stays within the confines of that terminal. As IBM PCs spring up wherever the appetite for data warrants them, microcomputers must be linked to mainframes to become effective corporate team players. As such, the latest trend for some startup companies is to develop the tools for the micro-to-mainframe link. Forte Data Systems' Dan Erlin is one such entrepreneur who discusses his product—an IBM PC plug-in board and associated software—which links the PC, operating as an IBM 3270-type terminal, directly to a mainframe via a serial RS-232 coaxial cable.

Thus, from the highest levels of protocol to the lowest wired connections comes a myriad of communication challenges for the computer designer to solve. Now is the time to meet these challenges by choosing from the crop of communication technologies becoming available.

Nicolas Mokhoff
Senior Editor
Hi~

resolution, low cost graphics should be more than a retrothought.

Why settle for a low resolution retrofit graphics terminal when you can have a VISUAL high resolution terminal with quality and reliability built in. And at a cost that makes retrofits overpriced.

The VISUAL 500 and VISUAL 550 emulate the Tektronix 4010/4014 but cost only about half as much. And they provide 585(V) x 768(H) resolution for sharp text and graphic display on a large 14” screen without the need to add boards or change the CRT. This superior resolution offers the ideal vertical to horizontal dot density ratio of 1:1 for balanced images and reduces the “stairstep” effect you get with most retrothoughts.

The VISUAL 500 provides selectable emulations of the DEC VT52, Data General D200, Lear Siegler ADM3A, and Hazeltine 1500 terminals. The VISUAL 550 is DEC VT100 protocol-compatible as well as a character or block mode terminal which complies to the ANSI X3.64 standard.

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.

VISUAL 500/550

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.

Why settle for a low resolution retrofit graphics terminal when you can have a VISUAL high resolution terminal with quality and reliability built in. And at a cost that makes retrofits overpriced.

The VISUAL 500 and VISUAL 550 emulate the Tektronix 4010/4014 but cost only about half as much. And they provide 585(V) x 768(H) resolution for sharp text and graphic display on a large 14” screen without the need to add boards or change the CRT. This superior resolution offers the ideal vertical to horizontal dot density ratio of 1:1 for balanced images and reduces the “stairstep” effect you get with most retrothoughts.

The VISUAL 500 provides selectable emulations of the DEC VT52, Data General D200, Lear Siegler ADM3A, and Hazeltine 1500 terminals. The VISUAL 550 is DEC VT100 protocol-compatible as well as a character or block mode terminal which complies to the ANSI X3.64 standard.

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.

VISUAL 500/550

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.

Why settle for a low resolution retrofit graphics terminal when you can have a VISUAL high resolution terminal with quality and reliability built in. And at a cost that makes retrofits overpriced.

The VISUAL 500 and VISUAL 550 emulate the Tektronix 4010/4014 but cost only about half as much. And they provide 585(V) x 768(H) resolution for sharp text and graphic display on a large 14” screen without the need to add boards or change the CRT. This superior resolution offers the ideal vertical to horizontal dot density ratio of 1:1 for balanced images and reduces the “stairstep” effect you get with most retrothoughts.

The VISUAL 500 provides selectable emulations of the DEC VT52, Data General D200, Lear Siegler ADM3A, and Hazeltine 1500 terminals. The VISUAL 550 is DEC VT100 protocol-compatible as well as a character or block mode terminal which complies to the ANSI X3.64 standard.

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.

VISUAL 500/550

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.
NETWORKS EXPAND AS PBXs GET SMARTER

Local area networks integrate with private branch exchanges as data acquires a new partner in voice.

by Nicolas Mokhoff, Senior Editor

In communication systems, 1984 may be the year of integration. True voice/data integration has been the quest of computer and communication design engineers since the beginning of the digital era. When the concept of digitizing audio signals was first proposed for data transmission and subsequently for voice transmission, and both had finally materialized, it remained only for designers to find an economical means for merging the two into a packet-format stream of information. While integrated voice/data networks have been designed for wide area network applications, and even for satellite transmission, the proliferation of remote processing applications recently prompted designers to develop local communication networks with integrated voice/data transmission capability.

Today, two mainstream technologies allow local distribution and communication of digital voice and data—private branch exchanges (PBXs) and local area networks (LANs). Sometimes the two technologies compete, and at other times they complement each other.

Integrated voice/data PBXs allow simultaneous switched voice and data communications without the use of modems. In any switching system, the flow of information passes from the point of origin to potential destinations via a switch that significantly reduces the total number of required paths. Several voice/data communication switching schemes represent alternatives to dedicated point-to-point data communication connections. These include multidrop, computer terminal-to-host connections; bus-type LANs (Ethernet, etc); and PBX-type LANs. Each of these schemes may have different architectures, media, speeds, bandwidths, protocols, and formats. The objective of each scheme is communication between terminals and host processors, between host processors, or between terminals.

The PBX's traditional function is to connect a number of telephone lines supporting telephone sets to each other and to a lesser number of trunks that connect the PBX to the outside telephone world. Each telephone line and trunk typically require one port or time slot on the system in order to operate.

As the PBX evolved from an electromechanical device to a computer-based, stored-program control
system using digital technology internal to the switch, it became evident that the PBX could become a vehicle for switching digital data between processors and peripherals without using modems. Potential benefits included removing modem cost, increasing transmission speed, and improving transmission quality and reliability. Also, access to the data processing environment could be accomplished without additional wiring and hardware.

Ideally, voice and data transmissions are multiplexed over a single twisted pair of wires, requiring only one port at the PBX. Data communication capability can then be perceived as an added feature gained with little incremental cost, since at least one twisted pair and one port are already required on the system for voice communication.

Implementing an integrated voice/data transmission efficiently depends on several variables: the number of channels and type of media needed to connect each telephone set or data device to the switch; the number of ports used at the switch; and the additional hardware needed in the system and at the terminal to accomplish integrated voice/data communication. These variables are usually found in the succeeding second-, third-, and fourth-generation PBXs.

Second-generation PBXs are digitally stored program-control switches designed for voice communication. Adding data communication capabilities was actually an afterthought. An example of a second-generation PBX is Northern Telecom's (Nashville, Tenn) SL-I. The same two twisted pairs that were originally installed for voice communications adapt for data transmission by adding a line card to the PBX for each data terminal, and a data interface device at the terminal site. An additional port is used for each data device. This type of PBX supports data transmission speeds up to 9.6 kbits/s and can potentially handle up to 56 kbits/s.

Third-generation PBXs were designed to support simultaneous voice and data transmission, either over the same twisted pair, or over parallel twisted pairs, without using an additional port. An example is the InteCom (Allen, Tex) IBX system, which requires two twisted pairs but only uses one port on the PBX. An additional circuit board is required at the switch and in the telephone set. Currently, these systems operate at up to 19.2 kbits/s and are expected to be available for rates to 56 kbits/s.

Fourth-generation machines debut

Last year, a handful of companies announced fourth-generation switches. Rolm Corp (Santa Clara, Calif), NEC Information Systems (Lexington, Mass), and CXC (Irvine, Calif) have designed systems that combine a PBX and a bus-type LAN.

Ztel (Wilmington, Mass), on the other hand, designed its Private Network Exchange, or PNX, from the beginning as an integrated voice/data network using a token-ring topology. Designers were able to fully integrate the voice features of a computerized PBX and high speed data into a single, unified system.

It made a lot of sense for Ztel to combine the two technologies. Several advantages are inherent in developing a PBX-based product. As opposed to installing coaxial cable, PBX wiring is already in place in most businesses, and the PBX voice functionality will always be required. Adding the LAN technology facilitates the linking of devices, such as facsimile and personal computers that require high speeds.

_One current trend is to use the PBX as a gateway to other network types._

According to Ztel, combining the PBX and LAN in the PNX lowers the cost of both voice and data communications, yields a more compact system, offers more features, and ensures better reliability and serviceability. These improvements are accomplished through the use of custom LSI circuits, software implementation techniques, and new types of fault tolerant, distributed system architecture.

The PNX system software strictly follows the International Standards Organization's (ISO) Open Systems Interconnection model and is implemented in the high level C language. This allows system designers to easily customize the PNX for specific industry applications. Currently, no other PBX allows this level of accessibility, according to Ztel.

Ztel made a radical departure from typical PBX architecture. The PNX architecture reflects current trends in the corporate environment. In a typical PBX star architecture, telephones and terminals connect to a central processor. The information flows through some common carrier to its destination, where it is then distributed to the proper recipient. This typical PBX environment is changing very rapidly. While the PBX function will always be needed for voice communications, the growing trend is to add productivity aids such as electronic mail and calendaring to the PBX.

Another trend is to use the PBX as a gateway to other network types. A gateway is needed when voice and data information exit a facility. Add to this a growing marketplace that requires significantly more information. While one data device currently serves every 10 to 15 office workers, within a few years one device will be required for five (or fewer) workers. With this explosion in devices, implementing separate communication solutions becomes very expensive.

The only solution that supports an integrated decision-making process within a corporation is total network communication that starts within a building, extends to a cluster of buildings, then
PERFORMANCE ARCHITECTURE:
Data Acquisition and Control.
Multi-User Computation.
High-Performance Graphics.
All Simultaneously.

Masscomp’s unique triple-bus Performance Architecture delivers unequalled system price/performance. With its dual-processor CPU and up to 7 megabytes ECC memory, the Masscomp MC-500 offers scientists and engineers outstanding computation power. With the addition of Masscomp-designed floating-point and array processors, throughput is even further enhanced.

The MC-500 runs a virtual memory, real-time UNIX™ operating system with Ethernet™ support. Supported languages include C, FORTRAN 77, and Pascal-2™. The Quick-Choice™ multiple-window user interface offers menu-driven access to system functions.

Key system capabilities include:

DATA ACQUISITION AND CONTROL
- Bit-slice Data Acquisition and Control Processor
- One million 12-bit analog samples/second
- One microsecond external-event response

MULTI-USER COMPUTATION
- 32-bit CPU with 4K byte cache
- 16 megabyte virtual address space
- 7 millisecond 1024-point complex FFT

HIGH-Performance GRAPHICS
- Independent 32-bit graphics processors
- 1024 x 800 x 2 x 1 pixel monochrome graphics
- 832 x 600 x 2 x 10 pixel color graphics

For more information on how the MC-500 is delivering results in industrial, university, government, and medical applications, call 1-800-451-1824.

MASSCOMP
One Technology Park
Westford, Massachusetts 01886
TWX: ESL 196520
Telex: 704353
Cable: MASSCOMP

Winner of the 1983 I-R 100 Award as one of the most significant technical products of the year.

Performance Architecture and Quick-Choice are trademarks of the Massachusetts Computer Corp. UNIX is a trademark of Bell Laboratories. Pascal-2 is a trademark of Oregon Software. Ethernet is a trademark of the Xerox Corp.

CIRCLE 75
continues nationally and internationally. Without a totally integrated network, it will be more difficult to achieve the information flow and transfer required to support decision making.

The PNX architecture shines

Ztel's PNX design was based on several determinations about the requirements such a network should meet. Ztel's engineering managers decided that their system needed voice communications equal or superior to a traditional PBX system, or it would be unacceptable. The system required great reliability because all of a company's communication requirements—voice, data, image, and video—would move through one system. Of course, it would incorporate local area networking as well.

This LAN would have to be compatible with some accepted standard. Adopting the IEEE 802.5 token-passing standard was a major step in this direction, especially since IBM has opted for a version of that standard for its upcoming LAN. Ztel engineers selected a token-ring scheme after evaluating both carrier sense multiple access/collision detection (CSMA/CD) and token-bus standards, and rejecting both because of performance inadequacies and reliability problems. Each ring in the PNX network operates at the IEEE 802.5 standard rate of 10 Mbits/s—the minimum rate needed for voice transmission.

In a token-ring network, the transmission medium forms a circle through each connected device. Information is communicated in sequential order around the ring. Devices transmit and receive information by appending or extracting messages from the medium as tokens circulate through the network.

The PNX digitizes the data and analog information as it enters the network. Data is also formed into packets, and these packets are intermixed with packets from other transmissions and routed through the network. They therefore make efficient use of available bandwidth.

To implement a LAN based on a token-passing protocol with a ring structure, Ztel added devices to the system processing units (SPUs) to provide the functionality of a data switch. Each SPU can perform three types of processing: switch processing to handle and connect voice and data calls; applications processing to perform tasks such as least-cost routing, directory look-up, or other value-added applications; and data conversion processing to format data into packets and provide protocol conversion between different types of equipment. SPUs can be added to expand the system. The failure of any one processor will not shut down the system; its work load can be distributed among other processors.

Devices such as phones and terminals can be interfaced to the SPU via a standard quad telephone line up to 5000 ft long that carries two information channels. The Ztel channel structure includes one digitized voice channel, one data channel, and two control channels of the correct size to guarantee correct data operations at 56 kbits simultaneously with voice.

Foreign computer equipment meeting protocol requirements can be attached directly to the token ring. This is done by using simple wall connectors, as defined by the IEEE 802.5 standard.

The PNX's very high throughput is due to its deterministic nature, which allows prediction of the worst-case performance of the network independent of its load. This is a valuable characteristic in both telephone and data communications. A deterministic network can achieve transmission rates high enough for transmission of video, graphics, and file services without fear of deteriorating performance.

An even higher throughput rate can be achieved by using multiple rings, which may be installed according to the required level of service. Ztel's initial release allows up to 40 rings to operate in one PNX system, with each ring operating at 10 Mbits/s, for total throughput of 400 Mbits/s. Thus, the PNX has the throughput potential to handle extremely high data rates that will be required in the near future by automated equipment. In addition, a high level of system reliability is possible with a multiple-ring network. If one ring fails, backup mechanisms redistribute that ring's traffic over other active rings.

As more bandwidth is required, more rings can be added incrementally at relatively low cost. While packaging artificially imposes the current limit of 40 rings, the architecture allows hundreds of rings. According to Ztel, future implementations will remove this packaging barrier.

PNX has both packet and circuit rings. The totally transparent circuit rings handle digitized video—one 10-Mbit circuit can handle 113 simultaneous conversations, each in a 64-kbit/s slot. Any data call can also be put on the ring but transmitting a 4800-bit/s data transaction over a 64-kbit/s slot is considered wasteful. The circuit ring can also be used to transmit video information.

LAN-compatible devices are connected to the packet ring, which transfers packetized data from source to destination. The PNX determines whether the circuit or packet ring will be used, and packetizes the information accordingly. Depending on the network's characteristics, there may be any number of circuit and packet rings.

IBM rings in new LAN

Because of its size, IBM will tend to dominate the networking market with the architecture and standard that it chooses. IBM also has a large commitment in its systems network architecture (SNA),
The control mechanism for regulating data flow in a ring topology is generally based on use of a token passed sequentially from node to node around the ring. The token contains a 1-bit indication that it is "free" (T = 0). This single free token circulates on the ring, giving each node in turn an opportunity to transmit data when it receives the token (Fig 1). A node that has data to transmit can capture the free token, change the token status to busy, and begin data transmission. The node that initiates a frame transfer must remove that frame from the ring and issue a free token upon receipt of the physical header. This allows other nodes an opportunity to transmit.

If a node finishes transmitting the entire frame prior to receiving its own physical header, it continues to transmit idle characters (contiguous Os) until the header is recognized. This ensures that only one token (free or busy) is on the ring at any given time.

IBM engineers chose the token-access control protocol because they say that it provides uniform access to the ring for all nodes. A node must release a free token after each transmission and is not allowed to transmit continuously (beyond a maximum frame size or preset time limit) on a single token. All other nodes on the ring will have a chance to capture a free token before that node can capture the token again. In some system configurations, it may be necessary for selected nodes, such as bridges or synchronous devices, to have priority access to the free token.

Setting priorities

A priority mode is used along with reservation indicators to control this access mechanism. Various nodes may be assigned priority levels for gaining access to the ring. A selected node can then capture any free token that has a priority mode setting equal to or less than its assigned priority. The requesting node can set its priority request in the reservation field of a busy token if the priority of that node is higher than any current reservation request.

The current transmitting node must examine the reservation field and release the next free token with the new priority mode indication, but retain the previous priority level for later release. A requesting node uses the priority token and releases the new token at the same priority so that any other nodes assigned that priority also have opportunity to transmit. When the node that originally released the priority free token recognizes a free token at that priority, it then releases a new free token at the level that was interrupted by the original request. Thus, the lower priority token resumes circulation at the point of interruption.

In the IBM LAN, normal token operation is monitored by a token monitor that is perpetually active in a single node on the ring. This function can be performed by any node on the ring and is necessary to initiate the proper error recovery procedure if normal token operation is disrupted. This includes the loss of a free token or the continuous circulation of a busy token, both of which prevent further access to the ring. The monitor function exists only for token recovery and does not play an active role in the normal exchange of data frames.

The ability to be an active token monitor exists in all active nodes attached to a ring. These other nodes maintain a standby monitor status and are prepared to become the new active monitor should a failure occur in the current active monitor. The standby monitors are essentially monitoring the ring to detect abnormal ring operation that could occur whenever the active monitor fails. Detection of an error condition by any standby monitor initiates a recovery procedure that allows it or one of the other nodes to become the new monitor.

While the LAN provides a basic transport mechanism for data transfer among nodes within the network, it does not provide all of the functions necessary for two nodes to manage and conduct a
meaningful two-way information exchange. The same higher level communication protocols implemented to control data transfer across public data networks are also applicable to data transfer across a LAN. Both the SNA concept and the ISO reference model separate network functions into layers to facilitate the description and implementation of the protocols. The SNA protocols can be implemented for managing information flow within a LAN as in any other SNA environment.

The functions of the lowest physical layer are unique to the particular transport mechanism implemented—whether it be a communication loop, a multidrop bus, or a token ring. The model's physical layer encompasses the basic functions associated with placing electrical signals onto the transmission medium. This includes such fundamental operations as signal generation, phase timing along the ring, and encoding of signal information using the differential Manchester scheme. These operations are performed within the ring interface adapter at each active node in the network.

The next higher layer, data-link control, is traditionally independent of the actual physical transport mechanism. It performs the functions necessary to ensure the integrity of the data reaching the layers above the data-link control level. The IEEE 802 Committee and the European Computer Manufacturers Association (ECMA) have proposed that, for LANS, the data-link layer of the ISO model, which corresponds to the same layer of the SNA, be further subdivided into two functional sublayers: logical link control (LLC) and media access control (MAC). This functional decomposition essentially separates functions into hardware dependent and hardware independent. Thus, compatibility between SNA and the ISO model implementation is ensured.

Proposed data-link sublayers

The MAC sublayer of a token-ring LAN would include functions associated with frame and token transmission that can be, but are not necessarily, performed by the interface adapter in each node. The LLC sublayer would include those functions unique to the particular link control procedures associated with the attached node and not the medium access one. This would permit various logical link protocols to coexist on a common network, such as a SNA-compatible token-ring LAN, without interfering with one another. Logical links are established primarily to ensure data integrity to the higher layers. Multiple LLCs may exist within each node. In these instances, a link multiplex function within the LLC layer directs incoming frames to the appropriate LLC task and also provides the correct address information for outgoing frames. LLCs are logically associated within nodes.

IBM engineers, like those at Ztel, do not rule out multiple-ring LANS in cases where data transfer requirements exceed the capacity of a single ring, or when the attached nodes are widely dispersed (eg, in a multifloor building or campus environment). These large networks may typically have several rings with 100 to 200 nodes per ring. In those cases, two rings can be linked together by a high speed switch, or bridge, which would provide logical routing of frames between the rings based on destination address information contained in the header of the frames.

A bridge can also change transmission speed from one ring to another. Each ring retains its individual identity and token mechanism, and could therefore stand alone in the event the bridge or another ring is disrupted. The bridge's interface to a ring is the same as any other node's interface, except that it must recognize and copy frames with a destination address for one of the other rings within the network. Also, several frames can be temporarily buffered in the bridge while awaiting transfer to the next ring.

The local network can be further expanded to meet larger data capacity requirements by interconnecting multiple bridges. This results in a hierarchical network in which multiple rings are interconnected via bridges to a separate high speed backbone. The backbone itself can be a high speed token ring or it may be a token-access bus link, such as a channel within a broadband cable TV system. The address field format is structured to designate the specific ring to which a node is attached, thereby facilitating the routing of frames through bridges.

Finally, a gateway node provides an interface between the token-ring LAN and a wide area network. Here the gateway node allows long-distance communication between nodes within different LANS. The gateway performs the necessary address translations, as well as speed and protocol conversions necessary to interface the LAN to these various transmission facilities. A gateway could also be used as an intermediate node between a token-ring LAN and nodes located in either a CSMA/CD- or PBX-based LAN.

A ring interface adapter at each node performs the primary functions associated with token recognition and data transmission. Advances in VLSI technology make it possible to delegate a large portion of the communication function to the adapter itself, thus freeing the node from this processing. The adapter handles basic transmission functions including frame recognition, token generation, address decoding, error checking, buffering of frames, and link fault detection.

There may be instances where a particular device with an incompatible communication interface is to be attached to the LAN. In such cases, a separate interface converter can be attached between the
New CMOS filters create 5 V 300-baud modem IC family.

Introduction of the MC145440 and MC145441 CMOS modem filters completes Motorola's creation of the first 5 V 300-baud IC modem family. These high-technology ICs perform the precision filtering required for Bell 103 and CCITT V.21 applications without additional external components, simplifying the design and manufacturing. Significant additional circuit-complexity and board-space reductions are achieved because these filters can operate on a single 5 V power supply.

Three modem options tailored to your application.

1 Lowest cost.

Either new filter pairs with the MC14412 CMOS modem in the industry's lowest-cost IC modem chip set, dollars less than even the closest multiple-supply, single-chip IC alternative. Single-supply operation and standard clock frequencies keep it simple and inexpensive.

2 Highest performance.

Teaming the recently introduced high-performance MC145445 CMOS modulator/demodulator with either new filter gives you a modem with the lowest bit error rate in the IC industry. Here, too, single supply operation enhances design simplicity and cost effectiveness.

3 Versatility—more bells and whistles.

For the most versatile 300-baud modem, with features galore, put the MC6860 modem to work with the MC145440 filter. Switch-hook detect, ring indicator, automatic answer and disconnect, and answer phone indicate output are typical of the options provided with this approach. It also benefits from single supply and standard clock frequencies.

Motorola covers 300-baud modem applications.

<table>
<thead>
<tr>
<th>Device</th>
<th>Protocol</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC14412/145440</td>
<td>BELL 103</td>
</tr>
<tr>
<td>MC14412/145441</td>
<td>CCITT V.21</td>
</tr>
<tr>
<td>MC145445/145440</td>
<td>BELL 103</td>
</tr>
<tr>
<td>MC145445/145441</td>
<td>CCITT V.21</td>
</tr>
<tr>
<td>MC6860/145440</td>
<td>BELL 103</td>
</tr>
</tbody>
</table>

All this, plus Motorola’s quality and reliability.

This 300-baud modem family has it all—lowest cost, highest performance, great versatility and the right chip set for any application. It’s from Motorola, recognized as a leader in CMOS and an innovator in communications circuits. Quality and reliability have been hallmarks of Motorola semiconductor products for over 30 years.

Send the completed coupon or write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036 for additional 300-baud modem details. Contact any Motorola sales office or authorized distributor for information, or call 512-928-6892 to speak with a marketing engineer.
device and the token ring to perform the conversions that are required to send and receive data over the LAN.

The IBM-TI affair

IBM is working with Texas Instruments (Dallas, Tex) to develop an adapter for a token-ring LAN. Requirements for an adapter to a LAN are essentially independent of the type of local network used. Engineers from both companies concluded that the requirements can be summarized as follows: performance, functionality, hardware and software compatibility, error detection and isolation, flexibility, quality, reliability, and cost.

Obviously, the adapter must meet serial data communication rates specified for the LAN. Due to frequency versus distance trade-offs, however, this rate should vary to allow longer distance connections. The IEEE 802 Committee has recognized this by standardizing a range of data communication speeds. For token-ring networks, the data transmission rate exceeds 10 Mbits/s. The VLSI architecture of an adapter should also accommodate the range of functions adapters will include, but partition the interface breaks for each increment of functionality at cost-effective points.

The two companies' engineers considered two approaches for their LAN adapter: a closely coupled design and a controller architecture design. In the closely coupled approach, the LAN peripheral coexists on the system bus with main memory, the host processor, and other peripherals. This environment leads to the LAN buffers for transmission and reception of data and the LAN linkware (or lower level software) sharing main memory with the attaching product operating system and application code. The host processor provides bandwidth to support the processing on low level interrupts and the execution of low level software.

Making the closely coupled configuration fit the initial adapter requirements resulted in many drawbacks. In the face of these drawbacks, TI engineers opted for a controller approach. The integrated design includes an engine, ROM, scratchpad memory, and flexible system interface (Fig 2). As a result, adapter requirements are met. System performance is isolated from the capabilities of the attaching product host processor and the system memory speed. This puts buffering of data flows between the host microprocessor and the asynchronous events on the LAN. Rapid-response interrupt processing necessary to support LAN traffic is also separated from the host.

The software required by the adapter for response-intensive low level functions resides primarily in the adapter processor memory space. As such, it does not require integration with the operating system. The very nature of a controller design is to isolate the function from a given hardware processor bus.

This allows interface of a broad range of processor types, thereby increasing the flexibility of the architecture for users.

Significant software is required just to support the lower levels of the data communication hierarchy. This software is integrated into the LAN adapter, ensuring that different vendors' software will act the same in different processor/memory system environments at the peer levels supported in the LAN adapter chip.

A high level of error detection and isolation capability is built into the adapter. By isolating the engine and control memory of the adapter from the host processor, the LAN adapter can execute diagnostics independent of the host. The adapter can also alert a LAN management facility that its attaching product is having a problem, thereby requesting reconfiguration.

By integrating the design of an engine and control memory from the beginning, operating cost and initial cost are lower than if a closely coupled architecture were used, according to TI engineers. Life cycle costs for end users are lower through a high level of integrity built into adapters of attaching products—this raises the network's overall availability. Exceptional fault isolation capabilities ensure rapid service, thereby also reducing cost. These features reflect through to the overall network level, resulting in a connection facility of high performance and availability with a very aggressive life cycle bit transport cost.

The adapter chip meets the ring transmission performance requirements, with speeds over 10 Mbits/s in full-duplex mode. With two DMA channels for transmit and two for receive, it is capable of receiving back-to-back frames on the ring.

Also, the adapter implements all protocol features. Extensive internal control code and data
If you've been waiting for a supermicro with UNIX® System V on a 68010-based processor, stop. Introducing the Callan Unistar™ 300. It's the single best supermicro you can buy. For a couple of reasons: One, the 10MHz 68010 CPU. It's the newest, fastest, best. It crunches numbers in a snap. And works beautifully with the new UNIX.

Two, the new UNIX System V. It's faster than UNIX System III. On the Unistar 300, it supports a host of languages. And when it comes to portability, flexibility and system support, nothing comes close.

There's more. The Unistar 300 allows for expansion to 172M bytes of high-speed disk storage with integral tape backup—all within one enclosure that easily fits under a desk.

Its convenient 12-slot Multibus® chassis lets you easily add options like networking, communications, floating point array processors and more. Up to 2M bytes of main memory provide real power for every user. And nationwide service is available through ITT/Courier.

Unistar 300. Finally a supermicro with super everything. Available today from Callan. For more information contact Callan Data Systems, 2645 Townsgate Road, Westlake Village, CA 91361. (800) 235-7055. In California (805) 497-6837. TELEX 910 336 1685.

Callan Unistar

*Callan and Unistar are trademarks of Callan Data Systems. UNIX is a trademark of Bell Labs. Multibus is a trademark of Intel Corporation.
buffering permit the adapter to send and receive MAC frames without user processor intervention, significantly reducing the load on the user processor bus. In fact, recent experience has shown that the limiting factor in LAN communication is the software layering overhead of sending or receiving frames. By providing much of this software in silicon, TI's token ring adapter reduces this bottleneck.

The adapter meets hardware compatibility requirements by being able to select from a variety of popular microprocessor family bus timings and 8- or 16-bit data transfers. Bytes can be swapped by changing pins on the chip, thereby maintaining sequentially transmitted bytes in increasing system address order, regardless of the system byte-numbering conventions.

The IC meets quality goals by implementing a special single-cycle mechanism during chip testing that allows the test program to check for possible stuck-at faults. Extensive checking performed by each adapter ensures high ring reliability. Thus, faulty adapters can be quickly isolated and removed from the ring.

More token chips

Another semiconductor firm with a token-passing LAN adapter chip is Western Digital Corp (Irvine, Calif). And, Standard Microsystems Corp (Hauppauge, NY) has developed the COM9026 IC, principally for the ARCNET, a token-passing PBX/LAN system from Datapoint Corp (San Antonio, Tex). Western Digital's WD2840 Token Access Controller (TAC) is designed to interconnect distributed intelligent devices via a shared broadcast medium such as coax cable, air radio, or twisted-pair party line. The medium is shared by all attached stations using a token-passing protocol. A station is a microprocessor-based device incorporating a TAC and connected to the network.

The key design goal of the TAC was to free the system designer from data communication concerns. For example, once the TAC is initialized, the host microprocessor need never be concerned with the protocol. It simply processes frames addressed to it (the TAC filters out all others) and generates any messages it wants to send (the TAC sends them when the token is received).

Because all functions affecting network performance (e.g., token processing and acknowledgment generation) are inside the TAC, the user need not be concerned about the type of host processor. The TAC is designed to interface to a microprocessor system already busy with a specific application. An example might be the microprocessor common in today's CRT terminals. A microprocessor in a terminal already must scan the keyboard and perform limited editing. Its leftover processing power is sufficient to drive the TAC, since it only handles data to/from that specific terminal. If the microprocessor falls behind momentarily, it only affects that terminal, all others on the network continue to enjoy full speed operation. Thus, a network of TACs is not slowed by its weakest link.

Western Digital engineers based the WD2840 on a highly microprogrammed device that incorporates three microcontroller, a two-channel DMA subsystem (shared by the three microcontrollers), a shared register file, two timers, and high speed bit-oriented controllers on a single NMOS LSI device.

The DMA subsystem inside the WD2840 consists of two internal sets of sixteen bit address counters, two independent byte counters, and the required control/sequencing logic. The value of doubling up is to support the full-duplex operation needed for loopback testing. In addition, this architecture gives the device the ability to interleave data and control block accesses from memory for optimum efficiency.

Where AT&T stands

Meanwhile, AT&T Information Systems (Morristown, NJ) engineers have developed a unique LAN architecture that stays away from both established types—CSMA/CD and token passing. Their concept combines the advantages of both distributed and centralized LAN architectures. Moreover, the intended media is wide band fiber optic cable. AT&T engineers contend that although a bus is a good means for interconnecting many information-handling devices because it offers modular growth and can employ simple techniques (e.g., polling or contention) for traffic handling, it is somewhat limited. Most computers use buses to interconnect their internal components. However, when a bus is used for a LAN where the distance between devices can be significant, propagation delays must be taken into account. These delays complicate the methods used to govern traffic on the bus, say AT&T engineers, and in general, the transport efficiency of the bus declines as distance and delays increase.

The engineers chose a centralized bus to solve this problem. The bus is made very short to promote high efficiency. Physically, the bus is realized as the backbone of a cabinet to which relatively long access lines can be connected via plug-in interface modules. Interface modules can be designed to give access to various device types, such as terminals, hosts, or personal computers. Thus, the advantages of modularity and simplicity are retained, while the problem of efficient traffic handling is solved. Also, fiber optics can be used in a straightforward manner.

Designers based the system on a central node containing a contention bus, a broadcast bus, and a switch module as its fundamental elements (Fig 3). This node acts as a fast packet switch that provides virtual circuit service. All data enters via the contention bus and passes through the switch module to the broadcast bus. Interface modules connected
Fig 3 AT&T's answer for including both a centralized PBX-like network and a distributing ring or bus network is to combine the two into a network that includes a central node with a contention bus, a broadcast bus, and a switch as the essential elements. In such a network, each node acts as a fast packet switch that provides virtual circuit service.

to both buses buffer and form the data packets. The packet is then placed on the contention bus in the next available time slot. Time slots are defined via a separate clock bus controlled by a clock module. If more than one interface module tries to place a packet on the bus in a given time slot, the contention is resolved in a nondestructive manner and the winning module places its packet on the bus. Each packet contains a source address that is read by the switch module and translated into a destination address. The translation is stored in a table within the switch module where entries have been set by a prior call setup process. In this way, a virtual circuit service is provided. The switch module then places the packet and its destination address on the broadcast bus to be picked up by the appropriate interface module for delivery to the destination device.

AT&T engineers have ensured that the central node functions with minimal delay. Propagation delay on the bus is less than a bit period even at multi-megabit speeds. This ensures "perfect scheduling" of packet transmissions. No time is lost in the contention process, and there are no idle periods when packets are ready for transmission, so bus access delay is minimized. In addition to low bus access delay, the switch module performs address translation in hardware so it functions quite rapidly. The delay through the module is equivalent to that of a single-packet time or time slot on the bus. Time slots are very short because the bus speed is high. Packet lengths are kept relatively short to promote efficiency and flexibility of transport.

Many devices can access the central node. Instead of running separate lines, the data streams can be efficiently combined into a single high speed line for transport to the central node. Optical fiber—an ideal medium for such transport—is very advantageous in physical plant applications. The system's centralized nature allows straightforward use of fiber without the need for taps. Of course, the difficulty in tapping a fiber adds to system security. Local Bell companies have already installed fiber optic LAN test beds in several locations.

**Perfect Schedules**

The centralized-bus architecture uses a contention mechanism to gain access to the bus. This results in a perfect scheduling of packet transmissions on the time-slotted bus. That is, in contrast to distributed bus and ring architectures, the centralized-bus system avoids destructive collisions as well as idle periods during which the transmission medium holds packets awaiting transmission. Moreover, this characteristic is robust with respect to selected packet size, bus transmission rate, and geographical separation among the attached devices. In addition, AT&T engineers say the scheduling of packet transmissions is flexible, permitting multiple priority classes, round robin-like scheduling within a priority class, and even IC and packet switching. With these features, real time synchronous data and voice can be readily integrated.

The contention off the bus is never missed because interface modules residing on a node or concentrator backplane transmit packets in fixed-length time slots. As shown in Fig 4, the packet format consists of a header followed by a data field. The header is composed of a priority code, module number, and channel number. The module and channel numbers are used in the virtual circuit addressing and routing of packets. The priority code

Fig 4 The contention method to access the AT&T short bus uses a packet format that consists of a header followed by a data field. The header, which consists of a priority code, module number, and channel number, specifies the time slot by having the contending interface module with the highest contention code transmit its packet in that time slot.
and module number comprise the packet contention code. Contention occurs at the beginning of each time slot when the contending interface module with the highest contention code wins the contention and transmits its packet in the time slot. Although the module number is fixed and unique to each interface module on the backplane, the priority code can change with time, allowing flexible distributed scheduling of packet transmissions.

The contention mechanism relies on two properties of the bus to achieve perfect scheduling of packet transmissions. First, the end-to-end propagation delay of the short bus is less than the time to transmit one bit. Second, each module can simultaneously transmit and receive with the (open collector) bus functioning as a logical OR gate. With these two properties, the bus contention operates as follows. At the start of each time slot, each contending module begins transmitting its contention code. After each bit, if a module's transmission differs from what is read off the bus, it stops contending. That is, if a module transmits a 0 and reads a 1, it drops out of contention and waits for the next time slot. Hence, by the end of the module number transmission, the module with the highest contention code wins the contention and continues to transmit the remainder of its packet without interference.

Contestation takes place on a bus separate from the one on which packets are transmitted. The module winning contention in one time slot transmits its packet in the next time slot on a higher speed, parallel data bus. With this approach, transmission rates on the order of 50 to 100 Mbits/s are possible, according to AT&T engineers.

A good competitor

The centralized-bus LAN produces perfectly scheduled packet transmissions, avoiding both collisions and bus idle periods when there are packets awaiting transmission. AT&T engineers conducted a study to contrast this with popular access schemes, such as CSMA/CD and token passing, for distributed bus and ring architectures.

With CSMA/CD, the access protocol efficiency is critically dependent on the ratio of the bus end-to-end propagation delay to the mean time to transmit a message on the bus. The former is determined by the bus length (with cable propagation delay approximately 5 µs/km) and the latter is a simple function of the message length and bus transmission rate. The ratio, denoted by \( \alpha \), increases with an increase in the bus length or transmission rate, or a decrease in the mean message size. The average delay versus load performance for CSMA/CD degrades from that of perfect scheduling as \( \alpha \) increases from 0 (Fig 5).

For a system with a 2-km cable length and a mean message length of 1000 bits, the three values of \( \alpha \), 0.01, 0.05, and 0.1, correspond to a bus transmission rate of 1, 5, and 10 Mbits/s respectively. As \( \alpha \) increases, the usable bandwidth provided by the bus diminishes and thus the delay experienced approaches infinity at smaller loads. Therefore, the load on the bus approaches this capacity limit, at which point, AT&T engineers contend, operation is unstable. The perfect scheduling of the shorter bus performance shown in Fig 5, which corresponds to \( \alpha = 0 \), is for an unslotted system.

As for token-ring architectures, AT&T engineers assert that media access efficiency decreases as ring latency increases. The ring latency equals the delay in transmitting a bit completely around the ring. This includes both the ring propagation delay and the processing delay at each ring interface unit. Degradation occurs in performance for a single token system as \( \alpha \) (now the ratio of the ring latency and mean message transmission time) increases. The ratio increases with an increase in the ring length, transmission rate, number of interface units, or processing delay per interface unit, or a decrease in the mean message size. For a system with 50 interface units, a 2-km cable length, and a mean message length of 1000 bits, the three values of \( \alpha \), 0.1, 0.5, and 1.0 (Fig 6) correspond to, respectively, a transmission rate and per interface unit processing delay of 5 Mbits/s and 1 bit, 10 Mbits/s and 8 bits, and 20 Mbits/s and 16 bits. Thus the usable bandwidth decreases as \( \alpha \) increases.
Protect your sensitive IBM data with our new Fiber Optic Link

- Plug compatible with IBM series 3250, 3270A, and 3270B equipment.
- Replaces coaxial cable with fiber optic cable.
- Up to 1 Km operating range — virtually immune to electromagnetic interference.

Versitron’s FDH-1 (fiber optic digital hybrid) was designed to replace the coaxial transmission path in systems equipped with the IBM 3250 or 3270 series equipment. The simple installation of a fiber optic link provides two very important benefits to the user. First of all, the security level of the transmission link is greatly improved since fiber optic cables are inherently immune to conventional wire-tapping techniques. Secondly, the system operating capability will be enhanced since fiber optic cables are impervious to virtually all types of electromagnetic interference. This includes, of course, interference from heavy duty manufacturing equipment and noisy adjacent cables.

Versitron’s FDH-1 combines the high speed capabilities of a coaxial cable with the inherent advantages of a fiber optic cable. By interfacing directly to the coaxial cable, the FDH-1 appears totally transparent to the rest of the system; thus eliminating any operating restrictions.

If you’re currently transmitting high speed data over a coaxial cable and you’re concerned about data security, give us a call at (202) 882-8464 and get all of the details on how our FDH-1 will not only protect your data; but may also actually increase the operating efficiency of your entire system.

The FDH-1 is available in a variety of different enclosures, including a sealed unit specifically designed for EMI/RFI suppressed applications.

Versitron, Inc.
6310 Chillum Place, N.W., Washington, D.C. 20011, TEL: (202) 882-8464
CIRCLE 78
TWX: 710-822-1179
When comparing the short contention bus to a token ring, AT&T’s contention bus again excels. As the ratio \( \alpha \) (the ratio of the ring latency to the mean message transmission time) increases, the performance for a single-token system degrades. This results in a smaller usable bandwidth.

From these comparison results, AT&T engineers conclude that average delay performance for the short-bus contention scheme exceeds that of CSMA/CD and token passing. In fact, its average delay performance is lower bound to that achieved by the other two schemes.

Throughput is an important measure of data communication system performance. At the data-link level, throughput depends on the serial bit rate (the rate at which data is actually transferred on the link), and the interframe spacing (the time that passes from one transmission or reception of a frame until the controller is ready for a new transmission or reception).

**A heavy-duty controller chip**

A powerful controller chip that accommodates a high throughput rate is the i82586 from Intel Corp (Santa Clara, Calif). Intel’s chip handles all the functions of a CSMA/CD controller. The i82586 operates at data rates up to 10 Mbits/s, which is about an order of magnitude higher than most LSI communication controllers now provide. Intel claims that alternative implementations to the i82586 require many chips to meet this bit rate. This rate is achieved because transmission and reception are performed by separate onchip machines dedicated to these tasks (Fig 7).

The i82586 can receive any number of back-to-back frames that maintain interframe spacing of at least 9.6 \( \mu \)s. This is due to the concurrent operation of three processors on the chip: the fast micro-machine that handles memory structure, the onchip DMA controller that transfers data between the chip and system memory, and the transmit or receive machines that interact with the network.

The chip is intended for four main application areas. As a serial backplane it acts like a network, interconnecting devices inside a hardware cabinet or a room. It replaces bulky “parallel” cables with a single twisted pair or coaxial, while still providing high bandwidth.

It also serves Ethernet and networks conforming to the IEEE 802.3 and 802.4 standards, which are intended for office automation and similar applications. The transmission medium is shielded baseband coaxial cable with a branching nonrooted tree topology. Maximum station separation is specified as 2.5 km and the bit rate, of course, can be up to 10 Mbits/s.

The chip can also be implemented in mid-range local networks such as Mirlan—the Intel and NCR joint effort targeted at cost-sensitive applications that do not require high performance. This network uses inexpensive cable plus hierarchical data link control flags as well as bit stuffing for frame delimiting. The data rate is 1 Mbits/s and maximum station separation 1.3 km without repeaters.
High Tech, Low Cost.

Mitsubishi gives you a better image at the best possible price. Our economical series of color displays is performance-matched to such applications as MIS business graphics, process control, word processing, and video arcades. And its technology comes straight from our top-line monitors.

Examples: Super-high contrast glass for an extended range of true, vibrant colors plus a very dense black. And a special anti-reflective coating to cut glare for easy viewing, hours on end. Here's customer-pleasing, high-technology in a proven, reliable package.

We make our monitors the way you want them. In 12", 14", and 16" diagonal sizes. With dot or slot mask. Resolution grades including high (.31 pitch) and medium (.37 pitch). With a choice of options, too.

We're geared to handle both small and large orders. The bigger you buy, the more you benefit. Order 1,000 or more, and Mitsubishi will custom-manufacture to tailor packaging and performance to your exact needs.

In addition to a great price, our stocking policy is another bottom-line booster. We'll stock your displays and ship them to you — on a tight schedule to keep your product flow high. And when we handle the inventorying, you improve your ROI and cash flow positions.

MITSUBISHI ELECTRONICS AMERICA, INC.
DISPLAY PRODUCTS GROUP
991 Knox Street
Torrance, California 90502
(213) 515-3993

MITSUBISHI ELECTRONICS
ADVANCED AND EVER ADVANCING

Mitsubishi Monitors.
Finally, the i82586 serves metropolitan networks where standard Cable TV cable is used. The topology is typically a rooted tree and data rates are in the 128-kbit/s range for a 30-km radius.

In the broadband arena, Interactive Systems/3M, (Ann Arbor, Mich) introduced its Videodata LAN/1 last year. The LAN/1 concept uses a token-passing protocol between intelligent modems called network interface units (NIUs), which route terminal-to-terminal and terminal-to-multiple-host communications with direct addresses. The 3M engineers state that broadband networks offer particular flexibility in that they can handle virtually any type of electronic information including video, audio, and digital data. Table 1 compares the key considerations that a vendor might have when evaluating topologies. Several important broadband applications hold almost universal value regardless of the kind of installation. The broadband LAN/1 network serves as an information utility reaching even the most remote point of a facility or complex with full communication capability. And, the network can be monitored using an IBM PC that is equipped with the appropriate cards and software. LAN/1 applications include data processing, word processing, security systems, energy management, video training programs, production control, and electronic mail.

Broadband offers capabilities of particular interest to specific kinds of organizations. For example, in large academic institutions, video is increasingly used for instructional purposes, videoconferencing, and audio/video training. Without distributed communication, an instructor wishing to use a particular film or videotape in a classroom setting must arrange for pickup of the program, setup of equipment in the appropriate room, operation of the equipment, and return of the program material and projection device. Because of its high bandwidth, a broadband system makes it possible to build a central video distribution center that contains all of the campus audio/visual software and projection/playback equipment, and distributes signals over the cable network.

| TABLE 1 | Key Considerations for Choosing LAN Topologies |
|---|---|---|---|---|
| Key considerations | Twisted wire | Baseband | Broadband | Fiber optics |
| Terminal type | low speed | | | |
| Central network intelligence | intelligent or dumb | | yes-PBX not required but can be done for network management | yes-no |
| Bandwidth | 3 MHz (limited distance) | 50 MHz (limited distance) | 440 MHz (many miles) | virtually unlimited |
| Capacity per cable | one channel | one channel | hundreds of voice video and data channels | one channel |
| Maximum number of terminals | limited by conduit space | limited by bandwidth of channel | unlimited | potentially unlimited |
| Videoconferencing | yes—but not full motion | no | yes | yes |
| High data rate graphics capability | no | no | yes | yes |
| Capacity for higher data and future expansion rate devices | very difficult | very difficult | easy | easy |
| Distance | unlimited with modems via phone network | 1500 m—one mile | 40 miles | unlimited |
| Repeater requirement | standard phone network | every 1500 m—very expensive, inefficient | ordinary cable TV amplifiers at 2000-ft spacing | every 4000 ft |
| Speeds | 9600 bits/s max | 50 Mbits/s max | 10 Mbits/s maximum | 200 Mbits/s |
| Typical configuration | point-to-point/multidrop/radial | radial/ring/point-to-point-bus | on each of many channels | tree and bus |
| Transparency | yes | no—must be adapted via special interface | yes—on dedicated subchannels | yes—only on dedicated fiber |
| Data error rate | $1 \times 10^{-5}$ | $1 \times 10^{-7}$ | $1 \times 10^{-9}$ | very low no |
| Noise vulnerability | yes | low | very high—tapper must now channel and encoding | very high no |
| Data security | very difficult | moderate—tapper must know encoding scheme | very easy easy | very difficult impossible today |
| Maintenance | new cable is difficult to install | fairly easy, but must watch limits on each cable | very easy easy | very difficult impossible today |
| Modifying network | yes | yes | yes—self-contained | yes—vulnerable to breakage |
| Ductwork required | unlikely | unlikely | no | no |
| Wiring in place | likely | unlikely | unlikely | no |

Source: Interactive Systems/3M
Let Fluke rescue you from the landslide of up-board failures.

Four billion microprocessors will be built into countless products this year. We're filling the world with micro-systems. But how can we test and service them all?

Fluke's 9010A Troubleshooter puts some fast, simple answers at your fingertips. It's the first tester so easy to use, you'll start testing the first day.

Fluke has pre-programmed the 9010A to find most common faults automatically. Press a single key and it checks for Bus, ROM, RAM, or I/O faults, displaying clear diagnostic messages. For faults beyond the bus, our smart probe uses both stimulus and measurement to quickly track failures to the node. With support for 32 types of microprocessors, the 9010A will test almost any product. Merely plug the correct interface pod into the microprocessor's socket and take control of the unit under test.

You can easily customize any 9010A test right at the keyboard. Or, for extensive programming, use our new 9010A off-line Language Compiler with a personal computer. It makes programming easier and up to 3 times faster!

Don't get buried in the PCB landslide. For less than $5,000 you can own a Fluke 9010A, complete and ready for testing today. For more information, contact your local Fluke representative or call 800-426-0361.

IN THE U.S. AND NON-EUROPEAN COUNTRIES:
John Fluke Mfg. Co., Inc.
P.O. Box C9090, M/S 250C
Everett, WA 98206
(206) 356-5400, Tix: 152666

IN EUROPE:
Fluke (Holland) B.V.
P.O. Box 5053, 5004 EB
Tilburg, The Netherlands
(010) 673978, Tix: 62297

Now write 9010A software off-line with our new Language Compiler and popular personal computers. It's a convenient tool that makes programming fast and easy.
The LAN/1 uses a token-passing protocol between intelligent NIUs without need for a host computer. Communicating devices in the network are connected to a single coaxial cable through microprocessor-based NIUs which process point-to-point transfer of data packets. Transmission cannot occur unless an NIU has possession of the network token, which is passed sequentially from one NIU to the next in a circular manner.

The NIU handles all message processing and formatting tasks, traffic acknowledgment, and automatic contention for network access on an equal share basis. Channel capture is not possible, yet the system allows each node maximum throughput based on traffic levels.

The overall LAN/1 data rate is 2.5 Mbits/s for up to 10,000 devices—2000 on each of five channels. Terminal transmission rates can vary from 300 baud to 19.2 kbits/s. NIUs are available in two-, four-, and eight-port configurations.

LAN/1 operates on five channel pairs of 6-MHz bandwidth each. Transmission from NIUs takes place at the lower end of each channel. A channel converter connected to the cable intercepts all transmissions, converting them to a secondary frequency at the high side of each channel, and remodulating the data for retransmission. Redundant circuitry in the converter ensures dependable operation. The network frequency spectrum ranges from 53.75 to 276 MHz in five channels. LAN/1 works with either a mid-split or super-split broadband coaxial cable system. The total system also accommodates point-to-point data transmission, video applications, and selected audio applications.

LAN/1 hardware design includes a network monitor unit (NMU), which analyzes network performance statistically to facilitate routine maintenance and troubleshooting. NMU data enables system management to adjust channel assignments for maximum communication efficiency. This monitor unit consists of an IBM PC equipped with a two-port NIU and LAN/1 network monitoring software. In addition to its monitoring function, the NMU operates as a conventional user port on the network.

The total LAN/1 system accommodates point-to-point data transmission, and selected video and audio applications.

In an attempt to forecast market growth for both baseband and broadband LANs, International Data Corp (Framingham, Mass) has differentiated current LAN offerings into baseband and broadband topologies regardless of the kind of access method used. Table 2 lists the number of LAN installations by baseband/broadband orientation as reported by vendors to the market research firm.

**Universal PC network**

Microcomputers such as the Eagle, Kaypro, IBM PC, and other incompatible machines will eventually be linked to the same LAN. One of the first vendors to offer this capability is Alspa Computer, Inc (Santa Cruz, Calif).

The company first introduced Alspa-Net, a low cost LAN for its own microcomputer workstations and terminals last year. Alspa then developed interface cards and software enabling different brand name computers to become nodes in the network. The card and software are installed in the node computer, not in the system master, so the modification does not affect system reliability. Now, Alspa interfaces the IBM PC and its look-alikes with Alspa-Net. The interface card and software cost

### TABLE 2

<table>
<thead>
<tr>
<th>Vendors contacted with installations</th>
<th>Baseband</th>
<th>Broadband</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Installed LANs worldwide as of 12/31/82 (as reported by vendors)</td>
<td>28</td>
<td>7</td>
<td>35</td>
</tr>
<tr>
<td>Installed LANs U.S. as of 12/31/82 (as reported by vendors)</td>
<td>15,189</td>
<td>758</td>
<td>15,947</td>
</tr>
<tr>
<td>U.S. percentage of total installed</td>
<td>10,488</td>
<td>645</td>
<td>11,133</td>
</tr>
<tr>
<td>Worldwide percentage installed work area LANs</td>
<td>69.0</td>
<td>85.1</td>
<td>69.8</td>
</tr>
<tr>
<td>Worldwide percentage installed facility wide LANs</td>
<td>62.7</td>
<td>20.0</td>
<td>60.6</td>
</tr>
<tr>
<td>Type of premise installations:</td>
<td>37.3</td>
<td>80.0</td>
<td>39.4</td>
</tr>
<tr>
<td>Office</td>
<td>66.3</td>
<td>25.5</td>
<td>64.4</td>
</tr>
<tr>
<td>Factory</td>
<td>8.6</td>
<td>40.5</td>
<td>10.1</td>
</tr>
<tr>
<td>School/campus</td>
<td>13.6</td>
<td>12.5</td>
<td>13.5</td>
</tr>
<tr>
<td>Military</td>
<td>2.9</td>
<td>6.2</td>
<td>3.1</td>
</tr>
<tr>
<td>Research/engineering</td>
<td>8.6</td>
<td>15.3</td>
<td>8.9</td>
</tr>
<tr>
<td>Average number of nodes per installed network—worldwide</td>
<td>22</td>
<td>73</td>
<td>30</td>
</tr>
</tbody>
</table>

Source: International Data Corp, Framingham, MA
It's time to get in sync with a revolutionary idea: High-density CMOS static memories that interconnect systems in ways never before possible. We call them BiPORT™ memories. Because unlike any other memory devices, they read and write at the same time.

The first in the series is the MK4501 FIFO, an asynchronous device that's organized 512 x 9 in a 28-pin DIP. It's the fastest, highest-density rate buffer available for interfacing fast processors with slower peripherals.

But that's only a glimmer of application potential. Now consider true parallel computing.

Quite simply, the MK4501 and future BiPORT memories enable you to synchronize processors with different clock rates so that they can communicate with each other. Without complicated arbitration circuitry. What's more, BiPORT memories are fully expandable by word size as well as depth.

All of which means that you can now create the equivalent of a much larger system. For a fraction of the cost.

The possibilities? As far as your imagination can take you. And all you have to do is get in sync.

For more information, contact Mostek, 1215 W. Crosby Road, MS2205, Carrollton, Texas 75006 (214) 466-6000. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 296.886.

BiPORT is a trademark of Mostek Corporation.
technology, has developed an Ethernet controller for personal computers, VisiCorp's VisiON, and 3Com's EtherLink. This type of network card makes it now possible to use local area networking (LANs) on a printed circuit card small enough to plug into the heart of the Nutcracker. The system also incorporates an Ethernet controller on a printed circuit card small enough to plug into an IBM PC and costing less than $1000. With the plethora of Ethernet-type LANs currently being touted, it is a wonder that users have a clear understanding of how to evaluate their choice. Several developments over the last two years have made personal computers as "workstations" and local area networking practical and economical. The IBM PC, introduced in 1981, was the first in a series of professional computers featuring 16-bit processors, main memory of 256 Kbytes or more, bit-mapped graphics displays, and hard disk drives. Taking advantage of these hardware capabilities, VisiCorp has developed VisiON, an integrated operating environment for concurrently running applications, with the window display and mouse features formerly found only in higher cost workstations such as Xerox Star. And 3Com Corp (Mountain View, Calif), using the latest VLSI chip technology, has developed an Ethernet controller on a printed circuit card small enough to plug into an IBM PC and costing less than $1000.

Last year VisiCorp, 3Com, and Xerox Corp (Los Angeles, Calif) teamed to combine these technologies in order to overcome some of the drawbacks associated with local area networking of personal computers. The low cost of personal computers, VisiCorp's VisiON, and 3Com's EtherLink make it now possible to use local area networking with just two personal computers connected by a simple coaxial cable, for under $10,000. Yet, this configuration is fully compatible with a full-scale Ethernet-based integrated office system and a wide range of office products.

With the plethora of Ethernet-type LANs currently being touted, it is a wonder that users have a clear understanding of how to evaluate their choice. Enter the Nutcracker from Excelan (San Jose, Calif). It purports to solve two long-standing industry problems: how to debug and test very complex, high speed multiple-node networks (particularly their protocol software components) and how to characterize, or define the operating limits of, a given LAN configuration.

For example, to do a complete and thorough debugging and testing, a user must be able to get access to every packet on the network. Excelan claims that Nutcracker is the only commercially available product providing such complete observability. Its observation circuitry operating at 10 Mbits/s (approximately 1000 times faster than most communication instruments), allows it to see every packet, even in a fully saturated system. Proprietary, high speed state machine logic with extremely powerful pattern recognition circuitry is the heart of the Nutcracker. The system also includes an 8086-based CPU and features over 900 Kbytes of RAM, a 20-Mbyte Winchester disk drive, and a 600-Kbyte floppy disk drive.

It is packaged as a single integrated workstation that includes a 12-in. monochromatic CRT with 82-key keyboard and an external 100-char/s matrix printer with graphics capability.

Thus, as the community of LANs merges with the colony of PBXs, more peripheral enhancements can be expected.
In a world where what is promised is seldom delivered, we have earned a reputation for dependability. Whenever industry needs better ideas in flexible media, Verbatim responds.

We were the first to develop and manufacture in volume the 5 Mbyte, 8" disk. The first high-volume producer of the 5½" minidisk, as well as the 96 tpi minidisk. And the first U.S. company to produce the new 3½" microdisk.

But then, leadership comes naturally to Verbatim. Having manufactured over 200,000,000 disks of all sizes and densities, we're the world's leading producer. In fact, one out of every four disks sold is made by Verbatim.

We maintain complete manufacturing facilities around the world as well as across the United States. Each plant is staffed with its own highly-trained service organization, ready to solve any customer problem.

Our commitment also shows in our continuing series of technology seminars. Purely non-commercial, these educational conferences are designed to keep engineers informed of the latest developments in flexible media.

It's all part of the Verbatim response. Advanced technology. Quality media. Reliable service.

So if it's flexible media you need, give us a call. We'll respond to your instructions, verbatim.

Verbatim
323 Soquel Way, Sunnyvale, CA 94086
(408) 245-4400

Nothing's better than a Verbatim response.
IF YOUR COMPUTER IS SO SMART, WHY CAN'T IT USE THE PHONE?
FROM MODEM CHIP SETS THROUGH STANDARD AND CUSTOMIZED MODEM CARDS, ROCKWELL INTERNATIONAL HELPS GIVE MICROS THE POWER TO COMMUNICATE.

In the highly competitive world of microcomputers and terminals, built-in telecommunications can give you a sales and profit edge.

But until now, 1200 and 2400 bps card modems haven't been reliable enough, small enough or inexpensive enough to meet your product needs for the 80's. The third generation of Rockwell's VLSI integral modems has changed all that.

First off, our VLSI capabilities mean that we can support you at any level your business considerations require: from VLSI chip sets through custom cards that we design according to your specific shape, connector and software interface requirements.

Then there's reliability. Based on our customers' experience with over half a million Rockwell integral modems already in use, we've documented an MTBF of 200,000 hours—nearly 23 years between service calls.

As for performance, you get virtually error-free transmission over unconditioned or dial-up phone lines because Rockwell integral modems offer auto-adaptive equalization.

Rockwell R1212 and R2424 integral modems are compatible with Bell 103, 212, and CCITT V.22 standards; the R2424 is also compatible with V.22 bis. And our smart auto-call unit can dial using tones or pulses.

The standard Rockwell full-duplex R1212 and R2424 are each configured on a 3.9" x 6.3" (100mm x 160mm) Eurocard, so they're easy to design into your system. And since higher speeds are the wave of the future, you can upgrade your system from the 1200 bps R1212 to the plug-compatible R2424 (the world's first full-duplex 2400 bps integral dial modem) without changing your design. And they interface to any industry standard microprocessor bus and/or an RS232 port.

Even if your computer can't use the phone, we know you can. Use it to call the Semiconductor Products Division, Rockwell International at (800) 854-8099. In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, CA 92660.

SEMICONDUCTOR PRODUCTS DIVISION

Rockwell International
...where science gets down to business

CIRCLE 83
How can you develop one system and offer your customers a choice of three?

Simple. Develop it around HP's new three-in-one microsystem. That way, you don't have to redesign your system to offer your customers a range of performance. Because the entire power range of HP's new A-Series computers fits into the same small, convenient package. At a slimmed-down starting price of $6110*

So you can offer 1 MIPS performance. Or floating point hardware and microprogramming in either a 1 MIPS or 3 MIPS computer. Whichever one your customer chooses, you can fit it easily into the same space in your system.

Identical software keeps it simple.

When you change processors, you don't have to go back to the drawing board with your programs. Because, in addition to compatible hardware, these computers run identical software. That's the best kind of compatibility you can buy.

Our A-Series family consists of the Micro 26, Micro 27 and Micro 29. The Micro 26 comes with integrated 9.4 Mb mini-Winchester disc and microfloppy. And it has 8 I/O slots, giving you plenty of room for our wide selection of I/O cards for instruments, measurement and control, and data-comm, to name a few.

The Micro 27 adds floating point hardware and microprogramming. And, for jobs needing up to three times the power, our 3 MIPS Micro 29 has got what it takes.

Our brand new operating system really performs.

That's one secret of our success. The new, full-function RTE-A real-time operating system provides the performance you need for your real-time automation applications. Ranging from dedicated machine control to supervising a network of computers.

This power, speed and I/O capacity also make our A-Series systems ideal for multi-user, multi-tasking environments.

Of course, these compact new computers are part of our newly expanded OEM program. This includes higher discounts and credits, extended warranties and free training. So you'll make more when you get to market. And you'll also get there faster with our new operating system and newly packaged microsystems.

If you'd like micro, mini or maxi performance in one micro package, call your local HP sales office listed in the white pages of your phone book. Ask for a technical computer representative. Or write for more information to: Hewlett-Packard, Attn. Greg Gillen, Dept. 11171, 11000 Wolfe Road, Cupertino, CA 95014. In Europe, write to Henk van Lammeren, Hewlett-Packard, Dept. 11171, P.O. Box 529, 1180 AM Amstelveen, The Netherlands.

*A600+ microsystem component, 128Kb memory, box, Winchester disc.

Prices are U.S.A. list in OEM quantities of 100 and include integrated peripherals, one interface card, RTE-A and 512Kb of memory for Micro 26 and Micro 27. Micro 29 includes 768Kb of memory.

CIRCLE 84
Micro:
1 MIPS for $7445

Maxi:
3 MIPS, plus floating point hardware and microprogramming, for $16,650

Mini:
1 MIPS, plus floating point hardware and microprogramming, for $13,140

Whatever the level of performance you pick, it fits in this little 7" x 19" x 25.5" package.
Ethernet and other local area networks

AUSCOM introduces the proven solution for connecting your IBM mainframes to Local Area Networks. Using the 8911 Programmable IBM Channel Interface, AUSCOM can connect your network directly to the channel and, through software, provide the necessary drivers to incorporate the LAN protocol of your choice. You select the LAN; AUSCOM will make the connection to your IBM!

by AUSCOM, INC.
the "IBM to Anything" people

2007 Kramer Lane • Austin, Texas 78758 • 512/836-8080
STANDARDIZING UPPER-LEVEL NETWORK PROTOCOLS

Data communication networks will communicate more efficiently once standards are defined for the upper-level layers of the International Standards Organization seven-layer model.

by David Berry

The need for network interconnection standards has always been apparent. Over the past few years, the emergence of reasonably priced network technology for network connections has increased networking awareness. However, the debate over network technology itself and its access methods—broadband versus baseband, deterministic versus probabilistic, and token access versus carrier sense multiple access—has masked the importance of protocols for data flow control in networking.

As the number of real applications has grown, the International Standards Organization (ISO) has drawn on the experience of proprietary networks, the Advanced Research Projects Agency Network (ARPANET), and the public data network to summarize both known and anticipated networking requirements. ISO has done this by dividing network protocol functions into distinct groupings. This has resulted in a formal specification called the Seven Layer Model. The object of the model is to organize related groups that can be standardized independent of each other. This enables each layer to be defined with minimum reference to any other layer. Thus nodes in a network can be "constructed" with these layers and communication between nodes is ensured via peer-to-peer protocols between each node's layers. (See Panel, "Peer-to-peer is more than just here to here.")

A diagram of a node with the connection to the network medium at the bottom and the user interface at the top (Fig 1) illustrates the model. The functional groups are vertically arrayed.

The primary interface between the classical host functions and the network itself occurs in the network layer (layer 3). This layer allows each host to communicate directly with any other host connected to the global network. Routing and mapping problems are transparent to the network layer service users.

Prior to 1975, layers 1 and 2 were all that were usually specified. Provided that nodes were connected physically on the same network cable, this was adequate. With the development of more sophisticated packet-switching among heterogeneous networks, however, the need for more sophisticated routing protocols became apparent.

The network layer creates a route through the globally interconnected set of networks over which two hosts can converse. To avoid traffic congestion of faulty equipment in nodes of gateways in the path, this may need to be dynamically monitored. There are two basic types of network layers—connection-oriented (CO) and connectionless (CL). The former provides logical or virtual circuits for use by higher layers. The latter deals with each packet independently—i.e., a datagram service.

In addition, traffic handling and packet fragmentation/reassembly may be required in order to use available physical circuits. The network layer...
service is closely related to that of the transport layer above it. (The two were once considered as a single layer.) One of the two layers must provide the virtual circuit over which packets are transmitted between hosts. Both implementations already exist. In public data networks, the X.25 protocol provides virtual circuits and error detection. In the ARPANET system, the transport layer provides a (co) service to the user on top of a less complex network layer than the X.25.

Currently, no obvious resolution between the two major types of network service is provided. A comparison of the two is shown in Table 1.

Datagram service is the most primitive of the two. Error and sequence control must be added by the transport layer in order to provide a reliable service to the user. In virtual circuits, much of the service is provided by the network layer itself. This is not always an advantage. When disk sectors are transmitted as packets with an embedded sector address, sequence is unimportant. In this case, delay of data to users because of sequence problems is inefficient and unnecessary.

The network layer itself usually consists of three distinct sublayers, shown in Table 2. Not all three sublayers need be present. Access protocols are not usually required on local area networks (LANs) since LANs tend to provide sophisticated medium access protocols as a part of the data link layer (layer 2). Packet-switched wide area networks (WANS), however, use complex protocols such as the X.25 at this point.

The harmonization sublayer is required only to connect two subnetworks with differing services, such as a CL LAN to a CO WAN. This can be very involved, and practical experience in this area remains limited. The internet sublayer is solely concerned with the problems of mapping and packet-routing between nodes.

### Table 1

<table>
<thead>
<tr>
<th>Issue</th>
<th>Virtual Circuit (Connection-oriented)</th>
<th>Datagram (Connectionless)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial setup</td>
<td>Required</td>
<td>Not possible</td>
</tr>
<tr>
<td>Destination address</td>
<td>Only during connect</td>
<td>In each packet</td>
</tr>
<tr>
<td>Error handling</td>
<td>Transparent to host (done in the subnet)</td>
<td>Done by host</td>
</tr>
<tr>
<td>End-to-end flow control</td>
<td>Done by the subnet</td>
<td>Not available in the subnet</td>
</tr>
<tr>
<td>Packet sequencing</td>
<td>Messages passed in order sent</td>
<td>Messages passed in order received</td>
</tr>
</tbody>
</table>

### Table 2

<table>
<thead>
<tr>
<th>Sublayer</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3a</td>
<td>Access</td>
<td>Provides the interface to the data link layer</td>
</tr>
<tr>
<td>3b</td>
<td>Harmonization</td>
<td>Provides a mapping of the services available to give a common set to sublayer 3c</td>
</tr>
<tr>
<td>3c</td>
<td>Internet</td>
<td>Provides the routing and address mapping required to cross the network</td>
</tr>
</tbody>
</table>
Develcon introduces

DEVELSWITCH

An advanced intelligent switching system for people who want it all.

Of course you deserve it all. And to satisfy your desire for performance, we’re introducing the Model 9006 Develswitch, a technologically superior intelligent data switching system. Once you learn more about it, you’ll find that Develswitch stands out from all others with its unique combination of advantages that reduce costs, provide extraordinarily wide applications flexibility, speed communications, enhance convenience and allow for easy growth. If you really want it all for your datacomm network, now you can have it with Develswitch.

Develswitch Model 9006 Intelligent Data Switching System — Features/Advantages

The Model 9006 represents the current state-of-the-art in intelligent data switching systems, and the logical evolution of our many years of switching experience. With automatic port contention and selection for thousands of synchronous or asynchronous connections, the 9006 incorporates sophisticated software enhancements which provide a high level of system customization features never before available, along with many new features that offer unprecedented performance advantages. With Develswitch, now you can have it all. Ask us today for technical literature or applications assistance.

Consider these Develswitch features:

- **CONTENTION AND SELECTION** for asynchronous and synchronous lines to speeds of 19.2 Kbps
- **ADVANCED SYSTEM SOFTWARE** increases applications flexibility, speeds communications, reduces costs
- **NETWORK SUPPORT** for up to 2000 lines per switch
- **16 USER-PROGRAMMABLE SYSTEM PROMPTS** allow customization to meet specific application requirements
- **PRIORITIZED QUEUEING** with update and exit options
- **FIELD-UPGRADABLE MODULES** provide virtually unlimited growth capabilities
- **SPEED SELECTABLE FORCE CONNECTIONS**
- **MULTIPLE PROCESSOR CONTROLLERS** to accommodate even the largest networks
- **OPTIONAL REDUNDANT POWER SUPPLY**
- **ENHANCED SYSTEM OPERATION DISPLAYS** show complete and instantaneous system status
- **AUTOBRAID OR COMPOURED speed/code/party connections**
- **PARTY LINE CONNECTIONS**
- **MESSAGE, FORWARDING provides current connect information**
- **CONFIGURATION MEMORY backed up by battery**
- **ACU SUPPORT**
- **TANDEM LINK HARDWARE/SOFTWARE** connects two or more intelligent data switching systems
- **5 Megs THROUGHPUT**
- **SYNCHRONOUS SELECTION** via a 321 protocol or Keypad Select Unit
- **DOUBLE SAMPLING** via operator command
- **TRUE AUTOMATIC SWITCHOVER** to redundant common logic
- **SPECIAL SOFTWARE ENGINEERING SUPPORT** through our customized software services to meet your precise application
- **8 CHARACTER PROGRAMMABLE PASSWORDS AND DIRECTIONS**
- **SELECTABLE TIME-OUT INTERVALS**
- **SINGLE OR TRIPLE BROAD DISCONNECT**
- **43410 OR HIGH LEVEL, Limited Distance Data Set line interface cards**
- **CHOICE OF 65-232, bar and strip, or two terminalized back panels**
- **INDIVIDUAL DIRECT LINE-TO-LINE ACCESS**
- **FULL DIAGNOSTICS** including over 70 error messages, over 20 statics and on-line validation of firmware
- **SUPPORTS ALL COMMON CHARACTER SETS** including ASCII, EXDOC, BCDOC, correspondence
- **COMPATIBLE WITH ALL DEVELOCON intelligent switching and data transmission products**
- **ONE-YEAR WARRANTY, NATIONWIDE SERVICE**

Develcon data transmission products . . . cream always goes to the top.

Develcon Electronics is a leader in data communications technology.
We are manufacturers of a complete line of data sets, intelligent switching equipment and network systems.
CONNECTION REQUEST
LENGTH: 1110 CDT 00000000 00000000 SOURCE CLASS

CONNECTION CONFIRM
LENGTH: 1101 CDT DESTINATION SOURCE CLASS

DISCONNECT REQUEST
LENGTH: 10000000 DESTINATION SOURCE REASON

DATA
LENGTH: 11110000 DESTINATION SEQUENCE

ACKNOWLEDGE
LENGTH: 0110 CDT DESTINATION EXPECTED

Fig 2  The transport level is the highest level that concerns itself with the movement of data across the network and where the real problems of the OSI must be solved. The OSI transport protocol standard headers shown here are compatible with most major standards organizations.

control, monitoring the amount of data not yet acknowledged as received; error detection, the ability to monitor the packet sequence for missing, duplicated, or missequenced packets; and error recovery, the ability to rectify errors detected by this or lower layers without host intervention.

To a large extent, the degree of complexity required in the transport layer depends on the quality of the network across which the data is being moved. Reliability may be a function of the network itself, but it may also depend on the sophistication of the protocols being run at the network layer. To reflect this, transport service is generally made available in one of five classes: Class 0—simple, for use with Comite Consultatif Internationale (CCITT) networks; Class 1—basic, not yet fully defined; Class 2—flow control, limits number of outstanding acknowledgements for packets sent; Class 3—error detection, detects mishaps in the flow; and Class 4—error recovery, corrects mishaps automatically.

The transport service provides a pair of queues between two users that carry both data and control information in a duplex manner. It provides this as a transparent service, which then removes any need for users to be concerned with the physical data transmission.

Examples of transport layer protocol implementation are the transmission control protocol used in ARPANET, the network services in DECNET, and transport control systems in systems network architecture (SNA). None of these is normally used with a CO network layer, as in an X.25 network. This highlights the main division in the current debate on the transport layer. An example of the headers used in the ISO transport protocol standard are shown in Fig 2.

With transport layer protocols, two different approaches have been taken. On the one hand, packet-switching proponents, headed by CCITT, have approached networks from the point of view of existing telephone networks. Much of the work to be done in the transport layer is already incorporated in the virtual circuit protocols of the X.25 network layer. Some vestigial functions are required, such as reset recovery, since the X.25 protocol allows asynchronous resets to the connections.

On the other hand, those involved with computer networks require more transport layers. The main driving forces behind this approach were the National Bureau of Standards (NBS) and the ARPANET community in the U.S., and the European Computer Manufacturers Association (ECMA) in Europe. The majority of computer and system manufacturers are supportive of their efforts for a more complex protocol since this is the layer at which the real problems of open system interconnection must be handled. The major standards at the transport layer are listed in Table 3.

Although Table 3 seems to imply a variety of standards, the ISO, ECMA, and NBS standards are in fact virtually compatible. At the time of writing, a single transport standard will shortly be ratified by ISO. This is based on the NBS/ECMA standards (which are compatible in all but some details) and includes a class that covers the CCITT requirements for a truncated transport protocol.

In the attempt to define protocols, the transport layer appears to be the highest layer at which it will be possible to find common ground among all applications for a single standard. This explains the comparative rapidity with which a common standard for this layer has been achieved.

Making the connection

The session layer functions are still the subject of major discussion in networking. Several existing networks (such as the ARPANET) dispense with the
Peer-to-peer is more than just here-to-here

The seven-layer OSI model serves as a road map for network users. Network communication begins when the user in one node addresses the top or seventh layer of that node. This layer then communicates with the corresponding layer in the other user's node with some form of peer-to-peer protocol. This is accomplished by having the seventh layer use the services of the next lower layer, much as the user makes use of the seventh layer. This lower layer, in turn, corresponds with its opposite peer layer by means of its own peer-to-peer protocol, which is transported using the service of the next lower layer.

The importance of this layered arrangement is that functions associated with a network connection are grouped in an ascending order with respect to the host, and in a descending order with respect to the medium. The decoupling of layers allows a wide degree of flexibility to the network system designer in choosing the functions needed layer by layer. Each functional group is concerned only with those tasks associated with the layer in question. A node can therefore be assembled in a highly modular fashion.

Functions that are associated with lower layer protocols include packet framing (grouping of characters and messages), error control (detection of erroneous data or formats), data encoding (bit coding of the characters being sent), and frame addressing (routing of frames to destination nodes). These functions are typically concerned with providing access to the transmission media.

Besides the required protocols to communicate between the same layer in different nodes, protocols are also needed for communication between different layers in the same node. One layer interacts with another via a protocol in three ways: peer-to-peer, where a layer communicates with the same layer of another node; service provider, where a lower layer provides a service to the next higher layer of the same node; and service requester, where a higher layer uses the services provided by the next lower layer of the same node.

To date, most of the network protocols that have been considered for standardization are peer-to-peer protocols. Information is passed from peer-to-peer by attaching a header to the beginning of the data packet that is to be transmitted. Each layer encodes its header according to its specification (see Figure.)

Each layer provides a service to the layer above and expects service from the layer below. It receives data units from the layer above, along with interface control units that indicate the service to be performed for the layer above. The data units will already contain appended headers with protocols from the higher layers. This is completely transparent to the lower layer—ie, the lower layer has no understanding of the protocol used by the preceding layer and has no way to distinguish upper-layer protocol headers from the data proper. The lower layer then operates on the data packet as required. It might, for example, encrypt the data or split the data into packet lengths acceptable to the network to be traversed. Finally, it will pass control to the next lower layer by means of another interface control unit. The header now appended to the packet is transparent to the next lower layer.

Upon receipt of the packet at the destination node, a similar process is performed in reverse order. Each layer examines the packet area where it expects to find its header. This is interpreted according to the protocol specification for that layer, and any remaining part of the packet is passed up to the next layer for further examination as required.

Not every packet originates or terminates in the application layer. Also, several physical packets are usually required to transfer one logical packet. The actual ratio depends on a number of factors, such as the protocols in use, the error rate of the network, and the number of fragments into which a packet must be broken.

The logical mechanism by which protocols are transmitted across the network is a set featuring commands known as primitives. These are encoded in the appropriate packet header. Each primitive is generated by a layer within a node and transmitted to its peer in the other node by means of the services provided by lower layers. A given layer invokes these services by passing a primitive, such as a REQUEST, to the lower layer. This appears in the destination node as a REQUEST being passed up to the peer layer by the lower layer. Responses are passed back in a similar manner in the opposite direction. Thus, orderly transactions are ensured.
session layer altogether. The basic session layer functions manage data transfer (using transport service to move raw data), and add three categories of user-oriented services: connection management, data transfer, and transfer management.

Connection management provides such features as remote user identification that allows the local resident operating system to determine user privileges at the remote node. Data transfer service provides simultaneous bidirectional data transfer between nodes. Transfer management provides some form of subunit synchronization within the entire data block to be transferred, permitting recovery from network errors without retransmission of the entire file. Dialogue between the session entities of two nodes proceeds as an interchange of data units via the transport service (Fig 3).

Discussion of the session layer centers around four main philosophies: the ECMA approach, as embodied in the ECMA-75 standard; the CCITT approach, as embodied in the S.62 standard; the American National Standards Institute (ANSI) approach, a simplification of both; and the ISO working draft, a combination of the ECMA and CCITT approaches.

The ECMA approach is based on the software architecture of mainframe session functions. It attempts to provide the user with a more generalized control of the transport services of the layer below. The functions provided include reliable, organized, and synchronized data transfer; four distinct service subsets; and an optional data quarantine function.

In addition, the commands that are used by the protocol can be classified into four groups: session (connect/release/abort); data (data/expedited); synchronization (sync/resync/endDU/tokens); and quarantine (deliver/cancel).

The CCITT approach is based on the requirements of the teletext service and makes a number of less general assumptions about the application than the ECMA approach. It is designed to operate on a public data network and assumes that the major use will be in a teletext environment. It has only one distinct class of operation. Within this class are a number of possible commands, divided into two groups—session commands and document commands. These groups correspond roughly to the session and synchronization commands of ECMA-75.

The ISO approach, as characterized by the last meeting of the TC97/SC16/WG6 committee in March 1983, has been to combine all of the facilities of both the ECMA and CCITT approaches. This has resulted in a somewhat cumbersome specification that includes all of the command types from ECMA-75, plus an activity management command group, plus exception reporting, capability data exchange, and typed data.

This complexity has not yet been well received in the U.S. and ANSI has yet to come to a definitive position. The group has neither issued a draft standard of its own nor modified one of the above. There is unlikely to be agreement on the basis of any of the above due to the feeling among major U.S. manufacturers that the session layer does not require this degree of complexity and corresponding overhead. The likelihood of a unified session standard being available in the next year is not good. It may even prove necessary to agree on multiple standards that are appropriate for differing applications.

**Speaking the language**

While layers 5 and below deal with the transmission of data units that are transparent to them, the presentation layer is more concerned with network user interface. As the name suggests, the presentation layer presents the user with data transferred on the network in an orderly and unambiguous manner. This layer is therefore application-specific, and any comprehensive standard that will define all its functions in one protocol is unlikely. Currently, a number of nonoverlapping protocols for the presentation layer are being defined. These include virtual terminal functions; video/teletext; packet assembly/disassembly (PAD) functions; and text compression and character coding.

The most comprehensive standard for the presentation layer so far is the ECMA-86 standard on generic presentation service (GPS). The standard describes a model of the layer and the services it provides. It defines the GPS as a set of common service facilities that are dependent on the underlying session service to establish and maintain contact between users of the presentation services. Once
Raised in a harsh environment, our DCS/86 16-bit Multibus compatible computer system can cope with industrial reality.

**Industrial Ruggedness**

Designed for industrial applications, the DCS chassis is solid metal with no plastic, injection-molded parts. The front panel is an aluminum casting and our Multibus card cage is aluminum with a low-noise multi-layer backplane. Only the finest mechanical components are used to insure structural integrity in the most adverse conditions.

**Reliability**

Industrial grade preburned-in chips are used. Our system modules are subjected to dynamic burn-in at 55°C for forty-eight hours in our environmental chamber. As a fully matured unit, every DCS system is completely tested for a minimum of 5 days with extensive system diagnostics. At DCS, reliability is not a slogan, it is our commitment.

**Unmatched Modularity**

Our DCS systems are created to meet virtually any industrial application. They permit the user to mix and match operating systems, high level languages, interfaces, fixed and removable storage with a complete range of Multibus peripherals. Hardware configurations in our standard 19" rackmountable chassis can contain fixed and removable hard disks in 5 1/4" and 8" sizes as well as standard or slim line floppies. Operating systems supported are CPM/86*, MPM/86*, MS-DOS*, Concurrent CPM/86* and RMX-86*; "C", Fortran and Pascal are among the high level languages used. Whether your applications involve real-time data acquisition, multi-user software developments or data base management for factory automation, the DCS/86 family has a configuration to meet your budget.

**Support**

Since 1979, DCS has been designing and manufacturing rugged industrial micro-computer systems for process/industrial control, data communications and software development. The DCS family has been abused in harsh environments the world over. DCS provides total systems support through our expanding network of direct regional sales/support centers in conjunction with our corporate customer support group. For further information call: 617-890-8200 or write:

Distributed Computer Systems
330 Bear Hill Road, Waltham, MA 02154

*Multibus and RMX trademarks of Intel

*CPM and MPM trademarks of Digital Research

*MS-DOS trademark of Microsoft
contact has been established, all communication between the users takes place according to the GPS protocol, known as the p-service. Access to the p-service by the user is performed by an implementation-dependent interface.

Within the GPS, many service subsets are possible. These correspond to applications, such as file transfer or database management. A specific presentation service and a protocol used to provide it should be defined for each application.

Virtual terminal protocols (VTPs) are a subset used at the presentation level. An example is the ECMA-88 basic class virtual terminal, which is a subset of the ECMA-87 standard generic virtual terminal description of a virtual terminal service. Virtual terminals are a convenient construct in networking.

In practice, both the terminal and the application have access to the data being transferred as a two-dimensional array. The array consists of a number of cells that can be accessed (read from or written to) by either. The main difference is that the application has direct access to the data structure, while the terminal user views it through the display device and modifies it using the keyboard.

The application and the terminal communicate by means of character strings. A string is entered via the keyboard, which is passively viewed by the application until it can be interpreted as a command or response. The application then takes over and performs the appropriate action. The result of this is then communicated to the operator by means of a message entered in the data structure.

Since the terminal and the application both have their own views of the data structure, it is the task of the virtual terminal protocol to synchronize their communication. It negotiates the compatibility of the data structure, and establishes a set of functions to be implemented in a standard fashion. However, it does not address the exact nature of the terminal itself.

In addition, the upper interfaces of the VTPs to the terminals concerned are nonstandard. However, the interface to the session layer and the protocol used to communicate with another node follow the VTP standard.

Teletext and videotex are examples of presentation layer functions. Both have their origins in the idea of a low-cost information service available to both the home and the business market. Information in the form of both text and graphics is disseminated by the network to some kind of display, usually a modified TV set.

The distinction between teletext and videotex is in the degree of user interaction. Teletext permits almost no control over the selection of the data transmitted. A number of information screens are repeatedly transmitted, and the user may select one to display. Videotex users equipped with a small keyboard can select from the data base available on the network. In real applications, these distinctions become blurred, and teletext and videotex are generally grouped together. Moreover, they provide a spectrum of services ranging from one-way transmission from dumb terminals up to enhanced services available on sophisticated two-way transmissions from external data networks and intelligent terminals.

Examples of teletext in use today are the Ceefax and Oracle systems provided by the two television networks in Britain, and the Antiope in France. The current market in Britain is the largest in the world for teletext and provides 100-page magazines via the blanking intervals (the period of time when the electron beam is being repositioned at the top of the screen for another pass) in ordinary TV broadcasts.

Both teletext and videotex point the way to electronic information delivery to the home and office as a matter of routine. Limited bandwidth broadcast systems are excellent media for news, sports, and entertainment guides. More sophisticated interactive systems can also offer teleshopping and electronic banking.

Both systems require that a universal standard for transmission of the information is available. This is less of a problem with text displays than it has been with graphics. However, within the last year, there has been a considerable increase in support for the North American Presentation Layer Protocol Standard (NAPLPS). This is a method for encoding visual information in a standard and compact manner. Graphic and textual information can be represented in a variety of modes, colors, and styles. In addition, facilities are provided by the protocol for the user to interact with the two-dimensional display in a very flexible manner.

NAPLPS is one of the three contenders for a presentation layer standard for a graphics protocol. Whether the European Conference European des Postes et Télégraphique (CEPT) or the Japanese Captain will be incorporated in, or simply supplanted by, NAPLPS remains to be seen.

The PAD functions of the presentation level protocols historically preceded the ISO model. For that reason, PAD is something of a misfit in that it belongs conceptually in the ISO model, but operates as if it were a part of the network layer.

The PAD was a parametric approach to a virtual terminal taken by the CCITT in their efforts at standardization. It contrasts with the virtual machine approach described above by using a predefined set of parameters to define all terminal characteristics.
FOR A REFRESHING NEW LOOK AT COLOR GRAPHICS PUT A GENISCO G-2200 IN YOUR SYSTEM. IMPELL CORPORATION DID!

The G-2200 is truly a refreshing approach to raster color graphics. It combines vivid colors, flicker-free picture clarity, and big screen readability with high speed graphics and extensive software support. The result is the most cost effective system on the market. That's why Impell Corporation selected it as the perfect color graphics companion to CAEMIS, their Computer Aided Engineering & Management Information Services package.

Impell is a major supplier of computer software and computer based management and engineering services to the utility industry worldwide. CAEMIS is a modular, three dimensional engineering design and data base management system which provides simultaneous access for all design functions and on-line access to design information. And, the Genisco G-2200 is its window to the world.

The G-2200 has all the features desired for CAD/CAM, CAE, scientific and business graphic applications including built in peripheral support for mouse, tablet and printer. It is software compatible with the Tektronix 4014 and supported by third party software. It will also emulate the DEC VT100 for text editing and data entry.

But the best reason to put a G-2200 in your system is picture quality. Up to 16 colors can be selected from a palette of 4,096 hues with a unique black matrix glass bringing them vividly to life. Graphics are displayed on a big 19 inch screen that is refreshed at 60Hz for flicker-free viewing while the 1024 x 792 resolution ensures sharpness and clarity. No comparably priced system can match the picture quality of the G-2200.

The G-2200 is available as an attractive, ergonomically designed desktop terminal, or it can be integrated in your own system as a board or as a controller. Whatever the configuration, you can be sure of Genisco's commitment to design and production excellence and to on-site support by its international network of offices.

For details on how the G-2200 can color your system, call us for a demonstration. It will be a most refreshing experience.
A set of these parameters is negotiated for each connection made. This is easy to implement, usually as a table-driven scheme. Additionally, the standards in general use for these PAD functions are all from the CCITT "X" series. They include X.3, X.28, and X.29.

The text compression and character coding parts of the presentation level protocol are terms used to describe the encoding of data to be transferred on the network and its subsequent decoding at the receiving node. This can usually be related to encryption.

Text compression attempts to reduce the amount of traffic on the network by encoding repetitive strings of characters—e.g., by putting blanks in a more compact form. The strings are then expanded to their original format at the destination.

Character coding is used when communicating between hosts that use incompatible coding for their data, such as extended binary-coded decimal interchange (EBCDIC), and ASCII 7 bits. There are few true protocols involved in either character coding or text compression, and little has been done toward universal standardization.

**Talking to the user**

Of all the layers involved in networking, the application layer provides the most diversity and yet the least opportunity for standardization. It is the one most intimately concerned with user processes. The term "user" is generally taken to mean any user process or user machine, not necessarily a person using the system directly. The diversity is particularly true in the present environment where a multiplicity of systems exists.

The boundary with the presentation layer separates network designers from true network users. This layer has received less detailed attention than any of the layers, in part because of the lack of motivation towards standardization. The activities associated with the application layer are usually considered to include file transfer control; database management; remote job entry (RJE) and data handling; electronic mail; and network operating systems.

File transfer protocols (FTPs) handle files that are accessed by remote users in a standard fashion. This differs from local file management provided by the operating system. The operating system creates files with unique names within the local system and manages them according to local conventions. For global networks, a network-wide file management system needs to be defined. In the local environment, the most common operation is file access. On the network, it is file transfer.

The criterion for file transfer is to establish network-wide conventions for unique file naming. The FTP identifies both the source and the destination, and locates the file(s) involved. Details such as privilege of access, code encryption, or compression and merging must be standardized.

After the initial control phase, the data transfer takes place with associated control between the two servers involved. In the transfer of long files, the session layer services can be vital to efficiency. Should an error occur during file transfer, the session protocol should be capable of establishing the most recent checkpoint up to which the data was correctly transferred and of restarting the transfer from this point, rather than from the beginning of the file.

**The application layer provides the most diversity and yet the least opportunity for standardization.**

Currently, the closest thing to a standard in this area is an ISO FTP. It includes a logical model to help define the concept of virtual filestore that enables access and file management in the global network as well as the local environment. As a result, nonhomogeneous processes will be able to function interactively.

Database protocols are a generic grouping that includes such specific examples as RJE and interprocess communication protocols. The need for data bases was advocated long before the advent of networking and the availability of lower cost distributed systems. Many applications have multiple geographic locations where data must be available and operated on. Relational data bases have evolved to meet the requirements of query processing, concurrency control, and the relational distribution problem. None of this has yet been standardized for the networking environment.

Communication paths between data bases can either exist within a single-user system, or can be used to connect several user systems over some form of network. In a distributed system, the distinction between a remote and a local connection becomes trivial. Any protocol standard for distributed data bases must control both the access and any associated communication in an orderly manner. Processes can be located either in a single system or across several systems. In the latter case, the liaison must be established in order to exchange information, whereupon it makes no real difference whether the process accessed is local or remote.

The RJE protocols are used to enter jobs or batches of jobs to a remote computer. These will access the network through some form of VTP at the presentation layer. It requires a degree of high level activity, with program files being transferred by an FTP. Little has yet been done to achieve standardization in this area.

The details of how FTps, distributed data bases, and RJEs will interact in the networks of the future...
is a matter of speculation. A general scheme is illustrated in Fig 4.

Electronic mail is the means whereby messages may be exchanged by the same network users. This has received considerable attention recently. It is also known as computer-based message systems and is conceptually divided into three sublayers within the application layer: user agent sublayer, which provides message preparation tools; message transfer sublayer, which provides transfer mechanism; and reliable transfer sublayer, which controls error recovery. While a number of vendors such as MCI Communications Corp (Washington, DC) provide electronic mail service, little progress has been made towards a standard.

Business data exchange is an area in which ANSI is attempting to reach a standard protocol agreement. The series of X.12 standards attempts to define protocols for the following common business issues: purchase order transactions (X12.1); invoice transactions (X12.2); and data elements (X12.3). Although these three standards have been officially approved, they have not yet been applied widely.

Network operating system is a generic term for the concept of distributing the functions of an operating system among the nodes of a network. It is a logical extension of hardware distribution implied by networks to the software itself.

Each host continues to run its prenetworking operating system, but the network operating system is implemented as a collection of user programs distributed among the nodes that manage data and communication in an orderly and uniform manner. Little has been done in this area, but the problems are closely related to those of a distributed data base. Thus, the functions of a node can be efficiently organized by adhering to the specifications of the seven layers of the OSI mode.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 719 Average 720 Low 721

**STEP MOTORS**

**.9° AND 1.8° HYBRIDS**

± 3% step angle accuracy  
± 1% hysteresis

All hybrid motors engineered to meet your specific OEM design parameters • Quality dock to stock programs tailored to your manufacturing needs

WARNER ELECTRIC Brake & Clutch Company  
South Beloit, IL 61080 • 815-389-3771

CIRCLE 89 COMPUTER DESIGN/February 1984 185
At NEC, you'll find quality memories in every category.

All in one place.
Chances are, we have the exact memories you're looking for. Leading-edge 25ns 4K static RAMs. 64K static RAMs. 128K UV EPROMs. New 256K DRAMs. And our remarkable one megabit ROM—the highest density ROM in the world.

These aren't promises of things to come. They're here. Now. And ready for your next design.

You can trust our memories.
At NEC, quality is understood. Fact is, you can expect 100% burn-in, standard. And a guaranteed AQL of 0.1%. Which means, with NEC, your memories will be worry-free.

A complete package deal.
Be reminded, our memory devices come in a variety of packages. Standard and skinny. Plastic and ceramic DIPs. Flat packages and leadless chip carriers.

So if you have designs on the future, remember NEC. For a never-ending line of quality memories.

NEC Memory Products

<table>
<thead>
<tr>
<th>Type of Memory</th>
<th>Technologies</th>
<th>Densities</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CMOS, NMOS1</td>
<td>1M, 2K, 4K, 8K, 16K, 32K, 64K, 128K, 256K, 1M</td>
</tr>
<tr>
<td>Static RAM2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic RAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PROM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UV EPROM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1MMOS refers to Mixed-MOS technology (CMOS and NMOS).
2High speed 4K and 16K devices available.

WE'RE TAKING ON THE FUTURE.

For a fast response about NEC Electronics' complete line of memory products, call TOLL FREE 1-800-556-2344, ext. 188. In California, call 1-800-441-2345, ext. 188.

NEC sales offices: Woburn, MA (617) 935-6330 · Melville, NY (315) 423-2500 · Poughkeepsie, NY (914) 452-4747 · Pompano Beach, FL (954) 785-8250 · Columbia, MD (301) 730-9600 · Norcross, GA (404) 447-4469 · Arlington Heights, IL (312) 577-9090 · Southfield, MI (313) 589-4242 · Bloomington, MN (612) 854-4443 · Dallas, TX (214) 551-9561 · Orange, CA (714) 837-5344 · Cupertino, CA (408) 446-0500

© 1983, NEC Electronics
Forget manual coloring and overlays. Versatec can draw your VLSI, gate arrays, and other complex IC designs. In minutes. In big E-size formats. And with hundreds of bright, vibrant shading colors to define data-paths, junctions, and layers.

Only Versatec electrostatic plotters draw with such speed, color, and reliability. Faster color gives you quicker turnaround and more through-put for a faster product design cycle. Discriminating color enables faster analysis of complex circuit designs.

All-electronic color means no pens or jets to skip or plug. This is color plotting you can count on, shift after shift, day after day.

Versatec electrostatic color plotters are available, complete with host-relieving processors and software, direct from Versatec or through leading CAD system houses, such as Calma and Intergraph. Circle the readers' service number for our free-brochure—"15 ways to use electrostatic color plotting."
THIS IS WHAT PRINTSTATION TECHNOLOGY IS ALL ABOUT.

Since its introduction in late 1981, the innovative Centronics technology behind the Printstation 350 Series has received OEM praise for its paper handling and reliability. With new Printstation family additions, we now offer new capabilities and higher speeds. Now, more than ever, the Printstation 350 family will provide OEMs with the flexibility to meet all their printing needs. Bar code printing, Large characters, Color, Graphics. More Multipass fonts. More speeds, from 50 cps (multipass) to over 400 cps (10 cpi). And more efficiency with an outstanding new breakthrough: a 1-, 2- or 3-bin automatic sheet and envelope feeder option.

Add these new capabilities to proven Printstation 350 innovations such as true multi-function paper-handling, and family design with 80% parts commonality—and you have the ideal OEM printer choice for all three information processing categories.

DATA PROCESSING.
Printstation 350 means exceptional throughput—approaching line printer speeds in DP applications such as: □ Program listings □ Business reports □ Data logging □ Spread sheets ...using full 6-part, single sheet or fan-folded forms ...and capable of operating at 100% duty cycle.

BUSINESS PROCESSING.
Whether in an office or on a loading dock, whatever a business needs, a Printstation 350 will print: □ Bar code tickets □ Mailing labels □ Insurance forms □ Purchase orders □ Sales charts & graphs □ Invoices ... on business cut sheet, instant tear-off and sprocket-feed forms ... with graphics ... and without afterthought options.

WORD PROCESSING.
A Printstation 350 means complete job flexibility with a choice of fixed pitch or proportional fonts for: □ Business correspondence □ Office memos □ Proposals □ Personalized and form letters □ Envelope addressing.

And with our new automatic sheet/envelope feeder you can maximize operator productivity at an amazingly low cost.

Attractive and quiet enough for every office but right at home in a warehouse, teller station or shipping department. — That’s Printstation 350. From Centronics—the first choice of OEMs worldwide. For a copy of our new Printstation 350 brochure, write Centronics Data Computer Corp., One Wall Street, Hudson, N.H. 03051. Tel. (603)883-0111

CENTRONICS PRINTSTATIONS

CIRCLE 92
PBX-BASED LANs: LOWER COST PER TERMINAL CONNECTION

Universal digital loop transceiver chip set offers attractive alternative to coaxial and fiber optic based local area network.

by Henry Wurzburg and Steve Kelley

To date, the major emphasis in local area networks has been on systems that provide a very high speed communication link by means of a single fiber optic or coaxial cable with multiple drops. These systems have installation costs that are attractive because they require the addition and routing of only a single cable throughout the office. In addition, these systems, whether they are the contention/arbitration type (such as Ethernet), or the token-passing type, are highly efficient at passing large data blocks at a very high speed. As such, they are well suited for communications between large data processing/storage machines. However, since their goal is to economically provide access to as many office workers as possible, these systems still have a few disadvantages.

Although most present and proposed local area networks (LANs) boast 10-Mbit/s data rates, they only have effective data rates of 40 kbits/s when fully loaded. This ignores additional slow-downs caused by contention. In addition, the maximum number of user drops is limited, in some cases to 256 or lower. Increasing the capacity requires the addition of more cable and the provision of gateways between systems. This adds considerably to system expense. Also, much intelligence must be provided at each drop in the system to handle data switching and protocol, which further increases cost.

However, many offices already have most of the equipment needed to form a LAN that has the advantages of low cost, easy expansion, and simple installation: the digital telephone switch or private branch exchange (PBX). These switches digitize the analog voice as it comes in from each phone and route it throughout the switch to its destination at 64 kbits/s. Virtually every office worker has a telephone. Therefore, widespread user access to such a PBX-based LAN is established with the existing installation of twisted-pair wiring. And, since the digital PBX is inherently a data routing switch, minimal intelligence is required at each termination of the LAN. The use of existing telephone wiring, easy expandability, and the low complexity required at user equipment interfaces result in a digital PBX-based LAN that has a considerably lower cost per connection than other approaches (Fig 1).

The PBX's ability to directly handle digital data is a comparatively recent development. Traditionally, analog telephone signals have been switched and transmitted using elements called crosspoints. Although implemented with various technologies, all crosspoints are designed to switch and propagate .3- to 3-kHz audio signals with small and
controllable losses. A standard dial-up phone connection supplies the user with a 3- to 3-kHz full-duplex audio channel that is adequate for voice and audible control tones, but will not pass either dc contact closures or digital data streams. The need and convenience of using the dial-up voice network for data transmission has long been recognized. Today, this need is served with modems.

A modem converts serial digital data into audible tones that are within the 3- to 3-kHz band. In its simplest form, a "1" is signaled with one tone frequency while a "0" is sent with another. However, the 3-kHz audio bandwidth constraint limits the toggling rate between audio symbols (bauds) to about one-half of 3 kHz, or 1200 Hz. Usable data rates vary from 300 to 4800 bits/s, depending on the complexity of the modem design, and the separation method used to let data pass in both directions. Modems will continue in widespread use because they are universally compatible with the dial-up network's analog channel capacity. However, during the last decade, the digital telephone switch has emerged as a means of implementing analog channels. Where that technology is used, it is now possible to bypass the modem and its speed limitations by employing the inherent digital capacity of the switch.

The digital switch is born

The 3-kHz audio channel on which all telephone equipment is standardized can be implemented by digitizing voice at the channel ends and producing interconnectivity with memory and logic instead of crosspoints. The input audio signal is sampled at 8 kHz and each sample is coded into an 8-bit byte using an amplitude compression standard called Mu-law pulse code modulation (PCM). The result is that an active audio port inputs 8000 eight-bit words/s to the digital PBX. Thus, a 64-kbit/s data stream replaces the 3-kHz audio channel internal to the digital switch.

The voice data bytes are typically time multiplexed into 2.048-Mbit/s streams consisting of 32 eight-bit conversation time slots. Programming port A to read port B's time slot, and port B to read port A's time slot at continuous 8-kHz intervals accomplishes a bidirectional telephone connection through the digital PBX. A central call processor does the port's time-slot programming based on dialing commands input from the ports on separate signaling channels. Thus, the digital PBX is nothing more than a programmable and fast read/write memory placed between ports that digitize and undigitize incoming and outgoing audio signals.

The speed difference between using a digital switch's ports instead of a modem can be illustrated by the following example. Suppose a dial-up data user unknowingly encounters a digital PBX. The "A" user supplies a data stream at some 1200 bits/s to a modem that converts the data to 1200-Hz analog symbols for the PBX. The digital PBX's port converts those 1200-Hz symbols to 8000 eight-bit bytes/s, which are placed in its time slot and read by port B. Port B reads 64-kbit/s data, puts out 1200-Hz analog symbols, and user B's modem decodes the symbols into 1200 bits/s. If users A and B only knew how to access port A and B's time slots, this whole transaction could occur 50 times faster with much less hardware.

In a typical application, the digital PBX switch and its time slots are centrally located on an office campus. They are also connected to telephones that are remotely located by distances of more than a mile via bundled twisted-wire pairs. The PBX supplies dc power to, and exchanges transmit and
Whatever you design, the Bruel & Kjaer 3360 can help you keep it quiet.

The secret to designing quieter machines is knowing where the noise comes from, not just how loud it is. Bruel & Kjaer's 3360 Sound Intensity Analyzer lets you know exactly that. Because it measures and records not only the noise level of your product, but the sound intensity as well.

This means you can perform detailed noise mapping that precisely locates excessive noise sources. And you can use our processor/plotter or your own to create hard-copy maps that let you compare sound intensity readings both before and after design fixes.

The B&K 3360 measures sound intensity across the entire frequency spectrum in real time in 36 one-third or 12 one-octave increments to ANSI standards. It performs complete conventional sound pressure analyses, too.

So, if you're trying to design a product end-users will love, keep it quiet with the 3360 Sound Intensity Analyzer. Circle the reader service number, or call us today for complete information and the name of your nearest B&K field engineer.
receive 3-kHz analog signals with, the telephone set over a one twisted (or untwisted) pair of 26-gauge or larger wire. Coincidentally, those wire pairs already exist near almost every potential dial-up data user in an automated office. If the 64-kbit time slot could be remoted out to the telephone set on the same twisted pair, access to a relatively high speed data switching facility would be achieved at far more locations than the most elaborate ring or bus coax scheme one could ever imagine. Due to the sheer volume of potential applications, the transceivers used to upgrade the miles of twisted pair to full-duplex digital service must be expensive and easy to use.

This is precisely the intent of a new IC family introduced by Motorola in the first quarter of 1984. The universal digital loop transceiver (UDLT) family consists of three CMOS devices. Two of these are the master and slave UDLT devices. The third is a data-set interface (DSI) device that provides a RS-232 to time slot data conversion so that existing data equipment can be interconnected to these new transceivers without modification.

**Chips provide for digital PBX**

The MC145422 and MC145426 master and slave UDLTs are designed to communicate at a full-duplex data rate of 80 kbits/s over twisted pair from 0 to 1.25 miles in length. The 8-kbit total has three basically independent channels: a voice or data channel of 64 kbits, and two 8-kbit channels. Typically, one 8-kbit channel is used for PBX signaling, while the second is available for up to 9600-bit/s use in data applications.

Since the PBX must read and write 8-bit bytes to and from each active port at precise 8-kHz intervals to support voice communication, the baud rate of the UDLTs is set at 256 kHz. The master UDLT at the PBX port receives an 8-kHz sync pulse from the PBX and transmits a 10-baud (8 + 1 + 1) burst at regular intervals. This burst arrives at the slave UDLT up to 12 µs (3 baud) later due to propagation delay on the wire. The slave totally receives the burst between 10 and 13 baud after the master's sync. The slave UDLT then responds with its 10-bit burst after a 4-baud delay for transient settling. The return burst arrives and is received by the master from 14 to 17 baud after the end of the master burst at the slave. This is no more than 30 baud after the master's original sync pulse. Since there are 32 baud periods per 8-kHz frame, the round-trip propagation time can be greater than 6 baud without error.

This full-duplex transmission method is called ping-pong, and conservative wire propagation data puts the ping-pong range at over 1.25 miles. The master/slave relationship between the PBX and the telephone set provides the set with precise frame synchronization such that the PBX time slots appear to have been remoted to the slave. Thus, the synchronous data device can be directly connected to the UDLT, while async to sync conversion is handled by the DSI chip, which is discussed later. The UDLT transmission technique uses one baud, or symbol, per bit, but the nonreturn to zero (NRZ) bit stream cannot be directly applied to the twisted pair. The UDLT uses triangular modified differential phase shift keying (MDPSK), as shown in Fig 2.

**Fig 2. The universal digital loop transceiver (UDLT) uses a modified form of differential phase shift keyed (DPSK) modulation that reduces spectral content of the transmission waveform while retaining the strength of DPSK transmission techniques.**

In classical DPSK, a “1” is indicated by the carrier being the same phase as that during the last baud, while a “0” is coded as a 180-degree phase shift in the carrier from the last baud. This scheme has been modified by replacing the phase reversals of the 256-kHz DPSK waveform with a half cycle of 128 kHz. This lowers the spectral content considerably. Since the system must conform to present and perhaps tougher future American (FCC) and the European (VDE) rfi and emi requirements, excessive spectral content is of great concern.

In addition, MDPSK has several advantages over other modulation techniques. MDPSK does not require a start bit, nor a balancing bit to prevent bias distortion due to dc buildup during the burst, since each bit has zero net dc. This allows each bit in the burst to be data information. Additional overhead bits in a ping-pong scheme would require that either shorter loops, or higher baud rates, be used. Also, a zero-crossing of the waveform always occurs during the middle of each baud, which simplifies baud boundary timing recovery. Field trials and extensive computer simulation have verified the overall performance of the MDPSK transmission scheme. They yielded a bit error rate of better than $10^{-7}$ for 99 percent of the loops using 26-gauge or larger wire at lengths up to 1.25 miles while operating in cables with 49 interfering pairs.

The UDLT transmission scheme occupies a 10- to 500-kHz bandwidth that does not include dc. Thus, the remote digital telephone can derive its power from the PBX. By using CMOS technology,
Announcing a Breakthrough in Metropolitan Data Transfer

Gandalf's New LDM 409 makes 9600 bps Modems Very Affordable

Now there's a low cost 9600 bps synchronous modem optimized for metropolitan range applications! The Gandalf LDM 409 bridges the gap between long-haul and short-haul modem capabilities and costs. Based on innovative digital signal processing technology, the LDM 409 is auto-equalized, microprocessor controlled, and includes digital loopbacks, a test pattern generator, an error detector, plus more. The modem operates on voice grade, 4-wire leased lines in constant carrier mode. All of this puts the LDM 409 in a class of its own.

The LDM 409 handles full duplex, point-to-point applications involving data transfers through multiple telephone exchanges where short-hauls are not satisfactory but distances do not warrant the cost and complexity of long-hauls. Call today to get two 9600 bps LDM 409s for the price of one 9600 bps long-haul modem. Complete details are available from your local Gandalf representative.

Gandalf
Fully supported technology from concept to customer

USA: Gandalf Data, Inc. (312) 541-6060
Canada: Gandalf Data Limited (613) 226-6500
Europe: Gandalf Services, S.A. 22-98-96-35
U.K.: Gandalf Data Communications Limited (0925) 818-484
Subsidiaries of Gandalf Technologies Inc.

CIRCLE 94
the total power dissipation of an active digital telephone instrument is 1/4 W when active and can easily be supplied by a 5-V switching regulator. Furthermore, a startup algorithm has been designed in both the master and slave to let the ping-pong interaction stop when the digital telephone is not in use. Moreover, the idle power dissipation is under 50 mW.

**Applying the remote time slot**

The slave UDLT puts an 80-kbit/s data capacity at a digital telephone's location. Fig 3 shows a minimum digital telephone connected to a UDLT-equipped PBX port. Three data sources are connected to the slave UDLT in this configuration. To provide voice telephone service at this telephone site, the MC14402 PCM monocircuit digitizes and undigitizes the audio signals for the 64-kbit/s channel compatible with the compression and sampling standards mentioned earlier. One 8-kbit/s data channel is interfaced to the dial, ringer, and phone feature hardware via a CMOS microprocessor. Signaling to the PBX may be standard dial-pulse formats or an expanded command channel for voice or data user features. Finally, the last 8-kbit/s channel is connected to the MC145428 DSI. With this UDLT connection, voice and synchronous data communication up to 9600 bits/s are possible simultaneously. Higher data rates can be achieved (if voice is not required) by using the UDLT's 64-kbit/s channel for synchronous data, or, in conjunction with the DSI, for asynchronous data up to 57.6 kbaud.

The DSI takes the async start/stop bit formatted characters from any RS-232 interface, removes the start/stop bits, and stores them in a first in, first out (FIFO) memory. This data is then reformatted for the 8- or 64-kbit/s channel using a low overhead synchronous bit-stuffing algorithm. Incoming synchronous data is decoded and loaded into another FIFO. Async start/stop characters are then output at the selected baud rate.

**PBX LAN configurations abound**

Converting an existing analog line only requires the swapping of the PBX analog line card with a UDLT-based digital line card, and the replacement of the user's analog telephone with a UDLT-based digital telephone or workstation (Fig 4). Routing the data through the PBX can be accomplished two ways without requiring any modification to existing PBX software. First, the data channel can be inserted directly into the voice channel using the UDLT's pin-controlled signaling bit insertion feature. This provides a direct data path connection between the two parties who are conversing. Or, if separate routing of data and voice is desired, the data channel can be inserted into another 64-kbit/s time slot at the digital line card. This allows voice and data connections to two independent destinations.

The user equipment could consist of either a basic digital telephone set featuring a data port for...
PURE GENIUS.

Low Cost OEM Image Processors for Multi-Bus, Q-Bus and IBM PC.

The IP-512 family of OEM image processing modules have set new standards with high performance features previously available only on systems costing much, much more.

The IP-512 is a modular, real-time image processor that's plug compatible with the INTEL MULTI-BUS and DEC Q-BUS.

It interfaces with a standard video source, stores images in single or multiple $512 \times 512$ frame buffers with up to 24 bits/pixel, and includes pipeline processing for real-time image averaging, summation, subtraction, convolutions, histograms, feature list extraction, erosion and dilation.

The modules contain programmable I/O Transformation Tables and provide for B&W and RGB output for full color processing.

Applications include factory inspection, robotic vision, medical imaging, industrial radiography, teleconferencing, microscopy and image analysis, among others.

Imaging Technology also introduces PCVISION, a real-time video digitizer for the IBM PC. PCVISION allows OEMs to provide low-cost solutions for many applications requiring image processing.

For details, call our Sales Department at (617) 938-8444. Or write to:

Imaging Technology Incorporated, 600 West Cummings Park, Woburn MA 01801 Telex: 948263

PCVISION is a trademark of Imaging Technology Incorporated. MULTI-BUS is a trademark of INTEL Corporation. Q-BUS is a trademark of Digital Equipment Corporation. IBM PC is a trademark of IBM Corporation. Copyright © 1984 IMAGING TECHNOLOGY INCORPORATED.
Fig 4 A full PBX system can be developed using the UDLT. This system not only supports voice switching, but also allows data routing utilizing the inherent capabilities of the digital PBX.

connecting terminals or other data equipment, or a workstation that has the code/filter and UDLT integrated into it to provide the telephone set function. If the data equipment communicates in an asynchronous start/stop format, the MC145428 (DSI) provides the interface. As shown in Fig 4, using digital line cards as entry ports to the PBX gains access to other LANs and centralized data facilities. Communication to these devices could be over twisted pairs using the UDLT, RS-232, coax, or fiber optic links.

If the existing telephone switch is not digital, or if the designers do not want to directly retrofit their PBX, an alternative approach to a LAN is feasible. This approach, which retains the advantages of easy reconfiguration and low installation costs, calls for the addition of an auxiliary data switch to the PBX (Fig 5). Additional equipment at the PBX location handles data switching, while the existing PBX switches voice conversations.

Connections to this LAN use existing telephone twisted-pair wiring and the user's analog telephone set is replaced by a UDLT-based digital telephone set or workstation. The data switch's UDLT-based digital line card is similar to that used for retrofitting a digital PBX, except that the voice data is reconverted to analog by a codec/filter and fed to the PBX's analog line card. The auxiliary switch

Fig 5 An alternative configuration with the UDLT can be obtained with the addition of a "data only" switch when access to the PBX is unavailable, or if an analog PBX is used.
then routes only the data. Since this switch does not have to handle voice protocol and call progress supervision (bus signaling, ring back dial-tone generation, etc), its software and hardware requirements are much less complex than those for a conventional PBX. This approach allows a LAN implementation with most of the advantages of the retrofitted PBX-based systems. However, it does not require the system designer to have any detailed knowledge of the specific PBX used for voice switching.

In many data networking applications, a need often arises for high speed, dedicated, and unswitched data links. Rather than installing new cabling or expensive modems, existing telephone twisted-pair wiring (with the UDLT as a limited distance modem) can provide a very low cost link. Synchronous 64-kbit/s data transmission at distances exceeding 1.25 miles can occur using a UDLT and a few MSI logic ICs for clock generation/gating. This results in an extremely low cost installation. Asynchronous operation is possible by using the MC145428 DSI in conjunction with the UDLT.

The chip set can be an alternative to a coaxial and fiber optic LAN.

(Fig 6). In fact, by using multiple DSIs with the UDLTs at each modem end, up to eight terminals can be multiplexed into the single UDLT modem link. Thus, by using master and slave UDLTs, the DSI, and the PCM monocircuit in various combinations, the 64-kbit time-slot capacity of the digital PBX can be used for voice/data LAN applications with the central simplicity of the dial-up network. The use of existing telephone wiring and lack of requirements for controller/port sophistication in the user equipment gives the PBX-based LAN several advantages over coax/fiber-based LANs. The network configuration can be host for both dumb terminals as well as for simultaneous intelligent-peer-to-

intelligent-peer communications. There is, therefore, the option to reconfigure the office and rearrange it with the same ease as standard telephone service.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 722 Average 723 Low 724

TIMEWISE...

Z80 CLOCK/CALENDAR SINGLE BOARD COMPUTER 5327A

'S250

- STD-Z80 Bus compatible
- 32K onboard memory space
- HAMMER/PROM may be intermixed
- Clock/Calendar with onboard battery
- Four-year calendar (no leap year)
- 24-hour clock
- Full Mode 2 interrupt capability
- Accepts up to 4 Bytewise memory devices (4 sockets)
- Memory address decoding of any 2K increment on any 2K boundary
- RS232/449 Serial Channel
- Software Serial Channel baud rate selection up to 768K baud with split Rx/Tx baud clock capability
- 3 additional cascadable onboard Counter/Timers Channels

STD MICROSYSTEMS 5327A Module, an inexpensive answer to your STD Bus Module needs for a single-board computer that incorporates a Real Time Clock with Serial I/O with battery Backup.

The 5327A Z80 Clock/Calendar includes 32K onboard memory space, RS232/449 Serial I/O channel full mode 2 interrupt capability, flexible memory and I/O addressing. STD MICROSYSTEMS has designed this single board computer to intermix HAMMER/PROMS/PROMS components of your choice. All STD MICROSYSTEMS Modules have full STD Bus compatibility and are competitively priced. The Model 5327 Module comes in 4 speeds:

Available Configurations:
- 0327-01A $230 Z80 Clock/Calendar SBC, 2.5MHz
- 0327-02A $260 Z80 Clock/Calendar SBC, 4.0MHz
- 0327-03A $280 Z80 Clock/Calendar SBC, 6.0MHz
- 0327-04A $310 Z80 Clock/Calendar SBC, 8.0MHz

STD MICROSYSTEMS offers 150 STD Bus and other Bus featuring Z80, 6800, 6809, 6502, and 8088 processor types utilized in a line of application oriented SINGLE BOARD COMPUTER MODULES for integration in your microprocessor system. Those who have recognized the cost savings and efficiencies of designs using off-the-shelf STD Bus Modules into their control, data acquisition, laboratory communications and other applications. PLEASE CALL US FOR OUR SOLUTIONS TO YOUR DESIGN REQUIREMENTS.

STD MICROSYSTEMS
398 Sherman Ave • Palo Alto, CA 94306 (415) 327-8800

CIRCLE 96 COMPUTER DESIGN/Feburary 1984
Not everyone is happy about it. For instance, our new 286/310 multi-user, multitasking OEM supermicro is going to make guys who push minis awfully uncomfortable.

You see, it's based on our advanced iAPX 286 microprocessor, the most powerful 16-bit processor in the world. To which we've added our 80287 math coprocessor as a, shall we say, turbocharger?

That little bit of technological tinkering makes it a very fast supermicro. Faster than a VAX* 11/750. In fact, according to independent benchmarks, the 286/310 is the world's fastest Xenix* supermicro.

It doesn't do too badly in iRMX* real-time OEM applications, either (3x the performance of any comparably-priced system.)

The kicker is the 310 costs less than $10,000. And that's list, quantity one. OEM quantities are so much less expensive it's embarrassing.

But before you start thinking about all the money you can make with the 310, let us tell you...
a little about how easy it'll be.

Like all Intel systems, the 286/310 is built on standards.

The MULTIBUS* architecture. The iRMX real time operating system. Ethernet* networks and protocols. And the Xenix* operating system. Not to mention the world's most-written-for microprocessor architecture, the 8086 family.

All of which makes the 310 a very open system. Open to all kinds of OEM configurations. And enhancements like integrated software, interactive speech, graphics, networking, even software-in-silicon. And that means it's also open to new markets and new opportunities.

You'll also be able to find service and support for you and your customers' systems from more than 80 service centers worldwide.

Which is what you'd expect from a company with more than a billion dollars in sales.


Enough said.
ON ALLOCATION

Why wait 6 months for LS? We deliver Semicustom in half the time.

If you're losing market share because of the lengthy lead times it takes to get LS, you need to talk to CDI now. We have the CMOS gate array for your application. Not only will we deliver semicustom prototypes in eight weeks, we'll ship volume orders in less than half the lead time of LS.

And most important, when you pick CDI as your semicustom partner, that's exactly what you get—a partner. One who provides the responsive guidance and all-out service necessary to fully support your long-term design goals.

Our near-perfect success rate in developing customer designs keep more than 90% of our 'partners' coming back.

CDI was first to make gate array technology practical—and we now license our patents throughout the industry, even to our competitors!

We're fast, we're good, and we prove it daily in close work with emerging growth companies and numerous Fortune 500 giants.

You don't need a 6-month wait. You just need CDI. Call John Stahl now at 408 945-5000 for complete information. Or write California Devices, Inc., 2201 Qume Drive, San Jose, CA 95131.
A SIMPLE GATEWAY FOR ODD NETWORKS

Ethernets talk to token-bus baseband networks via a gateway implemented with LSI chips.

by Joonnees K. Chay, Jeff Seltzer, and Naseer Siddique

As different types of local area networks are installed in both offices and factories, more users are finding a need to connect them with intranetwork interface controller systems. Currently, however, few vendors offer gateway controllers that allow many different networks to be connected. Thus, networks such as Ethernet, used in office applications where real-time response is not a requirement, cannot talk to token-passing networks that offer real-time response to the critical manufacturing process, and to robotics control operation.

An Ethernet can be connected to a token-bus network using a gateway that is based on a high performance, bit-stream manipulation scheme (Fig 1). The configuration assumes that the two network media can be interconnected locally without the need for long-distance communication. However, the same general hardware design and software structures can be applied to many network types, as well as to gateway halves that interconnect remotely located networks.

The gateway controller has stringent requirements. It must be able to receive back-to-back messages on either network interface and store the messages that are addressed to the gateway for later transmission to the opposite network. It must also be able to receive or transmit on one network while simultaneously receiving or transmitting on the other. To accomplish this, processing power is usually distributed among three controller subsections: two network interface controllers (Ethernet and token-bus), and one centralized gateway management controller. The functions of the Ethernet and token-bus interface controllers are shown in the Table.

Joonees K. Chay is applications manager for standard products at Signetics Corp, Bipolar LSI Div, 290 N Wolfe, Sunnyvale, CA 94086. Mr Chay holds a BSEE from Pennsylvania State University.

Jeff Seltzer is an applications engineer for standard products at Signetics' Bipolar LSI Div. He holds a BA in physics from the University of Pennsylvania and an MS in computer science from California State University.

Naseer Siddique is an applications engineer for standard products at Signetics' Bipolar LSI Div. Mr Siddique holds a BSEE from the University of Engineering and Technology, Lahore, Pakistan, and an MS in computer engineering from Wayne State University in Detroit.
The gateway controller should receive and transmit messages in the same manner as any other master/slave station. Each of the two network interface controllers has to handle all message traffic situations defined under its corresponding protocol. The controllers operate at network data rates up to 10 Mbits/s, as prescribed by IEEE 802 standards for both carrier sense multiple access/collision detection (CSMA/CD) and token-bus networks.

**Design considerations**

These requirements can be met by having the messages that are received by the gateway stored in a central buffer memory. These messages can then be processed to some extent by the gateway manager before they are ready to be retransmitted. This processing includes translation between each network’s data-link protocols. And, the demands on the buffer memory are significant.

The message packets on Ethernet and token-bus networks (and most other network protocols) are variable in length. In the case of the token bus, the packet length can vary from about 20 bytes up to over 8000 bytes. Moreover, messages addressed to the gateway are received from either network at random times. After protocol translation is completed, the message is held in queue until its destination’s network controller gains access to the media for transmission.

For Ethernet communications, the buffer must be ready to either supply a stored message for transmission, or receive a new incoming message on short notice. The latter usually occurs when another station’s transmission precedes or collides with the outgoing message.

At a 10-Mbit/s data rate, a new data byte has to be accessed by a controller every 800 ns. Within that time interval, the message buffer is able to access a data byte for each of the three controller subsections. If necessary, it will do so in different memory regions. In addition to handling all these varied requirements, one important objective is that the system make the most efficient use of available buffer memory space to prevent a buffer overflow condition. This requires a robust memory management scheme implemented in the gateway management controller.

One IC answers that call. The Signetics 8X305 bipolar microcontroller was designed for bit-manipulative I/O operations. Thus, it can execute 5 million instructions per second, including data I/O instructions. Its Harvard architecture separates the

---

**Functional Distribution of Three Gateway Network Controller Sections**

<table>
<thead>
<tr>
<th>Ethernet and token-bus controller section</th>
<th>Gateway management controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiving and transmitting message packets on the network media</td>
<td>Allocation of buffer areas to incoming and outgoing messages</td>
</tr>
<tr>
<td>Media access control functions (eg, Ethernet collision recovery, token passing, etc)</td>
<td>Arbitration of the central message buffer between the gateway manager’s processor and the two network controllers</td>
</tr>
<tr>
<td>Serialization, coding, and synchronization of the data stream</td>
<td>Interrupt handling and interprocessor communication with the network interface controllers</td>
</tr>
<tr>
<td>Packet destination address matching</td>
<td>Translation of the packet format into the data-link protocol of the destination network</td>
</tr>
<tr>
<td>CRC generation and error detection</td>
<td>Any additional higher level protocol translation and management functions</td>
</tr>
<tr>
<td>DMA to central message buffer</td>
<td>Interprocessor communication and interrupt handling</td>
</tr>
<tr>
<td>Interrupt handling and interprocessor communication with the gateway management controller</td>
<td></td>
</tr>
</tbody>
</table>

---

*Fig 1 Two local area networks, one CSMA/CD Ethernet, and the other based on a token-passing access method, can communicate via a gateway consisting of interface controllers for both networks, a message buffer memory, and a management controller. This configuration is independent of the distance between the networks.*
program address and instruction buses from its local data (IV) bus. This keeps system control and message data flowing at peak rates. The 8X305 architecture also supports configuring the system into separate independent buses for optimal data throughput. This allows network message data transfer operations to gain exclusive access to the central message buffer.

In contrast, conventional MOS microprocessor architectures allow the message buffer to be located within the processor's main memory and attached to its common address and data buses. In addition to message traffic, these buses are used by the microprocessor for instruction fetching and local working storage. Since the network controllers may not be able to gain immediate access to the processor's memory bus, first in, first out (FIFO) buffers are usually required to keep the message data flowing. Use of the bus by the network interfaces may also result in an overall reduction in the processor's data throughput rate.

However, the 8X305 supports separating the local program buses, local data bus, and system message buses, therefore allowing multiple independent operations to be performed in parallel. Yet, the I/O performance capabilities of the 8X305 let it access the message buffer as quickly as most MOS processors access their own memory.

The controller, coupled with the 8X310 interrupt control coprocessor (ICC), adds priority-set, multi-level interrupt handling capability. This gives the 8X305 the power to deliver realtime interrupt responses within about 400 ns. The 8X360 memory address director (MAD) completes the critical link for each of the gateway's controllers to access the central message buffer management.

Controlling the network interface

The gateway system's essential activity centers around the data bus. This bus interconnects the gateway management and the two network interface subsections (Fig 2). All message traffic flows over this data bus.

Messages on the data bus are passed to and from a network medium (Ethernet or token bus) through physical interface circuitry and serial interface control logic. Standard line driver and receiver circuitry form the physical interface to a baseband network medium. They fulfill the electrical requirements defined by the network's physical layer.
Sending packets via gateways

The gateway controller services the message-packet routing from one network to another, fragmenting packets for a specific destination network, and embedding internetwork packets in the format of the destination network protocol. Gateway controllers can be subcategorized as media translators, protocol translators, and application translator gateways. Media translators connect two networks that differ from each other only at the physical and the data-link layers. Media conversion gateways can be thought of as devices that bridge an otherwise incompatible gap.

Protocol translator gateways interconnect networks that differ from the physical to the presentation layer. Such gateways convert the media as well as the higher level network protocols.

Application translator gateways manage the higher level communication layers and handle application-specific tasks. The gateway has to receive a packet from a network, unwrap the network package, identify the destination address, calculate the optimal routing path, wrap it again into the next network’s package, and transmit it on the other network.

Translating these operations into design requires critical design considerations. For example, translation of a longer address to a shorter address and vice versa, translation of bit-oriented protocols (HDLC) to character-oriented protocols (Bisync), and translation of higher level protocols are typical problems.

The functions performed by gateways vary considerably, depending upon different interconnection strategies. For instance, a gateway interconnecting a token network to an Ethernet network will have to perform a different set of functions than a gateway interconnecting an X.25 network to Ethernet. Therefore, interconnecting heterogenous networks raises various questions. Are there any standards available? Should the protocols of one network be directly translated to the protocols used in another, or should both of them be converted to a standard protocol? What kind of performance will be achieved?

A case in point is an Ethernet that has to communicate with a token-passing network (see Figure). Suppose a station with address A17 on the Ethernet (network A) has a packet to be transmitted to a station with address B21 on the token bus (network B). The actual message will be formed by station A17’s application layer and passed to its presentation layer, which will transform (encode) the message. The next level, the session layer, handles functions such as recovery from abnormal situations and establishment of the connections across the network. Thus, it is not really in the way of the data flow.

The encoded packet, therefore, is passed directly to the transport layer. This layer encapsulates the entire packet into its data field, and generates and adds new headers to the packet. As the packet flows down to the network layer, new headers and trailers are added. This includes the final destination address on the token network (in this case, station B21). The actual header and trailer formats generated at each layer depend upon the higher level protocols used to
implement the corresponding layer. The packet format generated by the network layer will be passed to the data-link layer, which will generate the standard Ethernet packet at the link level, including the CRC field. The packet's destination address will be A49, the station address of gateway 1 on the Ethernet. This packet will then be passed on to the physical layer for transmission on the communication channel to the Ethernet side of gateway 1.

Upon receiving the packet, the Ethernet controller in the gateway will unwrap it by peeling off all the necessary headers and trailers inserted by various layers (the number of layers to be unwrapped will depend upon the type of gateway being used). In case of a media translator gateway, it will only unwrap up to the data-link layer of Ethernet, which will also include error checking.

By eliminating the fields added to the packet by the data-link layer, the message will be retrieved as it was in the network layer of station A17. The gateway controller will now convert the packet to a standard token-packet format by generating another set of headers and trailers inserted by various layers (the number of layers to be wrapped will depend upon the type of gateway being used). In case of a media translator gateway, it will only wrap up to the data-link layer of Ethernet, which will also include error checking.

Several different networks can be interconnected through multiple gateways. In such situations, a message that has to be transmitted from one network to another may need to be routed via a third network. The possibility of errors is of course increased, but one can assume that every gateway involved in transmission, reception, and translation of packets can detect and correct the errors. Suppose the packet transmitted by station A17 is destined for station C34 on network C, but the packet has to go through network B. The packet will first be reformatted for network B by gateway 1 and then again for network C by gateway 2.

Station A17 defines the immediate destination address (A49) in its destination field and the final address (station C34) in its network layer header, then forwards the packet to gateway 1. Upon reception, gateway 1 reformats the packet by replacing the source address with its own address (B14) and the destination address with the intermediate address for gateway 2 (B68). Gateway 1 also generates a new CRC, then forwards the packet to gateway 2. Upon reception, gateway 2 reformats the packet again, replacing the destination address field with the address of station C34 and the source address field with its own address (C55). Gateway 2 also calculates a new CRC, then forwards the packet to the final destination.

Data on the network medium is encoded so that the high/low logic levels convey both data and synchronization information. Several standard coding formats are currently used in both data communication and mass storage applications. The most common include "Manchester" and FM.

The serial interface control logic consists of an encoder/decoder circuit, a cyclic redundancy check (CRC) generator/checker, and a serializer/deserializer circuit. The encoder/decoder circuit translates between the encoded data on the medium and raw serial data. The decoder section must lock onto an incoming message's synchronization pattern and provide the data bits extracted from the message, as well as a clock signal by which the adjacent circuitry can strobe in the serial data. The decoder also detects coding violations that may be caused by line noise, but are also used intentionally by the token-bus protocol for certain message delimiters. The decoder typically employs a phase locked loop (PLL) to establish synchronization. In the transmit mode, the encoder section receives raw serial data and generates the encoded pattern at its own fixed clock rate.

Each network interface controller performs error checking and generation of CRC values (referred to as the frame check sequence in the token-bus protocol). It is necessary to regenerate a new CRC for each outgoing message because the packet header information is altered during protocol translation. Depending on its software capabilities, the gateway manager may correct detected errors in received messages. Otherwise, the message is tagged to inform the destination host of the error condition.

The serializer/deserializer logic converts between the raw serial data and parallel data bytes that can be transferred on the gateway's data bus. The encoder/decoder circuit synchronizes the serial interface. Every eight clock cycles, a parallel data byte is transferred between the shift register (which performs the conversion) and a holding register. Before the next byte is finished shifting (ie, within the next eight clock cycles), the holding register must be serviced (contents read or replaced). This is the point at which the network data stream synchronizes with the message buffer access cycles.

The serial interface control logic performs functions that are fairly common to various data communication and mass storage controller applications. Serial interface control logic implemented with discrete logic functions, or more advanced field-programmable arrays, or even gate arrays, typifies the current solution to management of the data stream. Inevitably, single-chip solutions will appear to replace discrete implementations.
The 8X305 microcontroller coordinates all the activities within the network interface control section. It controls data movement through the serial interface control logic and to and from the message buffer without actually standing in the data path. Instead, it sets up conditions that allow the buffer to be accessed directly by hardware. Arbitration logic in the gateway management section controls the actual real-time access to the buffer.

The message transfers on the data bus are very similar to conventional DMA in computer systems, except that the data bus is used exclusively for the message data traffic. For example, there is no host processor on the bus to contend with. These message transfers require that the controller generate a sequence of buffer addresses to accompany the data. The MAD performs that function.

After the microcontroller initializes the various registers and counters, the MAD chip can count through a sequence of addresses independently with respect to the 8X305's processing. In the gateway design, the MAD output connects to the system address bus, which runs parallel to the data bus. The MAD units in each of the three controller sections supply address information to the message buffer via the address bus.

A collection of I/O ports provides a multipurpose interface between the microcontroller and other parts of the system for passing data and control/status signals. All I/O ports and data-oriented peripherals, such as the 8X360, are connected to the microcontroller on a special local data bus called the IV bus. A 256-byte high-speed bipolar RAM (8X350) is also attached to the IV bus, which provides local working storage to the microcontroller.

Media access control (MAC) functions are distributed between the MAC logic (specialized hardware) and microcontroller software in each network interface controller. The 8X305's instruction execution and data transfer speeds allow the microcontroller to handle many of the packet-header processing and MAC functions in software. In turn, the size of the MAC hardware can be minimized. The primary duty of the MAC logic is to handle the operations that require an immediate response on the network.

The network controller activities are coordinated with the gateway management controller through the exchange of interrupts between the respective microcontrollers. Interrupt request signals coming in from the gateway manager are handled by the 8X310 ICC. The ICC attaches to the 8X305's program address and instruction buses to control interrupt calling and return transfers. The microcontroller is also interrupted to respond to certain network control activity requested by the MAC logic, and to occasionally service the MAD.

Interrupt requests to the gateway manager are software generated. A pair of I/O ports passes information directly between the controllers over a separate interprocessor bus. These exchanges are in conjunction with interrupt requests and include such information as interrupt type, buffer address, and message length. Since these interrupts often occur during real-time message transfers, the system data bus cannot be used conveniently to exchange the information.

The main functions of the gateway manager are to maintain the message buffer and to perform all necessary message packet translations and higher level protocol processing. As in the network interface controllers, the heart of the gateway manager is an 8X305 microcontroller that is interfaced to the message buffer RAM via an 8X360 MAD and an I/O port. Also included are the 8X310 ICC and I/O ports required to perform the interprocessor communication with the network controllers (Fig. 3).

**Buffer benefits**

The message buffer itself consists of 32 Kbytes of RAM. With a maximum token-bus message size of 8 Kbytes, this buffer size accommodates one incoming message on each network interface plus storage for other messages being translated or awaiting transmission. This message buffer is segmented by the controller into 128 pages of 256 bytes. Although this should be sufficient for this application, the buffer size can be doubled if extremely heavy traffic is anticipated or lengthy protocol translation routines are to be implemented. With an access cycle time of 200 ns, the buffer memory can serve all three controller sections within the required time interval of 800 ns (derived from the network transmission data rate up to 10 Mbits/s).

The buffer arbitration logic acts as a special-purpose standalone DMA controller (Fig. 4). At the end of every 200-ns memory access cycle, the DMA controller samples the buffer access request lines from each of the three controllers and arbitrates a memory cycle on a round-robin priority basis. In the worst-case situation, when all three requests are active during consecutive cycles, the arbiter rotates among the three controllers and grants each an access window every 600 ns. The logic required to perform this function is easily implemented using a few latches and a field-programmable logic sequencer (FPLS) circuit.

The buffer access request signal for a network controller is taken from the parallel data strobes of the serial interface control logic. This signal also triggers the local MAD to sequence to the next address in its assigned buffer space. When the arbiter grants the memory cycle, the corresponding MAD is enabled and a data byte is transferred in or out of the buffer over the data bus. Since all of the gateway manager's buffer accesses are software-controlled, the memory cycle requests for this
TELEVIDEO'S OEM BOOM.
FULL PARTNERSHIPS AVAILABLE.

To get where you want to go in the OEM universe, choose a partner who can go the distance with you. TeleVideo® assigns you one applications engineer throughout design, manufacture and delivery. We meet both your specifications and your business requirements. We'll manufacture your terminals in our new state-of-the-art facility. And we'll test your way With your QC standards.

We keep the contract simple, back you up with continued technical support, and live up to our reputation for reliability and quick delivery.

Contact us today, whatever your terminal requirements. And experience the confidence of a partnership with TeleVideo for yourself.

Call us at (800) 538-8725 for more information. (In California call (408) 745-7760) or contact your nearest TeleVideo office:

California/Santa Ana ............................................. (714) 476-0244
California/Sunnyvale ............................................. (408) 745-7760
Georgia/Atlanta ......................................................... (404) 447-1231
Illinois/Chicago ......................................................... (312) 397-5400
Massachusetts/Boston ................................................ (617) 860-1282
New York/New York ................................................... (516) 496-4777
Texas/Dallas ............................................................... (214) 258-6776
Central Europe (The Netherlands) ................................ (31) 2501-35444
Northern Europe (United Kingdom) ............................... (44) 9-905-6464
Southern Europe (France) ............................................. (33) 1-606-4412

CIRCLE 99
controller are generated by extended microcode bits programmed in the local microcontroller’s program memory. Extended microcode is a block of extra bits added to the program memory’s width to provide, with each instruction executed, signals for general control functions and for fast I/O port selection.

The software running on all three microcontrollers exists as a collection of realtime tasks. Except for initialization, all tasks in the network interface controller are invoked in response to interrupts that are received either from the gateway management controller or from local operational units. Most tasks that are in the gateway management

---

**Fig 3** The same chips that made up the heart of the network interface controller can be used for implementing the functions of the gateway management controller. The message buffer memory should be able to accommodate data from both the management controller and the two interface controllers within the 800-ns access time that is available in a network operating at up to a 10-Mbit/s rate.

**Fig 4** The buffer arbitration logic acts as a special-purpose standalone DMA controller. Using a few latches and a field-programmable logic sequencer (FPLS), this logic circuit samples the request lines from the three interface controllers every 200 ns and arbitrates a memory cycle to the message buffer memory according to the round-robin sequence specified by the FPLS truth table.
HOW TO MAKE YOUR SUPERMICRO LIVE UP TO ITS NAME.

Add DSD’s RAMTRAC™ MULTIBUS® controller.

You’re building a supermicro. A 16/32-bit CPU on one end. And a high-capacity 5¼” Winchester on the other.

Now, what are you going to put in the middle? A plain vanilla controller?

That’s a little like a Ferrari with a Ford transmission. All show and not much go.

On the other hand, you could use a controller that’s especially built to wring every last bit of performance out of supermicros.

DSD’s RAMTRAC controller.

It controls Winchesters, floppies and tape. All on a single MULTIBUS board.

And it’s packed with performance features like pipelined architecture for quick system throughput, support for the new high-capacity 15-head Winchesters, 24-bit addressing to run with the most powerful microprocessors, and 32-bit ECC.

Not to mention file oriented tape transfers, on-board data separation, and a whole lot more.

Match a RAMTRAC controller to your application.

Our line of three RAMTRAC controllers emulate Intel’s® iSBC® 215, iSBX™ 217 and iSBX™ 218. And they’re compatible with all SA460-, SA850-, SA1000-, and ST506-type drives.

Just select the model that’s right for your application.

<table>
<thead>
<tr>
<th>Model</th>
<th>5217</th>
<th>6217</th>
<th>7217</th>
</tr>
</thead>
<tbody>
<tr>
<td>Winchester</td>
<td>5¼”</td>
<td>5¼”</td>
<td>8”</td>
</tr>
<tr>
<td>Floppy</td>
<td>5¼”</td>
<td>8”</td>
<td>8”</td>
</tr>
<tr>
<td>Tape</td>
<td>QIC-02</td>
<td>QIC-02</td>
<td>QIC-02</td>
</tr>
</tbody>
</table>

Call DSD for details.

If your supermicro is going to live up to its name, you really ought to take a look at our RAMTRAC controllers, today. The easiest way to do that is to call the DSD Sales office in your area for a copy of our RAMTRAC controller data sheet.

Eastern Region Sales and Service: Norwood, MA, (617) 769-7620. Central Region Sales and Service: Dallas, TX, (214) 980-4884. Western Region Sales: Santa Clara, CA, (408) 727-3163.

DEXPO® East 84
See us at booth #1404.
controller are invoked by interrupts from the network controllers, with the exception of the packet translation routines. These run in the main program under the control of a primitive executive.

As mentioned earlier, the message buffer is divided into 128 pages with 256 bytes/page. The gateway management software maintains a table of 128 pointers in its local working storage that corresponds to the 128 pages. When a message received from a network controller runs over into more than one buffer page, the pointer for the first page will contain the address of the pointer for the second page which, in turn, contains the next pointer address, etc. Thus, a linked list is formed. The software includes several lists for packets currently being received, those waiting for protocol translation, those waiting to be transmitted, and free pages ready to be allocated to new messages. For each of the above processes (except free pages), separate lists are maintained for each of the two networks from which messages originate.

The first and last pointer of each list are tracked. As a process is completed on a buffer page or packet (packets may consist of one or more pages), the corresponding pointers are removed from that process' list and appended to the list for the subsequent process. For example, when a packet is finished being translated from token-bus protocol to Ethernet, the pointers for those message pages are removed from the "translate token-bus" list and added to the packet list awaiting transmission on the Ethernet.

**Initializing the gateway manager**

When the gateway manager is initialized, it links all the pointers to the free page list. Then, it allocates one page to each network receiver and sends each network interface controller an ALLOCATE-RECEIVE-PAGE (ARP) command. The command is sent by placing the ARP command code and the allocated page address on the interprocessor bus to the desired controller and generating an interrupt request.

When interrupted, the network controller prepares its MAD (8X360) with the received page address and awaits an incoming message. As a message addressed to the gateway is detected, the controller begins filling the designated buffer page and immediately requests another page to use in case the first one fills up. The network controller sends a REQUEST-RECEIVE-PAGE (RRP) interrupt to the gateway manager, which responds by sending another ARP command with a new page address. Each page allocated to that receiver is added to the receive Ethernet list or to the receive token-bus list.

As a page does become filled during an incoming message, the network controller is interrupted by its MAD. The MAD is then reloaded so that the incoming message begins to fill the new buffer page. At this time, another RRP interrupt is issued to set up for the next page.

When an incoming message terminates, the network controller sends a RECEIVE-MESSAGE-COMPLETE interrupt with the length of the last buffer page on the interprocessor bus. The gateway manager responds by transferring all page pointers associated with the completed message from the receive list and links them onto the appropriate translate list. A flag is then set to notify the operating system kernel to execute the protocol translation routines.

For basic media-translation operation, where only the data-link fields of the packet are altered, the network controllers are set up to leave sufficient padding at the beginning of each packet so that translation can be performed in place (i.e., without copying the message data to another buffer location). However, if additional higher level protocol translation routines require message copying, another pointer list (for each network) could be added to keep track of the intermediate pages.

After message translation is completed, the associated pointers are transferred to the transmit list for the opposite network. A TRANSMIT-PAGE command with the first page address is sent to the network controller. The MAC logic is armed and awaits the appropriate conditions on the network medium to begin (or attempt to begin) transmission of the outgoing message.

Similar to the receiving process, whenever the network controller begins to transmit a new packet of the outgoing message, it sends a REQUEST-TRANSMIT-PAGE (RTP) interrupt to the gateway manager so that it can continue to transmit when the current page becomes exhausted. The gateway manager responds to RTP interrupts with TRANSMIT-PAGE commands.

Upon completion of a packet transmission, the network controller sends a TRANSMIT-MESSAGE-COMPLETE interrupt that lets the gateway manager return all page pointers associated with the completed message back to the free page list, thereby making them available for new incoming messages. Thus, communications between different local area networks is assured through a gateway configuration that has LSI circuits and sophisticated software.
IT'S ABSOLUTELY, POSITIVELY, UNEQUIVOCALLY, AND WITHOUT A DOUBT EXACTLY LIKE RL01-02/RX02.

Meet the family of WINC-05™ dual-wide Q-Bus controllers from AED. The WINC-05/5 and WINC-05/8.

They're absolutely transparent to your DEC system, so your software never has to know the difference.

Each controller positively replaces the 5 standard dual-wide DEC controller cards, freeing up valuable backplane slots.

Both unequivocally adapt to the specifications of most popular disk drives with the simple change of a single PROM.

And without a doubt, they give you the most flexibility at a lower cost.

All from a field-proven product going into its second year of shipments. AED's WINC-05 family. Single controller boards with 5 ways to better the competition.

For prices and ordering information, call or write us at: 440 Potrero Avenue, Sunnyvale, CA 94086; (408) 733-3555 or (800) 538-1730 outside CA.

ADVANCED ELECTRONICS DESIGN, INC.

WINC-05 is a trademark of Advanced Electronics Design, Inc., RL01-02, RX02 & Q-BUS are registered trademarks of Digital Equipment Corporation.

CIRCLE 101
Able's new Easyway/E Ethernet port controller makes tying together networks of UNIBUS PDP-II and VAX computers easier than ever.

Easyway/E provides DEC systems with plug-in access to IEEE 802.3/Ethernet LAN's, with less CPU overhead and less network software than other Ethernet ports.

That's because Easyway/E implements ISO/OSI protocol layers 1 thru 4 on a single board occupying one UNIBUS backplane hex slot. Much of the potential LAN software you need is already in the firmware. So, your initial network development time and costs for DEC systems with VMS and RSX won't drag you under.

And this lifesaving implementation of protocol on-board also offloads the CPU, freeing up the processor to handle other tasks.

What's more, Easyway/E meets IEEE 802.2, 802.3 and NBS-4 standards for ISO/OSI layers 1 thru 4, so current and future communications with other DEC systems will be smooth sailing.

In fact, Easyway/E's architecture is designed to accommodate future networking needs. The single board is comprised of two modules, so tomorrow's protocols can be implemented quickly with less expense. Additional protocol support including X.25, SNA and TCP/IP will soon be available, as will software support for DECnet and UNIX.

Able offers a broad range of devices for DEC computers providing communications, memory expansion and inter-processor connectivity. All complying with FCC regulations.

So, to keep from getting stranded, pick your port carefully. Easyway/E. The standardized IEEE 802.3/Ethernet port for today and tomorrow.


DEC, PDP-11, VAX, UNIBUS, RSX, VMS and DECnet are trademarks of Digital Equipment Corporation. Ethernet is a trademark of Xerox Corporation. Patent pending for Easyway.
CONTROLLER AND MICRO TEAM UP FOR SMART ETHERNET NODE

The LANCE chip adapts 16-bit power of micro to form a true Ethernet connection.

by James A. Fontaine

A common problem associated with high speed data transfers in Ethernet-like local area networks is receiver-end data congestion, caused by a system’s failure to process messages and reallocate receiver-buffer space at an adequate rate. This is due to either insufficient processing capability or inadequate computer system bus bandwidth. An intelligent VLSI processor with dedicated memory can alleviate data congestion, thereby allowing efficient attachment of intelligent node devices. A number of local area network control chips are available to perform this kind of operation (see Panel, “Ethernet controller chip comparison”).

One possible configuration utilizes the Local Area Network Controller for Ethernet (LANCE) MK68590 chip in conjunction with a single-chip, 16-bit microcomputer like the MK68200. Ethernet’s performance level often depends directly on the throughput of a host computer. In addition, transmitted messages can only be generated by the host during the time it controls the system bus. However, if each message consists of large amounts of data, the amount of bus bandwidth available for host computer processing may become the factor limiting throughput.

An effective method to reduce bus congestion is the use of a 16-bit microcomputer, such as the 68200, for an Ethernet node’s local processor. The chip’s architecture provides for onchip ROM and RAM, as well as an onchip baud rate generator and timers that produce the interrupt time-outs necessary for implementing upper levels of the Ethernet protocol. The 68200 can handle message acknowledgment, buffer manipulation, frame-related errors, and software implementation of upper level protocols. This frees the main CPU to handle only the core of the messages.

Utilizing the leadless chip carrier (LCC) version of the 68200, both the private bus and the system bus can access an external memory-mapped I/O (see Panel, “A closer look at LANCE and the micro”). Up to 111 Kbytes of memory can be addressed with two independent bus structures, enabling concurrent host and node processor activity. Thus, the 68200 does not have to stop processing when the host or LANCE requires control of the system bus to load or unload messages. The 68200 has its own private bus and program space from which it can continue to execute. This architecture makes the 68200 an ideal processor in situations where concurrent activity from both a local processor and a host processor is required.

Two types of configurations can be supported with the 68200-68590 interface. One configuration is the standalone mode, used when interfacing a terminal or number of terminals via an Ethernet link to a main processor located up to 2.8 km away. In this configuration, the 68200 handles local processing of both transmitted and received messages, achieving economic interfacing of many terminals to the main processor. The second configuration uses the interface as a peripheral or a frontend processor to the host.

James A. Fontaine is senior architectural engineer at Mostek Corp, a subsidiary of United Technologies Corp, 1215 W Crosby Rd, Carrollton, TX 75006. He holds a BS in electrical engineering from Marquette University.
In some applications, it may be desirable to interface one or more user terminals to an Ethernet link, each with an individual interface (Fig 1). The 68200’s onchip serial port and baud rate generator make this configuration simple to implement. The chip’s serial channel provides for a double buffered receive and transmit interface with data rates up to 1.5 kbits/s if the clock is asynchronous, and up to 1.5 Mbits/s with a synchronous clock. It also provides for internal or external baud rate generation.

For user terminal and similar interfaces, the 10-Mbit/s message rate that Ethernet offers is not typically required. Therefore, a cost-effective configuration may be implemented in which a local node services many terminals (Fig 2). A series of universal synchronous/asynchronous receiver/transmitters (USARTs) can be placed on the private bus to accommodate more than one terminal. Also, a modem interface can be provided to link the Ethernet to other local area networks (LANs) via telephone lines. This provides a link to additional LANs at a reasonable cost, but at data rates much lower than those that can be attained by a direct Ethernet link.

Such a standalone configuration can also be used in other applications to reduce Ethernet’s cost. For example, designers can configure a printing station composed of a letter-quality printer, a fast line printer, and a plotter. Although the need to use all three simultaneously may not arise very often, each device can be accessed at any time.

**System peripheral configuration**

The second configuration, where the 68200-68590 interface acts as a peripheral or frontend processor to the host, greatly unburdens the host CPU as well as the system bus. The host can gain access to the local bus and transfer messages and commands to the 68200 by dumping them into memory space and then notifying the 68200 that a transfer has occurred. This is done by either interrupting the 68200 or setting a bit in a shared status block (Fig 3). The 68200 would have control of the node’s local bus, which may be accessed by both the LANCE and the
A CRASH COURSE IN DISK AND DRIVE TESTING:

Disk Testing
ADE RVA instruments will show you how to test excessive acceleration, flatness, radial waviness, datum positioning, axial run-out and thickness.

Spindle Testing
Learn the nuances of testing axial and radial runouts, bearing quality, axial/radial acceleration, non-repetitive runout, radial resonance, wobble, and high frequency vibration.

ADE Corporation
77 Rowe Street
Newton, MA 02166
Telephone: (617) 969-0600
Telex: 922415

Head/Assembly Testing
ADE RVA instruments give you advanced instruction on head positioning accuracy, head motion studies, dynamic flight characteristics, pitching and rolling.

ADE RVA instruments maintain quality control from design through production. Only ADE systems can measure dynamic displacements from tenths of microinches to thousandths of an inch from 0 to 50 KHz frequency response. Sign up for the ADE course (every major manufacturer of disks and drives already has).
host CPU. Using this configuration, the 68200 does not access the system bus; thus, the host must use its DMA function to pass messages and commands in and out via a two-ported memory.

While the 68200 can access both the local node bus and its own private bus, it has sole control of its private bus. The private memory will contain the node's operating system software required to implement the bottom three layers of the Ethernet specification (Fig 4).

Interface and control logic must be incorporated to perform local bus accessing as well as all of the memory access decoding that is required for the host, the 68200, and the LANCE to access memory.

---

**Fig 4** The Ethernet node processor can implement the first four levels of the ISO protocol model. Depicted here are the software functions that are needed to implement the Ethernet specification.
Five reasons why DEC users should buy Emulex communications controllers.

Broad product line featuring our new DMF-32 emulation.
Nobody covers LSI-11, PDP-11, and VAX-11 users' needs like Emulex. More than 15 software-transparent controllers emulating DH11, DZ11, DV11 and DMF-32. All deliver improved line-handling capabilities, in a smaller package, at lower costs.

More channels.
Emulex's new DMF-32 emulation is typical. One controller board handles up to 64 lines, vs. only eight per DEC module. And Emulex offers all lines with modem control, not just two. For even more lines, Emulex's Statcon Series is the answer. We simply add a low-cost port concentrator, so that with one controller board you can connect up to 256 remote and local terminals.

Easy growth path.
As your system grows, upgrading is simple with Emulex controllers. Just change PROM sets. Example: DH to DMF for $350. In addition, Emulex's advanced microprocessor architecture is consistent throughout the product line. Think of the inventory savings.

Fewer backplane slots.
Emulex communications controllers pack so much capability onto each board that fewer boards are needed. Take a 64-line DH11 emulation. Emulex does on one board what it takes DEC to do on 36. Think of the savings in rack space, to say nothing of price.

Lower prices.
For instance, a DEC DH11 controller lists at $8,950 per 16 lines, with expansion chassis costing $3,000 or more. Compare that to Emulex's CS11/H at $4,500 for the first 16 lines and $3,000 for each additional 16 lines. At 64 lines, you suddenly have savings of about $23,000 and a lot of extra slots to boot.

Don't speculate with your communications controller dollars. Invest in Emulex. Phone toll free: (800) 854-7112. In California: (714) 662-5600. Or write: Emulex Corporation, 3645 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626.

The genuine alternative.
GSA Contract #: GSOOK8401S5575
If one were to implement the node processor scheme using true dual-ported memory (memory that can be simultaneously accessed from two sources without ill effect), the host would not have to gain access of the local bus. It could instead simply read and write to memory via one access port while the 68200 reads and writes to the memory via the second access port.

The Ethernet packet format consists of a 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and a 46- to 1500-byte data field terminated with a 32-bit cycle redundancy code (CRC) as shown in Fig 5. The variable widths of the packets accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (eg, 1024-byte disk sectors). Packets are spaced a minimum of 9.6 µs apart to allow a node time enough to receive back-to-back packets.

The LANCE is intended to operate in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between chip and processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operation mode of the chip via two control registers. It is only during this initial phase that the host processor talks directly to LANCE. All further communications are handled via a DMA machine under microword control contained within the LANCE. Fig 6 is a block diagram showing the LANCE and serial interface adapter (SIA) that is used to create an Ethernet interface for a computer system.

The intelligent node processor not only unloads a congested bus but it also implements higher level IEEE 802.3 protocols. With effective software, the...
The designer has a variety of VLSI Ethernet controller chips from which to choose. There are presently five Ethernet controller chips available: MK65990 (LANCE) from United Technologies/Mostek, i82586 (LAN) from Intel, the R68802 (LNET) from Rockwell International, the 8001 (EDLC) from Seeq Technology, and the MB51301 (DLC) from Ungermann-Bass/Fujitsu. These devices can generally be grouped according to performance by comparing the performance specifications of their respective data sheets. The LANCE and i82586 can manage multiple simultaneous transmit and receive buffers while the EDLC, LNET, and DLC can manage only one transmit or receive buffer at any one time. The Rockwell, Seeq, and Ungermann-Bass/Fujitsu devices meet the IEEE 802.3 specification, and although they support the implementation of ISO layers 1 and 2, they leave implementation of multiple buffer management to the designer. The LANCE and i82586 also provide all of the layer functions mentioned above, but do so with a sophisticated buffer management technique along with the physical Ethernet protocol functions.

Both the LANCE and i82586 access the transmit and receive buffers by first accessing the descriptor rings to determine the starting address of the message buffer. This method provides multiple buffers for both transmit and receive, and does not require the host to provide a buffer address for each message. The Rockwell, Seeq, and Ungermann-Bass/Fujitsu devices support only one memory address at a time for transmit and one for receive. Thus, the host must supply this address each time a buffer is allocated for either receive or transmit.

The Seeq, Rockwell, and Ungermann-Bass/Fujitsu controller chips require external hardware to implement DMA capabilities, while both the Mostek and Intel parts have controlling microcode to perform onchip DMA operations on both sequential receive buffers and sequential transmit buffers. The LANCE has a contiguous ring arrangement allowing up to 128 transmit and receive buffers. The i82586 uses a linked list arrangement that allows software control of the unlimited number of buffers for each side. Both devices provide for multiple buffers within a single transmit or receive frame.

Both the Intel and Mostek devices provide flexible memory arrangements, allowing the designer to interface them to operating systems with little software effort. Meanwhile, the Seeq, Ungermann-Bass/Fujitsu, and Rockwell devices require the hardware designer to plan a memory access arrangement that accommodates the local software environment, all at the expense of added board real estate. The LANCE requires contiguous, 8-byte-aligned, buffer descriptor rings that localize all buffer descriptors at any properly aligned location within a 16-Mbyte address space, and also requires three word memory accesses to acquire the next buffer address. The i82586 device allows the buffer descriptors to be placed anywhere within a 64-Kbyte address range, with a linked list arrangement. It requires at least four word memory accesses to obtain the next buffer address. This is one more than the LANCE requires; the number of memory accesses is critical in sequential message handling.

Both the Intel and Mostek controllers have complete station, broadcast, and multicast address recognition capabilities. The Seeq chip requires external multicast address recognition. In contrast, Rockwell's chip supports only the single node and indiscriminate address recognition modes. LANCE, i82586, and the R68802 perform the binary exponential backoff algorithm, while the Seeq device performs only part of it. The Seeq device notifies the CPU of collisions and waits for CPU completion of the computed backoff interval.

Mostek's LANCE and Intel's i82586 must be regarded as superior devices to other available controllers. The LANCE and i82586 are equal in performance, with the exception of LANCE's greater allowable bus latency, which directly reduces the possibility of first in, first out (FIFO) overrun. According to Dale Taylor, Dave Oster, and Larry Green in their article, "VLSI Node Processor Architecture for Ethernet" (IEEE Journal on Selected Areas in Communications, Nov 1983, p 733), "The FIFO buffer in an Ethernet controller provides two valuable functions: more efficient bus/memory usage through multiple transfers for each bus acquisition (bursts) and more tolerance to long bus latencies. The deeper the FIFO is, the larger a burst transfer may be and the longer peak latency will be." Intel's FIFO is 8 words deep, while Mostek's FIFO is 24 words deep. It can be shown that the average allowable latency that LANCE offers is almost equal to twice that of the i82586, while the allowable peak latency is greater than three times that of the i82586. They continue, "the larger the allowable peak latency of an Ethernet controller is, the less likely it will suffer a FIFO overrun/underrun in a system with a highly utilized bus."

### Ethernet controller chip comparison

<table>
<thead>
<tr>
<th>Node Processor</th>
<th>Layer 0</th>
<th>Layer 1</th>
<th>Layer 2</th>
<th>Layer 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>i82586</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R68802</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EDLC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DLC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The designer has a variety of VLSI Ethernet controller chips from which to choose. There are presently five Ethernet controller chips available: MK65990 (LANCE) from United Technologies/Mostek, i82586 (LAN) from Intel, the R68802 (LNET) from Rockwell International, the 8001 (EDLC) from Seeq Technology, and the MB51301 (DLC) from Ungermann-Bass/Fujitsu. These devices can generally be grouped according to performance by comparing the performance specifications of their respective data sheets. The LANCE and i82586 can manage multiple simultaneous transmit and receive buffers while the EDLC, LNET, and DLC can manage only one transmit or receive buffer at any one time. The Rockwell, Seeq, and Ungermann-Bass/Fujitsu devices meet the IEEE 802.3 specification, and although they support the implementation of ISO layers 1 and 2, they leave implementation of multiple buffer management to the designer. The LANCE and i82586 also provide all of the layer functions mentioned above, but do so with a sophisticated buffer management technique along with the physical Ethernet protocol functions.

Both the LANCE and i82586 access the transmit and receive buffers by first accessing the descriptor rings to determine the starting address of the message buffer. This method provides multiple buffers for both transmit and receive, and does not require the host to provide a buffer address for each message. The Rockwell, Seeq, and Ungermann-Bass/Fujitsu devices support only one memory address at a time for transmit and one for receive. Thus, the host must supply this address each time a buffer is allocated for either receive or transmit.

The Seeq, Rockwell, and Ungermann-Bass/Fujitsu controller chips require external hardware to implement DMA capabilities, while both the Mostek and Intel parts have controlling microcode to perform onchip DMA operations on both sequential receive buffers and sequential transmit buffers. The LANCE has a contiguous ring arrangement allowing up to 128 transmit and receive buffers. The i82586 uses a linked list arrangement that allows software control of the unlimited number of buffers for each side. Both devices provide for multiple buffers within a single transmit or receive frame.

Both the Intel and Mostek devices provide flexible memory arrangements, allowing the designer to interface them to operating systems with little software effort. Meanwhile, the Seeq, Ungermann-Bass/Fujitsu, and Rockwell devices require the hardware designer to plan a memory access arrangement that accommodates the local software environment, all at the expense of added board real estate. The LANCE requires contiguous, 8-byte-aligned, buffer descriptor rings that localize all the buffer descriptors at any properly aligned location within a 16-Mbyte address space, and also requires three word memory accesses to acquire the next buffer address. The i82586 device allows the buffer descriptors to be placed anywhere within a 64-Kbyte address range, with a linked list arrangement. It requires at least four word memory accesses to acquire the next buffer address. This is one more than the LANCE requires; the number of memory accesses is critical in sequential message handling.

Both the Intel and Mostek controllers have complete station, broadcast, and multicast address recognition capabilities. The Seeq chip requires external multicast address recognition. In contrast, Rockwell's chip supports only the single node and indiscriminate address recognition modes. LANCE, i82586, and the R68802 perform the binary exponential backoff algorithm, while the Seeq device performs only part of it. The Seeq device notifies the CPU of collisions and waits for CPU completion of the computed backoff interval.

Mostek's LANCE and Intel's i82586 must be regarded as superior devices to other available controllers. The LANCE and i82586 are equal in performance, with the exception of LANCE's greater allowable bus latency, which directly reduces the possibility of first in, first out (FIFO) overrun. According to Dale Taylor, Dave Oster, and Larry Green in their article, "VLSI Node Processor Architecture for Ethernet" (IEEE Journal on Selected Areas in Communications, Nov 1983, p 733), "The FIFO buffer in an Ethernet controller provides two valuable functions: more efficient bus/memory usage through multiple transfers for each bus acquisition (bursts) and more tolerance to long bus latencies. The deeper the FIFO is, the larger a burst transfer may be and the longer peak latency will be." Intel's FIFO is 8 words deep, while Mostek's FIFO is 24 words deep. It can be shown that the average allowable latency that LANCE offers is almost equal to twice that of the i82586, while the allowable peak latency is greater than three times that of the i82586. They continue, "the larger the allowable peak latency of an Ethernet controller is, the less likely it will suffer a FIFO overrun/underrun in a system with a highly utilized bus."
The MK68590 LANCE is a 48-pin VLSI device designed to greatly simplify the interfacing of a microcomputer (such as the 68200) or minicomputer to an Ethernet LAN. This chip is intended to operate in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled NMOS technology and is compatible with several popular microprocessors.

The LANCE interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide, but byte transfers occur if the buffer memory address boundaries are odd. An added advantage is that the address bus is 24 bits wide.

One of the key features in LANCE is its onboard DMA channel and the flexibility and speed that it gives in communicating with the host, or the dedicated microprocessor, through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings (Fig A). There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "lookahead manner" to determine the next empty buffer in order to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

Implementing layer 2

In order to implement layer 2, primitives must be generated and contained in the Ethernet node’s firmware to execute the following procedures: routing information, error, echo, sequenced packet, and packet-exchange protocols. The routing information protocol provides a means by which the data base is maintained in a dynamic manner and therefore the way routers direct
memory and I/O, and as a dedicated I/O controller that can share a 16-bit system bus with a 68000 or other types of 16-bit microprocessors. This architecture makes it an apt choice as a node processor for standalone or peripheral configurations. In addition, the 68200 provides an onchip serial I/O port that significantly reduces the amount of interfacing hardware needed to connect the Ethernet node to a serial device such as a terminal.

Forty of the 48 available pins on the device can be used for I/O, and their functions are programmable. I/O capabilities include parallel I/O, three timers, a serial channel, and an interrupt controller. In the single-chip configuration, all 16 bits of Port 0, and 9 bits of Port 1, are used for general purpose I/O. Up to three of the pins on Port 1 can be programmed as external interrupt sources, and up to four pins can be programmed as I/Os for the onchip serial channel. All 8 bits in Port 4 can be used as simple inputs or outputs or can serve as timers. For example, TAI can be used as an input for timer A, an interrupt source, or a general purpose input pin. If it is used as an interrupt source, it can be selected simultaneously with either of the other two functions. With the LCC version in the bus grant mode, the processor can access up to 64 Kbytes using the system bus and up to 47 Kbytes using the private bus and onboard RAM (Fig B). Thus, the 68200 can access up to 111 Kbytes of memory. The LCC allows the 68200 to grant system bus use to a host or peripheral, and private bus use for concurrent operations.

The chip count for implementing intelligent nodes is low enough so that the entire intelligent Ethernet controller can be placed on a single standard PC board such as VME, Versabus, or Multibus. This facilitates an easy system integration of Ethernet throughout the entire product line, regardless of the particular application. Standard software may be written for the Ethernet frontend processor, and unique software may be written to enable the host to implement particular applications.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 728  Average 729  Low 730

Fig B On the memory map of the 68200 and the GP-LCC configuration, DMA window expansion allows access of up to 111 Kbytes of memory.

16-bit microcomputer chip with onchip CPU, ROM, RAM, and I/O that provide parallel expanded bus modes operating with a full complement of multiprocessing features. The user can select I/O architecture allowing the device to operate both as a high performance single-chip microcomputer with a fully expandable CPU that can address external packets to other routers on their way to the final destination. The error protocol provides a means for error reporting when a packet has been discarded. It is intended as a diagnostic tool for analyzing network performance. The echo protocol is used simply to echo, or return each received packet to its source in order to verify proper operation. The sequenced packet protocol provides transmission of successive internet packets by the use of sequence numbers.

Using these numbers ensures proper rearrangement of a packet once it reaches its destination. The final software required for the intelligent node processor’s operation is the interface software. This is necessary to ensure proper communication and message transfer between the host and the node processor.
HP's three-in-one logic analyzer... the HP 1630A/D.

HP's 1630 gives you all three: timing, state and software performance measurements with interactive analysis too. All for less than what you'd expect to pay for a timing and state machine alone.

HP's 1630 low cost powerhouse of logic analysis solutions is the one logic analyzer that sets new standards for price/performance and ease of use. Fill out the attached postcard to see how easy it is to get all the applications information you need to put the HP 1630 to work on solving your logic analysis problems.

Now you can bring the power of logic analysis to the entire development cycle. Right away, productivity gets a big boost. Because of the HP 1630's simple interface and low-cost peripheral compatibility, you speed through setups and documentation. In one easy-to-use instrument you get advanced hardware and software testing and debugging power. Plus the ability to quickly spot software bottlenecks and inefficiencies. It's like getting three analyzers for the price of one.

At $8600*, the HP 1630A gives you a total of 35 channels of state (to 25 MHz), or, in the interactive mode, 27 channels of state and 8 channels of timing (to 100 MHz). For $10,630*, the HP 1630D offers a total of 43 channels of state. In the interactive mode, you have a choice of 35 state and 8 timing or 27 state and 16 timing. Both models include software performance analysis. Also, you can add the HP 2671G Graphics Printer ($1,540*) or the HP 82161A Digital Cassette Drive ($450*) for storing or setting up data. And for a complementary measurement tool that helps characterize digital hardware, consider HP's 8182A Data Analyzer ($14,850*).

Software performance analysis.

Software bottlenecks or time-wasting routines won't stand in your way any more with this powerful new analysis mode. Histograms of time-interval distribution eliminate guesswork by showing you best case, worst case, and average time between any two events you define—nonintrusively—while your system is operating.
Timing analysis.
For timing analysis, the HP 1630 gives you pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. You can also monitor bus activity in the state mode, trigger on a given bus pattern, then view asynchronous status and control line activity in the timing mode. This quickly unravels problems such as I/O port malfunctions.

State analysis.
In the state mode, four user-defined terms can be used in any combination to define sequence, store qualification, trigger and restart conditions, so you get right to the problem. But that’s not all. The HP 1630 makes it easier yet by letting you assign alphanumeric labels to input channels and status or control line patterns. Measurements are then displayed in your system’s terminology for rapid interpretation.

Tell us your tough microprocessor system measurement needs.
Hewlett-Packard has the equipment and the expertise you need to guide you along the shortest path from problem to solution. To find out how we can help solve your particular application problem, use the instant reply postcard and get a copy of our brand new application note, “Improving Software Designs with Performance Analysis Measurements.” Or, call your local HP sales office listed in the telephone directory white pages. Ask for an HP field engineer in the electronic instruments department.

*Domestic U.S.A. price only.
CD 2/84
Lear Siegler
Quality and Reliability You Trust. High Touch Style You’ll Prefer.

This new generation of Lear Siegler video display terminals brings elegant High Touch™ style to our American Dream Machine (ADM™) tradition. The family features three new ergonomic terminals designed to meet the needs of OEMs and end users alike: the ADM 11, the ADM 12 and the ADM 24E.

Here is a whole new way for terminals to relate to people. Dozens of little touches add up to the convenience and comfort of High Touch.

For example, we put the power “on/off” switch and contrast control knob in front where they’re easy to reach.

The monitor not only tilts and swivels, it stops positively in almost any position.

The clean, crisp display features a large character matrix on an easy-to-read green or amber non-glare screen—made even easier to read by the hooded bezel. Screens are available in 12” or 14” sizes.

You get the best in style and ergonomics, plus all the outstanding performance features you’d expect from Lear Siegler (see chart).

Lear Siegler High Touch terminals are backed by the broadest network of full service centers anywhere, serving 3000 cities nationwide. And they’re made in America—designed, engineered, manufactured and shipped from Anaheim, California to provide you with the best local support.

Place your order today by calling your local Authorized Distributor or, for quantities in excess of 500 units, your Regional OEM Sales Office.

Call Lear Siegler at 800/532-7373 for the phone number of an authorized distributor near you: Advanced Technology · Continental Resources · The Datastore · Data Systems Marketing · David Jamaison Carlyle, Inc. · Digital Source · Dytec/South · Gentry Associates · Hall-Mark Electronics · Island Associates · Kierulf Electronics · M/A Com Alanthus, Inc. · Marva Data Services · M.T.I. · National Computer Communications · Pioneer (Standard, Harvey, Gaithersburg) · 2M Corp. · Wyle Electronics

Distributor Sales & Service: Boston (617) 456-8288 · Chicago (312) 279-7710 · Houston (713) 780-9440 · Los Angeles (714) 774-1010, ext. 219 · Philadelphia (212) 245-4080 · San Francisco (415) 828-6941 · England (04867) 80666 - From the states of CT, DE, MA, MD, NJ, RI, VA and WV (800) 523-5253.

OEM Sales: Chicago (312) 279-5250 · Houston (713) 780-2585 · Los Angeles (714) 774-1010, ext. 582 · New York (516) 549-6841 · San Francisco (415) 828-6941 · England (04867) 80666

Low-profile, tapered, DIN-standard keyboards with Selectric layout feature logical key groupings and adjustable tilt for comfort and efficiency. ADM 11 shown above.

<table>
<thead>
<tr>
<th>Terminal Compatibility</th>
<th>ADM 3A, ADM 5,</th>
<th>ADM 3A, ADM 5,</th>
<th>ADM 3A, ADM 5,</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADHIS Viewpoint</td>
<td>&amp; Regent 25,</td>
<td>&amp; Regent 25,</td>
</tr>
<tr>
<td></td>
<td>Hazelview 1400,</td>
<td>Hazardview 1400,</td>
<td>Hazardview 1400,</td>
</tr>
<tr>
<td></td>
<td>1420 &amp; 1500,</td>
<td>1420 &amp; 1500,</td>
<td>1420 &amp; 1500,</td>
</tr>
<tr>
<td></td>
<td>DEC VT-52</td>
<td>DEC VT-52</td>
<td>DEC VT-52</td>
</tr>
</tbody>
</table>

LEAR SIEGLER, INC.  DATA PRODUCTS DIVISION
901 E. Ball Road, Anaheim, CA 92805 (714) 774-1010

© 1984 Lear Siegler, Inc.

Selectric is a registered Trademark of IBM. Viewpoint and Regent are registered Trademarks of Applied Digital Data Systems, Inc. VT-52 is a registered Trademark of Digital Equipment Corporation.

CIRCLE 106
Wireless Keyboards are NEWS

...and Cherry is the NEWSMAKER!

Infrared link between keyboard and computer. In the most advanced, state-of-the-art low profile ergonomic designs. New... and now... from Cherry.

Full custom keyboard designs with CMOS electronic components. In your choice of the latest Cherry full travel, sealed contact technology... or our MX gold crosspoint contacts.

Special power circuitry requires power only when a key is depressed. Extends life of the four AA alkaline batteries.

Stock standards coming soon! Custom designs start now... standards available by June! An enhanced version of IBM PC keyboard with wireless capability. Also compatible with IBM PCjr.*

Custom or standard, you're assured of a reliable keyboard from a good solid source. Cherry. Your Keyboard Headquarters.

*IBM PC and PCjr. are the registered trademarks of IBM Corporation.
ESTABLISHING THE MICRO-TO-MAINFRAME CONNECTION

The 3270 emulator accommodates coaxial link with RS-232 serial data on the same card.

by Dan Erlin

As more personal computers are used in the corporate environment, their usefulness is hampered by the lack of communication with the mainframe. Establishing an effective communication link is becoming a necessity.

Given the preponderance of IBM mainframes in medium-to-large corporations, a desirable feature of the mainframe-to-PC interface should be an easy adaption to IBM's own communication environment. In most cases, this means emulating IBM's 3270 family of controllers and terminals. International Data Corp, a Framingham, Mass market research firm, estimates that 80 percent of potential IBM users want mainframe connectivity via 3270 protocols.

What is the best method? The PC can be connected to a host in a number of ways for it to perform the desired interactions and then return to its local processing tasks. In most cases, the PC must emulate another device to accomplish this.

One way is to use an asynchronous link, which is the most familiar and also the least expensive. However, while this link is appropriate for some applications, its typical data transmission rate of 300 to 1200 baud can limit its usefulness. A synchronous link, on the other hand, has the PC emulate the 3274 control unit, operating at 1200 to 9600 baud. While faster than an asynchronous connection, the synchronous link ties up a dedicated port on the host that could be put to better use by a cluster controller that is capable of supporting up to 32 users.

Protocol converters are currently available that can emulate a remote 3274 controller connection to the IBM 3705 communication processor and communicate with the PC over a switched or leased asynchronous line. This type of converter provides the user with full-screen capability. It also permits access to the mainframe by a number of PCs. This method, however, is not very cost efficient.

Dan Erlin is founder and chairman of Forte Data Systems, 1500 Norman Ave, Santa Clara, CA 95050. Mr Erlin holds a BA in business from the University of Southern California.
Fig 1  Plugging a PC78/79 into an IBM PC lets the user fully emulate the IBM 3270 environment. The board and its associated software are transparent to the operating system, access method, and application. The board includes an RS-232 link that is MS-DOS compatible and allows the PC to attach to printers and other peripherals.

Although connection costs vary considerably, there are common factors to consider when estimating total costs. These factors include the necessary modems, communication lines, and host frontend costs. In general, the most economical connection is a PC-to-mainframe link via coaxial cable. Coaxial cable provides a ready-made data pathway, but currently many personal computers do not have access to that pathway. Also, the coaxial link is incompatible with the available personal computer’s communication interface.

Within the past year, however, a handful of companies have introduced circuit boards that fit into an available expansion slot in the IBM PC or XT and thus provide that essential coaxial link. The board permits PC connection directly to the category “A” coaxial cable of a 3274/3276 cluster controller. No modems, phone lines, or special cabling are required. In addition, the control unit can be channel attached or remotely attached using binary synchronous communication (BSC) or systems network architecture/synchronous data link control (SNA/SDLC) protocols through the frontend processor. The associated software enables the PC to emulate a 3278-type terminal/display unit.

Transparency as a goal

Forté Data Systems’ PC78/79 interface board and its accompanying software can be used with the IBM PC in any operating environment where a 3278/3279 terminal is appropriate (Fig 1). The PC78/79 is transparent to the operating system, access method, and application. The PC can thus fully emulate an IBM 3278, models 2, 3, 4, and 5, or in the case of a PC with color monitor, emulate the 3279, models 2A, 2B, and 3A (Fig 2).

The PC78/79 software allows all communication and emulation functions to be soft loaded. Future upgrades or enhancements are accommodated by swapping diskettes without making any changes in PROM. Having the functional ability resident on the disk also allows an easy adaption to various vendors’ hardware. It is not necessary to design a new set of PROMs for each manufacturer.

In addition, a file transfer utility, which uses special interfacing subroutines, permits downloading of data files to the PC. These data files can then be manipulated by PC-resident application software. Menu selection, under MVS/TSO and VM/CMS operating environments, performs file transfers. Interfacing subroutines used in the file transfer enable end users to also write PC applications that can converse with host applications through the processor board.

To make the IBM PC function efficiently in the emulation mode, its processor (the Intel 8088) must not be burdened with communication responsibility. In addition, a high speed microprocessor on the PC78/79 board provides complete 3278 line protocol compatibility and maintains an image of the current 3278 display screen. This image is available for

Fig 2  The micro-to-mainframe link can be established in two ways with Forte Data’s PC78/79. The control unit can be channel attached or remotely attached using BSC or SNA/SDLC protocols. Either way, the PC is linked to the controller via the category “A” coaxial connection.
Fight the protection racket.

Why pay for back-to-back zeners to get positive/negative protection, when a single Panasonic ZNR can provide complete, highly reliable circuit protection in either direction... and for less cost.

These zinc oxide nonlinear resistors also provide an excellent alternative to PC circuits and spark gaps. Their ohmic values change in less than 50 nsec when subjected to impulse surges, so their response time is fast... without the discharge lag conventional gap-type arrestors can't avoid.

Result: you can use them for ground fault interrupter circuits or input line transient protection. Use them in applications ranging from low-voltage switchboards and communications equipment to video displays and TVs. Use them anywhere you want an economical, efficient way to protect vulnerable AC and DC circuits against repeated high voltage transients (positive or negative), or such steep-rise surges as those caused by lightning, switching or noise spikes.

Providing excellent temperature and humidity characteristics, ZNR's are available in a wide varistor voltage range—from 22 V to 1800 V in the PC-mountable D Series and the top-connected, flange-mounted E Series, and in stacked types for voltages up to 26 KV. Surge withstand capabilities are from 50 to 2,000 amps in the D Series, or 2,500 to 20,000 in the E. Our D series includes several UL recognized numbers for line voltage applications. For complete details, samples and prices, write or call: Panasonic Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5256.

With one Panasonic ZNR transient/surge absorber instead of back-to-back zener diodes
presentation when the PC is in its emulation mode. The microprocessor's architecture allows concurrent and independent operation of host and PC programs. The operator need only strike a single command key to place the PC in the emulation mode or return it to the current PC program.

A serial RS-232 interface provides access to a local printer, modem, or other peripherals. The serial interface and the coaxial link are combined on one card. This frees an expansion slot that is normally allocated to IBM's asynchronous adapter board.

Under MS-DOS, the user has the choice of operating in a resident or nonresident mode. The emulator program can become a subroutine to DOS, thus allowing the operator to toggle between the host environment and the MS-DOS environment. While resident 3278 emulation may require the PC to be configured with an additional RAM, the advantage of freeing up disk drives or other system resources may warrant this configuration.

The ability to configure various other elements with the PC78/79 is an added bonus. Customer preferences of keyboard layout can be accommodated, such as converting the IBM PC layout to the conventional 75-key ASCII keyboard. The user can also define the PC colors for any of the 3270 fields. In addition, multiple displays and monitors can be configured.

**Eying the competition**

Converting the PC into an intelligent workstation replacement for 3278-type terminals has also been addressed by IBM. The company has announced shipments of an emulation adapter and control program to begin in April of this year. As in Forte Data's device, which was first shipped some 10 months ago, the connection will be made via the coaxial cable to the 3274 control unit.

A close examination of IBM's emulator package, however, reveals a certain lack of consideration for the end user. For instance, unlike Forte Data's incorporation of the 3270 and RS-232 interface on the same board, IBM lacks an asynchronous RS-232 interface. While both products allow screen copy of the 3278/3279 session to a supported printer that is attached to the PC, the PC78/79 provides easier screen capture to the PC-DOS file. Diagnostics are standard in the Forte Data package. In developing its emulator package, Forte Data has provided PC users with important benefits achieved with soft-loaded software. While the potential for PC-to-mainframe connections has not been completely exploited, the software emphasis has furnished users with the tools to completely integrate their system. PROM or ROM are not required to be replaced when enhancements and upgrades are developed. This is not the case with the IBM emulator package.

The two products differ in other respects, with each having strengths and weaknesses. However, if performance is the primary criterion, Forte Data's PC78/79 delivers more capabilities and flexibility.

**C for flexibility**

The source code for the PC78/79 is written in a high level C language that gives the end user good flexibility to modify the emulation program. The card is then used as an I/O device and software can be compiled under a different operating system. For example, the emulation program could be modified to be compatible with QNX, a Unix (Bell Labs) look-alike operating system for the IBM PC that is marketed by Quantum Software Systems, Inc (San Jose, Calif).

The PC78/79 card has an onboard parity-checked screen buffer that ensures consistency in the error checking system. Data is received with parity, buffered with parity on the circuit board, and then transferred to the application program with 100-percent integrity. For users who transfer numerical and statistical data files, this feature is especially important.

Identifying problems that occur during initial load or during operation can sometimes be difficult for the experienced operator and next to impossible for the novice. The Forte Data product includes two diagnostic modes to alleviate user frustration. First, power-on diagnostics are executed before the PC78/79 attaches itself to the coaxial line. In addition, local diagnostics, which are menu driven, can be run to isolate problems suspected by the user.

The diagnostic portion of the program, called INSTALL, appears as a separate DOS command to the user. When executed, it allows the user to ascertain the error, obtain information on corrections to make (via INSTALL), and then proceed to solve the problem at hand.

While the ability to interface with the mainframe greatly increases the PC's utility, the next generation of products should more fully integrate the PC into the mainstream of a company's data processing facilities. In order to take full advantage of the PC-to-host coaxial connection, users should be able to take data they have developed with PC applications and make that information available to the mainframe, and from there to other PC users on the network.

Forte Data is planning to follow that direction with future products. The emphasis will be on the communication requirements of the end user—to provide the operation with a much faster and easier transfer of data and data files. Access to the data
We have the components that make your disc drive, your printer print, etc., etc.

We have the electromechanical components you need for your computers and peripherals. And the responsiveness you need to keep your production rolling.

For memory units, we supply solenoids and a complete line of brushless DC motors designed for 5½" to 18" disc drives. And linear actuators that position read/write heads in precise digital steps.

For printers, we make rotary steppers and subfractional HP motors, and magnetic pick-ups.

For microcomputers, minis and mainframes, Airpax magnetic circuit breakers assure positive protection. They're unaffected by ambient temperature, and serve the dual function of power switch and overload protection.

And Airpax thermostats monitor cabinet temperatures, and shut down systems instantly when overheat threatens sensitive circuits.

You can select from our thousands of standard models. Or we'll create a custom model for you, and produce a few dozen for prototypes, or millions for a production run.


AIRPAX

We give you control.

CIRCLE 109
will be provided via familiar PC-DOS commands. Users should not be burdened with having to learn
the mainframe's operating system or contend with
separate communication software. In a word, trans­
parency will be the key to future enhancements.
Currently under development is a hardware/software
package that will offer four major functions: stor­
age capability of PC-generated files on the main­
frame, electronic mail capabilities, complete data
and file transfers between the host and the PC
environment, and availability to the personal com­
puter of the mainframe's batch processing facilities.
Future capabilities will allow the host computer
to be an information repository for PC-generated
data (Fig 3). Most personal computers have two
locally attached floppy disks for storage. This
slows down some tasks that are data intensive. If
the host computer can offload PC-generated data,
then this would effectively add a gigantic hard disk
drive to every PC on the network. Since the method
of communication is via the coaxial cable, which
permits data to be transferred at a rate of 2.35
Mbits/s, the PC user experiences no performance
degradation while maintaining the access speeds of
the floppy disk.
The disk space on the mainframe would be
accessible by any user who could link to the owning
user's director. This way, data could easily be
shared between PC users, even if located in
different buildings or separate locations. (Some form
of encryption or decryption would be needed to
maintain file security.)

Even though the file setup in the mainframe is
enormously different from setting up PC files,
Forte Data's new product would provide an almost
transparent method to transfer data. Commands
learned on the PC for manipulating floppy disks
would be usable to move files to the mainframe
and back again. This function would allow a PC
operator to capture live data from an online data
base and use the information in an electronic
spreadsheet or other computation. For example, a
company's accounting files would reside in the
mainframe and normally not be accessible to an
individual manager. Given the new capability, the
manager could retrieve the profit-and-loss state­
ments for the last six months from the online data
base and analyze the data on the PC using the
VisiCalc-like application program.
The overriding objective of the functions just
described is to increase the capability and produc­
tivity of the personal computer. Forte Data's
operating philosophy is to move the personal com­
puter away from acting as a standalone computer
to functioning as a truly interactive professional
workstation.

Please rate the value of this article to you by
circling the appropriate number in the "Editorial
Score Box" on the Inquiry Card.

High 731 Average 732 Low 733

Alpha's OMNIGUARD is a unique series of state-of-the-art electronic cables that are hazard-matched to perform optimally even in the most hostile environments. Select the proper Alpha OMNIGUARD electronic cable, and you can bury it, without conduit. Immerse it in water. Run heavy equipment over it. Drag it. Splash it with oil, gasoline, alkali or acids. Use it under ground or in outer space. And nearly anywhere in between. Without risk.

Alpha's OMNIGUARD is available in five distinct cable constructions, utilizing specific materials for specific needs. Depending on your application, you can select the appropriate armor, shielding and jacket color options. And you can order Alpha's OMNIGUARD in quantities as small as 100 feet.

For more information, call your local Alpha distributor or write for your free Alpha OMNIGUARD catalog. It features detailed selection criteria which will enable you to specify the right Alpha OMNIGUARD electronic cable for your most demanding requirements.

IT COVERS THE RISK.
THE EMULOGIC® ECL-3211.

SCREEN
Automatically updated full-screen display of all registers and system status.

FAST KEYS
They’re fast, direct, and don’t get in your way. The most user-friendly operator aid available today.

MAPPING
Full-speed, full-range mapping in internal, external, and mixed modes.
Single-word resolution.
Full-range offsets.

BREAKPOINTS
Eight 78-line real-time logical breakpoints for every chip, concatenated via logical switches and counters.

CF/LOG
Selects screen with all Command File and Log function options.

TRACE
Breakpoint-controlled 511 x 72-bit real-time trace with precise disassembly.

TIME BASE
Multi-sourced time base—internal synthesizer or target clock.

LOAD
Selects LOAD screen with all options.

SET
Selects screen with all SET options.

BREAKPOINT
Selects screen with all BREAKPOINT options.

MEM
Selects screen with all MEMORY options.

DIS
Selects screen with all DISASSEMBLY options.
STILL THE BEST MICROPROCESSOR DEVELOPMENT SYSTEM YOU CAN GET.
AT ANY PRICE.

WORLD'S BEST EMULATOR.
It's the best you can buy. Pure and simple.
Built around DEC's LSI-11 CPU's, RT-11, and a full range of DEC options like RL02 hard disks, the Emulogic general purpose emulator supports more chips from more manufacturers better than any other system.
With the ECL-3211 you can find your bugs in the lab, before your customers find them in the field. It lets you probe into things that other systems can't even see. In fact, you probably can't define a condition that the 3211 can't trap. And yet it's easy to use.

"NO-WAIT-STATE" EMULATION.
Up to the full rated speed of every chip with all features implemented. Doesn't steal any interrupts, stack pointers, stack space, or memory space. Handles all types of interrupts in any mapping configuration. Logical switches, counters, and trigger outputs manipulated in real time at no cost to user program.

COMPLETE HELP FACILITIES.
Our new "FAST KEYS" and Advanced Command Syntax make it a snap to learn to use. You don't even have to read the manual to get started.
And once you've used it for one chip, you don't have to learn anything new for the next chip. The screen format is uniform for all chips, and all system functions are the same. All you have to learn is the chip itself.

WORLD'S BEST DEVELOPMENT SOFTWARE.
More powerful and easier to use than any in the field, the software tools available with every ECL-3211 let you develop and debug software as readily as hardware. So system integration gets done effectively and on schedule.

DEC Operating System. RT-11 Version 5 is standard for stand-alone ECL-3211's. (RSX-11M and VMS for multi-user systems.) It's the latest update of the field-proven PDP-11 operating system.
Keypad Editor. Full-screen-oriented KED Keypad editor that makes full use of DEC terminal functions.
Assemblers/Linkers. MACRO-11-based cross-assemblers and linkers for every chip. Mnemonics identical to original chip manufacturers. Pseudo-ops and directives of MACRO-11. No relearning from chip to chip.
Pascal/C Compilers. Available for most chips, they are true cross-compilers that produce executable code that can be run on the ECL-3211 or the target chip. Permit linking of assembly-level and compiler-level symbols and include utilities for standard load module format conversions.
High-Level Debuggers. Permit user to modify Pascal and "C" variables in the format of the high-level language. User can debug completely within the high-level language without reference to assembly-level parameters.
Advanced Command Syntax.
Expanded HELP facility, new memory display and MOVE commands, greatly enhanced command file functions.

Now you can activate command files from breakpoints as well as the keyboard, include pauses for user response, nest multiple files up to five levels deep. With the new LOG command you can store any sequence of operations for later use.

MORE CHIP SUPPORT.
Emulation, simulation, and full software development support packages for the following chips:

- Now shipping
  - 8080
  - 8086
  - 8085
  - 68000
  - 8048
  - 6809
  - 8088

- In beta test
  - Z80
  - 6502
  - 6502S
  - 80186
  - 68010
  - 9989

Scheduled for 1984
- 80188
- 68008
- 68020

WORLD'S BEST MULTI-USER SYSTEMS.
If you need to coordinate the work of a team of hardware and software engineers, don't forget to check into Emulogic's multi-user systems:

- EMUNET-1. RSX-11M-based system for the PDP-11 family of host computers. Up to 15 users.
- EMUNET-2. VMS-based system for the VAX family. Up to 60 users. Easy migration from stand-alone ECL-3211's and from EMUNET-1.

For more information on the ECL-3211 or our multi-user systems, contact EMULOGIC, Inc., Three Technology Way, Norwood, MA 02062, 617-329-1031 or 800-435-5001.
EMUNET is a trademark and Emulogic is a registered trademark of Emulogic, Inc.
LSI-11, MACRO-11, PDP-11, RL02, RSX-11M, RT-11, VAX, and VMS are registered trademarks of Digital Equipment Corporation. Z80 is a registered trademark of Zilog, Inc.
that you can build a portable, battery-operated computer with built-in MODEM and LCD display that synthesizes speech, tells time, reads temperature, voltage, or MPH, drives your printer, relay, or robot's arm, times events, "sleeps" when it's not in use, and, lives in your briefcase!

And you can get all the ICs from Hitachi.

- CMOS 4, 8, 16-Bit Microprocessors
- CMOS RAMs
- CMOS ROMs
- CMOS EPROMs
- CMOS Real Time Clock
- CMOS Programmable Timers
- CMOS Peripheral Interface ICs
- CMOS LCD Drivers
- CMOS Speech Synthesizers
- CMOS Gate Arrays
- CMOS A/D Converters
- CMOS Logic
- LCD Displays

If you're planning some new "dream" product design (perhaps a computer that fits in a matchbox), give us a call. We've been doing the "impossible" in CMOS for some time.

For more information about the CMOS Family, contact your local Hitachi Representative or Distributor Sales Office.

FAST ACTION

To obtain product literature immediately, CALL TOLL FREE 1-800-842-9000, Ext. 6809. Ask for literature number 703.
Today, people are solving their back-up problems with this fast, reliable, 10 MB disk cartridge drive.

IOMEGA's 10 Megabyte cartridge drive outperforms most winchesters.
So you can back-up 10 Megabytes from your fixed disk in less than 30 seconds.
The easy to use cartridge sports the industry's lowest price tag, only $30 each in OEM quantities.
IOMEGA's imbedded closed-loop servo guarantees interchangability of cartridges between drives. And the standard interface is SCSI compatible.
Solve your backup problems with the fast, reliable IOMEGA 10 Megabyte cartridge drive.
Call IOMEGA for a personal demonstration. And ask about our OEM Special Evaluation Offer.
IOMEGA Corporate Headquarters, 4646 South 1500 West, Ogden, Utah 84403. 801/399-2171. San Jose, CA 408/263-4476.

IOMEGA

Copyright © IOMEGA 1983
Transputer—a programmable component that gives micros a new name

It is a cross between a computer and a system building block, like a transistor, and it executes 10 MIPS. The entire IMS T424 transputer consists of a small, fast processor, 4 Kbytes of memory, interfaces to external memory and peripherals, and four high speed communication links. The transputer can respond to external interrupts within 600 ns and support simultaneous block transfers between the peripheral interface, the four standard links, and memory without significant degradations in processor performance.

System architecture is optimized to execute Occam, a concurrent programming language that was used to design the transputer itself. This software sees the system as a collection of concurrent processes that communicate with each other and with peripherals through channels. Programs are built from three primitives: assignment, input, and output. Assignment changes the value of a variable, input receives a value from a channel, and output sends a value to a channel. The same Occam program that a transputer network executes can run unchanged by a smaller network or a single transputer.

The three processes combine to form sequential, parallel, or alternative constructs. A construct is also a process, and can act as a component for another construct. Conventional sequential programs translate into Occam via variables and assignments, which then combine to form sequential constructs.

Concurrent programs translate to Occam by combining channels, inputs, and outputs to form parallel and alternative constructs. Each channel provides a one-way connection between two concurrent processes that communicate when both are ready. An alternative process may be ready for input from any channel, so that input is taken from the first channel to be used for output by another process.

Besides Occam, the transputer processor can be programmed in industry standard high level languages, such as C or Pascal. The processor executes programs sequentially—it implements parallel processes by sharing its time between the process sets that are active at any instant. For example, a currently running process continues to execute until it requires I/O communication. At that point, the processor temporarily abandons the running process in favor of the next process on the active queue. When the processor communicates with a ready channel, the message passes to the waiting process, which then goes to the end of the active queue.

Supporting two priority levels—0 for high and 1 for low—the processor maintains a queue of active processes for each level. When there are no active priority 0 processes, the latency is typically 600 ns, maximum 2600 ns. (Latency is defined as the time from the instant an external channel is ready to the start of the first instruction of the relevant waiting priority 0 process). If a priority 0 process is already executing, the waiting process links to the end of the priority 0 queue.

Four standard Inmos high speed links provide transputer communication and a variety of network configurations. Each link has two Occam channels: an output, and an input to carry data and link control information. Links operate independently and provide block transfers between transputers. The sending transputer transmits messages as a sequence of bytes, then awaits an acknowledgment. This signifies that the receiving transputer is ready to accept another byte.

Transmission is continuous because the receiving transputer acknowledges as soon as it starts to receive a data byte. Moreover, this asynchronous protocol guarantees reliable transmission despite sending or receiving delays. During transmission, both processes are set inactive and will link to the end of their respective active queues only after final byte acknowledgment.

Software sets data rates on each link using the LinkSet configuration channel. Highest frequency is 20 Mbits/s for a maximum data rate of 1.8 Mbytes/s on a channel.

Separating the peripheral interface from the memory interface optimizes each one for its principal function. The memory interface supports mixed memory systems that generate signals for both nonmultiplexed and multiplexed memory. Memory timing is selected by a

(continued on page 244)
program or externally controlled by a wait signal. The 32-bit multiplexed data and address bus interface extends the internal address capability to 4 Gbytes in a single linear address space. Nonmultiplexed cycles provide timing signals to drive industry standard RAMs and ROMs, while the multiplexed cycle provides RAS and CAS control signals for external address multiplexers.

Memory cycle types can be externally selected after the address is outputted, so memory systems can be mixed. If required, an asynchronous wait input externally determines memory timings. Memory cycle times and refresh frequency can be set by a program through the ExtMemSet configuration channel.

The peripheral interface accesses industry standard devices such as controllers, memories, and microprocessors. Its 8-bit bidirectional bus inputs or outputs byte sequences. Two control lines address external devices, and an Event input provides interrupt capability. Accessed via four standard output and input channels, the interface allows all eight channels to use the same 8-bit data path. The processor initiates transfers via handshaking. Transfers are synchronized to a separate external clock; asynchronous operation is also permitted, but at a lower speed.

Externally addressable device connections to the interface use one output channel as the address channel, another as the write-data channel, and a third as the read-data channel. Both addresses and data can be arbitrarily long byte sequences. The 4-Mbyte/s data rate allows the connection of high performance peripheral chips without FIFOs or DMA controllers.

Similar to an interrupt, the Event input communicates with a waiting process to schedule it. Typical latency is 600 ns. This input also enables the peripheral interface to respond to an access from a standard microprocessor bus.

To summarize, the entire transputer incorporates a number of hardware processes that represent its main concurrent elements. First, the processor receives an Occam program through one of the transputer communication links and begins executing. Second, the link controllers determine the state of their channel pairs and communicate with external devices.

Meanwhile, the memory interface controller determines the state of the memory interface and communicates with external memory. The peripheral interface controller follows along the same lines. In turn, the processor communicates with these hardware processes using a set of standard channels that is program controllable. The entire transputer process results in concurrency needed for high performance systems. Samples of the T424 will be available in the second half of 1984. Inmos, PO Box 16000, Colorado Springs, CO 80935.

Circle 260

---

**Ever reflect on a career in the Nuclear Navy?**

Take a good look at yourself. Your life. You’ve worked hard to get where you are. But where are you going from here?

Today’s Navy can turn your scientific or engineering studies into a nuclear specialty that will make you a part of a professional team. And it may take you farther than you ever thought you could go.

From a cruiser loaded with the latest electronic equipment, to a giant nuclear carrier, you’ll get valuable technical training in the Navy. Plus good pay, travel, free dental and medical care and 30 days’ vacation with pay, your very first year. Not to mention more experiences than you’d get in a lifetime on land.

Interested? Take a closer look at today’s Nuclear Navy.

Motivated? Then today’s Navy would like to have a look at you. Because people like you are a good reflection on us.

Call toll-free: 800-841-8000 (in Georgia, 800-342-5855).

**NAVY. IT’S NOT JUST A JOB, IT’S AN ADVENTURE.**
DIALIGHT LED CIRCUIT BOARD INDICATORS STEP UP YOUR PRODUCTION BY ELIMINATING PRODUCTION STEPS.

You'll save money when you stop mounting LEDs on PC boards the old way — bending leads, inserting holders, adding resistors — and start using LED Circuit Board Indicators from Dialight. Mounting our LED Circuit Board Indicators is easier and less time-consuming. They eliminate production steps and reduce labor costs. Not only is positioning faster, it's far more accurate. As soon as you insert the assembly you are ready for wave soldering. Dialight originated the idea of packaging LEDs for easy mounting on PC boards. And we've developed over 50 different Circuit Board Indicators in red, green, yellow and red/green bicolor. Choose single-element LEDs or QUAD-LED™ four-element arrays with a wide range of voltages with or without current limiting resistors. Send for our catalog. And the next time you need LEDs for PC boards, eliminate steps and save money — specify Dialight. 203 Harrison Place, Bklyn., NY 11237 (212) 497-7600 TWX: 710-584-5487

DIALIGHT meets your needs.
A North American Philips Company
Low cost plotter combines graphics command set and offline operation

To meet the demand for multiple color, low cost graphics plotting, Enter Computer is producing a six-pen plotter at an end user price of $1095. The Sweet-P 600, or “Six-Shooter,” stores six fiber-tip, Rapidograph-type, or ball-point pens in a rotating carousel to provide six colors online. Additionally, carousels can be switched to provide several palettes for writing on either paper or acetate.

The Sweet-P 600 takes either 8 1/2- x 11-in. or 11- x 17-in. paper. The pen moves along a single axis, the X-axis, while the paper is moved back and forth on the Y-axis by gripping rollers. The smallest addressable increment is 0.004 in., and maximum plotting speed is 14 in./s. Repetition accuracy for any given pen is the minimum step size of 0.004 in., while repetition accuracy from pen to pen is two step sizes, or 0.008 in.

Among the techniques that have enabled this degree of accuracy at a low cost is the use of stepper motors controlled by a microprocessor using ROM-based microstepping routines. The 600 also contains 19 internal character sets, including katakana, and a Sweet-P graphics (SP/GL) command set. The command set includes line, curve, and point drawing; axis and tick drawing; and routines for drawing and filling rectangles and wedges.

The Sweet-P 600 is also compatible with the Hewlett-Packard graphics language (HPGL) so that software written for the HP 7400 series plotters can also run the 600. In fact, there already exists a considerable large body of software packages from over 25 independent software vendors to run the Six-Shooter on a variety of computer systems including Texas Instruments, IBM, Digital Equipment Corp, Wang, Apple, and a variety of MS-DOS and CP/M systems.

The Six-Shooter has both RS-232 serial and Centronics-compatible parallel interfaces and can be used in an “eavesdropping” mode for a multi-user environment. There, it is placed between microcomputer and printer or between terminal and mainframe, and performs tasks when specifically instructed to do so. This is made possible by the 2-Kbyte buffer supplied or by using the optional 8-Kbyte buffer to download tasks. Even in a single-user microcomputer environment, the plotter can operate without tying up the computer resources, except to receive additional downloaded tasks.

Enter Computer, Inc, 6867 Nancy Ridge Dr, San Diego, CA 92121. Circle 262
Put powerful instrument control at your fingertips.

The new Fluke 1722A Instrument Controller combines the computational ability and interfacing flexibility you need with the rugged packaging and easy-to-use human interface your factory demands. All at a new, low price. Now you can integrate your next factory test, process control or OEM system faster and put your people to work sooner.

The power of the 1722A is a 16-bit single-board computer with 136K bytes of main memory. Its 12 MHz speed puts it in the same class as many minicomputers. Four programming languages are available to simplify programming, including Interpreted and Compiled BASIC, FORTRAN and Assembly. Each includes special adaptations for controlling IEEE-488-compatible programmable instrumentation. And if you already own a 1720A Instrument Controller, you can run existing software on the 1722A—without modification.

The modular mainframe easily mounts in a standard 19 inch rack and allows you to configure the interfaces and memory to your exact needs. The IEEE-488 (1980) and RS-232-C interfaces can be expanded with an optional IEEE-488 and RS-232-C interface card, parallel interface card or dual serial interface card. Onboard memory is expandable to 2.6M bytes with RAM cards or 1.4M bytes with bubble memory.

The 1722A's touch-sensitive display dramatically simplifies system operation. Once programmed, your system can be operated entirely from the CRT. The 1722A displays only the pertinent options, allowing you to structure the user's response to a system. This helps reduce mistakes and increase throughput.

The 1722A is priced at $7450 (U.S. list), including BASIC Interpreter, documentation and a limited one-year factory warranty. So get in touch with your local Fluke Sales Engineer or Representative. Or call us toll free at 800-426-0361 for more information.

IN THE U.S. AND NON-EUROPEAN COUNTRIES: IN EUROPE:
John Fluke Mfg. Co., Inc. Fluke (Holland) B.V.
P.O. Box 6060, M/S 250C P.O. Box 5053, 5004 EB
Everett, WA 98206 Tilburg, The Netherlands
(206) 356-5400, Tlx: 152662 (011) 6115973, Tlx: 52237

Use the new graphics capability of our 16-line, 80-character touch-sensitive display to create more effective operator prompts.

Copyright © 1983, John Fluke Mfg. Co., Inc.
All rights reserved.

Ad No. 4817-1722

CIRCLE 116
Laser-based optical disk drive stores 1 billion bytes

Digital Disc GD 1001 has features that set it apart from traditional recording technologies. Based on a solid state diode laser, the drive provides a 210-Mbit/in.\(^2\) (33-Mbit/cm\(^2\)) recording density and a 4.1-Mbit/s disk transfer rate. With three access methods—random, optimized random, and sequential—the drive allows direct access to any sector in the read or write mode and 3-ms access times within a band.

Because of its disk format, the read/write unit is easy to operate and highly reliable. The unit consists of an optical unit, optical head, linear motor, rotation motor, and a set of logic boards. The optical unit consists of a semiconductor laser module and a photo detector, while the optical head is actuated for both radial and vertical positioning of the laser beam (fine access). The linear motor provides the coarse access by moving the optical head and focusing it on the target track area. The rotation motor, on its axis, includes a disk seating and clamping device. Finally, the logic boards control servomechanisms and disk accesses.

A 12-in. (305-mm) diameter cassette encased disk eases all handling, storage, loading, and unloading operations. Each disk is preformatted in tracks and sectors. A sector can be directly accessed by its logical address. A spiral track organization allows continuous writing and reading of information streams. Once recorded, a physicochemical process (plastic copies) can entirely replicate a disk in one step.

The powerful automatic error detection and correction feature guarantees effective disk capacity. In addition, it maintains records at the quality level required in data processing environments, even after numerous years in archival storage. Data-handling software is kept simple since each record is physically located at a programmer-defined address. This eliminates the need to check physical copies of the disk. The user is kept informed on the level of difficulty that the error correction process has met each time a record is read back. This lets the user check file integrity. The optical disk will sell in the range of $6000 to $9000; the media range from $200 to $300. Thomson-CSF Communications, 360 N Sepulveda Blvd, El Segundo, CA 90245.

Open architecture characterizes programmable handheld computer

A versatile tool for technical professionals, the HP-71B is optimized for numeric computation and calculation. In contrast with earlier policy, Hewlett-Packard is providing extensive documentation on the unit's internal workings, and is actively seeking third-party vendors for software, hardware, and HP-IL products.

Based on a 4-bit processor, the computer accesses up to 1 Mbyte of virtual memory by bank-switching. It has an operating system, Basic, and a sophisticated calculator mode in 64 Kbytes of onboard CMOS ROM, as well as 16 Kbytes of CMOS RAM. At present, four slots below the front edge of the keyboard accept 16 Kbytes of RAM, 256 Kbytes of ROM, or any combination of the two. Only the size of available CMOS static chips limits plug-in memory.

At power-on, the operating system checks installed memory and configures it automatically. Thus, segmentation is transparent to the user's application program. Expanded ROM Basic includes enhancements for statistics, trig functions, and IEEE floating point math.

This spring, application ROM packages will be released for math, engineering, surveying, and text editing, as well as Fortran and assembly language development systems. Software comes in ROM, cassette tapes, or magnetic cards.

Interfaces for a magnetic card reader (photo upper right) and HP-IL connector (left) enable the unit to read and store programs. The reader plugs into the back of the unit, and the HP-IL connector inserts into a slot on the left. In addition, HP-IL controllers for the IEEE 488 bus, RS-232, and GPIO interfaces equip the unit to work with a broad range of peripherals.

The 8 x 132 dot-matrix LCD shows 22 out of 96 possible characters on the input line. This keyboard-controlled window scrolls horizontally as characters are entered. Alternately, an ASCII terminal can be the display device under control of a small Basic program.

Key definitions on the QWERTY-style keyboard are controlled by the gold “F” and blue “G” keys. Keyfiles, Basic extensions, simple display graphics, auto-start, and other programming aids facilitate custom features. The basic unit, with 16-Kbyte RAM and 64-Kbyte ROM, costs $550. Hewlett-Packard Co., 1000 NE Circle Blvd, Corvallis, OR 97730.

Circle 263

Circle 264
Introducing the World’s First LSI-II Emulating Multifunction Disk/Tape Controller.

Say hello to SPECTRA 25, the cornerstone of our new family of high-performance disk/tape controllers designed for use with DEC’s LSI-II computer.

This revolutionary O-Bus compatible single quad board lets you interface any combination of two SMD disks and four formatted 1/2-inch tape drives. By using extended commands to program the onboard E²PROM, you can easily select drive mixing, mapping, and many other features—all without removing the controller from the system.

The SPECTRA 25 emulates DEC’s RM02/5 and RM80 disk subsystems, and DEC’s TSII tape subsystem. It also provides complete emulation for operation with DEC’s RT-II, RSX-11M, RSX-11M-PLUS and RSTS/E operating systems.

To further enhance system performance, Spectra Logic offers SPECTRA STREAM™ software, a streaming tape backup utility that can back up an entire 80MB drive in only seven minutes.

Spectra Logic first introduced the multifunction concept back in 1979. And we’ve been quietly revolutionizing the market ever since with families of controllers that provide the high-performance, proven reliability, and added value you need to stay competitive.

We also offer the industry’s most comprehensive one year warranty, responsive nationwide service, and ongoing technical support.

SPECTRA 25 is the latest innovation in controller technology from the company with peripheral vision. Spectra Logic. For further information, including complete technical specifications, call or write us today.

Spectra Logic Corporation
1227 Innisbruck Drive, Sunnyvale, CA 94089
(408) 744-0930 TWX 910-339-9566
TELEX 172524 SPL SUVL

International Sales Office:
Belgium (32) (2) 5134892

SPECTRA STREAM is a trademark of Spectra Logic Corporation. © 1983 Spectra Logic Corporation

CIRCLE 117
Compact station engineers hierarchical VLSI design system

A high end design station called the MegaLogician combines powerful mainframe simulation with the verification functions of a breadboard in one desktop package. Its Ethernet interface controls integrated network communications between workstations, file or print servers, and mainframes. By simulating up to one million gates and making 100,000 evaluations/s, the MegaLogician is said to improve performance 100 times and capacity 10 times over existing design stations. Future capacities of 10 million gates are projected.

Graphics capability and automatic feature extraction help build circuits from the ground up. Database structure and architecture, including Intel's 286 CPU and a proprietary microcoded TTL circuit emulator, permit fast switching between different circuit views at any level of complexity. Changes in viewpoint (eg, from gate to functional level) take place within 3 s.

Gate-level editing describes in detail and manipulates individual gates and interconnections. Timing information for gates built from different processes, as well as interconnect lines, feed into logic simulation and timing verification programs. Multigate structures appear as functional blocks, and store as modules for future use. Text descriptions of finite state machines can be created or generated from flowcharts; PLA or ROM masks designed; and FPLAS, PALS, PROMs, and erasable PROMS programmed directly.

The behavioral level generates fault simulation and test programs for both individual circuits and for complete systems. Designers can model the effects of particular software programs or interrupt schemes and alter circuits as required.

The knowledge-based simulation process takes the net list produced during preliminary design and generates lists of “simulation primitives” corresponding to the circuit gates. Different primitives represent particular processes, such as CMOS and NMOS, and accurately model circuit parameters when “executed” by the simulation hardware. In essence, these primitives are microcode instructions for a specialized emulation engine. As the simulator executes its instructions in sequence, it accumulates timing and circuit performance information. This data is stored on disk.

The MegaLogician has 1 to 6 Mbytes of main memory, 4 to 8 Mbytes of simulation memory, a high resolution monochrome or color graphics terminal, a 40-or 80-Mbyte Winchester disk, and a 1-Mbyte floppy disk. System architecture supports up to 1-Gbyte virtual memory. Standard configuration costs $120,000. Daisy Systems Corp, 139 Kifer Ct, Sunnyvale, CA 94086. Circle 265

Condensing architecture makes small system perform big

The Eclipse MV/8000C can address 4 Gbytes of virtual memory and is program compatible with other Eclipse MV/ family computers. Using bit-slice architecture and a pipelined instruction processor lets the system run at a 220-ns microcycle speed. The compact 10.5-in. high rackmountable system uses both 256-Kbyte dynamic RAMs and gate arrays for its compact power.

The instruction processor interprets instructions for execution. After receiving an instruction sequence, it keeps up to four in a pipeline at one time. This achieves one onsite instruction execution every microcycle. It simultaneously executes one instruction while it decodes a second and fetches a third. A 1-Kbyte instruction cache that is directly mapped to the system cache buffers the system. Transferring instructions from the instruction cache and data from the system cache to main memory occurs simultaneously for improved performance.

Both system cache and main memory reside on a single 15- x 15-in. board that uses 2000+ custom gate array circuitry. The 16-Kbyte system cache ports to both the CPU and I/O system. With a 150-ns cycle time, it functions as a lookahead and lookback buffer for the system. Transfers between system cache and main memory occur at a rate of 16 bytes in 550 ns for a write, and 16 bytes in 440 ns for a read.

When memory control receives an address from the system cache, the circuitry addresses specific memory locations and performs error checking and correction on data transfers between the bank controller and main memory. It also provides byte parity checking on data transfers from the system cache. Each main memory location is put through a check at a 2-s/Mbyte rate. At the same time, refresh operations are performed on the 64- or 256-Kbit DRAM-based memory array.

As a hardware accelerator for the demand paging subsystem, the address translation unit (ATU) eliminates processor overhead for page translations. It maintains a table of recently referenced page addresses, using the fact that during processing, memory references tend to cluster in page groups that are repeatedly referenced. The 265-page table is stored in the ATU cache. When a program requests a page, the hardware first checks for the page location in the ATU cache. This relieves the processor from having to regenerate the translation for every page reference.

Other system features include an eight-level hierarchical security system, the full MV series instruction set, and a three-level independent I/O subsystem. The 32-bit system is priced at $55,500 for one, and $40,515 each in quantities of 20. Data General Corp, 4400 Computer Dr, Westboro, MA 01580. Circle 266
BUSINESS COMPUTING
THE PC MAGAZINE FOR BUSINESS

We're going to help you like no one else can.

The name of the business game is to get the greatest value out of your IBM Personal Computer or Compatible. And that's why our name is so important to you: Business Computing.

For starters, Business Computing is not a computer publication for technical people. It's a business publication written exclusively for people who use computers to generate better operating results.

This means no "computer speak," no jargon, no program codes, no games. Just clear, well-written business computing editorials on important subjects like Planning, Forecasting, Cash Management, Financial Modeling, Tax Planning and Project Management.

Here's how we help you each and every month.

Without software, your computer is useless. So our first responsibility is to keep you thoroughly up-to-date on what's available and how well it works. We'll try to keep you away from the lemons and steer you towards the best performers.

And we'll support it with case histories about business and professional people just like you to help you get the maximum value from your IBM PC or Compatible.

Plus you'll get the latest new-product information, a calendar of special events and seminars, and much, much more... all in one, convenient source: Business Computing, the monthly business-computing magazine for you, the IBM PC user.

And now you can get all of this valuable information for just $14.75, saving you 50% off the newsstand price. And your satisfaction is totally guaranteed. You can cancel at any time and get a complete refund. So subscribe today.

To subscribe: Just return the coupon or, for faster service, call toll-free: 1-800-331-2333. (Please call between 8:00 a.m. and 4:30 p.m. Central Time.) In Oklahoma, Call: (918) 835-3161.

To order circle Reader Service Number 118

Yes! Please send me 12 monthly issues of BUSINESS COMPUTING at the low annual subscription rate of $14.75 — 50% off the newsstand price.

□ Canada/Mexico $17.30 □ International $19.70 □ Please bill me.
□ Payment enclosed. □ This is a renewal.

Card # Bank # (MC Only)

Card type: □ MasterCard □ Visa □ American Express

Expires Signature

NAME (PLEASE PRINT OR TYPE)
TITLE
COMPANY
ADDRESS
CITY STATE ZIP

□ I currently own an IBM PC.
□ I do not own an IBM PC, but I am considering buying one.
□ I use an IBM PC at work.
□ I own or am considering an IBM-compatible computer.

Mail this coupon to: BUSINESS COMPUTING
Circulation Department
P.O. Box 815
Tulsa, OK 74101

S004
Winchester/floppy controller rules over diverse disk selections

Occupying only 16 memory locations, the GMS6529 intelligent module can control three Winchesters and four floppies. Its five onboard processors cover functions ranging from communication to error correction. They perform specific functions at maximum speed with minimal operating software.

A master single-chip processor operates at a 10-MHz clock speed. It performs all communication between the system and control processors and sector buffer RAM. The second processor works with a custom data separator device to perform all read/write operations to the disk. Used to lock phase locked loops to the incoming clock, it also drives some 8-in. floppy signals.

The third processor controls the 5½- and 8-in. floppies. The floppy controller contains a built-in data separator, write precompensation, and all seek functions. The fourth processor, as an error correction/detection unit, can automatically generate ECC or CRC on data stream. When it detects an error, it automatically corrects up to a 5-bit stream on a single data burst. A retry will also automatically start if the data cannot be corrected. In addition, this processor generates and verifies CRC/ECC on both data and ID files.

Finally, the fifth processor is an optional DMA device that transfers data to/from sector buffer RAM onboard to/from system RAM. It speeds the transfer rate by up to 10 times (when used in the halt burst mode) or 4 to 5 times (in halt steal mode). Another advantage is the decrease in user software needed to read/write to and from floppies or hard disks. A programmable counter generates a DMA grant signal that is normally generated by system processors. However, not all processors have this capability, so with the counter, the DMA option can be used with all four types of processors used in the single-board computer (6802, 6802, 6809, and Z80).

In addition to the five processors, a versatile interface adapter provides two ports for custom applications. The first port with eight I/O lines reads a DIP switch. The switch positions indicate to the operating software the following parameters: file booting, drive size and density, and whether or not a removable hard disk is installed. The other port performs hard disk removable functions, such as the disk being removed, write protected, and cartridge changed. This port is also used to format hard sectors and to generate system interrupts.

The controller is burned in for 72 hours and carries a full-year warranty. It is priced at $387 in 100-piece quantities.

General Micro Systems, Inc, 1320 Chaffey Ct, Ontario, CA 91762. Circle 267

Portable operating system easily adapts to specific microcomputers

Serving as a general-purpose microcomputer operating system, SI has several characteristics that distinguish it from other operating systems. Its machine independence and building block construction provide flexibility, while realtime facilities and machine language implementation deliver performance.

Taking user requests, a command processor causes appropriate programs to run. There are three types, all of which can reside in a single system. Switching between them occurs with a single command. The conventional processor accepts lines typed into the terminal, decodes the command into names and operands, loads the appropriate command program, and then gives it control.

The menu processor displays the command choices. The prompting processor is used like the conventional one. However, omitting required operands does not cause an error message to be printed and the command discarded. Instead, it prompts for each operand.

Any complete program can be used as a command. The system provides several commands, including assemble, back up, charge, clean, debug, and link. Other commands arise from word processors, spreadsheet programs, compilers, and interpreters.

A command list is a command sequence in a file. It is used like a command but is easier to compose. A file with commands executes directly. Ordinarily, each command will be invoked when the preceding one has finished. The command process provides a language for controlling command execution. Unlike conventional programming, changing a command list only involves its editing. No recompiling or relinking is needed.

System variables comprise the names and values that SI associates with the system information. They provide a way to alter the appearance and behavior of SI without rebuilding the system. The set command changes system variables, which the user can directly examine, set, and alter from a running program.

The system adapts to specific hardware on three levels. Moving SI from one architecture to another requires rewriting the code generation part of the compiler. To change system facilities, commands create a new system copy that includes or excludes particular features. To add a new device, the only requirement is a subroutine that acts as the device driver.

Currently available versions run on the 68000, Z80, 8080, 8085, and 8086/88, with versions planned for the 80186/286 and the 16032. Prices range from $200 to $1100.

Multi Solutions, Inc, 660 Whitehead Rd, Lawrenceville, NJ 08648. Circle 268
Here's Why

Precision Visuals

Is Now The Leader In

Graphics Software Tools!

One Program
Drives Many Devices

This single advantage can save you hundreds of hours of programming time. It enables you to use your hardware (both host computer and graphics devices) to its fullest. It protects your software investment against obsolescence and frees you from exclusive ties to hardware vendors.

Precision Visuals currently offers tailored interfaces for over 30 graphics devices from these companies: AED □ Applicon □ Calcomp □ Calcomp lookalikes □ Chromatics □ DEC □ Digital Engineering □ HP □ Houston Instruments □ IBM □ Imlac □ III □ KMW □ Megatek □ Pritronix □ Ramtek □ Raster Technologies □ Sanders □ Selanar □ Servogor □ Tektronix □ Tektronix lookalikes □ TI □ Trilog □ Versatec □ Visual Technology □ Zeta.

They Run On Most Popular Computers

Including IBM, VAX, PRIME, Hewlett-Packard, CDC, Honeywell, Data General, DEC 10/20, Harris, Univac, Cray, and DEC PDP-11.

Precision Visuals software tools require a surprisingly small amount of computer resources. Even on smaller machines they provide access to the full capabilities of the CORE graphics standard.

“...At Martin Marietta, DI-3000 serves as a common interface between our numerous graphics devices and software applications. We use DI-3000 for applications including structural analysis, business charts, graphs, animation, 3D modeling, and general-purpose graphics.”

Karin Bruce
Senior Graphics Software Engineer
Martin Marietta Denver Aerospace

Rich Capabilities Mean Limitless Applications

Precision Visuals software tools are proven in applications such as computer-aided design, business graphics, process control, mapping, geological data analysis, document layout, plus many specialized applications. System integrators (OEMs) use them as the graphics nucleus in turnkey systems and as the graphics component of database management and financial modeling systems.

$12,000 For Our Most Popular System

DI-3000*, the core system, starts at $8,000 and goes to $12,000 for our most powerful and best-selling level. Add $6,000 for GRAFMAKER**, the business presentation specialty system, and you’ll have one of the most versatile graphics systems available at any price. Other popular options include the METAFILE SYSTEM for a device-independent picture library, and our new CONTOURING SYSTEM for advanced surface graphics. These are single-CPU, end-user, U.S. list prices. Multiple CPU and OEM discounts are also available.

Find out how Precision Visuals graphics software tools can open a new world of flexibility, economy, and standardization for your graphics applications. Call us at 303/530-9000.
Control an orchestra
With one single chip.

Imagine a dynamic RAM controller that can access large banks of memory without missing a beat.
One that can handle the new generation of 256K DRAMs. And is fast enough to let your 16-bit system run at top speed. Without creating wait states.
With our new single-chip 74S408-2 and 74S409-2 DRAM controllers, you can reduce access times by 20 percent. And control more DRAMs than ever before.
Up to 88, to be exact.
A job that used to require up to 15 discrete parts.
So you save board space. Money. And design time.
Without sacrificing speed.
DRAM controllers from Monolithic Memories.
They’re helping orchestrate the fastest systems yet.
Find out how they can help you. Call your local Monolithic Memories representative today. Or write Monolithic Memories, 2175 Mission College Blvd., Santa Clara, CA 95050.

©1983 Monolithic Memories, Inc.

IdeaLogic. The big idea in system design.
(Them)
There are a number of infant CAE companies. But we've been supplying CAE workstations for the past 18 years. As an example, our software has already designed over two million PCBs. So if you're considering CAE systems, you can safely overlook all the two year olds. Simply look over the only 18 year old.

Racal-Redac
The world's most advanced CAE company.

4 Lyberty Way, Westford, MA 01886  (617) 692-4900

CIRCLE 121
Amnesia victim.

Without reliable battery support, your microprocessor-based product's volatile memory could get a bad case of amnesia ... with your customer as the ultimate victim. But if you're using Panasonic Lithium Batteries, your memory's getting maximum protection ... at a price that's competitive with mercury and nickel cadmium systems.

Our gasless, hermetically-sealed Lithium batteries are ideal for long-term memory applications in computers, office equipment, home appliances, even watches and calculators. They come in a variety of packages to suit your design: cylindrical, coin, pin or PC board-compatible Memory Mount types. Most sizes are available from stock. And don't worry about shelf-life: tests have proven that our Lithiums retain in excess of 95% of their original energy output after 10 years.

If you're concerned about losing your memory -- and don't want to make your customers 'amnesia victims' -- remember to specify Panasonic Lithium Batteries. For complete data on our full Lithium line, write or call today: Panasonic Industrial Company, Battery Sales Division, One Panasonic Way, Secaucus, NJ 07094; phone (201) 348-5266.

*Recognized under the Component Program of Underwriters Laboratories Inc.

* Does not include type BR-C.

Panasonic®
just slightly ahead of our time

Panasonic lithium batteries
Converter for dumb terminals

Protocol converter allows access to IBM mainframes and provides a communication path for 12 async devices. The Micro7400 has all standard 3270 capabilities and, in addition, it offers the ability to switch between two IBM hosts or between an IBM host and a minicomputer. A command port allows alteration of parameters such as priority assignments, and provides monitoring, diagnostic, and control facilities. Five models are offered with prices beginning at $2250.

Micom Systems, Inc, 20151 Nordhoff St, Chatsworth, CA 91311.
Circle 269

Communication processor

Designed to serve as a hardware engine for a range of standard communication protocols, the ICP is an intelligent processor that handles 2780/3780 and X.25 protocols. Peripheral I/O and other communication-related functions are off-loaded to raise throughput. As a terminal controller it uses ITH software to reduce the number of interrupts sent to the CPU. Interfacing to serial terminals at rates to 9600 baud, the software buffers the main processor by assembling character blocks in local memory. The unit costs $3950.

Zilog, Inc, 1315 Dell Ave, Campbell, CA 95008.
Circle 270

Protocol converters

Enabling ASCII terminals to communicate with IBM hosts, the series 100 emphasizes the price/performance factor. To IBM hosts, the devices are indistinguishable from IBM peripheral controllers. Terminals and printers supported by the series 100 appear to the host as IBM peripherals. Model 176 supports seven personal computers. Model 167 allows 3767 users to substitute low cost ASCII terminals and other peripherals for IBM SNA/SDLC devices. Pricing for the series starts at $2850.

Circle 271

Frontend processor

The 6100 communication subsystem allows Nonstop II and TXP systems to manage several hundred communication lines simultaneously. Data rates are up to 56,000 bits/s. Three transmission types (asynchronous, byte synchronous, and bit synchronous) and two line disciplines (point-to-point and multipoint supervisor) are available. It is microprogrammable on a per-line basis allowing different protocols, line disciplines, and line speeds to be mixed in a single system. Price is $23,900.

Tandem Computers, Inc, 19333 Vallco Pkwy, Cupertino, CA 95014.
Circle 272

Packet-switched network

The Sopho-Net network allows previously incompatible equipment to communicate freely, while it remains transparent. Node throughput rates are in excess of 1500 packets/s, node transit times are less than 20 ms, up to 4000 lines can connect to a node, and any number of nodes can make up a single network. The system carries all types of traffic: data, text, and image, and can superimpose any on the other. Systems are connected to the network in their native protocol so no hardware or software modifications are necessary.

Phillips Telecommunications Industries, PO Box 32, 1200 JD Hilversum, The Netherlands.
Circle 273

Two-unit processors

Improved design equips Comten 3650 communication processors to terminate up to three times the number of SDLC communication lines at the processor. The frontend and remote units support two hosts without an expansion cabinet. In addition, two improved price/performance models (88 and 88) manage up to 16 communication lines, 512 Kbytes of memory, and two hosts. Several configurations are available.

NCR Comten, Inc, 2700 Snelling Ave N, St Paul, MN 55113.
Circle 274

Fiber optic transmitter

Capable of speeds up to 100 Mbaud, the HFBR-1203/1204 operates at distances in excess of 1 km. The high optical power—7.4 dBm when coupled into 100/140-μm fiber—allows for applications in LANs and high speed computer links. Optical coupling scheme keeps optical power variation within 5 dB. An etched-well, 820-nm emitter provides thermal conduc­tion for the high optical power. In quantities of 100, the transmitters are $66 each.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 275

Virtual circuit switch

The Datakit VCS is a kit of compatible hardware modules assembled to provide a highly efficient network of terminal-to-computer and computer-to-computer communication. Architecture is designed to handle different protocols simultaneously. With the hardware, communication hubs link to LANs, and each link provides high speed transmission with low delay. The network uses a star topology with host computers at the center.

AT&T Western Electric, 222 Broadway, New York, NY 10038.
Circle 276

Digital line interface module

The MH9700 thick-film hybrid module provides 256 kbits/s of full-duplex communication between digital terminations over two common twisted-pair telephone cables. It shares the 2.048-Mbit/s, 32-channel, 8-bit/channel serial transmission format designed for PCM encoded voice and digital data. The module uses any four 64-kbit/s channels from a ST-BUS interface at the network port. In addition, it provides a line port and a microprocessor port. Switching is with asynchronous or synchronous data between any of the three ports. In a 40-pin DIP, price is $96.25 in lots. Mitel Semiconductor, PO Box 1663, Buffalo, NY 14203.
Circle 277

March Preview
Watch for a special article on printer technology
Integrated modems

The 2400-, 4800-, and 9600-bit/s modems offer reliability with LSI circuit design, compatibility with Omninux MUXES, and backward compatibility with modems. Switches mounted on the front change operating parameters. Loopback test functions speed system fault isolation. The 2400-bit/s modem is compatible with the 24-LSI Mark II modem and meets CCITT V.27 bis recommendations. Pricing begins at $700. Racal-Milgo, 8600 NW 41st St, Miami, FL 33166.

Distributed processing LAN

A LAN software system offers compatibility with both Unix and mixed MS-DOS/Unix environments. Designed to run on IBM PCs, it allows sharing of all devices and unrestricted files on a system. The software will turn each node into a window on the entire network and on connected networks through gateways. Software can be stored in a few centralized places and downloaded to any computer on demand. An unlimited license costs $250,000; 500-node costs $50,000, with basic licenses at $10,000, plus $200 a node. Phoenix Software Associates Ltd, PO Box 207, N Easton, MA 02356.

Networking extras

Additions to DECnet include an interface to connect all Q-bus micros, three Ethernet servers, remote fiber optic repeater, and supporting software packages. The Degna uses the 14400 transceiver and cabling to connect the computer to Ethernet coaxial cable. It operates at a 10-Mbit/s rate and provides both physical channel and data-link functions conforming to the latest specs. Price is $1150. Communication servers link Ethernet to other networks. Prices range from $17,000 to $26,995. Repeater enables designers to configure large Ethernet configurations up to 1000 m through a fiber optic link. Cost is $4400. Digital Equipment Corp, 10 Main St, Maynard, MA 01754.

Protocol conversion

Model 870 converts binary sync protocols into async, emulating the IBM 3270 cluster controller. The modular converter supports devices from one to eight channels each with its own microprocessor. The micro offers faster async conversion and the capability to support 256 terminals per host port. A rotary switch selects the data transmission rate, which ranges from 110 to 19,200 bits/in. An auto-baud rate detect feature determines the correct baud rate for each terminal. CRT controls are individually remapped for each terminal line, allowing full emulation. Cost of a basic system is $3395. Kaufman Research Manufacturing, Inc, 145 E Dana St, Mountain View, CA 94041.

Limited-distance modem

The LVS 76.8 allows thumbwheel-switch selection of eight sync speeds from 2400 to 76,800 bits/s. It operates at other speeds via an outside clock. At maximum speed, it can send data 5000 m on a typical 22-gauge wire. Either EIA RS-232-C or V.35 interface is available. The modem is programmed to provide standard EIA and line loopback testing from either end of the line. Prices range from $650 to $725. Complexx Systems, Inc, 4930 Research Dr, Huntsville, AL 35805.

Floppy disk controller

As a single-board STD bus device, the LSB-7810 simultaneously controls up to four disk drives in any size and format combination. An optional DMA controller frees up the host during disk transfer and provides full vectored interrupt capability. Interrupts are jump selectable. All drive parameters and sector lengths are software programmable for each drive. Quantity-one price is $280, plus $35 for the DMA controller. Axis, Inc, 7825 Engineer Rd, San Diego, CA 92111.

Multibus floppy controller

The V8004 supports both 5¼- and 8-in. disk drives, providing oncard data separation and double-density write data pre-compensation. Proper clocks are under software control for the disk being used. There are no oncard adjustments. Disk cable terminations mount in sockets for easy replacement. Fabricated with multilayer printed circuits, the card is a single-wide iSBX module 100 percent compatible with iSBX specs. Unit costs $450. Century Computer Corp, 14453 Gillis Rd, Dallas, TX 75234.

Intelligent controllers

The series 6000 attaches ESDI/ESTI disk and tape drives to a variety of host systems. The host computer bus is the SASI bidirectional bus interface. Both kinds of drives attach to the bus without sacrificing performance characteristics. Controller chip set features consecutive sector transfers, 2-Mbyte host data transfer rates, and intelligent buffer management. In 1000s, prices range from $225 to $350. ONIT, 557 Salmar Ave, Campbell, CA 95008.
“BUBBlES IRE HElPING NIXDORF BREAK INTO NEW SALES FIGURES.”

| 88112 55405 |

megabit of non-volatile memory. Capable of storing thousands of codes for any store.

The solid state bubble also outperforms disks and floppies in this demanding environment. Which means Nixdorf’s memory system runs maintenance-free 24-hours a day. So the downtime that means “no sale” is prevented. And the bubble’s high speed access even helps keep check-out lines moving.

The 7110’s small size also helps make Nixdorf’s stand-alone system self-contained and modular. So the system fits smoothly into any size retail organization, can be easily networked, and can grow as the store’s customer base grows.

Even if its customer base grows as fast as Nixdorf’s.

Whatever your line in electronics, Intel bubbles just may be the break you’ve needed.

So write us for more information.

Lit. Dept. Y7, 3065 Bowers Avenue, Santa Clara, CA 95051.

Or call us, toll-free. (800) 538-1876.

In California, (800) 672-1833.

Then, perhaps, celebrate your new sales figures with a French bubble product. Its computer code is shown above.

Dom Perignon, 1975.

Computer product codes. Each as unique as a fingerprint. Each representing a product and its cost. Designed to eliminate the time and expense of price tags and stickers, while providing critical up-to-the-second inventory updates.

In order to make efficient use of this system, a retailer must have fast and reliable access to thousands of codes, anytime. Unfortunately, a modular, computerized access has never been provided.

Until now, that is.

Nixdorf Computer has introduced an affordable system that is both easy to use and to install. A system that doesn’t discount quality, performance or reliability. A system made possible with a purchase from Intel.

Rather than counting on more RAM for keeping the data base, Nixdorf depends on an Intel 7110 bubble featuring a full
Disk SMD controller for Unibus

The MDB-RM11-Q (quad-size) emulates DEC's RM02/03/05, while the MDB-RK11-Q emulates RK06/07 disk drives. Each controller interfaces two physical disk drives (up to four logical units) to the PDP-11 Unibus. Either controller can simultaneously mix emulation modes within the same family. They are software transparent to all DEC operating systems plus Unix and TSX, and handle up to 56 Mbytes or 512 Mbytes per formatted device. Data capacity is 1.023 Gbytes with transfer rates to 10 Mbits/s. Prices range from $2800 to $3200. MDB Systems, Inc, 1995 N Batavia St, Orange, CA 92665. Circle 286

Drivers for LED display

The MS450 and MS451 drive 34 and 35 segments, respectively, with sink currents to 5 mA. They operate four- or five-digit alphanumeric displays with minimal interface to the display and data source. A serial data and clock signal transfer data. Both drivers feature continuous brightness control and TTL compatibility. No external resistors are required. The 40-pin plastic DIP costs $4.20 each in 100s. SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Circle 287

Mag-tape peripheral processor

Supporting the PDP-11 series of computers, model TC-200 is a single-board processor that takes one SPC slot in the backplane. It contains the necessary logic to control four 9-track tape drives. Speeds range from 25 to 125 in./s. Firmware provides an auto self-test verification routine on power up. The routine tests all internal registers, flags, and data paths. Read-after-write logic verifies data. The processor supports all DEC operating systems. Price is $3000 with delivery in 30 days. Computer Storage Technology, Inc, 1369 S State College Blvd, Anaheim, CA 92806. Circle 288

Floppy controller board

Proving the required governing, formatting, and interfacing logic between the VMEbus and disk drives, the DSSEFD/CONT-1 can handle four single- or double-sided 5 1/4- or 8-in. drives. The board occupies 24 Kbytes of memory, and base address is jumper selectable anywhere in the entire memory map. A hex display shows disk status and disk test results. The address bus and the control bus have TTL-compatible buffered inputs while the data bus has three-state, TTL-compatible buffered I/Os. Unit price is $1375. Data-Sud Systems/U.S., Inc, 2219 S 48th St, Tempe, AZ 85282. Circle 289

Serial I/O for Multibus systems

This board allows up to eight EIA RS-232E interfaces to connect to any Multibus system. With a 45-ns access time, the MP8158 is controlled by a USART containing an onchip baud rate generator. Therefore, each USART can be set at a different speed. Baud rate ranges from 50 to 19,200. It requires 32 I/O ports and its base address can be on any 32-port boundary. Standard I/O addressing uses a 16-bit DIP switch. Interrupt combinations can be set by strap selection. In one to nine quantities, price is $465. Burr-Brown, Data Acquisition and Control Systems Div, 3631 E 44th St, Tucson, AZ 85713. Circle 290

Disk controller slave

The Octafloppy is an IEEE 696/S-100 compatible slave card that provides up to 9.6 Mbytes of online storage via two strings of four drives. Each string can be either 5 1/4 or 8 in., single or double sided and single or double density simultaneously. It appears to the host as 16 1/0 ports with optional extended device addressing. Up to a 64-Kbyte transfer can be performed anywhere on the 16-Mbyte address space. An onboard wait state generator allows it to be used in 8-MHz systems. Single-quantity price is $495. Ackerman Digital Systems, Inc, 216 W Stone Ct, Villa Park, IL 60181. Circle 291

Winchester disk controller

Designed to maximize the I/O performance of multi-user, multitasking micro systems, the ACB-5500 board allows users to concurrently perform read or write operations on different disk drives. It supports seven host CPUs through a SASI/ANSI SCSI bus and four 5 1/4-in. Winchester drives of any capacity. The controller supports file sharing and shared disk applications through a reserve/release command. This command prevents access to a set of sectors that are being updated. Price is approximately $300. Adaptec, Inc, 580 Cotton Wood Dr, Milpitas, CA 95035. Circle 292

Signal memory recorder

The SMR-1 collects and analyzes transient waveforms. The modular unit provides each of 2 to 16 channels with 16 to 64 Kbytes of nonmultiplexed memory. Sampling is done at 1, 2, or 10 MHz with resolutions of 8, 10, or 12 bits. The 9-in. monitor displays in either Y-t or X-Y format. All functions and parameters are programmable by IEEE 488 or RS-232 interfaces or by front panel selection. A dual-time base allows pretrigger information to be sampled at one rate with other triggered data to be sampled at another. Soltec Corp, 11684 Pendleton St, Sun Valley, CA 91352. Circle 294
Memory and logic programmer

The 160 series universal programmer uses software (instead of hardware) that runs on a small computer. The complete system includes a programming station with two zero-insertion force sockets: one for devices of up to 28 pins, and one for 40-pin ICs. Software contains all the necessary programming algorithms and device data bases on floppy disks. Hardware includes an interface card that plugs into the computer, and a programming console containing power supplies and D-A converters that supply proper signals to the programming socket. Prices start at $4495. Valley Data Sciences Inc, 2426 Charleston Rd, Mountain View, CA 94043. Circle 295

Logic analysis system

The NPC-864ST combines a 48-channel state analyzer and a 16-channel 200-MHz timing analyzer into one package. It also includes a dual double-density floppy drive for test storage, automation, postprocessing, and performance monitoring using CP/M. Performance monitoring includes both time and event histograms with the time histogram used to display the percent of time the software takes to execute specific segments of code. Event histograms give the user frequency of occurrence information. Prices range to $19,500. Nicolet Paratronics, 201 Fourier Ave, Fremont, CA 94539. Circle 296

Portable floppy tester

Model PT-350 offers overlapping tests for data integrity and read-window margins. While a phase-locked loop generates a programmable data window, a programmable one-shot measures the relationship between read-data pulses and reference clocks. The tester has over 30 test routines and downloads to RAM for custom designed tests. It accommodates 8-in., 5½-in., and 3½-in. disk drives, FM or MFM encoded. Firmware holds 32 Kbytes of data integrity tests. In unit quantities, it is priced at $2995 complete. Applied Data Communications, Inc, 14272 Chambers Rd, Tustin, CA 92680. Circle 297

Test-generation system

Using a hierarchical approach that accepts functional and structural circuit descriptions, Hitest improves test program efficiency. The knowledge-based software uses a data base to automatically generate appropriate test programs. The package runs on VAX 32-bit virtual memory computers in combination with a color graphics test generation terminal. An interactive simulator provides accurate MOS simulation and logic strengths. Circuits designed on the HILO-2 simulator or on general-purpose computers (Apollo, VAX, Prime, or IBM) can be fed to the Hitest system. A typical system costs $200,000. GenRad, Inc, 170 Tracer Lane, Waltham, MA 02254. Circle 298

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

COMPUTER DESIGN/February 1984 263
Data-bus exerciser

Portable BUS-68000 exercises, tests, and troubleshoots MIL-STD-1553 systems. Local programming is via a front-panel, 24-pad keyboard and 10-character alphanumeric display. Remote programming is with an 8-bit parallel I/O port or optional IEEE 488 and RS-232 interfaces. Additional features include error generation and error detection, single or continuous messages, variable response time, and built-in self-test. The unit costs $4995 in quantities of one to nine. ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Circle 300

Scope calibration system

Calibrating scopes with bandwidths up to 1 GHz, the 400A makes fast controlled checks by a software/hardware combination. This consists of a Computest software package, IBM PC, color display, dual disk drives, and printer. Color options provide 16 foreground and 8 background choices. The system is priced at $28,500. Ballantine Laboratories, Inc, 90 Fanny Rd, Boonton, NJ 07005. Circle 302

Universal field tester

Through a DSA bus, the 2610 provides high speed data transfers essential to complex microprocessor-based devices. Available modules include diagnostic control, micro interface, measurement, and protocol floppy tests. Based on a Z80A micro, hardware consists of a 5-in. CRT, 256 Kbytes of memory, an 89-key tactile keyboard and a 3 1/2-in. disk drive. Prices start under $7000. GenRad, Inc, 300 Baker Ave, Concord, MA 01742. Circle 303

Winchester disk system

A 51-Mbyte universal mass storage system is compatible with Corvus host adapters available for IBM, TI, and Apple. The system uses run-length limited coding and a proprietary controller design for up to 60 percent more usable storage. In addition, transfer rates increase from 5 to 7.5 Mbits/s. Up to 64 users can share a single unit. A removable backup 1/2-in. tape cartridge with 32 Mbytes of online storage comes separately. The system costs $4595 and the backup is $1295. Sunol Systems, PO Box 1777, 1027 Serpentine Lane Pleasanton, CA 94566. Circle 305

Memory board with 64 Kbytes

The CMOS memory module has battery backup and a write protect feature. The DCM 64 accepts eight 8-Kbyte 6264s or 2-Kbyte 6116s, or eight 8-, 4-, or 2-Kbyte PROMs or EPROMs. The write protect functions to convert RAM into ROM. For example, during software development, a program can be written, executed, and debugged in RAM, then protected in ROM. An onboard NiCad rechargeable battery makes the module portable. In single piece, fully populated with eight 6264 RAMs, the board costs $850. Dynatek Inc, 22600-D Lambert St, El Toro, CA 92630. Circle 307
Universal floppy reader
Model TM-300 is a media translation system that accepts source computer data from floppy disks of any size, density, and format. It transfers data to an internal buffer memory where overhead formatting data is stripped away. Next, data is reformatted and written back out. In addition to disks, it unifies data formats for I/O ports and magnetic tape. A standard X-on/X-off feature enables the translator to accept realtime data communication input. IBM’s Bisync protocol is optional. The system costs $15,800. Applied Data Communications, Inc, 14272 Chambers Rd, Tustin, CA 92680. Circle 308

Magnetic tape systems
Designed for the Mostek/Prolog STD bus line of single-card computers, the systems are 1/2-in., 9-track and perform at 800/1600 bits/in. They use an intelligent micro-based controller that provides an 8-bit bidirectional parallel interface. Asynchronous handshaking and ping-pong buffering (2 Kbytes/dual) are standard features for maximum throughput. STD bus users are provided with data interchange and transportation via IBM/ANSI/ECMA and ISO-compatible tape and over 40 Mbytes of unformatted data storage for archival and/or disk backup. Prices range from $9575 to $11,950. Innovative Data Technology, 4060 Morena Blvd, San Diego, CA 92117. Circle 309

Dual-port static RAM
Organized as 1024 x 8, the SY2130 allows asynchronous reading and writing to a common-memory array. It features two separate 1/0 ports that give independent access to any location in memory. Two contention modes are available: in one, the contention is ignored and both operations proceed; in the other, onchip control logic arbitrates. An interrupt function controls and operates off a 5-V supply. In 100-piece quantities, the price is $42 for 48-pin ceramic DIPs. Synertek Inc, sub of Honeywell, 3001 Stender Way, Santa Clara, CA 95054. Circle 310

Infrared touch input system
Designed for the ISC 8000 series of 19-in. color graphics terminals, the touch system uses LED emitters and phototransistor detectors. They create a lattice of infrared light beams just in front of the display surface. When the screen is touched, light beams are broken and the computer responds to the reported X-Y coordinates of the touch. There is no overlay between the viewer and the screen, so screen brightness and resolution are unaffected. Carroll Touch Technology, 2902 Farber Dr, Champaign, IL 61821. Circle 311

Laser printing subsystem
Using laser technology and electrophotography, the 6100 prints forms, data, and text at speeds up to 103 pages/min. It allows the user to change font sizes and character densities within a single line. A large page buffer holds one or more pages of information, and allows incoming data to be printed continuously. Densities of 6, 8, 10, and 12 lines/in. and 10, 12, and 15 chars/in. are user options. Print resolution is made up of 240 x 240 dots/in. The printer is priced at $195,000. Storage Technology Corp, 2270 S 88th St, Louisville, CO 80028. Circle 312

Battery-operated matrix printer
The TTX 1280 portaprint uses rechargeable or replaceable 6-V batteries that provide 4000 to 5000 lines of print. In battery mode, the bidirectional printer features a 40-char/s print speed. With ac power, speed increases to 80 chars/s. A 5-x 7-matrix printhead produces a variety of character sizes and densities. The 3-lb unit allows bold or shadow printing, oversided printing, and condensed printing. Price is $199. Teletex Communication Corp, 3420 E Third Ave, Foster City, CA 94404. Circle 313

Mini magnetic card readers
Model 801 reads previously recorded data from cards that have magnetic stripes and meet current ATA, ABA, or Thrift specs. They can also read data from other cards with F/2F data properly placed on a magnetic track. The reader uses single- or dual-track read heads and a read only electronics package. They have no moving parts and can be mounted horizontally or vertically. Output is fully decoded into two lines representing serial data and clock using a proprietary LSI circuit. Vertel Div, Vertex Industries, Inc, 23 Carol St, PO Box 1123, Clifton, NJ 07014. Circle 314

Handwriting terminal
The Penpad consists of a writing tablet, control unit, pen, and display monitor. A menu-driven setup mode allows the setup of power-up terminal parameters. Once selected, parameters are stored in nonvolatile memory. Control unit handles serial asynchronous, TTY-compatible, ANSI X3.64 standard communications and offers line-buffered, page-buffered, character/coordinate, and graphics input modes. The system features dynamic character recognition that reads handwritten information. Pensect, Inc, 39 Green St, Waltham, MA 02154. Circle 315
The Only Way
You Can Get Q-BUS® Compatibility
And Interface Flexibility
With ANY or ALL These
5 1/4" Winchester Drives
is With
These Two Controllers

The ONLY WAY!

You can't get it with DEC. Or any other independent controller manufacturer. That's because these controllers feature DLOG's exclusive Universal Formatting™. That means you can mix or match any two compatible drives (ST506/412), regardless of heads, parameters, capacity, etc. This powerful feature offers you real flexibility in drive selection now...and expansion in the future. It's simple as unplugging one drive and plugging in another.

Model DQ615
• RK06/07 compatible
• Formatted drive capabilities 222.4 MB
• Maximum 8 logical units—two physical

Model DQ614
• RL01/02 compatible
• Formatted drive capacities 41.6 MB
• Maximum 4 logical units—two physical

They both have enhanced 32-bit ECC, 22-bit addressing and RT-11, RSX-11, RSTS and TSX-Plus.

DLOG Universal Formatting™ is also offered for the largest SMD I/O drives. And for your back up there are controllers for ½" tape, ¼" cassette and 5 1/4" and 8" floppy drives.

Contact your nearest sales office, distributor or DLOG directly for complete data on the way to unmatched Q-BUS compatibility and drive flexibility...THE ONLY WAY!
Low cost 68000 board
This 16-bit micro runs at 10 MHz and contains 17 internal 32-bit registers and a 24-bit program counter. Onboard memory consists of EPROMs and static RAMs, allowing the memory to run at full speed without wait states. Interfaces are a 24-line parallel and an RS-232-C. The system features a monitor in EPROM providing debug facilities, single step/trace, downline loader, and an EPROM programmer handler. A complete development system consisting of 280 host, cross assembler, 68000 CPU board, and EPROM programmer sells for about $1500.
Apollo Software, Bucklebury Alley, Cold Ash, Newbury, Berks, England. Circle 316

PC-compatible CPU board
Capable of supporting a no-disk, ROM-based system, the CP-88 features BIOS with MSDOS-compatible calling conventions. It can be combined with a memory board, video board, and floppy disk driver to operate as a hardware/software PC worklike. For applications requiring high speed complex math processing, an enhanced numeric processing extension is available. It can also serve as a remote control box at the end of a host computer in process control applications. Cost is $476. Electro Design Inc, 690 Rancheros Dr, San Marcos, CA 92069. Circle 317

Hybrid processor
An S-100 board with both Z80 and NS16032 chips, the 16KZ runs CP/M. Software tools permit individual Z80 subroutines to be replaced with NS16032 code using switch processor macro calls to transfer from one MPU to another. Hardware floating point and memory management units are options, operating at a 10-MHZ clock rate. The floating point unit implements high speed 64- and 32-bit floating point arithmetic, while the MMU implements program protection and debugging. Innervision Computers, 1632 Roll St, Santa Clara, CA 95050. Circle 318

Sixteen-bit microprocessor
The 6816 is completely hardware and software compatible with the 8-bit 6502. As a hybrid 8- and 16-bit CMOS processor, it accommodates the object code of its 8-bit predecessor as a subset. On power-up, it is in emulation mode, allowing for normal operation of existing 6502 monitor routines or operating systems. Software includes an operating system for the development of 6816 software. It is complementary to the underlying Prodos kernel, which handles all of the disk file management tasks. It will include a command processor, full-screen text editor, link editor, and several other utilities. Hayden Software Co, 600 Suffolk St, Lowell, MA 01853. Circle 319

All-CMOS board computer
While providing hardware and software compatibility with Intel's 8086/80/24, the CBC 80C/24 reduces power dissipation by 95 percent. The board comes in 3.58- and 2.5-MHz versions. Four 28-pin sockets allow 32 Kbytes of onboard RAM/EPROM. A lithium battery gives over 3 years of onboard memory backup. A total of 48 parallel I/O lines can be software configured as bidirectional or unidirectional. System software selects the data transfer format, control character format, parity, and communication baud rate. Pricing is $950 for the 8-Kbyte version. Diversified Technology, Inc, PO Box 748, Ridgeland, MS 39157. Circle 320

Floating point coprocessor
Designed for AIM's 8086 CPU board, a floating point device can replace the original CPU for increased computational capabilities. The upgraded board extends the CPU instruction set with arithmetic, logarithmic, transcendental, and trigonometric instructions. It implements the proposed IEEE floating point standard including all the single- and double-precision options. Applications are in robotics, graphics, numerical control, and process control. AIM Technology, 3333 Bowers Ave, Santa Clara, CA 95051.
Circle 321

Single-board computer for S-100
The SBC-300 is a high performance self-contained micro system designed around the Z80 micro family. It can perform as an IEEE 696 permanent bus master or as one of the slave processors on the bus to support multi-user applications. Features include 64 Kbytes of onboard dual-ported parity-checked memory, 1/O functions that include two full-duplex ports, and a SASI port with 8-bit bidirectional data buses. Two versions are available: the 4-MHz version is $741, while the 6-MHz version is $825. SDSsystems, Inc, PO Box 28810, Dallas, TX 75238. Circle 322

High speed central processor
Based on the NS16032 chip, the UB3050 processor features a Multibus interface. The CPU has full 32-bit internal arithmetic and a symmetric instruction set for high level languages. Board has an 8-Kbyte cache memory with an access time of 45 ns. The interface supports 16 Mbytes of memory with 25-bit addressing. Bus arbitration can be either serial or parallel. The memory management unit provides full virtual 24-bit address mapping into a 25-bit physical address space. A single board costs $3995.
Unidot, Inc, 602 Park Point Dr, Golden, CO 80401. Circle 323
System compatible with STD bus
The DT2712 provides 10 bits of resolution on 32 single-ended analog channels. It is powered directly from the 5-V supply on the STD bus. The input signals can be scanned at a throughput rate of 3300 samples/s. Compensation for timing differences is performed by an onboard jumper, making the board compatible with all STD bus processors. Jumper selectable for either I/O-mapped or memory-mapped addressing, it supports either software polled or vectored interrupt schemes. In 100s, price is $195. Data Translation, 100 Locke Dr, Marlboro, MA 01752. Circle 324

Not communicating?
The 232LT gets you talking.
Carroll's 232LT line tester/breakout box lets you examine the status of the RS-232 interface, simplifying troubleshooting and computer installation. Dual-color LEDs indicate the precise state—marking (-3V), spacing (+3V) or undefined (between -3V and +3V)—for the twelve most frequently-used lines. An extra LED is provided for monitoring additional lines.
Each signal line contains a DIP switch which can be opened to allow cross-patching. Pins located on either side of the DIP switches are useful as test points for meters and oscilloscopes.
The 232LT is signal-line powered, eliminating the annoyance of batteries, and it has the additional advantage of using a minimum signal current. Each LED provides a 3mA load at typical voltage levels of ±12V. (Stacking three LEDs in parallel can provide a 9mA approximation to the 10mA current limit of RS-232 drivers).
Accessories include jumpers, extension cable, user's manual, vinyl carrying case, and a handy RS-232/ASCII reference card. Guaranteed for one year. Priced at $175.00 (includes shipping); quantity discounts available. Distributor inquiries invited.
For immediate delivery or further information, call or write:
Carroll Touch Technology
a subsidiary of AMP Incorporated
2902 Farber Drive
Champaign, IL 61821
217/351-1700
TWX 910 245-0149

Converting rms to dc
With a guaranteed maximum nonlinearity of 0.02 percent, the AD637 operates from dc to 8 MHz. Fixed offset is ±0.5 mV and reading total unadjusted error is ±0.2 percent. The device computes the true rms value of complex ac waveforms. A crest factor compensation scheme holds additional measurement error to ±0.1 percent for crest factors of 3 and 10 percent duty cycles. The converter contains provisions for a decibel output and a denominator input. The output has a typical range of 60 dB with a ±1 dB typical error over a 7 mV to 7 V rms input. Pricing in 100s ranges from $15 to $23. Analog Devices, Inc, Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062. Circle 325

High capacity converter
On a single STD bus card, the DA-32 provides 32 channels of analog output. It uses only two I/O addresses and has a self-contained microprocessor. Specs include output range of 0 to 10 V, 8-bit resolution, 2-ns settling time, and 0.15 percent full-scale linearity accuracy, ±1/2 bit. Levels for each channel are set by writing a value for a channel to the odd port followed by the channel number for that value to the even port. Price is $455 in single quantities. rmac, 716 Capitola Ave, Capitola, CA 95010. Circle 326

High speed analog/digital system
The GMADIA-15B features 1-MHz conversion rates, 15-bit resolution, and multiplexing capability for 128 channels. The system is equipped with a sample and hold amplifier that provides a 1-ns aperture time. Maximum full-scale input voltage level is 10.24 V and the dc crosstalk between channels is less than ±0.005 percent of full scale. Specs include ±11 V, 70-dB common mode rejection, and 1.5-mV typical noise. Microcoded programmable interface has interchangeable logic adapters for compatibility with minis. Cost is approximately $10,000. Preston Scientific, 805 E Cerritos Ave, Anaheim, CA 92805. Circle 327

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.
KeyTronic's
SCREENED CONTACT™
Keyboard

This full-travel keyboard technology is the solution for any manufacturer who needs a keyboard without electronics.

- Rated at 50 million operations.
- Top-sealed.
- No silver traces or gold contacts.
- Does not utilize a printed circuit board.
- Low Profile (19 mm high at home row).
- Keys and key arrangement designed to your specifications.
- On-time delivery to your plant.
- Experienced personnel to service your account.

Key Tronic will respond to your manufacturing needs with our efficient people, quality products and in-house manufacturing capabilities. Call your Key Tronic representative today.
Development station for PC
The EZ-PRO II, with an in-circuit emulator and associated software, forms a complete development system. Each emulator has a cross-assembler, linking editor, and debugger that run on the PC. Emulators are transparent and run at full speed without wait states. Assemblers are written in C and are transportable to other processors. Sixteen-bit processor support includes the 68000, 8086, and Z8001/2. Basic cost is $3995, and emulators range in price from $1395 to $3395. American Automation, 14731 Franklin Ave, Tustin, CA 92680. Circle 328

Programmer board for VMEbus
Model DSEPROG-1 programs all JEDEC-approved EPROMs. Onboard firmware includes programming routines, monitor, and communication software. An intelligent peripheral controller's dual ported RAM handles VMEbus interrupts. The board can be located anywhere in memory and occupies 256 consecutive odd-numbered addresses. In addition, it has 48 Kbytes of MOS dynamic RAM. Jumper selectable rates range from 4.8 to 19.2 baud. Price is $1995. Data-Sud Systems/U.S. Inc, 2219 S 48th St, Tempe, AZ 85282. Circle 329

In-circuit emulators
Development support for 8085, Z80, and NSC800 works with Intel's iPDS. Software packages that run under ISIS-PDS or CP/M allow linking via the serial port on the iPDS to give the user emulation control from the console. In addition, the software transfers hex files between the host computer and the emulator. Devices provide realtime emulation, mappable memory, hardware breakpoints, and debugging facilities. Prices start at $1895 for the emulators and $100 for the software. Huntsville Microsystems, Inc, PO Box 12415, Huntsville, AL 35802. Circle 330

It pays to communicate
You can further your career by writing technical articles about the advanced work you're doing. Also, we pay an honorarium for all manuscripts that we publish. For a free copy of our Author's Guide, circle 502 on the Reader Inquiry Card.
Keep Your Eye on IMC...
for the Finest Quality
Electric Motors and Airmovers

Whether your order is large or small, custom or off the shelf, you can count on IMC for superior design, materials and craftsmanship as well as courteous service and quick delivery. For literature, please circle your reader service card or call our advertising department at 516/938-0800 for quick service or other information.
Graphics workstation

The Metamorph 15-in., 640- x 808-pixel monochrome display simulates an 8.5-in. x 11-in. sheet of paper. Hardware features include a 128-Kbyte display memory under the control of a 7220 graphics processor. The controller fills areas at 740 ns/pixel. Architecture is based on the 8888, which controls up to 256 Kbytes of programmable memory and up to 64 Kbytes of ROM. Supplied firmware allows emulation of DEC text and VT-125 graphics terminals, as well as Tektronix 401x graphics terminals. Unit price is $3495. *Companion Computer Corp*, 7404 Washington Ave S, Eden Prairie, MN 55344. Circle 331

Hardware/software package

The package allows PDP-11s and LSI-11s to run Intel micro development software. It consists of an 8000-compatible processor that plugs into the DEC system and software that emulates the ISIS operating system. Data transfers to an Intel computer by floppy disk or serial communication link. In most cases, the Intel software executes two to three times faster on a DEC system. CP/M is also supplied with the system. The package costs about $2000 for a single-user system and less than $5000 for a three-user system. *Decmation*, 3375 Scott Blvd, Santa Clara, CA 95051. Circle 332

Computational nodes

The DN460 and DN660 provide high end 32-bit supermini performance. They have an integrated hardware floating point processor to handle IEEE format single and double-precision numbers. With a 1-MIPS performance, the nodes include a three-stage, bit-slice pipelined processor with separate data and instruction caches; and a virtual address space expanded to 256 Mbytes per process. Available with color or monochrome displays, both nodes have low profile keyboards. A standard 12-Mbit/s LAN interface allows nodes to run on the same network. *Apollo Computer Inc*, 15 Elizabeth Dr, Chelmsford, MA 01824. Circle 333

Microprocessor development

Based on the IEEE 696/-s/100 standard, the Engineering Development Station (EDS) supports word/byte-wide ROM simulators and PROM/micro programmers. It features two double-sided, double-density 8-in. Shugart drives with a 2-Mbyte capacity; CP/M; 64 Kbytes of RAM; and two RS-232 ports. In addition, it has a 16-bit parallel port and a 4-MHz 280 with memory management. Up to 16 Mbytes of RAM can therefore be addressed. Each station has six card slots for easy placement of connections. Price in single units is $5995. *Inner Access Corp*, 517K Marine View, Belmont, CA 94002. Circle 334

Macrocell arrays

The HCA6348 has 4860 equivalent gates; the HCA6324 has 2295; the HCA6312 has 1200; and the HCA6306 has 648. The 3-micron silicon gate CMOS arrays constructed in two-layer metal technology yield loaded onchip gate delays of 2 ns. Input buffers operate at either TTL or CMOS voltage levels, while output buffers can drive 10 LS/TTL loads. Hardware macros implement 42 designs ranging from simple gates to shift registers. A variety of standard packaging options is available. Pricing is approximately $0.01 per gate for 10,000 pieces (plastic). *Motorola, Inc, MOS Integrated Circuits Group*, 3501 Ed Bluestein Blvd, Austin, TX 78721. Circle 335

Realtime graphics workstation

Either as a standalone workstation or as a terminal in a network, IRIS responds immediately to instructions without sacrificing functional range. The system is based on the geometry engine, which is a specialized floating point arithmetic chip. It performs all calculations for repositioning, shading, and other adjustments to 2-D and 3-D images. An array of either 10 or 12 engines handle rotation, translation, scaling, clipping, and perspective. Standalone workstation with disk is $60,000; $37,500 with terminal. *Silicon Graphics*, 630 Clyde St, Mountain View, CA 94043. Circle 336

Add-in package for Apple II

As an add-in board and software package, QPAK-68 turns the Apple II into a 68000 assembly language development system. The complete system includes a plug-in board to run 68000 programs, a combined editor/assembler for source code, and a debugger for testing. The board uses a 68000 that is driven from the 7.16-MHz clock so it can run in parallel with the 6502. It shares the Apple's 64-Kbyte memory space and can access the same memory and peripherals as the 6502. Local memory is 8 Kbytes of EPROM and 2 Kbytes of RAM, expandable to 32 Kbytes and 8 Kbytes, respectively. Price is $695. *Qwerty Inc*, 9252 Chesapeake Dr, San Diego, CA 92123. Circle 337

Hierarchical CAE design package

Designed for use on the IBM XT, the structured interactive design system (STRIDES) eliminates redundant drawing of common elements. The editing system allows a change in one document to be automatically incorporated into the overall design including update of pin, net, and material lists. It manages an entire document tree from the top block diagram to individual components that include VLSI equivalents at the gate array or chip level. Price is $1900. *FutureNet Corp*, 21018 Osborne St, Canoga Park, CA 91304. Circle 338

Software application modules

Designed for the Expert engineering workstation, software modules configure for electronic and electromechanical engineering, PC board design, or mechanical drafting. Types of modules include schematic design, logic simulation, and timing analysis. The simulation module is a true interactive logic simulator that enables verification of designs created with logic design software. It supports a large array of primitives—transistors and gates to RAMS, ROMS, and programmed logic arrays. Module prices range from $3900 to $10,000. *Versatec, a Xerox Co*, 2710 Walsh Ave, Santa Clara, CA 95051. Circle 339
Tools for graphics support
Designed for the IBM 5080 graphics system, the DI-3000's capabilities include 2-D and 3-D dynamic image transformation, complex polygon fill with colors or patterns, and complete color table access. Written in ANSI Fortran, the integrated system contains 200 user-callable subroutines. It supports a broad range of terminals and hardcopy devices, and allows existing applications to be transported with little or no modification. Prices for the 25-year license including driver will start at $12,000. Precision Visuals, 6260 Lookout Rd, Boulder, CO 80301. Circle 340

Expansion board for PC
The Time Spectrum SB384 facilitates memory expansion to 640 Kbytes and offers communication functions in a single chassis slot. Standard features include socketed RAM, calendar/clock with rechargeable battery backup, one asynchronous communication port, and a Centronics or data products compatible parallel printer port. Memory features are parity checking and error reporting, switch-selectable addressing on any 64-Kbyte boundary, and complete IBM hardware/software capability. Cost is $395. Persyst Products, Personal Systems Technology, Inc, 15801 Rockfield Blvd, Irvine, CA 92714. Circle 341

Single-board evaluation module
When connected to a terminal or host computer, a module evaluates virtual memory performance in Multibus-based 16-bit SAM-Z8003EVM. Resident monitor program and control unit control, inspect, and alter onboard and offboard resources, including memory, I/O ports, VMPU and PMMU registers, and breakpoint set and clear. The evaluation module, including board, control unit, monitor program, and two RS-232 connectors for terminal and host computer connections, is $2500. SGS Semiconduc­tor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Circle 342

Communication/cluster control
An expandable family of emulation subsystems, the PS-3270/BSC plugs into the IBM PC, PC/XT, and compatibles. It uses a Z808-based intelligent frontend processor with its own multitasking executive. The following systems can be emulated: single-station IBM 3276-2 control unit display with attached printer, small cluster system with printer and three downline display stations, or a large cluster system with printer and 13 display stations. Prices start at $1295. ABM Computer Systems, 23362 Peralta Dr, Laguana Hills, CA 92653. Circle 343

Cubit's new I/O Processor controls a CRT, printer and keyboard.
Using an 8085 microprocessor with its own memory, the board frees your system CPU to race ahead of slower peripherals. Terminal-like commands permit easy communication between this smart controller and the host-processor.

Bring distributed processing to your STD Bus system for $345 in single quantity. With stock to two week delivery, you won't have to wait long.

Cubit INC.
Division of Proteus Industries
190 South Whisman Road, Mountain View, CA 94041
Telephone: (415) 962-8237

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.
Video encoder circuit

The MC1377P combines RGB video information into a composite video signal using either NTSC or PAL formats. The chip contains a subcarrier oscillator, voltage-controlled phase shifter, two double-side band modulators, and RGB input matrices. The oscillator can be used as the master in a system or be driven externally. Inputs are ac coupled and a 1-V peak-to-peak input level produces full color saturation in the output. Price (in 100 to 999 quantities) is $2.35. Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036.

Circle 344

Parallel CMOS multiplier

Featuring 100 percent screening to MIL-STD-883 Class C, the IDT7216/7217 is manufactured with proprietary CEMOS I technology. The multiplier has a 90-ns clocked multiply over military temperature ranges with maximum power consumption at 440 mW. The chip is available in 68-pin surface-mounted LCCs and 64-pin flatpacks. Applications include graphics display systems, speech synthesis/recognition, and digital filtering. In 100-unit lots, prices begin at $120 each for the 145-ns commercial grade version. Integrated Device Technology, Inc, 3236 Scott Blvd, Santa Clara, CA 95051.

Circle 345

Monolithic quad D-A converter

The AD7226 combines four latches, four 8-bit D-A converters, and four output buffer amps on a single chip. Fully microprocessor compatible, the converter transfers data into one of four data latches through a common TTL-CMOS input port. Control logic signals permit the user to address each chip separately. Single-supply operation is from 11.4 to 16.5 V, and an additional — 5-V supply for dual operation provides higher accuracy. Housed in a 20-pin DIP, the converter comes in three packages for three operating temperatures. Cost is under $20 in 100s. Analog Devices, Inc, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.

Circle 346

Programmable interval timer

The CMOS 82C54 is a TTL compatible pin for pin replacement for the NMOS 8254. It consists of three independent, separately programmable 16-bit timers. Maximum timer count frequency is 8 MHz; a 5-MHZ 80C86/8086 system operates with no wait states. Standby power dissipation is 55 µW with a 10-mA operating current. Dual output voltage specification guarantees reliable operation in both NMOS and CMOS systems. The 24-pin chip comes in cerDIP and plastic. In quantities of 100, prices range from $15.40 to $79.73. Harris Corp, Semiconductor Sector, PO Box 883, Melbourne, FL 32901.

Circle 347

Resettable static RAM

Organized 1024 x 4 bits, the Am9150 uses a reset feature that clears the entire memory array in two cycle times. The architecture is suited for cache memory applications in mainframes, minis, and engineering workstations. Additional applications include address translation, memory mapping, and high speed buffer memory. Reset/clear feature allows use in video imaging and laser printing. The 25-ns device is packaged in 24-pin ceramic and is priced at $25 in 100s. Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086.

Circle 348

Metal-gate CMOS gate array

The TM3600 features a 13-ns/5-V gate delay, 3- to 5-V power supply, TTL or CMOS compatibility, and maximum clock frequency of 5 MHz at 5 V. After preparation of the proprietary mask, the wafer is processed, tested, and made available as dice or packaged parts. It has 69 bonding pads; package choices include LCC, flatpack, ceramic, cerDIP, and DIP. The cells perform logic functions such as gates, flipflops, counters, current/voltage source, and op amps. The 10,000-piece price ranges from $5 to $10. Telmos Inc, 740 Kifer Rd, Sunnyvale, CA 94086.

Circle 349
Register-file EEPROM
Integral address latch and input data latch eliminate the need for a 2048-bit EEPROM to hold address and data valid during the erase/write operation. Any byte can be written or erased without affecting the rest of the memory, or the entire memory can be erased in one cycle. The SY202E endures 1 x 10^4 write cycles and retains data for 10 years. Organized as 256 words x 8 bits, the chip comes in 18-lead cerDIP and plastic packages. Prices are $4.50 in 1000s. Syntek Inc, 3001 Stender Way, Santa Clara, CA 95054. Circle 350

Bell-compatible modem chip
The XR2123 is a CMOS IC that provides phase-shift keyed modulation and demodulation. It performs either 1200 bits/s (needed for Bell 212A compatibility) in full-duplex, or 2400 bits/s in half-duplex mode. Power consumption is 10 mW and the chip requires only a 5-Vdc supply. Modem is packaged in a standard 28-pin DIP. Price is $23 in 1000s. Exar Integrated Systems, Inc, 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088. Circle 351

Microcontroller in CMOS
The COP424C/COP425C has 1 Kbyte of ROM, while the COP444C/COP44SC contains 2 Kbytes of ROM. In addition to the CMOS instruction set, the controllers offer 50-µW power dissipation and instruction cycle times from dc to 4 µs. Based on microCMOS double-polysilicon gate technology, the chips are micors with all system timing, internal logic, ROM, RAM, and I/O. Users have up to 27 mask-programmable output options that can be programmed at the same time as the ROM pattern. Prices begin at $2.60 each in 100,000-piece quantities. National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Circle 352

Low noise op amps
The LT1007 and LT1037 offer 2.5 nV/√Hz wideband noise, 1/f corner frequency of 2 Hz, and 60 nV peak-to-peak, 0.1 to 10-Hz noise. Open-loop voltage gain is 20 million driving a 2000-Ω load. With a 600-Ω load, the amps achieve 12 million open voltage gain. The 1007 is internally frequency compensated for unity gain and guarantees 1.7 V/µs minimum slew rate. The 1037 is stable in closed-loop gains of five or more, and slows at a minimum of 11 V/µs. In 1000s, prices start at $4. Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Circle 353

Gate arrays with higher density
The Q1500A offers 84 I/Os; the QH1500A offers 120. Both arrays have 1500 gate densities and can be used in TTL, ECL, or mixed systems. Typical gate delays are 0.9 ns with flipflop toggle rates of 250 MHz. A 95-percent utilization is achieved with automatic layout. A high I/O-to-gate ratio relieves system partitioning problems, and a mixed TTL/ECL structure reduces system part count by eliminating transistors. Both arrays operate over the full military temperature range. Applied Micro Circuits Corp, 5502 Oberlin Dr, San Diego, CA 92121. Circle 354

Multiplying D-A converter
The 12-bit MP7623 features both integral and differential linearity at 0.2 ppm/°C maximum and monotonicity guaranteed over the entire temperature range. Settling time is less than 1 µs for a 20-V step to 0.01 percent. Specific applications include digital/synchro conversion, programmable amps, and automatic test equipment. Improved design makes the device latchup free, so no output protection diodes are needed. Also, a MSB technique reduces system feedthrough error and noise. The 100-piece price ranges from $12.45 to $40.65. Micro Power Systems, Inc, 3100 Alfred St, Santa Clara, CA 95050. Circle 355

Get your own
If you're reading someone else's copy of Computer Design, why not get your own? To receive a subscription-application form, circle 504 on the Reader Inquiry Card.

Software

Generic concurrent CP/M
The software can be configured for single- and multi-user systems and is compatible with PC-DOS. It supports networking via DR soft/net, and it features shared code support. This allows sharing of separately written code segments for lower memory requirements and reduced program loading time. It also supports Intel's 8087 math coprocessor chip. Based on a high performance file system, it includes multi-sectored I/O, record buffering, and directory hashing tables. Digital Research Inc, 160 Central Ave, Pacific Grove, CA 93950. Circle 356

Communication software
Applications for SNA, network management, and x.25 communication are available on the Tower 1622 under Unix and on the 9300 under ITX. Programs assume the SNA profile of several IBM devices, while development tools perform active logic traces and breakpoints. An SNA/JRE application, 3270 data stream compatibility, and x.25 packet level interface are available. NCR Corp, 11010 Torreyana Rd, San Diego, CA 92121. Circle 357

Realtime option for RT-11 systems
Share-eleven supports more than 10,000 interrupts/s. It provides kernel debugging facilities and a graphic system performance monitor for multi-user RT-11 systems. A full set of system calls and utilities eases realtime programming. Documentation is included. The Share-eleven realtime option costs $1500, while the basic Share-eleven is $1000. Contel Information Systems, Inc, Software and Systems Div, 4330 East-West Hwy, Bethesda, MD 20814. Circle 358

Network development
High level Bridge software customizes Ethernet communication servers. The software includes C compiler, a 68000 assembler, link editor, S-hex record for matter and downloader, and documentation. It supplies the tools needed to compile and assemble C source code. Available on nine-track tape (1600 bits/in.), it is in Unix tar format for customization. Price is $250. Bridge Communications, Inc, 10440 Bubb Rd, Cupertino, CA 95014. Circle 359
Virtual memory operating system
A release of iMAX 432 is aimed at designs for fault tolerant computer systems, Ada-based workstations, and 32-bit computer systems. The system performs deallocation and afterwards combines variously sized blocks into large contiguous blocks for new storage. The architecture supports a segmented memory management approach where segments can vary in size from 1 byte to 64 Kbytes. Software can be written in modular form to reduce development time and software maintenance. Price is determined by quantity, with the first copy at $8000, and each copy beyond 150 priced at $500. Intel Corp., 3065 Bowers Ave, Santa Clara, CA 95051. Circle 360

Application processor
Fourth-generation Pro-IV develops, modifies, and operates applications. The multiterminal multidata file development/runtime system processes Cobol, Basic, and Fortran files. Features include menu driven application development, common data dictionary, interactive screen and report definition, windowing, and auto-generated documentation. Development license is $20,000. Pro-IV, Inc., 119 Russell St, PO Box 595, Littleton, MA 01460. Circle 361

Management information software
Themis understands English questions and commands. It will retrieve information requested via keyboard for output on a screen or printer. Users can also ask for functions such as sorting, logical comparisons, and calculations. The initial version runs on the VAX-11. It uses 1.5 to 2 Mbytes of main memory and requires either Datatrieve or Oracle relational DBMS. Basic vocabulary of more than 900 English words can be easily expanded. Translation from English into database query adds 0.4 s to CPU time. Price is $24,500. Frey Assocs., Inc., Chestnut Hill Rd, Amherst, NH 03031. Circle 362

Operating software extension
Microsoft Windows upgrades MS-DOS to provide a universal operating environment for bit-mapped application programs. It allows independent software vendors to develop graphically based, integrated software packages that run without modification on any 16-bit micro. A window management feature allows users to view unrelated application programs simultaneously, and to transfer data from one program to another. Hardware requirements are 192 Kbytes of RAM, a mouse, two floppy drives, and a bit-mapped display. Microsoft Corp., 10700 Northup Way, Bellevue, WA 98004. Circle 363

Tell us what you like
Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.
Logic Analysis Enters a New Era

Combine innovative and comprehensive analysis power with easy and efficient operation and the new era begins.

Understandable. Exploit the power of more than 250 functions the very first time you switch on the PM 3551. All functions are clearly labeled above the softkeys, so it's easy to set up in seconds—even without the manual!

Expandable. Start with a 35-channel model to handle 8- and 16-bit multiplexed processors. Then expand to 59 channels to handle minis and 16-bit non-multiplexed processors. Other performance options include a 300MHz timing card, interfaces (RS232 and IEEE 488) plus disassemblers.

Triggering that thinks. Easily specify complex sequences with the IF, THEN, ELSE structured language. Use the “trigger on sequence break” to test polling routines.

Deep memory. Capture blocks of data that are followed, or separated, by a specific sequence of events. Stretch pre-trigger memory depth virtually to infinity.

Megaword timing. Using our transitional timing, capture and display two 20ns pulses occurring up to 5 seconds apart, with 20ns resolution. This means no more trading off resolution against memory. And it opens up new applications such as disk drives.

Processor support. Take advantage of manufacture oriented disassembly packages that give you full family support for the same price as competitors' single processor package.

The PM 3551 is configured to match not only your current but also your future requirements.


CIRCLE 135
Chassis for Q-bus
The 8700 series of logic enclosures is designed for users needing expanded capacity for existing LSI 11/23 systems. The 8705 chassis features a side-loading Q-bus backplane with 27 dual-wide slots. It also has a 300-W power supply, ac input connector with line filter and switch, cooling fans, and DEC-compatible power sequencing. Cost is $1600. The 8703 provides 18- or 22-bit memory address, while retaining the use of 18-bit Q-bus peripheral controllers. Cost is $5300.

Monolithic Systems Corp, 84 Inverness Circle East, Englewood, CO 80112. Circle 364

GOING BROADBAND?
You’re going OUR way!

Broadband versatility can be achieved in less time than you think. We have bus oriented (integrated) modems to solve specific broadband problems. We design custom products that solve one-of-a-kind problems.

Coherent Systems products are currently in use solving complex communications problems in high energy physics research, in local and wide area networking and in factory automation.

Put our experience to work for you!

Call us at 817-267-4167. Or write:

COHERENT SYSTEMS, INC.
3301 Airport Freeway, Suite 122 • Bedford, Texas 76021

Leadless chip carrier family
Three different designs mount VLSI chips on a minimum of board space without sacrificing easy assembly, inspection, economy, or reliability. The CPSS connector series includes a 160-pin socket with a hinged cover to hold a LCC securely. A second socket is JEDC type A 68-pin with a twist-on cover that can accept a heat sink. A LCC pin frame 68 consists of a glass reinforced thermal plastic frame with embedded connecting pins. Prices for the connectors run from $2 to $8 each in quantity. ITT, Cannon Electric Div, 10550 Talbert Ave, PO Box 8040, Fountain Valley, CA 92708.

Circle 365

Ribbon cables
The PTFE insulated series is compatible with insulation displacement connector systems approved under MIL-C-83503. The 0.050-in. pitch cables support widths up to 64 connectors, in AWG sizes of 24, 26, and 28. They provide a low dielectric constant, low crosstalk characteristics, fast signal speed, and a low dissipation factor. Nickel-plated version functions in extreme temperatures ranging from -65 to 260°C; silver-plated option provides solderability. W L Gore & Assocs, Inc, Electronic Products Div, 1505 N Fourth St, PO Box 1389, Flagstaff, AZ 86002.

Circle 366

Family of Ethernet cables
The 9880 is a trunk/coaxial cable with tinned copper conductor and cellular polyethylene. It has a four-layer shield. Standard put-ups are 500 ft, 1000 ft, and 1640 ft, with 1000-ft price of $933. The 9880 is a plenum non-conduit trunk/coaxial cable. Also with a four-layer shield, the cable has a bare copper conductor and a cellular FEP Teflon dielectric. Standard put-ups are 100 ft, 500 ft, 1000 ft, and 1640 ft priced at $4350. Belden, 2000 S Batavia Ave, Geneva, IL 60134.

Circle 367

Like to write?
The editors invite you to write technical articles for Computer Design. For a free copy of our Author’s Guide, circle 503 on the Reader Inquiry Card.
UNIX® IS A DINOSAUR
CP/M® & MS·DOS™ ARE TOYS
MULTI SOLUTIONS PRESENTS
THE WORLD'S FIRST
4th GENERATION
OPERATING SYSTEM

A SERIOUS
OPERATING
SYSTEM
S1
FOR TODAY
AND
TOMORROW

• PORTABLE
• MODULAR
• MULTIUSER
• MULTITASKING
• MULTI PROCESSING
• PARALLEL PROCESSING
• 64 CHARACTER NAMES
• 3 COMMAND PROCESSORS
• REAL TIME
• NETWORKING
• DISTRIBUTED PROCESSING
• HIERARCHICAL DIRECTORIES
• KEYED FILES
• ISAM
• VSAM
• B-tree
• RECORD LOCKING
• UNIX SOURCE COMPATIBLE
• WINDOWING
• BIT MAPPED DISPLAYS
• FULL SCREEN MANAGEMENT
• FULL SCREEN EDITING
• FULL MEMORY MANAGEMENT
• VIRTUAL MEMORY
• SEMAPHORES & LOCKS
• EXTENSIVE UTILITIES
• AND MUCH, MUCH MORE

S1 IS THE ONLY OPERATING SYSTEM WORTHY OF THE TITLE:
"THE NEXT WORLD STANDARD."

ONLY S1 DOES IT ALL.
NO OTHER OPERATING SYSTEM COMES CLOSE. CUTS DEVELOPMENT TIME FROM MAN YEARS TO MAN MONTHS.

Please send for our FREE S1 Book or Call 609-695-1337

IN TIME, ONLY THE BEST WILL SURVIVE: S1

*Reg. Trademarks: CP/M of Digital Research; Unix of Bell Laboratories Trademarks: MS-DOS of Microsoft, Inc.

See us at Comdex-Winter '84 Booth-363
CIRCLE 171
See us at SOFTCON-Booth L7223
Full-function small computer

The PC Traveler has a gas plasma display, with a full 80 x 25 format. The 9 3/4-in. screen offers complete graphics capability. It uses dual 16-bit 80186 CPUs for fast processing. The full-function 80-chars/s printer supports multiple print fonts, character sets, and dot-addressable graphics. It prints at 80 or 132 chars/line on letterhead or fanfold paper. Other features include a 6.2-Mbyte cartridge disk drive and a custom keyboard with key-initiated, ROM-based diagnostics. Cost is $4495. Strategic Technologies, Inc, 7001 Peachtree Industrial Blvd, Norcross, GA 30071.

SYSTEMS PROJECT LEADER

A broad technical background in addition to 5 years experience in the design of software systems for real-time applications is required. You will direct the activities of other project staff, maintain project schedules and budgets and work with other departments, customers and vendors to identify and solve problems in order to meet project objectives.

MICROCOMPUTER WITH UNIX

Based on the 68000, the 83/80 combines high throughput and a full Unix operating system. It conforms to IEEE 696/5-100 bus standards with a 10-MHz clock rate and memory management. A SMD disk controller yields 800-kbyte/s average transfer rate in read mode and 560 kbytes/s in write mode. The controller supports one or two 80-Mbyte hard disks. Standard 512 Kbytes of RAM expands to 3.25 Mbytes. Four-channel serial RS-232-C I/O boards use DMA for all outputs. Cost is $20,990 with Unix. Dual Systems Corp, 2530 San Pablo Ave, Berkeley, CA 94702.

Circle 370

SINGLE-BOARD COMPUTER

The Super 186 is a 16-bit, s-1oodevice built around the 80186. The 8-MHz computer configures as a standalone bus master or bus slave to serve single or multiple users. It features 256 Kbytes of memory expandable to 1 Mbyte, and a floppy drive controller that supports both 8- and 5 1/4-in. disks simultaneously. The computer also has four serial RS-232 and two parallel I/O ports, DMA controller, parity, and monitor EPROM to aid in initial loading. Price is $1650. Advanced Digital Corp, 5432 Production Dr, Huntington Beach, CA 92649.

Circle 371
Talent... determined... proud. The people behind Hughes Radar Systems Group are leading the challenge to new technical horizons. In an environment that stimulates and actively supports a diversity of technical contributions. Scientific resourcefulness... coupled with creative engineering. These people have made it an art.

At Radar Systems Group, Hughes people forge new frontiers in aerospace radars, weapon control systems and avionics, airborne displays, aero-vehicle data links and airborne electronic countermeasures equipment. Scientific explorations that extend radar technology's vision far beyond today's horizons.

At Hughes, there is a stimulating relationship between the people and their work. Between the individual and the team... the team and the group... the group and the company. A relationship that provides opportunity for substantial individual contribution. That's what Hughes Radar Systems Group is all about. People. People with vision and dedication. People participating in extraordinary ways. People like you.

People experienced in design, development, and manufacturing. Applying your talent to systems engineering, project/program management, design of circuits and mechanisms, and bringing these concepts to reality through the application of advanced manufacturing processes.

You are invited to call (213) 647-4900, collect, or send your resume to:
Hughes Radar Systems, Engineering Employment, P.O. Box 92426, Dept. DC-2, Los Angeles, CA 90009.

Creating a new world with electronics

Keyboard plug-compatible with PC
Besides familiar key placement, the low profile Inductive unit features micro-based electronics and solid state inductive switches. It comes with sync/async RS-232 format and TTL level ASCII serial output. Depressing a key moves a ferrite core into the field of a balanced differential transformer etched on the PC board. As inductive coupling changes, the transformer becomes unbalanced so a signal is received by the pulse circuitry. The model 88KT-15 is priced at $250 (1 to 9 pieces). Elco Corp, Keytek Div, 6424 Warren Drive, Norcross, GA 30093. Circle 372

Positive answers in real-time data acquisition and control

NEW RTP
HIGH SPEED SERIAL LINK
50 TIMES FASTER
DATA TRANSFER PLUS
REMOTE CAPABILITY

- Multiple Port High-Speed Serial Card
- Intelligent Remote Control Unit
- High-Speed Optical Modem
- Data Security
- Positive Data Transfer Response

Now your computer can communicate serially with RTP data acquisition and control equipment at one megabaud data rates. The RTP High Speed Serial Link provides an interface to our complete RTP Universal line. Data can be transferred in single words or in blocks, using RS-422 signal levels or fiber-optic cable. With the latter, your computer and the process can be as far as 6552feet (2000 meters) apart.

The integral Intelligent Remote Control Unit supports both digital and analog inputs and outputs, plus sequence of event time tagging and open transducer testing.

The High-Speed Serial Link is currently available for the Motorola 68000 I/O channel. Other interfaces will be available soon. Call or write for full details. (305) 974-5500, 4800 NW 70th St., Ft. Lauderdale, FL 33309.

BE RTPositive

Time-delay relays
The plug-in CB series features a CMOS IC to precisely control timing functions. Shortest timing range is from 0.1 to 1 s, while the longest is from 10 to 100 min. Relays have delay on operate, delay on release, and interval on timing modes. Depending on timing function and termination, spdt or dpdt contacts are available. Contacts are rated 10 A at 240 Vac. All models have octal-style plug termination. Cost ranges from $22.50 to $26.25 each in 100-piece quantities. Potter & Brumfield Div, AMF Inc, 200 Richland Creek Dr, Princeton, IN 47671.

Circle 373

Thin-film resistor and network
The devices offer an integration density of 600 kΩ/mm² with 0.001 percent and up to 0.0005 percent precision. Temperature coefficient is less than ±5 ppm / °C. Stability specs include less than 500 ppm drift after 1000 h at 155 °C, tracking characteristic is better than 1 ppm / °C, and relative stability between two resistors under stress is less than 200 ppm. Applications are in miniature networks such as A-D and D-A conversion circuits. Networks can be packaged bare or in chip carriers. Sfernice International, 117, bd de la Madeleine, BP 17-06021, Nice, Cedex, France.

Circle 374

Antiglare VDT filter
The CP-50 contrast enhancement filter uses a circular polarizer to reduce the effects of glare and to improve screen contrast. The polarizer absorbs ambient light falling on the screen rather than allowing it to bounce back to the user’s eyes. Filter attaches to the screen with self-adhesive mounts; no tool or assistance is needed to install or remove them. They are easy to clean with a filter-cleaning fluid. Cost is $49.95. Polaroid Corp, 575 Technology Square, Cambridge, MA 02139.

Circle 375
Matrix printer mechanism

The heavy duty 15-PM C accepts 3- to 16-in. wide perforated paper and prints at 275 chars/s, 10 pitch, and from one to six part forms. It uses a nine needle free flight head, rated for 1350 Hz at 0.025 stroke for over 300 million characters. The ribbon cassette is stationary and driven directly from the carriage motor. The dc motor uses an encoder with photocells in quadrature for motion control. Head moves bidirectionally. Price is $243, quantity 1000. Practical Automation, Trap Falls Rd, PO Box 313, Shelton, CT 06484. Circle 376

Hermetic infrared emitting diode

The OP231 series are GaAlAs devices available in hermetic TO-46 housings. Emitting wavelength centers at 875 nm to match the spectral response of silicon phototransistors. Improved coupling efficiency allows lower drive currents and improves reliability. Higher noise immunity means lower output signal amplification. Applications include signal/data transmission in scientific, military, and industrial markets. Optoelectronic Div, TRW Electronic Components Group, 1270 Tappan Circle, Carrollton, TX 75006.

Dual-redundant RTU

The BUS-45401 provides a complete intelligent interface between a serial MUX data bus and a three-state data highway. The unit’s interface appears to the subsystem as a 256-word memory mapped I/O. All RTU protocol, memory management, and built-in tests are performed without subsystem intervention. The device consists of a set of standard hybrid products including a dual transceiver, two encoder/decoders, RTU protocol hybrid, and dual-port memory. In addition, the card contains two transformers, a crystal oscillator, and three ROMs. Prices start at $3695. ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

High efficiency green LEDs

Lamps are two to three times brighter than standard green, and as bright or brighter than high efficiency red and yellow. Sizes are T-1, T-1 3/4, and T-3/4, with clear and diffused lenses and eight viewing angles from 24 to 180 degrees. They are also available in rectangular lamps. Price in quantities of 1000 is $0.23 to $0.48, depending on lamp type and intensity rating. General Instrument, Optoelectronics Div, 3400 Hillview Ave, Palo Alto, CA 94303. Circle 379

Choke on DIP footprint

The Multiple Choke provides simultaneous protection of eight data lines. It is used on computers, terminals, and other equipment that requires interfacing cables. Each winding gives inductance of 150 µH (reference 1 kHz and ±25 percent). Isolation is 1000 Vac between windings. The device mounts on a standard 16-pin DIP spacing with 0.042-in. diameter pins and a maximum height above the PC board of 0.430 in. Cramer Coil & Transformer Co, Inc, 1121 15th Ave, Grafton, WI 53024. Circle 380
WHY YOU SHOULD MAKE A CORPORATE CONTRIBUTION TO THE AD COUNCIL

The Advertising Council is the biggest advertiser in the world. Last year, with the cooperation of all media, the Council placed almost six hundred million dollars of public service advertising. Yet its total operating expense budget was only $1,147,000 which makes its advertising programs one of America's greatest bargains...for every $1 cash outlay the Council is generating over $600 of advertising.

U.S. business and associated groups contributed the dollars the Ad Council needs to create and manage this remarkable program. Advertisers, advertising agencies, and the media contributed the space and time.

Your company can play a role. If you believe in supporting public service efforts to help meet the challenges which face our nation today, then your company can do as many hundreds of others—large and small—have done. You can make a tax-deductible contribution to the Advertising Council.

At the very least you can, quite easily, find out more about how the Council works and what it does. Simply write to:


Ergonomic design keyboard

As standard equipment with the 8510 graphics computer system, the 8535 includes height and angle adjustment and a coiled connection cable. It provides a 128-character ASCII set and function keys for cursor control, space, carriage return, escape, and delete functions. The numeric keypad is active only in shift mode, otherwise it generates character and control codes for use as function keys. LSI n-channel MOS electronics perform keyboard encoding with n-key rollover. Terak Corp., 14151 N 76th St, Scottsdale, AZ 85260.

Circle 381

Brushless pancake motor

The 12-Vdc device is designed for direct drive of microfloppy disks. Its brushless design and use of ball bearings give it service life in excess of 10,000 hours. Rated load is 50 g-cm, rated current is less than 230 mA. Speed regulation is ±1.5 percent of 300 rpm over a torque range from 0 to 72 g-cm. Rise time to rated speed is 300 ms maximum. Starting torque is 150 g-cm minimum, and starting current is 700 mA maximum. Canon USA, Inc, Electronic Components Div, One Canon Plaza, Lake Success, NY 11042.

Circle 382

Silicon transistor

The BFQ 77 has a line width of only 0.8 µm and an operating range up to 6 GHz. Rated noise is 2.8 dB at 4 GHz (8-dB associated gain). The Circerec package is suitable for mounting on all types of PC boards. High service reliability is realized through multilayer metallization, ion implantation, self-aligning lithography, and additional double passivation. Microwave Semiconductor Corp., 100 School House Rd, Somerset, NJ 08873.

Circle 385

Switchable DIP attenuator

Balanced T type 7010 series has 50-, 75-, and 600-Ω impedance values. The eight-pole device configures in a standard 16-pin DIP. It uses a precision laser trimmed thick film resistor network, mating to a gold contact switch system. Custom design or standard attenuation increments of 0.1 to 1.5 dB are available. The 7010 comes unsealed, or sealed with a plastic adhesive that washes off. Prices range from $3 to $5. Vernitron Corp, VRN Div, PO Box 44000, St. Petersburg, FL 33743.

Circle 384

Video amplifier

The 3-bit digital device has 100-MHz bandwidth and 3.5-ns rise and fall time. It accepts either 3 bits of TTL or ECL (differential) digital information and directly converts the data into eight gray scales on the CRT. The amp is virtually glitch-free and eliminates the need for a D-A converter at the controller. Bit-mapped controllers can drive 3-bit planes directly into the CRT monitor. U.S. Pixel Corp, 59 Fountain St, Framingham, MA 01701.

Circle 386

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.
Does the 60-Hz monitor you're considering meet these design parameters?

| A computer graphics system is ultimately judged by the image on the display monitor. When your applications call for a super-high resolution monitor, here are some important factors to be considered: |
| **Simplicity** |
| A simplistic and functional display monitor design has a fundamental advantage in reliability and performance. |

| **Packaging** |
| With a compact, lightweight display monitor, you'll be able to design a more attractive enclosure* and even get higher performance. |

| **Safety** |
| A display monitor with 100 MHz video performance that merely looks good isn't good enough. It also has to conform to and meeting cost is a pretty big bill to fill. But at Ikegami, we're doing just that. As with all our display and broadcast equipment, we're reaching beyond mere specs to give you the kind of advanced design and performance you need for your system to meet excellent image quality. |

| Before you commit yourself to a 60-Hz monitor for your graphics system, take a look at what Ikegami's doing. We guarantee you, we'll really open your eyes. |

---

East Coast: 37 Brook Avenue, Maywood, NJ 07607 (201) 368-9171  
West Coast: 3445 Kashiwa Street, Torrance, CA 90505 (213) 534-0050.  
© 1984 Ikegami Electronics (USA) Inc.

| *For example, our current low profile 30 Hz monitor is interchangeable mechanically with our new 60 Hz. |
NO OTHER MILITARY COMPUTER CAN MATCH THE NEW ROLM HAWK/32.

HERE’S WHY:

Unmatched Performance
- 32-bit computational power and memory addressability
- 3.5 M.I.P.S. (fixed arithmetic operation)
- 1300 KWHETS/SEC. (single precision floating point)
- Main memory—up to 8 megabytes
- Cache memory—128 kilobytes
- External memory—maximum of 1120 megabytes on line disk (virtual memory support available)
- I/O bandwidth—12.0 megabytes per second

Unmatched Packaging Efficiency
- Compact size—1.4 cubic foot
- Complete integrated system: Central processor, Main memory, Floating point processor, Diagnostic processor, Power supply, High speed burst Multiplexer Channels, I/O interfaces (up to 7 in main chassis)
- Lightweight—90 lbs. maximum
- Low power consumption—400 watts maximum
- Mil-Spec Environmental Specifications—MIL-E-5400, MIL-E-16400, MIL-E-4158

Unmatched Price/Performance
- Under $150,000 in production quantity (Basic system with 2 megabytes of memory)

Unmatched Price/Performance
- Under $150,000 in production quantity (Basic system with 2 megabytes of memory)

Unmatched Delivery
- Shipments start October 1984

Unmatched Software Support
ROLM delivers the Hawk/32 with an extensive family of system software that includes Real Time and Virtual Memory Operating Systems, communications software and Ada® language support. (ROLM Ada support includes a DoD validated compiler, a powerful language development environment, and a choice of 32-bit commercial host development systems.) Hawk/32 is software compatible with Data General MV Series computers. ROLM maintains a worldwide service network.

For immediate information call Bob Farnsworth (408) 942-7655.

*Ada is a registered trademark of U.S. Department of Defense (OUSDRE-AJPO).
Digital image sensor

Using a 256 x 128 silicon array and menu driven software, the Micro D-CAM interprets, enhances, or stores images via a computer. With the added dimension of sight, the computer can be used in graphics, pattern and character recognition, and robotics. Utilities handle auto-exposure, multilevel gray scale, screen dumps, picture storage, and image enhancement. IBM PC and Apple II versions are available (RS-232 version available on special order). The sensor costs $295. Micromint, Inc, 561 Willow Ave, Cedarhurst, NY 11516. Circle 387

Custom-built logic switch

The microminiature device provides a direct digital interface for complex manual switching requirements. In a 0.865-in.-square package, the 28-position P/REL has a high temperature withstanding ability for wave soldering. The terminals are 0.016-in. thick for greater strength and can automatically be trimmed to any specified length up to 0.875 in. The switches sell for about $3 each in 1000-lot quantities. Standard Grigsby, a Gordos International Co, 920 Rathbone Ave, Aurora, IL 60507. Circle 388

Get your own
If you're reading someone else's copy of Computer Design, why not get your own? To receive a subscription-application form, circle 504 on the Reader Inquiry Card.

Wide-angle LED

Cylindrical sl.v 56 series features a precision cone-shaped clear lens with full 180-degree brightness. Users can mount the LED perpendicular to the PC board, but view it parallel to the board. Applications include mainframe card cages, telecommunication switch gears, and disk drives. Colors are red, orange, green, and yellow. Price in 1000 pieces is $0.25 each. Delivery is four to six weeks. Rohm Corp, PO Box 19515, Irvine, CA 92713. Circle 389

Digital filter

Providing eight delay stages, multipliers, and adders in a single IC, the TDC1028 is TTL-compatible for finite impulse response filters and multibit digital correlators. The bit-slice, video speed device provides a 20-megapixels/s throughput and 4-bit coefficient and signal data words. Format for words is selectable with a choice of two's complement or unsigned magnitude. Applications for the device include matched filters, pulse compression, waveform synthesis, and adaptive filters. TRW LSI Products, PO Box 2472, La Jolla, CA 92038. Circle 390

Instrumentation amplifier

Designed for high precision applications, the AD634 delivers maximum ± 0.001-percent nonlinearity. In addition, it provides maximum ± 10-ppm/°C gain tempco and maximum 0.2-µV peak-to-peak input and 10-µV output noise. Onchip gain setting network eliminates factoring in cost, temperature, and accuracy effects of external gain setting resistors. The pin-programmable gains permit maximum gain error from ±0.02 percent (G = 1) to ±0.5 percent (G = 1000). Four gain setting pins can connect for gains of 1, 100, 200, or 500. The 16-pin ceramic package is priced in 100s from $11.90. Analog Devices, Inc, Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. Circle 391

Hey Printronix!

Call Air Land Systems. And find out about our full line of microprocessor-based protocol converters and other data communications interfaces for line printers and other peripherals. We've already developed both hardware and software for most major communications protocols, and we're anxious to discuss your specific needs.

For example, our MPC-79 (photo) is specifically designed for PRINTRONIX printers. Some of the currently available protocols are listed at left.

AirLand Systems A name more OEMs should know!

2710 Prosperity Avenue • Fairfax, Virginia 22031-4387
(703) 573-1100 TWX: 710-833-1174 AIRLAND FRAX
to go the distance.

The more critical your networking requirements, the better proNET™ looks. Designed for total fiberoptic compatibility, proNET's token ring local area networks are delivering high-speed, high-throughput, reliable communications in uncommonly demanding systems.

Where security or factory environments...very long cable runs...fail-safe operation...ultra low error rate...and economical installed cost are essential, proNET goes the distance.

A major university networking 40 or 50 VAX™ 11/750s in a heavily interactive, data-intensive application specified proNET to provide a research facility "unbounded in what it would permit us to do." ProNET outperforms its competitors in benchmarks run under 4.2 BSD UNIX™ and DECnet™ via Ringway™.

ProNET definitely has the ring of reliability. No coincidence that companies like Apollo, Racal-Milgo, Ungermann-Bass, Ztel and now IBM have introduced or are about to introduce networks like proNET.

We'll demonstrate conclusively how proNET will take you the distance...supporting as many computers, terminals and workstations as you need...using the best media for your environment...with fast, accurate fault location and analysis...with fail-safe operation...and at the best installed cost. Call the nearest Proteon sales office or the factory directly at (617) 894-1980 or write Proteon, Inc., 24 Crescent Street, Waltham, MA 02154.

VAX and DECnet are trademarks of Digital Equipment Corporation. UNIX is a trademark of Bell Telephone Laboratories. Ringway is a trademark of Technology Concepts Inc.
Servomotor-controlled robot
The IRI M50-E is controlled by digital signals generated by a proprietary monoboard with eight micros. Servomotors improve velocity control of robot motion for more accurate path control. Operating at 400 Hz or above, the small-lightweight servos easily fit existing robot modules. Targeted for precision-oriented tasks, the robot is priced under $20,000. International Robomation/Intelligence, 2281 Las Palmas Dr, Carlsbad, CA 92008.

Digital servo system
The Model 2100-PT indexer provides precise closed-loop position control based on feedback from an optical encoder. It drives standard stepping motor translators and 25,000-step/rev motor/drives, thereby simplifying precision positioning. It connects to any standard incremental optical encoder (linear or rotary) and is suitable for ultraprecise X-Y table indexing (to 0.5 μm) and stall detection. The system is programmed via RS-232-C or optional IEEE 488 interface. Compumotor Corp, 1310 Ross St, Petaluma, CA 94952. Circle 395

Industrial microcomputer
The A-PAC, designed for programmable acquisition and control, combines a built-in analog and I/O interface with a personal computer and a logic controller. A selection of application programs is available for data logging, multiloop PID control, batch control, and distributed processing. Additional features are enhanced EPROM, battery-backed RAM, and clock/calendar. The startup kit has a CRT and keyboard peripherals, I/O interfaces, and cables. Cost is $5999. Action Instruments Inc, 8601 Aero Dr, San Diego, CA 92123.

Expert system generator
Artificial intelligence program Expert-Ease works by generating rules from examples. It will then remove redundant logic, producing a logic tree that specifies the key to the decision or the result. An expert or novice can use the inquiry facility to produce an expert decision, predict a result, or solve a problem. Applications are in fields of industry, commerce, and research. Expert Software International Ltd, 4 Canongate Venture, New St, Royal Mile, Edinburgh, United Kingdom. Circle 393

Optical inspection system
The P-SEE uses pattern verification as opposed to design rule inspection. It features nonspecular lighting that allows virtually no false readings. Cameras provide 1.67 square-ft/min of inspection at a 0.0005-in. resolution. Speed can be increased with extra cameras. Applications include inspection of PC boards, glass masters, inner layers, substrates, and flex circuits. System adapts to any host, or networks with other company equipment. DTF-MCO International, 5100 E 59th St, Kansas City, MO 64310. Circle 394

Talk to the editor
Have you written to the editor lately? We’re waiting to hear from you.
PUT MORE DRIVE INTO YOUR SYSTEM.

Teac’s FD-55 series half-high floppy disk drives run on a mere 5 watts. So now you can add more drives without the need to add more power.

In fact, Teac offers the only full line of 5¼ inch half-high mini disk drives that run on half the power of ordinary dual drive units.

And, with Teac’s brushless DC direct drive motors, you get less noise and longer life. Proven up to 10,000 hours.

So, if you’re feeling the need for more drive in your system, call us at (213) 726-0303 and we’ll get things rolling.

TEAC® ICPD
BUILT TO FANATICAL STANDARDS.

COPYRIGHT 1983. TEAC INDUSTRIAL COMPUTER PRODUCTS DIVISION, 7733 TELEGRAPH ROAD, MONTEBELLO, CALIFORNIA 90640

CIRCLE 143
Power monitor

The device features user-adjustable disturbance thresholds, disturbance value printouts, and ambient temperature and dc voltage level monitoring. It allows continuous analysis of line power quality at installation sites. An onsite pot adjustment triggers power disturbance recording. The unit monitors both the dc voltage of power supply and high frequency or spike on the dc supply line via a BNC. The monitor is priced below $2000. Sola Electric, 1717 Busse Rd, Elk Grove Village, IL 60007. Circle 397

Chassis-mountable power supply

Redesign of models CM 3.15.5 and 3.12.5 results in triple-output supplies that run cooler than before. Output of the 3.15.5 is ±15 V at 100 mA and 5 V at 500 mA, while output of 3.12.5 is ±12 V at 100 mA and 5 V at 600 mA. The 5-V output is isolated from the dual output so it can be used to power linear/digital circuit combinations. A clamp barrier strip secures wires without twisting. A recessed barrier strip makes tight connections while protecting the unit from damage. Calex Manufacturing Co, Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Circle 398

Power MOSFETs

The devices come in ratings from 50 to 500 V, 0.2 through 40 A, in six package configurations. Ultrafast switching speeds make them ideal for high frequency switching applications. The MOSFETs have low conduction losses at low blocking voltages up to 200 V. Also available are IGTS that offer high input impedance, voltage-controlled turn-on/off features of MOSFETs, and low on-state conduction losses of bipolar transistors. Initial offerings include 10- and 25-A, 500-V rated devices. General Electric Co, 1 Belmont Ave, Bala Cynwyd, PA 19004. Circle 399

Switching voltage regulator

The LAS 6320P series is a monolithic IC designed for fixed frequency pulse width modulation converter applications. Capable of output voltages from 2.25 to 24 V with output currents of 2 A, the chip features a temperature compensated voltage reference. In addition, it has a sawtooth oscillator with overcurrent frequency shift, linear trailing edge pulse width modulator, and transconductance error amp. The device is available in a 14-pin plastic DIP with prices ranging from $2.20 to $4.50 depending on quantity. Lambda Semiconductors, div of Veeco Instruments, 121 International Dr, Corpus Christi, TX 78410. Circle 400

Converting with 4:1 input range

Additional models in the WP series provide 25 to 30 W of isolated regulated power. They operate over a 9- to 36-Vdc input range and have outputs of 5 V at 5 A, 6 V at 4.5 A, 12 V at 2.5 A, and 15 V at 2 A. The units accept standard battery inputs of 12, 24, or 28 V with virtually no deviation in performance over the entire range. Features include efficiencies up to 85 percent, 500-Vdc isolation, input surge protection to 50 Vdc, and output noise of 5 mV rms, maximum. Prices range from $149.30 to $209, depending on quantity. Stevens-Arnold, Inc, 7 Elkins St, Boston, MA 02127. Circle 401

Filtered power module

The series FPM incorporates an IEC power input receptacle, on/off switch, fuse protection, emi filter, and a voltage selector. Isolation of the line and load wiring is provided by an emi filter directly at the input source. The IEC connector, together with the emi filter, eliminates virtually all coupling of the module. It uses either a 5-mm or standard ⅛ x ⅛ fuse; the voltage selector provides 120- or 250-Vac operation. Prices start at $17.88 in 100-piece lots. Stanford Applied Engineering, Inc, 340 Martin Ave, Santa Clara, CA 95050. Circle 402

Hey Dataproducts!

Call Air Land Systems. And find out about our full line of microprocessor-based protocol converters and other data communications interfaces for line printers and other peripherals. We've already developed both hardware and software for most major communications protocols, and we're anxious to discuss your specific needs.

For example, our MPC-51 and MPC-73 (photos at left) are specifically designed for DATA-PRODUCTS 8300/8600 and M200 printers. Some of the currently available protocols are listed at left.

Air Land Systems A name more OEMs should know!

2710 Prosperity Avenue • Fairfax, Virginia 22031-4387
(703) 573-1100 TWX: 710-833-1174 AIRLAND FRAX
“Looking for bus compatible data acquisition boards? You’ve come to the right guy.”

This isn’t just a line. Data Translation offers the most complete line of analog I/O boards available. Anywhere.

We have LSI-11™ Bus, MULTIBUS™, UNIBUS™, IBM PC™ Bus, STD Bus, and Apple™ Bus. You’ll never have to change buses to get the analog compatibility you need.

And you won’t be left stranded for help ... our user manuals and thorough diagnostics guide you through any technical roadblocks. All for the same low fare.

So whether you’re in scientific research or industrial control, call us. We’re the world’s leading supplier of analog I/O boards, systems and software.

We’ll have you up, and on line, in no time. Call (617) 481-3700.
Triple-output switcher

Model KFD-40E meets UL/CSA and international safety specs IEC 380 and VDE 0806. The 40-W dual-input unit is available with three outputs of 5 V at 5 A, 12 V at 2.5 A, and -12 V at 0.5 A. Applications include CRT terminals and modems. The 25-piece price is $74.

KEC Electronics, Inc, 20817 Western Ave, Torrance, CA 90501.

Circle 403

Dual-mode suppression filters

The devices provide control of line to ground noise and reduce low frequency line to line noise and transients. They will protect equipment from malfunctions due to conducted interference coming into the equipment from the line. Specs include rated voltage 115/250 Vac; rated frequency 50-60 Hz, 0.5 mA; and line to ground at 250 Vac/50 Hz, 1 mA. The filters are designed to meet UL and CSA standards. RTE Aerovox, Inc, 740 Belleville Ave, New Bedford, MA 02745.

Circle 404

Rechargeable lead-acid battery

Model RS-12150 is a 12-V unit with 1.3 Wh/cubic in. Sealed construction lets the battery be used in any position. The 15 Ah battery fills a gap between the 10- and 20 Ah capacities. Applications include UPS systems, telecommunication equipment, standby power for micro-based devices, and alarm systems. The battery weighs 12.8 lbs, can be recharged 300 to 400 times, and has a life expectancy of over 5 years.

Power-Sonic Corp, PO Box 5242, Redwood City, CA 94063.

Circle 405

Power transistors

Faster than comparable bipolar transistors, Power MOS devices function as majority carrier devices without storage time. Voltage drive requirements are just above threshold; high input impedance allows a voltage generator to drive them. The generator need only provide adequate charge of the input capacitance. The devices use an n-channel structure with multiple square cells. Twenty-eight types cover nine voltage ranges from 50 to 400 V. Prices in 1000-piece quantities range from $0.62 to $1.95.

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022.

Circle 406

Chip with negative voltage levels

With two external capacitors, the TSC7600 converts a 1.5- to 10-V input signal to a 1.5- to -10-V level. It allows 5-V digital logic systems to incorporate analog components without adding an additional main power source. The chip charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across output. The negative open circuit output voltage is within 0.1 percent of the positive input voltage. Available in 8-pin DIPs, prices range from $1.90 to $8.

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043.

Circle 407

Lithium power cells

The AL2-AA cells offer high performance, long life, and safety of lithium thionyl chloride batteries in a standard AA package. They feature durable stainless steel construction and a ceramic to metal seal for reliable operation. Cells deliver a standard open circuit voltage of 3.6 V and have a shelf life of more than 10 years. They are unaffected by spin, altitude, or position. Nominal capacity is 2 A-h at the 23-mA rate at 20 °C to a 2.5-V cutoff.

Altus Corp, 1610 Crane Ct, San Jose, CA 95112.

Circle 408

March Preview
Special Report on Advanced Digital ICs

Hey General Electric!

Call Air Land Systems. And find out about our full line of microprocessor-based protocol converters and other data communications interfaces for line printers and other peripherals. We've already developed both hardware and software for most major communications protocols, and we're anxious to discuss your specific needs.

For example, our MPC-29 and PCU-62 (photos at left) are specifically designed for GE 200 and 3000 printers. Some of the currently available protocols are listed at left.

* GE Data Communications Products recently acquired by Gencom Corp.

Air Land Systems A name more OEMs should know!

2710 Prosperity Avenue • Fairfax, Virginia 22031-4387
(703) 573-1100 TWX: 710-833-1174 AIRLAND FRAX

CIRCLE 146  COMPUTER DESIGN/February 1984 293
CONFERENCES

FEB 28-MAR 1—Compcon/Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142


MAR 12-16—International Conf on Robotics, Atlanta Hilton, Atlanta, Ga. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142


MAR 25-28—Numerical Control Society Technical Conf and Expo, Queen Mary Hotel, Long Beach, Calif. INFORMATION: Lisa Schultz, Numerical Control Society, 111 E Wacker Dr, Suite 600, Chicago, IL 60601. Tel: 312/644-6610

MAR 26-30—International Conf on Software Engineering, Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142


APR 4-11—Hannover Fair, Hannover, West Germany. INFORMATION: Delia Assocs, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

APR 5-7—Comdex/Winter, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

APR 10-12—Infocom, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

APR 18-20—Optical Data Storage, Monterey Convention Ctr, Monterey, Calif. INFORMATION: Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. Tel: 202/222-8130

APR 24-27—Comdec (International Conf on Data Engineering), Bonaventure Hotel, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142


APR 30-MAY 2—Workshop on Computer Vision, Hilton Hotel, Annapolis, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142


MAY 15-17—Electro, Bayside Exposition Ctr and Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 15-17—Mini/Micro-Northeast, Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

MAY 22-25—Comdex/Spring, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

MAY 26-30—International Conf on Software Engineering, Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 4-8—SID (Society for Information Display International Symposium), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

JUNE 5-7—International Symposium on Computer Architecture, Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-6517

JUNE 5-7—Symposium on Mass Storage Systems, Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. Tel: 303/494-5151

JUNE 6-8—Communications Architectures and Protocols, Montreal, Canada. INFORMATION: Rebecca Hutchings, Honeywell/FSD, 7900 Westpark Dr, McLean, VA 22102. Tel: 703/827-3982

JUNE 19-22—International Symposium on Fault Tolerant Computing, Hyatt Orlando, Orlando, Fla. INFORMATION: Richard Sedmak, Sperry Univar, PO Box 500, MS C15W12, Blue Bell, PA 19404. Tel: 215/542-3638

JUNE 24-27—Design Automation Conf, Albuquerque Convention Ctr, Albuquerque, NM. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 9-12—National Computer Conf, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 23-27—Sigsgraph Conf on Computer Graphics and Interactive Techniques, Minneapolis, Minn. INFORMATION: Lynn Valastyan, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

JULY 30-AUG 2—International Pattern Recognition Conf, Montreal, Canada. INFORMATION: ICPR Secretariat, 3450 University St, Montreal, Quebec, Canada H3A 2A7. Tel: 514/392-6744

SHORT COURSES


PLAY PRO BALL WITH OUR CLASSIC TEAM OF COMPATIBLE REAL-TIME COMPUTERS.

A real-time choice. From 16-bits to our new 32-bit CLASSIC.

Only MODCOMP has assembled an unbeatable team of real-time computers for demanding industrial, scientific and communications applications. Computers capable of responding to critical real-time interrupts faster than any other computer.

Now meet our new star performer, the CLASSIC 32/85. The statistics are impressive: A powerful and versatile operating system initiates large numbers of priority-based tasks in microseconds. Multiple sets of map caches and general purpose registers provide an unparalleled context switching rate when responding to critical real-time interrupts. And 64 megabytes of multiplexed memory permit high performance multiprocessor designs incorporating multiple CPUs and I/O processors.

The 32/85 is compatible with MODCOMP's entire team of 16-bit computers. In fact, it will run your application more than twice as fast as our 16-bit high-end model, the CLASSIC II/75.

Remember: For a winning combination of real-time performance and compatibility, there's one team that ranks above all the rest.

The CLASSICS from MODCOMP:

For more information, call our toll-free number today.

1-800-327-7042
Fortunately, our miniature switch is a lot smaller than its list of features.

As small as they are, you might not think there is much room for a lot of advanced features in our MML Miniature Manual Line.

But the truth is that the MICRO SWITCH MML has a combination of features you won’t get with other miniature products.

**Good looks** help your product look good. MML switches give you consistent, compatible, high-quality appearance.

**Human factors features** provide a better interface between your product and its operator. You get smooth button travel, positive tactile feedback, and a number of color and legend options, with LED or incandescent lighting.

**Variety** gives you unparalleled design freedom. Choose from coordinated pushbuttons, indicators, and mechanical interlocks, all in solid-state or contact versions. And you get flexibility from the MML mounting, termination, and electrical options.

You’ll find our line is still growing with additions like new encoding switches. There’s even an exclusive electrostatic discharge protection up to 25 Kv available on MML pushbuttons.

**Quality** means MML will perform as promised, to help your product do the same. All MML switches are designed to meet UL, CSA, and other international standards.

**Small size** allows you to downsize even complex panels, without giving up performance. MML offers all these features while taking up just 10 x 15 mm of panel space, with a housing only 17 mm deep.

**Authorized Distributors** offer local assistance and availability. So you get the MML product you need, when you need it.

**And a FREE sample offer.** Try an MML for size and see its advantages for yourself. For more information on MML, the free sample offer, and any of our other manual control products, contact MICRO SWITCH, Freeport, IL 61032. Phone 815-235-6600.

Together, we can find the answers.

MICRO SWITCH
a Honeywell Division

CIRCLE 148
Scope measurement system
Circle 410

Isolated input MUX
Data sheet summarizes essentials of DMS504; plug compatible with LSI-11, Multibus, IEEE 488, and RS-232/RS-422 formats, the unit handles input voltages of ±5 mV to ±10.24 V full scale. DI-AN Micro Systems, Ltd, Cheshire, England.
Circle 411

Flat-panel switches
Ordering catalog gives technical and application background for RAFI 15/19 dust and waterproof push buttons, accompanied by construction and dimensional drawings. Ledex Inc, Vandalia, Ohio.
Circle 412

Macrocell library
Software data book has tools for semicustom design of LSI II5000 series gate arrays on Daisy Systems Logician, Mentor Graphics Idea 1000, and Valid Logic SCALD system engineering workstations; macrocell model data sheets, tutorial documentation, and information on gate array design rules are included. LSI Logic Corp, Milpitas, Calif.
Circle 413

Modular switches
Brochure highlights momentary and alternate versions in various keycaps and bezels, covering cross sections, specs, function-principles, and wiring diagrams. MEC, Electronic Components Group, Minneapolis, Minn.
Circle 414

Cards for STD bus
More than 35 cards are featured in 16-page catalog detailing Approach series microcomputers for machine control and Romaid 2704 programmer/simulator for software debugging. Micro-Link Corp, Carmel, Ind.
Circle 415

Digital panel meters
Selection guide covering 22 manufacturers tabulates about 80 panel meter features as they relate to specific applications; typical listings include scaling adjustments, control outputs, data formats, mounting techniques, display types, and reliability considerations. Nationwide Electronic Systems, Inc, Streamwood, Ill.
Circle 416

Circuit data to CAD/CAM
Application note describes how to transfer circuit information from typical CAD/CAM systems to automatic testers, as well as how to generate circuit files off-line. Advanced Microcomputer Systems, Inc, Coral Springs, Fla.
Circle 417

Custom resistor networks
Eight-page technical bulletin details specs for axial lead, high reliability, lug terminal, subminiature, and printed circuit type resistors, following up with circuit applications and diagrams for encapsulated networks. Armetec Industries, Inc, Manchester, NH.
Circle 418

Sockets and assemblies
Ordering catalog lists over 200 Asmann components, including DIP, test and transistor, and LED/LCD sockets; carrier assemblies; and contact terminal strips. Precision sockets fit standard DIPS with a 0.100- x 0.100-in. pin spacing. ebm Industries, Inc, Unionville, Conn.
Circle 419

Molded disconnects
Bulletin describes continuously molded, fully insulated female Pan-Term units supplied on 3000-piece reels for wire ranges from 22 to 14 AWG. Panduit Corp, Tinley Park, Ill.
Circle 420

Data communication equipment
Circle 421

Professional plotters
Folder features Hiplot DMP-41 and -42 models, listing firmware commands as well as operating and electrical/mechanical specs. Houston Instrument, Austin, Tex.
Circle 422

Pancake synchros and resolvers
Circle 423

Transmission line assemblies
Twenty-page source book covers design and testing of multiple- and single-signal assemblies and accessories; chart cross-references part numbers with cable, connector, and measurement data. Chabin Corp, Chico, Calif.
Circle 424

Unix ported to minicomputer
Four-page leaflet outlines Unix System it implementation in dataCASE/5, which offers over 1-MIPS performance, 560-Mbyte storage, and 5-Mbit/s data transfer. Computer Automation, Naked Mini Div, Irvine, Calif.
Circle 425

Ceramic disks and capacitors
Forty-page catalog provides detailed specs and performance curves for low voltage, temperature compensating, rectangular plate, and medium to Hi K, as well as disk and high voltage, ceramic capacitors. Murata Eric North America, Inc, Marietta, Ga.
Circle 426

Test and measurement
Eighty-page catalog features 13 scopes including a 100-MHZ, four-channel and a 50-MHZ, two-channel dual time base model, along with four frequency counters ranging from 80 MHz to 1 GHz. Leader Instruments Corp, Hauppauge, NY.
Circle 427

Low cost PC drafting system
Specs and detailed price list summarize IBM XT/PC 68000 two-dimensional drafting system with three-dimensional modeling, which is also compatible with the full range of PC software. Summit CAD Corp, Houston, Tex.
Circle 428

Portable test equipment
Six-page folder features the Tracer-2 signature analyzer, which generates a characteristic waveform pattern on a 2.5-in. CRT; the 3-lb miniscope MS-230 and other portable testers are also outlined. Non-Linear Systems, div of Kaypro Corp, Solana Beach, Calif.
Circle 429
Coaxial cable assemblies

Full-line, 120-page catalog gives electrical, mechanical, and environmental data for subminiature and miniature connectors, along with field-replaceable launchers and semi-rigid cable assemblies. Applied Engineering Products Inc, New Haven, Conn.

Circle 430

Thin-film hybrids


Circle 431

Instrumentation computer

Booklet features six pages of hardware and software specs for multitasking model 6000, with applications in instrument control, industrial automation/test, military/aerospace, and manufacturing. Wavetek, Inc, San Diego, Calif.

Circle 432

Card connectors

Technical data describes and specifies DIN 41612 printed circuit card connectors in styles B, C, and D; drilling layouts and prices are included in 12-page catalog. Amlan Inc, Stamford, Conn.

Circle 433

Video course in VLSI design

Brochure describes introductory VLSI design course, which deals with principles and techniques through first silicon. Course consists of 17 color videotapes, study guide, and textbook. Massachusetts Institute of Technology, Center for Advanced Engineering Study, Cambridge, Mass.

Circle 434

Electronic components

The 160-page 1984 catalog contains specs, performance curves, and dimensional drawings for over 12,000 in-stock items. Mouser Electronics, Santee, Calif.

Circle 435

Read-only CMOS memories

Twenty-page brochure lists complete line of mask-programmable ROMS, detailing pinout diagram and significant features for each basic type. RCA/Solid State Div, Somerville, NJ.

Circle 436

Open frame linear power

Eight-page brochure lists complete electrical/mechanical specs and tabulates voltage/current ratings for Universal series. ACDC Electronics, Ocean-side, Calif.

Circle 437

Idris application software

Third-party directory lists over 20 application packages running under Unix look-alike operating system; also included are product profiles, hardware requirements, and prices/ordering information. Whitesmiths, Ltd, Concord, Mass.

Circle 438

Stock relays

Forty-page bulletin describes physical and electrical characteristics of reed, solid-state, hybrid, sensitive, and power relays; selection guide identifies switching capabilities, coil voltage ranges, contact styles, and series number. Sigma Instruments, Inc, Braintree, Mass.

Circle 439

Piezoelectric buzzers

Six-page bulletin gives spec charts and technical diagrams for electronic buzzer elements, covering styles, dimensions, characteristics, mounting modes, resonator frequency formula, and driving circuits. Rosenthal Technik North America, Inc, Providence, RI.

Circle 440

Equipment for emi/emi

Fifty-two page guide describes and specifies over 500 items from major manufacturers; reference section lists handbooks on emi/emi technology. Tucker Electronics Co, Garland, Tex.

Circle 441

Solid state relays

Miniature units rated at 25 A, 120/240 Vac are subject of six-page brochure that gives engineering specs, dimensional and wiring diagrams, and current/surge graphs. Grayhill, Inc, La Grange, Ill.

Circle 442

Storage management

A 486-page handbook presents a line of controllers and support devices for Winchester and floppy disks, as well as Winchester board and main memory products; items feature proprietary VLSI and are compatible with SASI, Multibus, general purpose, and custom interfaces. Western Digital Corp, Irvine, Calif.

Circle 443

Local area networks

Thirteen-page booklet explains access methods and environmental factors involved in selecting a LAN, discussing 10-Mbit/s Unit-LAN in detail; baseband, broadband coaxial, and fiber optic cable are covered. Applitek Corp, Wakefield, Mass.

Circle 444

Technical overview of Z8

Twenty-three page booklet on single-chip microcomputer family describes entire line of circuits and support products, including development module and Z-Scan 8 in-circuit emulator. Zilog, Inc, Campbell, Calif.

Circle 445

Microcircuit packaging

Illustrated short-form catalog explains design, production, packaging, and applications for DIPs, solid sidewalls, TO-5 and TO-8 headers, all-metal flats, and power hybrids. Airpax Corp, Cambridge, Md.

Circle 446

Slide-on coaxial connectors

Sixteen-page brochure outlines design features, sizes, electrical properties, and performance of miniature to subminiature connectors. Sealelectro Corp, RF Components Div, Mamaroneck, NY.

Circle 447

Variable-frequency ac

Folder profiles family of Class D ac power sources; performance specs for standard 12-to-72-kVA models in single- and triple-phase versions are included. Helionetics, Inc, Irvine, Calif.

Circle 448
The big difference in VMEbus hardware from one company to another is the company.

The VMEbus is making a tremendous impact internationally. Through our involvement, we've learned that all VMEbus products appear to be pretty much alike, but there are important differences.

Take it from us, when you're buying VMEbus equipment you're really buying the manufacturer. His services, standards, prices and promises.

Products can be virtually the same. It's the company that makes the biggest difference. And that's why BICC-Vero hardware is recognized by international companies for its remarkable performance, reliability, precision, and compatibility.

Our extensive inventory and efficiency guarantees you immediate delivery on all VMEbus products. Orders are handled by our worldwide network of subsidiaries and distributors to ensure prompt service and customer satisfaction.

BICC-Vero offers these VMEbus products from stock right now: IEC connectors, prototype boards, backplanes, extender cards, power supply with power monitor module, card frames and front panels.

When you need VMEbus equipment, turn to us.

Our hardware is as fine as anybody's. It's the company that's better.

BICC-VERO
ELECTRONICS INC.

BICC vero

A BICC Company
171 Bridge Road
Hauppauge, NY 11788
(516) 234-0400
TWX: (510) 227-8890

4001 Leaverton Court
Anaheim, CA 92807
(714) 630-2030
Telex: 277732

TELEPHONE: UNITED KINGDOM (04215) 66300 • FRANCE (4) 402-46-74
• WEST GERMANY (0421) 82818 • SOUTH AFRICA 53-7846/7 • CANADA (613) 384-1142

CIRCLE 149
HOW TO ORDER:
15-DAY FREE EXAMINATION
(U.S. AND CANADA ONLY)
Simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine. Your book will be sent to you for your 15-day free trial. If you are satisfied, keep the book and an invoice will follow. Otherwise return the book by the end of the 15-day period, and owe nothing.

REAL-TIME COMPUTING
With Applications to Process Data Acquisition and Control
by Duncan A. Mellichamp
Become expert at controlling and monitoring a wide variety of EDP processes. Real-Time Computing shows you how to design the best system for specific applications, effectively manage each system, and use sampled-data mathematics to design and analyze computer-controlled processes. It explains the use of multitask programming, multiple computer systems, and hierarchical configurations.
$39.50 Circle 455

OPERATING SYSTEMS
A Pragmatic Approach
by Harry Katzan
Computer pro Harry Katzan provides here authoritative coverage of the construction, functions, and terminology of operating systems. He fully explains such areas as dynamic loading and address translation, use of public and private storage, and virtual memory, data sets, and access methods. "A valuable addition to any computing library."
374 pp, 6 x 9, $10.95, February Circle 456

ABSTRACTION MECHANISMS AND LANGUAGE DESIGN
by Paul N. Hilfinger
The research reported in this book advances the art of designing programming languages. It sets forth some design principles for abstraction mechanisms and demonstrates their power by showing how they led to improvements in the design of Ada, a new language devised for the Department of Defense and one that will be wisely used in DOD-related projects.
173 pages, 30 illus., $27.50 Circle 457

FORMAL SPECIFICATION OF INTERACTIVE GRAPHICS PROGRAMMING LANGUAGES
by William R. Mallgren
Formal specifications of practical software systems have become widespread—except in the area of computer graphics systems. Because of the variety of special constructs that are needed in graphics programming, these systems have been invariably described by informal means. Some of the difficulties have been overcome in this book, which documents for the first time a complete method for specifying all parts of interactive graphics programming languages.
269 pages, 16 illus., $35.00 Circle 458

ALGORITHMS FOR GRAPHICS AND IMAGE PROCESSING
by Theo Pavlidis
Technological developments over the past ten years have made computer graphics and image processing by computer popular. Contained in this book is an indepth treatment of pictorial information processing by computer, including computer graphics, computer image, processing and pictorial pattern recognition. An ideal reference source for students, industrial employees and advanced hobbyist.
Introducing the Freedom 200.
No other VDT gives you more, for less.

For only $745, the Freedom 200 gives you more user-relevant functions and optimized ergonomic features than any other standard VDT.

You get 106 keys, clustered for maximum user efficiency.

Plus 10 user-programmable non-volatile function keys (256 bytes worth) for a host of applications.

Plus 11 cursor control keys, including tab by word for easy editing.

Plus flexible non-volatile set-up modes, full page or status line, to easily configure your terminal exactly the way you want it.

Plus user-definable smooth scrolling regions, with selectable scroll rates.

Plus split-screen capability.

Plus 128 ASCII characters, with 86 extended graphic characters for forms creation.

Plus non-embedded attributes (visual and data entry).

Plus double-high/double-wide characters.

Plus programmable answerback message for enhanced security.

Plus programmable time out, to prolong the life of your screen.

Plus easy serviceability, and space for add-on boards.

Plus two-page standard memory in emulation modes and one-page memory in native mode, with additional memory optional.

Plus 8 foreign character sets.

Plus TeleVideo 950 and Lear Siegler ADM 31 emulation.

Plus more.

To find out more, contact your local Liberty dealer or distributor.

Or call Liberty direct.

(415) 543-7000.

No other VDT gives you more, for less.
The Class of '84

At Brown Disc, we have spent the last two and a half years developing sophisticated flexible disc coating formulations, processes and quality methods. We have timed our developments to coincide with the growing maturity of the flexible disc industry.

Volume users of flexible discs are becoming increasingly aware of the need for a higher quality flexible disc. End-users are demanding more out of their systems. This means you need the best diskette, at a competitive price. With Brown Diskettes, you can be sure you have the best. If you've evaluated our products, you know our quality.

In our new 106,000 square foot manufacturing facility, we produce 3¼", 3½", 5¼", and 8" media with capacities up to 6.34 megabytes. With our advanced spin-coating technology, we can also help you develop future systems that utilize high density flexible disc drives.

Put Brown Disc's advanced technology to work for you. Give us a call at 1-800-654-4871...we'll be happy to talk straight with you. 1984 is our year. Make it yours, too.
The I.E.E.E. 796 Version of the well known Promblaster™. This board programs 1K x 8 to 32 x 8 eeproms: 2508, 2716, 2732, 2732A, 2763, 2764, 2764A, 27128, 27256.

- Function as an I/O device
- Uses fast programming algorithm on 2764's and up

Software: Written in C, and menu-driven. Contact:

ACKERMAN DIGITAL SYSTEMS
216 West Stone Ct., Villa Park, IL 60181
(312) 530-8992

CIRCLE 478

6800 Family Cross-Software

6800/01/05/09 microprocessor software development tools for PDP-11, VAX, IBM or other mainframes: Cross-Assemblers, High-level Languages, PL/I, W Compilers, Linker, and Simulators.

CP/M CROSS SOFTWARE for the NS16000

INCLUDES:

- Cross Assembler
- Cross Linker
- Debugger
- Librarian
- Pascal Cross Compiler

Prices start at $500 for Assembler only.

SOLUTIONWARE CORPORATION
1239 Mt. View-Aviso Rd. Suite B
Sunnyvale, CA 94086
408/745-7818

CIRCLE 483

I0-5026

Now VME systems can be designed with all the mechanical ruggedness and simplicity of other bus structures, yet with the full performance only possible with VME. The VME 805 is one of the family of card cages with 5 slots. Other units offer 7, 9, 12, 16, or 20 slots all with full compliance VME backplanes. It's particularly easy to configure systems with both double size and single size boards with Electronic Solutions proprietary center adapters. Each adapter converts a double size slot into two single size slots, and they can be installed, relocated or removed in seconds. For Technical or Application Assistance call: 800-854-7086. In California 800-772-7086.

CIRCLE 483

Serial PRINTERS! PLOTTERS! PUNCHES! ROBOTS!

Convert What You Have To What You Want!

• RS232 Serial
• RS422 Serial
• Bidirectional
• Latched Outputs
• Programmable

No longer will your peripheral choices be limited by the type of port you have available! Our new High Performance 750 Series Serial Card provide the missing link. Based on the popular 75C245 silicon, the Card offers 8-bit synchronous data rate selection to 19.2K, with handshake signals to maximize transfer efficiency. Detailed documentation allows simplified installation. Order the Model 770 (Serial) or Model 775 (Parallel) Today!

CALL (805) 487-1666 or 487-1666

For FAST Deliveries

CIRCLE 477

SOLID STATE POWER FET AC/DC RELAY

Teledyne’s C46/C47 series are pin compatible replacements for DIP reed relays where low EMI switching, high reliability and long life are required. Switches AC or DC up to 400V. On-resistance as low as 7 ohms. Control voltage range is 3.8 to 32VDC. Optical coupling provides 1500VDC isolation. Features no offset voltage, low off-state leakage, and high switching speed. $5.80 ea for 5000 pcs.

TELEDYNE RELAYS, 12525 Daphne Ave, Hawthorne, CA 90250. Tel: (213) 777-0077.

CIRCLE 480
The RAM Board That Remembers.

GDX®

NVRAM-256 Expansion Module
- Stores 256 bytes of information
- No batteries required. Runs from 5 volts
- Combines static RAM with "shadow" E2 PROM
- Fast operation: read/write to RAM (300 nsec);
  Recall (1.2 usec); bulk store (10 msec)
- Direct, auto-increment/decrement address
  register functions
- Reliable, long life
- Quantity 1 Price $240, available from stock to
  30 days

General Digital Corporation
700 Burnside Avenue, E. Hartford, CT 06108
(203) 528-9041
Expansion modules for all requirements

CIRCLE 484

COMPUTER DESIGN/SUPER DECKS

- Now 90,000 circulation - 75,000 qualified Computer Design U.S.
  subscribers, plus 15,000 pass-along
  engineer inquirers
- Six mailings in '84 - January, March, May, July, September and November
- Less than a penny per card for 6 time
  users.
- Rates start at $1195.00 and go down with
  frequency.
- Closing 21st of previous month of
  mailing.

Contact Shirley Lessard, Computer
Design, 119 Russell St, Littleton, MA
01440. Tel: Toll Free (800)225-0556.

CIRCLE 490

MULTI-PORT SERIAL CARD FOR
S-100 (IEEE-696) SYSTEMS

Designers who need an IEEE-696 serial
interface card have a choice of either 2 or 4
ports with the Multi-Port Serial Card. Each
port can operate as either a "data set" or as
a "data terminal." Independent baud rate
generators for each port (50-19,2k baud)
and an 8-level vectored interrupt controller
are provided. 36" cables are included.

Single Qty: $280.00 (4-port), $210.00
(2-port).

Seattle Computer Products, Inc.
114 Industry Dr, Seattle, WA
98033. Tel: 1-800-426-8936.

Dealer and OEM inquiries are invited.

CIRCLE 491

FLOPPY DISK CONTROLLER
FOR S-100 (IEEE-696) SYSTEMS

Disk Master™ by Seattle Computer con-
trols as many as four 8" and four 5.25" flopp-
ny disk drives simultaneously, in any combi-
nation. It can be configured for virtually any
floppy disk drive on the market. The Disk
Master based on the 1793 disk controller
chip. It is fully IEEE-696 compatible and can
be used with CPU's operating to 10 MHz.
Single quantity: $325.00. Dealer and OEM
inquiry: 1 Price. Seattle Computer
Products, Inc., 114 Industry Drive,
Seattle, WA 98033. Tel: (800)426-8936.

CIRCLE 482

Ada® PROGRAMMING WORKSTATION

MC68000 based computer system supports
development of Ada™ programs. Providing
the highest performance native code
compiler commercially available, LabTek
utilizes Telesoft-Ada which is expected
to validate 1984. Price including 768K
RAM, 15MB Disk and Telesoft-Ada $14,990.

Labtek Corporation
111 Saugatuck Ave, Westport, CT 06880
(203) 227-5334
Ada® Registered trademark US Govt AIPO

CIRCLE 485

Two Channel Interface at Single
Channel Prices

SERIAL-2S Expansion Module
For low cost serial communication with
system peripherals
- Two independent RS-232C compatible
  ports
- Based on popular 8251A USARTs
- Uses baud generation circuitry of host
  single board computer
- Quantity 1 Price $760, available from
  stock to 30 days

General Digital Corporation
700 Burnside Avenue, E. Hartford, CT 06108
(203) 528-9041
Expansion modules for all requirements

CIRCLE 486

Two Channel Interface
at Single
Channel Prices

SERIAL-2S Expansion Module
For low cost serial communication with
system peripherals
- Two independent RS-232C compatible
  ports
- Based on popular 8251A USARTs
- Uses baud generation circuitry of host
  single board computer
- Quantity 1 Price $760, available from
  stock to 30 days

General Digital Corporation
700 Burnside Avenue, E. Hartford, CT 06108
(203) 528-9041
Expansion modules for all requirements

CIRCLE 486

ZY8000™ MULTIBUS™ SBC
Z8001 or Z8002 16-bit CPU (6 MHz); 32K
or 128K DRAM (upgradable to 612K); up to
48K static RAM or EEPROM; up to 256K
EPROM; 2 RS-232 ports (82030 SCC); 40
parallel I/O lines and six 16-bit counter
 timers (28036 CIOs); vectored interrupts;
two 8-bit DIP switches. EPROM resident
Debug Monitor, MICRO CONCURRENT
PASCAL, C, FORTH, VRTX. Develop Z8000
software on your IBM PC, PDP-11, Intel
MDS, Olivetti M20 or any 8080/Z80 CP/M
system. Z8000™ Zilog, Multibus™ Intel
Corp. SINGLE BOARD SOLUTIONS, 7669
Rainbow Drive, Cupertino, CA 95014.
(408) 253-0181

CIRCLE 489

COMPUTER DESIGN
February 1984
You already know about ILS, the world standard in signal processing software. Currently performing in hundreds of VAX and PDP-11™ sites, ILS has met the rigorous standards for inclusion in DEC’s™ exclusive EAS library. Applications include speech, noise and vibration, seismology, acoustics, biology, sonar, radar, medicine and simulation.

What you may not know is that lightning has struck. ILS is now infinitely more flexible and versatile. Just look how it can work wonders for you:

**Workstation ILS — save up to 60%.** Now there’s VAX-quality signal processing software for use on the DEC MICRO/PDP-11. Convenient and versatile, these programs are ready to run—and priced to save up to 60% over traditional ILS.

**ILS-SKY — megaflops at micro prices.** Supercharge your signal processing with new ILS-SKY, which integrates software calls to the SKYMNK array processor from SKY Computers, Inc. ILS-SKY gives you lightning-fast signal processing at the lowest price in the industry. Get instant high performance from your array processor without programming!

**Even more ILS choices.** If you don’t need the whole ILS package, you don’t have to buy it. Now you can get either ILS/DSP or ILS/SPEECH separately, to save you money and increase productivity.

If you still don’t believe in miracles, we’ll even tell you how to buy the SKYMNK processor and ILS-SKY software in binary form at a special package price. We’ll also send a brochure and price list on the complete range of ILS products. If you’d like to see ILS in action, we’ll set up an on-line demonstration with your compatible graphics terminal and modem. Or ask about our ILS videotape presentation. Once you see this miracle, you’ll believe it.

**Signal Technology, Inc.**
5951 Encina Road
Goleta, CA 93117
Call toll-free (800) 235-5787
In California, (805) 683-3771
TWX 910-334-3471

Germany • TCAE GmbH, Tel: 8/39/6067, Telex: 527823
Sweden • 3K Tre Konssultor AB, Tel: 076/30176, Telex: 15559
Switzerland • Computer-Graphics AG, Tel: 1/932 3424, Telex: 87547
Japan • Riken Corp., Tel: 3-945-1411, Telex: 163772
U.K. • Logica Ltd., Tel: 093260/3135, Telex: 267413
VAX, PDP-11, and DEC are trademarks of Digital Equipment Corporation.

CIRCLE 152
AD INDEX

Able Computer ................................................................. 214
   Cochrane Chase Livingston & Co Inc
ACC ................................................................................. Cover IV
Ackerman Digital ............................................................... 303
ACM/Siggraph ................................................................. 263, 265, 267
ADE Corp ............................................................................. 217
   Floudaras Associates Inc
Advanced Digital Corp....................................................... 104
   Evergreen Communications
   Advanced Electronics Design
   Reiser Williams De Yong/C&W
Advanced Micro Devices .................................................. 12, 13
   Keyel/Donna/Pearlstein
Air Land Systems ............................................................... 287, 289, 291, 293
   Stackig Sanderson & White, Inc
Airpix Corp, Inc ................................................................. 235
   Lewis, Gilman & Kynett Inc
Alpha Wire Corp ................................................ ................. 237
Alps Electric (USA) ............................................................. 38, 39
   Industrial Marketing Associates
American Hoechst Corp ..................................................... 109
   Creamer Inc
AMP .................................................................................. 132, 133
   Lewis, Gilman & Kynett Inc
Amphenol, an Allied Co. .................................................... 84, 85
   Marsteller, Inc
Analog Devices ................................................................. 86, 87
   Giardini/Russell Inc
Applied Micro Circuits Co ................................................... 79
   Manning & Associates
AST Research ................................................................. 65
Atasi Corp ........................................................................... 134, 135
   Lone, Lord & Schon
Audiotronics ...................................................................... 95
Auscorn ............................................................................. 174
   Bonner McLane Advertising Inc
Bailey Controls Co ............................................................. 280
   Equity Advertising
BICC-Vero Electronics Inc ................................................... 299
   Business Pearce Ltd
Business Computing ........................................................... 251
Brown Disc Manufacturing ............................................... 302
Bruel & Kjaer .................................................................... 193
   Advertising Assistance, Inc
CalJens ................................................................. 141
   Jansen Associates Inc
California Devices ............................................................. 202
   Winston Advertising Inc
Callan Data Systems .......................................................... 157
   Abert Newhoff & Burr Inc
Carroll Touch Technology ................................................... 268
   Richard Newman Associates Inc
Centronics ......................................................................... 190
   Mullen Advertising Inc
Cherry Electrical Products ................................................. 230
   Kolb & Bauman Advertising, Inc
Chrislin Industries ............................................................. 14
Cipher Data Products ......................................................... 70, 71
   Richter & Carr
Coherent Systems ............................................................. 278
   Pattillo Advertising Services
Compower ................................................................. 263
   Power Products Promotions
Computer Automation ......................................................... 55
   Cochrane Chase Livingston & Co Inc
Computer Products ........................................................... 282
   Marvel Inc.
Conrac Corp ...................................................................... 82, 83
Control Data Corp ............................................................. 18, 19
   E H Brown Advertising Agency Inc
Copley Press/CELO .............................................................. 303
   McCann-Erickson Inc
CSP ......................................... 26
   Amsterdam Advertising
Cubit .................................................................................. 273
Cybernetic Micro Systems ................................................ 304
Dataram Corp ..................................................................... 5, 16
   Louis Zimmer Communications Inc
Data Systems Design ......................................................... 211
   Tyce • Fultz • Bellack
Data Translation ............................................................... 292
   Quinn & Johnson/BBDO Inc
Del-Tron Precision ............................................................ 308
   Technell Inc
Develcon Electronics ......................................................... 177
   Robert H. Fuller Advertising
Dialight Corp ..................................................................... 245
   Greenstone & Rabasca Advertising Inc
Digi-Data Corp .................................................................. 96
   Business Marketing Inc
Distributed Computer Systems ............................................. 181
   Media Concepts Corp
Distributed Logic Corp ....................................................... 266
   Ron Jenner & Co.
Diversified Technology ..................................................... 304
   Electronic Solutions
   Bowen and Associates, Inc
Elite Corp ........................................................................ 93
   Dana Graphics
Emulex Corp ....................................................................... 219
   Jansen Associates Inc
Emulex Micro/LAN Systems ............................................... 114, 115
   Jansen Associates Inc
Emulogic ........................................................................... 238, 239
   Giardini/Russell Inc
Engineering Specialties ....................................................... 303
   Darryl Lloyd Advertising
Epson America ................................................................. 97
   Darryl Lloyd Advertising
Equiptop Electronics Corp .................................................. 308
   Tom Morris Inc
Exar Integrated Systems ..................................................... 66, 67
   Stephen Grossman Advertising
John Fluke Mfg Co Inc ....................................................... 165, 247
   Forward Technology
   Cencom
   Fujitsu America ....................................................... 50, 51
   Shaffer/MacGill & Associates, Inc
   Fujitsu America ....................................................... 144
   Ebey, Utley, van Bronkhorst

COMPUTER DESIGN/February 1984.
High Performance Multibus® Modularity

MPA-2000 CPU/Intelligent I/O Controller
- STANDARD MULTIBUS INTERFACE
  - Multimaster
  - Single cardslot height (even with plug-in modules)
- UNIQUE MetaPaket™ ARCHITECTURE
  - High speed hardware/firmware technique allows message transfer between intelligent devices
- SOFTWARE AVAILABLE

- ON-BOARD 8 MHz. iAPX-186 CPU WITH:
  - Full 16M address capability
  - 64K EPROM
  - 128K RAM with parity (64K can be dual-ported)
  - i80130 OSF (iRMX-86* kernel)
- EIGHT PROGRAMMABLE DMA CHANNELS
- LOW PROFILE PLUG-IN MODULES
  - Field interchangeable
  - Modules for Serial I/O, Disk, Parallel I/O, LAN
  - Serviced by DMA channels
  - Can be configured as iSBX* module sites

CIRCLE 153
Low Cost Subminiature Ball Slides

LOW FRICTION, LOW INERTIA, PRECISION BALL SLIDES—preloaded to eliminate backlash and side play in head carriages and other reciprocating mechanisms in disk drives, printers, plotters, and copiers.

Hardened stainless steel balls roll on hardened way rods for long life without added lubrication. Anodized aluminum bodies ground top and bottom. Stackable for XY positioning. Custom and special designs available.

Sizes start .23" high x .38" wide x .50" travel, capacity ½ lb. Linear accuracy .0005 inch/inch. Repeatability .0002 inch.

COMPARE OUR PRICES—Popular sizes in stock. Call (203) 775-4041 for 12 page catalog and price list, or see us in THOMCAT.

De-Trol Precision, Inc.
934 Federal Road Route 7
Brookfield, CT 06804
(203) 775-4041

CIRCLE 154

QUIPTRON

COMPUTER FURNITURE
for the electronic office

QUIPTRON is a totally new line of ergonomically-designed modular computer furniture. The new QUIPTRON line offers perhaps the largest selection of sizes available. Included are work stations with electronic compartments featuring E.I.A. hole spacing, CRT terminal stands, universal printer stands, pedestal and angular work stations. All are available in 8 standard colors and unlimited special colors.

Static control systems to solve static discharge problems are offered for the entire product line. Included are conductive floor and table mats, grounding kits, and operator heel and wrist straps.

Call or write us for a colorful new folder describing QUIPTRON MODULAR WORK STATIONS.

QUIPTRON MODULAR WORK STATIONS

AD INDEX

Fujitsu America ................................................................. 68, 69
Peter Wong & Associates

Gandall Data .......................................................................... 195

General Cable Co. ............................................................... 57

General Digital Corp. .......................................................... 304
Standish Associates

Genicom .................................................................................. 146

Cabeil Eanes Advertising

Genisco Computers ............................................................. 183

B.J. Johnson & Associates Inc

Gould ..................................................................................... 100, 101

Tucker * Fultz + Bellack

GTCS Corp ............................................................................... 107

Business Marketing Inc

Heurikon Corp ......................................................................... 276

Gutzman McFee McLaughlin & May

Hewlett Packard ...................................................................... 125, 224-227*
Tallant/Yates Advertising Inc

Hewlett Packard ...................................................................... 172, 173

Wilton, Coombs & Colnett, Inc Advertising

Hitachi America Ltd ............................................................... 10

Cooper-Cameron Inc

Hitachi America Ltd ............................................................... 240, 241

The Creative Consortium Ltd

Hughes Aircraft Co .............................................................. 281

Bernard Hodes Advertising

Hunter & Ready ........................................................................ 48

Doug Gotthoffer & Co

Ikegami .................................................................................. 285

Jerman Spitzer & Felix

Imaging Technology .............................................................. 197

Cooper/GK

IMC Magnetics Corp ............................................................. 271

Foray Advertising

Inmos ...................................................................................... 72

Tallant/Yates Advertising Inc

Intel .......................................................................................... 142, 143, 200, 201, 261

Chiat/Day/Hoefer Inc Advertising

Iomega Corp ........................................................................... 242

Ofield & Brower

ITT/Cannon Electric ............................................................. 91

Abert, Newhoff & Burr Inc

Kennedy Co ............................................................................. 1

R L Thompson Advertising

Key Tronic ................................................................................ 269

EJtene Co

Kontron Electronics ............................................................... 81

Labtek ..................................................................................... 304

Lear Siegler ............................................................................. 228, 229

Leasametric ........................................................................... 127

Doyle Dane Bernbach/S.F.

Liberty Electronics ............................................................... 301

Lincoln Computer Products .......................... 303

The Torrey Group

Marinco Computer Products ............................................. 151

Rossin Greenberg Seronick & Hill Inc

308 COMPUTER DESIGN/February 1984 CIRCLE 155
Memory Protection was Never Easier.

Now you can permanently solder MPD's new coin or horizontal battery holder right on your PC board. Standard 3 volt lithium cells for reliable memory back-up systems clip right in...

- Sturdy, high-temp UL94V-O Valox® material
- Stainless steel nickel plated contacts
- Easy insertion and removal of batteries
- Efficient, economical
- Custom battery holders available on request.

For all the details, call or write today.

CIRCLE 156

RS 232 TO CURRENT LOOP CONVERTER

- DC TO 9600 BAUD
- 20ma/60ma OPERATION
- TELETYPewriter COMPATIBLE
- FULL/HALF DUPLEX
- MODEL 64—HOST POWERED—$80
- MODEL 65—SELF POWERED—$100
- FULLY PROGRAMMABLE

Teylebyte Technology, Inc.
148 New York Avenue
Halesite, NY 11743
(516) 423-3232
In 1955, the artificial heart valve was just an idea. This year, it saved my life.

For over 30 years, The American Heart Association has invested research money in ideas. Lifesaving ideas like the artificial heart valve, cardiopulmonary resuscitation and drugs to control high blood pressure. Today, these ideas save lives.

Despite this progress, one of every two American deaths is caused by diseases of the heart and blood vessels.

If today's ideas are to grow into the lifesaving techniques of tomorrow, the American Heart Association needs your support now.

American Heart Association, We're Fighting for Your Life.
Multiwire permits greater component densities with fewer signal levels. Using polyimide-insulated wire to form interconnections, Multiwire boards accommodate component densities of 2.0 IC's per in² and greater.

Multiwire delivers better electrical performance. Our boards outperform multilayer in all applications requiring tight-tolerance controlled transmission lines.

Multiwire shortens the design cycle by weeks. We can design your board from as little input as a schematic or net list, reducing your in-house design time. And when you make revisions, you'll get new boards back in days instead of weeks.

Revising Multiwire designs costs thousands less. Instead of redrawing costly artmasters, we just key the change into our computer.

Introducing our Advanced Manufacturing Group. Multiwire technology provides the most advanced circuit boards. But sometimes even our leading edge designs are not enough for your requirements. That's why Multiwire has established the Advanced Manufacturing Group—a new facility with design and manufacturing specialists dedicated to solving the interconnection problems for your next generation of products. To learn more, just fill out and return the coupon.
DATACHECK II
THE ULTIMATE BREAKOUT BOX

We call it the ultimate breakout box because of all the features we pack into this pocket-size unit. Count them. 23 major features...all in an easy-to-use, reliable package. No wonder Datacheck II is the ultimate breakout box.

EASY TO USE
• Top to bottom functional panel layout.
• 25 individually numbered breakout switches.
• Four-state indication on all key signals (mark, space, clocking, undefined).
• LED’s separated by signal source (DTE and DCE sides).
• Pocket-size, illustrated operators manual.
• 24-page instructional application notes.

RELIABLE
• Power off/reset button (conserves battery life).
• Molded ABS plastic case with metal hinge for durability.
• Two 9 volt batteries.
• Separate compartment for cable and jumpers.
• Gold-plated recessed pins.

ADDED FUNCTION
• Polycarbonate face (lettering can’t wear off).
• Recessed LED’s.

• Detachable RS-232C ribbon cable (connection flexibility).
• Two-way and three-way jumper cables.
• Independent mark and space source pins.
• Dual tristate monitors for secondary signals.
• Power ON/OFF switch for extended interface reconfiguration.
• Dual pulse trap circuits (isolate intermittent signals).
• Optional Baud Rate Counter (measure transmission frequency).
• Optional Voice Frequency Monitor (listen to the condition of the phone line).
• Optional rechargeable batteries.
• Optional metal case.

ONLY $239.
NAVTEL
FOR THE TESTING TIMES

TELEPHONE (416) 669-9918

A division of Atelco
Every year, Computer Design's 90,000 subscribers fill in the most detailed qualification form required by any magazine in the world. Why? Because this form tells us who you are, where you are, what your functions are, what your company does and what you do. It tells us the kinds of projects you are working on, the kind of products you deal with, and where they are used. It becomes the starting point in planning our editorial program.

The information you provide helps us to select the kinds of features, special reports and surveys that will be of immediate, practical use to designers of computer based systems.

The other side of the coin is the value advertisers place on circulation as a major criterion in media selection. As everyone knows, the more advertising pages we carry, the more editorial pages we can provide to you without cost. The bottom line is a better magazine that can speak your special kind of technical language, page after page, issue after issue.
C-Grid: the Molex .100" x .100" PCB interconnection system.

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

The C-Grid system achieves its high density capability by using .025" (0.64mm) square pins for the male connector parts, set in a .100" x .100" (2.54 x 2.54mm) matrix. The pins can either be placed directly in the board or used in volume with wafer bodies.

To load loose pins into the PC board, Molex offers a patented single- or Multi-Pinsetter® capable of up to 156,000 insertions per hour — the fastest on the market.

Shrouded and unshrouded headers are available in straight and right-angle wafer bodies.

First in Customer Service ... Worldwide

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

The C-Grid system achieves its high density capability by using .025" (0.64mm) square pins for the male connector parts, set in a .100" x .100" (2.54 x 2.54mm) matrix. The pins can either be placed directly in the board or used in volume with wafer bodies.

To load loose pins into the PC board, Molex offers a patented single- or Multi-Pinsetter® capable of up to 156,000 insertions per hour — the fastest on the market.

Shrouded and unshrouded headers are available in straight and right-angle wafer bodies.

First in Customer Service ... Worldwide

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

The C-Grid system achieves its high density capability by using .025" (0.64mm) square pins for the male connector parts, set in a .100" x .100" (2.54 x 2.54mm) matrix. The pins can either be placed directly in the board or used in volume with wafer bodies.

To load loose pins into the PC board, Molex offers a patented single- or Multi-Pinsetter® capable of up to 156,000 insertions per hour — the fastest on the market.

Shrouded and unshrouded headers are available in straight and right-angle wafer bodies.

First in Customer Service ... Worldwide

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.

C-Grid is the most advanced high density interconnection system Molex has ever designed for board-to-board, wire-to-board and wire-to-wire applications. It features selective plating, for the highest performance at the lowest cost, and offers you a wide variety of companion products for convenient design flexibility and reliability.
The fastest...the largest memories... the easiest to program...

MARS-432 Array Processor
Speed
A high-speed programmable arithmetic processor used as a peripheral to a general purpose computer.

The state of the art in 32-bit floating point array processors. Direct addressability of up to 16 million words (64 megabytes) of data memory and direct access to the high-speed internal data bus assure the user of highest throughput rates.

MARS-432 Array Processor Features Include:
- Add and multiply times of 100ns
- Computational power of 30 megaflops
- Computes a 1024-point complex FFT in 1.7ms
- DMA transfers at I/O bus rates of 20 megabytes/sec
- Data memory read or write in 100 ns
- Memory paging for uninterrupted processing during I/O transactions

MARS-432 Array Processor
Memories
Program and data memories compatible with programs written for today's array processor applications.

Program Memory
Virtual and physical address space of 4K words - standard. Expanded configuration uses a 4K cache memory to extend total memory to 64K words.

Data Memory
Data I/O is supported by DMA transfers into data memory with a physical address space of 16 million words. A data memory page-loading feature provides the option of zero overhead background loading of data during time critical program execution. No DMA cycle stealing overhead is incurred. Uninterrupted processing can occur simultaneously with high-speed I/O transfers.

MARS-432 Array Processor
Software
An architecture specifically designed to support a FORTRAN compiler and other software development tools.

FORTRAN Development System (FDS)
FORTRAN compiler, linker, and trace/monitor provide high-level language access to the MARS-432.

Microcode Development System
Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

AP Run Time Executive Support Package (AREX)
As the interface to the MARS-432 at run time, AREX provides processor initialization, I/O operations, and array function execution.

Applications Libraries
Extensive applications libraries include math, signal processing, and image processing.

NUMERIX
For additional information on the MARS family of high-speed Array Processors, write or call: Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500 TELEX 948032

CIRCLE 163
Network Designers—
Introducing the simplicity
of a Remote Procedure Call
...ACCES XNS.

ACCES XNS is ACC's networking protocol package ready for use on
popular minicomputers and workstations. It links applications and system
level programs to data files and processing services in your distributed
computer environment...through simple Remote Procedure Calls.

The ACCES XNS Protocol Package adheres to Xerox protocol standards:
Courier, SPP, and IDP—making it compatible with other standard products,
present and future.

Whether you are responsible for designing a communication environ­
ment around your company's product line, or interconnecting your
company's computer resources, ACCES XNS meets your network design
requirements.

To learn more about ACCES XNS, Courier, and
Remote Procedure Calls, phone ACC at (805) 963-9431
and we'll gladly send you the ACCES XNS Brochure.

We Make Advanced Computers Communicate.