Brings a new dimension to Unibus efficiency for $1983.

Tape Dimension III is the only buffered tri-density (GCR/PE/NRZI) TS-11™-emulating controller on the market. The combination of its unique asynchronous handshake design and 64K byte buffer enables it to take full advantage of bus speeds without the risk of causing data late conditions in other bus transfer operations. It makes Tape Dimension III particularly adaptable to systems with high speed disk drives.

And more. The 64K byte buffer provides total immunity to data late conditions, even at high-speed data rates on a highly populated peripheral bus. In fact, Tape Dimension III actually has greater capability than the TS-11!

Tape Dimension III is completely software-transparent to the VAX™ and PDP-11™ Unibus environment including diagnostics in VMS.

The Tape Dimension III controller supports up to four dual density (Pertec compatible) drives or four tri-density (STC or TELEX type) drives. It is a single embedded hex PC board that fits into any standard SPC slot.

This new dimension in tape transfer dramatically reduces the ratio of protocol to information data. And dramatically increases the efficiency of Unibus utilization. Find out how much it can improve your system throughput. Call or write today for complete information and the name of your nearest distributor (limited quantities) or regional sales representative (OEM quantities).
You've concluded that you need the performance and capacity that only an 8 inch Winchester drive can provide. Which one should you buy? There are 109 different models available. Of this 109, only 39 are 8 inch floppy form-factor compatible. 28 of these 109 perform an average seek in 30 milliseconds or less. And of this 109, only 17 offer true SMD compatibility.

Puzzled?

Only one company provides a disk drive with all the features — Kennedy and Model 7300

with the right size, the right interfaces and the right price.

Write or give us a call.

KENNEDY
An Allegheny International Company
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TELEX 472-0116 KENNEDY
TWX 910-586-3249

SPECIFICATIONS:
  • 41 and 82 MB Capacities
  • Rotary Voice Coil 30 msec average seek
  • SMD, ANSI or PICO BUS
  • Interfaces
  • 1209 KByte/sec transfer rate
  • Available 30-45 days ARO
  • Q100: $2,560/$3,195

KENNEDY • QUALITY • COUNT ON IT
CIRCLE 2
At 660 MHz, Tektronix' Color DAS is the fastest logic analyzer ever.

660 MHz.
A fleeting 1.5 ns between sample intervals. No other logic analyzer even comes close.
Transform glitches from ghosts into definable, displayed data. Resolve individual byte transfers on a mainframe data bus. Whatever your application, the Color DAS's new 91A04 Data Acquisition Card redefines the meaning of high-speed logic measurement.
Want to correlate superfast hardware events with their software counterparts? Simply team the 91A04 card up with other Color DAS cards targeted at software acquisition. Through the instrument's patented "arms mode", you get a totally time-aligned picture of concurrently acquired hardware and software events.
It's all part of the power you'll find only in Tektronix' Color DAS, which also includes the industry's first color-coded display, data widths to 104 channels, pattern generation and microprocessor software design support.
Put 660 MHz to work today.
Contact your nearest Tek Sales engineer or write us for more information.

Tektronix
COMMITTED TO EXCELLENCE

Copyright © 1983, Tektronix, Inc. All rights reserved. LAA-378

Circle 3 for Literature
Circle 4 for Sales Contact
Memories from the last (?) Anaheim NCC

Attendance at NCC '83, whether or not it met the predicted 120,000 to 130,000 figures, was notably heavy—in most of the exhibit areas. Although temperatures in the Pavilion (better known as "The Tent") were said to have reached nearly 115 °F, exhibitors in other areas of the Convention Center and at the Disneyland Hotel found crowds of people to view their products. However, because of the problems with exhibit facilities and local hotel space, reports indicate that in future years NCC will alternate between Las Vegas and Chicago, beginning in 1984 in Las Vegas. Those cities are considered to be the only ones with adequate space for this conference.

Notable in the drive (pardon the pun) to offer small disk drives with greater storage capacities was a family of 5¼" minifloppies from Amlyn Corp. For example, the model 1560 drive provides up to 3.3M bytes of unformatted capacity using double-sided recording.

This year, Control Data announced its Cricket 3½" Winchester disk drive, offering 6.38M bytes of unformatted data storage. This drive uses thin film read/write heads (similar to those in the company's larger disk drives) and nickel-cobalt plated recording media. Custom LSI chips handle servo functions and read chain control.

Although not yet incorporated in any manufacturer's available drives, 5¼" diskette media introduced by the Spin Physics unit of Eastman Kodak are said to be capable of storing up to 10M bytes using vertical recording technology. The media use isotropic cobalt-doped magnetic particles (0.2 µm long) to support both vertical and horizontal magnetization.

Weighing less than 11 lb and operating from either a rechargeable built-in battery or ac power, the PC-5000 is Sharp Electronics' introduction to the portable computer market. It can be used either standalone or coupled to a host computer and is based on an 8088 microprocessor. The portable computer contains 128K bytes of RAM (expandable to 256K) as well as 128K bytes of bubble memory storage and 128K bytes of ROM in cartridge.

Scotsman III, introduced by Racal-Vadic, compresses data at a 2 to 1 ratio. It can compress a 192k-bit data stream, transmit it over a 9600-bps line, and reconstruct it back to 19.2k bits. Four 9600 bisync or two full-duplex 9600 lines can be compressed and transmitted over a single line. The unit is compatible with async, bisync, X.25, SDLC, and HDLC protocols.

Multiple communication lines can be connected to one or more VAX, PDP-11, DECsystem 10, and System 20 computers with the Attach system announced by Able Computer. It allows up to 128 terminal lines to be connected via a single composite cable.

A keyboardless color executive terminal was shown by Santa Barbara Development Laboratories at an off-NCC site. This terminal features touch screen data access and voice control of data entry and editing functions. By touching one of several screen images, the user can access information in less than 1 s. Described by the designers as "user transparent," the system can be used for many phases of communications, information presentation, and office automation. Product introduction is scheduled for late this year.

A generic version of the Unix operating system carrying Western Electric's blessing (and certification) will soon be available for use with three popular 16-bit microprocessors. In a mutually beneficial collaborative agreement, Western Electric has entered into "software development arrangements" with Motorola, Intel, and National Semiconductor for the 68000, iAPX 286, and 16032 processors, respectively.
Pretriggers

Distributed processing architecture that promises to optimize performance is based on use of a minicomputer for resource allocation and multiple 16-bit microprocessors for task processing. SyFanet, offered by Computer Automation's Commercial Systems Div, is linked by a broadband network in a proprietary CSMA/CA transmission scheme.

Attributes of both per-line switched PBXs and packet-switched LANs are blended in a distributed communication system from CXC Corp. The Rose system supports from 192 to 50k subscribers with multiple processing nodes and variable bandwidth allocation from 64k to 33M bps.

Integration of data with digitized voice is accomplished by Sydis using a multiprocessor system connected through a LAN. VoiceStation employs several 68000s as application servers, file servers, or voice processors for both switching voice messages over the same system and performing voice digitization and recording. Thus, voice messages can be stored and edited as data files and appended to documents such as word processing files.

Clearer viewing of complex 3-D wireframe images is possible by removing hidden lines and polygon backfaces. In one case, recent software enhancements to the Anvil 4000 mechanical CAD/CAM system from Manufacturing Consultants and Services focus on the mathematical model. In another case, enhancements to the Template graphics software tools from Megatek emphasize image processing. Both efforts have the same visual effect.

A very high resolution color display system that combines liquid crystal and CRT technologies was described by Tektronix engineers at the recent Society for Information Display conference. Color can now be added to displays without degrading resolution, making the system feasible for use on small instruments.

Simultaneous logic design and physical layout are accomplished on a design workstation introduced by Valid Logic. SCALDstar combines monochrome and color CRT displays, with design parameters available to both. When the cursor on the logic diagram is placed at a particular location, the layout display cursor moves to the corresponding circuit elements.

A self-contained 16-bit "mobile" microcomputer that weighs 9 lb and can operate up to 8 h on its rechargeable batteries was shown by Gavilan Computer at the spring Comdex conference. User interface is via an integrated touch panel that moves a pointer on the screen to the file or item desired. Price for a basic system will be under $4000.

Microcomputer interface to major mainframes is accomplished by Tab Products on its System 800 and 1600 desktop computers through combined bisync and async transmission capabilities. This eliminates the need for dumb terminals and frontend controllers.

Ruggedized data and program storage systems for portable, mobile, remote, and difficult environments, introduced by Targa Electronics Systems, are designed around removable bubble memory cartridges. Present cartridges contain 256K bytes, but the company foresees 1M byte in future cartridges.

Computer Design (ISSN-0010-4566) is published monthly, with a thirteenth and fourteenth issue respectively in April and October by PennWell Publishing Company, Advanced Technology Group, 119 Russell Street, Littleton, MA 01460. P. C. Lauinger, Chairman; Philip C. Lauinger, Jr., President; Joseph A. Wolking, Senior Vice President; H. Mason Fackert, Group Vice President. Second-class postage paid at Littleton, MA 01460 and additional mailing offices. COMPUTER DESIGN is distributed without charge to U.S. and W. Europe-based engineers and engineering managers responsible for computer-based equipment and systems design. Subscription rate for others is $50 in U.S.A. and $75 elsewhere. Single copy price is $5.00 in U.S.A. and $7.50 elsewhere. Microfilm copies of COMPUTER DESIGN are available and may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Road, Ann Arbor, Michigan 48106. POSTMASTER: CHANGE OF ADDRESS-FORM 3579 to be sent to COMPUTER DESIGN, Circulation Department, P.O. Box 593, Littleton, MA 01460 (USPS 127-340).

* Computer Design is a registered trademark of Computer Design, a PennWell Publication, 119 Russell Street, Littleton, MA 01460. All rights reserved. No materials may be reprinted without permission. Phone (617) 486-901.
FROM THE LEADER

Look to the leader — Dataram — for your DEC-compatible semiconductor ADD-IN memory. Offering not only the broadest, most complete line of semi ADD-INs, but the most capable...no matter what your yardstick. Compatibility, throughput, cost, power efficiency, size...no matter how you measure capability, Dataram DEC-compatible semi ADD-INs are the clear leader.

A leadership position earned by improving on DEC's price and delivery...and then adding features available from no one else in the industry.

The chart provides a glimpse at the industry-pacesetting family of DEC-compatible semi ADD-INs. Call us today at (609) 799-0071, and we'll give you a close-up look at the products that have made us the leader.

### DEC Mini

<table>
<thead>
<tr>
<th>DEC Mini</th>
<th>Dataram ADD-IN</th>
<th>Board Size</th>
<th>Maximum Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSI-11®</td>
<td>DR-115S</td>
<td>dual</td>
<td>64 KB</td>
</tr>
<tr>
<td>LSI-11</td>
<td>DR-215</td>
<td>dual</td>
<td>256 KB</td>
</tr>
<tr>
<td>LSI-11</td>
<td>DR-213</td>
<td>quad</td>
<td>1.0 MB</td>
</tr>
<tr>
<td>PDP®-11</td>
<td>DR-114S</td>
<td>hex</td>
<td>256 KB</td>
</tr>
<tr>
<td>PDP-11</td>
<td>DR-114SP</td>
<td>hex</td>
<td>256 KB</td>
</tr>
<tr>
<td>PDP-11</td>
<td>DR-214</td>
<td>hex</td>
<td>1.0 MB</td>
</tr>
<tr>
<td>PDP-11</td>
<td>DR-144</td>
<td>hex</td>
<td>256 KB</td>
</tr>
<tr>
<td>PDP-11</td>
<td>DR-244</td>
<td>hex</td>
<td>1.0 MB</td>
</tr>
<tr>
<td>VAX®-11/750</td>
<td>DR-175</td>
<td>hex</td>
<td>256 KB</td>
</tr>
<tr>
<td>PDP-11/70</td>
<td>DR-275</td>
<td>hex</td>
<td>1.0 MB</td>
</tr>
<tr>
<td>VAX-11/750</td>
<td>DR-178</td>
<td>extended hex</td>
<td>512 KB</td>
</tr>
<tr>
<td>VAX-11/730</td>
<td>DR-278</td>
<td>extended hex</td>
<td>2.0 MB</td>
</tr>
<tr>
<td>VAX-11/780</td>
<td>DR-120</td>
<td>extended hex</td>
<td>256 KB</td>
</tr>
<tr>
<td>DECSYSTEM 2020®</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dataram also provides core ADD-INs, core and semiconductor ADD-ONs, memory system units, memory management, and a wide range of memory-related accessories for DEC users.
System technology

28 Software: Programming language adds flexibility for artificial intelligence
34 Computers: Supermini doubles performance
47 Integrated circuits: Advances make CMOS serious VLSI contender
48 Memory systems: QIC no guarantee for compatibility
64 System elements: Components make systems fault tolerant
66 Data communications: Data and voice share wire
70 Microprocessors/microcomputers: Z80 code expands into large systems

System design

91 Control & automation: Managing yields by yielding management to computers
by Ronald D. Barker—Productivity receives a boost when the precepts of modern data processing are applied to information management in the automated factory.

103 Computers: Twelve bits are usually better
by Robert C. Sanford—Processor architectures need not come in multiples of eight. The pluses of 12-bit architectures are many and include streamlined instruction sets and a large memory range.

121 Data conversion: Advanced data acquisition aids the handicapped
by Andrew Davis and Ari Berman—Computer based acquisition and analysis tools are providing pathologists and researchers with insight into the mysteries of the spoken word.

137 Data communications: Generating Huffman codes
by George Grosskopf, Jr—Time and space are saved when alphanumeric data are compressed and represented by these efficient encoding schemes.

SIGGRAPH'83

78 Sophisticated computer graphics and interactive techniques are becoming indispensable in applications ranging from CAD/CAE and robotics to image synthesis and office automation. At its 10th annual conference next month, ACM's Special Interest Group on Computer Graphics will size up the scope of graphics technology today and forecast what is shaping up for tomorrow.
**Special report on semiconductor memories**

New technologies and approaches to memory have surfaced in the last few years. This month's "Design Frontier" report examines some of these developments. The staff report explores the directions being taken by nonvolatile memory development. Two other articles deal with particular memory devices—one with a FIFO buffer and the other with a new EEPROM. Another report deals with a virtual memory management chip.

---

**System components**

<table>
<thead>
<tr>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>199</td>
<td>Integral universal counter/timer upgrades oscilloscope</td>
</tr>
<tr>
<td>200</td>
<td>5½&quot; Winchester packs up to 380M bytes</td>
</tr>
<tr>
<td>200</td>
<td>Color printers integrate text and graphics on plain paper</td>
</tr>
<tr>
<td>202</td>
<td>STD-bus development system matches language to job</td>
</tr>
<tr>
<td>202</td>
<td>LSI based networking microcomputer</td>
</tr>
<tr>
<td>204</td>
<td>Data communications</td>
</tr>
<tr>
<td>211</td>
<td>Memory systems</td>
</tr>
<tr>
<td>212</td>
<td>Interface</td>
</tr>
<tr>
<td>216</td>
<td>Test &amp; measurement</td>
</tr>
<tr>
<td>216</td>
<td>Microprocessors/microcomputers</td>
</tr>
<tr>
<td>220</td>
<td>Development systems</td>
</tr>
<tr>
<td>222</td>
<td>Peripherals</td>
</tr>
<tr>
<td>228</td>
<td>System elements</td>
</tr>
<tr>
<td>230</td>
<td>Integrated circuits</td>
</tr>
<tr>
<td>234</td>
<td>Computers</td>
</tr>
<tr>
<td>234</td>
<td>Software</td>
</tr>
<tr>
<td>236</td>
<td>Control &amp; automation</td>
</tr>
<tr>
<td>236</td>
<td>Interconnection &amp; packaging</td>
</tr>
<tr>
<td>240</td>
<td>Power sources &amp; protection</td>
</tr>
<tr>
<td>242</td>
<td>Data conversion</td>
</tr>
</tbody>
</table>

---

**Departments**

<table>
<thead>
<tr>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Up front</td>
</tr>
<tr>
<td>11</td>
<td>Publisher's perspective</td>
</tr>
<tr>
<td>17</td>
<td>Editorial</td>
</tr>
<tr>
<td>24</td>
<td>Letters to the editor</td>
</tr>
<tr>
<td>244</td>
<td>Calendar</td>
</tr>
<tr>
<td>246</td>
<td>Literature</td>
</tr>
<tr>
<td>252</td>
<td>Advertisers' index</td>
</tr>
<tr>
<td>255</td>
<td>Designer's bookcase</td>
</tr>
<tr>
<td>256</td>
<td>System showcase</td>
</tr>
<tr>
<td>259</td>
<td>Reader inquiry card</td>
</tr>
<tr>
<td>259</td>
<td>Change of address card</td>
</tr>
</tbody>
</table>

---

**Designers' preference survey**

<table>
<thead>
<tr>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>225</td>
<td>Computers, graphics &amp; software</td>
</tr>
</tbody>
</table>

**Editorial reviewers for parts of this issue:**

- Lee Edwards
- G. Perrone
- John Satta
- Arthur Seidman

*Appearing in Domestic issues only*
Precise answers instantly: now waveform measurements are automatic!

Now you can cut from minutes to seconds the time it takes to perform most common waveform measurements. By automatically performing all routine measurement tasks, the Tek 7854 minimizes errors and gives you more time for more productive activity.

Touch a front panel key and the 7854 digitizes repetitive signals up to 400 MHz. Stores them. Measures them. And displays the answer. For any rise time measurement, for example, you need only press two keys—AQR and RISE—to consistently obtain a precise, repeatable answer on-screen. There is no painstaking set-up, no decision-making, no mental calculation required.

Time savings and risk reduction are even more dramatic in more complex tasks, such as calculating the area under a power curve or determining instantaneous power from current and voltage waveforms... both the work of a few seconds on the 7854.

You can develop your own measurement routines using the companion waveform calculator. You can make virtually any sequence of procedures automatic, then leave operation to lesser skilled operators and technicians. You can even connect the 7854 to host computers and mass storage via the standard IEEE-488 interface bus.

More than 30 plug-ins let you reconfigure capabilities at will.

Like all Tek 7000 Series scopes, the 7854 keeps expanding in value. Add high-sensitivity differential amplifiers. Comparators. Counters. Spectrum analyzers. Or sampling plug-ins that let you digitize repetitive signals up to 14 GHz. At any time, you can add new performance at a fraction of the cost of a monolithic instrument.

Allow yourself more time for creative problem-solving. In this era of hand-held calculators, it's about time you let the 7854 begin making your life simpler and your time more productive. Call your Tektronix Sales Engineer today!

For further information, contact:
U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc.
P.O. Box 4828
Portland, OR 97208
For additional literature, or the address and phone number of the Tektronix Sales Office nearest you, contact:
Phone: 800/547-1512
Oregon only: 800/452-1877
Telex: 910-467-8708
TLX: 15-1754
Cable: TEKTRONIX

Europe, Africa, Middle East
Tektronix Europe B.V.
European Headquarters
Postbox 827
1180 AV Amstelveen
The Netherlands
Phone: (20) 471146
Telex: 18312-18328

Canada
Tektronix Canada Inc.
P.O. Box 6500
Barrie, Ontario L4M 4V3
Phone: 705/737-2700

The Answer
By Any Measure

Circle 6 for Literature
Great ideas, plus hard work, business sense and commitment to customer satisfaction. That's what it takes to be a Value Added Remarketer for IBM.

IBM is looking for business people with specialized industry experience. For companies that can successfully merge our systems with applications software. For those to whom quality is fundamental.

Put IBM to work for your customers.

To begin with, IBM wants qualified VARs to have the broadest choice of systems and software: the IBM Personal Computer, Displaywriter, Datamaster, CS-9000, System/36, and Series/1 with its new enhancements.

These products carry IBM's reputation for quality. Equally important, all have access to IBM's nation-wide service.

That means VARs who work with IBM have more to offer their customers. But that's only part of what IBM can offer to its VARs.

Put IBM to work for you.

IBM also provides VARs with tools to assist them in marketing to their customers and prospects.

For instance, IBM helps VARs with business shows and product literature. We help VARs create their own direct mail programs.

And IBM brings prospects with special needs together with VARs who have unique solutions. It's done with a special referencing system which supplies information about our VARs' offerings to IBM's sales-force.

IBM's Value Added Remarketer Program: Great ideas, hard work and business ability are what's required. For more information, call 1 800 IBM-VARS or send in the coupon.

Some of our VARs' best ideas began on the backs of envelopes.
In the increasingly complex computer product marketplace, the need for discriminating magazine editors is growing. Designers and integrators are demanding concentrated editorial coverage of their specialties as well as timely reports on emerging technologies and applications.

Few technical publications can continue to do the job effectively without improving their editorial staffs' technical expertise. New sister publications such as *Telecommunication Products + Technology*, coupled with extra issues of *Computer Design* on automation & control and office system design, underscore the need to continuously upgrade and expand our staff. Our stringent hiring requirements ensure that you will be served by editors of the highest caliber. To meet your system design needs, *Computer Design* has always been written by designers and integrators for designers and integrators.

That is why, at this time, we are very pleased to introduce a new senior editor who has been in the trenches with you. Nicolas Mokhoff, both design engineer and accomplished writer, is heading up our new field office in New York City. From there, he will be in constant contact with companies in the North Atlantic states and through the Southeast into the Midwest. Joining Nicolas on our editorial staff is another engineering graduate, Malinda Banash. Malinda is a member of the IEEE Computer Society and the Society of Women Engineers. As assistant editor, she will be responsible for technical support of the editorial staff here in Littleton.

We are also very pleased to announce that two fine journalists who carry impressive publishing credentials are joining the copy-editing staff. Leslie Ann Wheeler and Lauren A. Stickler will assume the important task of maintaining the standards and editorial quality of our magazine.

Good people...people who share your interests...are playing an important role in keeping you up to date with all the advances within the computer based system design market. If you get a chance, drop them a line or call them with some important industry news or applications.
Finally, a single source for multi-processor designed for OEMs and systems integrators. Now that's intelligent.

Intelligent Systems introduces the Datavue multi-processor, multi-user computer system.

The Datavue system offers OEMs and system integrators a powerful solution for multi-user, multi-tasking, terminal-based environments—and all the advantages of single-sourcing.

With Datavue you configure just the right amount of computer power for current needs and deliver to your customers a simple, economical growth path from one to eight users. **Advanced systems architecture delivers stand-alone performance.** For advanced applications—decision support systems, office automation, management productivity, and even process control—Datavue provides a simple computing environment with a dedicated computer for each user (or control application). Up to eight computer cards can be inserted in the Datavue system which resource shares mass storage and common I/O. Each user gets a full microcomputer with a Z80A, 64Kb RAM, and CP/M* 2.2. As a result, all users get stand-alone performance with the economies of a multi-user shared resource system.

Intecolor 2405

Add intelligent terminals to meet your customers' needs. Since 1973, Intelligent Systems has been a world leader in designing and manufacturing color graphics terminals. Now, you can profit from our expertise with: The Intecolor 2405, the indus-
multi-user computer systems

Advanced architecture gives each user a microcomputer card with a Z80A and 64Kb RAM, and lets you add up to eight terminals.

In addition, you can add users for only $450 each. Consequently, you can deliver precisely the computing power your applications need.

**Datavue’s unique single-user home system is fully compatible and only $1995!** To supplement your sales of Datavue’s multi-user systems, you can offer a single-user home system that can be used as a stand-alone or with a modem to communicate with the base system.

The home system includes a Z80A, 64Kb RAM, 1 Mb floppy, two RS232-C ports and CP/M 2.2. And it’s very competitive—in function and price—with personal computers.

**Put it all together with Datavue.** Stand-alone performance. Up to eight users. Price and profitable margins. Powerful options, from synchronous communications to 80Mb mass storage, and more. Color, graphics, and wide-screen terminals (or use your own). A huge library of off-the-shelf CP/M 2.2 software. Plus, the unmatched advantages of single-sourcing.

That’s Datavue multi-processor, multi-user systems. That’s Intelligent Systems.

**More Information.** Datavue is shipping now. OEM contract discounts are available. And a limited number of dealerships are open. For details, contact Marketing Communications at 404/449-5961, TWX 810 1581.
**DISK SYSTEMS**

- **$ SPECIAL • LOW PRICES • SPECIAL$**

**Cl-1240-WF**
42 megabyte Winchester disk system with controller, 42 megabytes fixed and 2 megabytes floppy backup. $6995.00

**Cl-1220-TF**
Dual drive, double density, double sided, 2MB capacity floppy, plus DMA LSI 11 controller, occupying 3½" of vertical space. $2695.00

**Cl-520**
10MB 5½" Winchester with 2MB 5½" floppy, RX02/R02 or RX50/WD50 emulation. $3995.00

**DON'T ASK WHY WE CHARGE SO LITTLE, ASK WHY THEY CHARGE SO MUCH.**

**Chrislin Industries, Inc.**
31352 Via Colinas • Westlake Village, CA 91362 • 213-991-2254
TWX 910-4134-1253 (CHRISLIN WKVG)

LSI 11 is a trademark of Digital Equipment Corporation.

**CIRCLE 30**

---

**More Room ... More Multibus Cages.**

**More Room**
You get more room for extra cards without increasing overall size, because our design gives you greater inside dimensions.

**More Reliability**
All cages are constructed of sturdy, durable anodized aluminum with a single mother board backplane ... a concept that increases reliability and minimizes interconnections.

**More Models**
We have more models than all our competitors combined. Choose a cage with 3, 4, 5, 6, 7, 8, 9, 12, 14, 15, 16, 20, 24 or 26 slots for the right solution to your problem. We have models with either 0.6" or 0.75" card centers and can even accommodate wirewrap cards.

**More Rack Mount Models**
Standard 19-inch rack mounting available for all cages.

**More Warranty**
A three year warranty is your assurance of quality.

**For Fast Delivery.**
Call our toll free number (800) 854-7086
In Calif. call (619) 292-0242
In Canada Call: Transduction Ltd. (416) 625-1907

---

**Electronic Solutions**
5780 Chesapeake Court
San Diego, CA 92123

**MULTI-CAGE®**
Fully Multibus Compatible, Terminated Mother Board.

---

**COMPUTER DESIGN**

PennWell Publishing Company
Advanced Technology Group
119 Russell Street, Littleton, MA 01460
Tel: 617/486-9501

- **Editor in Chief**, Saul B. Dinman
- **Executive Editor**, Michael Elphick
- **Managing Editor**, Sydney F. Shapiro
- **Technical Editor**, Chris Brown
- **Senior Editor**, Peg Killmon
- **Associate Editor**, Deb Hightberger
- **Assistant Editor**, Malinda E. Banash
- **Senior Copy Editor**, Suki Adams
- **Copy Editors**, Jocelyn J. Melanson, Leslie Ann Wheeler
- **Asst Copy Editors**, Lauren A. Stickler

**New York Field Office**
- **Senior Editor**, Nicolas Mokhoff
- 230 Park Ave, Suite 907, New York, NY 10169, Tel: 212/986-4310

**Western Field Offices**
- **Managing Editor**, Tom Williams
- **Field Editor**, Sam Bassett
- 540 Weddell Dr, Suite 8, Sunnyvale, CA 94089, Tel: 408/745-0715
- **Field Editor**, Joseph A. Aseo
- 5199 E Pacific Coast Highway, Suite 303A, Long Beach, CA 90815, Tel: 213/597-6894

**Production Manager**, Linda M. Wright
**Assistant Production Manager**, Lou Ann Morin
**Production Assistant**, Philip Korn
**Design Consultant**, Ken Silvia
**Technical Art**, Designline

**Publisher**, Ronald W. Evans

**Director of Marketing**, Gene Pritchard
**Promotion Director**, Steve Fedor
**Marketing Services/PR Mgr**, Linda G. Clark
**Advertising Coordinators**, Cherie LaFrance, Sally H. Bowers
**Circulation Director**, Robert P. Dromgoole
**Controller**, David C. Ciommo
**Computer System Manager**, Ken Spiewak
**Data Services Manager**, Wanda Holt
**Data Services Assistant**, Sue Bowker

**Chairman of the Board**, P.C. Lauinger
**President**, Philip C. Lauinger, Jr.
**Senior Vice President**, Joseph A. Wolking
**Group Vice President**, H. Mason Fackert
**Group Vice President**, Carl J. Lawrence
**Vice President/Finance**, V. John Maney
**Vice President**, L. John Ford
Dollar for dollar you get less for your money with our 32-bit board sets.

We've hit two new lows with our QUADRABYTE™ price and profile. And in this case, less means more. It means more flexibility. More reliability. More value-added potential for the OEM.

Priced at under $13,000 in quantities of 100, QUADRABYTE has a remarkably small profile. Yet, it gives you all the throughput, modularity, expandability and performance you could want, and a variety of options. This lowest-priced, true 32-bit board set package provides maximized profits for you.

QUADRABYTE comes from the field-proven, powerful Gould CONCEPT/32™ family of superminicomputers. With the MPX-QB real-time operating system, applications are handled faster while supporting a larger variety of languages and software tools to simplify programming. And, you get the additional advantage of immediate delivery.

The scope of the board set product line allows total flexibility in your design process. Our products range from a basic 32-bit board set nucleus to packaged configurations with field-proven options. Buy just what you need for your specific application.

Gould has a commitment to building the best board level computer with off-the-shelf delivery at the lowest price. Why should you settle for less? See how we measure up.

Call or write Gould S.E.L. Computer Systems Inc. de Puerto Rico, 1224 North University Drive, Plantation, Florida 33322. 1-800-323-0320.
MPC Puts the Big Picture in Graphic Detail

**DEC™ VT Plug Compatible**

Today's price competitive alternative for ANSI 3.64 video display terminals, the MPC 1250 uses an enlarged 14" screen and sophisticated bit map graphics to fully emulate the DEC™ VT/125. For smart alphanumeric editing, the MPC 1200 emulates full functionality of the DEC™ VT/131-VT/132 Series. The 1250 accepts all REGIS™ operating system software.

Not only does the 1200/1250 Series deliver superior emulation of the DEC VT models, but they offer the extras you've been looking for ... like an ergonomic design with video and screen enhancements. Any way you view it, the heavily featured MPC 1200/1250 Series gives you the DEC™ VT alternatives worth looking into!

**Available Now!!!**

Why wait through long factory lead times? Your local MPC distributor can deliver your MPC 1200/1250 DEC™ VT plug compatibles, loaded with extras, from stock today.

A worldwide distribution network provides sales and service for the MPC family of sophisticated CRT terminals. Call (703) 430-1800 for the name of your nearest distributor.

**You’ll See Built-in Extras at no Extra Cost!**

MPC's 1200/1250 Series brings you the costly options of other terminals as standard features. Take a closer look at the extras in MPC's new generation of engineering excellence:

- **Superior Monochrome Graphics.** Color Optional; 1250 Model
- **640 x 480 Readable bit map**
- **24 Programmable Function Keys,** plus programmable numeric keypad, store up to 36 individual function sequences in NVR.
- **Eight pages of Video Memory**
- **Double High, Double Wide Character Capability**
- **40, 80 or 132 Columns,** user selectable
- **Flexible Split Screens**
- **Enhanced Scrolling: Jump, smooth, and bi-directional**
- **Selectable Video Attributes** and adjustable brightness controlled from keyboard
- **Two RS-232 Ports**—bidirectional and independently controlled
- **14" Non-Glare Screen**
- **Detachable Keyboard meets European DIN specs.**
- **Soft Set-Up Plus Host Configurable**
- **UL Listed, FCC & CSA Approved**

**Contact Your Nearest MPC Distributor**

- **Kierulf Electronics:** Call your Kierulf Division. (outside Calif. 800-338-8811)
- **Computer Peripherals,** Richardson, TX (214) 644-3606
- **Digital Solutions,** Marietta, GA (404) 955-4488
- **Dayton-Forrester Associates,** Canoga Park, CA (213) 701-0127
- **Procom Sales,** Elk Grove, IL (312) 860-1028
- **The Tricom Group,** Hicksville, NY (516) 681-2222
- **Mid-Com Communications Inc.,** Southfield, MI (313) 353-5696
- **Computer Dataco, Kansas City, MO (816) 221-1212**
- **Peripheral Business Systems, Kirkland, WA (206) 823-6661**
- **Peripheral Equipment,** Pleasant Grove, UT (801) 785-5009
- **Dynamic Systems North West,** Mukilteo, WA (206) 745-5311
- **RC Data,** San Jose, CA (408) 946-3800
- **Trans Alaska Data Systems,** Anchorage, AK (907) 561-1776
- **Andor Systems,** Ontario, Canada (416) 746-2775

**a division of C3 Inc.**

Micro Products Company
Rte 634 & Acacia Lane
Post Office Box 198
Sterling, Virginia 22770
Tel.: (703) 430-1800

C3 Inc.
Kingewick House
Summinghill, Berkshire
England SL578J
Tel.: (851) 848980
Ph: Asset (C990) 23491

CIRCLE 13
RALLY 'ROUND THE ECONOMY

Some 18 months ago, the Reagan Administration initiated Project Exodus to stem the flow of American technology into the Soviet Union. This project, and its attendant Controlled Commodities List (CCL) that the U.S. Department of Defense maintains as a classified document, has been a thorn in the side of many high tech manufacturers. Not only are the CCL's contents unavailable to the average industrial or commercial system manufacturer, but the enforcement of Project Exodus—dependent upon the interpretations of as many as five separate government agencies—has proven to be capricious at best.

Most of our industrial and commercial computer system manufacturers rely on exporting 30% to 50% of their business to Europe. As the United States climbs out of the recession, Europe will not be far behind, requiring more U.S. exports. This export business will be vital to the next U.S. boom period. However, Project Exodus has the potential to seriously hamper this plan, and even to finish off some of the smaller recession-starved companies eagerly awaiting the coming boom.

Originally, Project Exodus was implemented as a panic measure and is valid only through the summer; it will come up for renewal in the fall. Since its inception, there has been vigorous debate between high tech "have" and "have not" states. The high tech state legislators have argued with Congress to clean up the bill's provisions; they have also spent a great deal of time helping some of the smaller manufacturers fight the bill's fluctuating provisions regarding company exports. Legislators from non-high tech states have argued that though the Soviet Bloc is behind us for the moment, we should not indirectly provide them with our technology through some of our European trading partners who do not object to doing business with the Soviets. These same legislators, however, argue that the Soviets are now technologically ahead of us and that, in order to catch up, we must again embark on a technological spending binge like we did in the Sputnik days. A question that defies logic is, If the Secrecy Act's provisions prevent most manufacturers from finding out the CCL's contents, why don't they also prevent truly classified technology from leaving this country?

As the debate over Project Exodus' renewal warms up—it is already becoming hot in many of the high tech states—it would behoove all of us to make our voices heard by our congressional representatives. We should demand at least sensible provisions for the enforcement of such a bill, if not seek defeating the measure on the grounds that normal secrecy provisions should be sufficient to protect us from technology leaks. If our voices are not heard, the fallout predicted because of overcrowding in the marketplace may just come sooner than we expected—and for an entirely different reason.

Saul B. Dinman
Editor in Chief

A reminder to those of you who have not responded to the readership study in Computer Design's Automation & Control Premier Edition: please turn to p 174 of that issue, answer the questions on the Reader Inquiry Card on p 181, and get it back to us. We need your valuable feedback to help us plan next year's editorial calendar. Thank you.

Best Technical Article of the Month—November
"Understanding the High Speed Digital Logic Signal!"
Malcolm Davidson, Heaviside Industries, Ltd

This article will now compete with other monthly winning articles for the 1982 editorial excellence award.
Well, Motorola's still trying to get the 68000 System together. Unfortunately, it's not only too late. It's too slow.

THE 68000 WAS FAST.
BUT THE iAPX286 IS A WHOLE LOT FASTER.

The new 286 is three times faster than the 68000. Even our extremely cost-effective 186, which integrates 20 LSI devices into one chip, outperforms it. (Sorry, Motorola.)

And you can forget what Motorola's been saying about memory. The 286 not only addresses 16 Megabytes of physical memory, it addresses 1 Gigabyte per user of virtual memory.

Unlike the 68000, the 286 even has the memory management, the protection, and the operating system interface functions built on to the chip itself. So you get software protection and software-in-silicon with no external components to drain the juice out of your CPU.

But there's a lot more to the iAPX86 family than performance.

© 1983 "Partnerchip" is a trademark of Advanced Micro Devices, Inc.
THE WORLD'S FIRST PARTNERCHIP.

The Partnership gives you two responsible domestic sources:

Intel and Advanced Micro Devices.

(Motorola has their second sources spread out from here to Tokyo. Not one comes close to offering you the entire product line.)

Together, we have more peripherals on the shelf than any other 16-bit family. And since we've signed an agreement to exchange parts, masks and R&D, we'll be delivering a lot more than promises over the next 10 years.

So if you want the system that'll keep you way out in front, climb aboard the Partnership.

It's a lot better than what Motorola's peddling.

The iAPX86 People.

Advanced Micro Devices
901 Thompson Place, Sunnyvale, CA 94086 • (408) 732-2400
SHUGART DRIVES.

1/2 OFF.
No, it's not a sale. It's just a way of telling the world that Shugart now has a whole line of half-height floppy disk drives. Half of which are our new 5.25" Mini-floppies. Or, if you will, mini Minifloppies. The SA455/465 double-sided drives. Both offer improved performance and reliability over conventional minis. And more design flexibility, because of a technology that demands only half as much space.

So you can create smaller, more competitive systems. Or build more storage capacity into existing designs by putting two drives in the space of one. Moreover, both the 48tpi SA455 and 96tpi SA465 are compatible with their relatives, the industry standard SA400/405 and SA410/460. So there's no need for a major revamping of hardware or software.

And once they're in place, you'll find they use 45% less power than ordinary 5.25" drives. While delivering snappier access times (in the case of the SA465, 3 msec track-to-track). And even better reliability—an impressive 10,000-hour MTBF. A 25% improvement over most full-height drives.

Then there's the other half of the story. Our new 8" half-heights, the SA810 singlesided and SA860 double-sided floppies. They too give you more performance and reliability out of a lot less hardware. They too eliminate major redesign. Since the controller interface, mounting holes and internationally recognized DC power supply requirements are fully compatible with the industry standard SA801 and SA851 8" drives.

The SA810/860 are also the only half-heights offering true electrical compatibility with the existing user base of over 4 million 8" disk drives.

And all our half-height drives feature rapid-start direct drive DC motors for better reliability, speed control and longer media life than any other floppy disk drive. Of course, Shugart still offers the industry's most complete line of full-height floppy and Winchester drives. Plus an extra-economical 2/3-height Minifloppy™ the entry level SA200.

And our newest small wonder, the SA300 3.5" microfloppy.

All backed by the largest and most experienced engineering, sales and service organizations in the business.

Which is our way of giving you more. Even if it's only half as much.

For more information, contact Shugart Corporation, 475 Oakmead Parkway, Sunnyvale, CA 94086, 408/733-0100 (Hamilton/Avnet, authorized distributor).

Shugart
Right from the start.
SEEQ SETS
ANOTHER STANDARD
FOR 5V E² ROM.

FAMILY PLANNING.
Family planning. It's the way to get flexibility in E² designs. And it's why Seeq's "B" family of latched E²ROM makes it practical to plan today's memory needs around a technology that's growing up fast.

For starters, the 52B13 (16K), 52B23 (32K), and 52B33 (64K) all offer fast 1 msec write times, 200 ns access times, and standard JEDEC bytewide pinouts. So expanding from 16K to 64K is a simple upgrade. Not a complex redesign. And with onboard latches (another "B" family standard), E² designs are easy to implement as well as alter.

$6, $15, $40—all in the family.

At Seeq, we use the most advanced technology to make E² more cost-effective. It's a family tradition.

Last year, our oxynitride process produced the world's first 16K 5V E²ROM—eliminating all need for expensive high voltage circuits.

Today, our new 2 micron dry plasma process makes our 64K 52B33 the right solution for all high-performance 16- and 32-bit microprocessor systems.

And this unique combination of technology and market demand will make our E² competitive with older nonvolatile technologies in half the usual time.

That's why by December you'll be able to get your hands on production quantities (25,000 units minimum) of our 64K 52B33 for only $40. Or our 32K for $15. Or our 16K E² for just $6* Check that against EPROM prices. And check the coupon for a way to put our "B" family E² to work at December's prices right now.

And feel free to ask us for whatever else you need. Just call (408) 942-1990. Say you're a friend of the family.
Plugging in poses problems

Designing computers presents a problem that appears to have been ignored by writers, designers, and manufacturers. This problem has continued for the 20 years I have been involved with evaluations and installations. Within clusters of equipment, each component needing power is uniquely powered, requiring a separate power receptacle for each device.

Few manufacturers or suppliers configure centralized, fused power for their particular sets of equipment in total. Some do not have common plugs within their configurations. A 4-plex should be able to configure a small expandable system of CPU, disk, printer, and modem, except that the modem could have a power converter and possibly a channel alignment device. The converter's construction usually denies access to at least one other outlet; in addition, the channel device is uniquely powered—hence, you're short two outlets. Want to add more peripherals? Each will take at least one additional outlet.

Looking behind some of today's "pcs" and "workstation" configurations, you will find a jungle of power cords, power strips, I/O cables, and a back wall of 2- to 10-horsepower outlets. Most buildings today were not designed to support the recent burst of PCs and terminals. In fact, try to convince a non-computer oriented electrical engineer of your requirements for power and cable routes. Lots of luck! Few, if any, buildings will be torn down and rebuilt to support the computer world. However, some are being built or modified to fix the need.

In my opinion, the logical, easiest, and best solution to this aggravation is to have a fused power block on a central unit—with the possible addition of internal isolation transformers. At the very least, it sure would be nice to have a fused power block on a central unit—with the possible addition of internal isolation transformers. At the very least, it sure would be nice to have a fused power block on a central unit—with the possible addition of internal isolation transformers. At the very least, it sure would be nice to have a fused power block on a central unit—with the possible addition of internal isolation transformers. At the very least, it sure would be nice to have a fused power block on a central unit—with the possible addition of internal isolation transformers. At the very least, it sure would be nice to have a fused power block on a central unit—with the possible addition of internal isolation transformers.

The DEC Ethernet products are available with DECnet networking software. With this combination of hardware and software functions, it is possible to copy files, send electronic mail, create and access distributed database management systems and datatrieve files, access remote directories, and log onto other systems.

Additionally, the capabilities of a local area network Ethernet are integrated with our wide area networking services, making Ethernet a segment of a much larger network. Today, inside the DEC, several Ethernetes operate as parts of the DEC engineering network that consists of over 200 computers in locations from California to England.

Ethernet functions offered from DEC are also integrated with SNA and X.25 gateway capabilities. This allows an Ethernet user to access corporate data bases through an SNA gateway or send messages across X.25 public packet-switched nets.

Thomas D. Rarich
Digital Equipment Corp.
1925 Andover St
Tewksbury, MA 01876

Unfortunately, the parts played by both DEC and Intel in the development of Ethernet were not adequately emphasized in this article. Although both were mentioned, possibly further discussions would have made the article more replete.

What is "The Alps Advantage", and why is it important to you, our customers? Essentially, The Alps Advantage encompasses a whole series of custom benefits, brought together to give a competitive edge in your marketplace.

For designers, engineers, and manufacturers—a vast array of electronic, mechanical components and system solutions. Particularly noteworthy:

Welcome to the
Alps Advantage for their
innovative technology, state-of-the-art performance, and high degree of miniaturization, built-in quality and long-life reliability. It also means a never-ending flow of new product introductions and helpful application engineering assistance from our Technical Product Managers.

For purchasing and production people, The Alps Advantage takes on other meanings—competitive pricing, automated manufacturing facilities and on-time deliveries. Equally important, it means a special kind of philosophy based on a spirit of teamwork and cooperative customer relations.

The Alps Advantage is everything you need to improve your products and enhance your competitive position—and everything you’d expect from a world-class supplier. Since its founding in 1948, Alps Electric Co., Ltd. has experienced steady, stable growth—to a level of worldwide sales now up to $1-billion per year!

We look forward to the opportunity of putting The Alps Advantage to work for you—to get started, please contact The Alps Sales Rep nearest you:

<table>
<thead>
<tr>
<th>AL</th>
<th>Huntsville (Jack Harvey &amp; Assocs.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AR</td>
<td>Phoenix (Eltron)</td>
</tr>
<tr>
<td>CA</td>
<td>Santa Clara (Kaye)</td>
</tr>
<tr>
<td>CA</td>
<td>Woodland Hills (Relcom, Inc.)</td>
</tr>
<tr>
<td>CA</td>
<td>San Diego (Cero)</td>
</tr>
<tr>
<td>CO</td>
<td>Englewood (Nelligan Co.)</td>
</tr>
<tr>
<td>FL</td>
<td>Plantation (Gallagher &amp; Assocs.)</td>
</tr>
<tr>
<td>GA</td>
<td>Norcross (Jack Harvey &amp; Assocs.)</td>
</tr>
<tr>
<td>IL</td>
<td>Arlington Heights (Micro Sales, Inc.)</td>
</tr>
<tr>
<td>IN</td>
<td>Indianapolis (Jack Harvey &amp; Assocs.)</td>
</tr>
<tr>
<td>KS</td>
<td>Kansas City (BC Electronic Sales, Inc.)</td>
</tr>
<tr>
<td>KS</td>
<td>Wichita (BC Electronic Sales, Inc.)</td>
</tr>
<tr>
<td>MD</td>
<td>Timonium (Allen Assocs.)</td>
</tr>
<tr>
<td>MA</td>
<td>Waltham (Technology Sales, Inc.)</td>
</tr>
<tr>
<td>MI</td>
<td>Oak Park (A. Blumenberg Assocs., Inc.)</td>
</tr>
<tr>
<td>MN</td>
<td>Minneapolis (RSI)</td>
</tr>
<tr>
<td>MO</td>
<td>St. Louis (BC Electronic Sales, Inc.)</td>
</tr>
<tr>
<td>NJ</td>
<td>Boonton (PAS Assocs.)</td>
</tr>
<tr>
<td>NY</td>
<td>Smithtown (PAS Assocs.)</td>
</tr>
<tr>
<td>NY</td>
<td>Albany (Reagan/Compaq)</td>
</tr>
<tr>
<td>NY</td>
<td>Endwell (Reagan/Compaq)</td>
</tr>
<tr>
<td>NY</td>
<td>Fairport (Reagan/Compaq)</td>
</tr>
<tr>
<td>NY</td>
<td>New Hartford (Reagan/Compaq)</td>
</tr>
<tr>
<td>NC</td>
<td>Raleigh (Burgh-Knecht Assocs., Inc.)</td>
</tr>
<tr>
<td>OH</td>
<td>Rock Hill (Norman Case Assocs.)</td>
</tr>
<tr>
<td>OK</td>
<td>Tulsa (Norcom, Inc.)</td>
</tr>
<tr>
<td>PA</td>
<td>Willow Grove (Harry Nash Assocs.)</td>
</tr>
<tr>
<td>TX</td>
<td>Dallas (Norcom, Inc.)</td>
</tr>
<tr>
<td>TX</td>
<td>Austin (Norcom, Inc.)</td>
</tr>
<tr>
<td>VA</td>
<td>Lynchburg (Burgh-Knecht Assocs., Inc.)</td>
</tr>
<tr>
<td>WA</td>
<td>Bellevue (Venture Electronics)</td>
</tr>
<tr>
<td>CA</td>
<td>St. Laurent (Vite! Electronics)</td>
</tr>
<tr>
<td>CANADA</td>
<td>Mississauga (Vite! Electronics)</td>
</tr>
<tr>
<td>CANADA</td>
<td>St. Laurent (Vite! Electronics)</td>
</tr>
<tr>
<td>CANADA</td>
<td>St. Laurent (Vite! Electronics)</td>
</tr>
<tr>
<td>TN</td>
<td>Johnson City (Jack Harvey &amp; Assocs.)</td>
</tr>
<tr>
<td>OH</td>
<td>Rocky River (Norman Case Assocs.)</td>
</tr>
<tr>
<td>PA</td>
<td>Willow Grove (Harry Nash Assocs.)</td>
</tr>
<tr>
<td>TX</td>
<td>Dallas (Norcom, Inc.)</td>
</tr>
<tr>
<td>TX</td>
<td>Austin (Norcom, Inc.)</td>
</tr>
<tr>
<td>VA</td>
<td>Lynchburg (Burgh-Knecht Assocs., Inc.)</td>
</tr>
<tr>
<td>WA</td>
<td>Bellevue (Venture Electronics)</td>
</tr>
<tr>
<td>CANADA</td>
<td>Mississauga (Vite! Electronics)</td>
</tr>
<tr>
<td>CANADA</td>
<td>St. Laurent (Vite! Electronics)</td>
</tr>
</tbody>
</table>
The Alps Advantage in 5½" floppy disk drives:

Miniaturized for less space, more storage capacity. Since 1948, miniaturization has always been an important part of The Alps Advantage. In our 5½" floppy disk drives, the advantage is immediately apparent: you can double (or quadruple) your storage capacity in the same space! And it's all done without any sacrifice of design or performance features.

Brushless DC motor. Models available with standard brush motor, or new brushless DC motor with 10,000 hours life rating and higher operating reliability without brush noise.

Built-in electronics control board. Models also available as mechanism only, without analog control board.

High speed access time. Choice of 5 or 12 millisecond track-to-track access time, achieved by the use of a unique steel belt head carriage design.

Up to 500 Kbytes storage capacity. Single or double side, single or double density models. 48 TPI track density. Head load time 35 millisecond. FM (single density) or MFM (double density) recording method.

Automatic disk eject. Media removal is fast, smooth and easy.

Simple design, high reliability. High precision ultra-thin stepper motor is combined with a unique hub collet configuration in a simple, reliable design for improved accuracy in head positioning and media clamp centering.

Improved disk life. A ceramic based magnetic head protects the media from excess wear and provides increased accuracy of data readout.

World-wide acceptance. Many thousands of Series 2000 drives have been delivered to OEM manufacturers throughout the world. You can easily learn what they already know about The Alps Advantage—just write or call today.

Low profile Series 2000. Only 1.61" thick—half the size of conventional units!
OUR SMALLEST ACHIEVEMENT IS THE INDUSTRY’S BIGGEST SUCCESS.

The Tandon 8" and 3½" Floppy Company is the world's largest producer of 8" ThinLine™ drives.

And now we're ramping up for high volume production of single and double-sided 3½" drives.

When we introduced the half-height 8" floppy drive, we expected system designers to go wild over it.

You did. Some of you stacked two of our drives to double system storage to as much as 3.2MB without increasing system size. Others took advantage of our small achievement to reduce system size instead.

Whatever you’ve done with our ThinLines, we want to thank you for having the confidence in them to give us an overwhelming lead in the half-height 8" market.

Now we're using our experience in making drives small to make them even smaller. Our new 3½" drives are now in production in four versions. 500K byte single-sided and 1MB double-sided Tandon interface models. And Sony interface-compatible drives of the same capacities.

We plan on becoming the world’s leader in 3½" the same way we became the world’s leader in half-height 8". By focusing our energies on building more drives, better, at a lower cost than anyone else.

Like all Tandon companies, we start with a high degree of vertical integration. And an aggressive commitment to R&D no one can match.

We’ve also established ourselves in a brand-new facility with all the latest manufacturing and test equipment. So we can triple our current leading monthly production rate while ramping up to meet the burgeoning 3½" market.

Just because we’ve become a success by thinking small doesn’t mean our plans are modest.

TANDON 8" AND 3½" FLOPPY COMPANY.
Programming language adds flexibility for artificial intelligence

For systems that manage large data bases with complex control logic, such as expert systems or other phases of artificial intelligence, Symbolics, Inc has integrated attributes of Flavors into its Zetalisp compiler. Flavors is an object-oriented programming language used on the company's 3600 computer system (see Computer Design, May 1983, p 280). The Flavors system allows designers to bind operations and data structures together and to construct well-defined message paths for user interfaces.

In general, the point of object-oriented programming is to construct new data types by defining the data structures associated with the type as well as defining generic operations valid for those data. Specific instances of these types are then created. Each instance maintains local state information and uses the defined operations to interact with the user. Thus, data and procedures are encapsulated as objects of the new data type. This method shields users from the actual implementation and permits programs to be easily developed and maintained.

In this implementation of the Flavor system, flavors are the abstract data types and methods are the generic operators. Objects are flavor instances that are manipulated with messages requesting specific operations. Instance variables hold local state information for a flavor instance. Applications are implemented by first defining the flavors in one part of the program and then creating flavor instances in another.

New flavors can inherit methods and instance variables from existing flavors, or they can explicitly define unique methods and instance variables. In either case, designers explicitly declare the relationships among flavors. For example, certain flavors can be specified in order to define others. An inherited method can be executed conditionally, depending on the flavor declarations. Method definitions of new flavors can override, augment, and otherwise change the methods of existing flavors.

The Flavor system bases its type and method dependencies on a graph structure (multiple parents) that allows arbitrarily complex flavors to be created while still retaining modularity and ease of maintenance. After flavors are defined, flavor instances are allocated and used with a constructor function. Flavor definitions can contain the local variables' initial values. In many cases, initial values can also be declared in the call to the constructor function. Flavor definitions can contain the local variables' initial values. In many cases, initial values can also be declared in the call to the constructor. The system provides accessor methods for instance variables whose values are externally available to the instance. It also provides mutator methods for instance variables that can be changed by other parts of the program.

Once flavor instances are created, they either receive messages that pass arguments to local variables or they request procedure results. In fact, operations are implemented as function calls that accept arguments.

An example of how the Flavors system works is shown in Zetalisp's user defined condition system. The condition system detects exceptional events that occur during program execution and provides a means to respond to those events with user supplied code. Each standard class of events (eg, errors such as dividing by zero) has a corresponding flavor called a condition.

Reporting an event occurrence creates a condition object that is an instance of that flavor. These instance variables contain further information about the event, such as the condition's various parameters. A signaling mechanism then searches for a user supplied code that assumes control. This handler accesses the instance variables for that condition object. The handler can (continued on page 30)
The Spinwriter™ handles any business form you can conjure up.

No matter what your business forms, no matter what size, shape or format, the NEC Spinwriter printer can handle them. Automatically. We have eight forms handlers. All quickly and easily user changeable. There’s a single-sheet feeder with an add-on second bin or envelope feeder. There’s also a cut-sheet guide, a bi-directional tractor, demand document tractor with tear bar and copy separator, manual inserter and bottom feed. With some of our forms handlers, you get functions unavailable anywhere else—like bi-directional paper movement and ultra-fast ribbon cartridge changing with forms handlers in place.

Of all printer companies, only NEC designs and manufactures its own comprehensive family of forms handlers. We built them especially to go with our printers, so they give you the same reliability that has made our Spinwriters a legend.

Our Spinwriters have the industry’s most remarkable uptime standards. More than two years between failures! They need no preventive maintenance or routine lubrication. Ever. And, with only three major spares, they usually can be fixed in only 15 minutes.

Whatever the size or shape of your business form, a Spinwriter can handle it, quickly and reliably. It’s not magic, it’s NEC.
either continue execution (perhaps after repairing a piece of code), or retry the operation at a specified point earlier in the program.

Designers can either specify conditions that are very specific to a particular set of circumstances or others that are more general. Also, they can choose the level of response to conditions according to a particular application's needs.

Custom user interfaces are also implemented with windowing techniques based on the Flavors system. Designers mix their defined flavors with other flavors contained in the window library. Each window is a Zetalisp object and an instance of some flavor (momentary, multiple choice, or multiple menus). To manipulate a window, a program sends it messages. These messages can alter the appearance and shape of that window, control cursor position, and perform I/O operations. Windows also understand many graphics operations that handle drawing points, lines, and regular polygons. The user supplied flavors control or modify the predefined flavors' behavior to suit the specific application. Symbolics, Inc, 257 Vassar St, Cambridge, MA 02139.

Circle 240

Setting sail against the software pirates

Picture this: an antiseptic, $10,000, state of the art desktop microcomputer. Now, imagine it plastered with all manner of odd-sized authorization stickers so that it looks like the cab door of an interstate tractor trailer rig. Sound far-fetched? Not so. This version of "computing 1984" is exactly what is envisioned by Whitesmiths, Ltd, the Concord, Mass software house specializing in C-related products.

The stickers are there to prevent software piracy. They authorize an individual computer to run a specific copy of a program. In a stratum that depends equally on users finking on their fellows, customers defacing their expensive hardware, and the establishment of legal precedents covering "licensing under copyright," Whitesmiths hopes to find a safe harbor from software pirates.

"For every legitimate copy of most popular software packages, between 4 and 10 pirated copies are in circulation," claims Bill Plauger, Whitesmiths' swashbuckling president. He adds that, as a result of this piracy, software developers are losing up to 50% of their rightful earnings. According to Plauger, this situation is threatening the economic health of many software producers.
Introducing the BC-500.
A simple display of intelligence.

Mechanical simplicity, uncomplicated circuitry, and ease of maintenance add up to a cost effective, quality display—the BC-500, the newest 15-inch CRT from Ball. But, design simplicity isn't all you get. The BC-500 gives you the features you want and the performance you have to have. Like an extended video bandwidth that assures crisp, clear alphanumeric presentation. Horizontal line rates available up to 23 kHz. All electronic components on one main circuit board for ease of maintenance.

In addition, the simplicity of the BC-500 gives you design flexibility. A variety of frames are available; wire or sheet metal frame chassis design is strong, compact and lightweight. And what's more, by virtue of the simple single circuit board, a 15-inch monitor is finally available in kit form for easy installation in custom applications.

But, best of all, incorporated into the Ball BC-500 is the experience of 20 years of design and over a million units in the field. That experience shows in the quality and reliability of each Ball product.

The Ball BC-500. High performance in a high quality raster scan display. For the 12-inch version specify BC-400. For a demonstration or information, call our nearest sales office. It's that simple.
Software piracy
(continued from page 30)

Plauger feels that the standard solutions—end-user licenses and patents—are ineffective deterrents to piracy. The former are cumbersome and expensive to execute, the latter of questionable legal validity. So, what to do?

For Whitesmiths, the solution is licensing under copyright. In theory, this tactic relies on existing copyright laws, as amended in 1980 to cover computer programs. These amended laws protect the form or expression of ideas (in programming languages or binary code) rather than the underlying logic or algorithms. It is Whitesmiths' opinion that the amended copyright laws are stringent enough to facilitate the prosecution of commercial pirates—those who copy for a profit. For the time being, disk duping user groups and computer science students are safe.

By extending, or licensing copyrights to OEMs and end users, the rather limited rights of pure copyright are expanded. This expansion allows users to make and retain limited copies of programs on magnetic media. For instance, users may make one authorized copy of a program for storage within a specific computer, and archival copies for private use. The catch, however, is that a specific computer is authorized to run each program.

Thus, a user cannot buy a copy of Whitesmiths' UNIX-like operating system, Idris, and lend it to a friend. Nor can a user, in good conscience, copy a Whitesmiths program onto several mass storage units attached to different computers. Software can be bought and sold with hardware, however, and OEMs need not report such transfers. This last aspect of the plan greatly simplifies the OEMs' life.

The instrument of Whitesmiths' plan is the authorization seal (see Photo). This intricately drawn seal is sold with the software and must be promptly affixed to the machine on which the software will, forever after, run. The detailed and difficult to counterfeit seal carries two series of numbers, one of which identifies the product. The other series of numbers identifies the program that the machine to which the seal is affixed is authorized to run. In this case, a Whitesmiths cross compiler is running under RSX-11 with a POS-11 target.

The key to this software protection scheme—enforcement—seems also to be its Achilles' heel. The burden of guilt falls most upon users, for it is they who must bring violators to Whitesmiths' attention. In the laissez faire world that is microcomputing, it is questionable whether or not users can be imbued with so high a sense of duty. Part of the reason is that software producers have not, to date, been successful in convincing users that a $1200 floppy disk is really 10 times as valuable as a $120 floppy disk, and therefore worthy of protection.

In any case, Plauger is optimistic about the cooperation he will receive from his customers: "We are . . . so convinced that everyone else is as concerned about piracy as we are that we are asking everyone to participate." Plauger adds, "If our software is running on a computer that does not display an authorization seal, that software is probably not an authorized copy. I urge you to report such incidents to me."

Piauger claims that he will vigorously enforce his ownership rights in court and exhorts other software producers to follow his lead by adopting a similar authorization seal.

Whitesmiths' attorney, Henry Dane, is more circumspect in his appraisal of the authorization seal program. He did not speculate on the likelihood of user cooperation, but he did emphasize that, in his opinion, the company is on firm legal ground where software copyright laws are concerned. Though unable to cite any recent legal precedents or litigation relating favorably to licensing under copyright, Dane has no doubt that Whitesmiths will get a sympathetic hearing in court if, and when, the time comes.

Though confident about cooperation, Company President Plauger is slightly less assured where legal (continued on page 34)
The IBM PC is an effective development system for products which use the 8086 and 8088. MTOS real-time operating systems are compatible with the IBM PC...

What a marriage!

Distributors Worldwide

ipi Industrial Programming Inc.

the standard-setter in real-time operating systems

100 Jericho Quadrangle, Jericho, New York 11753
(516) 938-6600 • Telex: 429808 (ITT)
Software piracy (continued from page 32)

matters are involved. At a recent press conference, he said, "We know that we are taking some chances by pioneering this concept . . . [but] our attorneys assure us that we are in a good position. They say that you can recognize pioneers by the arrows in their backsides. I sure hope I dodge most of the arrows."

Whether on firm ground or pioneering, the Whitesmiths strategy for combatting software piracy is interesting on several counts. First, it illustrates the gravity of piracy, a problem that has even penetrated the highly specialized environs of Whitesmiths' market.

Second, this strategy demands customer accountability unheard of in any other buyer/seller relationship. Third, if it is to be viewed as anything more than an elaborate ruse, the antipiracy program will require considerable financial resources to support ongoing litigations.

In a practical sense, Whitesmiths' approach is most likely to serve as a deterrent to, rather than an ironclad prohibition of, commercial piracy. As Atari has shown in the microcomputer game arena, the best defense against piracy may actually be a boisterous offense. As the folks at Whitesmiths set sail to meet the software pirates, the first legal broadsides have yet to be fired.

—Chris Brown, Technical Editor

Superminis doubles performance

Highly pipelined parallel architecture, Advanced Schottky TTL, fast static RAMs in dedicated caches, and hardware design innovations including a "board-slice" floating point processor and separate address generator are key features of Data General's latest bid in the mainframe-class superminicomputer arena. While doubling the performance of its earlier high end MV/8000, the company has cut cycle time in the Eclipse® MV/10000 from 220 to 140 ns.

The 32-bit virtual memory machine gleaned 2.5M-Whetstone/s single-precision and 1.9M-Whetstone/s double-precision performance for up to 192 users. This is backed by 16M-byte main memory, 18.50-byte online storage, 4G-byte virtual address space, and 2G-byte program size. Cross development of AOS/RT32 realtime and AOS/VS virtual storage operating systems accommodates CAE and technical timesharing as well as real-time computational applications.

A bipolar bit-slice microsequencer directly accesses the writable control store every 140 ns. As an option, the control store expands from 4K to 8K words (425K to 850K bits), reserving 4K words for the computer's instruction set and 4K words for user-programmable microcode. Within the loadable store, field groups are assigned to control specific processing subsystems. This permits many hardware resources to be managed simultaneously with reduced microsequencing overhead.

A single-board integer processor performs the system's main arithmetic and logic functions, including 16- and 32-bit integer arithmetic, number shifting, and data translation/validation. It has a fixed-point ALU; 2-port, 32-bit register file; and 256-register scratchpad memory. The single-board processor executes macroinstructions like add, load, and store in one 140-ns cycle, offloading logic functions to other processing subsystems if necessary.

Under direct control of the microsequencer, the floating point processor operates synchronously with the integer processor, performing integer multiply/divide operations to offload that processor if directed. Two identical boards compose the floating point unit, which divides the execution task by using one (continued on page 39)
New Amdek

3" micro-floppydisk drive system!

AMDISK-III . . . OEM's choice:

- Works with standard 5¼" controllers
- Up to 1 megabyte of unformatted double density storage
- Ideal for industrial data collection/storage applications
- Microfloppy's hard plastic diskette offers increased durability vs. 5¼" floppies
- Automatic shutter protects media
- Small form factor for easy storage

Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Double Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td>250K</td>
</tr>
<tr>
<td>Uniformated Per Surface</td>
<td>250K</td>
</tr>
<tr>
<td>Media</td>
<td>250K</td>
</tr>
<tr>
<td>Record Surfaces</td>
<td>80</td>
</tr>
<tr>
<td>Tracks</td>
<td>80</td>
</tr>
<tr>
<td>Recording</td>
<td>8946</td>
</tr>
<tr>
<td>Max Recording Density</td>
<td>9946</td>
</tr>
<tr>
<td>Track Density</td>
<td>100</td>
</tr>
<tr>
<td>Transfer Rate</td>
<td>250K</td>
</tr>
<tr>
<td>Access Time</td>
<td>55</td>
</tr>
<tr>
<td>Average Access Time</td>
<td>55</td>
</tr>
<tr>
<td>Track to Track</td>
<td>3</td>
</tr>
<tr>
<td>Setting Time</td>
<td>15</td>
</tr>
<tr>
<td>Average Latency Time</td>
<td>100</td>
</tr>
<tr>
<td>Motor Start Time</td>
<td>0.7 (ms)</td>
</tr>
<tr>
<td>Data Speed</td>
<td>300</td>
</tr>
<tr>
<td>Reliability</td>
<td>10</td>
</tr>
<tr>
<td>Error Rates</td>
<td>10</td>
</tr>
<tr>
<td>Soft Error</td>
<td>10</td>
</tr>
<tr>
<td>Hard Error</td>
<td>10</td>
</tr>
<tr>
<td>Seek Error</td>
<td>10</td>
</tr>
<tr>
<td>Media</td>
<td>3 inch Cartridge</td>
</tr>
<tr>
<td>Drive interface</td>
<td>Plug Compatible with 5.25 inch FDD</td>
</tr>
</tbody>
</table>

External Interface

Connector: 34 pin (Shugart)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Signal</th>
<th>Pin No.</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Unreset</td>
<td>10</td>
<td>Stop</td>
</tr>
<tr>
<td>4</td>
<td>In use (option)</td>
<td>22</td>
<td>Write data</td>
</tr>
<tr>
<td>5</td>
<td>Drive select 3</td>
<td>24</td>
<td>Write gate</td>
</tr>
<tr>
<td>6</td>
<td>Drive select 3</td>
<td>24</td>
<td>Write gate</td>
</tr>
<tr>
<td>7</td>
<td>Drive select 0</td>
<td>26</td>
<td>Track 60</td>
</tr>
<tr>
<td>10</td>
<td>Drive select 0</td>
<td>26</td>
<td>Track 60</td>
</tr>
<tr>
<td>12</td>
<td>Drive select 1</td>
<td>30</td>
<td>Read data</td>
</tr>
<tr>
<td>14</td>
<td>Drive select 2</td>
<td>32</td>
<td>Unused</td>
</tr>
<tr>
<td>16</td>
<td>Drive select 2</td>
<td>32</td>
<td>Unused</td>
</tr>
<tr>
<td>18</td>
<td>Direction</td>
<td>33</td>
<td>Ground</td>
</tr>
</tbody>
</table>

NOTE: Single head per drive

Evaluation samples

$480

Includes two-drive Amdek unit with built-in power supply, 4 diskettes and application literature. Call (312) 364-1180.

The AMDISK-III Micro-floppydisk System is an engineering breakthrough in disk size, storage capacity, media protection and user convenience. Designed to serve many applications, the Amdek system is ruggedly constructed to provide years of trouble-free operation. Warranty is 90 days (parts & labor).

Put the new AMDISK-III to test . . . its recording format, data transfer rate and disk rotation speed are compatible with 5¼" floppydisk drives. Call, or write for evaluation samples at only $480.00 . . . or circle the reader service number for full technical details.

2201 Lively Blvd.  •  Elk Grove Village, IL 60007
(312) 364-1180  •  TLX: 25-4786
REGIONAL OFFICES: Calif. (714) 662-3949  •  Texas (817) 498-2334

Amdek . . . your guide to innovative computing!
Now, 16K x 4 DRAMs.
Finally, the 64K organization you’ve been waiting for at speeds you’ve been hoping for

16K x 4 DRAMs are here...in the new INMOS IMS2620 series. They give you a choice of 100, 120, and 150ns access times. What’s more, they’re available in low-cost plastic packaging. That’s good news all around. Because it means greater design flexibility and high performance at reasonable cost.

The 16K x 4 organization is a natural for graphics applications and other high performance designs where high data rates are required. And provides a factor of four reduction in chip count when you upgrade from 16K x 1 to 16K x 4 DRAMs. Look to this organization when you need the most in system performance, flexibility and economy.

Our growing 64K DRAM family also includes the 64K x 1 IMS2600 series. With INMOS’ "Nibble Mode," they deliver effective cycle times below 85ns with a 100ns part.

Both the 16K x 4 and 64K x 1 organizations include our “CAS before RAS” refresh-assist function, which reduces support circuitry...and system cost.

For a low-cost introductory offer of our new 100ns 16K x 4 DRAM, call an INMOS distributor today.

Check the chart.

<table>
<thead>
<tr>
<th>Organization</th>
<th>Part No.</th>
<th>Access Time</th>
<th>Cycle Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>16K x 4</td>
<td>IMS2620-10</td>
<td>100ns</td>
<td>160ns</td>
</tr>
<tr>
<td></td>
<td>IMS2620-12</td>
<td>120ns</td>
<td>190ns</td>
</tr>
<tr>
<td></td>
<td>IMS2620-15</td>
<td>150ns</td>
<td>240ns</td>
</tr>
<tr>
<td>64K x 1</td>
<td>IMS2600-10</td>
<td>100ns</td>
<td>160ns</td>
</tr>
<tr>
<td></td>
<td>IMS2600-12</td>
<td>120ns</td>
<td>190ns</td>
</tr>
<tr>
<td></td>
<td>IMS2600-15</td>
<td>150ns</td>
<td>230ns</td>
</tr>
</tbody>
</table>

Introductory EVALUATION OFFER

Contact your local INMOS distributor for two each of the 100ns IMS2620P-10, 16K x 4 DRAM and technical information ($25). Limit three offers per customer. Offer expires Aug. 31, 1983.

Then call an INMOS distributor today. Arrow Electronics
Anthem Electronics
Future Electronics
Lionex Corp.
RAE
Complies in a snap!

This new Spectra-Strip® two-piece backshell simply snaps over a D-Sub connector with extruded jacketed shielded cable. That's all it takes to help put you in compliance with Docket 20780 of the FCC's "Technical Standards for Computing Equipment" (see the test results below).

Little cable preparation is needed. You retain mass termination capability. You get built-in strain relief over a wide range of cables. And the backshell is stainless steel to withstand rough handling.

Our D-Sub backshell fits the Spectra-Strip 817 connector and all UL-listed jacketed, shielded planar cables.

For more information, contact your nearest Amphenol sales office or distributor listed here. And be sure to ask about our complete custom cable assemblies.

![Graph showing frequency vs. dB for different cable configurations](image-url)

Amphenol World Headquarters: 2122 York Road, Oak Brook, Illinois 60521
Sales Offices: Atlanta (404) 394-6296 • Boston (617) 475-7055 • Chicago (312) 986-2330 • Dallas (214) 343-8420 • Dayton (315) 294-0461 • Denver (303) 443-4786 • Detroit (313) 722-4120 • Greensboro (919) 392-6273 • Houston (713) 444-4096 • Indianapolis (317) 842-3245 • Kansas City, Mo. (816) 737-3937 • Knoxville (865) 690-4728 • Los Angeles (213) 352-3180 • Miami (305) 961-2100 • Milwaukee (414) 282-2277 • Minneapolis (612) 333-4596 • New York (212) 364-2270 • Orlando (305) 676-5504 • Philadelphia (215) 745-1427 • Phoenix (602) 305-9327 • St. Louis (314) 969-2277 • Salt Lake City (801) 364-6481 • San Diego (714) 272-5401 • San Francisco (415) 732-8990 • Seattle (206) 455-2325 • Syracuse (315) 455-5786 • Washington, D.C. (703) 524-8700
Canada: Montreal (514) 482-2510 • Toronto (416) 291-4401 • Vancouver (604) 278-8736
International: Oak Brook, Illinois TELEX 206-054

© 1983 Allied Corp.

CIRCLE 26
Mainframe-class supermini (continued from page 34)

Dedicated pipelines, caches, and buses allow Data General's Eclipse MV10000 subsystems to operate concurrently with minimal contention. Microcode has been extended from 80 to 104 bits to take advantage of expanded system organization and provide better control of parallel operation.

board for single-precision (32-bit) and both boards for double-precision (64-bit) operations. Parallel design dedicates separate hardware ALUs for mantissa, sign, exponent, and multiply/divide functions. Accuracy is improved through 72-bit wide data paths that allocate 56 bits to the mantissa and 8 bits to the exponent, with 8 guard bits.

Four pipeline levels in the instruction processor provide for concurrent fetch, decode, and execution of macroinstructions. Each instruction sequence is carried through the pipeline in various stages of completion, with one exiting every 140 ns. The directly mapped instruction cache (64-bit) operations. Parallel design dedicates separate hardware ALUs for mantissa, sign, exponent, and multiply/divide functions. Accuracy is improved through 72-bit wide data paths that allocate 56 bits to the mantissa and 8 bits to the exponent, with 8 guard bits.

Four pipeline levels in the instruction processor provide for concurrent fetch, decode, and execution of macroinstructions. Each instruction sequence is carried through the pipeline in various stages of completion, with one exiting every 140 ns. The directly mapped instruction cache supports a fifth cycle. Under microprogram control, the address generator will perform 32-bit arithmetic to offload the integer processor.

In virtual memory applications under AOS/VS, the 70-ns address translator is a hardware accelerator for the demand paging function. Operating in conjunction with the instruction processor and address generator, the unit translates logical addresses sent from the address generator into physical addresses. A high speed 4K cache contains a lookup table that stores 14 bits of recently translated addresses for up to 1024 individual pages in physical memory. Furthermore, these 14 bits (continued on page 45)
For the microcomputer software engineer who doesn't have time to make mistakes.
Tek's new Pascal Language Development System supports you from the first line of source code to the last line of debug.

Conventional Pascal has supported only certain phases of microcomputer software design. Until now.

Tek goes all the way with the Pascal Language Development System (LANDS) for the 8560 Multi-User Development System. A Language-Directed Editor cuts time recompiling.

The Pascal Language-Directed Editor catches and flags syntax errors before they ever reach the compiler. A Pascal Compiler targets directly to microcomputer design.

The Pascal LANDS Compiler has an extensive array of microcomputer enhancements, including full I/O access and interrupt servicing. Even complete support of I/O simulation during initial emulation and debug. And an optimizer that typically reduces code by 20 to 40 percent compared to other compilers.

An Integration Control System automatically configures the hardware/software interface. An exclusive from Tek, the Integration Control System (ICS) works from a simple list of user-supplied parameters to generate the hardware/software interface code. Including memory configuration, interrupt handling and initialization/reset code. Integration tasks now take minutes instead of days.

Pascal Debug speeds hardware/software integration. Pascal Debug completely eliminates time-consuming translations of low-level debug information back into its Pascal counterparts. You can now debug in the same language you programmed in.

Put Pascal LANDS on your design team today.

Contact your local sales engineer or write us at the addresses below.

U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc., P.O. Box 4828, Portland, OR 97208.
Phone: 800-547-1512, Oregon only 800 452-1877
Telex: 910-467-8708, Cable: TEKTRONIX
Europe, Africa, Middle East Tektronix Europe B.V.
European Headquarters, Postbox 827, 1180 AV
Amstelveen, The Netherlands, Telex: 18312
Canada, Tektronix Canada Inc., P.O. Box 8500, Barrie,
Ontario L4M 4V3. Phone 705 737-2700

Circle 27 for Literature
Circle 28 for Sales Contact
Seagate's ST400 Series is the most popular family of Winchester disc drives ever offered. And no wonder. These 5¼" Winchester disc drives deliver more value for your money. More quality. More reliability. More performance. And all at a better price.

The ST400 Series offers the right capacities. 6.38, 12.76 or 19.14 megabytes (unformatted). All use the same industry-standard ST506 controller and matching mini-floppy form factor for easy upgrade.

The right features.
All use manganese-zinc heads, advanced stepper motor, metal band actuator, open loop head positioner, and patented air flow spindle pump. An onboard microcomputer provides buffered seek and fast step algorithm for an average seek of 85 milliseconds, including settling time.

The right quality.
Seagate backs the ST400 family with a full one year warranty, our industry-leading "105% Seagate Guarantee," and the world's biggest support team devoted entirely to 5¼" Winchester drives.

Meeting special needs.
Looking for faster, more reliable removable storage? Go with our new ST706.
Need a more compact drive? Pack more data in less room with our new ST206 half-high Winchester. Both new drives store 6.38 megabytes (unformatted) with reliable bit and track densities.

We have what you want in Winchester.


### The ST400 Series

<table>
<thead>
<tr>
<th>ST406</th>
<th>ST412</th>
<th>ST419</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unformatted capacity (MB)</td>
<td>6.38</td>
<td>12.76</td>
</tr>
<tr>
<td>Formatted capacity (MB)</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Average access time (ms)</td>
<td>85</td>
<td>85</td>
</tr>
</tbody>
</table>

Now Shipping In Volume

Seagate Technology

360 El Pueblo Road, Scotts Valley, California 95066 (408) 438-6550, TELEX 172114 SCVL
Regional Sales Offices: Hopkinton, Massachusetts (617) 435-6966; Newport Beach, California (714) 801-9964; Richardson, Texas (214) 783-678; Schaumburg, Illinois (312) 397-3727
European Sales Office: Kreilsterstrasse 21, 8000 Munich 80, West Germany, 89-43-13-900, TELEX 5213379
Authorized U.S. Distributor: Arrow Electronics

"Turning the tide in disc technology"
Invest in Time
Your Customers Can't Wait

Getting your project completed on time is critical. Investing in the right software tools puts time on your side.

We write software for a living. We understand the importance of time to the professional programmer. To complete projects on time you need good software tools. So we create high quality, timesaving tools for users of DEC and MC68000-based computer systems.

**Pascal-2 Compiler** It generates fast, compact code. Because the compiler does the optimizing, programmers can spend time on other programming tasks. Because Pascal is a structured language, other programmers can easily read your programs. Indeed, it's the language most programmers are learning today.

Additionally, programs written in Pascal-2 are portable. Now you can change hardware without having to re-write your software.

**Additional TimeSavers** The time you save with our Pascal-2 compiler is only the beginning. We also provide a full line of other TimeSavers. *Pascal-2 source-level Debugger* for true high-level debugging ease. *SourceTools* for control and management of changes to source programs. *Concurrent Programming Package* for real-time scheduling and device drivers. *Profiler* for identifying performance bottlenecks in programs.

The Pascal-2 Compiler is now available on UNIX for the MC68000 and PDP-11 computer systems.

**TimeSavers from Oregon Software.** Your customers can't wait. And neither can you.

**Oregon Software** 2340 SW Canyon Road Portland, Oregon 97201 (503) 220-7760 TWX: 910-464-4779

The Pioneer in Performance Pascal

DEC and PDP-11 are trademarks of the Digital Equipment Corporation. MC68000 is a trademark of Motorola Inc. UNIX is a trademark of Bell Labs.
Mainframe-class supermini (continued from page 39)

are concatenated into full physical addresses. When a program requests a page, the address translator checks for the location of that page in the cache; a "hit" obviates the address regeneration step.

Moreover, address translator logic controls access to all programs, data, and files via hardware. This imposes an 8-level security structure upon the system's 4G-byte address space. Each ring corresponds to one of the eight segments maintained by the AOS/VS operating system for demand-paged virtual memory management. Rings are prioritized, and higher privileged rings assigned to critical system processes such as operating system or memory and file management software. Application programs and user data usually reside in outer, lower privileged rings. Communication between rings is allowed only after the system confirms proper accessibility, according to a hardware implemented hierarchy.

A 16K-byte directly mapped system cache is the primary interface between memory and the rest of the system. To reduce system overhead associated with updating the cache image in main memory, this cache assumes a write-back (ie, rather than write-forward) approach. Two independent 32-bit ports manage system cache and memory, reserving one for CPU access and the other for I/O activity; each has a bandwidth of at least 28.4M bytes/s.

System cache data storage is organized in 1K blocks, and memory contents are transferred to the cache at the rate of one block every 560 ns. Lookahead/lookbehind buffering improves the hit rate for both sequential and iterative programs. When data requested by the central processor are in the cache, a memory address can be accessed in 140 ns. At a 95% cache hit rate, effective average memory access is 175 ns.

By doubling the bandwidth available to the CPU, dual-channel intelligent I/O controllers can meet a wide range of applications, peripheral performance characteristics, and transfer rates. One I/O controller is standard; the second is optional. Each controller's burst multiplexer channel (BMS) bus supports eight bus loads and eight BMS controllers, with 14.2M-byte/s input and 10.0M-byte/s output. Nova®/Eclipse compatible data channel (DCH) buses provide direct memory access. Supporting up to 16 loads, the DCH bus is used for general purpose I/O, disk backup, and communication networking applications. Each DCH bus has 1.4M-byte/s output and 2.0M-byte/s input.

Up to 192 user terminals are supported by intelligent asynchronous controllers that relieve the CPU of character interrupts, buffering, and communication protocol overhead. For interprocessor or medium to high speed communications, up to four intelligent synchronous controllers provide eight communication lines supporting SDLC, HDLC, and IBM's BSC protocols. Each synchronous controller contains a 16-bit microEclipse computer, host and line communication interfaces, and 128K-byte memory.

The system control processor acts as the computer's diagnostic subsystem. It incorporates a 16-bit microNova computer with its own operating system and 128K bytes of address space. Diagnostics can run with power supply and only two boards functioning—the system control processor and one I/O controller.

MV/10000 is hardware and software compatible with other Eclipse MV family computers. Languages supported include COBOL, FORTRAN 77, PL/I, BASIC, C, RPG II, APL, Pascal, and DG/1. The basic 2M-byte configuration costs about $211,000.

Data General Corp, 4400 Computer Dr, Westboro, MA 01580.

Circle 241
Introducing the DPS-2400 Dimensional Processing System™ from Aptec. It's an evolutionary system concept that lets you configure powerful attached subsystems — using your choice of multiple array processors and other peripherals — free from the bottlenecks of current approaches.

Data acquisition and multiprocessing systems deliver far greater power when controlled by DPS-2400 than when controlled directly by your host.

The solution is simple when you start with DPS.

DPS-2400 attaches to the UNIBUS* of your VAX® or PDP-11® computer to form the central node of an attached subsystem using UNIBUS-compatible peripherals. DPS contains a 24MB/sec. Data Interchange Bus to handle multiple, concurrent data transfers without loading your UNIBUS. Up to 24MB of high speed mass memory provide efficient data staging for pipelined and parallel processing used in 2-D and 3-D applications. And, a set of fully programmable Data Interchange Adapters provide individual control of all DPS subsystem peripherals, including up to ten array processors.

Because DPS is designed specifically for multiprocessing and dataflow operations, it can greatly increase the efficiency and throughput of a single array processor. DPS makes systems with multiple APs not only possible, but extremely economical. And, because it off-loads subsystem control, DPS frees your host for the higher level supervisory tasks for which it is best suited.

Aptec support speeds and simplifies application development.

Hardware integration is greatly simplified by DPS's full compatibility with your UNIBUS peripherals and a variety of standard, available array processors. Our STAPLE** application development software, and field application assistance, are provided to get you up and running in the shortest possible time.

The Dimensional Processing System from Aptec. There's no simpler, faster, or more economical route to a working solution for scientific computing.

For more information or to arrange a demonstration contact Aptec today.

*UNIBUS, VAX and PDP-11 are trademarks of Digital Equipment Corp.
**STAPLE is Aptec's Structured APplication Language & Executive.

APTIC COMPUTER SYSTEMS, INC.
10180 S.W. Nimbus Avenue
Portland, OR 97223 (503) 820-8840
Telex 437167

CIRCLE 33
Advances make CMOS serious VLSI contender

Major advances in CMOS are leading this technology toward dominance in increasing application areas, especially those that demand low power consumption and portable operation. In fact, engineers are no longer speculating about whether or not CMOS will become predominant but rather about which CMOS technology will win out—or, indeed, whether an industry standard CMOS technology will emerge.

In addition to the low power consumption for which it is well known, CMOS, in aiming for greater densities, also must address reliability, high data bandwidth, and increased speed issues. Intel Corp has announced its CHMOS-D III process technology, which addresses all four issues. Although it has not announced any specific product, the company has demonstrated this technology in the form of a 70-ns 64K DRAM.

Using an HMOS-like silicon substrate, CHMOS uses a P-channel memory cell embedded in an N-well biased at $V_{DD}$ potential. Soft errors induced by alpha particles are partially prevented because the N-well array acts as an effective minority carrier barrier.

Soft error resistance is further improved due to CHMOS’ ability to create much thinner storage gate oxides than before, which increases the capacitance of any size memory cell. The greater the capacitance, the larger the charge that can be stored; hence, it becomes less likely that the charge disturbance caused by an errant alpha particle will cause an error.

Intel reports that by using CHMOS it has achieved gate oxide thicknesses of under 150 Å—down from 1200 Å—and an average gate capacitance of about 145 femtofarads using a 250-Å gate oxide thickness. Gate capacitance in Intel’s 2164A HMOS 64K DRAM is 85 femtofarads.

Significant improvements in power consumption have also been reported. Intel claims that operating current is about one-half that of the HMOS 64K DRAM, or 28 mA at a 135-ns cycle time. Standby current at 5 µA amounts to about one-fifth that of the HMOS product.
**CMOS advances**
(continued from page 47)

word line technique to improve both the word delay and the column current. In the 64K RAM, the cell array as well as the word line is divided into eight 1K blocks. The word lines are arranged so that current flows only in a selected block, thus reducing overall power consumption. Mitsubishi reports a one-eighth reduction in column current. Address access time of 50 ns has also been reported.

With the prospect that CMOS may well become a dominant VLSI technology, some observers predict that there will be a variety of CMOS technologies responding to differing speed, power, noise, and radiation requirements, as well as process compatibility and analog capability requirements. N-well CMOS, however, appears to be gaining popularity, especially in the memory area, because of its speed and its ability to avoid latchup problems when used at scales below 2 microns. An even greater prospect is to go beyond single-crystal substrates to epitaxial wafers. The latter are particularly attractive because of their relative immunity to latchup at short channel lengths, while silicon-on-insulator (SOI) options become less attractive due to high cost.

**QIC no guarantee for compatibility**

Proposed standards for quarter-inch tape cartridge drives are intended to help establish that medium as the likely choice to back up rigid disk drives. Yet, many members of the Working Group for Quarter-Inch Cartridge (QIC) Drive Compatibility admit that the adoption of the QIC-02 interface and QIC-24 format specifications will not guarantee total compatibility between streaming drives and controllers.

ANSI and the European Computer Manufacturers Association (ECMA) currently have both proposals under consideration. There are, however, specific concerns that will, no doubt, be the focus of future ANSI and ECMA discussions.

For example, a total of three command sets are defined in the QIC-02 interface proposal. Yet only one set will be required for all controllers and drives. Also, magnetic specifications in the QIC-24 format proposal leave considerable latitude for different drive implementations. Idiosyncrasies among these drives (eg, unique erasing schemes) can inhibit the ability to exchange cartridges.

Unquestionably, more work is needed before these standards are adopted. Meanwhile, system designers should keep one phrase in mind: "let the buyer beware."
CalComp introduces the MBA.

Every computer system has the business basics—accounting, finance, administration.

But when end users or OEMs add CalComp's M-84 plotter, their system becomes an MBA (Master of Business Art) that produces presentation-quality graphics for less than $2,000.

The M-84 actually makes your system a little smarter. It's based on the Z80 microprocessor and has built-in firmware for five line styles, selectable character rotation, six different character sets and circle, arc and sector generation. It can also work as a printer and digitizer.

M-84 is fast, precise and quiet. It plots at speeds up to 17.7 inches per second with resolution of .004 inches on paper or film for overhead projection.

M-84 is analytical and easy to maintain. Diagnostics test and report on interface and plotting functions on your command.

The M-84 is versatile. There are three standard interface models—Centronics, IEEE and RS-232, and most popular applications software packages, including ISSCO's DISSPLA and TELL-A-GRAF, SAS/GRAF and Digital Research CP/M-based Graphic System Extension.

Our M-84 is colorful—8 pens, 8 colors. The high number of pens means faster plots and easier operation because users won't have to switch pens to get more colors.

Don't wait to get your M-84. Call your CalComp representative today:

California Computer Products, Inc., M/S3, 2411 West La Palma Ave., Anaheim, California 92801. In continental U.S. except California, call (800) 556-1234, ext. 156. In California (800) 441-2345, ext. 156.
Meet HP's new 1630 Logic Analyzer
a bottleneck... and ecstatic when we

From now on it makes no sense to buy an analyzer that offers timing and state measurements only. Not when you can have these capabilities plus interactive analysis and software performance measurements too. All for less than the cost of a good timing and state machine alone.

That's what you get with HP's new 1630A/D Logic Analyzer. It delivers advanced hardware and software testing and debugging power. Plus the ability to quickly spot software bottlenecks and inefficiencies. And a way to resolve hardware/software fingerpointing conflicts. With one low-cost instrument.

HP's new 1630 extends the power of logic analysis to span most of the development cycle. And productivity gets a big boost. Because the 1630's simple interface, combined with low-cost peripheral compatibility, speeds setups and documentation. Best of all, it's affordable for even the smallest lab.

At $8,600, the 1630A gives you 35 channels of state (to 25 MHz), 8 channels of timing (to 100 MHz), or, in the interactive mode, 27 state and 8 timing.

For $10,630, the 1630D offers 43 channels of state or 16 timing.
In the interactive mode, you have a choice of 35 state and 8 timing or 27 state and 16 timing. Both models include software performance analysis.
Here's what all that capability can do for you.
You’ll be amazed when it shows you how you the price.

Software Performance Analysis

Ever had a software bottleneck? A routine that takes too much time? Those problems won't stand in your way with this powerful new analysis mode. Histograms of time-interval distribution eliminate guesswork by showing you best case, worse case, and average time between any two events you define...nonintrusively...while your system is operating. Great for benchmarking. And spotting out-of-spec modules.

Interactive Measurements

Now there's a logical way to resolve hardware/software fingerpointing feuds. The 1630 lets you monitor bus activity in the state mode, trigger on a given bus pattern, then view asynchronous status and control line activity in the timing mode. This quickly unravels problems such as I/O port malfunctions. Similarly, you can establish trigger conditions based on timing parameters, then view state activity. This correlates hardware malfunctions to software errors. For example, a false reset due to a glitch.

Timing and State Analysis

In traditional operating modes, the 1630 delivers new sequencing, triggering, and store qualification power. For timing analysis, this includes pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. In the state mode, four user-defined terms can be used in any combination to define sequence, store qualification, trigger and restart conditions. With these resources, you get right to the problem. Without sorting through tons of data.

But that's not all. The 1630 makes it easier yet by talking your language. You can assign alphanumeric labels to input channels and status or control line patterns. Measurements are then displayed in your system's terminology. In addition, the 1630, with low-cost peripherals, performs inverse assembly. So you see listings in target microprocessor mnemonics. From now on, you needn't struggle with time-consuming conversions.

Histograms of memory space activity show where the action is. If you've got a bottleneck, this display leaves no doubt about its location.

Get all the details on this advanced analyzer. See how it takes the drudgery out of logic testing, debugging and analysis, speeding your project to completion. Call your local HP sales office listed in the telephone directory white pages. Ask for an HP field engineer in the electronic instruments department.

* U.S.A. list prices only.

HEWLETT PACKARD

CIRCLE 36
Shown are IBM-PC® compatible programs. The Columbia VP portable runs MS-DOS® plus five other operating systems.

INTRODUCING THE COLUMBIA VP PORTABLE.
IBM-PC COMPATIBILITY AT AN AFFORDABLE PRICE.

World Headquarters: 9150 Rumsey Road
Columbia, MD 21045
(301) 992-3400
TWX 710-862-1891

West Coast: 3901 MacArthur Blvd.
Suite 211
Newport Beach, CA 92660
(714) 752-5245
Telex 277778

Europe: Limittenstr. 94
4050 Moenchengladbach 2
West Germany
02166-47097
Telex 852452

Call our distributor nearest you.
Access Systems
Wellesley, MA
(617) 237-7743

Advanced Management Systems
Aurora, CO
(303) 752-2972

Peripherals Plus, Inc.
Montreal, Quebec, Canada
(514) 849-7533

N.I.D.I. (National Instrument Distribution Inc.)
Dayton, OH
(513) 433-4503

Distributors in Australia, Austria, Belgium, Colombia, Denmark, Hong Kong, Israel, Italy, Malaysia, Netherlands-Antilles, Norway, Portugal, Spain, Sweden, Switzerland, United Kingdom, Venezuela.
Ahead in industry compatibility.

Today, the Columbia VP portable takes on hundreds of IBM-PC compatible software programs and IBM-PC add-ons or peripherals.

What's more, six other Columbia-supported operating systems are available—CP/M-80, CP/M-86, Concurrent CP/M-86, OASIS-16 and XENIX available soon—stretching the Columbia VP's software compatibility beyond any other personal computer you can buy.

Get started with thousands of dollars worth of software FREE.

Every Columbia VP portable is shipped with fully supported software that will save you thousands of dollars on your initial purchase. That means your Columbia is up and running right out of the box.

Included is:

- Perfect Write®
- Perfect Filer®
- MS-DOS®, with RAM disk
- Macro/88 Assembler
- MS-BASIC®
- Space Commanders™
- Fast Graphs®
- Perfect Speller™
- Perfect Calc
- Asynchronous Communications Support
- Columbia Tutor
- Home Accountant
- Plus®
- CP/M-86®
- CP/M-86®

Full feature performance at an affordable price.

The Columbia VP portable features an 8088 16-bit CPU, 128K RAM, (additional 128K, optional), 640K in dual disk drives, one IBM-PC compatible expansion slot, one serial and one parallel I/O, IBM-PC-compatible keyboard, and a 9" built-in monitor with graphics.

The best news of all is the price: $2,995—including software. And the Columbia is built with lasting value in mind. Rugged single board design plus the flexibility to expand and personalize your Columbia VP.

Made in U.S.A.—supported worldwide.

All Columbia hardware and software are backed by our dealers and distributors worldwide with national service provided by Bell & Howell. Call for the name of the dealer in your area. Let us show you a whole new world of performance and value.

COLUMBIA DATA PRODUCTS, INC.
QIC compatibility (continued from page 48)

Viewed as a layered shell, compatibility among QIC-02 drives becomes easier to discern. Basic commands offer full compatibility, with vendor-unique commands offering no compatibility.

commands will be supported, several vendors have chosen the same commands to augment the standard set. Archive, Cipher Data Products, and Tandberg Data, as well as Wangtek (Culver City, Calif), claim they will support those commands that enhance streaming operations. The WRITE WITHOUT UNDERRUNS command allows the tape drive to continue streaming even if data from the host are momentarily interrupted. Redundant data are written until new information is sent. The READ N FILE MARKS and WRITE N FILE MARKS help reduce the number of commands the host issues. SEEK EOD (end of data) provides a means to get past the last record and continue streaming. As multiple vendors augment the standard commands with these optional commands, a de facto standard emerges.

Otherwise, vendors are following no real pattern in implementing optional commands. Both Archive and Cipher Data Products will support a self-test instruction, but will use proprietary diagnostics. Tandberg Data will support all optional commands, while Data Electronics will not implement any. Designers should, therefore, carefully match application requirements with the capabilities of the standard and optional command sets. Multiple sources may be required for drives that implement desired optional commands.

Tape controllers face a similar dilemma. All QIC-02 controllers must support the standard command set, but have the flexibility to support a portion or all of the optional set. Key to this is the involvement of the controller in translating host system commands into drive commands.

For firmware based controllers, such as the Gypsy from ADES (Pomona, Calif), implementing all or part of the optional set requires considerable modification of the microcode responsible for interpreting system calls. Also, the variety of ways that optional commands are implemented on different drives places an enormous burden on the controller to keep track of possible differences. The company has bypassed these concerns by only supporting the standard commands.

For example, Mike Newton, engineering manager with Data Electronics (San Diego, Calif), says that reading a 4-track cartridge with a 9-track head can cause problems because of the different signal amplitudes needed. Background noise can also hamper reading tapes made on different drives due to varying erasure techniques. According to Newton, half-inch tape drives encounter problems even with the IBM 9-track format. Competing drives may be compatible with IBM drives, but not with each other.

Without the frames of reference available with half-inch tape drives, Wangtek Engineering Manager Jerry Fuchs says that it will be interesting to see which vendor will make changes when one drive cannot read a cartridge made on another. Newton believes that a spirit of informal cooperation among vendors will iron out differences.

(continued on page 56)
Lundy computer graphics maintenance always generates a very reassuring picture for you and your company.

The Lundy service network offers you 4 types of service, over 40 service locations, 6 maintenance depots, over 130 service personnel, plus a special backup service team consisting of over 30 trouble shooters.

Lundy computer graphics terminals, workstations and rack-mounted generators have earned a well-deserved reputation for reliability. But if a problem does arise, you want service—and you want it now. Lundy delivers.

Service tailored to your requirements.

Lundy offers you a choice of four types of service:

1. Network Service. We assign highly trained personnel from over 40 service locations nationwide. Available service options include: on-call, on-site or time and material.

2. Backup Service. To guarantee that even the most difficult problem finds its solution, we maintain a special troubleshooting team. Sixteen engineers and 15 technical specialists are available to help our customers anywhere.

3. Customized Service. If your particular operation calls for special service requirements, we sit down with your people to discuss and analyze your precise needs. Then we plan a program that meets those needs.

4. Depot Service. This service covers instances when it is impractical to repair equipment on site. Equipment is shipped to one of the nearest 6 maintenance depots for immediate attention.

Whichever type of service is best for you, you can count on our trained and experienced servicemen. And their training is constantly updated by a series of Training Refresh Seminars held at regular intervals at our service centers.

We’ll help you see more in graphics.

When you take a close look at our graphics terminals, service, support, software, systems capability, enhancements—and our company—you’ll understand why Lundy can help you see more in graphics now and in the long term.

For more information, write Lundy Electronics & Systems, Inc., Glen Head, New York 11545, or call: (516) 671-9000.
QIC compatibility
(continued from page 54)

It should be emphasized that the QIC-02 and QIC-24 proposals complement each other, but do not require each other for implementation. The QIC-02 interface can support existing formats from Archive, Cipher Data Products, Data Electronics, and Tandberg Data. The QIC-24 format can be used with separate interfaces from Control Data (Minneapolis, Minn), Kennedy Co, (Monrovia, Calif), and 3M (St. Paul, Minn) as well. However, neither standard has allowed room for such developments as 3M's drive that uses a 600' (183-m) cartridge with 16 tracks. New standards will be needed as such developments gain industry acceptance.

—Joseph Aseo, Field Editor

Onboard cache memory

Tying main memory with its own high speed cache, the High Density Memory with Cache (HDMC) memory board from Systems Group accelerates data transfers in Multibus systems. The 2K x 16-bit static RAM array (35-ns access time) handles about 85% of the read operations, with the slower 256K x 22-bit dynamic RAM array (200 ns) used to store seldom accessed data. Data are transferred on a byte or word (16-bit) basis.

Using a modular cache configuration also overcomes problems associated with fixed-size caches in conventional systems. In these systems, performance typically degrades as large amounts of main memory are added. Perhaps more critical, a hardware failure in the cache RAM shuts down the entire system because such memory is typically located with the CPU.

In contrast, the HDMC expands the size of the cache RAM as main memory is added. This ensures that system cache performance is maintained. Fatal system errors do not occur since hardware failures on a memory board have no direct impact on the CPU.

Designed to minimize system overhead, the memory board uses address and data latches during write operations to free the processor. The remainder of the write operation is handled onboard, enabling the processor to supervise other system tasks. Furthermore, no wait states are imposed on the processor for precharging the dynamic RAMs between write operations. This task is also handled onboard as part of the write cycle.

Data transfers are further reduced for Multibus systems if designers take advantage of the board's dual-ported architecture. An onboard bus (plus bus) can be used to support separate processors on each board. Use of the Multibus could then be limited to interprocessor communications. Bus arbitration logic is included to handle competing requests from either bus on a first-come, first-served basis. Requests occurring while the internal bus is active must wait. As a result, redundant multiprocessor architectures can be realized without resorting to custom hardware.

If applications only require a single bus, the bus arbitration logic can be defeated and data transfers accelerated even further. Read access times are reduced from 70 to 20 ns through the elimination of arbitration delays.

The modular cache does not require software drivers to maintain it. In fact, cache operations are transparent to the rest of the system. The CPU merely issues read/write commands. During write operations, data are written directly to main memory and the cache simultaneously. Onboard hardware logic arbitrates between accesses to main memory and the cache during read operations.

Implementing a write-through algorithm eliminates software overhead because it does not require the cache to be cleared each time a miss occurs. The clearing algorithms typically cause considerable system overhead in RAM-intensive applications implemented on multiple port systems, according to the company. Assuming that the most recently written data are the most accessed simplifies cache updates so that they merely write over old data as misses occur. Seldom accessed data still reside in main memory. The cache is kept current because the first read request after a write operation always guarantees a miss.

Complementing the write-through algorithm is a cache tag scheme similar to the scheme found on systems from Texas Instruments (Dallas, Tex) and Charles River Data Systems (Natick, Mass). Main memory is now organized into 128 pages, each the same size as the cache memory. The upper address bits (A12 to A20) uniquely identify each page. The lower address bits (A0 to A10) describe locations within each 2K x 16-bit boundary.

When a 22-bit address is passed during a read operation, the upper address bits are sent to a tag comparator, while the lower address bits are used to determine the location in cache memory. While data are being read out on the data bus, the upper address bits are compared with the upper address bits stored in the cache address tag RAM. The addresses in the tag RAM are stored during the write operation that places data in the main memory. If the two addresses match, a cache hit occurs and the cycle ends after 70 ns.

A cache miss occurs when the address stored in the cache tag RAM does not match the upper address bits passed during the read operation. Control logic then initiates a data transfer from main memory. Both the cache RAM and its tag RAM are updated simultaneously by writing over those locations where the miss occurs. The total time required to handle a cache miss is 430 ns. Besides handling cache and dynamic RAM, the control logic (continued on page 58)
Multiwire permits greater component densities with fewer signal levels. Using polyimide-insulated wire to form interconnections, Multiwire boards accommodate component densities of 2.0 IC's per in² and greater.

Multiwire delivers better electrical performance. Our boards outperform multilayer in all applications requiring tight-tolerance on impedance controlled transmission lines.

Multiwire shortens the design cycle by weeks. We can design your board from as little input as a schematic or net list, reducing your in-house design time. And when you make revisions, you'll get new boards back in days instead of weeks.

Revising Multiwire designs costs thousands less. Instead of redrawing costly artmasters, we just key the change into our computer.

Introducing our Advanced Manufacturing Group. Multiwire technology provides the most advanced circuit boards. But sometimes even our leading edge designs are not enough for your requirements.

That's why Multiwire has established the Advanced Manufacturing Group—a new facility with design and manufacturing specialists dedicated to solving the interconnection problems for your next generation of products. To learn more, just fill out and return the coupon.
IMMOBILIZES
PARTICLES
PERMANENTLY

Vacuum-deposited Parylene coating ties down microscopic particles permanently.
- Protect disk drives from lost data, head crashes
- Super thin (down to .004-mil) transparent coating resists abrasion, moisture, chemicals, lubricants
- Ideal for castings, actuator magnets, ferrites, PC boards, magnetic shaft seals.

Nova Tran has the key to ultra-long disk drive MTBF performance. Call for details on economical application engineering and production services.

NOVA TRAN CORPORATION,
100 Deposition Drive
Clear Lake, WI 54005
715/263-2333
TELEX 29-0220

CIRCLE 40

Again this year, many of FORTUNE'S 500 will hire many of DeVRY'S 5000.

It makes sense. From campuses throughout the U.S. and Canada, DeVry graduates in Electronics and Business oriented Computer Science measure up to their specs. And the reasons why they do, make sense, too.

See how well our grads can meet your needs—now and in the future. Call or write for your Free booklet on Hiring Technical Graduates.

DEVRY INSTITUTE OF TECHNOLOGY
BELL & HOWELL EDUCATION GROUP
2201 W. Howard St., Evanston, IL 60202
Write or Call
(800) 228-8000
for your Free Booklet on Hiring Technical Graduates.
Ask for Mike Bouman.
In Illinois, call (312) 328-8100.
In Canada, call (416) 741-9200.
Ask for Dex Walker.

SYSTEM TECHNOLOGY/
MEMORY SYSTEMS

Onboard cache memory (continued from page 56)
generates support timing for the dynamic RAMs and also generates the acknowledge to the requesting bus.

The memory board ensures high data reliability by featuring a hardware error detection and correction unit. This unit generates 6 syndrome bits for each 16-bit data word written into main memory (dynamic RAMs are 22 bits wide). During read operations, the error correction code (ECC) logic corrects single-bit errors and flags double-bit errors as the syndrome bits are decoded. Initialization logic fills the dynamic RAMs with valid ECC information before the first read access on power-up, and inhibits access until the operation is finished. Initialization allows the board to be used without modifying system software and gives the system the benefit of power monitoring.

Since the cache handles most read operations, dynamic RAM refresh can occur simultaneously with them. The refresh operations are postponed if a read access to dynamic RAM is needed. However, processor wait states are imposed if a read access occurs while a refresh operation is in progress.

The dynamic RAM arrays are expandable to 2M bytes when 256K-bit RAM chips are available. Addressing and control logic were designed with this expansion in mind by providing a 22-bit address space. Information on the HDMC's price and availability is obtainable upon request. Systems Group, a div of Measurement Systems and Controls, 1601 Orangewood Ave, Orange, CA 92668.

Circle 243

July Preview—
Watch for a major staff-written review on workstations for computer aided engineering.
HP's 5180A...the Waveform Recorder for bench and ATE.

From now on, your waveforms have few secrets.

Now, those difficult time, amplitude, and frequency measurements of repetitive and transient signals needn't be a problem. Because HP's 5180A Waveform Recorder lets very few signals escape detection. And it reveals your captured waveform's important characteristics. The reason? It combines the features you need for reliable signal capture, accurate digitizing, and fast processing.

For example, flexible digital triggering snares those hard-to-capture random transients. You get the entire signal, single shot, from the 5180A's 10 bit resolution, 20 MHz ADC. And a 16k-word memory gives you lots of storage for complex events. The 5180A also delivers exceptional dynamic performance, which means accurate results. That's important in tasks such as frequency domain analysis where your results must be reformatted. And DMA (Direct Memory Access) means fast data transfer to a computer for rapid signal processing.

Your solution for benchtop or system use.

As an integral part of your custom automatic test system, the HP 5180A, is the first in a new generation of universal waveform recorders. All front-panel controls are accessible via HP-IB. Measurements stored in memory can be read out in either ASCII or binary format, or transferred at up to 1 Mword/sec via DMA. Combined with an HP Series 200 desktop computer, the HP 5180A forms the core of a very powerful and versatile waveform capture and analysis system.

In benchtop applications, simply attach an HP 1332A display and you have a powerful, stand-alone test instrument. For truly impressive hardcopy output, connect a digital plotter such as the HP 7470A directly to the built-in HP-IB port for fully annotated plots.

In either environment, the 5180A can do the job of several instruments, saving you cost and complexity.

Can the 5180A handle your difficult measurements?

In disc drive testing, the 5180A's 16k memory can capture an entire sector of data.

You can use the 5180A's bi-level trigger to capture DC-erased drop-outs. And an external timebase input allows compensation of data to capture long events or equivalent time sampling of repetitive signals up to 70 MHz. In the video world, post trigger delay lets you capture a specific line in a frame. And 40 MHz bandwidth means there's no phase distortion. For VCO testing, the 5180A provides a dual timebase for measuring both settling time and post tuning drift in a single record. Have you ever needed to strip off the AM and FM modulation from a single radar pulse? With the 5180A you can do it. In fact, this waveform recorder is built to handle a host of difficult measurements, including power-supply characterization, radar IF processing, laser pulse measurements, and many more.

HP has the support you need for those critical applications. A large and growing library of contributed software is available to you, including 1 second Fast-Fourier Transform (1K record) and DMA routines. In addition, each HP 5180A, like every HP product, is backed by our worldwide service and systems engineering staff.

Want more information?

Contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department, and request a copy of our full color data sheet.
Why make the Wyse decision?

IF COLOR IS A LUXURY YOU THINK YOU CAN’T AFFORD, THINK ABOUT OUR WY300—the smart color terminal as low as $975.

The WY300’s high-resolution 8-color display adds vivid relief to any text editing or data entry task, without adding significantly to the price you’d pay for monochrome.

*Quantity 100
Ergonomically designed with a swivel and tilt CRT and a detachable keyboard, the compact WY300 fits into the workplace as comfortably as it does into your budget.

On top of that, the WY300 gives you a host of features like a soft downloadable character generator, extensive alphanumeric and line drawing symbols, and compatibility with most standard, monochrome oriented, off-the-shelf software.

Best of all, the WY300 is plug compatible with our monochromatic WY100’s and most ASCII terminals. So, using color is as easy as it is inexpensive.

Need more information? Call or write us today. We’d like to convince you our smart color terminal is your wisest buy.

WYSE TECHNOLOGY, 3040 N. First St., San Jose CA 95134, 408/946-3075, TLX 910-338-2251, in the ent. call 516/293-5063, call toll free 800/538-8157, ext. 932, in CA, 800/672-3470, ext. 932.
Presenting StacPac™ systems and modules.

This is a brand new deal for systems integrators. StacPac systems and modules. Modular storage and backplane units that stand alone or stack together to form the basis of a small but powerful tabletop computer.

They’re available in either DEC® or Multibus® compatible versions. And there are lots of advantages to both.

On the DEC side, you can put a StacPac system in places a rack-mount just doesn’t fit.

On the Multibus side, you can use our StacPac system to deliver serious minicomputer performance with microcomputer economy.

Either way you get greater flexibility to configure just the right system. And the easy upgradability to expand it whenever you like.

But perhaps one of the most important advantages is that you can protect your software investment—and your customers—because inside, you’re still selling the same system. You’d just never know it to look at it.

Which brings up another point. Underneath that slick, compact exterior is the very latest in storage technology. 8” slimline floppy drives. High capacity, highly reliable 8” Winchesters. Compact ¼” cartridge tape drives. And the best high performance controllers in the business. (Packaged systems are also available without controllers at your option.)

And if you’re thinking about 5¼” storage, there’s our 5¼” Winchester/floppy module. (Available in the Spring of 1983.)

Configuring an elegant system solution is a simple matter of picking out the storage option you want and adding your own CPU boards, I/O and memory to our uncommonly accommodating backplane units.

Naturally, we back it all up with HyperDiagnostics™, Rapid Module Exchange™ and HyperService™. Some of the most economical and intelligent service features ever devised.

And you can have more information about StacPac modules just by writing for our brochure.

But you just watch. You start marketing your systems in our StacPac modules and your competition will say you have an unfair advantage.

And you know something? They’ll be right.

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. Eastern Region Sales and Service: Norwood, MA, (617) 769-7620. Central Region Sales and Service: Dallas, TX, (214) 980-4884. Western Region Sales: Santa Clara, CA, (408) 727-3163.
Components make systems fault tolerant

Fault tolerance requires duplication of processors, interconnections, and memory arrays. Intel's FRC configuration (a), which preserves computation results while halting processing, uses two complete sets of system elements. QMR (b), which provides automatic transparent error detection and correction, requires four complete sets.

Two added components in Intel's Micromainframe family—the iAPX 43204 bus interface unit (BIU) and the iAPX 43205 memory control unit (MCU)—provide the switching and interface circuitry needed to build fault-tolerant multiprocessor systems. The units combine to replace entire boards of discrete components that are normally needed to detect failures and must switch to a redundant processor, bus, or memory. All fault detection and recovery functions are transparent to the application software.

System configurations can range from partial fault tolerance with functional redundancy checking (FRC) to complete fault tolerance with quad modular redundancy (QMR).

An FRC system consists of a master general data processor (GDP), which handles normal processing; a redundant "checker" GDP, which runs parallel to the master and can take over processing at any time; two or more BIUs, which connect to GDP's local bus to parallel, redundant system master buses; and two MCUs per memory array, which check each other, correct errors, and connect to the system master bus. Each GDP consists of a 43201 instruction decode unit, a 43202 microexecution unit, and a 43203 interface processor that maintains communication with I/O subsystems.

The FRC configuration requires twice the number of GDPs and control circuits as a minimum functional iAPX 432 system does, while the QMR configuration requires four times the number of GDPs. Both redundant systems depend on the functions provided by the BIU and MCU devices.

BIU is a switch that accepts access requests from the GDP and, based on the physical address, decides which memory or buses will be used. BIUs also arbitrate bus contention among the several GDPs that can be part of a system.

A QMR system is essentially two FRC systems running in parallel—each GDP, BIU, MCU, and memory array has a "shadow" backup ready to take over instantly in case of trouble. Fault detection and a disabled, failed GDP or memory array are transparent to both application and system software, although the system software is notified after the recovery is complete that a failure has occurred.

A QMR system consists of two FRC systems in parallel—each GDP, BIU, MCU, and memory array is a redundant pair. Fault detection and a disabled, failed GDP or memory array are transparent to both application and system software, although the system software is notified after the recovery is complete that a failure has occurred.

The FRC configuration requires twice the number of GDPs and control circuits as a minimum functional iAPX 432 system does, while the QMR configuration requires four times the number of GDPs. Both redundant systems depend on the functions provided by the BIU and MCU devices.

BIU is a switch that accepts access requests from the GDP and, based on the physical address, decides which memory or buses will be used. BIUs also arbitrate bus contention among the several GDPs that can be part of a system.

An MCU interfaces memory arrays to the system master bus. These arrays can consist of all types of RAM components, even partially failed ones. The MCU treats memory as 32 data bits, 7 bits of error correcting code, and 1 spare bit. It (continued on page 66)
Now, a Logic Analysis System that puts a bench-full of instruments at your fingertips.

The NPC-764. It just makes good sense. When performing logic analysis and other measurement functions, you shouldn't have to face different sets of knobs, switches and dials. That's why we've developed the NPC-764, the Electronic Workbench. Now your analysis tasks are all done the same way—with a familiar ASCII keyboard and easy-to-use, self-prompting menus. Simple keystrokes are all it takes to run tests and record data on disk. And all logic analysis and other internal functions are ROM-based and ready to go on power up. No messy setups. No relearning of multiple instruments.

The NPC-764 includes a 48-channel State Analyzer and a 16-channel, high-speed Timing Analyzer. And, as optional plug-ins, a single-channel Digital Storage Oscilloscope, a 5-function Counter-Timer/Signature Analyzer, and bidirectional Serial Tester.

But the NPC-764 is more than just a multiple-function instrument. It also incorporates a GPIB controller and RS-232 MASTER/SLAVE capability. Standard. A common set of commands lets you control the internal analyzers and any GPIB- or RS-232-compatible devices you include in your setup—pattern generators, emulators, spectrum analyzers, PROM programmers . . .

And that's not all. The NPC-764 is a full desk-top computer, with floppy disk storage and a CP/M® operating system. Use it for general-purpose computational tasks or the execution of commercially available CP/M programs.

The NPC-764, with all its internal measurement functions, requires less than half the investment of the equivalent instruments purchased separately. And the ASCII keyboard and menus are so user friendly it sets a new standard for the industry.

Not quite ready for all this capability? Start with our basic NPC-748. It provides exactly the same measurement functions, but 16 fewer state channels and no floppy disk drive. Upgrade easily to the NPC-764 at any time.

There's a whole lot more we'd like to tell you about the Electronic Workbench. For additional information, applications assistance or a personal demonstration, just give us a call: (800) NICOLET, (415) 490-8300 (Calif); TWX: 910-381-7030. Nicolet Paratronics Corporation, 201 Fourier Avenue, Fremont, CA 94539.

*CP/M is a registered trademark of Digital Research.
Fault-tolerant systems
(continued from page 64)
automatically refreshes dynamic RAM arrays and scrubs single-bit errors as a background task. Further, only a modest amount of external logic is required to interface the MCU to the storage array RAMs.

The iAPX 432 is designed for large scale realtime control and transaction processing systems. Both the BIU and the MCU will be generally available the second half of this year. In quantities of 100, the BIU is priced at $262.50 and the MCU at $497.50.

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 244

Data communications

Data and voice share wire
Reducing the need to rewire buildings, data-over-voice multiplexing schemes piggyback data atop voice on existing twisted-pair telephone wire. These techniques offer an alternative to local area networks that depend on costly coaxial cable as well as digital voice/data private branch exchanges (PBXs).

Data-over-voice techniques are well suited for large facilities such as college campuses and high-rise office buildings needing to upgrade their data handling capabilities. Typically, these sites already have an extensive investment in PBXs and voice-grade telephone lines. Such facilities would have difficulty installing coaxial cable to handle local area networks, such as Ethernet, because of cost and duct capacity. Likewise, voice/data PBXs that digitize voice may not be economically feasible if present voice-only PBXs can be modified to handle data via data-over-voice multiplexing.

Several products are now available to meet these needs. Micom Systems, Inc (Chatsworth, Calif) and Teltone Corp (Kirkland, Wash) address the need for intrabuilding communications with carrier systems capable of handling data rates up to 19.2k bps at a range approaching one mile. Interbuilding communications for a total distance approaching three miles is handled with the Line Miser system from Gandalf Data, Inc (Wheeling, Il). Distances exceeding three miles are handled with the narrowband model 6860 Speech Plus system from RFL Industries, Inc (Boonton, NJ).

All of these systems use frequency division multiplexing to create data channels on top of (or within) the voice band that extends from 0 Hz to 4 kHz. Like Micom's Instalink460, these systems all exploit the minimal signal losses and fairly wide bandwidth of twisted-pair wire. According to Micom, signal losses increase linearly with frequency to nearly (continued on page 68)
Our Past Is Your Future

Ikegami Technology

For systems applications requiring high quality, dependable CRT display monitors, Ikegami brings you the technology of the future, today. An innovator in video technology for over 36 years and the world's leading producer of high quality broadcast camera systems and monitors, Ikegami has applied its unparalleled experience to the design and production of display monitors for the computer industry. Put Ikegami's Emmy award-winning digital techniques for automatic setup to work for you.

HDM Series

Ultra high resolution for your most demanding graphics systems. Ikegami's HDM Series color and monochrome display monitors utilize a delta-gun, raster-scan CRT and superb quality wide band, high speed scan, video amplifiers to provide the precision you need (up to 1280 x 1024 pixels interlace mode), plus the long life and easy maintenance you demand from a top quality graphics display. Available in 19V and 25V CRT sizes.

The CD Series (CDA/CDB)

Quickly becoming our most popular line of high resolution in-line gun color CRT display monitors. If your requirements are for high resolution (up to 1024 x 1024 pixels interface mode), stable operation and very low maintenance, the CD Series may be your solution. Available in 13V and 19V analog or digital models, the compact-size CD Series is perfect for simulation, medical, CAD/CAM and other high resolution applications.

The UD Series

Medium resolution, digital drive, color display monitors for business graphics systems. The Ikegami UD Series provides high performance (615 x 240 or more pixels interface mode) at a very economical price.

The BDM Series

High performance, flicker-free monochrome CRT display units that bring Ikegami quality to word processing or on-line data entry systems. Available in green or white display and standard CRT sizes (5", 9", 12", 14" and 15").

Easy Interface. Easy Maintenance.

Ikegami display monitors are designed to interface with your equipment, quickly and easily. There's no complex rework ... no hassle. Ikegami's sophisticated design virtually eliminates maintenance problems, so you know your Ikegami displays will continue to bring out the best in your systems, year after year.

For more information on high-performance CRT display units designed to meet your needs, today and tomorrow, write or call Ikegami today.

We are the future.

CIRCLE 47
Data-over-voice
(continued from page 66)

The Instalink46t terminal unit uses short haul modem techniques to create two data channels above the voice frequency for full-duplex transmission. An M464t central unit splits off the data signals so that voice signals can be routed to the PBX.

1 MHz. This provides a comfortable margin for the 200-kHz bandwidth used with the Instalink460. Extraneous noise, such as channel crosstalk, is minimized because twisted-pair wire acts as a balanced carrier. The only noise encountered comes primarily from other data channels operating at the same frequencies.

The Micom system transmits data from a terminal to the computer between 160 and 178 kHz and receives data from the computer between 68 and 76 kHz. With phase-coherent frequency shift keying schemes, asynchronous full-duplex transmissions up to 19.2 kbps are achieved.

Teltone's DCS-2 carrier system (Computer Design, May 1982, p 68) implements its data channels at much lower frequencies. Remote station units transmit data between 36 and 40 kHz, and receive data between 72 and 80 kHz. As a result, full-duplex asynchronous transmissions are reduced to 9600 bps. The Teltone and Micom systems both claim an operating range of 5000 cable-feet from terminal to PBX wire center or computer center.

Using 24-gauge wire typically found between central offices and customer sites, Gandalf Data extends the range of its carrier scheme to almost 18,000 cable-feet. Asynchronous or synchronous full-duplex transmissions occur at 9600 bps.

The Line Miser transmits data from the remote terminal between 48 and 36 kHz, with data received between 84 and 96 kHz. According to a Teltone engineer, Malcolm Klug, these longer distances are possible due to lower attenuation with the thicker 24-gauge wire. Both the Teltone and Micom systems are geared to handle the thinner 26-gauge wire usually found in PBX-to-telephone systems.

However, all of these systems terminate at the voice PBX in the same manner. A central unit removes the data from the line prior to arrival at the PBX or outside telephone system. In fact, telephone lines usually terminate at a large distribution frame rather than at the switchboard itself. At this point, voice and data signals separate through frequency splitting and voice lines reconnect to the PBX side of the distribution frame. Data lines are routed either directly to computer ports, to a data PBX to gain access to multiple host computers, or to a high speed multiplexer for transport to a remote site.

Due to the separation of voice and data transmissions, normal telephone and PBX operations (e.g., ringing and dialing) do not hinder the data carrier system. Although ringing and hook transients cross into the data frequencies, extensive filtering reduces signal levels well below these systems' signal-to-noise thresholds (e.g., -55 dB for the Line Miser). Klug notes that most noise problems occur when strong signals going from the terminal to the host encroach on weaker signals going from the host to the terminal.

Thus, the operating frequencies selected to implement the data channels must temper the transmission speeds and distances traveled. Higher speeds and longer distances require more extensive filtering and signal extraction schemes, according to Klug. Distances exceeding 18,000 cable-feet are impossible to implement with wideband techniques. Such is the case because, in order to improve voice quality, telephone companies place inductance coils on the lines.

Narrowband techniques operating within the voice range overcome this barrier. The RFL Speech Plus carrier system shifts the voice band upward from 1.2 to 2.35 kHz to between 2.15 to 3.4 kHz. The voice band from 300 to 830 Hz remains unchanged. Voice compression creates a single 600-Hz data channel (830 to 2150 Hz) that allows 1200-bps half-duplex asynchronous transmissions. Previous implementations only allowed 600-bps transmissions.

Apart from narrowband multiplexing, the Speech Plus system operates like the others. Data signals split off from the voice line for routing to a computer, data
IBM Compatible
3200 bpi Tape...the
new standard for high
capacity disk backup.

CacheTape
Improves System Performance—
with 92 MB of Winchester Backup.

3200 bpi—
A New Tape Standard

With the announcement by many
computer manufacturers of the availability
of 1600/3200 bpi tape drives, the primary
requirement (a large user base) for standardi-
dization exists. Why 3200 bpi? The choices
in tape density until now have been 1600
bpi tape (46 MB) or expensive 6250 bpi
tape (180 MB). The new choice is 3200 bpi
tape with 92 MB capacity at a low incremen-
tal price ($375) to the standard 1600
bpi tape drive. Substantially less expensive
than 6250 bpi with better performance in
most applications, Cipher's CacheTape also
offers the added benefit of standardization.

Start/Stop Performance

CacheTape provides superior perfor-
mance versus tension arm, vacuum column,
100/25 ips streaming, and 50 ips 6250 bpi
(GCR) tape drives. As an example, the fol-
lowing benchmark comparison provides
typical performance data for a file-oriented
backup application:

<table>
<thead>
<tr>
<th>Benchmark Time*</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Streaming Tape (variable speed, 1600 bpi)</td>
<td>23 min.</td>
</tr>
<tr>
<td>Vacuum Column (125 ips, 1600 bpi)</td>
<td>7 min.</td>
</tr>
<tr>
<td>CacheTape Model 891 (1600 bpi)</td>
<td>7 min.</td>
</tr>
<tr>
<td>CacheTape Model 891 (1600/3200 bpi)</td>
<td>6.4 min.</td>
</tr>
<tr>
<td>CacheTape Model 891 (3200 bpi)</td>
<td>5.9 min.</td>
</tr>
</tbody>
</table>

*Benchmark measured on a DEC PDP-11/34 under RSTS** for
available tape drives.

**OEM Quantities

For higher capacity disk backup, 3200
bpi density offers 184 MB of disk backup
with only one reel change.
CacheTape offers field-proven stream-
ing mechanics, fully automatic loading and
threading, and compact package size...and
still performs disk backup and transactional
applications as well. CacheTape is the total
solution to your tape drive needs.

Call or write for a free benchmark
brochure that explains the performance
advantages and how to calculate in
advance the benefits of CacheTape.

Software Transparent

Cipher's CacheTape products are com-
pletely software transparent with current:
vacuum column or tension arm start/stop
tape software. CacheTape provides start/stop
tape performance for tape applications
such as file-oriented disk backup, trans-
actional journaling, tape sort/merge,
and data acquisition. Utilization of a cache
memory in the tape drive means that CacheTape
can provide higher performance than exist-
ing tension arm or vacuum column tape
drives at much less cost. Just plug
CacheTape into your system now...and
benefit from total software compatibility.

Up to 40% Less Cost

CacheTape Model 891
(with 1600 bpi) ....................... $3420**
CacheTape Model 891
(with 1600/3200 bpi) ............... $3795**
versus 125 ips vacuum column .... $6100
versus 50 ips 6250 bpi (GCR) ........ $7000
(estimated)

UNIX Friendly

UNIX™—the emerging operating system
of the 80s—now has with CacheTape an
easily integrated, low cost, standard tape
drive with superior performance. Do other
alternatives make sense anymore...particularly if software development time
and resources are scarce?

CacheTape
with 3200 bpi...
the new standard
• Up to 40% less cost • Tape adapter
compatibility • Software transparent
• Superior performance • UNIX friendly
Available Now

Cipher Goes Beyond

Cipher
data products, inc.

CIPHER DATA PRODUCTS (UK) LTD.
Camberley, Surrey, England
Telephone: 0276-682912
Telex: 858329

CIPHER DATA PRODUCTS GmbH
Munich, West Germany
Telephone: (089) 578-9100, TWX: 910-335-1251

CIPHER DATA PRODUCTS GmbH
Paris, France
Telephone: (1) 668 87 87
Telex: 203935

CIPHER DATA PRODUCTS S.A.R.L.
Paris, France
Telephone: (1) 668 87 87
Telex: 203935

10225 Willow Creek Road, P.O. Box 85170, San Diego, California 92138
Telephone: (619) 578-9100, TWX: 910-335-1251

CIRCLE 48
Data-over-voice
(continued from page 68)
multiplexer, or data PBX. To aid in normal PBX operations, the control signals on the voice line are retained. System designers considering data-over-voice implementations should evaluate the different products' advantages and disadvantages. For instance, the total cable distance traveled must be balanced against required transmission speeds and overall cost. Configuration and pricing information are available from the manufacturers.
—Joseph Aseo, Field Editor

MICROPROCESSORS/MICROCOMPUTERS

Z80 code expands into large systems

The Z816, a full-feature member of the Z800 family, incorporates four DMA channels, four counter/timers, and 24 bits of address space with memory management. The CPU is fully compatible with the Z80 instruction set and supports additional instructions.

An 8-bit Z80 compatible microprocessor with onchip memory management and peripherals expands Z80 code into the world of higher performance systems. Zilog's Z800 can address 16M bytes of memory and execute code at 1M to 5M instructions/s depending on the data bus width. The microprocessor supports all documented Z80 opcodes and runs all Z80 programs with the proviso that existing timing loops may have to be adjusted to accommodate the Z800's faster execution speed. The system provides Z80 software a migration path into higher performance systems using the latest 16-bit peripherals. It also includes large address spaces and enhanced microprocessor capabilities for advanced designs.

Actually, the processor comprises a family of four chips: the Z8108 and Z8208 support 8- and 16-bit non-multiplexed bus peripherals, respectively, and the Z8116 and Z8216 support Z-Bus multiplexed 16-bit peripherals that are also used with the Z8000. The family is further divided into two package sizes—a 40-pin (Z8108 and Z8116) and a 64-pin (Z8208 and Z8216). Both 40-pin packages are limited to 19 bits of address space and do not support the onchip peripheral. The 64-pin versions support all 24 bits of address and onchip peripherals including one onchip UART, three counter/timers, one timer, dynamic memory refresh circuitry, and four DMA channels.

An onchip memory management unit (MMU) divides the 64K-byte logical address space manipulated by Z80 programs into pages. It then maps these pages into the Z800's larger physical address space. Depending on whether or not the Z800's program/data separation is enabled, these pages are either 8k or 4k bytes in length. Using this technique, 16-bit logical addresses are translated into 24-bit physical addresses for the Z8208 and Z8216, or into 19-bit physical addresses for the Z8108 and Z8116.

Memory management techniques used by the Z800 allow system and user modes of operation and also the separation of programs and data. Address translation, which can be done in both system and user modes, can also be done so that instruction references are separated from data references. This separation allows programs up to 64K bytes long to manipulate up to 64K bytes of data without operating system intervention.

Including different types of commonly used peripherals onchip reduces system cost and design complexity. In addition to the peripherals mentioned, all family members contain an onchip oscillator/clock generator and programmable refresh circuitry for dynamic memories. All onchip peripherals lie in standard Z80/'I/O address space and can be accessed by Z80/'I/O instructions. In addition, some of the (continued on page 72)
AYCON 16/SERIES

brings high performance color graphics down to earth.

Only AYDIN CONTROLS' 15 years of experience in raster scan color graphics could bring you a display computer with the total capability of the AYCON 16/SERIES...and now at such an affordable price!

The overwhelming acceptance of the AYDIN original Model 5216 allows us to offer an enhanced version of this field-proven unit. Check this unmatched combination of systems/hardware features available with the AYCON 16/SERIES:

- Up to 1024 x 1024 pixel x 16 bit (Z-axis) color display.
- Refresh at up to 60Hz.
- A variety of video modules.
- Characters in three sizes.
- Vectors at 800 ns per pixel.
- 80 x 48 character A/N overlay.
- Multiple 16-bit micro's. AYDIN software or you program them... even up to 14!
- Single or multiple WORKSTATIONS...up to four!
- High-resolution RGB monitors - delta or in-line gun.
- Graphics Firmware with fill and zoom standard!
- AYGRAF/CORE 2-dimensional Firmware/Software with World-to-Screen translation, rotation, and scaling...world coordinates of 64K x 64K!
- Plus AYGRAF/3D, AYGRAF/LIST, and support Software.

But if all this is not enough to excite you, how about more economy with standard PACKAGED SYSTEMS, single or multiple WORKSTATION pre-engineered for the most common color display applications?

If you're ready to fly with your color graphics display application, we can help you "get off the ground" with a system to meet your industrial, business, scientific or commercial requirements.

Aydin Controls
Command Performance in Color Graphics
414 Commerce Drive, Fort Washington, PA 19034 (215) 542-7800, TWX: 510-661-0518 Telex: 6851057

See us at NCGA Booth #s 2049, 2050, 2146-2148 & 2150

CIRCLE 49
Embedded EEPROM is reprogrammed in-circuit

The Seeq 72720 self-adaptive microcomputer addresses applications requiring remote programming ability. These applications include robotics, learning machines, laboratory instruments, and maintenance diagnostic equipment. This microcomputer is also designed for applications requiring nonvolatile memory that can be erased and programmed without removal from the system.

One of the advantages of embedding nonvolatile electrically erasable read only memory (EEPROM) onboard single-chip microcomputers is that the EEPROM can be erased and reprogrammed without removal from the system. Although not frequently valuable because the reprogramming procedure is still slow, this feature will become much more important as procedure time diminishes. The first such devices will result from an agreement between Seeq Technology, Inc, and Texas Instruments to apply Seeq's EEPROM technology to TI's TMS7000 family of 8-bit single-chip microcomputers.

Under the terms of the agreement, Seeq will develop versions of the TMS7000 using a 2K x 8-bit 5-V only EEPROM in place of TI's standard ROM. Several different family members will be produced with the integrated EEPROM, providing a range of capabilities. Seeq will then make available the resulting integrated microcomputer packages to TI starting in 1984. The first part to be produced, a 72720 self-adaptive microcomputer, is targeted for applications that require remote programming ability.

Functionally and electrically inter-changeable with the TMS7020, the Seeq 72720 includes an additional program instruction that allows the device to program and alter its own nonvolatile EEPROM. It also has an additional 128 bytes of internal RAM for a total of 256 bytes. Additional registers and control logic forbid external access to the internal program memory after the stored program has been verified and execution has begun.

(continued on page 74)
VISUAL 300/330.
Excellence in Ergonomics, Emulations and Economics.

Both the VISUAL 300 and VISUAL 330 combine VISUAL ergonomic elegance with excellent emulation capability.

For example, the VISUAL 300 complies to the ANSI X3.64 standard and is protocol-compatible with DEC VT100/VT52® terminals. And the VISUAL 330 emulates the DEC VT52, Lear Siegler ADM-3A®, Data General D200, and Hazeltine 1500.

Nothing compares to these VISUAL terminals when it comes to ergonomics. They are designed in lightweight plastic and can easily be swiveled and tilted for maximum operator comfort. A "menu-style" set-up mode eliminates all cumbersome switches. Other human design features include:
- 12" or 14" non-glare screen, available in green or white phosphor
- High density 7x9 dot matrix characters; 7x11 in lower case
- 25th status line
- Detached keyboard, with coil cable
- Sculptured keycaps with matte finish for low glare
- N-Key rollover

- Audible keyclick, user enabled
- Jump, or 2-speed smooth scrolling
The versatile VISUAL 300 and 330 offer a package of standard features unmatched by any terminal in their class:
- Block and character transmission
- 12 user-programmable non-volatile function keys, each capable of storing 32 characters
- Blink, underline, reverse, bold and blank video attributes require no display space
- Line-drawing character set
- Split screen
- Full editing
- Programmable non-volatile columnar tabbing, or field tabbing, forward and backward

The U.L. listed VISUAL 300 and 330 exceed FCC Class A requirements and U.S. Government standards for X-ray emissions. All this at surprisingly low prices. Call for details on the VISUAL 300 and 330—the flexible terminals.

Service available in principal cities through Sorbus Service, Division of Management Assistance, Inc.

VISUAL Technology Incorporated
540 Main Street, Tewksbury, MA 01876
Telephone (617) 851-5000. Telex 951-539
Embedded EEPROM
(continued from page 72)

Information can be written into the 72720's program memory by having the CPU execute a single PRG instruction or by applying external address, data, and control signals, as in standard EEPROMs. The CPU's PRG instruction uses the TMS7000's indirect addressing mode to load data from the accumulator into the address pointed to by a register pair. Under CPU control, a byte of memory can be programmed in 13 ms, which allows the 72720 to be remotely programmed via a serial link at rates greater than 600 baud. This is accomplished without data buffering.

Security is implemented by a 1-bit control register in the processor's I/O address space. When this bit is set, which can only be done by the CPU, the onchip inhibit logic will block data transfer from the EEPROM to the external data bus. Only an externally generated block erase, which also erases the EEPROM's entire contents, can reset (clear) the inhibit bit. Thus, the user can be assured that proprietary program code cannot be read once the system is activated.

Remote and self-adapting programming abilities will allow designers to build systems whose software can be altered to suit an application's requirements without human intervention. Such products can also be designed to modify the programs or data in their own memories as circumstances dictate.

With appropriate software, remote servicing, such as uploading stored data and downloading new programs or parameters, can be done by telephone. Maintenance diagnostic monitors can be installed in equipment located in remote areas, with the 72720 tracing and recording operational sequences up to and including failures.

By itself, the Seeq 72720 is not particularly impressive in terms of speed or capabilities—equivalent performance could be obtained by using an EEPROM and a conventional microprocessor. However, when the principle behind the 72720 is applied to other architecture, significant gains in both speed and functionality can be expected. Using CMOS technology, for instance, will significantly decrease power consumption. Two-micron design rules, along with optimized microcode and chip layout, will also heighten performance.

With a tenfold speed increase that is possible with improvements in the EEPROM portion of the microcomputer, the devices will be very useful in applications such as voice technology. Realtime adaptive filtering, fast Fourier transforms, and pattern recognition will be both possible and cost effective. Seeq Technology, Inc, 1849 Fortune Dr, San Jose, CA 95131.

Circle 246
FutureNet's DASH-1 Revolutionizes Schematic Design and Documentation!

Perfect Schematics on Your IBM*PC
Imagine, sitting at your IBM Personal Computer, producing perfect schematics in a fraction of the time it would take using normal design techniques. Gone forever are the tedium and agony associated with manual design, drafting, and documentation.

FutureNet's DASH-1 Schematic Designer is the only system tailored specifically to the needs of the electronics engineer. It can make you five times more efficient as a designer, and nearly eight times more efficient when it comes to revisions.

Parts Libraries Included
No more sweating over IC data books. The DASH-1 Parts Library (on disk) includes TTL, popular microprocessors, memory and support chips, plus discrete components, complete with pinouts and pin functions. With a keystroke you can call up the symbols you need or quickly create new symbols. Using the mouse you can move symbols or areas of a drawing and interconnect them. And annotation is a snap. Typically, a schematic that would take eight hours to produce manually can be completed in one to two hours on the DASH-1.

Ah, the ecstasy of it all!

Captures Data for Documentation
DASH-1 does much more than create a perfect schematic. With your design data captured automatically on disk, essential documents — Net Lists, Lists of Materials, Design Check Reports — can be produced at will. Think of the hours of drudgery you'll save by eliminating these time-consuming, error-prone tasks. Plus, you'll have peace of mind knowing that DASH-1 will locate many common design errors before they reach the hardware stage.

DASH-1 Talks to Other Systems
The DASH-1 interfaces with other computer or CAD systems, transferring all your schematic data in a flash. Direct connection to VAX's or PDP-11's is especially easy.

The $5,980 Miracle
After seeing DASH-1 in operation, engineers from large and small companies alike have said, "We need this!" They're pleased by the price, too. Just $5,980 for the Add-on Package to your IBM PC. Complete turnkey systems including the IBM PC and the new IBM XT with 10 Mb Winchester hard disk and printer are available at prices starting at $12,960. Call FutureNet today for more information on the amazing DASH-1. You'll become a far more efficient designer overnight! So long Agony... hello Ecstasy.
Chips gain speed and flexibility

A family of high speed digital processing chips with a 200-ns cycle time and a 5M-instruction/s execution time has been announced by Texas Instruments. One member of the family, the TMS320, is presently being sampled for applications such as image processing, speech recognition and synthesis, and instrumentation control.

While this device is especially fast—its 60-member instruction set consists primarily of single-cycle and single-word instructions—it has been optimized for control and computation and not for use as a general purpose CPU. Also, its onboard RAM is adequate for 64-point fast Fourier transform implementations. The company intends this chip as a replacement for multichip bit-slice devices available now.

Based on a modified Harvard architecture (separate data and program memories), the chip allows transfer between the two memory areas. In this way, constants can be stored in program memory and program branches can be taken on the basis of data computations. Data memory consists of 144 16-bit words of onchip static RAM.

A fast arithmetic logic unit (ALU) on the chip can multiply two 16-bit signed 2's complement numbers in 200 ns to form a 32-bit product. Although the ALU maintains all operands internally as 32-bit numbers, input and output are 16 bit. A single-cycle 0- to 16-bit barrel shifter and the ability to use offchip RAM or ROM further increase device flexibility.

First versions of the chip use different methods of storing programs: the TMS320M10 microcomputer version has 3K bytes of masked ROM onboard, while the TMS32010 microprocessor version can use up to 8K bytes of external memory. The SMJ32010 is a MIL-STD-883B version of the microprocessor.

The chip family is fabricated using silicon gate NMOS and 2.7-micron design rules. It operates from single 5-V power supplies, typically dissipates 950 mW, and is provided in standard 40-pin plastic or ceramic DIPs.

Samples are now being provided, and production quantities will be available soon. In 100-piece quantities, devices are $120 in ceramic packages and $105 in plastic. The military version price is $577.43 in 100-piece quantities. Texas Instruments, Semiconductor Group, PO Box 401560, Dallas, TX 75240. Circle 247
TOWER™ 1632.
A SHAPE YOU CAN WORK WITH.
AT A PRICE YOU CAN LIVE WITH.

We call it “computer a la card.”

Up to six microprocessor-based controller cards mounted into Tower™ 1632’s Multibus* give system builders a range of hardware options until now available only to those with the resources to design, develop and manufacture a totally new system from the ground up.

You see, anyone could give you industry standard interfaces. Only Tower 1632 gives you the power to fully exploit all your options.

But it won’t overpower your budget. Buy only what you need. Tower 1632 will arrive from the factory tailored for any application from one to sixteen users.

It’s the system builder’s ideal foundation. Mass storage options, for example, range from a megabyte to a gigabyte. From networking to peripherals, it’s as ready for the future as it is right for today. And the operating system, derived from UNIX**, delivers maximum software capability and portability.

So if your next computer isn’t everything you want in a computer—no more and no less—you didn’t call us. (The number is 1-800-222-1235.)

Tower’s OEM price starts under $10,000. And its performance never stops.

In Ohio (513) 445-2380.
In Canada (800) 268-3966.

BUILT FOR SYSTEMS BUILDERS.
TOWER 1632.

*Multibus is a trademark of Intel.
**UNIX is a trademark of Bell Laboratories.
Conference on Computer Graphics and Interactive Techniques
Cobo Hall, Detroit, Michigan
July 25 to 29, 1983

Drawing from a growing repertoire of computer graphics installations, SIGGRAPH '83 exhibitors and Technical Program speakers are expected to plumb every aspect of computer graphics design. An exhibitor forum adjacent to exhibition areas will host product expositions on hardware trends, CAD/CAM/CAE, and future applications. Strong showings are expected in the fields of engineering workstations; refresh vector, raster, and storage tube display systems; graphical input; image processing; film/paper hardcopy equipment; and software support.

The 10th annual conference is sponsored by the Association for Computing Machinery's Special Interest Group on Computer Graphics in cooperation with the Engineering Society of Detroit, IEEE Technical Committee on Computer Graphics, and Eurographics.

Formal presentations at SIGGRAPH are broken up into two groups: tutorial/seminar courses during the first two days of the conference, and Technical Program panels/paper presentations over the remaining three days. Technical Program sessions likely to interest Computer Design readers are listed on the following pages.

Locations for the full-day tutorial/seminar courses are being scheduled concurrently at Cobo Hall, Westin Hotel, Veterans Memorial Building, and the Engineering Society of Detroit. One 2-day tutorial will introduce both graphics application software development and the Graphical Kernel System (GKS) being developed by ANSI and ISO. Session 6, which is geared to software engineers who plan to use GKS, will examine practical applications of the standard as well as the problem of converting existing applications to GKS.

Distributed Graphics Systems (Session 21 on Tuesday) will discuss how to provide integrated graphics capabilities through a network of processors, computers, and data facilities. Lecturers will explain how to design fairly independent functional modules for allocation in a distributed network.

Monday's Session 11 will introduce general issues and future trends in CAD/CAM/CAE, before exhibiting vendors in companion Session 12 give technical descriptions of their CAD systems the next day. Alternately, scheduling Session 13 for Monday will open up the tutorial on solid modeling for mechanical CAD/CAM/CAE applications. Starting with basic principles, representations/algorithms, applications, and systems, the meeting will proceed to examine recent research as well as a contemporary solid modeler. Advanced topics will be pursued Tuesday during Session 14, when speakers will delve into oct-tree representations, Boolean operations, finite element meshes generation, and robot simulation.

Other promising options include Monday's Session 16, during which the role of interactive graphics in VLSI design and the use of VLSI in computer graphics systems will be considered.

Throughout the conference, a juried art show will display computer-generated sculpture, drawings, prints, and murals. Video and film works will be shown with frame buffer and interactive installations. In addition, film and video programs on Tuesday and Wednesday nights will screen sophisticated scientific, artistic, and commercial motion graphics.

For registration information, contact
ACM SIGGRAPH '83, PO Box 72045, Chicago, IL 60690.
Tel: 312/644-6610

(continued on page 80)
Black and white facts about color graphics.

Fact 1. Software development is expensive.

Raster Technologies' Model One graphics systems feature software tools that speed application development. Like an integrated local debugger, Command stream translator, Local command execution, A complete HELP facility. And truly easy to use macro programming. These unmatched software tools save you time and money.

Fact 2. Software redevelopment is even more expensive.

With Raster Technologies' truly compatible Model One family, you can take advantage of the latest hardware without any software rewrites. This means an easy upgrade to a more powerful product while still using the same graphic commands, program development tools and host library. So the application developed for the best hardware today can run on the best hardware tomorrow. Without modification.

Fact 3. Performance is a lot more than good specs.

Graphics performance goes beyond pixel and vector timing specs. It is the ability to display a complex picture without having to wait. Provide instantaneous interaction between an application program and its user. And efficiently communicate with a host computer. The kind of total graphics performance you should measure before you buy.


The Model One family from Raster Technologies offers maximum flexibility at the lowest cost. Because it lets the user select the combinations of display resolution, color and refresh rates that are right for that particular application. Factors that are different for every application.

Fact 5. Graphics technology is moving fast.

Raster Technologies is dedicated to one business: graphics. All our development efforts focus on advancing graphics technologies. With the latest microcircuitry, The newest and fastest microprocessors. The most advanced display list architectures. And the most innovative pipelined multiple processor designs. All to advance graphics capabilities compatibly. And keep today's customers with us tomorrow.

Fact 6. You should benchmark the Model One.

The Model One 25 features vivid full color imaging performance with 512 x 512 resolution. The Model One 40 features ultra high 1024 x 1024 resolution. The Model One 60 features 100% flicker-free 60 Hz non-interlaced display with 768 x 576 resolution. All support our Advanced Graphics Application Development Firmware and powerful display list package. Put the Model One family to the test.

Raster Technologies

The benchmark of computer graphics.

9 Executive Park Drive
North Billerica, Massachusetts 01862
(617) 667-8900
TWX: 710-347-0202

See Us at Booth #1832 at NCGA
and Booth #849 at SIGGRAPH '83

CIRCLE 55
Technical Program Excerpts

Image Generation I
Wed 9 to 10:30 am, Cobo Arena
Chair: E. Catmull, Lucasfilm
"Pyramidal Parametrics"
  L. Williams, New York Institute of Technology
"Lighting Controls for Synthetic Images"
  D. R. Warn, General Motors Research Labs
"Artificial Texturing: An Aid to Surface Visualization"
  D. Schweitzer, University of Utah

Computer Graphics in Higher Education
Wed 9 to 10:30 am, Cobo Hall A
Chair: J. D. Foley, George Washington University
Panelists: A. Bork, University of California, Irvine; M. Brown, Digital Productions; R. King, Sheridan College; A. van Dam, Brown University; and M. Wozny, Rensselaer Polytechnic Institute

User Interface
Wed 10:45 am to 12:15 pm, Cobo Arena
Chair: D. Bergeron, University of New Hampshire
"Towards a Comprehensive User Interface Management System"
  W. Buxton, M. R. Lamb, D. Sherman, and K. C. Smith, University of Toronto
"Syngraph: An Automatic Interaction Generator"
  D. R. Olson, Jr and E. P. Dempsey, Arizona State University
"A Graphics Editor for Benesh Movement Notation"
  B. Singh, Schlumberger-Doll Research; and J. C. Beatty, K. S. Booth, and R. Ryman, University of Waterloo

Advances in New Display Technology
Wed 10:45 am to 12:15 pm, Cobo Hall A
Chair: S. Sherr, Westland Electronics
Panelists: I. Chang, IBM Corp; T. Maloney, PanelVision; P. Pleshko, IBM Corp; E. Schlam, Eradcom; and P. Seats, Thomas Electronics

Raster Algorithms
Wed 3:45 to 5:30 pm, Cobo Arena
Chair: A. Fournier, University of Toronto
"Near-Realtime Shaded Display of Rigid Objects"
  H. Fuchs, G. D. Abram, and E. D. Grant, University of North Carolina, Chapel Hill
"A Scan-Line Hidden Surface Removal Procedure for Constructive Solid Geometry"
  P. R. Atherton, General Electric Co
"Ray Tracing Algebraic Surfaces"
  P. Hanrahan, University of Wisconsin, Madison
"Ray Tracing Fractal Surfaces"
  J. T. Kajiya, California Institute of Technology

Technical Implications of Proposed Graphics Standards
Wed 3:45 to 5:45 pm, Cobo Hall A
Chair: D. Straayer, Tektronix Inc
Panelists: P. Bono, Athena Systems; R. Ehlers, Evans & Sutherland Computer Corp; G. Enderle, Karlsruhe Nuclear Research Centre; T. Reed, Los Alamos National Lab; D. Shuey, McDonnell Douglas Automation; M. Skall, National Bureau of Standards; E. Sonderegger, SIGGRAPH; and T. Wright, ISSCO

*Technical Program sessions are subject to last-minute changes.
UNCOMPROMISING CRAFTSMANSHIP

That's what makes us different. The critical difference for superior digitizer performance. ALTEK applies precision craftsmanship to every facet of construction. The result...

UNCOMPROMISING ACCURACY
Every DATATAB®, large or small, has resolution, stability and repeatability of .001". Accuracies to ±.003"...the highest in the industry.

"Uncompromising Accuracy for consistent results"

UNCOMPROMISING DEPENDABILITY
DATATAB®’s patented design, proprietary construction and simple control electronics make periodic maintenance unnecessary. Performance is unaffected by use, temperature or humidity.

"Uncompromising Dependability for long term reliability"

UNCOMPROMISING VERSATILITY
Unequaled variety of sizes, models and interfaces. Just compare.....sizes up to 42" × 130". Models with opaque, backlit, rear projection, translucent or restrained cursor surface. Controllers range from a single printed circuit board to standalone workstations.

"Uncompromising Versatility.....a DATATAB for any application"

UNCOMPROMISING...Our Customers wouldn't have it any other way.

GRAPHIC DIGITIZERS by:

ALTEK Corporation
2150 INDUSTRIAL PARKWAY
SILVER SPRING, MARYLAND 20904
TEL: 301-622-3906 TMX: 710-825-0422
See us at NCGA Booth #s 337 and 338 and at Siggraph Booth #467.
Applications
Thurs 9 to 10:30 am, Cobo Arena
Chair: H. Freeman, Rensselaer Polytechnic Institute
"Computer Graphic Modeling of American Sign Language"
J. Loomis, H. Poizner, U. Bellugi, and A. Blakemore,
The Salk Institute of Biological Studies; and
J. Hollerbach, Massachusetts Institute of Technology
"Incense: A System for Displaying Data Structures"
B. A. Myers, Xerox Palo Alto Research Center
"Graphical Style—Towards High Quality Illustrations"
R. J. Beach, University of Waterloo; and M. Stone,
Xerox Palo Alto Research Center

The Simulation of Natural Phenomena
Thurs 9 to 10:30 am, Cobo Hall A
Chair: C. A. Csuri, Ohio State University
Panelists: J. Blinn, Jet Propulsion Lab; J. Gomez, Ohio State University; N. Max, Lawrence Livermore National Lab; and W. Reeves, Lucasfilm

Anti-Aliasing Techniques
Thurs 10:45 am to 12:15 pm, Cobo Arena
Chair: J. Clark, Stanford University
"A Parallel Scan Conversion Algorithm with Anti-Aliasing for a General-Purpose Ultracomputer"
E. Fiume and A. Fournier, University of Toronto; and L. Rudolph, Carnegie-Mellon University
"Anti-Aliased Line Drawing Using Brush Extrusion"
T. Whitted, Bell Labs
"Edge Inference and Applications"
J. Bloomenthal, New York Institute of Technology

Solid Modeling
Thurs 10:45 am to 12:15 pm, Cobo Hall A
Chair: R. N. Goldman, Control Data Corp
Panelists: D. Gossard, Massachusetts Institute of Technology; R. Riesenfeld, University of Utah; H. Voelcker, University of Rochester; and T. Woo, University of Michigan

Systems and Standards
Thurs 2 to 3:30 pm, Cobo Arena
Chair: R. Hopgood, Rutherford-Appleton Research Labs
"A Device-Independent Network Graphics System"
D. U. Cahn and A. C. Yen, Lawrence Berkeley Lab
"A Core Graphics Environment for Teletext Simulations"
D. F. Dixon, RCA/David Sarnoff Research Center
"Minimal gks"
R. W. Simons, Sandia National Labs

Shape Representation
Thurs 3:45 to 5:15 pm, Cobo Arena
Chair: R. Riesenfeld, University of Utah
"Local Control of Bias and Tension in Beta-Splines"
B. A. Barsky, University of California, Berkeley; and J. C. Beatty, University of Waterloo
"Topologically Reliable Display of Algebraic Curves"
D. S. Arnon, Purdue University
"Curve-Fitting with Piecewise Parametric Cubics"
M. Plass and M. Stone, Xerox Palo Alto Research Center

Industrial Strategies of Japanese Computer Manufacturers
Thurs 3:45 to 5:45 pm, Cobo Hall A
Chair: T. Kunii, University of Tokyo
Panelists: T. Ikedo, Seillac Company Ltd; K. Ishimura, Yamaha Research Institute; K. Iwata, Graphica Computer Corp; K. Naito, Daini Seikosha; and S. Saimi, Japan Radio Corp

Geometric Input Techniques
Fri 8:30 to 10 am, Cobo Arena
Chair: I. Carlbom, Schlumberger-Doll Research
"Solid Model Input through Orthographic Views"
H. Sakurai, Nissan Motor Co; and D. G. Gossard, Massachusetts Institute of Technology

(continued on page 84)
FROM THE SIZE OF THIS PAGE TO THE SIZE OF YOUR PALM.

INTRODUCING CERMETEK'S HIGHLY INTELLIGENT 212A-TYPE MODEM COMPONENT.

A complete integral 212A modem component. At Cermetek, modem technology has evolved to reduce the size of an integral 212A-type modem from a very large PCB down to the size of a component. In a space of 8 square inches, the CH1760 implements a fully featured 212A-type modem, including an FCC registered telephone line interface and advanced autodial capability.

No more custom PCBs. Since the CH1760 is a standard modem component and is fully featured, you no longer have to commit to a custom PCB to enjoy 212A-type modem integration. No NREs or custom contracts to worry about.

Command driven operation. The CH1760's intelligent command interpreter enables you to easily control modem operation through the exchange of serial ASCII characters. This promotes simple system integration.

Features:
- Small size 2.4" x 3.6" x .05"
- Serial command driven operation
- 300/1200 BPS operation
- Bell 212A and 103 compatible
- Auto/Manual dialing - DTMF or PULSE
- Auto/Manual ANSWER
- Auto/Force selection of DTMF or PULSE dialing
- Auto speed selection
- Auto parity selection
- Call progress tone detection (dial, busy, ring-back, modem answer tone and human voice)
- 32 digit last number dialed storage
- Memory expansion port (stores an additional 68 telephone numbers or log-on messages)
- TTL Host serial interface

Please mail me additional information on the CH1760.

Cermetek Microelectronics
Sunnyvale, CA 94086
TEL: (408) 734-8150

CH1760
300/1200 BPS INTELLIGENT MODEM

VALUES IN SQUARE IN.

<table>
<thead>
<tr>
<th>Year</th>
<th>1979</th>
<th>1981</th>
<th>1982</th>
<th>1983</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>120.0</td>
<td>90.0</td>
<td>45.0</td>
<td>8.0</td>
</tr>
</tbody>
</table>

(408) 734-8150
"Spatial Input/Display Correspondence in a Stereoscopic Computer Graphic Workstation"
C. Schmandt, Massachusetts Institute of Technology

"Advanced 3-Dimensional Computer Graphics for Craniofacial Surgical Planning and Evaluation"
M. W. Vannier, Mallinckrodt Institute, Washington University; J. L. Marsh, St. Louis Children's Hospital, Washington University; and J. O. Warren, McDonnell Douglas Aircraft Co

Computer Graphics and Visual Designers
Fri 8:30 to 10 am, Cobo Hall A
Chair: A. Marcus, Aaron Marcus and Assocs
Panelists: D. Coates, Design Consultant; and W. Mitchell, CAD Design Group

Solid Modeling
Fri 10:15 to 11:45 am, Cobo Arena
Chair: J. Dill, Cornell University
"Localized Set Operations for Solid Modeling"
M. Mantyla and M. Tamminen, Helsinki University of Technology
"Design of Solids with Free-Form Surfaces"
H. Chiyokura and F. Kimura, University of Tokyo
"High Speed Display Processor"
A. L. Thomas, University of Durham

Artists Interfacing with Technology: Basic Concepts of Digital Creation
Fri 10:15 to 11:45 am, Cobo Hall A
Chair: F. Dietrich, West Coast University
Panelists: L. Cuba, Independent Artist; D. Gerbarg, New York University; A. Lippman, Massachusetts Institute of Technology; and D. Sandin, University of Illinois, Chicago

Raster Techniques
Fri 1:15 to 2:45 pm, Cobo Arena
Chair: M. Stone, Xerox Palo Alto Research Center
"An Inexpensive Scheme for Calibration of a Color Monitor in Terms of cIE Standard Coordinates"
W. Cowan, National Research Council of Canada
"Interactive Image Query System Using Progressive Transmission"
F. S. Hill, Jr, University of Massachusetts; S. Walker, Jr, University of Maine; and F. Gao, Beijin Normal University
"Graphics in Overlapping Bit-Map Layers"
R. Pike, Bell Labs

Solid Modeling: A User Perspective
Fri 1:15 to 2:45 pm, Cobo Hall A
Chair: F. W. Bliss, Ford Motor Co
Panelists: C. Machover, Machover Assocs; M. Smith, Bendix Corp; and C. Vogel, General Motors Corp

Image Generation II
Fri 3 to 4:30 pm, Cobo Arena
Chair: T. Whitted, Bell Labs
"Particle Systems—A Technique for Modeling a Class of Fuzzy Objects"
W. T. Reeves, Lucasfilm
"Temporal Anti-Aliasing in Computer Generated Animation"
J. Korein and N. Badler, University of Pennsylvania
"Modeling Motion Blur in Computer Generated Images"
M. Potmesil, Bell Labs; and I. Chakravarty, Schlumberger-Doll Research
Well, IBM claims yet another first.

By offering the p-System™ on their Displaywriter and PC, it becomes the only operating system they market for both. They obviously know a good thing when they see it.

But then so did Apple®, Commodore, Corvus™, TI, Digital, HP Osborne®, Philips, Sage®, Zenith, NEC, and Olivetti, for that matter.

And as a microcomputer manufacturer, you can see why. Applications sell hardware. But in the 16-bit marketplace, there just aren't enough applications available. Or are there?

Right now, there are hundreds of high-quality p-System applications. Like general business applications. Vertical applications for medicine, law, and real estate. And integrated professional productivity tools such as spreadsheets and word processing. The list goes on.

With the p-System, these applications can be running on your machine, too. Sooner than you thought possible.

And, with the p-System you can offer your customers the most complete set of microcomputer software development tools anywhere. Including compilers for UCSD Pascal™, FORTRAN-77, and BASIC, a screen editor, 10 macro assemblers, a print spooler, graphics utilities, and a host of others.

The p-System, the Universal Operating System™ makes it possible with real portability across all 8 and 16-bit micros. We can make it possible for you, too. Inexpensively. After all, IBM is offering it on the PC for just $50.

So check into acquiring the world's only Universal Operating System yourself. IBM did. And how often do they make a bad move?

Finally, once is enough.
We just eliminated solder across the board.

Now you can keep solder off your pc backplanes, completely. Because the AMP compliant ACTION PIN contact is into everything. It’s in our zero insertion force connectors. Our one and two-piece pc board connectors. Our telecommunications-style connectors. Our subminiature Ds. Our interconnection system headers. Even our new power distribution taps.

Yet the solderless advantage is only part of its story. Our compliant pin also prevents costly plated-through hole damage. It’s forgiving enough to relax hole tolerances—and yet assure a gas-tight fit, every time. You can replace damaged pins a number of times, too, without losing any performance.

There’s more. You can apply every one of these different AMP connectors with one basic production machine—across the board.
AMP Facts

New one-piece distribution tap with compliant pin for power I/Os.

Compliant pin in new two-piece connector system allows higher pin count and lowers daughter card rejects.

To eliminate solder and get more information, call the AMP ACTION PIN Desk at (717) 780-4400.
AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.
Digital’s new multi-user, multi-tasking Micro/PDP-11™ gives you all the microcomputer you need to solve your application problems. At a price almost anyone can afford—$9,200.*

The Micro/PDP-11 is a powerful micro that’s small enough to fit just about anywhere. It’s available in rack mount, floor mount, and tabletop versions. And includes CPU, a 10 Mb 5¼” Winchester, 800 Kb floppy back-up, and auto-self diagnostics for I/O, CPU and mass storage.

But what puts the Micro/PDP-11 in front of all the others is what’s behind it.

More software.

Over 2,000 developed applications are available for laboratories, factories, offices, and other businesses. And thousands of PDP-11 trained programmers ready to write even more.

A wide choice of operating systems. Including RSX-11, RSTS/E, RT-11, DSM-11, MicroPower/Pascal, and UNIX.**

A variety of languages such as BASIC, FORTRAN-77, COBOL-81, C, DATATRIEVE, PASCAL and DIBOL.

Thousands of peripheral hardware interface products.

And the support of Digital’s worldwide team of over 18,000 sales and service professionals. Ready to answer any question. Or solve any problem.
No other micro can stand up to the Micro/PDP-11.
Monolithic Systems Corporation has always been synonymous with Multibus technology. In fact, MSC has the distinction of having designed the first patented single board computer. Other firsts include: the first use of 64K RAM elements, on-board EPROMs, floppy disk controllers, APU's, user selectable addressing and multimaster CPU configurations. These board level accomplishments have benefited OEM's for over 12 years and have culminated into a powerful line of systems, the MSC 8800 series.

As the leading innovator in Multibus products, Monolithic Systems offers a family of systems intended to do things never done before. Systems to assist and create test programs for the scientific and industrial markets, to be multi-user and multi-tasking, to be expandable, rugged and reliable beyond anyone's expectations. Available with operating systems by Digital Research, the MSC 8800 series and board level products will be prominent factors in Multibus applications now and in the future.

For more information about Monolithic Systems Corporation and its Multibus product line call Toll Free 1-800-525-7661.
MANAGING YIELDS BY YIELDING MANAGEMENT TO COMPUTERS

Productivity receives a boost when the precepts of modern data processing are applied to information management in the automated factory.

by Ronald D. Barker

One of the ironies of modern computer technology is that its creators—the engineers—are often the last to reap its benefits. Only recently, computer based tools like computer aided design/computer aided manufacturing and information management systems have made inroads into the design labs of America. For a profession that hastily abandons the slide rule for the electronic calculator, this spotty application of computer technology is, indeed, enigmatic.

Impinging realities of modern economics are changing this situation, however. The push for increased productivity, as exemplified by factory automation, is providing an avenue for the introduction of computer based tools into many facets of manufacturing and design. Unfortunately, much automation is taking place haltingly and haphazardly. As a result, factories are ending up with a diverse mix of tools, systems, and functions that are incompatible and isolated. This being the case, it is often impossible to integrate these elements into a factory-wide information system.

One starting point from which to attack this integration problem is yield management. In addition, the architecture of a system designed to manage yield can also be applied to any highly technical manufacturing environment. The concepts implicit in such architectures are central to factory-wide integration of computer based information management.

Yield management is defined as the collection and analysis of data, and the presentation of information that enables engineering and production staffs to understand and manage elements that comprise yield within their environment. When, where, and how data are collected and used to effectively manage yield are key issues in the design of such a system. The decisions made during the automation process lay the groundwork for yield management development.

The microprocessor problem
Availability of inexpensive microprocessors has dramatically increased the range of potential applications for computer based automation in manufacturing. However, to fully tap the increased yield potential of these applications, a change must occur in the decision process of what gets automated, and how. Isolated, standalone applications are no longer sufficient. To maximize productivity, systems must be implemented that integrate manufacturing data into a factory-wide information system. This data can then be used to model and manage manufacturing process yields. Yield is defined as the ratio of products passing final test to all products manufactured. Fig 1 points out the inherent isolation and inadequacy of standalone applications. In such situations, correlating manufacturing-step data into the larger world of the factory is extremely difficult.

Ronald D. Barker is manager of process analysis systems at IBM, General Technology Div, Essex Junction, VT 05452, where he is responsible for engineering data collection, data bases, retrieval, and presentation. Mr Barker has a BS in mathematics from Arron University and an MS in mathematics from Ohio State University.
While microprocessors were being implemented for manufacturing applications, a different evolution was occurring in the administrative applications of computers in the factory. Typical applications included payroll, billing, and inventory. The administrative environment became characterized by large data processing centers, big mainframe computers, and integrated data bases.

Administrative applications require integrated data bases since orders have a direct relationship to many aspects of the manufacturing exercise including: billing, inventory, and what goes into the salesman’s paycheck. The relationship between raw material quality, defect density, process control conditions, and final test results is not as well-defined. However, according to Castrucci et al, it is possible to develop a yield model for semiconductor processes that describes yield as a function of process parameter values. The concept, of course, can be applied to other highly technical manufacturing processes, given the ability to collect, integrate, and present the relevant information.

Key to determining applicability of the yield management concept is the ability to detect defects that lower yields. Once detected, these defects can be related to specific process steps, and then fed back as process corrections based on the defect analysis. For example, in a multiple-step manufacturing operation, defect detection is accomplished by an inspection for quality levels or misprocessing. A measurement for conformance to specifications or a functional test can also be performed. Ideally, the data collected in each detection mode can be analyzed to determine probable cause of the defects. To increase yield, corrections can then be fed back to the process steps that introduced the defects. This closed loop process is illustrated in Fig 2. A problem arises, however, due to the separate evolutions of automation and data processing. Automation processing is distributed; mainframe data processing is centralized. As a result, these opposite ends of the application spectrum must be the starting point for developing an integrated yield management system.

**Yield management system**

Four steps are required to develop and implement a yield management system. First, yield must be defined. Yield usually means different things to different people in the factory. Exactly how yield is defined is not as important as the consistency with which the definition is observed. Everyone who participates in managing the factory yield, from process step operator to plant manager, must embrace the same definition of yield. In its simplest sense, yield is defined as the ratio of products passing final test to all products manufactured.

**Fig 1** The isolated nature of present data collection methods used in manufacturing provides little benefit. Despite efforts expended collecting such data, they are of little value when no mechanism exists to integrate them into the overall manufacturing process.

**Fig 2** A manufacturing process that provides for feedback improves productivity and yield. Establishing data gathering and feedback loops enables operators to gain control of product flow and process efficiency.
Once yield is defined, the second step in implementing a yield management system is to isolate the elements that affect factory yield. Here, many questions need to be raised. For example, what are the known yield detractors (e.g., breakage, misprocessing, or loss)? Are there invisible yield detractors such as a reprocess cycle where a product may languish forever? Are there yield bonuses, such as last month's reprocessed products appearing this month as extras? What are the suspected but unconfirmed yield detractors? The entire manufacturing process, in successive layers of detail, needs to be examined to establish measurement tools and targets.

The third step provides the financial base from which to judge the affordability of the hardware and software to be installed. After examining the yield elements determined in step two, decisions need to be made on the potential productivity gains resulting from increased yields. In other words, practical yield objectives need to be set. These are not black and white decisions. Rather, they involve many facets of a manufacturing operation and require the full involvement of the engineering, systems, and financial staffs. For example, a 1% yield loss during the first few manufacturing steps may be acceptable due to the investment required to correct it. A 1% yield loss in the final manufacturing steps may be unacceptable because of the added value to the product as it nears completion. Therefore, significant investment to correct this loss may be warranted. Also, the amount of hardware and software necessary to encompass large segments of the manufacturing process, or identify major process interactions as yield detractors, may be prohibitively expensive. In this case, system implementation may be deferred. It is thus important to decide which elements should be attacked first. This decision should be predicated upon the potential productivity increase due to improved yield, and reasonable yield increase objectives.

Gathering the required tools is the final step. Tools are more than hardware, software, data analysis, and reports. In fact, one essential tool is the organizational structure itself. Manufacturing control and engineering personnel must be organized in such a way that management responsibility coincides with the defined yield elements. All personnel must understand the yield objectives defined in step three, as well as their measurements. A clear definition of objectives helps to implement a successful yield management system.

**Yielding to the hierarchy**

System architecture is, in actuality, a mirror of all data collected in the factory. Several characteristics of the architecture become apparent when defining the yield management process. The foremost is its hierarchical nature. Fig 3 illustrates a typical yield management system architecture.

The hierarchical nature of the data determines the product mix and the volume that is manufactured. A high level of this hierarchy may be cost objectives. Those help determine manufacturing volume and mix, and are generated by sales forecasts. Sales eventually translate into orders and manufacturing schedules, a more immediate and intermediate level of manufacturing control data. At a low hierarchical level is machine control data.

Yield data are in a similar hierarchy. At the highest level are relationships across product lines and many manufacturing steps. Intermediary levels
of yield data may be yielded through logical groupings of manufacturing steps. Low levels may be measurements of component quality or conformance to specification.

What seems to be required, then, is a system architecture that mirrors and complements this data structure. A hierarchical architecture with levels of functions, data analysis, data presentation, and data storage allows interaction with the system that is consistent with established ways of viewing the information.

When examining system interactions, data acquisition (the lowest level of the architectural hierarchy) provides a good example.

Data acquisition at a process step level is an isolated function. It might involve a material quality measure or an inspection result. In either case, it does not require interaction with data collected at other steps. Thus, the lowest level of the architecture is characterized by limited scope of function, elementary analysis, limited data presentation, and no data storage. Luckily, these characteristics describe the distributed computer automation already in existence in the factory. This primitive level of automation can serve as the basis for building a factory-wide information management system.

An intermediate level of the hierarchy consolidates the data from the low level collection systems into the first elements of an information system. The intermediate level, which recognizes correlations among results collected from several low level segments, provides functions to manage those correlations. Initially Stapper,2 and later Melan et al,3 demonstrated the techniques of using correlation analysis among yield elements to feedback process corrections. For example, if the first microprocessing steps have been isolated as a yield element, the intermediate level for the architecture would be assigned the tasks of collecting the elemental data types, storing them, producing correlation analyses, and presenting information that spans several process steps.

At a high level of the architecture, functions relating business parameters to yield can be found. Issues to be resolved by these functions are what happens to yield when volume and mix change, and the rate of yield learning. These functions naturally merge the business applications of the existing data processing center into the new functions of yield management. Data stored at this level span the factory and must be kept for a long time to establish trends. The information presented here depicts yield as a function of the entire factory environment. This layer of the architecture coincides with, and enhances, existing data processing operations.

Thus, it is apparent that this layered, hierarchical architecture bridges the gap between the distributed, automated base and the centralized, data processing base from which a yield management system began. The Table, “Yield Management System Task Assignments,” summarizes the functions, presentations, and storage of data in the system architecture.

Implementation issues—getting it to work

A distributed base is a starting point to implement a yield management system. Layers of function are added to this base until the existing data processing center is reached. Key technical issues need to be resolved and key business factors determined if a yield management system is going to grow into a complete implementation.

Three key technical issues arise immediately: database structures, data communications methods, and application development methods. Database strategy must revolve around implementation, maintenance, and enforcement of a factory-wide data dictionary. This requires collecting and correlating hundreds of different data elements from

<table>
<thead>
<tr>
<th>Level</th>
<th>Functions Provided</th>
<th>Data Analysis</th>
<th>Data Storage</th>
<th>Data Presentation</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>Product planning</td>
<td>Trend analysis</td>
<td>Long-term statistical summaries</td>
<td>Reports</td>
</tr>
<tr>
<td></td>
<td>Correlate business functions</td>
<td>Correlation analysis</td>
<td></td>
<td>Interactive query</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Interactive planing</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Statistical analysis</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Online inquiry</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Collection verification</td>
</tr>
</tbody>
</table>

|        | Correlation across set of lower levels | Status reports | Short-term, across many elements | None |
|        | Monitor for known yield detractors | Correlation analysis |                | |
|        | Data collection | Failure analysis |              | |
|        | Microprocessor interface | Pass/fail edit criteria |              | |
|        |                    | Go/no-go decision criteria |              | |
Introducing Zilog's new generation of microprocessors—the Z8003™ CPU with virtual memory. It lowers the cost of resident system memory, extends program-code portability and provides a convenient interface for large auxiliary storage. It's the ideal microprocessor for those big system applications.

Virtual memory in the Z8003 chip eliminates the need for program overlays, as well as the physical memory size constraints found in other chips. Programmers can design as if they had 16MB of physical memory. And users can run large programs more economically than previously possible with any other microprocessor.

A new Z8015 Paged Memory Management Unit (PMMU) adds dynamic memory relocation and protection capabilities to Z8003 systems. Each Z8015 handles sixty-four 2,048-byte pages of logical address space which map into 16 MB of physical memory.

The Z8003 CPU is the world's first 16-bit processor with a 32-bit general-purpose register set. All arithmetic (including multiply and divide) are performed at remarkable speeds of up to 14 MHz. It brings you one step closer to Zilog's 32-bit processor—a single chip which will have all features of the Z8003 CPU and the Z8015 PMMU.

Find out how the Z8003 virtual memory CPU and the Z8015 PMMU surpass what you’re currently using. Fill out the coupon and mail to: Zilog, Inc., Components Tech. Publications, 1315 Dell Avenue, MS A1-4, Campbell, CA 95008. Or call TOLL-FREE (800) 272-6460.

□ I'd like more information at this time.
□ Please have a salesman contact me.

Name ___________________________
Title ___________________________
Company ________________________
Address __________________________
City _____________________________
State __________________ Zip ______
Phone ____________________________

Zilog
Pioneering the Microworld.
An affiliate of EXON Corporation
Time and cost are key business factors in implementing yield management.

diverse areas of the factory for extended periods of time. This activity has a low likelihood of success without centralized data control. The database management system chosen must, of course, be able to work with the dictionary. Further, it must be diverse enough to handle the layered storage depicted in the architecture, from small amounts of data with few correlations to large amounts with many, complex correlations. Also, a consistent interface to the application programmer must be maintained.

Data communication methods must provide consistent communication among system layers from microprocessor to mini, to small mainframe, to large mainframe. Each layer of the architecture filters out detail and passes on a higher level of information. The lowest level of the hierarchy provides for local attachment of terminals.

Undoubtedly, layered architecture will be implemented on several different types of computers. Ideally, a language should be chosen for application development that spans micro, mini, and mainframe boundaries, and provides maximum flexibility in applying the programming resources.

As in any system implementation, time and cost are key business factors in implementing yield management. The implementation schedule and cost depend on the technical maturity of the programming and engineering staffs. Organizational maturity of the management staff, complexity of the manufacturing operation, and economics of yield productivity also play a role in system implementation.

Merging engineering measurements into the hierarchical structure, and attempting to correlate the results, requires broad-based technical experience. In addition, the management team must be flexible enough to reorganize when necessary to reflect yield element definition. They must also be mature enough to accept a new set of objectives and measurements as well as a new organizational hierarchy if that is deemed necessary. The intransience of the human element should not be underestimated.

Moreover, manufacturing complexity will slow the implementation process. More products, manufacturing steps, and complex flows result in additional data collection points and correlation among yield elements. Consequently, more time is required to understand the relationships and provide data collection hardware.

The growth path from the distributed-centralized starting point to a mature yield management system is evolutionary. From isolated yield elements, consolidation occurs in one section of the next higher layer of the architecture. Implementation proceeds apace with technical and organizational learning. The rate and extent of implementation depend on the economics involved. In general, yield-increase targets generate higher productivity. Picking the right targets and the correct elemental yield points that should be initially attacked is a combined business and technical decision.

As experience and technical maturity are gained, more extensive parts of the architecture can be implemented. Accelerated investment in such a system may be based on a commitment to climb a yield learning curve more quickly. An important business factor to consider is that the first steps in establishing both the architecture and the viability of the concept are relatively inexpensive. Using the existing factory automation base, and adding a small hardware and software investment to it, creates a new way to manage the information generated.

Due to the inexpensive microprocessor, it is economically feasible to use computer resources to help manage yield in the automated factory. The described architecture for a yield management system is a generalization of the system that is boosting factory productivity at the IBM semiconductor plant in Essex Junction, Vermont. Its hierarchical nature mirrors the data required to manage yield, and its implementation evolved from a distributed automation and centralized data processing base.

The time and money invested in a yield management system must be entirely consistent with demonstrable productivity gains. With a mature yield management computer system, however, yield becomes a more manageable element of factory productivity.

References
The system builder's best choice for color graphics is a CS5000 color system from SCION. Its basic component is MicroAngelo, the single board graphics display computer that has revolutionized monochrome display capability with low cost 512x480 pixel graphics resolution and 40 line by 85 character text capacity. When MicroAngelo boards are combined, they create high resolution color graphics that have a unique advantage. The displayed image is a combination of transparencies. So you can add, modify or delete images by transparency rather than as an entire image. SCION's Series CS5000 builds an image with up to 8 bit planes, each generated by a MicroAngelo board. You select the assignment of those bit planes to transparencies. Each transparency can display $2^n - 1$ colors where $n$ is the number of bit planes it uses. 2 bit planes would make a three color transparency, 8 bit planes would make a 255 color transparency. Once each transparency has been defined, your host can work with it independently, generating and modifying its graphics and text without interacting with the others. The independent transparencies are combined by the Color Mixer board which also assigns one of 16.8 million possible colors to each color of each transparency.

Your computer talks to the SCION Color System in SCREENWARE, SCION's high level display firmware language. SCREENWARE commands are used by the computer in each MicroAngelo bit plane to generate graphics and text primitives. User interface is made simple with prompted system set-up using SCION's ColorPak.

MicroAngelo based color graphics systems are easy to use. Just plug the boards into your Multibus or S-100 host. Or use the freestanding work station configuration with its RS-232 interface. In each case, you get high resolution color graphics for such a low price you can’t afford to design your own.

Think SCION for your graphics display needs. Think MicroAngelo. Call us at (703) 476-6100.

System shown is a Model CS5000S. A trademark of Intel Corp.

SCION

if the image is important.
HOW TO BUILD A STATE OF THE ART SYSTEM WITHOUT LIVING IN A STATE OF ANXIETY.

There are simpler things than working on the ragged edge of technology. We know. We live there.
Which is one of the reasons Intel is the one company uniquely qualified to relieve your worries.

Another is because when we produce the leading edge in commercial & military microprocessors (which is rather often), we don't do it in a vacuum.
Every new processor, including our new 186 and 286 works with the full set of peripherals.
And the standard MULTIBUS® interface.
And Ethernet®, just in case you've got networking on your mind.
We can remedy your software problems, too. With four different operating systems, and five languages each for 8- and 16-bit microprocessors.
All these standards mean you get to market fast, fast, fast. And get to spend your money on more important things. Like your unique application software, for instance.

Want to improve performance, reduce development headaches, and speed up the overall design effort? Take our software in silicon chips.
You'll feel better about our design support, too. From distributed Network Development Systems complete with Project Management Tools to portable development systems to the latest in VLSI instrumentation.
Plus over 125 field applications engineers who make house calls. And more than 1,000 customer workshops each year.
Call us at (800) 538-1876. In California, (800) 672-1833. Or write Intel, Lit. Dept. Z 12, 3065 Bowers Avenue, Santa Clara, CA 95051. And we'll see you get a copy of our full line product guide.

Because if you're going to push the state of the art, you should do it with someone who knows how it feels.

*Ethernet is a trademark of Xerox Corporation.
Low-power, 1-chip breakthrough CMOS microcomputer with
Motorola introduces the first self-programming EPROM.

And it's in volume production, today. With a special introductory offer that erases any doubt about price.

This powerful CMOS 8-bit microcomputer contains an UV EPROM and a self-programming bootstrap in ROM — along with RAM, I/O, timer and oscillator — all on a single fully-static chip. Motorola's MC1468705G2.

The 2,096 bytes of UV-erasable EPROM will let you now run what can be a truly innovative product through field trials and test marketing—complete prototype evaluation — and spin off interface and customer variations to an expanded market base without the delays and expense suffered from desired program changes on ordinary mask-ROM microcomputers.

**Uniquely adaptive on-chip intelligence.**

Unleash your imagination with this single-chip microcomputer's unmatched flexibility in low-power environments demanding frequent program changes.

The versatile on-board EPROM programmer routine allows the micro to actually field-program unused EPROM by as little as a byte at a time, adapting your product in real time, according to changes in data collection.

Of course, should your need for high-volume production take you to a ROM-based version of this CMOS microcomputer, the EPROM programmer is no longer necessary. In its place is a different routine that allows the microcomputer to test itself.

**Unique power-saving modes.**

Yes, the MC1468705G2 is low-power CMOS, with fully static operation all the way down to DC. And yes, it thus takes but a single +3 to 5.5 V power supply.

But the power-saving magic is really in the on-chip WAIT and STOP modes.

With a WAIT mode of 0.8 mA typ and a STOP mode of 5 µA typ, the MC1468705G2's supply current is merely 3 mA at 4.5 V typ under most full-speed operating conditions.

**Have it both ways.**

Plug in this one power miser, the MC1468705G2. Then, whether you crank out hundreds of systems or spit them out by the tens of thousands, there is no faster, cheaper, low-power way to market than with the world's first CMOS prototyping tool.

The UV EPROM and self-programming routine let low-quantity production hit the market running as versatile field-programmable, stand-alone systems.

But, if you're going for high-volume applications, the unique user-programmable EPROM and self-programming bootstrap ROM move you quickly through field tests that can then leapfrog you straight to a pin-compatible, debugged masked ROM. With new-found confidence. And low-priced ease.

Either way, you win. With dramatically-slaosh development costs and blazing-fast turnaround time.

And, when you replace existing multi-chip CMOS sets or power-hungry NMOS micros with the MC1468705G2, your customers win big also. With higher reliability and lower cost, as well as reduced size, weight and power for adaptive-intelligence applications.

To the MC1468705G2's UV EPROM and self-programming bootstrap ROM, add in 112 bytes of RAM, 4 bidirectional 8-bit I/O ports, an 8-bit timer with 7-bit prescaler, external and timer interrupts as well as software interrupt, and a master reset and power-on reset, and you've got it: the world's only user-programmable CMOS microcomputer, with unbeatable performance...straight out of the proven M6805 Family of microcomputers, with full software compatibility. And a plug-in twin of its forebear, the MC146805G2.

**How to get '84 prices.**

Our leadership CMOS processing wins you far more than leading-edge products. You get the opportunity to try out up to five pieces per department for just $30 apiece. Right $30 each. Our projected early-1984, low-quantity pricing.

To qualify, send us your P.O. and a letterhead request, stating department, name and shipping address (no P.O. boxes, please), and briefly describe your intended application. In generic, non-confidential terms, of course. Offer valid in USA and Canada only. We'll hold this special offer open only until September 30, 1983, so get your P.O. and letter in soon. Send to: 830 MC1468705G2 Motorola CMOS Microcomputers - L10 3501 Ed Bluestein Blvd. Austin, TX 78721

For a data brochure to get you going, contact your nearest Motorola sales office or authorized distributor. Or write to Motorola Semiconductor Products, Inc. P.O. Box 20912, Phoenix, AZ 85036 — or use the coupon, below — for the CMOS microcomputer solution for your INNOVATIVE SYSTEMS THROUGH SILICON.
FROM PETROCHEMICAL PROCESSING TOUTILITY SYSTEMS

FLIC PUTS YOUR SYSTEM IN CONTROL

FLIC software links your system with the world of process monitoring and control. A highly interactive, distributed software system, FLIC combines real-time monitoring and control with exceptional user friendliness. And FLIC’s modularity and configurability allow you to target your control system to a broad spectrum of vertical markets, from petrochemical processing to utility systems.

FLIC’s preprogrammed, “fill-in-the-blanks” functions allow a user to define control strategies and configure the system to a plant’s exact process control needs, without programming. A complete real-time FORTRAN facility is included, should special programs be required.

FLIC features a unique facility for user-creation of graphic CRT display formats tailored to a specific plant and process. FLIC’s friendly man-machine interface utilizes simple commands and color graphics for maximum ease of use. FLIC supports a variety of operator interface aids, including touch screens, function buttons, track balls and joysticks.

Designed for use with DEC and MODCOMP operating systems, FLIC supports input/output equipment of most major manufacturers. FLIC can be implemented in hardware environments ranging from single, standalone computers to highly available, hierarchical computer networks.

Since 1972 FLIC has provided process control technology to industry, with over 80 systems installed worldwide. Now merged with Quadrex and its expertise in the exacting field of nuclear power generation, Quadrex FLIC Computer Systems, Inc. offers you the advantage of a complete software system for every process control requirement.

For a demonstration of the FLIC system, and more information about OEM agreements, please call Tim Pellegrino at (609) 924-3900.

AVAILABLE ON DEC

QUADREX FLIC COMPUTER SYSTEMS, INC.
TWELVE BITS ARE USUALLY BETTER

Processor architectures need not come in multiples of eight. The pluses of 12-bit architectures are many and include streamlined instruction sets and a large memory range.

by Robert C. Sanford

Microprocessors have come a long way in just 10 years, and predictably, many features and functions have been added to them during that time. The most recent entries sport features designed specifically for multiprocessing and memory management. Yet, most microprocessors have followed the architectural precedents laid down by the 8008. As a result, today's processors suffer from several serious limitations.

First, the microprocessor units (MPUs) are Von Neumann structures centered around memory. The central element, however, should be the arithmetic logic unit (ALU), since it alone permits computation. Second, buses are multiplexed both internally and externally for direction and sometimes functions such as address and data. The chief reason for external multiplexing is that MPUs are pin limited; this is because MPU manufacturers will not use larger packages. Third, because data are handled in ASCII, all MPUs are based on a *de facto* 8-bit byte. (An 8-bit byte allows only 256 different instructions of all types, but even 16-bit MPUs do not offer enough different instructions.) In addition, most

MPUs use a general register bank instead of dedicated registers. These banks are often random access memories (RAMs) because regular, orthogonal layouts use less silicon.

Consider the following as well: basic address space, 16K, requires 2 bytes (1 word for a 16-bit MPU) for addressing. Expansion or segmentation requires at least 1 more byte. Newer MPUs with more complex instructions require more than 1 byte for some instructions, plus an address. This complicates programming and, as a result, some desirable or useful functions are unavailable. Finally, more emphasis is placed on how much read only memory (ROM), RAM, and input/output (I/O) are squeezed onto a chip than on what functions are available.

Perfectly viable computers have been produced using 4, 8, 12, 16, 18, 19, 21, 24, 32, 48, 56, and 64 bits as a word length. Before ASCII, most word lengths were multiples of 6 bits because most data were in IBM 6-bit code. Now, MPUs are based on multiples of 8 bits. This need not be the case, however. Nontraditional designs have many advantages.

Robert C. Sanford is an electronics consultant. His office is located at 512-D Sandra Ave, Arcadia, CA 91006. Mr Sanford is responsible for digital, microprocessor, and analog design on contract. Previously, he was a senior engineer for Resdel Engineering. He holds a BSEE from the University of Missouri.
Breaking with tradition

A first break with tradition is choosing a 12-bit byte. This design uses only 48 pins of a 64-pin package. The 12-bit byte is ideal for the popular 12-bit digital to analog and analog to digital converters. Twelve bits also allow up to 4K different instructions. In such a scheme, 4K of memory can be directly accessed.

By treating this 4K of basic memory as a page, all MPU memory reference instructions can work over it with just 1 address byte. As shown in Fig 1, the first bit in each instruction determines whether an address uses 1 byte (direct) or 2 bytes (extended) addressing. A 1-byte direct address provides a full 4K MPU. To gain direct access to 16M bytes, change that 1 bit in any memory reference instruction and use 2 address bytes.

For direct addressing, the most significant address byte goes out as all zeros. Two-byte addresses are used when the bit is set for extended addressing. Using special instructions PGE (page) and NPG (no page) permits the use of only 1 address byte. PGE locks up the most significant byte so that any following instructions require only 1 address byte. The MPU appears to have an address space of 4K, but that page can be placed in any 4K memory area. NPG returns the MPU to normal. This places a useful part of memory management inside the MPU where it belongs.

The next 3 bits offer eight choices, six of which are addressing modes for memory reference instructions. The other two choices provide register indirect addressing and nonmemory instructions. The remaining 8 bits offer 256 different instruction types. In addition to direct or extended memory addressing, that first bit allows two types of register indirect addressing and doubles the 256 nonmemory types. In total, there are 512 nonmemory, 512 register indirect, 1536 direct address, and another 1536 extended address instructions possible.

Complementary metal oxide semiconductor (CMOS) memories, both RAM and erasable programmable read only memory in N x 1 and N x 4 configurations, are ideal for 12-bit schemes. These structures keep the data inputs and outputs separate. Beyond 4 bits wide, memories multiplex inputs and outputs. Even though there are many byte-wide (8-bit) CMOS memories available, some studies of future memory use indicate that the two traditional structures will find continued use in large memories.

A second break with tradition is prohibiting both internal and external bus multiplexing (Fig 2). This means there are no 2-way buses and no sharing of data and addresses on MPU pins. Since a bus can only pass information in one direction at a time, multiplexing for direction or function only slows down an MPU. Data enter from the outside on one data bus to either memory register M or instruction register I and exit to the outside on a separate data bus that features 3-state drivers. The 24-bit address bus, which also has 3-state drivers, is not shared with data.

The MPU's row of registers has an input side and an output side. A single letter identifies each register as required by the assembly mnemonic code. At the left is register M, which accepts memory output whenever it is not functioning as an instruction byte. At the top of Fig 2, there are two buses feeding the ALU at the far right. Note that all paths funnel through the ALU since it is the one element that lets the MPU compute. Data on one bus can only be added or passed through by the ALU. On the other bus, data can be added, subtracted, passed, or inverted (complemented). Logic functions AND, OR, and XOR use both buses while other instructions use one or both buses.

When Xs are located near buses and register inputs, they represent CMOS transmission gates. All the gates feeding a particular bus form a multiplexer. This, however, does not add multiplexing to the MPU because data are only going one way. In CMOS, such a multiplexer is conventionally made from transmission gates instead of logic gates. This is done because the transmission gates are simpler to work with, much faster, and can also be used for analog signals.
Fig 2 In the proposed 12-bit architecture, bus multiplexing is avoided in order to improve performance. All data paths funnel through the ALU via two special function buses. A high performance ALU is essential in such a scheme.

An architecture rich in registers
In the 12-bit MPU, data from any register must pass through the ALU; that is why a high speed ALU is so important. Every instruction causes a transfer from one or two registers through the ALU to some other register, which can be one of the two sources. The bypass bus in Fig 2 is only used during some swaps and for some addresses in special instructions.

Register M holds memory outputs and feeds both sides of the ALU so that the ALU sees memory as just another register. An instruction can use M as easily as any other register. Arithmetic or logic functions called out by the instruction can occur on a transfer to or from memory just as easily as between registers. This fosters many new types of instructions.

Remember that in a mainframe, mini, or MPU computer, a register is a place to store data or an address. If it is expected to count—to be incremented or decremented—the register's contents must be passed through an ALU or separate incrementer/decrementer and then back to the register. This ties up other hardware and takes time. The 12-bit MPU uses true hardware counters. They can count faster, and count while the ALU is doing other things. Register E is a down counter while P, S, X, Y, and Z are all 2-byte up/down counters because they deal with addresses.

If data in a conventional computer are to be shifted right or left they must go from a register, through some shifting device, and back to the register. In MPUs, the shifter has usually been a set of gates to shift left 1 bit, pass through data unchanged, or shift right 1 bit, sometimes as part of the ALU. Another scheme uses a hardware shift register somewhere in the data path. This register can provide multibyte shifts.

Accumulators A and B can be used separately or together as double-width accumulator D. Since shifting is an accumulator function, A and B are true hardware shift registers. Data can be shifted in the register while the ALU is occupied. Rotate and shift instructions can control A alone (short shifts) or both registers as D (long shifts).

The memory register, program counter, and accumulators are designated M, P, A, and B. Transparent register T stores temporary results from the ALU and is unavailable to the programmer. It is
useful during outputs to slower memory. Flags are in condition code register F.

Free registers G and H, forming part of the 12-bit MPU, provide scratchpad capability and programming flexibility. These can be used either separately or together as double-width register K. Many instructions manipulate data into and out of these registers. Except for shifting, they are full accumulators.

Another powerful programming tool is an index register. With traditional or true index registers, a direct address is read from memory and an offset value stored in the register is added to the contents in order to create an effective address. If the offset is zero, the program goes where the address stored in memory dictates. With some exceptions, MPUs depend heavily on register indirect addressing. This is inverted traditional indexing. Not many MPUs offer traditional indexing.

Register X in the 12-bit MPU is a true index register. It feeds the ALU plus/minus bus so that its contents can be added to any address register or to memory register M. Register X deals with addresses and reaches all of memory. It is a 2-byte up/down counter. Any single byte address can be indexed anywhere in memory. If the most significant byte of X is zero, only one addition will be performed to speed up throughput.

Register S is the stack pointer for the 12-bit MPU. It handles addresses and must be incremented and decremented, so it is a 2-byte up/down counter. Various instructions allow S to be used for program purposes.

Address pointers are also extremely useful. Providing traditional indirect addressing—not register indirect—allows any memory location to be used as a pointer. Register Z is used to hold indirect addresses. In addition, address register Y is used for register indirect addressing. Address register Y is another 2-byte up/down counter.

Register Y can also move data memory to memory. In this case, Z holds the destination address and Y holds the source address. Since both are counters, clocking them lets the programmer go through a block of addresses. A simple protocol when using instruction MFM (memory from memory) allows single or block transfers. Since Y can be manipulated with several instructions, it can be an indirect addressing register for programmers who prefer that mode.

Counter E keeps track of how many blocks of data are transferred. Since blocks can be up to 4K bytes long, an entire page can be transferred. Counter E is also a true down counter. It can be directly loaded with a number instead of requiring a complement. The letter E does not stand for anything in particular but can be considered as enter count. If E’s contents are zero, instruction CNT (count) loads the following byte into E. If it is not zero, CNT decrements E. This single instruction is used for both loading and counting. A flag in register F is set whenever E is not zero and reset when E is zero. A jump instruction permits a program to sample for a zero count so that E can be used as a conventional programmable counter up to 4K bits. It is also used internally during multiply, divide, normalize, and shift instructions.

Flag register F differs from the other registers. It consists of flipflops that can be individually set or reset by the results of ALU and shift operations, and various instructions. Bits C, S, V, and Z are the usual flags found in MPUs in a condition code or flag register (Table 1). Bit F is a true flag and is available on a package pin as both an input and an output. The only requirement is that the external line must be treated as a bus and kept tri-stated except when it is actively driven. It can be read at any time. Although this does multiplex a pin, at least two more pins would be needed to control the flag without multiplexing.

This 12-bit MPU now includes all the functions necessary for a truly versatile microprocessor. Data registers A, B, G, H, and M feed both ALU buses so that arithmetic or logic can occur on any instruction. Registers E, F, P, and S require only straightforward transfers. They feed only the plus only bus. Meanwhile, X feeds the other bus, and its contents can be added to memory and addresses. Registers T and Z are unavailable to the programmer.

Another register the programmer cannot use is instruction register I. It accepts memory outputs during instruction fetches and consists of two levels of transparent registers that create a 2-stage fetch pipeline. An instruction from memory falls through immediately to I₁ where it feeds the decoding and control hardware. If the decoded

---

**TABLE 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Flag flipflop (available on a pin)</td>
</tr>
<tr>
<td>C</td>
<td>Carry bit</td>
</tr>
<tr>
<td>S</td>
<td>Sign bit</td>
</tr>
<tr>
<td>V</td>
<td>Overflow (signed arithmetic)</td>
</tr>
<tr>
<td>Z</td>
<td>Zero</td>
</tr>
<tr>
<td>E</td>
<td>Counter E contains a count</td>
</tr>
<tr>
<td>B</td>
<td>BCD mode</td>
</tr>
<tr>
<td>I</td>
<td>Interrupt enable</td>
</tr>
<tr>
<td>H₁</td>
<td>Half-carry (low-order decade)</td>
</tr>
<tr>
<td>H₂</td>
<td>Half-carry (middle decade)</td>
</tr>
<tr>
<td>P</td>
<td>Page mode</td>
</tr>
<tr>
<td>A</td>
<td>ASCII pack mode</td>
</tr>
</tbody>
</table>
FOR MULTIBUS AND EXORCISER COMPATIBLE BOARDS...

NOBODY MATCHES BURR-BROWN!

When you need I/O boards, there is one place to call. Burr-Brown.

**SELECTION**
Over 35 boards compatible with Intel Multibus alone . . . 30 with Motorola EXORciser, DEC LSI-11, and Zilog.

**QUALITY**
Each board is made with the technical precision and reliability that has become our trademark worldwide, because every board is burned in at 70° centigrade for 120 hours.

**PRICE**
You can have the exceptional performance and selection of Burr-Brown at a price that's competitive with anyone ...and a full-year warranty to back it up.

### MICROCOMPUTER INPUT/OUTPUT BOARDS
#### INTEL AND NATIONAL MULTIBUS COMPATIBLE
Intel ISBC80 and IS80, ICS80 and MIPS8000, National BL80 and Starplex, and other Multibus Systems.

<table>
<thead>
<tr>
<th>MODEL NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP8418-PGA</td>
<td>15-channel Differential/31-channel single-ended, Fixed gain, 12-bit.</td>
</tr>
<tr>
<td>MP8418-PGA</td>
<td>15-channel Differential/31-channel single-ended, Programmable Gain, 12-bit.</td>
</tr>
<tr>
<td>MP8418-AO</td>
<td>15-channel Differential/31-channel single-ended input, Fixed Gain, 12-bit, 2-channel output, ±10VDC, 12-bit (individual DACs)</td>
</tr>
<tr>
<td>MP8418-PGA-AO</td>
<td>15-channel Differential/31-channel single-ended input Programmable Gain, 12-bit, 2-channel output, ±10VDC</td>
</tr>
</tbody>
</table>

**ANALOG INPUT/OUTPUT**

#### ANALOG INPUT

<table>
<thead>
<tr>
<th>MODEL NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP8316-I</td>
<td>16-channel 0-20mA, 12-bit (common DAC).</td>
</tr>
<tr>
<td>MP8316-V</td>
<td>16-channel ±10VDC, 12-bit (common DAC).</td>
</tr>
<tr>
<td>MP8840</td>
<td>16-channel RTD 1-wire (100 ohm or 1000 ohm).</td>
</tr>
<tr>
<td>MP810</td>
<td>24-channel Dry-Contact Closure, 1.5mA Wetting Current at 24VDC.</td>
</tr>
<tr>
<td>MP902</td>
<td>32-channel Relay, 0.5A at 28VDC</td>
</tr>
<tr>
<td>MP830-72</td>
<td>72-channel TTL levels. User configured in 8-channel increments of inputs or outputs.</td>
</tr>
</tbody>
</table>

**DISCRETE INPUT/OUTPUT**

- **MOTOROLA EXORCISER COMPATIBLE**
  - Motorola Exorcerer, Rockwell System 65 and Synertek Systems.
  - **ANALOG INPUT**
    - MP7217: 16-channel, single-ended, Fixed Gain, 12-bit.
  - **DISCRETE OPTICALLY ISOLATED INPUT**
    - MP7120: 24-channel Dry Contact Closures, 1.5mA Wetting Current at 24VDC.
  - **DISCRETE REED RELAY OUTPUT**
    - MP702: 32-channel relay, 0.5A at 28VDC.
  - **DEC LSI-11 COMPATIBLE**
    - LSI-11, -112, -11/23 PDP 11/03, 11/23
    - **ANALOG INPUT**
      - MP1216-PGA: 16-channel Differential/32-channel single-ended, Programmable Gain, 12-bit.
    - **ZILOG 280 COMPATIBLE Z80, MCS**
      - **ANALOG INPUT/OUTPUT**
        - MP2216-AO: 16-channel Differential/32-channel single-ended inputs, Fixed Gain, 12-bit, 2-channel ±10VDC outputs, 12-bit (individual DACs).
instruction does not require a memory access, the MPU fetches the next instruction, which stops in $I_1$ until the present instruction is completed.

On the ALU input buses (Fig 2), either or both buses can be fed from ground during certain instructions, as in other MPUs. An input to the plus/minus bus is marked "6's." When adding or subtracting packed binary coded decimal (BCD) numbers with a binary adder, some answers will be wrong. Most MPUs have a decimal correction instruction that adds six units to each BCD decade (10 units) where a carry-out occurs. This carry-out is usually called H and appears as a half-carry flag in the condition code or flag register. Since the 6's to the plus/minus bus makes it easy to correct for subtraction as well as addition.

Dealing with BCD

A large amount of data moving to and from memory is in BCD but buried within ASCII characters. Whether an MPU uses an 8- or a 12-bit byte, only the 4 least significant bits (LSBs) are of interest for BCD. A byte must be brought in, masked, and packed before BCD arithmetic can be performed. Special added instructions RRH (right rotate Hex) and LRH (left rotate Hex) rotate accumulator A 4 bits at a time to aid in packing and unpacking BCD decades, but do not change the need for masking.

In Fig 2, the star alongside the input to M and another above the data output drivers represent a special function that instruction BCD enables and BIN (binary) disables. When BCD is active, all but the 4 LSBs of data memory or I/O are gated to prevent any data from getting to M. The inputs to M are clamped to zero. ASCII BCD characters are masked on the way in.

By using instruction AOM (A ORed with memory), the BCD decade in M is ORed with A on the way into A. An RRH instruction then rotates the decade to the 4 most significant bits (MSBs) of A. Packing three BCD decades is thus much faster than the conventional MPU way.

The other star above the data output drivers indicates that during BCD conditions all but the 4 LSBs are gated and the driver output is a true ASCII character. A binary three (0011) is gated out of the middle decade to form the ASCII character and the 4 MSBs are gated out as zeros. Unpacking reverses the packing scheme by using MFA (memory from A), and by LRH rotating the decades the opposite way. Instead of the usual masking and merging steps required by most MPUs, this method translates ASCII to packed BCD and back again to ASCII with I/O gates and versatile instructions.

Bit F can also be controlled with the program. It can be set and reset directly. Jump instructions allow sampling for program decisions. In addition, bit F is the MSB of register F. If the contents of register F are transferred to A, the bit F appears in A in the sign-bit position and can be manipulated by all the instructions dealing with the sign. This flag is intended for control of or by external hardware. It can be used to provide a serial I/O capability.

Flag bit E indicates the contents of counter E. It is set whenever E contains a count and reset when E is zero. Jump instructions allow bit sampling to use counter E as a conventional counter. Bit B simply indicates that the MPU is in the BCD mode. It is set by BCD and reset by BIN.

When bit 1 is set, all interrupts are accepted. When it is reset, NMI is still accepted but IRQ and INT are disabled. Bits H₁ and H₂ are decade carry-outs from the ALU and are used internally for decimal correction.

Bit P indicates the page mode. When P is set, the most significant byte of an address is locked to its present value, and all extended 2-byte addresses are held to one 4K address space determined by the locked upper byte. Here, E is programmed for extended addressing. One address byte is used. If the lowest 4K space (zero page) is desired, programs for direct and again use 1 address byte. This permits the programmer to move between the zero page and any other page. Full control without paging is retained using normal direct and extended addressing.

Bit A (for ASCII) is set by instructions PCK (pack), UPK (unpack), and reset by NPK (no pack). To overcome the inefficiency of a 12-bit byte for ASCII characters, PCK and two start addresses (they can be on different pages) are programmed to set up a memory to memory transfer with special conditions. Three ASCII inputs are packed into 2 bytes inside the MPU and stored in memory as 2 bytes instead of 3. Either address can, of course, be an I/O function. Programming UPK and 2 addresses does the opposite; each of 2 inputs is unpacked and stored in memory as 3 ASCII bytes. Instruction NPK returns the MPU to normal from either mode. Programs containing long strings of ASCII characters to be stored or unloaded can use this pack mode macro.

Providing lines for adequate control

Table 2 shows the control functions in a 64-pin package. As in all modern MPUs, two leads are provided for a crystal to control an internal oscillator. One of these lines can also be used as an input for an external clock. This signal is divided down sufficiently to provide all the internal MPU timing signals.

Reset involves clearing registers E, F, and P. Register E is cleared to get a zero count to agree with its flag bit in register F. Clearing F allows the MPU to escape from all special conditions and to inhibit interrupts. Register P is cleared so that it contains address zero, which is the usual restart vector where the starting address of a program is placed.
Microterminal: small, smart, tough ... easy to install ... simple to interface and operate - the logical, space saving substitute for bulky, fragile CRT's!

Rugged and water resistant for in-plant use - uncomplicated keyboards plus bar code wand and mag stripe reader options are perfect for factory data collection. Priced for OEM's and styled to enhance control consoles.

Serial ASCII (110 to 19,200 baud). RS-232-C, RS-422 and 20mA current loop communications. Only 8.5" x 4.5" x 0.6" and priced from $192.00. Request new full line Microterminal brochure.

Data Acquisition and Control Systems Division
3631 E. 44th Street, Tucson, AZ 85713 (602) 747-0711

<table>
<thead>
<tr>
<th>Model</th>
<th>Alpha Display Characters</th>
<th>Baud Rate</th>
<th>Data Buffers: Characters</th>
<th>Keyboard</th>
<th>Function Keys</th>
<th>Features</th>
<th>Supply Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>TM71</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) Alpha</td>
<td>14</td>
<td>Full feature</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM77</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) Numeric</td>
<td>14</td>
<td>Larger keys</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM77-I/O</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) Alpha</td>
<td>14</td>
<td>TTL I/O</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM77-I/O</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) Numeric</td>
<td>14</td>
<td>Larger keys</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM71B</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) 5 x 50(2) Alpha</td>
<td>16</td>
<td>Bar Code</td>
<td>+24VAC/DC</td>
<td></td>
</tr>
<tr>
<td>TM71MS</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) 5 x 50(2) Numeric</td>
<td>16</td>
<td>Wand Mag Stripe Reader</td>
<td>+24VAC/DC</td>
<td></td>
</tr>
<tr>
<td>TM77B</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) 5 x 50(2) Numeric</td>
<td>16</td>
<td>Bar Code</td>
<td>+24VAC/DC</td>
<td></td>
</tr>
<tr>
<td>TM77MS</td>
<td>16</td>
<td>110-19200</td>
<td>320(1) 5 x 50(2) Numeric</td>
<td>16</td>
<td>Wand Mag Stripe Reader</td>
<td>+24VAC/DC</td>
<td></td>
</tr>
<tr>
<td>TM71M</td>
<td>16</td>
<td>110-9600</td>
<td>320 Alpha</td>
<td>14</td>
<td>Military</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM70</td>
<td>12</td>
<td>300 &amp; 1200</td>
<td>36 Alpha</td>
<td>8</td>
<td>Low cost</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM76</td>
<td>12</td>
<td>300 &amp; 1200</td>
<td>36 Numeric</td>
<td>8</td>
<td>Larger keys</td>
<td>+5VDC</td>
<td></td>
</tr>
<tr>
<td>TM25</td>
<td>8</td>
<td>300</td>
<td>8 Numeric/Hex</td>
<td>7</td>
<td>Low Cost</td>
<td>+15VDC</td>
<td></td>
</tr>
<tr>
<td>TM27</td>
<td>8</td>
<td>300-4800</td>
<td>8 Numeric/Hex</td>
<td>6</td>
<td>Low Cost, polled</td>
<td>+8 to +12VDC</td>
<td></td>
</tr>
</tbody>
</table>

1. Two 80-character input buffers - two 80-character output buffers. 2. 5 x 50-character buffers also included for bar-code and magnetic-stripe reader data. 3. User programmed.
This requires the first 2 bytes in page zero to serve as a 2-byte address so that the program can start anywhere specified in memory. Address zero can also be reached by the RES (reset) instruction.

External flag line F (described earlier) and R/W are used for data direction. This 12-bit MPU has three interrupt lines. NMI and IRQ are 6800-type interrupts that automatically save all registers (15 bytes) before acknowledging the interrupt and vectoring to the interrupt routines. The only difference is that NMI cannot be inhibited by flag bit 1 as IRQ can; they also use different vectors.

Line INT is a different type of interrupt. It stores only F and P before acknowledging, tri-states the address bus, and then waits for a 24-bit address on the address lines, somewhat like the 8080 scheme. This provides a faster interrupt and lets the programmer decide what other registers, if any, are to be saved.

When line ACK acknowledges an interrupt, it goes high during the first instruction fetch after automatically saving registers. If the interrupt is INT, ACK can be used to gate a 24-bit address onto the address bus, and point to the start of the interrupt program. This same line acknowledges direct memory access (DMA) and holds inputs. During a DMA request, ACK remains high as long as the buses are tri-stated for external signals, and acts as a BA (bus available) line. During HOLD, ACK stays high as long as the MPU is inserting wait cycles and is effectively in a halted state. Thus, the buses are unavailable. Since CMOS is completely static, HOLD can insert wait cycles indefinitely and be used as a HALT line.

The line marked ENA carries a hybrid signal. It is timed so that the leading edge occurs after the address lines have been stabilized. This line can be used to latch addresses into memory or I/O. The trailing edge matches the trailing edge of the CL (clock) line much like the valid memory address line of a 6800. This lets it externally latch data. The remaining available line indicates the instruction fetch cycle. This information is available with many MPVs. It is useful in timing external hardware such as memory management circuitry and code disassemblers.

What is in a mnemonic?

In general, the mnemonic code follows some simple rules based on this hardware concept and allows hundreds of instructions in a fairly regular set. The most common abbreviations are used for the exceptions. Some functions and programming tricks have been added that do not appear in any other MPU. For instance, any memory reference instruction can use any address mode.

Each instruction mnemonic consists of three letters. Table 3 defines each letter. Each register is
Test System Solutions; Boxed And Ready To Go!

Full line of Multibus compatible I/O cards:
- Voltage input (including thermocouples)
- Current input
- RTD inputs
- Pulse inputs
- Discrete inputs from TTL to 220VAC
- Voltage output
- Current output
- Discrete outputs from TTL to 220VAC
- Serial RS-232 and current loops up to 8 channels for operator and system interfacing

64K RAM memory
Programmable in Microsoft BASIC or UCSD Pascal

Tired of configuring, assembling and programming board level systems for each new product test setup?

There's an easier, more practical solution: CS400 Series - a complete, fully assembled and tested controller with the versatility to handle a host of test routines. It includes Multibus™ compatible I/O board options with interface software plus user friendly programming in familiar Microsoft™ BASIC or the UCSD p-System™. CS400 Series keeps program and data storage on 5 1/4" diskettes plus microcassette options. A Centronics compatible printer port is standard and an internal 40-column printer is optional.

Put all your product test system requirements in one desk-top or rack mount package from one proven source. Request descriptive brochure.

Data Acquisition and Control Systems Division
3631 E. 44th Street, Tucson, AZ 85713 (602) 747-0711

TOMORROW'S SOLUTIONS TODAY
identified by a single letter. The first letter in an instruction can stand for a register, a shift direction, a flag bit, or a jump. The middle letter can be an ALU function, a type of shift, or a jump condition. The last letter can be a register, a flag bit, or a numerical value of unity (one) or zero.

Most instructions are register to register transfers so that the first and last letter represent registers. The first is always the sink, where the data end up. It can also be a source, or one of two sources. The last letter of an instruction can either be the same register, a second source, or a value. Data must always pass through the ALU, and the middle letter determines what happens to it. Data can pass, be inverted, or be complemented. The ALU can add, subtract, or perform logic. Each function is represented by a letter, so an instruction tells where the data will end up, where they came from, and what happens to them, all with just three letters.

In the 12-bit MPU, register M, which can be treated like any other source register, stores data input from memory. Temporary register T (unavailable to the programmer) stores outputs to memory that are referenced as M. For all programming purposes, memory looks like any other register.

Some examples of the format would be AFM, APM, ALM, AAM, AOM, and AXM. These examples load A from memory, performing the functions From, Plus, Less, AND, OR, and XOR on the way. Reversing A and M would do the same while storing A. All these and many more can be used with any data registers, single or double. They and X and Y can be incremented (XPU), decremented (YLU), set to all 1's (AGU), or reset (MGZ). Address registers P and S need only From (SFP) and Swap (PSS). These instructions total 202 plus 112 memory-reference types.

In the hardware, a reset line sets P to zero, and the MPU to address zero. The reset line also resets F to clear all special conditions. Instruction RES does the same thing. Both the line and the instruction reset (restart) the MPU at the address contained in memory locations zero and one.

Two instructions from the 6800—SWI and WAI—are included. These 2 instructions stack all 15 registers. SWI goes to its own vector location immediately while WAI simply halts operation and waits for an interrupt. WAI has its own vector location. Even if the interrupt is INT, the registers are already stacked, and the programmer can enter the interrupt program immediately, without worrying about saving registers. Return from any type of interrupt is RTI.

There might be some unfamiliar instructions in Table 4 (eg, CNT, which was explained earlier). In general, floating point instructions are not suitable for this MPU, but some users may want floating point capabilities. To make that easier, instructions NMZ and NRM are included. Instruction NMZ causes accumulator A or D, whichever is selected, to shift left until the sign bit differs from its right-hand neighbor and then to stop. The accumulator holds the normalized number and sign while counter E holds the exponent, or number of shifts. Instruction NRM reverses this action, shifting right until counter E holds zero and extending the sign. Writing a floating point routine should be quite simple.

Input from memory or I/O goes to register M. On the way, some gates are put on the upper 8 bits. These bits are used by instructions BCD and PCK.
Last seen the Zax 8086-8088 Emulator offers more features than any other stand alone in-circuit debugger available. Watch for 8086 and 8088 emulation to 8 MHZ, plus 8086-8087 and 8088-8077 co-processor emulation to 5 MHZ.

Some of the standard features to look for on the Zax ICD-178/8086-88 Stand Alone Emulator are 128K of mappable memory (expandable to a full 1 Megabyte), 13 breakpoints, in-line assembler for code patching, full upload/download to host computers with no special software, displays in Hex/ASCII or disassembled code, and a 2K x 80 real time trace buffer. Also runs in either MIN or MAX modes. To assist you in software debugging and system integration, there are 30 different debugger commands.

If you have seen, or would like to see this or any of the other Zax emulators call 800-421-0982.

Zax Corporation
8311 Westminster Ave., Westminster, California 92683
Toll Free 1-800-421-0982  CA, HA, AK 714-898-2373
**TABLE 4**

<table>
<thead>
<tr>
<th>Mnemonics</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCD</td>
<td>Memory input accepts only lowest 4 bits; outputs BCD or Hex in true ASCII format</td>
</tr>
<tr>
<td>BIN</td>
<td>Binary mode; returns to normal from BCD mode</td>
</tr>
<tr>
<td>CMP r</td>
<td>Compare register; subtracts register from accumulator A but does not change A</td>
</tr>
<tr>
<td>CNT</td>
<td>Count; if flag bit E is set, decrements counter E; if flag bit E is reset, inserts following byte as contents of counter E</td>
</tr>
<tr>
<td>COR r</td>
<td>Correct register; uses flag bits H and L for decimal correction of packed BCD</td>
</tr>
<tr>
<td>DIV</td>
<td>Unsigned 24-/12-bit division</td>
</tr>
<tr>
<td>DVD</td>
<td>Signed 24-/12-bit division</td>
</tr>
<tr>
<td>ENB</td>
<td>Enable interrupt; sets flag bit I</td>
</tr>
<tr>
<td>HLT</td>
<td>Halt MPU operation; waits for interrupt or reset</td>
</tr>
<tr>
<td>INH</td>
<td>Inhibit interrupt; resets flag bit I</td>
</tr>
<tr>
<td>JMP</td>
<td>Unconditional jump to effective address</td>
</tr>
<tr>
<td>JSR</td>
<td>Jump to subroutine at effective address</td>
</tr>
<tr>
<td>LRH</td>
<td>Left rotate Hex</td>
</tr>
<tr>
<td>MPY</td>
<td>Signed 12- by 12-bit multiply</td>
</tr>
<tr>
<td>MUL</td>
<td>Unsigned 12- by 12-bit multiply</td>
</tr>
<tr>
<td>NMZ r</td>
<td>Normalize register A or D; shifts left until sign differs from next bit; counter E holds exponent</td>
</tr>
<tr>
<td>NOP</td>
<td>No operation; increments program counter</td>
</tr>
<tr>
<td>NPG</td>
<td>No page; returns to normal from page mode</td>
</tr>
<tr>
<td>NPK</td>
<td>No pack; returns to normal from pack mode</td>
</tr>
<tr>
<td>NRM r</td>
<td>Normal; reverses normalize procedure</td>
</tr>
<tr>
<td>PCK</td>
<td>Pack mode; masks inputs and packs 3 ASCII characters into register D, then outputs 2 packed bytes</td>
</tr>
<tr>
<td>PGE</td>
<td>Page; locks upper byte of program counter P and address register Z so that extended addresses require only 1 byte</td>
</tr>
<tr>
<td>PSH r</td>
<td>Push register onto stack; advances stack pointer S</td>
</tr>
<tr>
<td>POP r</td>
<td>Pop top of stack to register; decrements stack pointer S</td>
</tr>
<tr>
<td>RES</td>
<td>Reset MPU to address zero; same as reset line</td>
</tr>
<tr>
<td>RRH</td>
<td>Right rotate Hex</td>
</tr>
<tr>
<td>RTI</td>
<td>Return from interrupt</td>
</tr>
<tr>
<td>RTS</td>
<td>Return from subroutine</td>
</tr>
<tr>
<td>SWI</td>
<td>Software interrupt; stacks all registers and vectors through SWI address</td>
</tr>
<tr>
<td>TST r</td>
<td>Test register; sets flags S or Z as tested; no effect on register</td>
</tr>
<tr>
<td>UPK</td>
<td>Unpack; inputs 2 bytes to register D, then outputs 3 ASCII characters</td>
</tr>
<tr>
<td>WAI</td>
<td>Wait for interrupt; stacks all registers and halts until interrupt or reset occurs</td>
</tr>
</tbody>
</table>

Outputs to memory or I/O are on a separate bus, with 3-state drivers. Another eight gates are included in these drivers. When programming BCD, the input gates hold off data on the upper 8 bits and insert zeros on those bits into register M. An ASCII BCD character is masked so that M stores only the 4 BCD bits.

Various instructions unpack the three BCD decades and output them one at a time to get ASCII BCD back. On the way, the gates in the output drivers turn the pure BCD back into ASCII BCD. To get back to normal inputs and outputs, program BIN and all the gates open. With BCD, the programmer must do the packing and unpacking. If a great deal of BCD arithmetic is used in a particular program, the function can go into a subroutine.

Extended addressing is indicated by an E after a memory reference instruction, followed by 2 address bytes. If PGE is programmed, the upper byte of program counter P and address register Z are locked. If a 1-byte direct address is used, it will still go into the first 4K or zero page. If E is programmed, 1 address byte can still be used, and the address will be in the 4K page indicated by the locked upper byte P or Z.

It is possible to jump around in memory by using 1- and 2-byte addressing or, by using PGE with only 1-byte addressing. To change any page but the zero page, program NPG, insert a new 2-byte address, then PGE again. This could even be put into an assembler as a pseudo instruction; program EA for extended address instead of E and the assembler takes care of inserting the new page number. NPG allows the MPU to escape from the page mode.

MFM allows the transfer of single bytes or strings of bytes between locations in memory or between memory and I/O. A simple protocol programs MFM, source address, CNT, number of bytes, and sink address. Since transferring only 1 byte would be cumbersome, the assembler could recognize a letter (eg, Z for zero) following MFM. Then, only MFM and two addresses are needed. Since this 12-bit MPU allows any addressing mode for any memory reference instruction, either or both of the addresses can be direct, extended, paged, indirect, or indexed. A block of memory can therefore be transferred from one page to another very easily.

**Addressing modes provide flexibility**

There are many addressing modes available in the 12-bit architecture. If E is not programmed after an instruction, it will be a 1-byte absolute address (direct). With E, the instruction needs 2 bytes. Indirect is selected by N after the instruction or after the E. This is a true indirect where the address in memory contains the effective address of the instruction instead of data. Indexed instructions are indicated by X. With this type of indexing, a 1-byte address can be put anywhere in memory. By using
indirect, a pointer in memory can point to a table. By adding N,X after an instruction, it goes indirectly through the pointer and the index steps it through the table.

Another useful addressing mode is program counter relative (P). In most MPUs, this mode is usually used for branches and is often unavailable to the programmer. An offset value is stored in memory and added to the program counter to form an effective address.

Most MPUs include immediate addressing. It is useful if the data are not changed during the program. The term immediate is used because the data follows immediately after the instruction, in place of an address. In earlier use, it replaced the address in a fixed length word.

The next two modes do not require a memory reference because the address is in register Y. Addressing register Y can be used like H and L registers in an 8080 or Z80. In the 6800 and others, this is called an index register and is indicated by X. Actually, however, it is an indirect addressing register like H and L, only it can also add an offset value stored in memory to the register’s contents. This forms an effective address. It is the reverse of true indexing. This mode is indicated as Y,X (register indirect, indexed).

An MPU built to these hardware guidelines from modern silicon gate CMOS can have greater throughput and outperform all existing CMOS MPUs. It will also give most N-channel metal oxide semiconductor MPUs a run for their money. Decoding and control for such an MPU should be relatively simple because the bit structure of instructions lends itself to simple decoding. The hardware should be equally simple to control.

In total, there are 260 nonmemory and 2310 memory reference instructions, including all memory modes. Undoubtedly, users will think of others that have been left out.

These innovative concepts for MPU design can be used to overcome the limitations of present MPUs. Although the concepts and techniques can be used in a 16-bit MPU, more pins are required. The input and output buses could be combined, but larger chip carriers are the right answer. An ALU in Schottky transistor-transistor logic (TTL) can be made very fast, so such an MPU could be built in TTL if desired. Remember, however, that any attempt to save silicon by changing any of the concepts is bound to slow down performance, limit capabilities, or both. In any case, the 12-bit concept is worthy of serious consideration.

Please rate the value of this article to you by circling the appropriate number in the “Editorial Score Box” on the Inquiry Card.

High 704  Average 705  Low 706
There's only one single-chip hard disk controller that really lives up to its name.

Ours.

μPD7261D

---

Theirs.

ST506

SMD

Sync Detector

FIFO

ECC
NEC’s single-chip HDC, the µPD7261D. It outperforms the competition one to five.

At NEC, we don’t think a single-chip HDC should require three or four extra chips to make it do all you want it to do. Obviously, not everyone agrees.

But, unlike the competition’s, our single-chip HDC has all the essentials built right in. Including control commands for both SMD and ST506 interfaces. ECC error detection. Sync detection. And even an 8-byte FIFO to compensate for DMA controller latency.

Not only does our single chip do more, it does everything better. For example, its data speeds are 20% faster than any other HDC (12MHz/SMD and 6MHz/ST506). It uses higher level commands so it needs less software. And it performs overlapped seeks, which means it can position read/write heads for more than one drive simultaneously.

Even more impressive is the versatility. You’ll be able to use the µPD7261D to control virtually any hard disk, from 5” Winchesters to 14” SMDs. And it can handle as many as 4 ST506 and 8 SMD disks at the same time.

Our controller is ready to save you time and space right now. And we’re fully second-sourced.

NEC is already famous for its floppy disk controllers (µPD765A for standards and minis; µPD7265 for microfloppies). Now we’re out to make a reputation for our µPD7261 Hard Disk Controller. The world’s first single-chip HDC that deserves its name.

For a data sheet, contact NEC Electronics, One Natick Executive Park, Natick, MA 01760, Attn: Hard Disk Controllers.
HERE'S THE TEN WE OWED YOU.
In 1978 Fairchild promised you a full family of high-speed, low-power FAST™ logic. And we meant it:

Introducing the 74F160, 161, 162, 163, 174, 192, 193, 299, 323 and 524. Everything from high-speed flip-flops to counters to registers, and even an 8-bit comparator. And all with the unmatched performance characteristics that make FAST the unmatched performance choice.

Now there are 63 ways to go FAST. We owed them to you. And you owe them to yourself. For the complete FAST Data Book, call or write Fairchild Digital Products Division, 333 Western Avenue, South Portland, Maine 04106.

**FAST**

**63 WAYS TO GO FAST.**

- 10 gates
- 10 multiplexers
- 9 flip-flops
- 9 arithmetic circuits
- 8 counters
- 5 decoders
- 5 drivers/transceivers
- 4 shift registers
- 2 latches
- 1 RAM
The Shortest Distance Between Your Micro and Data Storage.

DTC has what you want in Winchester controllers. Host adapters that match our controllers with all popular microcomputers. Winchester control plus streaming tape and diskette support. Backup control with selective direct tape access or automatic save/restore. Programmable for different Winchester models. For information, circle our readers' service number. For faster response, call (408) 496-0434. In the East, call (617) 275-4044.

DTC Drive enclosures and integration services can simplify your system needs.

Helping you manage information
Data Technology Corporation
2775 Northwestern Parkway
Santa Clara, California 95051
Tel: (408) 496-0434
East Coast (617) 275-4044
TWX: 910-338-2044

CIRCLE 69
ADVANCED DATA ACQUISITION AIDS THE HANDICAPPED

Computer based acquisition and analysis tools are providing pathologists and researchers with insight into the mysteries of the spoken word.

by Andrew Davis and Ari Berman

Speech—it is not only one of the most complicated stimuli that humans perceive, its generation is one of the most skilled activities people engage in. Thus, it is not surprising that ear, brain, or vocal system injuries can have devastating impacts on human functions. Although prosthetic devices and special training are available to help some of the hearing and speech impaired, help is often unavailable for many of the more severely impaired. Consequently, there is a continuing need to better understand speech perception and production in order to find new ways to prevent or treat speech and hearing handicaps.

Speech research is technically intensive and, by necessity, interdisciplinary. Several social, psychological, and biological factors are involved. An adequate understanding of speech mechanisms requires input from linguists, psychologists, ear-nose-throat physicians, neurologists, speech therapists, and audiologists. In addition, speech research requires expertise in technical areas such as acoustics, mechanics, electronics, and, lately, computer hardware and software.

Historically, limitations in these technical areas have most impeded progress. Studies of speech perception require precise control over the time and frequency properties of sounds. The speech signal must be systematically dissected and then recreated in various ways to examine each acoustic component's contributions. In addition, since speech production involves a complex interaction of acoustic, physiological, and mechanical processes, its study necessitates sophisticated measurement of muscle movements and an ability to synthesize speech gestures.

Technically, both these tasks are extremely difficult to perform. The earliest speech studies used tape, wire, or disk recordings, signal generators, analog filters, mixers, and switches to measure, manipulate, or synthesize speech. Unfortunately, even though people hear speech as a series of discrete elements called phonemes, it really consists of spectrally varying cues that overlap in time. For this reason, a simple filter cannot extract a single
varying cue, and an analog recording cannot be cut into segments corresponding to phonemes. Neither can speech production be cut into segments corresponding to phonemes, nor can it be studied by examining a simple linear combination of movements or vocal tract shapes.

However, the advent of computer based recording, editing, and synthesizing promises great advances. Computers allow scientists to digitally record natural speech signals and gestures. In addition, computers can perform the high speed calculations required to spectrally analyze signals or synthesize dynamic speech events. All this can be done while maintaining precise control over temporal and spectral details.

Unfortunately, using a computer in these contexts presents several problems. Unlike analog analysis, computer processing involves manipulation of discrete digital values stored in memory or on a mass storage device. This raises several design issues. For one, what are the memory and storage requirements for recording or synthesizing speech signals? Also, what digitization rates are appropriate and possible? And finally, how are hardware and software to be optimized for speech research?

In part, the amount of storage required depends upon the duration of the signal to be analyzed. The smallest speech segments that carry linguistic information are from 20 to 100 ms long. However, these segments ordinarily occur in the context of syllables or words that are up to 1 s long. This fact plays an important role in perception because overall speech segments contain temporally distributed, redundant information that increases speech intelligibility in noisy or distorted environments. This redundancy is particularly important to the hearing impaired, whose auditory systems add distortion. Thus, the study of speech segments in their natural environment requires digital samples at least 250 to 1000 ms long.

Two additional factors dictate durations longer than this, however. Since speech events occur rapidly, it is often necessary to record a signal window two or three times as large as the target event. An optimal window seems to be about 2.5 s wide. The second factor influencing duration is whether individual speech segments called suprasegmentals are to be studied.

Suprasegmentals are signal characteristics conveyed during relatively long sequences of smaller segments. They include the sentence intonation and amplitude contours and are typified by the difference between the utterance “You know why!” and “You know why?” Suprasegmentals also reveal emotional or psychological information. An increase in speech rate might signify heightened speaker anxiety. The study of suprasegmentals is particularly important for developing speaker-recognition systems. Analysis of suprasegmental features requires digitalization of utterances over a wide range of sample periods, from tens of seconds to minutes. The storage limitations of older computer systems demanded that suprasegmentals be studied by breaking large utterances into smaller, more manageable segments — a very tedious process. Today, the direct-to-disk system of storage greatly increases the efficiency and the flexibility of such analysis.

A powerful tool used in modern speech research is Data Translation’s DT4136 LAB-DATAX acquisition system. This unit provides high speed continuous data flow to microcomputer memory and/or disk storage. Based on a 16-bit computer, it includes the company’s specialized analog to digital (A-D) interface with its unique random access memory (RAM) channel file multiplexer, a digital to analog (D-A) interface, and a realtime programmable clock (Fig 1). Together with the package of FORTRAN callable subroutines, the system provides up to 250k-sample/s throughput to memory or 100k-sample/s throughput to disk without the loss of any interbuffer data points. The high disk throughput can be sustained until 36M bytes of disk storage have been filled. Hence, speech signals can be recorded for time periods well over 1 min.

The DT4136 LAB-DATAX used in signal processing applications includes an LSI-11/23 processor from Digital Equipment Corp; an advanced architecture A-D interface (the DT3382), providing up to 250-sample/s throughput with 12-bit accuracy; the DT3371 two-channel D-A converter with up to 400k-sample/s throughput; and a programmable realtime clock. Software components include the RT-11 operating system, FORTRAN compiler, and a continuous performance subroutine package (CPLIB), designed to be linked to a user’s FORTRAN application program. This subroutine package supports a maximum data buffer size of 98,048 samples, which is filled in .392 s if the A-D device is operating at top speed.

Real world data acquisition problems
Gathering data from an experiment or real world process with a microcomputer or minicomputer based data acquisition system has been traditionally limited to either slow data rates or small numbers of data points. These limits result from hardware and software constraints imposed by 16-bit architectures, instruction execution times, software designs, operating system overhead, and throughput-to-disk limitations. These limits arise not only when one signal must be sampled at a high rate, say 50 kHz, but also in seemingly modest multichannel situations. For example, sampling 16
Help your programmers respond to new applications. Free them from the ASCII code trap with the ANSI Intecolor 2405. When your users are demanding color and graphics to solve their applications needs, adding more non-ANSI terminals to your system is like chaining the hands of your programmers. If your new terminals aren't ANSI X3.64, you may be locked into a generation of non-standard application programs and protocols. Your programmers may have to write translation codes for each application you want to update. And that means less flexibility, plus increased programming costs.

ANSI X3.64, color and graphics at an unbeatable price. Now you can make the break to ANSI—the industry standard protocol with unlimited control sequences—and color graphics with the Intecolor 2405 for $1295, single-piece price. Your Intecolor 2405 is completely ANSI compatible. (It also includes all ASCII codes.) Best of all, the Intecolor 2405's brilliant color graphics will help you convey more information, more quickly, and with greater comprehension than monochrome.

All the VT100 features you need in a conversational terminal. Terminal-based vector graphics on an 80 column by 24 line screen. Baud rates from 50 to 19,200. English language setup with non-volatile setup memory. Two full pages of screen RAM. A precision in-line CRT with auto degaussing. A 6MHz 8085 microprocessor with four hardware interrupts. Plus an option for defining and storing 72 functions you can recall with a single keystroke.

For only $1195, you can get our compact, attached keyboard version. And you can mix and match, with quantity discounts starting at 25 terminals.

Act now. Get all the advantages of color, vector graphics and ANSI X3.64.

At $1295 it's a small price for freedom.

$1295. A small price for freedom.

For details, contact Marketing Communications at 404/449-5961, TWX 810 766 1581.

NOTE: If your P.O. is received by 5/31/83, you may take advantage of our introductory offer of $995 for a single evaluation unit (U.S. domestic only).
channels at 2 kHz per channel for 2 s requires a system level A-D rate of 32 kHz and the storage of 64k samples.

When A-D converters operate below 20k samples/s, the central processor can be called upon to directly manipulate the A-D interface, using programmed input/output data transfers. However, when acquisition rates of greater than 20 kHz are required, the A-D board must move the data to memory using direct memory access (DMA) I/O.

Usually, when an analog input signal is measured, a multiplexer is directed to switch to the specific channel. A sample-and-hold circuit is fed by the multiplexer's output. When the multiplexer has settled, the sample-and-hold circuit is allowed to sample the value. Now, actual A-D conversion can begin. The A-D trigger first switches the sample-and-hold to hold and then starts a successive approximation A-D conversion. Once the conversion is complete, an interface board makes a DMA request. When the A-D interface becomes bus master, data are transferred to memory. This process is repeated until a buffer of data has been acquired.

Once a buffer in memory is filled, its data must be written into a disk file while the A-D converter transfers data to a second buffer. When the second buffer is full, it will also be sent to the disk while the A-D converter again fills the first buffer. This mode of operation is called double buffering.

Memory buffer data can be moved into a disk file at very high rates. Unfortunately, the data can be transferred only when the disk's read/write head has been correctly positioned and an appropriate storage area on the disk surface has come under this head. The time required for each of these events to occur is highly variable. Therefore, each data buffer must be large enough to hold data until the previous data buffer has been written to the disk, or until the disk is ready to accept data from the new buffer. The entire data acquisition process resembles a series of pipelines: data conversion, transfer of data from the A-D interface to memory, and transfer of data from memory to disk.

The first pipeline is the A-D subsystem, which is capable of converting 250k samples/s. The second pipeline is the computer bus and the A-D interface board. When data are ready to be transferred to memory, the interface requests bus control. Because the DMA latency (i.e., the time between the DMA request and the DMA grant) can be more than 4 µs, the analog data word is moved from the A-D converter module to an onboard data buffer. Therefore, a second A-D conversion can begin almost immediately after the first is complete. The A-D interface will perform either single-word or double-word DMA transfers.

By transferring more than one word at a time, the time lost during the DMA arbitration can be averaged over more than one data transfer. The decision to transfer a single word, or a pair of words, is left to the very last moment. By waiting, the probability of performing a double transfer is maximized. A double-word transfer allows the onboard DMA to "catch up" when a DMA latency is unusually long.

Disk drive, the third pipeline, introduces a DMA latency factor far greater than that of other components. Adequate-sized data buffers are required to overcome the up to 40 ms delays encountered in
RESOLUTION
800 x 480 High Speed Quality Graphics.

TEKTRONIX 4014 EMULATION
Most all the Tektronix features are supported including:
4010 and 4014 Emulation, Plot 10 Compatible, 4096 by 4096
Addressable Plot Area, Variable Line Types, Point Plot,
Vector Plot, Incremental Plot, Write Thru Mode and built-in
crosshair cursor.

SPECIAL FEATURES
Selanar Native Mode Command Structure, Area Fill, Circle,
Arc and Box Commands.
Also variable scale factor for changing image size, relo­
catable origin, special write modes, switchable video.

SINGLE BOARD DESIGN
The SG480 is a small single board design (4.5 by 5 inches)
and simply plugs into the VT100 STP port. Only one small
cable is required. The SG480 comes with a replacement
CRT tube and attached yoke —simple installation without
critical adjustments.

DEC TERMINALS SUPPORTED
VT100, VT132. In addition Selanar has comparable prod­
ucts for the VT101 and VT102 plus other products for the
VT100, VT103, VT105, and VT180.

HARDCOPY
Hardcopy is standard for the DEC LA34 format. Options
currently available are for C.10h, Epson, Data South,
Texas Instruments, and Selanar's SG120 PLUS with DEC's
LA120.

OTHER SELANAR GRAPHICS™ PRODUCTS
Televideo 925, 950, 970, Lear Siegler ADM3A, 3A+, 5. Qume
QVT Series Terminals (Exclusive). DEC LA120.

SELANAR SG480
Sales and Marketing: 4212 N. Freeway Boulevard,
Sacramento, CA 95834 (916) 921-9700
transferring data to disk. The CPLIB software package utilizes a pair of data buffers, each of which is 8192 bytes long.

Despite careful integration of hardware and software, the maximum continuous throughput to disk of conventional systems is limited to approximately 10k samples/s. The switching process of conventional A-D interfaces imposes this limit. When a conventional A-D interface has finished filling a buffer, it stops acquiring analog data and issues an interrupt to the processor, which then requires from 20 to 100 µs to respond.

When the processor finally begins to execute the interrupt service routine, it must load the A-D interface with the information necessary to restart the acquisition process. Typically, this information includes the new buffer address, the number of samples to acquire, and an A-D control word. This restart process takes approximately 50 µs for an LSI-11. During both the interrupt latency period and the interface restart period, a conventional A-D cannot acquire data.

Speech is a highly skilled action and, as such, involves the simultaneous activation of many muscles.

The consequences of the A-D's not being active for a variable period of time are twofold. First, while the A-D is shut off, it cannot receive trigger pulses from the device, such as a programmable clock, which controls the sampling rate. Therefore, the minimum clock period (the intersample interval) must be larger than the maximum period during which the A-D is inactive. Otherwise, some requests for samples (clock ticks) will be ignored (thus, samples will be lost). Obviously, if no points are to be lost, the worst-case A-D restart condition must determine the maximum sampling rate. With careful design, the restart time can be held to 100 µs, so the maximum sampling rate is 10k samples/s.

Second, while the clock is inactive it cannot sense trigger pulses that may be sent to it. Thus, the clock cannot inform the software that it has missed a data point. For this reason, any attempt to drive the A-D at a speed higher than 10k samples results in the undetected loss of one or more data points. These lost data points cumulatively degrade the time-domain analog data being acquired and, in certain situations, render the data invalid.

Careful design for higher throughput

With its specialized analog I/O hardware and software and its Winchester disk optimized for data throughput, the DT4136 system provides a larger data buffer (98,048 samples) than did previously available laboratory data acquisition systems, as well as higher throughput rates to memory. But, a major breakthrough is the system level integration. With wrap-around buffer management, this allows continuous throughput to disk at 100k samples/s.

This system achieves high performance by the introduction of innovative hardware and software techniques for data acquisition interfaces. The hardware architecture, which supports 250k-sample/s throughput, multiple triggering and sampling schemes, and a RAM channel/gain list file for user programmable gain and multiplexing, is based on a threaded buffer interrupt handling system.

Such an approach allows the DMA hardware onboard the A-D interface (also the D-A interface) to chain between buffers without stopping the data acquisition process. An interrupt is generated when a buffer is nearly full, rather than when it is actually full. However, unlike conventional hardware approaches for data acquisition, the A-D interface in this system does not stop when it issues an interrupt. Instead, it continues to fill buffer A.

Meanwhile, an interrupt service routine performs the functions necessary to have the system begin filling buffer B. While buffer B is filling, the software determines how much additional data were put into buffer A, after the initial interrupt. Via bookkeeping, additional data are redirected into buffer B. In addition, while buffer B is filling, buffer A's contents are being sent to disk. When it is nearly full, buffer B will likewise generate an interrupt service request and the process will repeat. This A-B-A-B buffer scheme provides continuous, no data-gap data acquisition up to the limits of available disk storage.

To support these continuous data transfers, the software package comprises a library of routines designed to be linked to a user's FORTRAN application program under the RT-11 operating system. Combining several techniques makes continuous data acquisition possible. Drivers are system resident, that is, they are really RT-11 device handlers rather than device drivers linked to the user's application program. Hence, I/O requests can be handled as RT-11 system requests. This ensures that the drivers are resident even if a user's program fails. Although this makes the CPLIB drivers more complex to design, it provides for smaller and faster interrupt service requests.

Another unusual aspect of this software is that the drivers dequeue an I/O request as soon as the I/O starts, rather than after it ends. This approach allows the I/O drivers to prepare for the next I/O request while the first is still running. Completing all possible calculations in the initiation (startup) section of the device handler minimizes interrupt service routine execution time. Dequeuing also gives the software time to manage the threaded buffer bookkeeping tasks.
Chairmen of the boards!

The UDS shipping crew has directed a lot of boards! Modem boards for a multitude of OEM customers are on their daily agenda.

Upstream from our chairmen of the boards is a highly automated, high-volume modem manufacturing facility, and a staff of industry leaders in OEM modem design and economical board layout.

UDS modem boards are available in 103, 201, 202, 208 and 212A Bell-compatible versions, as well as a 9600 bps modem that’s operable over either dial-up or dedicated lines. All our dial-up versions are FCC certified for direct connection to the switched network.

In low-cost standard configurations or space-saving custom layouts, UDS OEM modems set the highest standards for reliability and cost effectiveness. Prove it to yourself with your next modem buy. Contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/837-8100; TWX 810-726-2100.

Universal Data Systems

DISTRICT OFFICES:
Old Bridge, NJ, 201/251-9090 • Blue Bell, PA, 215/643-2336 • Atlanta, 404/998-2715 • Chicago, 312/441-7450 • Columbus, OH, 614/895-3025 • Boston, 617/875-8868
Richardson, TX, 214/880-0002 • Englewood, CO, 303/694-6043 • Houston, 713/988-5506 • Tustin, CA 714/972-4619 • Sunnyvale, 408/738-0433

CIRCLE 72
Measuring speech mechanisms accurately

In any data acquisition situation, the appropriate sampling rate is dependent upon frequency range and desired resolution. For speech, vocal tract acoustic characteristics and the human ear’s resolving power define the frequency requirements. Speech production can be modeled as an acoustic filter transfer function for a varying-cross-sectional-area tube excited at one end by a noise source (e.g., the larynx or Adam’s apple). The excitation source is a roughly trapezoidal or triangular wave with a rich harmonic structure extending to approximately 10 kHz. Fundamental frequencies of around 100 Hz for men and 200 to 300 Hz for women and children are typical. The vocal tract above the larynx acts as a series of dynamic filters that shape the harmonics of the fundamental to yield an output signal. This signal varies in amplitude and frequency depending on changes in cavity size.

Larynx vibration is only one of the ways the vocal tract can be excited. In whispered speech, air is pushed past an open larynx, creating a broadband hiss that is then shaped by the tract. Hiss excitation can also be produced at other points along the vocal tract by constricting air flow. This occurs for sounds such as the s in see or the j in justice. Suddenly releasing air pressure to create a burst of noise, as with the k in key, is another instance of localized sound production. Hisses, constriction noises, and bursts all can have meaningful frequency components above 10 kHz.

The diversity of speech research problems and approaches requires that each laboratory develop much of its own software.

Taken together, these acoustic components of speech require a bandwidth of at least 10 kHz. Often a bandwidth as large as 15 or 20 kHz is necessary to contain speech data. Bandwidth requirements are further complicated during digital signal playback analysis. Here, signals must not only be recreated at precisely the same rates at which they were recorded, but they must be mixed accurately to create stereo reproduction. Several experimental applications require simultaneous playback of two signals—for instance, to study the effect of one sound upon the intelligibility of another. This dual channel playback not only doubles signal storage requirements but also increases the required bandwidth by 20 to 40 kHz.

Bandwidth directly determines the digitizing rate required. The widest bandwidth (BW) for a particular rate (R) is known as the Nyquist frequency and has the value \( BW = R/2 \). For example, an acoustic bandwidth of 15 kHz requires a rate of at least 30 kHz. Fortunately, the system described here provides stable external timing and maximal true rates (input and output) of up to 250 kHz. Coupled with large data storage capacity, these features allow speech signals of long duration to be recorded (or synthesized) and played back one or two at a time, with natural fidelity and accurate timing.

Although multichannel audio recording is not frequently required in speech research, multichannel recording of audio plus other analog information is commonly required. This need arises when the coordination of the vocal tract activities producing speech are examined.

Speech is a highly skilled action and, as such, involves the simultaneous activation of many muscles. Control problems are common in many speech disorders ranging from stuttering, to the overly nasal sound of deaf persons’ speech, to the complex misarticulations found with injuries to the muscle control centers in the brain. Investigating these disorders, as well as normal speech mechanics, involves the simultaneous monitoring of muscle activity, articulator movement, and acoustic output. A typical application might examine larynx activity, jaw movement, lip muscle activity, nasal air flow, and acoustic output (Fig 2). Differences in the relative timing and degree of these variables subtly distinguish the sounds of the letters m, n, b, and p. A deaf person’s speech is often characterized by abnormal nasal air flow during pronunciation of m or p. This produces what sounds like n or b. Using multichannel monitoring, the nature of the incorrect control of nasal air flow can be studied and new approaches to speech therapy suggested.

Not surprisingly, this sort of multichannel recording presents technical problems. Principal among them is the differing data rates required for each channel. The audio recording, as previously noted, can require digitization rates approaching 30 to 40 kHz. Muscle electrical activity, detected by fine wire electrodes fastened to the skin, requires data rates of only 100 Hz or so. Air flow as measured with a thermistor, larynx vibration as measured with a sensitive accelerometer, and jaw movement as measured with a strain gauge demand even lower sampling rates. Most A-D systems allow for multiplexed multichannel recording. Unfortunately, many of these systems also require that all channels be sampled at the rate of the highest data rate channel. A multichannel measurement, as shown in Fig 2, requires rates in excess of 150 kHz. With this method, nonaudio channels are grossly oversampled, and valuable data storage is squandered.

The LAB-DATAX system is designed to eliminate this problem by using random channel addressing. Here, the appropriate choice of an overall

128 COMPUTER DESIGN June 1983
the genius is in the design
the proof is in the image

THE DIFFERENCE between a conventional RGB monitor and Hitachi's monitors with Digital Dynamic Convergence™ (DDC) is the difference between a snap-shot and a professional photograph.

Proven Dependability
Most importantly, the Hitachi DDC system has proven to be a success in the field. Hitachi quality keeps them working; Hitachi innovation keeps them in demand.

<table>
<thead>
<tr>
<th>CONVERGENCE CHART</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Hitachi Monitor</strong></td>
</tr>
<tr>
<td>Quality Circle</td>
</tr>
<tr>
<td>Full Screen</td>
</tr>
</tbody>
</table>

Colors Display Monitors • Clearly the Finest

Come discover the total DDC picture at the Hitachi Trade Show Booth.

CIRCLE 73
Fig 2 Shown here is a typical multichannel data acquisition situation encountered in speech research. Data relating to muscle movements, sound production, and cavity constriction are simultaneously gathered from several channels and recorded on disk. Data can then be displayed, compared, and recombined to ascertain where speech related problems lie.

The sampling rate, in conjunction with a channel-addressing scheme, allows the audio channel to be sampled more frequently than other channels. Now, each channel can be digitized at a rate closer to optimum.

This performance is achieved by the use of a RAM channel file implemented on the A-D (and D-A) interfaces. The multiplexer channel file is an onboard 1024-byte RAM, which is divided into four 256-byte pages. The LSI-11 processor has read/write access to the RAM so that it can store (and read) the channel numbers to be input or output in any desired sampling order. Each entry in the channel list file on the A-D interface includes 6 bits for channel number information and 2 bits for gain determination. On the D-A interface, the RAM includes 6 bits for channel number and 2 bits for a deferred trigger mode.

Access to the channel list from both the processor and the A-D or D-A converters is controlled by a set of pointers that allow the user to set the board to scan, within a 256-byte page, only as much of the channel list as is required during an operation. The channel address pointer automatically increments after each conversion until it matches the final address pointer. It automatically resets to the value held in the start address pointer at this time.

RAM channel list file flexibility includes three conversion schemes, each of which can be controlled by software or external triggers. With the single-channel approach, each trigger causes one element in the channel list to be converted. With the channel-scan approach, each trigger causes the entire list from start address pointer to final address pointer to be converted. With the burst mode, each trigger causes a preset number of conversions (specified by a word count register) to be performed, regardless of how many times the channel list must be scanned. None of these conversion schemes require processor intervention and they can be performed at the full speed of the A-D or D-A interface.

Editing acquired data
Digitized speech information is rarely studied in its raw form. Analysis usually requires averaging input root mean square amplitudes or relative decibel levels. In addition, experimental interest may focus on one of two input segments. The desired segment must be extracted from its context for further examination. Although some automatic signal processing schemes have been developed for such analyses, most experimental approaches require an interactive mode in which the scientist reviews recorded data and marks events of interest. Such editing is virtually impossible in the absence of a computer-controlled signal display. Some applications use a cathode ray tube to plot stored data. Other more crude systems use a storage oscilloscope to display successive segments of data. By repeated searches of the data stream, the scientist can isolate and mark segments for analysis or excision.

LAB-DATA X offers an alternative to these options. The high speed D-A system is designed to dump digitized data in a dynamic, point-plot mode.
using a standard, X-Y display, laboratory oscilloscope. A few simple software commands scroll up to eight channels of stored data, from memory or disk, across the screen. Labeling of channels, sample number, and instantaneous amplitudes are automatically provided. The display software, directly accessible by user-written FORTRAN programs, provides listings of marked segments for further analysis. In addition to providing relatively inexpensive signal editing, the display option maximizes use of the unique signal storage and D-A conversion system modes.

The diversity of speech research problems and approaches requires that each laboratory develop much of its own software. Unfortunately, as advances in technology extend signal processing possibilities, increasing technical complexity makes programming difficult. For instance, the DEC 11/23 system provides for both virtual memory addressing beyond the 16-bit word limitation and for non-central processing unit DMA bus control. Using virtual memory greatly increases the amount of storage available, and the device-driven DMA also increases signal throughput. Use of these and other sophisticated features requires a programmer intimately familiar with both the hardware and machine language. Sadly, few laboratories can afford this kind of support personnel.

A distinct advantage of the LAB-DATAX system is its application-oriented software. All subroutines in the DTLIB and CPLIB packages are designed for easy incorporation into user-developed FORTRAN programs. Since the packages are authored by software professionals familiar with the demands of speech data acquisition, subroutines fully exploit the advanced technical features of both the DEC 11/23 and the data acquisition hardware.

Joining powerful computing and data acquisition hardware with accessible, yet effective software helps to meet the rigorous demands of speech related data acquisition. The result of this technical commingling is most gratifying. When technology serves humanity in such profound and therapeutic ways, it is at its most noble.

Acknowledgments
The authors would like to thank Robert J. Porter, Jr, PhD, professor of psychology, University of New Orleans, and clinical professor of otorhinolaryngology and biocommunications, Louisiana State University Medical School, for his help in preparing this article.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 707  Average 708  Low 709
Operating a manual control with a finger seems simple enough. But the process of designing the interface between people and machines can be complicated. To communicate effectively, the operator needs to understand and react to the appearance, sound and feel of the machine's controls. In addition to these human factors, there are other considerations like aesthetics, reliability and the availability of components.

Ultimately, to choose the best manual controls for your interface, you'll need a wide selection of products to choose from. And probably some help making the choice. Only one company meets all these needs. MICRO SWITCH.

With MICRO SWITCH you'll get design flexibility from the broadest selection of manual switches available from a single source anywhere in the world. You get more options on both sides of the panel, so you have more freedom to design your product the way you want it.

Up front, your functional choices include discrete manuals such as pushbutton, toggle, paddle, and rocker switches, as well as keyboards and touch panels. Most discrete manuals are in stock, or can be assembled on a modular basis to fit your exact needs. Keyboards and touch panels are easily custom-designed to meet your special requirements. All together, there's a virtually limitless combination of colors, legends and types of illumination possible.

Behind the panel, your choices continue with a variety of military qualifications and worldwide agency approvals. Electrical ratings range from just a few milliamps to twenty-five amps, in contact or solid state varieties. You can also choose oiltight sealing and other...
This so many ways of a finger.

protection for severe environments, as well as a wide variety of package sizes, including a new miniature line.

Having this wide selection means you can specify the best combinations of performance and price for a variety of needs, while enjoying the economy of working with just one company.

Manual controls are the critical point of communication between your product and its operator. Based on our human factors experience, we can help you design for the human half of this interface. Your options include visual, audible and tactile feedback, plus a variety of sizes, shapes and colors.

In addition to our other advantages, you get the kind of quality that makes your product better, too. Because our manual switches are built to do what we say they will, as long as they're meant to. And they share a distinctive, high-quality look. Giving your product a consistent, aesthetically pleasing appearance.

Whatever your man-machine interface needs, give MICRO SWITCH a chance to help. Our experienced field sales and application engineers are eager to get involved early in your design process, to counsel you on the selection of manual controls for your application. And no matter where you do business, MICRO SWITCH is nearby with manufacturing, sales, and service locations worldwide—including our network of distributors for local service and availability.

For the location of a sales office or authorized distributor near you, call 815-235-6600. Or write to MICRO SWITCH, Freeport, IL 61032. With our help, you’ll find the manual controls that work best. For fingers. And for you.

Together, we can find the answers.

MICRO SWITCH
a Honeywell Division
On the line or in the field...

Slash digital test and repair from HP.

Products are getting smarter. Microprocessors are appearing in everything from test equipment, to point-of-sale terminals, to self-service gas pumps. But with increased functionality often come increased headaches. Especially when production test, field service or in-house repair personnel must try to diagnose and correct difficult logic faults deep within a 100-IC board.

Testing Smarter.
Realizing this trend, smart design engineers have, for over five years now, been helping their companies achieve significant savings in product test and rework by including signature analysis in their design strategy.

"No-Trouble" Troubleshooting
The results can be dramatic. By incorporating signature data into schematics and fault trees, the time it takes to locate and repair a component malfunction can be reduced by up to 80%. Troubleshooting of complex digital systems now becomes as reliable and easy to follow as traditional analog troubleshooting. Test a circuit node and compare its signature to the known correct signature for that node. If the signatures don't match, backtrace until they do. You've found the faulty node.

Investing in Productivity
Perhaps you've thought about the time saving and cost saving benefits of signature analysis, but were put off by the design investment. Consider this: Up-front engineering time required to incorporate signature analysis rarely represents more than a 1% increase in total design time. In fact, typical results have indicated no more than a 1 to 4 man-week increase out of a total 180 man-month design project.

Also, sophisticated tools such as the new HP 5500S Logic Troubleshooting System make the process of producing signature analysis test and service documentation essentially automatic.

Minimal Design Overhead
To use signature analysis, each circuit node must be exercised with an arbitrary, but repeatable, bit pattern. Often, this is just an adjunct to existing self-test code. In most cases, an additional 5% of ROM space will handle it. And it's usually as simple as supplying a routine to cycle through address locations.

In hardware, you simply watch for the possibility of feedback paths influencing signature detection. The solution is often as simple as installing jumpers to break paths, or a few switches and pull-up resistors to guarantee the status of particular signal lines.

Error Detection Accuracy to 99.998%
Using an HP-developed technique for data compression, our family of signature analysis products can detect errors in arbitrarily long bit patterns to an accuracy of 99.998%. Single bit errors are detected with 100% accuracy. This far surpasses the performance of most other fault-location techniques, and brings effective component-level diagnostic capabilities within the reach of most production departments and field service organizations.
Good News At The Bottom Line
In terms of dollars saved, signature analysis can help you realize significant benefits. Increased troubleshooting power can help you reduce production test and repair time, reduce service costs, and possibly cut in-the-field subassembly replacement stock. Conservative calculations for a typical product design effort incorporating signature analysis show an Internal Rate of Return (IRR) of over 100%.

The HP Family of Signature Analysis Tools
Now that you know the benefits of HP signature analysis, you should also know that we have a full line of cost-saving tools to get you going.

For the optimum in automation, versatility, and power, look to the HP 55005S Logic Troubleshooting System, priced at $9675*. This system condenses your product operation knowledge and diagnostic procedures into a computer-assisted troubleshooting database. It automatically generates annotated signature lists for test documentation, and leads test personnel through guided backtrace troubleshooting for fast fault isolation.

If you already have an HP desktop computer, or want similar versatility at lower cost, the logical choice is the HP 5005B Signature Multimeter ($3825*). Interfacing via the HP-IB, or controlled manually, it can measure frequencies, time intervals, voltages, and resistance values, in addition to full-function signature analysis.

For the same measurement features in a standalone package, or for field test applications where low cost is important and HP-IB compatibility is not, specify the HP 5005A ($2815*).

Tops in value is the new HP 5006A Signature Analyzer. At just $995*, this dedicated signature analyzer is your lowest-cost entry into automated signature analysis. In the systems test environment, it can be controlled by a desktop computer via the HP-IB. And for the ultimate in portable computer-aided troubleshooting in the field, just combine the HP 5006A with an HP handheld computer via the built-in HP-IL interface. For fast manual testing, a composite mode lets you probe multiple nodes without comparing each signature. Simply compare the composite signature with the expected result. If they match, all is well. If not, just recall individual signatures from memory until the faulty node is found. It's just another HP signature analysis technique that delivers faster testing and fault isolation.

Save on Existing Designs Too
If you already have a product in the field, you can still take advantage of HP signature analysis without costly redesign. The HP 5001 family of Microprocessor Exercisers are preprogrammed testers specifically configured for particular microprocessor chips. Each exerciser provides reliable testing of the target chip, system RAM, ROM, I/O ports, address and data busses, and more. There's even a socket to plug in a customized PROM for unique tests not covered by the 5001 standard array.

For More Information...
Give us a call. We'll be glad to send you a complete information package on HP signature analysis: products, techniques, and applications. Contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

* U.S.A. list prices only.

CIRCLE 76
This New Fiber Optic Modem will Extend a DCE Interface to Any Point in Your Local Area Network.

Plus a whole lot more.

- Can also be used for standard modem applications
- Automatically accepts or supplies DCE/DTE clocks
- Fully supports all EIA handshaking signals
- Provides secondary data channel

In short, you can use our new fiber optic modem between any two plug compatible units in your local area network. And it won’t require any jury-rigging or looping clock and interface signals. That’s because, from an operating standpoint, our fiber optic modem looks just like an EIA cable; whether you’re going from a long-haul modem to a remote terminal or from a CPU port to a printer. And it’s just about as easy to install as a cable — we even provide two separate connectors (DTE and DCE) on each modem. YOU determine how our modem will function simply by selecting which connector you use!

from the advantages inherent with fiber optics (traffic security plus noise immunity) but also from the exceptional operating performance. Our very low error rate and continual signal quality monitoring means that you’ll operate with a higher throughput and less downtime than ever before.

Versitron manufactures a complete line of fiber optic products for Local Area Networks. Our 20 years’ experience in fiber optic is reflected in the performance capabilities of our products.

For the full story on how our complete line of fiber optic products will solve your Local Area Network problems, give us a call at (202) 882-8464. Or write:
GENERATING HUFFMAN CODES

Time and space are saved when alphanumeric data are compressed and represented by these efficient encoding schemes.

by George Grosskopf, Jr

Modern computers store and transmit vast amounts of data. As the requirements for storage and transmission increase, the physical limitations of the computer system become evident. One way to partially overcome these limitations is by using Huffman encoding techniques to compress data. Huffman encoding produces optimum, variable length codes that represent a finite number of characters. These characters can be alphabetic, numeric, or alphanumeric. In fact, Huffman encoding methods can be used with ASCII characters. Here, the ASCII 7-bit word used to represent up to 128 alphanumeric characters can be compressed to allow additional data to be stored or to reduce the time required to transmit the data.

When using Huffman encoding with ASCII characters, shorter Huffman codes are assigned to characters that frequently occur. Longer codes are assigned to characters that are less frequent. This assignment can be depicted as

\[ P(1) \geq P(2) \geq P(3) \geq \ldots P(N-1) \geq P(N) \]

where \( P(1) \) is the probability of character 1, \( P(2) \) is the probability of character 2, and so on. \( N \) is equal to the number of characters to be coded. The assignments for the length of the codes must be

\[ L(1) \leq L(2) \leq L(3) \leq \ldots L(N-1) = L(N) \]

where \( L(1) \) is the length of the most probable code, \( P(1) \); and \( L(2) \) is the length of the next most probable code, \( P(2) \), etc. Though it is possible that codes for characters with the same probability of occurrence can differ in length, interchanging these codes will not affect the total number of bits required to store or transmit a message.

Some restrictions on the Huffman code of characters do exist. For instance, no two coded characters can be represented by identical code words. Also, codes are constructed in such a way that shorter codes will not appear, bit by bit, as the first part of a longer code. Two coded characters, with a code length of \( L(N) \), have codes that are the same except for the last bit in the codes. Finally, each possible sequence of \( L(N) - 1 \) bits must be used either as a code or one of its prefixes must be used as a code.

Generating Huffman code

Huffman codes are generated from tables. Table 1, a Huffman code reduction table, illustrates the steps required to generate typical Huffman codes. The first step required in generating Huffman codes is to list probability values, or reduction
TABLE 1

Huffman Code Reductions

<table>
<thead>
<tr>
<th>Char</th>
<th>Col 1</th>
<th>Col 2</th>
<th>Col 3</th>
<th>Col 4</th>
<th>Col 5</th>
<th>Col 6</th>
<th>Col 7</th>
<th>Col 8</th>
<th>Col 9</th>
<th>Col 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.27</td>
<td>0.27</td>
<td>0.27</td>
<td>0.27</td>
<td>0.27</td>
<td>0.27</td>
<td>0.27</td>
<td>0.27</td>
<td>0.28</td>
<td>0.44</td>
</tr>
<tr>
<td>4</td>
<td>0.16</td>
<td>0.16</td>
<td>0.16</td>
<td>0.16</td>
<td>0.16</td>
<td>0.20</td>
<td>0.20</td>
<td>0.20</td>
<td>0.24</td>
<td>0.44</td>
</tr>
<tr>
<td>3</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td>0.06</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td>0.04</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td>0.02</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Huffman Code</td>
</tr>
</tbody>
</table>

1 1 6 0 0 1 0 0 0

codes, of the set of characters to be compressed. These values were calculated from the list of phone numbers in Table 2. The list of probability values appears in column 1 of Table 1. The column is organized with the most probable character at the top, and the least probable character at the bottom.

It is mandatory that the two least probable characters have codes of equal length, and that two coded characters, with a code length of L(N), have codes that are alike except for the last bit. To allow for these restrictions, the bottom two reduction codes must be combined. This combination is referred to as an auxiliary character.

To accommodate the final restriction on codes, that each possible sequence of L(N) – 1 bits must be used either as a code or one of its prefixes must be used as a code, a new column must be created (column 2). This column contains all the reduction codes that were not previously combined, plus the new auxiliary character. In creating this column, the auxiliary character will be handled and referred

TABLE 2

Encoded Bit Requirements

<table>
<thead>
<tr>
<th>Phone Number</th>
<th>Number of Bits for ASCII Codes</th>
<th>Number of Bits for Huffman Codes</th>
<th>Number of Bits for Binary Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>423-2000</td>
<td>49</td>
<td>18</td>
<td>28</td>
</tr>
<tr>
<td>699-1054</td>
<td>49</td>
<td>23</td>
<td>28</td>
</tr>
<tr>
<td>853-9494</td>
<td>49</td>
<td>24</td>
<td>28</td>
</tr>
<tr>
<td>486-0100</td>
<td>49</td>
<td>22</td>
<td>28</td>
</tr>
<tr>
<td>233-6530</td>
<td>49</td>
<td>23</td>
<td>28</td>
</tr>
<tr>
<td>792-4400</td>
<td>49</td>
<td>21</td>
<td>28</td>
</tr>
<tr>
<td>243-1000</td>
<td>49</td>
<td>19</td>
<td>28</td>
</tr>
<tr>
<td>TOTAL</td>
<td>343</td>
<td>150</td>
<td>196</td>
</tr>
</tbody>
</table>

138  COMPUTER DESIGN June 1983
Never before was PROM programming so totally versatile. But never before did Kontron offer its new EPP Engineering Programmer.

The EPP can handle whatever your programming needs are — MOS, CMOS, bipolar, *E²PROM, PAL*, FPLAs. And Kontron’s EPP will be able to handle the 128K and 256K devices when they’re available.

The Kontron EPP offers 64K RAM standard and multiple I/O formats to help you communicate with all popular development systems. And only Kontron can offer you a TRANSKON communication format for transferring data over long distance lines with full error recovery and delay compensation.

Total flexibility RAM data set, insert, delete and block move are standard. Memory search mode, logic mode for making changes in RAM data. A standard built-in UV eraser is keyboard programmable up to 99 minutes with time displayed. RS232 serial interface is standard, with optional serial, Centronics-parallel, or IEEE-488 available.

All that, plus the new Kontron MOS Development Module that programs more than 25 MOS, CMOS, *E²PROMs and single-chip processors*. The MDM operates with both the EPP Programmer and the MPP Programmer, and features access time check with selectable voltage levels for engineering or QC critical part checking. For use with dumb terminals, a built-in cursor control editor is available.

For gang programming all popular MOS EPROMs (up to eight at a time), check out Kontron’s Universal Gang Module. It’s compatible with the EPP and MPP programmers.

All together it spells total flexibility — and *only* from Kontron.

*PAL is a registered trademark of Monolithic Memories, Inc.
to as another reduction code. The column must be rearranged by order of probability and will also contain one less reduction code.

Once again, the bottom two reduction codes are combined to form a new auxiliary code. A third column is now formed using all the reduction codes that were not combined in column 2 and the new auxiliary code. This procedure is repeated until a column with only one reduction code results. (See column 10 of Table 1.)

Now, Huffman codes can be generated from the reduction table. A bit is defined in a Huffman code if the reduction code or the auxiliary character of the character to be coded is contained within a bracket. If the reduction code or the auxiliary character is located in the upper portion of the bracket, then a bit in the Huffman code is defined to be 0. This bit is defined to be a 1 if the reduction code or the auxiliary character is located in the lower portion of the bracket.

For example, the shaded area of Table 1 highlights the generation of the Huffman code for the character 7. Column 1 shows the reduction code for the character 7 contained within the lower portion of the bracket; therefore, a bit in the Huffman code is defined to be 0. This bit is defined to be a 1 if the reduction code or the auxiliary character is located in the lower portion of the bracket.

Columns 3 and 4 do not contain combinations of the auxiliary characters for the character 7; therefore, these two columns do not define a bit in the Huffman code for the character 7. (Note that columns 3 and 4 do contain combinations of the auxiliary characters for the characters 1, 5 and 9, 2, respectively.) Another auxiliary character for the character 7 is contained within the upper portion of the bracket in column 5; thus, the next bit in the Huffman code is defined to be a 0. This procedure is continued until all auxiliary characters contained within brackets are employed to define the Huffman code for the character being coded.

Table 3 illustrates the Huffman codes generated with the aid of the Huffman code reduction table.

The right column is a tabulation of the Huffman bit patterns used to represent the characters in the left column. Using ASCII codes to represent the phone numbers of Table 2, the number of bits required by a computer to store or transmit this information is 343. Applying the Huffman codes of Table 3 to the problem, the total number of bits required to represent the same information is reduced to a mere 150. This represents a savings of approximately 50% in the number of bits required to store or transmit this data. More importantly, the same computer system can double the amount of phone numbers it stores, or halve the time required to transmit them.

Obviously, ASCII codes are not the optimum set of codes employed to represent the phone numbers used in Table 2. If 4-bit binary codes are employed to represent these phone numbers, the number of bits required to store or transmit them would only be 196. Employing Huffman codes instead of the binary codes to represent the phone numbers means a savings of approximately 30% in the number of bits required to represent them.

**Wide-ranging Huffman code application**

Huffman encoding can be employed in facsimile equipment, digital television, and word processors. In word processors, Huffman encoding can increase storage capacity at no extra cost.

Huffman encoding need not be limited to just characters either. It can also be used to generate codes for common combinations of characters, known as digraphs, as well as commonly used words such as and, is, the, or the mnemonics in an assembler. Although these combinations might not be the most probable, they could offer additional compression. Computers and dedicated word processors also store additional control characters to control printer and disk formats. These control characters can be encoded, removing the conflict between these special control characters and the variable-length codes generated by Huffman encoding. In short, Huffman encoding techniques can provide many advantages to systems where storage is at a premium or data transmission rates must be maintained on existing hardware.

**Bibliography**

WE JUST CAN'T LEAVE A GOOD THING ALONE.
How could we leave it alone?
When you've introduced the highest performing 16-bit CPU on the market, you've just got to make it immediately available at the board level.

Look at the stand alone specs of the 286. It offers three times the performance of any other microprocessor. It's got memory management and protection, on chip. It has 16 Mb of physical memory. It's compatible with Intel's new 80287 Math Coprocessor. And it's more than a match for today's powerful 16-bit operating systems.

Now, imagine all that raw power in the company of an Intel board.
Powerful, yes. But we couldn't leave the 286/10 alone.
So we designed it as part of a family. Joining five other new high performance MULTIBUS® boards and a real-time operating system: Intel's new iRMX™ 286R. Fully compatible with our industry standard iRMX™ 86 Operating System and its languages.

But we still couldn't leave the 286/10 family alone.
So we designed it to be totally compatible with every one of our iSBC 86, 88 families. A MULTIBUS board for every price and performance level. Complete with software.
But then, we couldn't even leave all our boards alone.
Not with board extensions available. Like our new iLBX™ Intel's Local Bus Extension. It offers arbitration-free, direct access to high performance memory. With three times the performance of any other bus system.
All this togetherness comes down to Intel's concept of "Open Systems." Giving designers and management complete flexibility, through our entire product line. Rapid, easy access to VLSI, via industry standards.

And naturally, when you go with Intel, you'll never be alone. We'll be there, with hardware and software support. Training, consulting and servicing. Helping you to reduce your risk, by minimizing your initial investment and maximizing your design's total potential.
Call us, toll-free. (800) 538-1876. In California, (800) 672-1833. In Europe and Japan, contact your local Intel Sales Office. We'll send you information on our new high performance products and a board development kit. A kit that'll get you started for less than $10K.
And, if you don't mind us saying so, that alone should be enough to make you want to call.

3065 Bowers Avenue, Santa Clara, CA 95051
Ding, dong, the "Which" is dead. Our newest low price Winchester disk controller lowers the boom.

If, by any chance, you've been uncertain which company has the lowest price, highest value Winchester disk controllers, our new WDI000-05 will lay that "which" to rest.

Simply put, the WDI000-05 is the new price leader in hard disk controllers. How much a price leader? Our one-piece price, if you care to order an evaluation unit, is just $150. Can you imagine what we must be selling these for in OEM quantities!

The WDI000-05 is designed for those systems builders who a) want to offer a hard-disk based system to stay competitive and, b) who recognize our pre-announced progression of controller boards puts you on the path to higher performance and lower cost.

Our new WDI000-05 is no stripped-down model, either. It includes our remarkable VLSI WDI010 Winchester Disk Controller, and WDI100-II Support Device. There is on-board sector buffering, data separation, write precompensation and error-checking, too. All on one board, designed to mount atop a 5½" drive.

Call our Controller Hotline, 714/966-7827, for up-to-date details. Or send us your company PO or check for $150 and we'll send you an WDI000-05 board for evaluation. It's our way of keeping you on top of things.

Components Group. 2445 McCabe Way, Irvine, CA 92714. (714) 557-3550

WESTERN DIGITAL CORPORATION
Introducing the Munchkin, the lower cost solution to 5½” floppy disk control.

Looking for a lower cost solution to interfacing 5½” floppy disk drives to your system? Let our new WD1770 show you the way. We call it the Munchkin. You'll call it the economical solution you need in today's price sensitive systems market.

The WD1770 is a diminutive one-chip controller/formatter that masters both single and double density 5½” floppies. It gives you all the features of our FD1793. Plus Digital Data Separation and Write Precompensation. On one chip. With just 28 pins. Component count is reduced, too. Which saves beaucoup board space. And on-chip digital data separation eliminates the manufacturing cost of tweaking PLL data separation.

A single read line is the only input required to recover serial FM or MFM data from the disk. Data rates are selectable. So are sector lengths. And a new programmable Motor On feature pre-enables the spindle motor. Stepping rates are compatible with the FD1793. Or, for rates of 2, 3, 5 or 6 msec. specify the WD1772 version.

Why wait? Call our Controller Hotline at 714/966-7827 for immediate information. Or write Kathy Braun on your letterhead for a free sample. Then find out for yourself why we say the Munchkin is such a big deal.

*Munchkin is a trademark of Western Digital Corporation
Timely Processor Support

Ever have to settle for a second-choice microprocessor because language and emulation support wasn’t available for your first choice? Put HP’s 64000 Logic Development System in your lab and that frustration is gone.

That’s because HP’s microprocessor support strategy results in assemblers and emulators for virtually any 8- and 16-bit microprocessor...well ahead of the support available from manufacturers.

How is that possible? With the 64000 system, you can select the tools to build your own assembler and emulator. For assembler support all you need are the instruction set of your processor and HP’s user definable assembler. Easy-to-follow instructions will have you assembling code in a matter of hours.

As for emulation, once you have the chip, our Universal Emulator lets you get to work in an execute-only environment in just a few days. And full emulation capability is typically just a matter of weeks. Because we supply hardware and software that’s about 80 to 90 percent complete. You do some interface design and complete the software package. Everything you need is supplied, including step-by-step instructions and a design example using a popular microprocessor. Compare this approach to the year or two you’d wait for normal support...if you get it at all. HP also provides full support for a host of 8-and 16-bit processors, with more on the way. So don’t let lack of support slow you down or compromise your designs.

Marginal Signal Conditions

No need to let marginal signal conditions and other timing related gremlins hold you up either. Because the 64000’s timing analysis subsystem combines sophisticated triggering, high speed, 8k memory depth, and postprocessing for measurement capability not available in timing analyzers until now.

For example, our dual-threshold mode identifies noise problems and marginal signal levels. And helps you solve bus loading and bus conflict problems.

In the fast mode, 400 MHz speed yields the resolution necessary to resolve critical timing margin problems. New statistical analysis capabilities increase resolution and give useful data for system characterization. And the ability to trigger on transitions, pattern durations and post-processed data conditions give you valuable capabilities in studying control-signal timing relationships such as handshake related problems.

The 64000 Timing Analyzer sets new ease of use standards too. Directed-syntax softkeys simplify measurements. And label assignment lets you analyze results in terms of your system’s nomenclature.

With this analyzer, you get to the root of timing problems fast.

Hardware/Software Fingerprinting

Whose fault? Software or hardware? The 64000, with both timing and state subsystems, and even emulation, can resolve that quarrel in short order. That’s because one subsystem can arm or trigger another for real-time interactive measurements.

For example, you can set the timing analyzer to trigger on a middle threshold that lasts too long. Then view state flow to see the affect. Or, you can trigger on state and view timing, which is useful for debugging I/O port malfunctions.

In analysis/emulation interaction, you might monitor software activity with the analyzer, then send a signal to the emulator to halt operation if a specific trace specification occurs. Now, you can study the analyzer trace listing around the suspected problem area. Or, use the emulator to examine register contents and control further operation.

Take this logical path in settling fingerprinting debates and you’ll push those designs closer to production.
Software Bottlenecks

The 64000, with software performance measurement capability, quickly eliminates these nightmares. Symbolic tracing makes measurements a programmer's dream. And histogram displays give you a graphic picture of bottlenecks and software inefficiencies. This new tool shows system activity as a function of software modules so you can see where the concentrated action is. You can determine how long it takes to execute a given module of code as you vary input parameters. See software traffic patterns. And compare software modules in terms of the percentage of time and occurrence they require in your programs.

These measurements are real-time, not post-processed trace data, which means you can interact with trace displays as well as perform overview measurements on single-shot events.

Software in the Weeds

That's where new software often ends up. But the 64000, with the state analysis subsystem, gets you back on track quickly. First, because this analyzer speaks a programmer's language. Symbolic tracing lets you define parameters in familiar source-code symbols and labels. For example, you can instruct the analyzer to find sequences and trigger points by module names and labels. And with HP's directed-syntax softkeys, defining a measurement is usually just a matter of a few keystrokes.

Inverse assembly means this analyzer speaks your microprocessor's language, too. That makes it easy for you to interpret displayed information, because now you don't have to convert analyzer displays to microprocessor mnemonics and symbols. All this in a real-time analyzer, not a simulator or intrusive run-until-search type of analyzer.

But it's also important to be able to position the measurement window with precision. We do that too.

Extended trace specification features let you navigate through complex code to the portion you want...and display only pertinent information. That's because you can combine trigger, store and count functions in any combination, to a total of eight terms, each as wide as the number of channels installed (to 120). Add to that the ability to define up to 15 sequence terms, or a combination of sequence terms and enable/disabled windows, and there aren't many nooks or crannies where software bugs can hide. That means you'll debug software pronto.

One System for Standardization

From start to finish of the development cycle, HP's 64000 Logic Development System can help you speed your designs along. It covers software development, downloading, emulation, hardware and software analysis, and system performance measurements. All with a single keyboard and display that speeds setups and simplifies measurements.

You can choose from two system stations, too. One benchtop station, with 10 card slots, gives you the most expansion capability. The transportable station, with 5 card slots, is a popular development unit for individual bench and field use.

Whichever station you choose, you can configure for dedicated function or combination measurements. You can use each in a standalone situation or as part of a multiuser, distributed processing network. It's a development system that makes sense for labs both large and small.

For details on the 64000 Logic Development System and available subsystems, call your local HP sales office listed in the telephone directory white pages. Ask for your HP field engineer in the Electronic Instruments Department.
DISK EMULATION
THE COMPLETE SOLUTION
FROM AMPLEX

For Faster Throughput and Maximum Uptime

Now Ampex provides the complete solution to peripheral memory problems with a choice of Megastore® memories — either nonvolatile memory with up to 8 MB capacity or volatile memory with 64K DRAMs and up to 32 MB capacity. Both are nonrotating, have no latency, and offer access times in microseconds. They eliminate head crashing, have no moving parts and are insensitive to temperature, dust, shock and vibration. Popular emulations include DEC, DATA GENERAL and HONEYWELL.

All Your Memory Needs

Ampex has answers to all your memory needs. To find out how our broad engineering experience and extensive production capability can help you, call Ampex now. Call toll-free 800-421-6863. In California call 213-416-1412. Ampex Corporation, Memory Products Division, 200 North Nash Street, El Segundo, California 90245.

AMPEX
Ampex Corporation • One of The Signal Companies®

CIRCLE 81
SPECIAL REPORT ON
SEMICONDUCTOR MEMORIES

Although the price per cubic foot of computer memory has not changed drastically in the last 30 years, the number of bits in that cubic foot has skyrocketed, and the memory itself is a lot smarter. System sizes are shrinking, address spaces are expanding, speeds are increasing, prices are falling, and chip makers are producing large numbers of innovative memory devices along with the chips to control them.

More functions are being squeezed into smaller boxes. Microcomputers now have additional memory, faster response, and a much better human interface than the computers of 10 years ago. Putting those functions into a typewriter-sized package has required the development of entirely new memory technologies. Nonvolatile memories—various kinds of PROMs, bubbles, CMOS with battery backup, and others—have appeared since that time, and other varieties are constantly coming to market.

The new 16- and 32-bit CPU chips are putting sophisticated operating systems and large number-crunching programs on microcomputers. Despite the spectacular rise in RAM capacity (and drop in price), continuously keeping all this software in memory is impractical and undesirable. The rise of multi-user systems makes memory space increasingly valuable. Virtual memory management has been available in mainframe software for years and is now migrating to microcomputers—in silicon. A number of manufacturers are producing memory management units to go with their powerful CPUs.

Parkinson's Law states that a work load increases to fill its time and space allocations. Computer applications are no exception, but for one difference—if they work too fast, the peripherals they control cannot keep up. Using memory to put a buffer between a fast processor and a more leisurely peripheral is nothing new, but more capable devices like FIFO buffers are taking over the job from RAM and leaving the CPU free for computing.

Keeping data accessible when the power is off once involved many trade-offs. While tapes and disks are cheap and spacious, they are also slow. Batteries and uninterruptible power supplies are expensive and not always reliable, and ultraviolet erasable PROMs are slow to program and erase. With the advent of electrically erasable PROMs (EEPROMs) in the last three years, however, there is an alternative. With prices that are following the traditional semiconductor learning curve, these EEPROMs will be much more common in the years to come.

Sam Bassett
Field Editor
What's unique about the GE 3000 printer family is its commonality.

“They’re all the same only different.” That’s the simple advantage of General Electric’s new GE 3000 series of printers...single design simplicity without the application limitations of a single model product line.

Our basic concept is application driven price/performance matching. Choose speeds from 40 to over 400 cps. Single or dual mode printing. Type quality from EDP to NLQ. Multi-color printing. Graphics. 80 and 136 column models. Selectable type fonts. Accessible, easily programmable set-up by either the operator or the system. Multi-model flexibility...all with high parts commonality.

Now, you can stock just one line of printers, yet meet a diversity of needs. Enjoy every advantage of single source supply. With each printer backed by General Electric’s worldwide service.

Take a close look at any of the GE 3000 printers. You’ll find they’re easy to use, lightweight, functionally styled, reliable tabletop matrix printers. And when you take the entire GE 3000 series altogether, they stack up beautifully compared to everything else on the market today.

General Electric. We introduced the first fully electronic printer with LSI circuitry in 1969. And our complete line today makes us the industry leader you should look to first.

First In Electronic Printing.
For the solution to your printing needs, call
TOLL FREE 1-800-GE PRINT


GENERAL ELECTRIC
Special report on semiconductor memories

153 Nonvolatile chip menu grows to suit various applications
*by Rob Mortonson and Sam Bassett*—Matching devices and applications is not as simple as it used to be. New technologies and increased capacity in nonvolatile memories give designers wide freedom of choice.

169 Virtual memory management expands microprocessors
*by Gary Martin*—A memory management unit combines demand page swapping with onchip cache for a 124-bit virtual address space.

181 FIFO—the glue holding systems together
*by Ching-Lin Jiang and Michael Bolan*—Dual-port, high density FIFOs are playing a greater role in interconnection. The latest generation offers HCMOS compatibility as well as onboard SRAM and independent access.

191 No waiting—EEPROM at work
*by Kendall W. Pope*—In addition to allowing TTL level *in situ* programming, today’s EEPROMS write and erase without delaying their host microprocessor.
INTRODUCING THE WORLD'S FASTEST ECL RAMs.

And the next fastest.
And the next to the next fastest.

Address access times of 7nsec. Maximum. And block access times of 4nsec. Maximum!

These specs belong to the world's fastest ECL RAMs. Fujitsu's new MBM10422A-7 and MBM100422A-7. Both are results of our patented DOPOS (Doped Polysilicon) and IOP-II (Isolation by Oxide and Polysilicon) manufacturing processes. Both give you low power dissipation (0.7mW/bit) and 256 x 4 organization. And both are fully compatible with their respective industry standard 10K and 100K families. Plus, our 100K series gives you on-chip voltage compensation for improved noise margin.

When higher density is a must, but speed records aren't, look into our fully decoded 1K x 4 MBM10474 and MBM100474. Ideal for high speed scratch pad, control and buffer storage tasks, they deliver access times of 15nsec and low 0.7mW/bit power dissipation.

For main memory, control and buffer storage applications, our MBM10480 and MBM100480 give you the highest densities available anywhere. They're 16K x 1 products of an entirely new cell technology using the active pull-up (PNP) technique. They give you access times under 25nsec, extremely low power dissipation (0.04mW/bit) and very small cell and chip sizes.

Each of our ECL RAMs is fully compatible with industry standard 10K or 100K families. And if you're thinking about switching to an MOS part, you'll be happy to know these second-generation ECL RAMs deliver far lower cost per bit than the ECL products you've probably been dealing with.

For literature, call 800-556-1234 (ext. 82). In California, call 800-441-2345 (ext. 82). For samples, contact your nearest Fujitsu sales office. We'll set speed records to deliver the ECL RAMs you want.

FUJITSU MICROELECTRONICS
Technology that works.

FMI, 3320 Scott Boulevard, Santa Clara, CA 95051. 408/727-1700.

FMI Sales Offices
- Boston 617/969-7920 · Chicago 312/934-6600
- Dallas 214/669-1616 · Minneapolis 612/454-0323
- New York 212/273-6660 · Northern California 408/866-5600
- Southern California 714/547-9925.

CIRCLE 83
NONVOLATILE CHIP MENU GROWS TO SUIT VARIOUS APPLICATIONS

Matching devices and applications is not as simple as it used to be. New technologies and increased capacity in nonvolatile memories give designers wide freedom of choice.

by Rob Mortonson, Contributing Editor, and Sam Bassett, Field Editor

Designers trying to match their application requirements to available solid state, nonvolatile memories will find a greater choice of varieties and vendors. From read only and programmable read only memories to the frequent read/write NOVRAM, manufacturers are offering devices to meet the present needs of an array of applications.

Inevitably, there is some overlapping of functions between devices as well as occasional jousting for sockets. Nevertheless, each nonvolatile device type has an application area all its own. What have been changing are the characteristics of those exclusive areas. For example, the minimum volumes for read only memories (ROMs) and maximum volumes for erasable programmable ROMs (EPROMs) are continuing to rise.

Simple economics has kept electrically erasable PROMs (EEPROMs) from breathing too heavily down the neck of EPROMs. There appears to be a 2 to 2.5 premium factor in their relative price per bit which, of course, favors EPROMs. Nevertheless, where in-system reprogramming is critical to an application, EEPROM has either carved out a unique socket opportunity or eliminated EPROM from consideration.

The very high price per bit premium for nonvolatile random access memories, or NOVRAMS, keeps them from threatening volatile RAM devices supported by battery backup. This application, however, appears to be the primary one for these components. So far, the use of these components has been confined to applications where battery backup is unacceptable or where the amount of storage is critical yet small.

Although not a semiconductor technology, bubble memories are solid state and packaged in a way that makes them alternatives to other nonvolatile chips for certain applications. After a clamorous beginning with many vendors announcing impending design efforts, the bubble went through a rather severe shakeout during which such notables as Texas Instruments (Dallas, Tex), National Semiconductor Corp (Santa Clara, Calif), and Rockwell International (Newport Beach, Calif) virtually abandoned the technology. Intel (Sunnyvale, Calif), who entered the fray somewhat late, had captured an early market share by leaping in with a 1M-bit part.

Today, the domestic bubble market is served by Intel and Motorola (Austin, Tex). A recent agreement between the two giants has Motorola in lockstep with Intel on technology and packaging. Fujitsu Microelectronics, Inc (Santa Clara, Calif) and Hitachi America, Ltd (San Jose, Calif) are also mounting a bubble effort. Unlike Intel and Motorola, who appear to be playing a component-level strategy, the two Japanese manufacturers have concentrated so far on bubble boards and cassettes.

Originally, bubbles were used for mass storage-like functions in harsh environments. Their inherent
With the peripheral control circuitry implemented in CMOS, Signetics' 64K EPROMs are both fast and economical on power. These products are the first fruits of Signetics' highly automated Albuquerque fabrication plant.

immunity to shock, heat, and contaminants made them the only alternative in areas that would have proven catastrophic for rotating mass storage systems. However, a new niche has appeared for these high density memories. More computer manufacturers are putting them in portable computers as a form of working storage—that is, a selective group of records and files gleaned from a master storage system and carried along with the portable computer. Systems from Grid Systems Corp (Mountain View, Calif) and Teleram Communications Corp (White Plains, NY) have already proven the efficacy of this procedure. Fujitsu has recently announced a personal computer—the BC—that uses bubble cassettes for the same purpose.

In each of these six nonvolatile product areas—ROMs, PROMs, EPROMs, EEPROMs, NOVRAMS, and bubbles—manufacturers have announced new products. Some products feature higher capacity, faster speeds, or more flexibility through onchip functions. Some are the result of technological innovations. Others are combinations of several of these
characteristics. The trends in these six areas are important to consider because they will affect design decisions and selection criteria of devices in future products.

**ROMs: bigger, cheaper, faster**

There are quite a few 256K ROMs available now, but NEC's (Natick, Mass) Electronic Arrays have a 1M-bit complementary metal oxide semiconductor (CMOS) ROM. These devices can accommodate twice the number of bits that are directly addressable by most 8-bit microprocessors. However, access time is a slow 5 µs. Thus, for most of today's ROM applications, the current crop of 256K chips have the leading edge. The fastest appear to be Synertek's (Santa Clara, Calif) 200-ns version of its SY32356 and Signetics' (Sunnyvale, Calif) 23256A, operating at the same speed.

Others start at 250 ns, and all companies offer slower, cheaper versions for applications that are more cost- than speed-sensitive. Synertek is working on a CMOS 64K chip and Motorola is reputed to be developing a 256K device. Speeds and power dissipations for these devices are not yet definite. Synertek makes a smaller, faster ROM family—the SY3316—with 80-ns access times and a latched ROM version aimed at use in pipelined bit-slice architectures, according to Chris Peterson, strategic marketing manager for Synertek's memory products.

Technologically speaking, most ROMs are still built using N-channel technology in the matrix or NOR configuration. Manufacturers create a fabrication mask from the data tapes given them by customers. Where the bit should be a logic one, nothing is done to create an active device and the voltage level remains high at the output. Conversely, a logic zero is implemented by creating a thin oxide active device that is in an "on" state when selected and shows an output zero voltage level. The mask determines the locations of these active devices in accordance with the tape's program data.

CMOS ROMs are also being developed. Here, one uses p-channel and N-channel device pairs to form simple logic gates for the peripheral decode circuitry. Only during transitions from one state to another is appreciable current drawn. Thus, a CMOS device consumes less power than an equivalent N-channel only type.

Without question, the largest market for ROMs continues to be in game modules or TV game cartridge applications. The game's program is stored indelibly in ROM, which is packaged in a plastic container with an edge connector. Inserted into a microprocessor based game, the ROM program determines such things as screen format, scoring, and sound effects. The actual game dynamics are the result of the processor sampling the game controller position, firing button, and image position data, which are dynamically written and read in RAM chips contained within the game system itself.

The second largest application area is in program memory for general purpose microprocessor based systems. With capacities topping 256K, ROMs can store whole language compilers and operating system software. For systems such as word processors that are used primarily for one application but can also be used for others, a ROM can be used to store the word processor application and operating software. Thus, users do not have to load a diskette each time the system is powered-up. For other applications, the ROM could be deselected and an appropriate program could then be loaded into RAM from diskette.

ROMs promise to continue being the lowest cost read only memory; the trade-offs are masking charges and lead times. Lead times can be as short as 3 weeks for prototypes, but 8 to 12 weeks appear to be the norm for production quantities.

Mask charges are the tooling costs passed on to the customer; they are one way for ROM manufacturers to ensure adequate volumes and margins. At certain minimum volumes (usually negotiable), these charges tend to disappear. These charges also tend to shift lower volume orders to other alternatives such as EPROMs. Most ROM makers balk at requests to quote prices. The standard response is, "It depends on quantity and delivery expectations." Mostek (Carrollton, Tex) volunteered that the price per bit for its 256K device in 100 quantities is about $0.004. How one chooses to use a ROM is critical in taking advantage of its inherently low cost. If the program to be stored is subject to change even once, ROM may not be the most economical approach.
EPROMs: fewer users care about the “E”
More and more designers are putting EPROMs into sockets once reserved for ROMs. The reason is simple: their once-high premium has melted away. Coupled with EPROM’s user programmable abilities and increasing capacities and speeds, the more favorable EPROM prices have had a significant effect on the memory’s application niche. Originally, the erasable feature made them attractive for very low volume and prototype development because they were easily modified and could be purchased in low volumes without a mask charge penalty.

Today, it appears that most EPROMs are used in ROM applications that are too low in volume for ROM or that require faster turnaround. In essence, like the ROM, they are programmed once and never altered. The windowless, 1-time programmable EPROMs being sold by NEC are evidence of this fact. By putting the EPROMs in plastic rather than ceramic packages, and by programming them once, they really become MOS PROMs. The advantages are lower cost compared with EPROMs and faster turnaround than with ROMs.

It is interesting how quickly the EPROM manufacturers have scrambled after the ROM market. In the past, it was not unusual to have a 2-year gap between a ROM introduction and that of a comparably large EPROM. Today that gap has narrowed to less than a year. In fact, Intel’s 27256, a 256K EPROM, was introduced only about six months after the 256K ROMs were.

A lot has happened since Dov Frohman-Bentchkowsky developed the floating-gate avalanche-injection MOS transistor (FAMOS) and with it the erasable PROM technology (see Panel, “Floating gates: the common link”). In addition to Intel’s 256K device, there are several 128K chips in or soon to be in circulation from Seeg Technology (San Jose, Calif), Intel, Mitsubishi Electronics America, Inc (Sunnyvale, Calif), Toshiba America, Inc (Tustin, Calif), Hitachi, Fujitsu, and Oki Semiconductor (Santa Clara, Calif).

The bulk of the EPROM business is in the 64K area. The industry standard 2764 is available in a variety of speeds and power consumptions. The majority of devices offer speeds from 450 ns down to 200 ns. Typically, Icc specifications are 135 to 150 mA. NEC claims the low power NMOS prize with a 64K part that consumes only 80 mA.

For really low power 64K applications, Fujitsu announced a CMOS part with 40-mA active and 1.1-mA standby current ratings. Signetics is reportedly working on 64K and 128K CMOS EPROMs at its new, highly automated, Albuquerque fabrication plant. Rumor has it that the parts will be 30-mA devices with less than 100-ns access times. National Semiconductor has already staked its claim in the CMOS EPROM territory. The company offers a 16K and a 32K part. Both parts offer 53-mW active power (about 11-mA Icc) and 5.3-mW standby. The 32K NMC 27C32 has a 350-ns version, and both parts come in 450-, 550-, and 650-ns versions. National Semiconductor is planning to sample a 256K CMOS part by year’s end.

Device scaling allows rapid capacity and speed increases. Intel’s 256K has cell sizes of only 36 square microns compared to 108 for its 2764. With the variety of EPROMs in N-channel MOS (NMOS) and CMOS, plus capacities from 16K to 256K, it would seem likely that EPROMs will push even harder against ROMs in many applications. Interestingly, the EPROM memory market is still dominated by U.S. manufacturers, unlike the volatile memory market where Japan has garnered major shares in the higher capacities. Domestic manufacturers enjoy a 56% share of the 32K EPROM market and about a 95% share of the 64K market, according to Dataquest (Cupertino, Calif), a respected market analysis firm.

EEPROMs: the benefit of in-system programming
The close relationship between EEPROMs and EPROMs is apparent as soon as one looks at a diagram of the cell structure (see Panel). The floating-gate tunnel oxide structure (called FLOTOX by Intel) permits writing and erasing by having electrons move through potential barriers onto the
Robots?
Not the walking, talking kind, of course. But fully automated machines that produce 128K ROMs faster and better than any human.
You'd be amazed at the delicate precision of their mechanical arms, doing everything from automatic die prep and lead frame preform insertion to eutectic die bonding. And their rapid-fire automatic lead bonding is 10 times faster than manual methods.
They're the results of the advanced technologists at NEC, designed to perform to an inhuman standard of quality.
What that means to you is dramatically higher quality and fast turnaround. 128K prototypes in 40 working days. Production quantities in just 12 to 14 weeks.

Take your pick: CMOS or NMOS.
Our new 128K CMOS ROMs save space and extend product life in low-power applications. Available in standard 28-pin plastic package or 52-pin flat package.
Or choose our 250 ns NMOS ROMs. Edge-triggered for speed and power. In 28-pin plastic or ceramic package.

Come see the robots.
To arrange a tour or just to find out more, write or call NEC Electronics U.S.A., Inc., Electronic Arrays Division, 550 E. Middlefield Rd., Mountain View, CA 94043, (415) 964-4321. Woburn, MA (617) 935-6339; Melville, NY (516) 293-5660; Columbia, MD (301) 730-8600; Pompano Beach, FL (305) 785-8250; Southfield, MI (313) 352-3770; Rolling Meadows, IL (312) 577-9090; Dallas, TX (214) 931-0641; Orange, CA (714) 937-5244; Cupertino, CA (408) 446-0650.
Oh, and don't worry, we also have the very best people in the industry telling these mechanical wizards what to do.

NEC Electronics U.S.A., Inc.
Electronic Arrays Division
Floating gates: the common link

EPROMS and certain EEPROMS have a lot in common. In 1971, Dov Frohman-Bentchkowsky developed the floating-gate avalanche-injection MOS transistor (see Figure). This transistor has the gate surrounded completely by a silicon-dioxide insulator and injects high energy electrons into it from either gate or source. The electron energy levels are created by elevated electric fields in the channel, enabling the electrons to jump the energy barrier posed by the silicon/silicon dioxide junction between the substrate and the gate dielectric.

Once the electrons penetrate the gate oxide, they are drawn by electrostatic attraction to the floating gate, which has been capacitively coupled with a positive bias on the gate above it. Once sufficient electrons are collected on the floating gate and the threshold voltage is elevated to the point where the device channel conducts, that cell is "programmed."

To erase the cell, the floating gate's electrons must be subjected to collisions with high energy ultraviolet photons. As the electrons absorb energy from these collisions, they can traverse the barrier and make their way back to the substrate.

The floating-gate tunnel oxide EEPROM process uses a similar floating-gate structure. However, a thin tunnel oxide is created that allows electrons to tunnel in accordance with the Fowler-Nordheim tunneling mechanism. Again, these electrons are collected on the floating gate and, ultimately, conduction is induced in the channel. To erase this cell, the drain is held positive while the gate is grounded, thereby reversing the tunneling process and removing the electrons from the floating gate.

Because of the thin oxide (less than 200 Å thick), there are two factors involved in EEPROMs: endurance, or the number of times the cell can be programmed and erased, and retention, or the length of time that the number of electrons remains high enough to ensure adequate threshold potential.

EEPROMs appear to be at the same evolutionary point as were early EPROMs. That is, the technology has been accepted but the architectural details and product features still need to be settled on. At the 64K level, indications are that Intel and National Semiconductor will follow Xicor, Inc (Milpitas, Calif) and offer products that are largely compatible with other memories. These will be self-timed, 5-V only devices with onchip latches; they can be connected to a conventional memory bus without creating havoc due to unfamiliar waveform timing requirements, according to Richard Orlando, product marketing manager at Xicor.

In fact, Xicor has already announced its 64K, as has Hitachi. National Semiconductor is rumored to be moving faster than expected, and may be bypassing its NMC 98C32 32K CMOS product by...
IT'S TIME TO TAKE YOUR PLOT 10 IDEAS OUT OF STORAGE.

Give your imagination the benefit of the latest graphics technology, with a D-SCAN dual-microprocessor GR-2412 raster terminal.

For example, the GR-2412's remarkably fast, remarkably accurate 4014 emulation makes it a snap to add color and selective erase to existing PLOT 10 routines.

And its high resolution 1024 x 780 raster display, with exclusive anti-aliasing hardware, means image quality that rivals a storage tube.

If your ideas grow too big for PLOT 10 to handle, you can always take advantage of the GR-2412's unsurpassed collection of standard graphics features. Like local transformations. Closed figure drawing. Up to 768K bytes of local segment memory. And a software utility package that can replace lines of PLOT 10 code with a single FORTRAN statement.

Something else to consider while you're thinking about the future.

Our past. D-SCAN products have been field proven for over a decade. And every one is crafted by Daini Seikosha Co., Ltd. (Seiko), known worldwide for its precision watches, robots, and computer peripherals.

For immediate information on the GR-2412, contact Seiko Instruments U.S.A., Inc., 2620 Augustine Drive, Santa Clara, California 95051. Telephone (408) 727-0768.

Because ideas in storage don't get any better. Just older.

D-SCAN
Seiko Instruments U.S.A., Inc.
Synertek's 256 x 8 EEPROM represents a different trend for these products. Whereas many manufacturers are pushing to higher capacities with conventional EPROM- and ROM-like EEPROMS, some are making smaller products with I/O port-like interfaces. These are ideal for use as external memories, since single-chip microcomputers interface more easily with them than with conventional memories.

announcing a 64K product instead. As with other CMOS memories, the cell array is done using N-channel floating gate but the peripheral circuitry is done in CMOS, according to Drew Osterman, the company's MOS memory marketing manager.

The first 16K EEPROM was Intel's 2816. It required both higher voltage and external wave shaping for programming and erasing. Its look-alikes, too, required external support. Now, with Intel's 2817A, National Semiconductor's compatible NMC 9817, and other compatibles, much of the external circuitry has been put onchip.

Larger devices, like NCR's (Miamisburg, Ohio) 32K 52832 and Inmos' IMS 3630, are putting onchip latches on the die so that several bytes of data can be shifted in quickly without holding up the bus for the typical 10-ms write and erase cycles. With these onchip latches, the microprocessor can hand off the data to the chip in a few hundred nanoseconds, freeing the bus to do other things. Dramatic reductions in programming time are accomplished with this method. For example, in the IMS 3630, it could take 83 s to fully program a 64K EEPROM, but with the chip's 64 bytes of registers, the whole chip can be programmed in only 128 cycles or about 1.2 s, according to Fred Jones, Inmos' strategic marketing manager for memories. "The effect is to have our 3630 behave much like an edge-activated RAM," Jones said.

Whereas some EEPROM manufacturers are keeping one step behind the capacities of EPROMS, others are opting to produce smaller parts. General Instruments (Hicksville, NY) makes the ER5901, a byte-wide 128- x 8-bit device, and also a 16 x 16 serial device. The first device finds much use as a DIP-switch replacement in terminals and other systems, and the serial device finds use as a memory device in stereo receiver and TV receiver electronic tuning, according to Mort Kalet, the company's EEPROM product marketing manager. National Semiconductor is another company that has found a niche for its 256- and 1K-bit EEPROMS. "Automotive manufacturers are using them for electronic odometer memories," marketing manager Osterman explained. Interest in National Semiconductor's 8-pin, mini-DIP EEPROMs for automotive odometers is growing domestically as well as overseas, according to Osterman. NCR is another vendor that produces and markets a 16 x 16 serial EEPROM.

Seeq Technology announced a family of EEPROMS that includes a 16K, a 32K, and a 64K part that Ken Kwong, memory products marketing manager, says will be available this year. Kwong is the most outspoken of those who see EEPROMS rapidly pushing EPROMS to the wall in terms of price. "The major cost factors are die size and testing," Kwong explained. Testing costs for EEPROMS could fall below those for EPROMS because of the more favorable write and erase speeds. Kwong claimed that Seeq's use of innovative metal line plasma etching has helped to scale EPROMS down from the more typical 10 microns to 6 microns. As a result, said Kwong, Seeq is producing 64K dies that are actually smaller than 64K EPROM dies.

Others are more reluctant to prophesy a major collision between EPROMS and EEPROMS. The consensus is that the 2 to 2.5 price premium per bit is likely to remain intact for a while longer, ensuring that the competition between the two remains more frictional than head-on.

Like EPROMS, EEPROMS are being read with 200-ns or longer cycles. One notable exception is Motorola's MCM 2832, which has a 150-ns maximum read access specification.

Programming: an issue with EPROM and EEPROM

The ability to both program and erase an EPROM hastened its early popularity. This quality, coupled with the ability to perform these tasks in-system, is EEPROM's key advantage. However, manufacturers of both types of memory are concerned with shortening the time it takes to program their devices.

Intel described a method for programming EPROMS in which a 1-ms pulse is applied while the Vcc level is held to 6 V. (Traditionally, a nominal 50-ms programming pulse is used for each cell.) As soon as the cell exhibits a one-to-zero transition, it is hit with a longer pulse four times the total of the sum of pulses up to that point. Thus, if the transition occurs
Each of the above computer systems is different. Not just outside because of color. But inside as well, because each is configured for a totally different set of user needs.

They are Momentum 32/4s, inside and out perhaps the most versatile desktop business systems ever offered to OEMs.

**Styled By Bertone. Powered By 68000™ And System III UNIX™**

The look of the Momentum 32/4 gives you an immediate sense for its capabilities. Its lines wrap smartly around the most compact chassis in its class, a chassis really in a class by itself, thanks to the styling of Italian master designer, Bertone. But while style can catch the attention of the OEM, only performance can keep it. And with the Momentum 32/4, that performance starts substantially with the industry-standard M68000 microprocessor and the enhanced System III UNIX operating system—but there's more of the same.

**More Innovation And Versatility: From The Graphics Package To The Storage Package.**

For OEMs, market edge comes with system uniqueness. Uniqueness achieved with the least hassle for the fewest dollars.

The Momentum 32/4 performance features give OEMs that edge.

There's Direct Memory Access and the proprietary Memory Management Unit, both of which significantly enhance system throughput. There's 1/2 megabyte of RAM memory, standard. Three additional serial ports, standard. Word processing and spread-sheet, standard.

The versatility of the Momentum 32/4 is apparent everywhere. There's a completely customizable external I/O board. A powerful graphics board option, controlled by its own 68000 processor, features 256K of RAM and functions that are totally software definable. Even the storage package offers the versatility of two Winchester cartridge drives, delivering ten megabytes of on-line capacity as well as removable backup capability.

**Put Momentum Behind Your System.**

The Momentum 32/4 provides plenty of reasons why you should. But there are others. One is the fact that the 32/4 is part of, and fully compatible with, the largest and highest quality line of UNIX-based 68000 computer systems in the industry. And the fact that the 32/4 is the product of a company that makes only UNIX-based 68000 computer systems. A company that can boast unmatched configuration versatility within its standard product line. But a company that also knows you have to work closely with OEMs—to be, wherever necessary, an extension of their operations, from custom design through quality control. And lastly, a company with the engineering and manufacturing resources to deliver these high-quality products in quantity, on time, at the lowest possible cost. Momentum. Put it behind your system today.

---

32/4 is a trademark of Momentum Computer Systems International.
UNIX is a trademark of Bell Laboratories.
68000 is a trademark of Motorola Corporation.
after two pulses, another pulse 8 ms long is used and the cell is adequately programmed in about 10 instead of 50 ms.

The scheme allows up to 15 pulses before the cell is declared faulty. Thus, cell programming could take as long as 60 ms. However, according to Intel's Don Knowlton, 5- or 10-ms programming is much more the norm. Called "intelligent programming algorithm," the process can be used on any manufacturer's EPROMs. PROM programmer manufacturers Data I/O Corp (Issaquah, Wash) and Pro-Log Corp (Monterey, Calif) are incorporating such algorithms in their systems' hardware and software.

Other methods for speeding up programming are gang programming of two or more EPROMs and special chip control lines that allow several cells to be tested at once. Many manufacturers are adopting such innovative techniques to speed up EPROM testing in order to better control production costs.

**Bipolar PROMs cannot be beaten for applications requiring speed.**

As already mentioned, many of the newer EEPROM products have onchip latches. These latches permit several bytes of data to be loaded quickly into the latches, then to be written internally to the EEPROM array, which is isolated from further bus activity. In addition, NCR and Inmos permit the actual voltage thresholds to be determined both during manufacture and later while the parts are in a system. From those data, storage retentivity can be calculated and, if necessary, the device can be quickly reprogrammed to avoid potential loss of data at some later time.

Another EEPROM feature that could increase programming speed is a bulk chip erase function. There is some difference of opinion, however, in the practicality of that function. Xicor's Orlando feels that some users see chip erase as a threat. "Some found out early that depending on how they socketed their EEPROMS, they could accidentally erase the first byte on power-up," Orlando explained. "The prospect of wiping out the whole chip's memory by mistake is even more intimidating." Hence, chip erase is not a feature on Xicor's X2864A.

RAM chips, the proverbial scratchpads of a computer, are rapid read/write memories and are used for very temporary storage of interim data. However, when the power goes down, unless the RAMs are backed up by batteries, the chips develop amnesia and the data go away. Elaborate approaches to quickly dumping RAM storage to disk upon sensing a drop in supply voltage have been tried, but the fear of losing important data from volatile memories still looms large in the hearts and minds of computer users.

CMOS RAMs with battery backup are a simple way to ensure against such data losses. However, for remote systems in facilities where personnel cannot visit very often to check on the batteries' health, the risks increase. Enter the NOVRAM, typically a static RAM with an EEPROM shadow. In most cases, the chip behaves like a static RAM, but upon power-down, it stores its data in EEPROM. If NOVRAMs were priced only slightly higher than RAMs and batteries, one would expect a wholesale shift to NOVRAMs for such applications. However, right now, NOVRAMs are expensive. One reason is that they encompass a fairly recent technology. Another reason is that the one-for-one memory redundancy is a gluton for silicon die area.

Xicor established the NOVRAM concept with its 4-bit wide family, including the X2210 and X2212, 64 x 4 and 256 x 4 chips, respectively. It has since developed 8-bit wide 1K, 2K, and 4K parts, the 2001, 2002, and 2004. NCR has mirrored the Xicor line with its own 4- and 8-bit products fabricated in SNOS and NMOS. Except for the prefix 5, the part numbers are identical (eg, 52210, 52212, and so on). NCR also makes a 128 x 4 52211, a chip that Xicor does not make.

General Instruments has announced its 4K ER5304, but the product appears to be on the back burner since the company's attention is mainly focused on its EEPROM products. Intel, too, will join the select club of NOVRAM makers when it introduces its own 4K device. Intel's part, like those of NCR, is reputed to have automatic power-up recall. This feature provides automatic copying of the EEPROM data to the RAM upon power-up.

As battery-backed-up RAMs are serving applications, NOVRAMs are also being used (like some EEPROMs) for DIP switch replacement in terminals and other peripheral systems. Xicor also makes a 16 x 16 serial device, the X2444, which it says is a

**Featuring metal lines scaled down from the typical 10 microns to only 6 microns, Seeq Technology's S2B13 16K EEPROM enjoys a die size comparable to similar capacity EPROMs. This EEPROM is said to actually have a smaller die than the company's own 64K EPROM.**
Now GEN.II™ delivers Tek 4010/4014/4027 compatible graphics on your VT100, VT101, VT102, VT103, VT131, or VT132.

Generating cost-efficient yet sophisticated images on your DEC™ terminal first begins with your choice of VT100™ Series displays. Then add Digital Engineering’s GEN.II Retro-Graphics terminal enhancement. Our plug-in upgrade transforms an otherwise "dumb" terminal into a multi-featured bit-map graphics workstation, capable of plotting complex business and technical renderings. In a raster-scan resolution of 800 by 480 and in concert with your Tektronix®-based program.

But best of all a Retro-Graphics enhancement costs only a fraction of what you’d pay for an equivalent graphics terminal: about $1200-1800, depending on the GEN.II model you order.

**Introducing GEN.II Retro-Graphics for DEC.**

**More graphics power and Tek™ simulation.**

An easily installed PC card assembly, our second-generation enhancement provides emulation of the Tektronix 4010 graphics terminal plus one-color simulation of the Tek 4027 color graphics terminal.

And for extra power — and compatibility with your existing or future Tek 4014 applications programs — GEN.II for DEC also features one-color 4014 simulation. With little or no software modification.

In addition, GEN.II’s 32 Kb’s of “local” intelligence ensures that images come up quickly — and costly terminal-host data transmissions are held to a minimum. And because GEN.II is based on industry-standard Tektronix protocol, graphics programming and operation are considerably eased. Case in point: by entering from the keyboard or computer the following command string

```
PIE 100, 0, 360, 45
```

an eight-sided polygon with a radius of 100 will be plotted and its interior will be filled with a shading pattern. (GEN.II maps 4027 colors to dithered shades). With similar high-level command strings, GEN.II will also perform arc and vector drawing. Define and shape text characters. Store and recall graphs. And, while in 4014 mode, perform additional graphics annotation using all four 4014 character sets. And you get all this with no loss of existing terminal features.

**Software compatibility ensures your long-term investment.**

Since our GEN II products for DEC provide 4010/4014/4027 compatibility, their use with utility and applications programs, whether now or in the future, is guaranteed. Currently, more than 20,000 Retro-Graphics products are performing successfully on graphics programs such as DISSIPLA® and TELLACRAT, PLOT10™, Template™, DI-3000™, and ILS®.

**Graphics I/O and solid backup throughout.**

Digital Engineering has built a solid foundation of “user-chosen” interactive tools for GEN.II. For instance, a crosshair cursor and light-pen port (for our optional light pen) are standard features, while optional interfaces allow you to simultaneously interact with a digitizer while outputting to an impact or non-impact serial printer and video device.

Comprehensive documentation assists at every level of operation. A worldwide distribution network assures prompt delivery and backup. And whether you tap our service network or opt for on-site service — from one of the largest field service organizations in the world — your needs will be quickly met.

DEC’s VT100, VT101™, VT102™, VT103™, VT131™, or VT132™ and Digital Engineering’s GEN.II Retro-Graphics — for high-grade imaging in a low-cost graphics system.

Call us today for full details, demonstration, and the name of your local Retro-Graphics distributor — your “one-stop” source for graphics.

Retro-Graphics is a registered trademark and GEN.II is a trademark of Digital Engineering, Inc. © 1983 Digital Engineering, Inc.
fine companion for single-chip microcomputers. Unlike microprocessors that are designed for external memory interface, single-chip devices deal with the outside world through ports. According to Xicor's Orlando, a serial device like the 2444 is a good fit with the port interface architecture. He feels that using a separate microcomputer chip plus a small NOVRAM is a far better solution than making a monolithic single-chip with onboard EEPROM as Seeq Technology is doing. Said Orlando, "It's a lot cheaper to use a $2 single chip and a $2 NOVRAM than to pay $30 for a monolithic." One can see how Xicor prices its serial device.

**Bubbles were once touted as the be-all and end-all of memory technology.**

As for other devices, the 100-piece price quotes for NCR's line are $5.50, $8, and $12 in ascending order of capacity for its 4-bit wide parts; and $16, $28, and $61 for the byte-wides. The premium for NOVRAM is glaring when one considers paying $61 for a 1K part!

As long as the preferred device continues to be a 6-transistor static RAM cell coupled one-for-one with either floating-gate or SNOS EEPROM cells, price reductions due to smaller dies will be slow in coming and not very dramatic. However, in a recent International Electronic Devices Meeting (IEDM) paper, Mostek's D. Guterman suggests using a single transistor dynamic RAM cell tied to a small EEPROM cell made using a vertically integrated triple-polyisilicon process. The end result is a 1.5-mil² cell. This method could lead to future higher density, lower cost NOVRAMS.

**Bipolar PROMs: the niche still exists**

Remember bipolar PROMs? They are still around and cannot be beaten for applications requiring speed. The biggest, the Fujitsu 7143, is just 64K, but read access is a rapid 55 ns. This PROM was built using diffused eutectic aluminum vertical fuses. Unlike the surface-level, horizontal fusible links in other PROMs, these links are subsurface. According to Allen Hu, product marketing manager for bipolar PROMs, fusing the links will not rupture the passivation layers.

Signetics is now announcing a 32K 80-ns part using its nichrome fuse technology. However, Signetics' Geoff Dyer said that faster parts are in the works. He explains that these parts will obtain the higher speed by switching from junction isolation to oxide isolation with a technology called avalanche-induced migration (AIM). Signetics is expected to announce a 16K with speeds down to 30 ns or better. And, by November, it expects to have a 32K in the new technology with twice the speed of the current one.

Harris (Melbourne, Fla) is another 64K PROM vendor, but the main business still seems to be with 16Ks and 32Ks. National Semiconductor's DM875321 is a 55-ns 32K device; Monolithic Memories (Sunnyvale, Calif) makes one specified at 50 ns. These devices obviously do not compete with 200-ns EPROMs for sockets. In fact, the largest application continues to be in program and control store, particularly in bit-slice processor based systems.

System pipelining is an approach in which a processor overlaps operational cycles. For example, the processor may be fetching the next instruction while it accesses the preceding data and executes the instruction before that one. Some manufacturers, National Semiconductor for one, are putting registers in their PROMS to support such pipelined architectures. In essence, the data in the first location are latched in the register while the PROM is already setting up the next data word.

Monolithic Memories, which has been steadfastly committed to bipolar technology with PROMS as a major part of its business, is not rushing to a 64K part. When asked why, Dan Medler, product marketing manager, answered that demand for that part has not become widespread. He sees the part as attractive primarily to the military at this time. Fujitsu's Allen Hu confirmed that view by estimating that more than 50% of his company's 64K business is for military applications.

**Bubbles: still floating, not bursting**

Bubbles are an interesting technology. They have been included in this article because, like the others, they are solid state, nonvolatile memories. Unlike other memories, they do not use semiconductors. Instead, they are a magnetic technology most similar in concept to Core memory. Core, like the vacuum tube, has largely been displaced by semiconductor memories, but the bubble continues to control certain application areas.

Historically, bubble technology was pioneered at Bell Laboratories (Short Hills, NJ). Early proponents of the concept were Texas Instruments and Rockwell. A bit later, National Semiconductor announced a research and development effort aimed at producing bubble products. One of the last domestic manufacturers to try its hand at bubbles was Intel. But Intel entered tumultuously by starting at the 1M-bit level and truly leapfrogging its competitors.

For users, bubbles were an enigma. Engineers versed in 5-V square wave pulses were now faced with triangle current pulses and strange timings. Those manufacturers who offered a bubble chip and left the interface and control details to the
Memorex Introduces 14" Drive Capacity And Performance In A 5¼" Disc Drive Package.

When Memorex decided to be a major manufacturer of 5¼" products, we already had an edge. An edge which we have now designed into a new family of 5¼" disc drives which not only meets today's system requirements but has designed-in capabilities to support tomorrow's needs for even higher capacity and performance.

The Memorex 500 Family: Expandability, Accessibility And Reliability.

The first three members of our 500 Family, the 510 Series, feature a choice of 30, 50 and 70 megabytes of capacity with an industry-standard 5¼" disc drive interface. Average seek time is 25ms which, when combined with our switch-selectable "SECA" mode, significantly reduces net system time-to-data. Our linear voice coil actuator and advanced servo design give a maximum seek time of only 45ms and a track-to-track time of just 3ms. But even more significantly, this technology sets a base for future drives with higher capacities and even faster access times.

Above all else, reliability and quality are key to the 500 Family design. By choosing a base design with capabilities well beyond the current series, our drives feature servo and read channels with extremely wide operating margins. And by using an advanced electronic architecture with five interconnected microprocessors, we provide adaptive control systems which continually monitor critical parameters throughout the life of the drive and make dynamic adjustments to compensate for wear and component aging. In this way we obtain and retain true reliability throughout the life of the system.

Working Within The Systems: Today And Tomorrow.

It's a Memorex tradition, a summary statement that speaks to our experience, technology and resources. And it's a commitment to supply a complete family of 5¼" rigid disc products, such as our 400 Series fixed/removable drives for system back-up, our 510 Series drives for high capacity with fast access, and products yet to be announced in the 400 and 500 Families.

Call Memorex OEM today for complete information.

Memorex Corporation, OEM Equipment Sales, San Tomas at Central Expressway, Santa Clara, CA 95052, (408) 987-3308, Telex 334492.
In Europe: Staines, England 078451488, Telex 93508, Hamburg, West Germany 0406322075, Telex 215019, Frankfurt, West Germany 06116051, Telex 411240, Liege, Belgium 041644544, Telex 23438
It takes only five support chips to interface a microprocessor to Intel's 4M-bit bubble memory. The host bus is tied to the 7224 bubble memory controller and the host treats the entire subsystem as a typical I/O subsystem. All pulse shaping and timing is handled by the support integrated circuits.

designer found a largely unresponsive audience. Perhaps, thorough planning, hindsight, or both led Intel to announce its bubble chip with an array of support components that would simplify a designer's interface problem. In effect, the control complexity was designed into the support chips, leaving designers with a fairly straightforward peripheral-like interface.

In their early days, bubbles were touted as the be-all and end-all of memory technology. Visionaries saw bubbles cutting a swath through the likes of RAMs, ROMs, PROMs, and even disks. More sober outlooks had bubbles gaining a foothold in harsh environment system applications, increasing their share according to price and speed factors. Bubbles have, in fact, gained that foothold. They are used for storing operation programs for automated machinery and numerical control machines. Another demand just beginning to emerge is what some call "working storage," a kind of briefcase of the future. With a large market forecast for small, battery-operated portable computer workstations, bubbles offer a means to travel with much file storage in a relatively small volume.

A typical scenario has a user downloading from a data base the portions of files that he or she might need while traveling or while away from company headquarters. Of course, tape cassettes or flexible disks can be used for that purpose, too. However, bubbles are faster than both cassettes and disks and are very portable. As the number of portable systems grows, bubble use in portable applications will probably grow commensurately.

As for vendors, the original list of participants has dwindled considerably. Rockwell, Texas Instruments, Mitel Semiconductor (San Diego), and National Semiconductor have all moved on to other things, citing a variety of reasons for their respective decisions. Domestically, Intel and Motorola continue to build and sell bubble memories. Hitachi and Fujitsu make up the Asian vendor list.

Today's largest bubble is the Intel 7114, a 4M-bit device. Its architecture is very similar to that of the original 1M-bit 7110, but the number of its quads has doubled to eight and the number of bubble sites in each loop has also doubled to bring a four-fold capacity increase.

Intel is using X-ray lithography to achieve its submicron widths, but continues to use a 50-kHz field rotation rate. In addition to Intel's 1M-bit bubble, Fujitsu and Hitachi are also believed to be sampling their own 1M-bit parts. They, however, use a 100-kHz field rotation frequency and their parts, at 13 to 15 ms, operate faster than Intel's at 40 ms. The trade-off is that the Japanese-made products are not specified to the same upper temperature limits as the Intel parts are. Intel will guarantee operation at 70 °C, whereas Hitachi guarantees it at 60 °C and Fujitsu at 50 °C.

Motorola and Intel recently agreed to a second-sourcing arrangement whereby they will use the same technology and architecture plus compatible packaging. Both will probably continue to stress Intel's component-level strategy. In contrast, Fujitsu and Hitachi have emphasized a board-level and cassette-level marketing posture. They both offer bubble board products at the 1M-bit level that include the necessary support circuitry. Interestingly, both Fujitsu and Hitachi use far more support chips for their bubbles than do Intel and Motorola.

Price competition is warming up, but with so few players, no one appears ready to sacrifice profits. Current prices on the street are about $200 to $300 per megabit in OEM quantity.

With the present state of the bubble market, the vendor list should remain stable. In the face of rapidly increasing markets such as that of working storage, others may again venture into bubble manufacturing. It is a safe bet that bubble prices will not fall dramatically—but fall they will.
The best micro-mini you've never seen. It's on the previous page. All alone. Because there isn't another computer made with the power, the performance and the low price of the Plessey System 6600/6700.

We've put the squeeze on the minis. Our micros are the closest thing to a mini that you can get. And getting them from us costs about 30% less.

The Plessey System 6600 is our 256 kbyte powerhouse. The fastest 84 Mbyte Winchester hard disk known to man. A 9x hex-wide backplane. Six communications ports standard, add more if you need them.

Or go to our System 6700. It's the top of our line and packs all the wallop of a 22-bit mini while still allowing you to use 18-bit controllers. It's everything that the 6600 is, but has Plessey memory mapping and supports up to 4 Mbytes of main memory. So you get faster response times and more users per system for your business, scientific industrial and communications applications.

The 6600 can be easily upgraded to the 6700 by adding our memory mapping board and additional memory (no cabling, no software changes).

And both systems can be expanded with floppies, more hard disks, start/stop and streamer tapes, terminals and any other peripherals you need.

DEC and UNIX and CP/M and you.

Both systems support whatever you're doing (or will be doing) in software: DEC™ operating systems like RSX-11M/M+™, RSTS/E™ and RT-11™ or TSX-Plus.™ UNITY™ (System III UNIX™) and the new crop of software. M-11 (MUMPS) and hordes of public domain applications. And even CP/M™ and all those low-cost programs.

And you can use BASIC, COBOL, DIBOL™, C, PL/I, FORTRAN, Pascal and MACRO™ languages to develop your programs just the way you want them.

Don't miss out.

For a closer look at the best micro-mini you've never seen, contact: Plessey Peripheral Systems, Computer Systems Division, 17466 Daimler, Irvine, California 92714. (800) 854-3581 or (714) 540-9945 in California.
Virtual memory systems offer an appealing solution to the problem of limited memory capacity in microprocessors. Whereas the 64K-byte address space of a decade ago may have been adequate for applications of that time, today's multi-user, multiprogram environment requires a much larger address space than ever before.

There are several ways of designing a computer system that will handle the memory capacity needed in a large address space environment. The approach used by many mainframe manufacturers—to ship a full complement of physical memory with each system—does give the user enough memory to service the total address space potential of the host central processing unit (CPU), but it is very expensive.

The virtual memory approach is to divide the total memory into two parts: main memory directly accessed by the CPU, and peripheral memory (e.g., disk) that complements main memory in providing the total address space. If designed correctly, this virtual memory is completely transparent to both programmer and user, who have the illusion of possessing more main memory than actually exists. A very sophisticated virtual memory system also offers user and memory protection, and a certain amount of debugging capability.

What has made virtual memory systems so appealing, however, is that when properly designed, they offer an inexpensive way of obtaining large amounts of address space because of their use of low cost peripheral memory.

How virtual memory works
All of today's 8-bit devices are limited to a 64K-byte address range. With the advent of the 16-bit microprocessor, the user's address range expanded somewhat, with one manufacturer offering 1M-byte and others 24-bit (16M-byte) address ranges. With the introduction of National Semiconductor's NS16000 family, the available address range was extended to a full 16M-byte address space, but the new CPU can operate many times faster because it was designed with 32-bit registers, arithmetic logic units, and internal data paths.

by Gary Martin

Gary Martin is a systems development engineer for National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, where he is involved in technical marketing. Mr Martin holds a BS in computer science from The College of William and Mary, Williamsburg, VA.
DEMAND PAGED LOGICAL AND VIRTUAL ADDRESS SPACE

TOTAL OF 32,768 PAGES FOR 16,777,216 BYTES OF DEMAND PAGED VIRTUAL MEMORY

PAGE SWAPPING AS REQUIRED

(a)

Fig 1 With demand paged memory (a), page swapping involving disks employs pages of uniform size and a simple replacement algorithm. Segmented swapping (b) needs a more complicated replacement algorithm to match incoming segments with available memory space.

For a large address space to be beneficial and still stay within the competitive price range of a small computer system, computer designers hope to implement virtual memory that, in essence, allows the original equipment manufacturer to combine primary storage (main memory) with secondary memory—such as disk—in such a way that memory management functions appear transparent to the user. In this way, extremely large operating system software and application programs can be used without the user having to worry about the system's hardware limitations.

In a virtual memory computer, the user’s program only references virtual addresses, which are translated to physical addresses. Virtual addresses reside either in main memory, in which case the program continues normally, or in disk memory. If the referenced address is on disk, a user’s program is suspended. A special system routine is called up that swaps the disk location with an unused main memory location. Once this routine is completed, the user’s program is resumed. For maximum efficiency, locations that are likely to be referenced next are brought from disk into main memory at the same time.

Segmentation versus demand paging

The two predominant types of virtual memory used today are segmentation and demand paging (Fig 1). Demand paging—the basis of the company’s NS16082 memory management unit (MMU)—is far more efficient and faster than the segmentation approach.

Segmentation divides the address space into a number of segments of varying length, each corresponding to specific programs or data. Segmentation’s limitations emerge when attempting to allocate the main or disk memory resources. The minimum unit that can be swapped when using segmentation is the segment itself. This means that a segment must reside entirely in physical (main) memory or disk, and that there must be a contiguous hole large enough in main memory...
It's your choice.
At Rosscamp, we build the industry's finest, most dependable ¼-inch magnetic tape drives to back up high-capacity Win­chesters. Our D160 records 160M bytes on 24 tracks in less than 20 minutes, uses standard ¼-inch tape, and fits into an 8-inch envelope. No one else can say that.

No one.
So for Winchester back up that really works, come to the experts. Us. Write for details on our Evaluator Package, and see for yourself how well we back you up.
Think about it. You've come a long way in storage capacity.
And that means you've got a lot more to lose.

ROSSCOMp
We're backing up your future.
16643 Valley View Avenue, Cerritos, CA. 90701 (213) 926-5533
CIRCLE 91
whenever a segment is swapped in. If a large segment of data—about 100k bytes—has to be swapped out of main memory to make room for another segment that the program needs to continue, all 100k bytes must go, not just some. This not only ties up the system and local bus for the direct memory access transfer, but it demands higher disk drive transfer rates.

Other problems arise if, in the middle of an instruction, the program finds that the data it needs must first be swapped from disk into main memory. If there is no facility for abort and retry instructions, then all data segments must be in memory simultaneously. If they are not, a segment fault is detected and the program stops.

This is the primary reason such systems demand large amounts of main memory. Consider, for example, a program that is 20k bytes long with data tables of 100k bytes. Therefore, the minimum amount of main memory required each time that the program is loaded for execution is 120k bytes. Not many systems can afford that kind of main memory for several tasks.

Another major problem with some segmentation schemes involves the small number of segments that can be active at the same time and the granularity of protection. For instance, one manufacturer's MMU allows 32-segment descriptors to reside onboard for high speed translation. This may seem like enough for most applications, but it is not. Each task alone consumes one descriptor for its program and another for its data. More typical programs take up to four or five descriptors. For this reason, an average system can allow only a few tasks to be active at a time. Segment descriptors must be loaded before, and remain for the duration of, the program segment's execution.

As an additional handicap, segment descriptors can only identify memory spaces that are multiples of a power of two (eg, 2K, 4K, or 16K). To allocate the right number of bytes for a particular segment, extra descriptors must be used, thereby consuming an already expanding descriptor space.

If, as is many times the case, more bytes are assigned to a data structure than are needed, the excess bytes become wasted space. This process is known as internal fragmentation. If a program is 1500 bytes long, for example, and 2K bytes are allocated for it, 500 bytes or 25% of the space is wasted; either segment descriptors are added to gain resolution (at the cost of scarce descriptor space) or memory is lost through internal fragmentation. Either alternative is unacceptable.

Segmented systems exhibit another often debilitating problem called external fragmentation. Since various-sized segments are used, it is necessary to find a proper-sized hole to place them in before swapping. External fragmentation results when the holes between segments are too small to accommodate an incoming segment. When this occurs, the operating system must decide whether to take out a segment large enough to create the required space or to crunch existing segments to make enough room. The first option is usually the one chosen because few computer architectures allow the dynamic relocation of programs and data required by the second. Fragmentation occurs with both primary and secondary storage.

The replacement algorithm assumes the role of determining which segment to swap out. In segmented systems, this decision has a great impact on system performance. If a small segment is removed, it may not create enough space; hence, several segments may have to go at once. If a large segment is taken out, much time is wasted on the transfer, throughput is diminished, and performance once again suffers. As an additional complication, if a large segment is swapped out, the space can become fragmented by smaller segments. When an attempt is made to swap the original segment back in, the hole no longer exists.

As can be seen, the optimum replacement strategy for segmentation is important. Not only is the probability of referencing a given segment difficult to predict, but the penalty for making a wrong decision is high. In addition, the operating system overhead for replacement algorithms and swapping has adverse effects on overall performance.

In recent years, the advantages of demand-paged virtual memory have caused some large computer makers to abandon the segmentation approach entirely. For example, following IBM's lead in its System/370 of the 1970s, Digital Equipment Corp has designed demand paging into its VAX-11 series, as has Data General in its MV8000 minicomputers.

Demand paging—the way to go

Demand paging systems solve all of the problems experienced by the segmentation approach to virtual memories. Demand paging divides both the virtual address space and main memory into equal-sized segments, called pages. The most obvious advantage of this method is that, because all pages are of equal size, pages can be swapped without leaving unusable fragmented spaces. In addition, it is not necessary to swap in all of a program's pages at once, just the page or pages required to carry out the immediate routine. This greatly reduces the time spent in swapping, since, as in the case of the NS16000, pages are only 512 bytes long. As a result, operating system overhead and performance improve tremendously.

Since there is absolutely no external fragmentation problem, the penalty for making a wrong prediction on a page swap is also greatly reduced.
NOBODY DELIVERS DEC CONTROLLERS LIKE PLESSEY.

Because nobody has the range of DEC-compatible controllers and mass storage subsystems that Plessey has.

Controllers, floppies, cartridges, disc packs, Winchester and magnetic tape, including a proven 1/4" streamer. All the storage you need for your LSI-11, PDP-11 or VAX computers. (Complete subsystems with savings of up to 50%, too).

Just check the chart, then check us out at (800) 992-8744.

We can also help your budgets and your systems with communications multiplexers. And with a huge selection of memories, typically 30% less expensive than the DEC equivalents. 32 kbytes to 1 Mbyte. ECC, parity and non-parity. MOS and non-volatile core.

They're fully DEC-compatible, but run up to 30% faster, occupy less space and come with an extensive 1-year warranty.

And we'll back you up with our own worldwide network of factory-trained specialists. They can service products from a variety of vendors and answer all your questions about configuration, operation or software. You get the responsiveness of an in-house technician at a fraction of the cost.

Nobody else even comes close.

For the rest of the story, contact: Plessey Peripheral Systems, Computer Products Division, 1674 McGaw Avenue, Irvine, CA 92714. Telephone (800) 992-8744 or (714) 540-9945.

PLESSEY. ASK ANYBODY.

©Plessey Peripheral Systems 1983 DEC, LSI-11, PDP-11, VAX trademarks Digital Equipment Corp.
The replacement algorithms concentrate on which page must be replaced rather than which segment. Hence, many programs can have pages in main memory simultaneously, and share memory with pages that have been most recently used. This reduces the frequency of page swapping.

The NS16000 also fully supports abort and retry instructions. Any memory reference—whether for instructions or data—can be terminated in mid-cycle. When this happens, the microprocessor saves the state of its operations to allow an instruction retry. An instruction retry occurs after the page containing the instruction or data is swapped into main memory. This means that both program and data pages can be swapped in dynamically (on demand). The implication, of course, is that a greater number of processes can reside in far less physical memory than is possible with segmentation.

In addition, this system allows a great variety of protection codes on each page. The MMU can be programmed to prohibit any combination of read or write references, depending on the task at hand. Protection can also be differentiated between supervisor and user modes.

Debugging has been designed as a function of the NS16082 MMU. The reason for this design is that it is in an excellent position to monitor program behavior because it resides on the address and data buses (Fig 2). Debugging is provided by the breakpoint and program-flow registers. Breakpoint registers can be programmed to monitor the address bus for any read, write, or execute reference. Program-flow registers record the addresses of consecutive, nonsequential program fetches and can be used to reconstruct the most recent two branches in the instruction flow.

Because of the nature of virtual memory, two sets of translation tables can be used within the system. This dual address space mode allows independent mapping of computer tasks and acts primarily to secure the operating system from destruction. This feature can be used to run several operating systems on one machine and to simply keep user tasks and the kernel physically separated. Thus, the operating system never loses control of the machine.

Dynamic address translation

To reduce the number of NS16000 CPU and MMU pins (there are 48 for each), both units share the same multiplexed address/data bus. During the time the MMU needs to access memory translation tables, the MMU can assume full control of the bus. The address space itself is divided into 32,768 fixed pages of 512 bytes each (Fig 3), as opposed to 64K bytes for some other microprocessing systems using segmentation schemes. This enables the NS16000 to transfer data in and out of memory quickly and uniformly.

The MMU keeps track of the logical and virtual addresses requested by the CPU. To do this, it uses page and pointer tables that are stored in main memory. These tables, which surprisingly do not require large amounts of memory, contain pointers indicating where to go in physical memory. An entire 16M bytes of virtual memory will use only one 1024-byte page table with 256 pointer tables of 512 bytes each, for a total of 132,096 bytes devoted to address mapping.

Although dynamic address translation looks complicated, it is quite simple to understand. For example, to keep track of a byte of data referenced by a logical or virtual address, but actually stored in a physical address, the MMU uses the 8 most significant bits of the 24-bit virtual address to locate 1 of the 256 32-bit entries of the page table. The MMU knows where the page table is kept in main memory through one of its two page table registers.

The contents of this page table entry (PTE), in turn, point to the start of 1 of 256 different pointer tables, each of which contains 128 (32-bit) entries. Once the pointer table has been located, the 7 next significant bits of the virtual address locate one of the entries, which contains the actual page number of the memory location. Once the physical address of the page containing the data has been located, the MMU translates the location (offset) of the data within the page directly from the 9 least significant bits of the virtual address.

A look at some of the details of a PTE will illustrate just how much usable information is included (Fig 3). In addition to the 16 bits devoted to the page frame number (the high order 16 bits of a physical page address), there is a valid (V) bit that, when set, indicates that the corresponding page is resident in physical memory. When the V bit is

![Image](https://via.placeholder.com/150)
RCI's Trapix Series of Real-Time Image Processing Systems are in use in industry, government, research and teaching institutions throughout the world.

The Trapix's efficient design and extensive use of the latest semiconductor devices, including 64K RAMS, dramatically reduces costs. For the OEM system builder, the modular design enables the configuration to be tailored to your applications. For the end user, a complete turnkey processing system is available including internal LSI 11/23* computer, 256KB program memory and 30MB Winchester Disk. In addition, RTIPS*, the powerful new image processing software package designed specifically for the Trapix, allows you to process your images immediately.

Whether your application requires signal processing of nuclear or radiological medical images, real-time edge detection and pattern recognition, processing of infrared data from video tape, or general purpose image enhancement and display, the Trapix can handle it.

- Up to 4MB of image memory
- Unique 16 bit video speed Pipeline Image Processor
- Real-time histogram calculator, pixel counter and pixel locator
- Vector generator with a 32 bit microprocessor and user loadable instruction memory providing near real-time pixel processing
- Very low noise and stable 8 bit or 10 bit video digitizers with programmable gain and offset
- 1Kx1K progressive scan acquisition and processing at 7.5 frames per second
- Internal time base correction for direct operation with video tape recorders
- Remarkably small size, modular design and low cost make the Trapix an outstanding value for OEM and end user applications

For information about today's cost effective solution to your image processing needs, contact Recognition Concepts, Inc. Write to us on your company letterhead to receive a video taped Trapix/RTIPS demonstration.

*LSI/11 is a registered trademark of Digital Equipment Corp.
*RTIPS is a registered trademark of TAU Corp.

RECOGNITION CONCEPTS, INC.
924 Incline Way, P.O. Box 8510, Incline Village, Nevada 89450 (702) 831-0473 Telex: 170058
INNOVATORS IN IMAGE PROCESSING
See us at SIGGRAPH, Booth #148
CIRCLE 93
Fig 3 Any of 16,777,216 bytes of dynamic address translation of the NS16000 family can be located in physical memory by just selecting a PTE (8 bits), which references a pointer table (7 bits), which in turn points to the 512-byte page in physical memory. The byte location referenced within that page corresponds to the offset in the original logical address. Shaded areas indicate memory areas available for PTE expansion in larger systems.

cleared, any attempted reference to the page will cause the MMU to abort the reference. This, of course, is followed by location of the page on disk and a page swapping algorithm. The PTE also contains 2 protection level bits that control user access to pages. Divided between user and supervisor modes, these 2 bits can allow read-only, full-access, or no-access levels of accessibility.

Finally, a modified (M) bit indicates when the page mapped has been modified and whether a page needs to be written to mass storage when it is de-allocated from physical memory. A referenced (R) bit indicates when a page has been referenced. It is tested and cleared periodically by the operating system in order to compile frequency of reference statistics for each page currently in memory. This information is then used to determine the least frequently used pages when swapping in new pages from main memory. It is interesting to observe that the availability of unused portions of the PTE (shaded sections of Fig 3) permits the future expansion of the MMU to include both greater mapping space and conditional references.

Onchip cache

When a virtual (logical) address is passed from the CPU to the MMU, the MMU first attempts to match it with a special associative cache contained on the chip. This cache contains the 32 most recently accessed virtual addresses (15 bits) as well as their translated physical addresses (16 bits).

If the address requested by the CPU matches 1 of the 32 cache entries, the CPU is allowed access to the physical address immediately. This virtual to physical address translation takes only one clock cycle. Since the associative cache memory located directly on the CPU contains 32 of a possible 512 page address entries, it is easy to see how a logical to physical address translation happens so fast (Fig 4). Each cache entry contains not only the physical address of the information sought, but an associated protection level encoded in 2 bits. If the requested address is not present in the cache, however, the MMU must fetch both page and pointer table entries from memory before address translation can be performed. This can take up to 30 clock cycles.
Sprague Electric’s new Brochure WR-189 provides the basic facts on interface ICs for current-sourcing. These drivers excel in interfacing low-level logic (TTL, CMOS, NMOS, PMOS) and high-current or high-voltage relays, solenoids, lamps, motors, and displays. For your copy of informative Brochure WR-189, write to Sprague Electric Co., Technical Literature Service, 555 Marshall St., North Adams, Mass. 01247.
Although transparent to the user, the MMU associative cache has proven to be a powerful tool for hastening processing speeds. It has been calculated that a CPU entry will be present in the cache about 97% of the time. Such a hit ratio means that 97% of all references will take only one clock cycle.

If the next instruction address is not contained in the cache, the MMU must obtain the required entry address directly from the physical memory page table. In order to do this, the MMU floats the CPU bus by activating its Not Float (NFLT) signal, which turns over bus control to the MMU. The MMU, following a replacement algorithm already programmed in the hardware and transparent to the user, also updates the associative cache with this latest entry. Although the replacement algorithm causes the least recently used mappings to be replaced with the most recent ones, the MMU will fill an empty spot that appears in the cache before replacing an item in the cache.

It normally requires up to 20 clock cycles or 2 µs to fetch the PTE from main memory. Then, whether the page containing the required information is resident in main memory or on disk is determined. If it is in main memory, the CPU is released to access the data. If the page is resident on disk, however, the page must be swapped into main memory before the data are available for CPU access.

The benefits of the described memory page swapping methods are many. Moreover, with the advent of low cost disk memory storage, NS16032 CPU and NS16082 MMU users now have, with the virtual memory system, the cost advantages of a computer that has a minimal amount of expensive main memory. This system also has the large memory space formerly associated only with large mainframe computer systems. In fact, this system not only provides a less expensive way of obtaining large memory address, but an easier way of implementing it. Typical applications include intelligent terminals, workstations, business and personal computers, integrated office systems, graphics, telecommunications, and industrial and process control. Other applications include high performance games, computer aided design/computer aided manufacturing, synthesis, artificial intelligence systems, and radiation-hardened/high speed military systems.
Welcome the newest member of the Panasonic non-impact printer family.

Meet the EUY-3T, the new Panasonic Non-Impact Printer that’s minimal in size but not in capability. It prints 40 alphanumeric characters on 80mm paper. Offers thermal printer performance with dot addressable graphics capability. And low power requirements (just 5V/2.5A) make it very economical to operate.

It’s the latest addition to a line of electro-sensitive and thermal printers famous for being big in reliability, but small where it counts: in size, in cost and in operating noise.

All Panasonic Non-Impact Printers have low all-DC power requirements. And our microprocessor interface modules accept 8-bit Parallel or byte Serial data input (model 3T is also Centronics-compatible). So they’re perfect for ATE, printing calculators or other designs requiring low-cost hard copy.

Think our new baby is cute? Ask for complete data and prices—contact Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-8080.

At 14 ozs., it’s positively precocious.

<table>
<thead>
<tr>
<th>Series</th>
<th>Column Capacity</th>
<th>Paper Width</th>
<th>Outside Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>EUY-2</td>
<td>15</td>
<td>36mm</td>
<td>71.9 x 33.5 x 55.9 mm</td>
</tr>
<tr>
<td>EUY-3T*</td>
<td>40</td>
<td>80mm</td>
<td>121 x 48.5 x 67 mm</td>
</tr>
<tr>
<td>EUY-10</td>
<td>15, 21, 32, 40</td>
<td>60mm</td>
<td>90.4 x 42.4 x 110 mm</td>
</tr>
<tr>
<td>EUY-5</td>
<td>32, 40, 64, 80</td>
<td>127mm</td>
<td>195 x 65 x 70.1 mm</td>
</tr>
</tbody>
</table>

*Thermal only

Panasonic
Industrial Company

CIRCLE 95
NOW—SUPER-PERFORMING 5¼" WINCHESTERS WITH BUILT-IN RELIABILITY.

UNIQUE SHOCK-MOUNTED BASE deck assembly isolates heads and media from external vibration. Automatic actuator restraint and manual shipping lock prevent head movement during shipment.

VERTICAL OR HORIZONTAL MOUNTING in the same space as a 5-1/4" FDD permits easy integration into FDD-based systems.

TWO INTERFACE OPTIONS: 4.84 MHz (NRZ I/O data) or 5.0 MHz (MFM I/O data, compatible to ST506/ST412). The transfer rates permit WREN to be matched with off-the-shelf controllers for easy systems integration.

ROTARY VOICE COIL ACTUATOR provides 45-millisecond average access time including head settling.

NEW 45 mSec AVERAGE SEEK TIME.

THE WREN™

The Model 9415 WREN disk drive gives you a host of value-added features. From microcomputer and LSI control logic to special-formula media, high technology has finally delivered a 5-1/4" Winchester with more reliability.

Compare for yourself. Call your local Arrow or Kierulf distributor today. Or write: OEM Product Sales, HQN08H, Control Data Corporation, P.O. Box 0, Minneapolis, MN 55440.
FIFO—THE GLUE HOLDING SYSTEMS TOGETHER

Dual-port, high density FIFOs are playing a greater role in interconnection. The latest generation offers HCMOS compatibility as well as onboard SRAM and independent access.

by Ching-Lin Jiang and Michael Bolan

Primarily because of the introduction of the microprocessor, computing power costs are now so low that the connections can cost more than the computers themselves. To lower these costs and to simplify rate buffer applications, first in, first outs are often used as connecting tools. But, they have been relegated to low bit density, they have expansion difficulties, and they do not have the advantages of high performance complementary metal oxide semiconductors, all of which impair their usefulness as connecting tools.

There are, however, a number of dual-port memories that are configurable with Mostek's BiPORT™ cell. One such compatible memory is the MK4501 first in, first out (FIFO), which will also carry an MK68000 family designation, MK68345. Its development is significant in that it makes possible innovative applications for memories as connector devices, particularly because it provides improved methods for interconnecting systems.

Most system designers are familiar with the use of memories as video buffers, disk buffers, and printer buffers. Historically, static random access memories (SRAMs) have been used to implement the buffer function. These examples, however, are all dual port in nature, and the use of a single RAM to implement them significantly increases system design complexity. It is now possible to configure dual-port memories in a variety of ways to meet specific application needs.

Interconnect problems and approaches

Today's system designers face a bewildering number of interconnect problems. Transporting data across a time boundary and providing the necessary elasticity (buffering) for different data rates are the two
Avoiding this problem is fundamental to reliable system operation. Arbitration minimizes, but does not eliminate, the possibility of synchronization error. The essence of this technique is to narrow the time window of sensitivity—i.e., speed up the clocks—until the probability of timing collisions is insignificant in a given application. The window of sensitivity is equal to the few nanoseconds of setup time, plus the hold time. If the clock rate is very slow—one or fewer events per hour—the possibility of a problem becomes extremely remote. However, as the clock rate is increased, the problem becomes more acute. In practical circuit design, parameters such as high transistor gain, short propagation delay, and multiple strobes can narrow the window. Even when careful attention is given to circuit design, circuit performance verification can be so difficult as to limit the usefulness of this technique.

Handshaking is another common method of transporting data across a time boundary. Data transfers are constrained to follow a strict protocol of request, acknowledge, and transmit. The biggest disadvantage is the hardware overhead needed to generate the handshake signals and the time needed for synchronization. When used in computer systems, this approach often results in substantial software overhead, with correspondingly slower execution times.

Another technique involves the use of a dual-port memory. An essential requirement is that the hardware be able to support simultaneous writes in Port X while Port Y is reading. The development of such a memory cell in high performance complementary metal oxide semiconductors (HCMOSs) is important because it can also help simplify subsystem interconnection.

The Table shows the variations possible for a dual-port memory. Although the BiPORT cell allows asynchronous reads and writes in either port

| Port Variations |
|------------------|------------------|
| Port X           | Port Y           |
| Write only       | Write only       |
| Read only        | Read only        |
| Read/write       | Read/write       |
| Sequential       | Sequential       |
| Random           | Random           |
| Serial           | Serial           |
| Parallel         | Parallel         |
| Synchronous      | Synchronous      |
| Asynchronous     | Asynchronous     |
The OEM’s Choice for Multibus* Quality and Reliability

NEW 512K Memory Boards

128K-512K Dynamic RAM with EDC
Error detection/correction (EDC), high speed and increased noise immunity are standard features that give you a number of user options with this versatile new board. Completely Multibus compatible, this board allows you to add 128K, 256K, 384K or 512K of RAM to any 8- or 16-bit system without making changes. It decodes the full 24-bit address bus for a system-wide memory of 16 megabytes and runs at a fast read access time of 275ns. EDC corrects all single-bit errors without processor intervention. It also flags double-bit errors, generating an interrupt so input ports can be read to determine which RAM chip failed. Or, you can strap the board to interrupt on any error. And noise won’t bother this board, either — its five-layer construction incorporates power and ground into the two internal layers. High reliability sockets with integral by-pass capacitors further minimize noise.

128K-512K Parity Only Dynamic RAM Board
This new board delivers all the quality features of the 128K-512K EDC Dynamic RAM Board except that parity detection is used rather than error correction. The parity circuitry will detect any single-bit errors, optionally generating an interrupt so the CPU can determine which row of RAMs had the error. Four easy to read LED’s on the top of the board show the check condition, allowing fast replacement in the event of a failure. Writing to the corresponding output port clears the parity error. Completely Multibus compatible, the board runs at a rapid 245ns access time. And here’s some refreshing news about wait states — the on-board arbitration circuitry cuts down on wait states caused by refresh cycles. You also get hidden refresh — if the processor accesses another board in the system at any time between refresh cycles, a new refresh cycle is initiated to overlap the memory cycle on the other board.

OEM quantities and pricing are available on these and on Central Data’s complete line of Multibus boards. For more information call or write.

* Multibus is a trademark of Intel Corporation. Prices shown are quantity 100, 512K RAM.
Because bits are usually part of a larger unit (a)—a byte or a data set—the integrity of the data can be jeopardized if a simultaneous write or a simultaneous read/write is attempted (b).

on the same cell, data bits in a system are normally interdependent. Sets of bits make up a byte, sets of bytes make up a data base [Fig 2(a)]. Often these set relationships must be preserved. Fig 2(b) shows the conditions under which the integrity of the set is in jeopardy. Because bits are normally not independent entities, but have a set relationship, a more significant accomplishment is moving a set of data bits (a byte or word) across a time boundary while maintaining its integrity. One implementation in the BiPORT series is a device following FIFO rules. This device allows simultaneous writes and reads, but not at the same location, thereby maintaining integrity of the set. A FIFO can therefore be used to avoid synchronization problems.

Data rate disparity between the sending and receiving subsystem is another difficulty that system designers face. To overcome this, data must be allowed to accumulate or to be buffered. The SRAMs that have been used for this purpose have two distinct drawbacks: the circuitry needed to generate address information and a need for the overhead circuitry to create separate input and output ports. The buffer space required is a function of the rate disparity: the greater the disparity, the larger the buffer must be. The MK4501's main application is as a rate buffer capable of absorbing and sourcing data being transmitted at different clock rates, such as interfacing fast processors to slow peripherals.

Because rate buffer applications are often concerned with overflow and underflow conditions, FIFO full and empty flags are provided to prevent such conditions. Ideally, a FIFO should be large enough that full and empty flags are rarely generated, so that the direct attention of the sender and receiver is not needed, and data transfer can proceed automatically. If the sender or receiver must spend much time dealing with overflow and underflow, little time is left for more important tasks. When interruptions for full and empty flags reach an extreme, the subsystem begins to thrash, allowing no time for useful work. For this reason, the low bit density of previously available FIFOs has limited their usefulness.

Architecture and bipolar circuit limitations also restrained earlier FIFO approaches. The most popular devices resemble shift registers in which data are dumped in one end and fall out the other, after propagating through the entire depth of storage. A consequence of this approach is a rather long fall-through delay, which exhibits itself as a delay between the time data are written and the time data can be read. As the FIFO depth increases, this delay also increases, making expansion awkward.

Bipolar devices are inherently larger than the equivalent complementary metal oxide semiconductor (CMOS) devices, permitting fewer gates on a chip of a given size, and requiring significantly more power to operate. For this reason, FIFOs have been available only at low bit density and high power dissipation.

A high density monolithic FIFO
The MK4501 is the highest density monolithic FIFO available. The package pinout is given in Fig 3 with pin functions and performance characteristics listed in the accompanying key. This pinout is designed to serve many generations of higher density FIFOs. A key feature of this memory, its 8-element BiPORT

![Fig 2](http://example.com/fig2.png)

![Fig 3](http://example.com/fig3.png)
From Raymond Engineering.
The better back-ups.

For accuracy, simplicity and reliability, you can't beat the Winchester Repeater™ series of cassette back-up drives. Introducing the 10 mbyte WR-100 and the 20 mbyte WR-1000 Winchester Repeaters. The intelligent solutions to the 5¼'' Winchester disk back-up dilemma. Offering superior data reliability and cost-effectiveness in the 5¼'' disk footprint. For more information, contact Raymond Engineering Inc., Raycorder Products Division, 217 Smith Street, Middletown, CT 06457. (203) 632-1000.
RAM cell (Fig 4), consists of a SRAM cell augmented with an additional set of access transistors and bit lines. The cell size is 40 \( \mu \text{m} \times 50 \mu \text{m} \). A clear advantage of a memory array formed by these cells is that it can be read and written independently, from two separate ports. An efficient FIFO can be constructed using this dual-port array supported by the appropriate addressing schemes and status logic circuitry.

The 512 x 9 FIFO memory chip consists of four building blocks [Fig 5(a)]. The memory function block includes the matrix, the read/write control logic, and the location pointers. The flag generation block uses counters and comparators to create empty and full status flags. The expansion logic block provides the input and output control signals to expand the depth of the FIFO, while the reset block generates commands to reset all FIFO operations.

The memory matrix is organized into 128 rows and 72 columns, split into two halves, made up of dual-port RAM cells. Read pointers address the 128 read word lines that are in the center of the chip. Two identical sets of write pointers are placed at the right and left sides of the matrix for the corresponding 128 write word lines. Two 4-bit column pointers are used to access the bit lines for the read and write operations. The pointers consist of CMOS shift registers.

The MK4501 operation depicted in Fig 5(b) uses two independent pointer rings to address the BiPORT memory array. Using shift registers only in the pointer rings and BiPORT RAM cells as storage elements provides efficient usage of silicon real estate, resulting in very high density monolithic FIFOs.

To begin MK4501 operation, a reset command is sent into the device by drawing the RS input low. During the reset, both the internal read and write pointers are set to zero (Wo, Ro), and an empty flag is internally generated to inhibit any read functions.

This FIFO initiates a write cycle on the falling edge of the write enable control input (W) provided that the full flag (FF) is not set. Data setup and hold time requirements must be satisfied with respect to the rising edge of W. The data are stored sequentially and independent of any ongoing read operations. To prevent a data overflow condition, the FF will go low whenever the internal write pointer catches up with the read pointer, and further write operations will be inhibited. Upon completion of a valid read operation, the FF will go high and a valid write can begin.

Similarly, the device initiates a read cycle on the falling edge of the read enable control input (R) provided that the empty flag (EF) is not set. In the read mode, it provides fast access to data from 9 of 4608 locations in the static storage array. The data are accessed on a FIFO basis independent of any ongoing write operations. After \( R \) goes high, the data outputs will return to a high impedance condition until the next read operation. In the event that all data have been read from the FIFO, the EF will go low and further read operations will be inhibited: the data outputs will remain in high
As you can't see, the terminal on the left has a low-cost Rockwell R24DC modem built in. It's connected directly to the U.S. dial-up network with nothing more than a standard telephone jack. No acoustic coupler. No phone. No tangled wires.

It's easy to connect the R24DC modem inside your terminal. It's LSI-based, with the entire 2400 bps modem and data access arrangement on a single 5"x 7.85" plug-in card. With power requirements of ±12V and +5V, it consumes only 3 watts.

Rockwell's R24DC integral modems are FCC-registered and both Bell- and CCITT-compatible. And they're widely used in point-of-sale terminals, and for cleaning up PBXs, data concentrators and data communications devices.

To get the inside story on Rockwell modems, call the Electronic Devices Division, Rockwell International at (800) 854-8099.

In California, call (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, California 92660.
impedance. Upon completion of a valid write operation, the EF will go high, and a valid read can begin. The maximum latency can be just one cycle time. Fig 5(c) shows the timing diagrams of the previously described read/write operations.

This FIFO’s word width can be expanded beyond 9 bits simply by connecting the corresponding input control signals of multiple devices. Any one device can detect status flags (EF and FF). Fig 6(a) demonstrates a method of implementing an 18-bit byte width by using two MK4501s. Any byte width can be attained by adding devices.

The basic pointer ring architecture shown in Fig 5(b) provides an easy means to expand the FIFO depth to greater than 512 bytes. Basically, the rings of the individual devices can be externally connected through the expansion in (XI) and expansion out (XO) signals to form an arbitrarily large ring of pointers in a multiple-device FIFO system. Fig 6(b) demonstrates depth expansion using three MK4501s. Any depth can be attained by adding more devices. This FIFO operates in the depth expansion configuration when certain conditions are met.

The first device must be designated by grounding its first load control input (FL), and all other devices must have FL in the high state. The expansion out (XO) pin of each device must be tied to the expansion in (XI) pin of the next device. External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all EFs and the ORing of all FFs—i.e., all must be set to generate the correct composite FF or EF [Fig 6(b)].

One additional feature of this device is the retransmit capability for systems having data writes less than 512 bytes between resets. The FIFO can be made to retransmit data when the retransmit enable control input (RT) is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. R and W must be inactive during retransmit. It should be emphasized that this retransmit feature is not compatible with the depth expansion previously described where the same pin is used to designate the first active device in a ring of FIFOs.

**FIFO solves rate buffering problems**

An application of the MK4501 to the Harris Corp’s Mind™ series of distributed data processing systems is a good example of how to solve rate buffering problems. This application involves connecting a disk controller to a memory system through a direct memory access (DMA) controller. If the data rate coming from the DMA controller can exceed disk capability, the data rate from the disk controller can vary by ±2%.

Using several MK4501s for rate buffer memory eliminates timing problems and smooths the data transfer. This application involves a 16-bit data bus. As a result, two FIFOs are required to implement the data bus. (The parity bits are not required in this application.) The data bus must also be bidirectional, and because this FIFO is designed to pass data in only one direction, a total of four is required to meet the bidirectional need.

Moreover, the application requires that entire sectors be read or written at a time. Because a sector length is 128 bytes, the 512-byte depth of the MK4501s is more than adequate to meet the requirement. If a read-from-disk operation is desired, the processor gives the disk controller the appropriate commands. The disk controller responds by writing data to the read-data FIFOs. After the first byte in a sector has been written, the empty flag goes to the inactive state (EF = VOH), which signals the DMA circuitry to start reading data. Data are continuously transferred from the disk through the DMA to memory until the processor terminates transfer from the disk controller. The DMA can
move data faster than the disk controller can, but the full flag of the read data FIFO is connected to the interrupt network of the processor, should an error or overrun condition occur.

If a write-to-disk operation is desired, the processor circuitry gives the DMA the appropriate commands. The full flag from the write-data FIFOs is used to tell the DMA that the FIFOs are not full and data transmission can occur (FF = VOH). The DMA will then write data to the FIFO buffers in an attempt to completely fill them. When the buffers are full, the full flag changes state (FF = VOL), terminating the DMA request. The MK4501 will then generate a full flag prior to completing the last write cycle that causes the buffers to be full. This gives the DMA time to recognize that the DMA request has been terminated prior to doing another write cycle. Transfer from the FIFO to the disk is accomplished by the disk controller under the direction of the processor.

Software is designed so that an underrun condition, FIFO empty, should not occur. However, the empty flag of the write-data FIFO is connected to the interrupt network of the processor, should an error or underrun condition occur. The R and W signals are generated by the appropriate control device (disk controller and DMA) and conditioned with timing signals. Only a minimum of interface

logic is required to use the MK4501. The tri-state buffers of the FIFO allow direct connection to the processor and disk controller bus, eliminating the need for multiple bus transceivers.

Future products using the BiPORT cell will also encompass shared storage for tightly coupled processors. More advanced rate buffers are also under development to further increase FIFO bit density and performance.

References
RESOLVED
... the difference
in color graphics displays

When you need better convergence, linearity and color purity across the screen and from edge to edge, then you need SRL's advanced-performance Model 2106 In-Line Color Display.

The Model 2106 offers you a 100 MHz ultra-high bandwidth. You get consistent brightness of narrow horizontal and vertical grid lines.

Factory convergence never deteriorates. No pots to adjust...no buttons to push. You get superb convergence, all the time.

You don't need to buy several monitors or make circuit changes to satisfy your multiple line/frame rate needs. Simply select one of 16 ranges with our unique Select-a-Rate.

And we offer you even more benefits at no extra cost: differential video inputs, separate horizontal and vertical drive inputs, an adjustable bezel that allows you to insert anti-glare filters, and the custom engineering services you need to solve your specific configuration and source signals.

Our 19-inch model features 1280x1024 resolvable triads (0.31 mm spacing), while our 13-inch model has 1024x768 or 1280x1024 resolvable triads (0.31 mm and 0.21 spacing).

Compare the Model 2106's features and benefits...review our specifications and find out why our color displays resolve the difference in color graphics displays. Contact us today for more information.

Now available...64kHz horizontal frequency at 36kHz prices.
NO WAITING—EEPROM AT WORK

In addition to allowing TTL level *in situ* programming, today's EEPROMs write and erase without delaying their host microprocessor.

by Kendall W. Pope

As control, monitoring, and portable or remote data gathering applications become commonplace, the designers of such systems often find themselves between a rock and a hard place. At issue is memory. The choice facing designers has traditionally been whether to use random access memory or read only memory for storing small amounts of program code and data.

Random access memory (RAM) is attractive because it makes the inevitable debugging and altering of programs infinitely easier. Its main drawback, however, is its susceptibility to the loss of information during a power failure. Although battery systems alleviate this problem, the solution is a real-estate and cost-intensive one.

Read only memory (ROM), on the other hand, is immune to the volatile frailties of RAM and requires no external power or refresh mechanism. Unfortunately, the very nonvolatility that makes ROM attractive also limits its flexibility in many applications. Code resident in ROM (including programmable ROM and ultraviolet erasable programmable ROM) is difficult to alter. At the very least, chips must be removed from circuits, erased, reprogrammed, and then reinstalled. This is a time-consuming, cumbersome and—in some applications—an impossible procedure.

It seems, then, that there is a need for a nonvolatile memory chip that can be programmed and reprogrammed *in situ*. Such a chip must also allow programming to take place quickly (in 1 s) to be of any practical value. Other desirable features might include the ability to reprogram individual words stored within the chip as well as an architecture that facilitates easy interfacing with other circuit components.

Enter the latest generation of electrically erasable programmable ROMs (EEPROMs). The basic cell of the EEPROM is a floating gate transistor (Fig 1) in which the threshold voltage can be changed by the application or removal of a charge on the floating gate. The EEPROM is constructed from a number of these cells by completely surrounding each polysilicon floating gate with a silicon dioxide layer. Because less than 10% of a charge placed on the floating gate leaks away in 10 years, EEPROMs provide nonvolatility. The EEPROM uses a thin oxide layer to pass electrons to and from the floating gate, thus facilitating cell programming.

Kendall W. Pope is an applications engineer at Synertek, 3001 Stender Way, Santa Clara, CA 95051, where he is responsible for all memory products. He holds a BSEE from California Polytechnic State University at San Luis Obispo.
Fig 1 The floating gate transistor memory cell threshold voltage responds to a charge placed on the floating gate. The cell is fully static, yet it can be reprogrammed if a charge is applied sufficient to initiate Fowler-Nordheim tunneling through the dielectric layer (tunnel oxide).

An EEPROM's physical mechanism of programming is known as Fowler-Nordheim tunneling. This occurs when an electrical field is applied across a thin silicon dioxide insulator. As the electric field approaches 10 MV/cm, electrons penetrate the silicon dioxide layer and tunneling begins.

The tunneling mechanism is bidirectional, thus allowing each gate to be charged as well as discharged. If the insulator is less than 200 Å thick, programming levels of approximately 20 Vdc are possible. In this case, an onchip charge pump is used to generate voltage levels adequate for programming from 5-Vdc sources. The onchip charge pump eliminates the need for externally generated, high voltage programming pulses and associated pulse-shaping circuitry.

A charge pump is a relatively straightforward circuit and works as follows. The erase/write voltage \( V_{pp} \) is generated internally and limited by a shunt regulator. This mechanism appears in Fig 2(a). An additional shunt is used to clamp \( V_{pp} \) to \( V_{cc} \) when the cell is not erasing or writing. This clamp is released once for each individual erase or program operation, producing a \( V_{pp} \) pulse that swings between 5 and 20 Vdc [Fig 2(b)]. The leading edge of this pulse is ramped by a rise time control circuit in order to prevent damage to the memory transistor's tunnel dielectric.

The voltage multiplier, or charge pump, depicted in Fig 3 operates in a manner similar to the technique used to raise a metal oxide semiconductor transistor's gate voltage above the supply level. Coupling capacitors \( C_1 \) to \( C_{n-1} \) are driven by internally generated clocks (\( f \), \( \bar{f} \)) and pump packets of charge along the diode chain \( D_1 \) to \( D_m \). Because the nodes between diodes are not discharged, the average potential (\( V_1 \) to \( V_m \)) increases progressively from input to output along the diode chain. In the configuration depicted in Fig 3, the voltage that results at the output of the diode chain is more than sufficient for EEPROM cell programming.

The combination of Fowler-Nordheim tunneling and an onchip charge pump allows 20-Vdc programming levels to be generated from 5-Vdc supplies. As a result, a compact package of nonvolatile, yet easily alterable, memory can be fabricated.

Extending EEPROM capability
A producer of EEPROM devices, Synertek uses charge pump techniques in its SY2801A memory chip. This fully static chip allows TTL level programming to take place in 10 ms and is packaged in standard 16-pin, dual-inline format. Unfortunately, for many applications, this chip's 20-ms erase/write cycle is too slow. In these situations, it is often necessary to latch incoming data with

Fig 2 Erase/write voltage is generated from TTL levels onchip (a) and limited by shunt regulators. The 20-Vdc pulse waveforms (b) that result are more than adequate to write to and clear memory cells.

Fig 3 An onchip charge pump circuit uses a succession of capacitors and diodes to raise TTL-input voltage levels to a value sufficient for EEPROM programming.
# 256K CMOS RAM

Better Performance than Bubble - at a Comparable Price

Compare these Key Features:

<table>
<thead>
<tr>
<th>Feature</th>
<th>INTEL ISBC 254 - 2A BUBBLE MEMORY BOARD</th>
<th>DTI CBC 256 CMOS STATIC RAM BOARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus</td>
<td>Multibus</td>
<td>Multibus</td>
</tr>
<tr>
<td>Memory Size</td>
<td>256K bytes</td>
<td>256K bytes</td>
</tr>
<tr>
<td>Operating Voltages</td>
<td>5V, 12V</td>
<td>5V</td>
</tr>
<tr>
<td>Operating Currents</td>
<td>3.0A, 1.4A (max.)</td>
<td>100mA (max.)</td>
</tr>
<tr>
<td>Cycle Time</td>
<td>48 milliseconds avg.</td>
<td>500 nanoseconds typ.</td>
</tr>
<tr>
<td>Card Slots Required</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0°C-55°C</td>
<td>0°C-70°C</td>
</tr>
</tbody>
</table>

**ADDITIONAL FEATURES OF DTI'S CBC 256 INCLUDE:**
- All - CMOS technology.
- Flexible addressing: 16 bit with paging or 20 bit contiguous (24 bit available Aug. '83)
- 8 or 16 bit data words.
- 3-year data retention time.
- 256K, 128K, 64K, 48K, 32K and 16K byte versions.

For more information regarding the CBC 256K CMOS Ram board, or any of our other all-CMOS Multibus boards, call or write Bill Long, CBC Product Manager at (601) 856-4121.

Multibus and ISBC are trademarks of Intel Corp. Above specifications taken from manufacturers current published data.

CIRCLE 102
external circuitry. This latching complicates interfacing EEPROMs with the rest of the circuit elements and often requires more circuit board real estate than can be justified.

To alleviate these problems, the company developed the SY2802E chip (Fig 4). This EEPROM incorporates all the onchip logic necessary to allow it to function as a 256- x 8-bit nonvolatile memory register file. Featuring a general purpose, bus-oriented interface, this chip is well suited for use with most microprocessors. Included in its architecture are an 8-bit data latch, a status register, and timing and control circuitry. Because of the chip's data latch circuitry, a microprocessor does not have to wait for it to complete an erase/write cycle. In fact, the processor can go about its business without regard for any EEPROM activity.

Essentially, the chip serves as a small lookup table for a microprocessor. Its main focus is actually not software storage, but rather, the storage of data such as calibration constants. Thus, the main problems that the SY2802E addresses are in timing and control areas. Because the chip has a full set of onboard control logic—plus control signals for the microprocessor to work with—it does not need a traditional architecture of its own. As a result, the device looks like an input/output (I/O) location rather than an area of memory, resulting in several benefits when the chip is used with I/O oriented microcomputers.

To interface externally, the SY2802E ties into a data bus and data port. All operations can be port oriented and internally controlled. No longer is the designer limited to a BUSY signal coming from an EEPROM. Now, because access to a status register is available, processors that cannot be interrupted can be used. In addition to a 3-state bidirectional 8-bit data port, this EEPROM has conventional chip select (CS), register select (RS), read/write (R/W), and strobe (STRB) inputs. For external wait state or polling operation, a chip clear/store (CLR) cycle status flag—BUSY—is available.

The SY2802E also has seven modes of operation. (See the Table.) The reading mode requires two cycles. First, the address is loaded into the 8-bit address pointer, and, second, the data from the selected location are read. Both the address and data are transmitted through the same 8-bit port, and 8-bit address data are relevant only to internal locations.

The writing mode also requires two cycles. As with the read cycle, the address pointer is loaded first. Then, by loading the data input register, the byte erase/write operation is initiated. Therefore, during the byte erase/write operation, the microprocessor is free to perform other tasks. Both the BUSY bit and bit 7 of the status register are set

<table>
<thead>
<tr>
<th>Operational Modes</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td>CS</td>
</tr>
<tr>
<td>Read Register File</td>
<td>0</td>
</tr>
<tr>
<td>Read Status Register</td>
<td>0</td>
</tr>
<tr>
<td>Write Address Pointer</td>
<td>0</td>
</tr>
<tr>
<td>Write Data in Latch</td>
<td>0</td>
</tr>
<tr>
<td>Deselected</td>
<td>1</td>
</tr>
<tr>
<td>Write Inhibited</td>
<td>0</td>
</tr>
<tr>
<td>Block Clear</td>
<td>0</td>
</tr>
</tbody>
</table>

x = Don't Care  
\( \uparrow \) = Positive Transition  
\( \downarrow \) = Negative Pulse
And dust. And dirt. And heat. And vibration. All the elements that can cause a disk drive to turn sour.

But thanks to a fresh idea from MPC Peripherals, Apples® can now run in the most demanding environments.

With BUBDISK™, a MPC memory module more rugged than a disk drive. More versatile than a RAM card.

A board that uses an Intel 7110 bubble.

The 7110 gives BUBDISK a full megabit of solid-state memory. As well as three times the data access speed of a floppy. Over 1000 times the data integrity of tapes or disks. Plus a 10-year MTBF. Assuring that BUBDISK will smoothly work in environments where other types of mass storage have trouble operating at all.

Because the Intel 7110 bubble is non-volatile, MPC's BUBDISK retains its memory through power failures and power surges. Or when you simply turn the Apple off.

And BUBDISK makes Apples portable as well as durable, because it doesn't require battery back-up. Allowing Apples to operate just about anywhere, for any application. From truck stops to oil rigs. Grain elevators to highway maintenance.

So remember. If reliable memory is going to make or break your design, protect it with Intel bubbles.

Call Intel, toll-free. (800) 538-1876. In California, (800) 672-1833. Or write Intel Corporation, Lit. Dept. #Y-2, 3065 Bowers Avenue, Santa Clara, California, 95051.

MPC delivers solutions

Apple is a registered trademark of Apple Computer Inc. BUBDISK is a trademark of MPC Peripherals Corp.
In this microcontroller configuration, Port 1 (P10 to P17) is byte configured as an 8-bit data I/O port and handles address and data. Port 2 (P20 to P22) is bit configured and handles register select (RS), chip select (CS), and BUSY signals.

During the erase/write operation. During this operation, only the status register is accessible. Depending on the circumstances, the microprocessor can interact in one of the following methods:

- Processor is held in wait states until BUSY inactive
- Processor is in a tight program loop using status register read and branch on minus (bit 7)
- Processor works on other tasks, periodically polling the status register (bit 7)
- Processor uses the trailing edge of the BUSY signal to activate an edge triggered interrupt

In addition, the SY2802E can be block cleared to all zeros. As with data store, the clear cycle need only be initiated. All the timing is controlled internally, and BUSY and status (bit 7) become active. Again, during the clear cycle, only the status register is available.

One of the most distinguishing characteristics of EEPROMs is that the number of erase/write cycles is limited. As the voltage level between the on state (logic 1) and the off state (logic 0) decreases, it becomes hard for the sense amplifiers to recognize which state is represented. Synertek designs its EEPROMs to meet a minimum of $1 \times 10^4$ endurance cycles. Endurance is word independent, and adjacent words are unaffected during endurance cycling.

**Using EEPROMs effectively**

The SY2802E can be used in situations where the system's memory addressing space is used up. This is often the case in systems using a Z8 processor or the like. Here, all memory addressing space is usually quickly filled. Because the company's EEPROM acts and looks like a peripheral to the processor, no memory address space is needed (Fig 5). The address and data are passed from the microprocessor to the EEPROM as two consecutive 8-bit data transfers. Address is contained in the first, data in the second.

A more sophisticated application for this EEPROM is possible in data collection and manipulation settings. In surveying, for example, maps and charts are made from readings often taken under severe conditions. Generally, 128 readings are taken over a 2-acre site. To enable mapping, a computer based device must have the means to measure distance by focus as well as by angle of tilt. These values along with rotation allow a map to be drawn.

By sampling location information, a microprocessor based unit can calculate angle, distance, and rotation in seconds. To make this function fully automatic, a nonvolatile EEPROM, configured as a register file, can be used to store the readings. Once the data are safely stored, the field unit incorporating EEPROMs can be connected to a base unit that has a printer. A typographic printout can then be quickly generated.

In a hypothetical sequence of operation, the start button (reset) is pushed. Then, the lens is focused (or an autofocus lens is used). While the rotation is being stored, the microprocessor reads the distance sensor. As soon as the first storage sequence is complete, the distance is stored. While distance is being stored, the angle sensor is read, and the height from ground zero is calculated. When the distance storage is complete, the height is stored. As soon as the height is stored, the unit shuts everything off until the start (reset) is pushed again.

Because this 256 x 8 EEPROM can store 256 (8-bit) words, it is ideal for this application. This chip provides designers with an alternative to the standard RAM versus ROM choice. The chip's nonvolatility, ease and speed of programming, and in-circuit programmability make it perfect for use in any portable data gathering device. In addition, applications that place components beyond the designer's reach, such as military or space systems, can also benefit from the remote programmability of modern EEPROMs. It seems likely that as portable systems proliferate, so will the EEPROM.

**Acknowledgments**

The author would like to thank Bob Salter and John Turner for their contributions to this article.

---

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

<table>
<thead>
<tr>
<th>High 722</th>
<th>Average 723</th>
<th>Low 724</th>
</tr>
</thead>
</table>
THE
WINCHESTER
BACKUP
SYSTEM

Just plug it in your computer system. No additional hardware or software is needed. Transfer data to a 17.2 megabyte tape cartridge. Perform file search, update records, edit and reformat data. Use it for Winchester backup, data logging, or archival storage applications. Interfaces are built-in for RS-232, Multibus, S-100, 8-bit parallel, or Ohio Scientific. For full details on the Model 150 contact: North Atlantic Qantex, 60 Plant Avenue, Hauppauge, NY 11788 (516) 582-6060
GET THE POWER YOUR Q-BUS SYSTEM WAS DESIGNED TO GIVE

It's Plug-In Simple with Remarkable DEC-Compatible Technology from Andromeda Systems

The WDC11 Triple Function Compatible Controller: Its Power is Amazing Versatility

Interfaces with 8- and 5¼-inch Winchester and floppy disk drives, and includes an intelligent bootstrap ROM. This LSI-11 compatible Controller emulates these standard DEC devices: RK-05, RL-01/2, RP-02, RX02. That's only a sampling of the freedom of selection you have with the WDC11 Controller. It adds performance to your LSI-11 computer system. Easily and cost-effectively.

Winchester Add-On Subsystems: Their Power is Speed, Storage Capacity, Reliability, Compactness, and Low Cost

Get major throughput gains from your LSI-11 floppy-based system at a cost you can live with. Andromeda's popular MDS series, with a 5¼-inch Winchester drive, has a data transfer rate over eight times that of an RX02 floppy! Standard DEC emulations are available. Includes built-in bootstrap and formatting.

All Andromeda Winchester Subsystems will quickly and conveniently cover your mass storage needs for today and tomorrow.

Complete Turn-Key Computer Systems: Their Power is Big Overall Performance for Small Space and Cost

One totally integrated package includes computer and disk drives. For example, the 11/M1-W (pictured) holds a standard 5¼-inch Winchester disk drive, 2 x 5 card cage, control panel, and power supply.

Andromeda Turn-Key Computer Systems are easily expandable, and may be custom-configured to fit your processing requirements, space constraints and budget. Specify 8-inch disks if you wish, or dual drives, or floppies...or a combination.

Andromeda is the Q-Bus specialist. Our single objective is to develop fine products that unleash the power that is inherent in your DEC LSI-11 system.

Call or write today for more information. We'll be in touch.
Integral universal counter/timer upgrades oscilloscope

An expansion module for the HP 1980A/B oscilloscope adds the accuracy and counting modes of a universal counter to the setup and display capabilities of a programmable oscilloscope. The HP-IB programmable HP 1965A performs universal counting and gated timing measurements with 500-ps resolution, ±10 ps. The combined, integrated system has a trigger view feature that eliminates measurement uncertainty and replaces the technique of externally gating a counter with an oscilloscope. Continuous calibration allows specification of any waveform portion as the interval to be measured; an additional waveform is generated on the display to show the interval being measured.

Without manual setup, the system measures rise time, fall time, pulse width, duty cycle, propagation delay, and phase shift. A menu-driven auto-parameter key provides a choice of accurate, repeatable measurements. The system finds absolute maximum and minimum, sets trigger levels, and measures time intervals for standalone applications. Timing measurements can be made on amplitude signals as low as 3 mV; trigger circuitry offers a wide dynamic range and measures complex waveforms with resolution to 40 µV.

Scope and counter measurement paths are characterized to each other to reduce systematic errors. Together, they make period and frequency measurements up to 100 MHz with 9-digit resolution. A time-interval function measures the time between user defined start and stop points. Typical time-interval measurements include time between edges of a complex pulse train and the propagation delay between a clock and a data stream. Events functions, which are selected through soft keys defined by the oscilloscope’s CRT, count the number of occurrences of one or more signals. Events functions can be used to detect glitches or intermittent pulses and include A (gated), A during B, ratio A/B, totalize A, totalize A + B, and totalize A – B.

Also accessed through the display menu, the reference function can zero all paths to the probe tip of the reference signal. This makes it possible to null out propagation delays caused by different cable or probe lengths. In addition, a known value can be set as a reference for frequency, period, time-interval, and events functions. Reference functions can also be set up manually when measuring variances or drift.

Unarmed, armed, and gated modes are generated using the scope’s main and delayed sweeps. This gating capability makes it possible to specify the desired waveform interval for measurement. Burst frequency, time interval between pulse train edges, or propagation delay between specific edges on channels 1 and 2 can be measured.

For accurate measurement-interval gating, arm delay positions the start of the intensified marker, and gate width controls the marker’s duration. The system then calibrates readouts and measurements. Counting sources A and B can be assigned to main or delayed signals as channel 1, channel 2, external, or line.

Besides channel 1, channel 2, and trigger-view waveforms, the system will generate a count view showing the interval being measured on a realtime waveform. Measurement resolution can be selected based on the digits of resolution required and measurement time allowed. In auto-resolution mode, the counter/timer automatically selects the resolution to update measurement results every 2.5 s.

Other system features include a 50-setting alarm timer and a realtime, battery-backed clock displayed on the CRT. Two auxiliary BNCs on the counter provide a 10-MHz oscillator I/O and a TTL pulse for driving devices like a trace recording camera.

The HP 19800A waveform measurement library has software for automating time-domain measurements and performs statistical analyses on measurement results. Given the software library and full HP-IB programmability of both counter/timer and scope, many setup and measurement functions can be completely automatic. Moreover, the system can be set up from the front panel and the setup learned by a computer. The HP 1965A gated universal counter costs $2535; the HP 1980A/B scope is $10,500, and the HP 19800A waveform-measurement library, $1000. Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 318
5¼" Winchesters pack up to 380M bytes

EXT-400 family disk drives employ the company's enhanced small disk interface (ESDI) to transfer data between disk and host computer at 10 MBps. This is twice the transfer rate of the standard ST506/412 interface, and the company is actively working to make the ESDI an industry standard. Drives have capacities of 75M bytes (2 disks), 175M bytes (4 disks), 280M bytes (6 disks), and 380M bytes (8 disks). The fast transfer rate allows up to 14,873 flux changes/in. A 2, 7 run-length limited encoding scheme yields a bit density of 22,310 bpi, which is 50% higher than is possible with conventional MFM encoding. The drives use nonreturn to zero data transfer between drive and controller, since the data separator is on the drive itself—not on the controller, as in ST506 compatible drives.

Moreover, the family's Whitney-type ceramic composite head sliders are 33% smaller than the conventional Winchester sliders. They feature 2-rail construction, with the ferrite recording gap at the outermost edge. This design, in conjunction with the small slider size, allows a higher exploitation of the disk surface than with conventional Winchester heads.

Using plated media, the drives store 25.5M bytes per disk surface, with 1224 cylinders. Average access time is 30 ms. EXT-400 members are designed with a spindle motor that allows up to 8 disks to reside within the 5¼" form factor. Standard features include Maxtorq rotary voice coil actuator, closed-loop servo system with dedicated servo service, and Maxpak printed circuit board with surface mounted devices for control and read/write electronics.

In quantity-1000, the drives cost from $1295 to $3695 each, depending on capacity. Maxtor Corp, 5201 Lafayette St, Santa Clara, CA 95050. Circle 319

Color printers integrate text and graphics on plain paper

Series 200 EPM (Photo) employs a solid state raster line printhead that produces 200 dots/in² on smudge-free plain paper. Because the printer is based on nonimpact technology, it can be programmed to generate a virtually unlimited array of text and graphics characters and symbols.

The 8.27" (21-cm) wide printhead has over 200 nibs/in, with an "all points addressable" feature for graphics. The printer processes up to 6 pages each minute—equivalent to about 300 lines/min. Built-in sheet feeder and output stacker manage paper flow.

Series 200 input is a 1-MHz video bit stream, which is buffered internally, then fed to the printhead one raster scan line (1680 pixels) at a time. The image is transferred to paper from the ink donor roll, which consists of thin backing material coated with a nondegradable dry ink. Thermal nibs melt the ink on the donor roll just before a pressure roller pushes it against the paper. Each donor roll produces up to 1300 pages.

A second release, the Series C ink jet printer, also uses plain paper—either cut sheets or rolls—and prints 20 cps with 120-dot/in² resolution. Clay coated paper can be used for high quality color printing. Ink dries on standard paper in 1 s.

Sixteen-nozzle head featuring drop-on-demand technology can put a dot of ink virtually anywhere on the page. The desktop unit uses 4 nozzles for each of 4 colors to produce a total of 7: cyan, black, magenta, yellow, violet, green, and red. The Ink jet generates color backdrops, halftones, multiple color intensities, and complementary imaging. Five halftone levels are available for printing graphics.

When printing text, the unit employs a 4-pass mode that generates 12 x 16 resolution; when printing special graphic mosaic or symbols, a 5-pass mode prints with 12 x 20 resolution. The 96-char ASCII set and 64 mosaic chars are stored in PROM. Besides the U.S. configuration, 5 standard European character sets are available: French, Norwegian/Danish, Spanish, German, and British.

Series C ink jet printers will be available in the 3rd quarter 1983, at about $1250. Series 200 EPM is available 90 days ARQ and lists at $4995 quantity-one. Diablo Systems, Inc, 24500 Industrial Blvd, PO Box 5003, Hayward, CA 94545.

Circle 320
D/3D INTERACTIVE COLOR TERMINAL
MATROX GXT-1000

THE NEW MATROX GXT-1000 color graphics terminal delivers true 2D/3D interactive performance. It’s fast. It’s intelligent. It’s high resolution. And it costs less than $10,000 in OEM quantities. Complete.

THE GXT-1000 TRANSFORMS, CLIPS AND DRAWS lines at speeds of up to 20,000 vectors/second. Area filled rectangles at 5000 rectangles/second. True 3D 1000 polygon pictures with hidden surfaces removed and shaded in 10 seconds.

HOST WORKLOAD AND COMMUNICATIONS ARE GREATLY REDUCED. The GXT-1000 allows the user to down load complete object data files, using 64K x 64K x 64K virtual co-ordinates, to local memory. The terminal contains up to 22 Mbytes of RAM and disk memory for local picture segment storage, (up to 2000 active segments). Once downloaded, all data manipulation and viewing can be performed locally, in near real-time, without host support.

HIGH RESOLUTION
- up to 1280 x 1024
- 4 to 16 video planes
- 256 color look-up table per surface
- 19" high res. color monitor
- interlaced or non-interlaced

HIGH SPEED
- 80286 graphics engine
- 6 pipelined slave processors
- up to 20,000 short vectors/sec
- up to 5000 filled rectangles/sec

HIGH PERFORMANCE
- 64K x 64K x 64K virtual addressing
- local picture storage up to 22 Mbytes on disk
- local segment storage up to 1 Mbyte (2000 segments) in RAM
- full 2D transformations standard
- 3D with hidden surface removal and shading optional
- multiple viewports and dialog areas (up to 64)
- real time pan in 64K x 64K virtual space

LOCAL I/O SUPPORT
- host interface via RS-232, RS-422/449 or parallel DMA
- detachable low profile keyboard
- complete interfaces for data tablet, optical mouse, printer & plotter
- add-on Winchester/floppy disks

OEM OPTIONS
- desktop or rackmount electronics
- available unbundled as Multibus board set
- VAX host software package

Multibus, 80286 - TM INTEL VAX - TM DEC

matrox
electronic systems ltd.

5800 Andover ave.,
T.M.R., (Montreal) Quebec
Canada H4T 1H4
Telex: 05-825651
Tel.: (514) 735-1182
CIRCLE 106
STD-bus development system matches language to job

An advanced software development system gives board-level microcomputers a self-contained hardware/software environment for developing realtime applications. DV-9 features 2 independent STD-bus systems: a development computer and a target backplane. Dual-backplane architecture maintains a stable, full-function development system apart from the experimental target application. In addition, the system supports a software library offering Pascal, COBOL, BASIC, C, and D-Forth, as well as assembly language. In many cases, this lets engineers choose the language that best fits a particular application as well as their own language preference.

Development tools operate under OS-9, a modular operating system similar to UNIX that controls a full multi-user, multitasking environment. The system will generate ROM resident software based on either OS-9 or D-Forth. The development computer generates and maintains application source code and develops OS-9 based applications, while the target backplane configures application hardware and software.

LSI based networking microcomputer

Firmware-controlled LSI Micro 6 CPU is fully compatible with the DPS instruction set. In addition, the microcomputer runs menu-driven General Comprehensive Operating System (GCOS) 6 MOD 400, Release 3, which is used on the larger DPS 6 and Level 6 minicomputers. Program development capabilities include full-screen editor and ANSI standard FORTRAN, BASIC, COBOL, and Pascal. Moreover, an 8086 processor option plugs into the system’s base logic board to support MS-DOS, CP/M 86, and a wide range of application software.

The computer has 128K-byte main memory expandable to 512K bytes: one or two 51/4” diskettes store 650K bytes each (formatted). The desktop version field upgrades to a floor model that provides another 20M bytes of Winchester disk storage as well as support for a second video workstation.

A separate processor controls I/O and provides full functional compatibility with DPS peripheral systems. Two RS-232-C/RS-422-A asynchronous ports and an optional synchronous port are supported. The synchronous port communicates with Honeywell’s distributed systems architecture (DSA) and non-DSA Honeywell hosts, as well as with IBM hosts that use BSC and SNA protocols. The computer also supports public and private X.25 packet-switching protocols that access public data and value-added networks. Character-synchronous or bit-synchronous protocols are supported in half- or full-duplex modes.

An antiglare 12” (30-cm) green phosphor screen offers 720 x 300 resolution in an 80-column x 25-line display. A character generator table contains up to 256 symbols that are software loaded to accommodate different character sets. The ergonomic design features tilt and swivel monitor base and reprogrammable detached keyboard with color-coded function keys. Desktop microSystem 6/10 configuration starts at $3995; hard disk model starts at $9995.

Honeywell Information Systems Inc, 200 Smith St, Waltham, MA 02154. Circle 322
ADAC offers the widest selection of complete LSI-11 systems and function cards... both analog and digital. And now two new software subroutine libraries support all of ADAC's extensive line of interfaces for LSI-11. ADLIBRT is fully compatible with RT-11 (single user) real-time operating system software. ADLIBRSX enhances RSX-11M (multi-tasking/multi-user) operating system software.

Both ADLIB packages are simple to use, yet powerful, software tools that slash the time needed for program development.

ADLIBRT and ADLIBRSX support:
- mV Level A/D Conversion
- Temperature Measurements
- High Level, High Speed A/D Conversion
- TTL Level Digital I/O
- Discrete, High Voltage, AC/DC Interfaces
- Pulse Counters and Pulse Trains Out
- Optically Isolated Discrete I/O
- Contact Closure Sensing
- Discrete High Current Outputs
- Programmable Clock
- Serial Interfaces

Call, write or circle the number below to obtain our ADLIB data sheet and new catalog describing all of ADAC's LSI-11 compatible interfaces.

ADAC corporation
70 Tower Office Park • Woburn, MA 01801
(617) 935-6668

CIRCLE 107
Statistical multiplexer PIN 9106 was developed for async minicomputer systems requiring error correction from remote terminals or printers. Two async channels can operate at up to 9.6k bps; 4 channels at 4800 bps. Combined data rate is 19.2k bps, while composite link operates at 9600 bps sync or async. Multiplexer is compatible with 212-type 1200-bps full-duplex modems, and features 2K-byte buffer, menu-driven parameter selection, and LED diagnostic indicators. Gandalf Data Inc, 1019 S Noel, Wheeling, IL 60090.

Circle 323

Micro/mini datacom
StationMate is a data communications system consisting of a stat MUX; an intelligent modem with auto-dialing; and a LAN interface, XLAN, which supports 64 devices over a 5000' (1524-m) bus. System is Bell X.25 compatible and has 3 data ports with RS-232-C connectors. Other features include 16K-byte segmented buffer, auto baud, diagnostics, menu-driven setup and configuration with password security, and error-free data transmission with detection and retransmission on error. System is priced at $1450. Complexx Systems, Inc, PO Box 12597, Huntsville, AL 35802.

Circle 324

PBX voice/data modem
Full-duplex, 2-wire ComNet 48 provides sync and async data communications at 4.8k bps, and isochronous operation at 300 to 1.2k bps. Use of existing twisted pair wires eliminates need for a central switch, additional cabling, and changes to the main distribution frame. The unit plugs directly into an existing wall telephone jack, and features auto-answering of terminals and computer ports. As a standalone unit, ComNet 48 rackmounts to accommodate 12 modules in one 8.75" x 19" (22.23- x 48-cm) cage. Avanti Communications Corp, Aquidneck Industrial Park, Newport, RI 02840. Circle 325

Protocol link to small computers
Stored on a 5¼" floppy diskette, a software package enables small computers to emulate the IBM 3278 bisync display terminal when attached to a DataLynx/3270 or /3274 protocol converter via dedicated or dial RS-232-C series port. The program also allows a computer to emulate the ADM3A terminal. Moreover, it permits an IBM PC to operate at 9.6k bps, and includes menu options for 300-, 1.2k-, 2.4k-, 4.8k-, or 9.6k-bps operation. Local Data, 2701 Toledo St, Torrance, CA 90503.

Circle 326

Compact component modem
Mounting directly into a PCB, CH1760 is an 8 in², Bell 212A compatible modem. In component form, the modem offers a TTL host interface that allows the host to send serial async commands over serial lines. As an intelligent modem, it provides call progress tones and 6 dialing procedures. The component stores a 32-digit last number dialed, but supports an external RAM port for storing up to 52 additional numbers or log-on messages. Other commands include 8 diagnostic test modes, voice/data switching, and data transparency. Priced at $495, volume discounts are available. Cermetek Microelectronics, 1308 Borregas Ave, Sunnyvale, CA 94086.

Circle 327

Single-board sync modems
Two sync modems, NP-96 and NP-48, provide baud rates of 9.6k and 4.8k bps, respectively. Designed for full-duplex, point to point applications, modems are CMOS-LSI implementations of QAM modulation, phase jitter compensation, and equalization techniques. Front panel indicators display line status and diagnostic and configuration information. The NP-96 provides fallback rates of 7.2k and 4.8k bps when line conditions do not support the full rate. The NP-48 sells for $1800, the NP-96 for $2750. Network Products, Inc, Research Triangle Park, NC 27709.

Circle 328

Network stat monitor
LocalNet 50/120 statistical monitor connects to a network via an RS-232-C interface. Users specify time periods for the screen to display cumulative information and peak data value on data packets transmitted, characters sent, sessions connected, and channel usage. This allows flexibility to monitor network conditions and optimize network traffic. Monitor uses standard ASCII terminal and 1-page 24 x 80 format. Sytek Inc, 1225 Charleston Rd, Mountain View, CA 94043.

Circle 329
THE BUS STOCKS HERE:

PSM-512A: 512 kbyte Multibus™ memory with ECC, 275 nsec access time. Fixes single-bit errors, flags multi-bit errors.
CIRCLE 108

PSM-512P: 512 kbyte Multibus parity memory, 240 nsec access time. Very economical.
CIRCLE 109

PSM6463: 64 kbyte non-volatile CMOS Multibus memory, 200 nsec access time. 350 hour standby with on-board rechargeable NiCd's, 8 years with lithium. For process control, telecommunications, other critical applications.
CIRCLE 110

NEW PSM1VA: 1 megabyte VERSAbus™ memory with ECC, 300 nsec access time. Lots faster and much less expensive than Motorola and IBM equivalents. Full 32-bit VERSAbus compatibility.
CIRCLE 111

If you're on board the Multibus or VERSAbus, we've got the memories you need to get where you're going faster, for less. ECC, parity and non-volatile CMOS. All in stock now, all with one thing in common. Their first name is Plessey.
And since Plessey makes them all, they all have high reliability, a one year warranty and Plessey support worldwide.
For more information, just contact Plessey Microsystems, 451 Hungerford Drive, Rockville, MD 20850. (301) 279-2892, TWX 710-828-9815.
Irvine, CA: (714) 540-9931.
In Europe, contact: Towcester, UK: (0327)50312, Telex 31628. Paris: 776 41 06.
Noordwijk: (01719) 19207. Munich: (089)2362226. Rome: (06) 350189.
Or get on board fast by calling (800) 368-2738 today. Your bus ought to be going our way.

Multibus is a trademark of Intel
VERSAbus is a trademark of Motorola
Digitizer improves voice quality
Series 1000 voice digitizer converts voice to digital bit stream for full-duplex transmission. Digital interface is RS-232-C and voice interface is PBX tie or other voice channel. Speech, data, and several voice channels can be transmitted simultaneously using multiplexers. Built-in diagnostics from the board to system level via keypad or loop-back configurations are standard. Digitizer is compatible with other series 1000s and with TSP 100/200. Time and Space Processing, Inc., 3410 Central Expy, Santa Clara, CA 95051. Circle 330

Data multiplexer for PABX
SX-200® and SX-100® divide output from a PABX RS-232 port into 4 categories. Data are then transmitted via RS-232 interface or 20-mA loop to separate terminal devices. Programmable character length, stop bits, baud rate, and parity are standard features. Housed in a compact, locking metal cabinet, the data multiplexer comes with its own power supply. If commercial power fails, unit features data "cut through" to preassigned port. Mitel Corp, 350 Legget Dr, PO Box 13089, Kanata, Ontario, Canada K2K 1X3. Circle 331

Ethernet network repeaters
When used with local repeaters, a remote unit allows up to 1000 m of fiber optic cable to be added to the Ethernet network between any 2 baseband cables, extending the network to 2500 m. A local repeater prevents distortion of information traveling more than 500 m over baseband cable segments. Both versions operate at a 10M-bps data rate. The local repeater is $2500 and the remote repeater (including a local repeater), $7700. Ungermann-Bass Inc, 2560 Mission College Blvd, Santa Clara, CA 95050. Circle 332

High speed modem
The Data Mover v.29 modem operates at 9600 bps. Its manufacturer claims that using it for data transmission over a leased line for one hour per day over a 5-day week (48-week year) is cost competitive with using lower speed modems to send data over the PSTN. The Data Mover incorporates a single PCB that makes extensive use of CMOS LSI circuitry; the calculated MTBF exceeds 30k h. Seven front-panel LEDs indicate operational status, and routine system diagnostics can be carried out via three PCB mounted switches. Easydata Ltd, 7 Carleton Rise, Welwyn, Herts AL6 ORP, England. Circle 333

HAVE IT YOUR WAY!
Custom Modems

Need a special interface? Call Omnitec Data.
Want translation for security? Call Omnitec Data.
Tired of compromising system design because of arbitrary modem constraints? Call Omnitec Data.
Want your own case? Call Omnitec Data.
Need a dependable, quality modem supplier? Call Omnitec Data.

Put Omnitec Data's 17 years of modem technology and manufacturing know-how to work in your terminal system or other OEM configuration. The unique micro-processor design implementation employed in our extensive family of Bell licensed, 212A compatible standard modems permits us to quickly and simply design to meet the exact specifications of your system. For details about Omnitec Data custom and standard modems phone Dan Mitchell, 1-800/528-8423 or write him at Omnitec Data, Incorporated, 2405 South 20th Street, Phoenix, Arizona 85034, 602/258-8244.
GTCO DIGITIZERS MAKE YOU NUMBER ONE

We're the largest producer of electromagnetic digitizers. So we can deliver field proven tablets in the quantity you need... when you need them.

Our Digi-Pad family uses new technology to provide unique digitizer features.

■ PRESSURE PEN
  The pressure sensing pen option gives the operator a more natural input... perfect for the artist.

■ 4D
  The 4D option provides another independent variable proportional to stylus tilt and direction... like a joy stick.

■ SELF DIAGNOSTICS
  A 4-tone alarm reports test results for all components including the tablet grid... insuring digitizer integrity.

Every Digi-Pad is compatible. So when you develop your software and interface around our smallest and least expensive Digi-Pad (under $1000), you can interchange any other size Digi-Pad without redesign. Digi-Pad is also compliant with U.L., FCC and many other standards.

Give your system an edge. Choose the number one digitizer from GTCO. Call us at (301) 279-9550 today.

GTCO Corporation
1055 First St. Rockville, MD 20850
(301) 279-9550 Telex 898471

CIRCLE 113

See us at NCGA, booths 2032 and 2033
Network multiplexer

**GEN•NET 1262** is a sync/bisync network multiplexer. Design includes 168-kbps speed on 4 composite links, high buffer storage, and 96 channels. System is available in 8- or 24-channel models. Multiplexer has a supervisory port and provisions for auto retransmission of data on error. All link and channel characteristics are selected and set individually for flexibility. Channel priority, diagnostics, and password protection are also featured. General DataComm Industries Inc, 1 Kennedy Ave, Danbury, CT 06810. Circle 334

Small DDP office system

With multifunction capabilities, model 565 is a small cluster distributed data processing system. It provides a Winchester disk drive and streaming cartridge tape backup, and supports 4 terminals. Hardware capabilities include up to 512K bytes of memory; 185-ns, 6-MHz processor speed; and communications support. Operating system, interpreter, and 25 utilities are part of the software, while word processing, text editor, and compiler are optional. Northern Telecom Inc, 259 Cumberland Bend, Nashville, TN 37228. Circle 335

**VAX Ethernet connection**

DEUNA, Ethernet-to-Unibus communications controller, is a microprocessor based design for maximum throughput with minimum host intervention. Controller implements channel access and data link management functions. On-board diagnostics detect device errors and provide simple isolation. Loop-back diagnostics allow more detailed isolation. With 32K-byte buffer space, the unit is priced at $3500 and is scheduled for delivery in July. Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Circle 336

**Intelligent modem**

R212A is an auto-dialer modem that can store up to 10 phone numbers, each with an accompanying 30-character description. With HELP commands, user can dial from the keyboard or use a single keystroke to dial from the memory. If line is busy, modem can automatically link to an alternate number or redial the last number dialed, even if the number is not in memory. Software allows all option settings and test features to be controlled from the keyboard. Priced at $495, modem is Bell compatible (212A, 103, 113) and has battery protected memory. Rixon Inc, 2120 Industrial Pkwy, Silver Spring, MD 20904. Circle 337

LOW COST, HIGH ACCURACY

**CAPACITIVELY COUPLED POSITION TRANSDUCERS**

Farrand High Gain INDUCTOSYN® linear and rotary position transducers, custom designed to meet size, accuracy, and environmental requirements, can cost as little as $10.00 each in production quantities.

Accuracies to ±50 microinch, repeatability to ±20 microinch. Pitch to user specification; .010" to .020" typical. Auxiliary control signals, such as End of Travel or Track Location, can be included. Any substrate material, from cast aluminum to fiberglass tape. Thermal time constant adjustable to match user structure, eliminating inaccuracies during warmup.

Farrand Industries, Inc.
99 Wall Street
Valhalla, NY 10595
(914) 761-2600
Telex: 646640

INDUCTOSYN® is a registered trademark of Farrand Industries, Inc.
Selecting software is really a game of strategy: positioning the right product at the right time for the most effective results.

At Whitesmiths, Ltd., our full line of software products is designed to do just that and more. Our time-tested compilers are available for five architectures, complete with Pascal translators and cross-support for a wide range of environments. From the MC68000, to the IBM PC, to the DEC Professional, our compilers and cross compilers cut software development time and reduce dependence on operating systems and instruction sets.

Idris, our exclusive operating system, is powerful, small and extremely portable. Written almost entirely in C, it runs where other operating systems can't even fit - on an MC68000 with no memory management hardware, for example, or on a bank-switched 8080 or Z80. And it outperforms UNIX on comparable systems - an MC68000 with memory management hardware, for instance, or any PDP-11 or LSI-11. It even makes good use of a VAX, so you know you won't outgrow it!

In addition, our full line of Software A La Carte lets you select just the pieces you need to tailor our products for your unusual requirements. From portable libraries to special purpose tools, all A La Carte items are tested, easy to use, and very affordable.

To make things even simpler, Whitesmiths, Ltd. has introduced a new marketing tool: the Authorization Seal. Instead of hassling with complex license agreements and other legal stumbling blocks, you simply affix a serially numbered Authorization Seal, issued with each sale, to any machine that retains a copy of our software. End of hassle. All our customers - end-users, OEMs, and sublicensees - benefit from the elimination of multi-tier licensing agreements and detailed record keeping.

Compilers, Idris, Software A La Carte, and the Authorization Seal; together they can position you for today's competitive market - and tomorrow's. Before you make your next move, call or write to Whitesmiths, Ltd. today. We'll be glad to help you play to win.

Whitesmiths, Ltd.,
97 Lowell Road, Concord,
MA 01742, (617) 369-8499
TLX: 951708 SOFTWARE CNGM.
"TO ALL YOU OEM'S WHO ASKED FOR LINE PRINTER SPEED AND TYPEWRITER PRINT QUALITY:

YOUR LINEWRITER IS READY."

—John Tincer, President

Recently we asked what you wanted most from the next generation of line printers. You told us in no uncertain terms: typewriter quality print at line printer speed; more reliability and less need for service.

So we built it—a printer that embodies everything you want and eliminates everything you don't want.

We built your line printer. The Centronics Linewriter 400.

We can't describe the superior print quality—so we'll let you judge for yourself. Just look at the unbelievable difference between the Linewriter 400 and standard band printer samples.

To build the Linewriter, we developed some proprietary innovations that redefine established line printer technology.

For reliability—LSI and VLSI electronics and up to 15 KV ESD immunity throughout. To improve throughput we included statistical printbands and early end of print. Then we finished it off with human-engineering features: extensive self-diagnostics and an alphanumeric display to pinpoint specific problems; resonating ribbon cassette that doubles ribbon life; 2860 hr. MTBF; 0.5 hr. MTTR and no scheduled preventive maintenance, plus a 55 dBA (optional) sound level.

The result is the Linewriter 400—the line printer that makes every other 300-500 LPM printer obsolete.

Which is no less than you should expect in a line printer you had such a large part in specifying. And one it took Centronics technology to build.

To find out more about the Linewriter 400 call our Line Printer Division (313) 651-8810, Ext. 342. Or write to us for more information and free print samples to Centronics Data Computer Corp., Dept. A, One Wall Street, Hudson, NH 03051.

OFFSET REPRODUCTION.
**System Components/Memory Systems**

**Cassette backup Winchesters**

II-10 (10M bytes) and II-20 (20M bytes) are Winchesters for the IBM PC. Featuring a high speed streaming tape cassette backup, the systems can be user configured in up to 10 logical volumes under PC DOS and up to 14 logical drives under CP/M-86. Utility programs include preserve, which saves and restores data on volumes in image fashion. Also included is filesave, which saves and restores data as single files or sets of files. Storage systems allow DMA operation and parity and error checking. The II-10 is priced at $2995; the II-20 is $3795. Sysgen Inc., 47853 Warm Springs Blvd, Fremont, CA 94539. Circle 338

**Memory subsystem increases VAX capacity**

Memory modules contain 64K-bit chips to increase VAX-11/780 main memory to 32M bytes. Memory subsystem contains memory controller and array boards that plug into the memory backplane. Existing systems users can upgrade memory through the controller and array boards or through the expansion cabinet. Prices, with controller, range from $28,900 for 2M to $36,000 for 4M bytes. Memory modules, sold in 2M-byte increments, range from $9000 for 2M to $34,000 for 10M bytes. Digital Equipment Corp., 146 Main St, Maynard, MA 01754. Circle 339

**Board expands 8086 memory**

VLS-C memory system expands capacity by 24 times and increases operating performance of 8086 based single-board computers by 50%. Both ports can access 1.5M bytes of EEC RAM with 450-nsec cycle time and 250-nsec access time. Board is supplied with contiguous and/or noncontiguous addressing, memory mapping, paging, and 32K-byte segmentation through 16M-byte range. Error status is displayed by onboard LEDs and through status registers. Basis for future cache memory implementation is available. All semiconductor components are in sockets for easy repair. OEM prices range from $1395 for the 512K to $3895 for 1.5M-byte system. Advanced Digital Technology, 696 E Trimble Rd, San Jose, CA 95131. Circle 340

**Floppy/Winchester memory system**

Multibus compatible, 51/2" floppy/Winchester Stacpac module provides a 500K-byte double-sided floppy drive and either a 40M- or 20M-byte Winchester. Two controller/interfaces are available: 5215 handles 51/2" Winchester and floppy and 5/4" streaming tape; 5217 adds file-oriented tape transfer capability. Prices for the floppy/Winchester module begin at $3895; controller/interfaces begin at $950. Volume discounts are available. Data System Design, Inc., 2241 Lundy Ave, San Jose, CA 95131. Circle 341

**Q-bus compatible memory**

PINCOMM 25S+ memory card has 1M-byte "quad-wide" CSR parity and uses 64K RAM technology. It is compatible with the DEC Q-bus series, PDP-11/25S, and other DEC Q-bus or extended Q-bus computers. PINCOMM 215S+ has double the capacity of the DEC MSV11PL (M8067) and can be installed in H9273-A or H9273-B backplanes. Its 22-bit addressing capability needs only 4 slots to allow user to add memory to complete the 4M-byte range. All board functions are switch selectable. Memory capacity ranges from 128K to 1M bytes. The 18-bit wide memory is organized with two 8-bit data bytes and two byte parity bits. Trendata Corp., 3400 W Segerstrom Ave, Santa Ana, CA 92704. Circle 342

**Magnetic tape drive**

A compact magnetic tape drive equips medium-sized IBM computers with many performance and storage capabilities of the company's larger units. IBM 3430 magnetic tape subsystem offers about 3.5 times the data rate and storage capacity of the current comparable model, the 3410. The device can operate with the IBM System/38 models 4, 5, and 7, as well as with virtual storage System/370 models 135 to 168, and 303X and 4300 processors. IBM Corp., Information Systems Group, 900 King St, Rye Brook, NY 10573. Circle 343

**JOIN THE PROFESSIONALS**

RTCS Products give your PC/MDOS computer, professional program development capabilities, just like Intel's Series III or System 86/330. RTCS offers a family of Operating System Development Tools.

**RTCS UDI**

The UDI allows your PC to execute Intel's Compilers, Assemblers and Utilities. Features: Memory Management, File Management, PC/MDOS File Structures, 8087 Support. REDUCED! $995.00 $500.00

**RTCS PC/RMX**

The RTCS PC/RMX lets your PC run under Intel's Real-Time Operating System, iRMX. Features: Up to 65536 tasks, Hierarchical Directories, Multi-User Capabilities, Supports IBM Peripherals, Hard Disk Support, Ethernet Support. $2250.00

**RTCS UDEBUG**

The RTCS UDEBUG is a powerful system debugger. 8087 support. Symbolic debugging. $750.00 $195.00

**RTCS PC/SBC**

Execution Vehicle

The PC/SBC allows your PC to control the execution of any of Intel's SBC Computers. Both download and upload capability. $750.00 $195.00

MDOS is a trademark of Microsoft Corp. SBC & iRMX are trademarks of Intel Corp.
High-density memory boards
A high density Multibus-compatible DRAM module with 197-nS access time and 303-nS cycle time (typ), the TMM40020 comes with up to 512K bytes of onboard RAM. The device provides memory expansion for all Intel 8080 and 8086 systems and can be upgraded to 2M bytes. Available with or without parity checking, the unit complements the TMM40010A, a Multibus-compatible module that includes std error detection and correction onboard. The TMM40020 operates in an address space of up to 16M bytes and supports word transfers, as well as high, swap, and low-byte transfers. Texas Instruments Inc, Semiconductor Group, PO Box 401560, Dallas, TX 75240. Circle 344

Winchester subsystems
Available in 16M- and 24M-byte capacities, the ISIS-II-compatible DataSafe Winchester subsystem can be placed directly on top of Intel Series II and III (or MD$-800) development systems. This allows engineers to increase their development system's speed and capacity without sacrificing bench space. The subsystems automatically protect data during power failures without special power-down sequences. The portable units can be moved without mechanical interlocks or other special precautions. Prices are $6500 for the 16M-byte version and $7995 for the 24M-byte model. Winchester Systems Inc, 14 Laurel Hill, Winchester, MA 01890. Circle 345

Streaming tape subsystems
MTS-1012/130 and MTS-1012/150 are 0.5" (12.7-mm), 9-track, 1600-cpi, IBM/ANSI/ECMA and ISO-compatible magnetic tape systems for DEC's Unibus and Q-bus computer systems. Both the 130 (Unibus) and 150 (Q-bus) use the IDT series 1012 Virgo, which operates at 100 ips streaming and 12.5 ips start/stop. All drives support up to 10.5 reels. Features include 160k-byte/s data transfer in streaming mode, over 6500 hours MTBF with diagnostic and self-test, DEC TM-11/TU-10 emulator, and IBM and DEC packing in either byte or word transfer. Unit price is $6495. Innovative Data Technology, 4060 Morena Blvd, San Diego, CA 92117. Circle 346

INTERFACEx

4-function IBM card
SystemCard for the IBM PC features serial and parallel interfaces, up to 256K bytes of RAM, and a calendar/clock with battery backup. Centronics-type parallel interface includes a print spooler buffer memory that allows use of the computer while printing a document. Async serial interface allows hookup to std remote data transmission terminals, modems, or letter quality printers. The device comes with either 64K or 256K onboard RAM. Disk emulator software is included. Microsoft Corp, 10700 Northrup Way, Bellevue, WA 98004. Circle 347

STD bus board
Z80 Smart Card operates with a 4-MHz Z80A processor; includes RAM, ROM, serial I/O, and diagnostic firmware; and is RS-232 compatible. Onboard switch selects either standard or STD bus diagnostic unit processor mode; programs can be executed in either mode. In processor mode, card acts as regular CPU and can drive additional memory or I/O cards. In diagnostic mode, it will test any card in the system with functions such as display/alter memory, test keyboard, test RAM, and read/write to I/O port. In quantities of 2 to 9 the card is $245. Forethought Products, 87070 Dukhobar Rd, Eugene, OR 97402. Circle 348

Color graphics controller
Based on a 16-bit microprocessor with 128K bytes RAM and 64K bytes ROM, Model One/25 color graphics controller is suited for imaging applications. Supporting image memory configurations of 512 x 512 with 24-bit planes, controller allows data to be represented in 16M colors. A pixel mover and DMA are available for high speed data transfers. Software features include integrated debugger, HELP facility, local command interpreter, and 4014 emulator. With applications in business graphics and CAD, the controller sells for $10,500. Raster Technologies, Inc, 9 Executive Park Dr, North Billerica, MA 01862. Circle 350

Temperature controller
A temp controller, 8203 RIOS, designed for use with a video terminal or computer, provides 8 temp input channels. Each channel has 0.25 °C resolution over a 60 °C span and is user adjustable from 55 to 150 °C. Controller incorporates a microprocessor, 4K bytes of EPROM, and 2K bytes of optional EEPROM. Up to 64 remote stations with 1024 separate control points can be directed from as far as a mile away. Controller will be available at a single-quantity price of $400. Crydom, div of International Rectifier, 1521 Grand Ave, El Segundo, CA 90245. Circle 352
New panel printers: ordinary paper is one of many smart benefits

Plain paper
Digitec's new family of panel mount printers uses plain paper. Benefits: It's inexpensive and readily available. It won't gum up the printhead as thermal and electrosensitive coated papers can. Your output is crisp, easy to read, won't fade. It reproduces.

OEM applications
New Model 6610 is $150 below competitive units. It's the first panel mount printer to feature a true RS-232-C/20mA I/O. Benefit: standard port permits easy interface with computers, controllers —any serial device, including the new generation of µ-P-based DPs.

New Model 6620 with byte serial port offers off-the-shelf compatibility with byte serial computers and peripherals.

Both new 24-column OEM printers feature an exclusive, optional 2K nonvolatile buffer. Benefits: large bursts of data can be accepted without slowdown. Battery backup prevents data loss in power outs. Get more speed and reliability than other panel printers offer.

Since our new OEM printers are µ-P-based, application-matching is easy. Graphics? Just tell us what you require.

- Use plain roll paper.
- Drop-in replacement for thermal and electrosensitive panel printers.
- DIN size adaptable.
- Choice of serial, byte serial, and BCD inputs for easy interface.
- µ-P-based for custom OEM application.
- Programmable and addressable dot matrix printing; graphics.

New DPI printer
For replacement or new panels, 16 or 22 column Model 6630 with parallel BCD input interfaces directly with most digital panel instrumentation. Half the price of competitive designs, the 6630 offers you the full value of our new printer technology.

An exclusive battery-backed program clock option lets you print calendar headers, real time, or both. It can also trigger timed readings from DPs.

Request Bulletin 4400, or call for demonstration.

Contact Digitec. 513-254-6251

Digitec Corporation
918 Woodley Road, P.O. Box 458
Dayton, Ohio 45401-0458
Telex: (310) 687-4219
DMA interface

The GPIB-796 is a Multibus to IEEE-488 interface that supports DMA transfers to/from Multibus memory in 64K bytes at 500k bytes/s. Memory addressing capability lies in a high speed 24-bit counter that allows the user to place buffers in memory regardless of size. Present software package is compatible with UNIX operating system; other modules will be available written in C and microprocessor assembly languages. Provided with full documentation, the interface is priced at $1295 with OEM discounts available. National Instruments, 12109 Technology Blvd, Austin, TX 78759. Circle 353

Compact graphics controller

The HRG2 packs a high resolution color graphics controller on a Multibus board. Hardware capabilities include 5K-byte video RAM, 80-MHz video output, 16-color simultaneous display, DMA interface, and up to 2M pixels/plane. Analog and digital output formats are provided. With the addition of a multi-plane controller board, multiple HRG2 boards can be used to create a 256-color raster display. Std configuration is 1K x 1K x 4 (interlaced); additional overlay plane on daughterboard is optional. Ikier Technology, Inc, 42 Pleasant St, Watertown, MA 02172. Circle 354

You could sell your hardware a lot easier if you had a coast-to-coast service team.

Now you can hire Bunker Ramo's

Your prospects don't want downtime. So no matter how good your hardware is, if you can't offer prompt, professional field service, they'll buy from someone who can.

Now you can offer this kind of support. Bunker Ramo's field service organization will provide service for your equipment anywhere in the nation.

Bunker Ramo has more than 50 years' experience supporting on-line, real-time DP and communications systems in critical applications: brokerage firms, banks, insurance offices—places where downtime means loss of revenue.

Today there are highly trained Bunker Ramo field engineers working out of 120 locations throughout the country; their activity is monitored at all times by a sophisticated, on-line, real time dispatch system. Chosen for their basic electronic aptitude, the field engineers receive initial training at Bunker Ramo's training center before being assigned to their field duties. Their skills are constantly being updated to keep them current with new technologies.

It's the kind of professional field service force that you would be proud to call your own.

You can.

Bunker Ramo is now offering its expertise in maintenance and repair to other manufacturers. For more information, call Bob Land, Director of Service Marketing, at (203) 386-2011, or write him at the address below. And find out how you can call our field service team your own.

Bunker Ramo Information Systems
35 Nutmeg Drive, Trumbull, CT 06609

An Allied Company

Z8 BASIC controller board

Based on the Zilog Z8671, a Z8 computer/controller comes with a BASIC interpreter, up to 6K bytes of RAM and EPROM onboard, an RS-232 serial interface with switch-selectable baud rates, and 2 parallel ports. The self-contained board expands to 124K and is optimized for use as a dedicated controller. CRT terminal connection allows immediate programming in BASIC or machine language. The Micromint, Inc, 561 Willow Ave, Cedarhurst, NY 11516. Circle 355

Q-bus and Multibus interfaces

Interface cards integrate model 521 high resolution display and digitizer/viewer systems with Q-bus and Multibus computers. The 4 interface registers appear as contiguous memory locations including 1 for image data and command register, and 2 to address image memory. Multibus interface is equipped with prefetch/delay store to increase data transfer speed. Each interface is one bus load to the host and at $1995 includes interconnecting cable and documentation. OEM discounts are available. Datacopy Corp, 1070 E Meadow Cir, Palo Alto, CA 94303. Circle 356
The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.

How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

The result: a triumph over the convergence factor. Find out what it can do for your next color terminal or monitor, and ask about our full line of quality color and monochrome CRTs. Write or call: Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5278.

The achievement of Panasonic high resolution in-line color CRTs.
Winchester disk exerciser

The Tracker handheld Winchester tester exercises 5 1/4" drives having a Rodime or ST 506 interface without corrupting data on disk. All unintentional write operations are prevented by the write protect interlock facility. Main interface status lines are constantly displayed on 6 LEDs; operational errors are indicated via audible alarm. Step rates are programmable over 30µs to 25.5 ms to emulate the step rate of most disk controllers. The unit can address up to 1024 cylinders. The price is $500. Rodime PLC, 25801 Obiero, Mission Viejo, CA 92691. Circle 357

Portable data transmission testing

A transmission impairment measuring set (TIMS) and a bit-error rate test set (BERT) combine to form HP 4935S, a data transmission set. System makes the transmission-impairment measuring and verify proper installation of data transfer rate is SM bps. Single-unit price is $500. Rodime PLC, 25801 Obiero, Mission Viejo, CA 92691. Circle 357

Digital event trigger generator

DEI-18 digital event trigger generator allows users to generate 1 output from a group of specified input states. Up to 18 TTL or LS/TTL compatible inputs are accepted, including clock and control lines. When the digital event occurs, 1 trigger output is generated. The true level for each of the 18 signal lines is switch selectable for high, low, or "don't care" input states. Generator derives its 5-V at 50-mA power from the circuit under test. Input connector is a std 20-pin header with 0.025" (0.064-cm) square posts. Price is $99, or $129 with 20-conductor input cable. Connecticut microComputer, 36 Del Mar Dr, Brookfield, CT 06804. Circle 359

Analog board test system

Implemented in Motorola's EXORBUS compatible modules, the Sleuth ATS (analog test system) measures voltages within a ±100-V range in its std configuration. Resolution is selectable down to ±10 µV. Std counter/timer permits frequency measurements in the audio range. All input multiplexer functions are implemented in arrays of fast mercury-wetted relays. Std modules include A-D and D-A converters, as well as sample/hold and peak measuring instruments capable of single-ended and differential measurements. Sleuth Tester Div, Engineering Consultants and Publications, 9 S 69th St, Upper Darby, PA 19082. Circle 360

Digital storage scope offers 4-channel display

PM3305 35-MHz digital storage scope provides 8K bytes of divided memory. Display mode uses 4K-byte memory and includes 2-channel input, sensitivity from 2 mV to 10 V/div, and time-base speeds from 100 ns to 0.5 s/div. Pre-trigger facilities include time-base extension to 5 s/div and 2 additional floating channels. A sequential sampling system stores repetitive signals up to the 35-MHz bandwidth and supplies an integral min/max function for storage and detection of glitches and pulses as short as 50 ns. Display can be expanded 10 times and memory segments can be displayed on a 4 or 40 times greater scale. Philips Test and Measuring Instruments, Inc, 85 McKee Dr, Mahwah, NJ 07430. Circle 361

Protocol monitor simulator

The latest in a line of protocol monitor/simulators, the Dyna-Test 1600 portable tester can be used to isolate malfunctions; perform qualitative measurements; or simulate a modem, terminal, or computer port in the data network. Principal features include an integral tape capable of capturing data at rates as high as 56k bps, a protocol key that stores operating parameters for 7 different lines, and clear text display of the SDC or HDLC control bytes. The device supports most std protocols, including IBM 360. Std interfaces and data codes are available. Dynatrace Data Systems, 7644 Dynatech Ct, Springfield, VA 22153. Circle 362

Single-board CP/M computer

Multibus compatible board KG-802, when combined with CP/M 2.2, forms a single-board computer with 64K-byte RAM. 280A CPU runs at 4 MHz and board can support single- and double-density disk formats that interface to Shugart 801 disk drives. Other features include 4K-byte boot PROM, 2 RS-232-C ports, 8 vectored interrupts, and a CP/M+ 2.2 operating system. Price is $995. Raster Graphics Inc, PO Box 23334, Tigard, OR 97223. Circle 363

Rocker switches

The 0815 series switches are rated at 12 A, 125 Vac, and 0.5 HP, 125 to 250 Vac, and come optionally with 15 A, 125 Vac, 0.5 HP ratings. Solid or lighted rockers are available in a range of colors, with customized legends. Std bezels are black. One-piece molded plastic, snap-in mount cases fit into 0.55" x 1.125" (1.4- x 2.858-cm) openings and hold securely in 0.031" to 0.251" (0.079- to 0.638-cm) thick panels. Quick disconnect 0.25" (0.64-cm) terminals or 16-gauge wire leads are supplied. Circuits available are SPST, SPDT, SPST center-off, and SPST with integral 125-Vac neon lamp or optional 6- to 14-Vdc or 28-Vdc filament lamp. McGill Manufacturing Co, Inc, 1002 N Campbell St, Valparaiso, IN 46383. Circle 364
The Architectural Breakthrough

The latest development in digital image processing is here! It's a major breakthrough in systems architecture from Vicom Systems, Inc. And it combines patented hardware and software features you've been waiting for to give you unequalled speed and flexibility in a variety of applications.

The Fully-Integrated System The VICOM Digital Image Processor is a versatile computing tool... the first to use the architecture of the Motorola 68000 microcomputer. The entire system—lookup tables, image pixels, registers, array processor, and RAM memory—resides in the direct address space of the 68000, providing the ultimate in accessibility and efficiency.

The VICOM system can operate as a real-time scene analyzer, a peripheral processor to a host computer, or a stand-alone digital image processor.

Image Processing . . . Without Programming The VICOM Digital Image Processor is easy and fast to operate. You can perform complex operations and make changes simply, without having to write a program.

The VICOM Image Processing Software package (V.I.P.S.) includes over 100 high-level interactive commands that significantly reduce project implementation and execution time.

Experience the VICOM Breakthrough for yourself. Call or write for more details and a demonstration.

Vicom Systems Inc.
2307 Bering Drive
San Jose, California 95131
(408) 946-5660 (800) 538-3905
TELEX 171603 VICOM SYS

Vicom. The next generation in image processing.
These days, it takes more than superior features to sell your imaging system. It takes a dazzling image, be it color or monochrome. Because from your customers' point of view, what's on the screen is more important than what's behind it. That's why you should look into using a high resolution KRATOS monitor in your system.

**MINIMIZED JAGGIES**

At best, most raster-scan monitors display curves as staircases, and straight lines as jagged ones. To improve this situation, some manufacturers alter their image through software manipulation. But that merely disguises the problem. KRATOS has a better approach.

<table>
<thead>
<tr>
<th>Model</th>
<th>Color/Mono</th>
<th>CRT size (diagonal)</th>
<th>Deflection angle</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1000</td>
<td>mono</td>
<td>19-inch</td>
<td>114°</td>
</tr>
<tr>
<td>M1200</td>
<td>mono</td>
<td>19-inch</td>
<td>90°</td>
</tr>
<tr>
<td>M1200</td>
<td>mono</td>
<td>25-inch</td>
<td>90°</td>
</tr>
<tr>
<td>KM1400</td>
<td>color</td>
<td>19-inch</td>
<td>90°</td>
</tr>
</tbody>
</table>

**1024 LINES, NON-INTERLACED**

Our 1280 pixel x 1024 line format is non-interlaced. So at any given instant, KRATOS monitors display twice as much data as comparable top-of-the-line interlaced monitors. And that's clearly an advantage for you.

**COLOR OR MONOCHROME**

At KRATOS, we offer you a clear choice of high resolution monitors: both color and monochrome models.

Our KM1400 color monitor is probably the best raster-scan monitor on the market. It maintains color fidelity without a flicker. The result is no eye strain, and something every customer likes to see—improved productivity.

We also offer three picture-perfect monochrome models: the reliable M1000, the precision M1100 with its smaller spot size and 90° deflection tube, and, to give you the big picture, the 25-inch M1200. All models are available in both landscape and portrait formats.

**HIGHER REFRESH RATE AND BANDWIDTH**

As you can imagine, presenting data at this high rate is no easy task. So to keep the display from flickering, KRATOS monitors provide a 60Hz refresh rate (64KHz horizontal scan rate). And that's nothing to blink at.

To further refine your image, KRATOS monitors use a video amplifier with a bandwidth of 100MHz. Technically speaking, that means a rise and fall time of less than 3.5 nanoseconds per pixel. To your customers, it means a brighter, clearer view of things.

**SEE US SOON**

So no matter what your application: CAD/CAM, medical imaging, NMR, or graphic simulation to name a few, KRATOS can do wonders for your image. Not to mention your sales.

For more information about these and other KRATOS products, call or write us at 101 Cooper Court, Los Gatos, CA 95030; phone (408) 395-3700; TELEX 171946.

**WHAT A KRATOS MONITOR CAN DO FOR YOUR IMAGE.**

© 1983 KRATOS Display Systems

See us at NCGA booth #2251
Flexible single-board computer
Eliminating the need for separate memory, I/O, and time functions, the
STD-147 is a Z80A single-board computer. STD bus compatible, it features
3.69-MHz Z80A with crystal clock, program disable of 16K-byte EPROM,
time/calendar, 8 programmable control lines, and 2 programmable timers. With
optional 64K-byte DRAM the unit is $395; without, $250. Micro-Link Corp, 14602
N U.S. Hwy 31, Carmel, IN 46032. Circle 365

19M-byte, 16-bit micro
Model 140 offers 50% more disk storage capacity—19M bytes in contrast to
12.8M bytes—than other models in the 1000 series. Basic configuration includes
CPU with 128K bytes of main memory; 1M-byte floppy disk drive; 5.25", 19M-byte hard disk drive; and 2 RS-232-C ports. Including operating system, this
configuration costs $8995. Micro Five Corp, 17791 Sky Park Cir, Irvine, CA
92714. Circle 366

Z80A based universal board
M-11, a Z80A based computer board, provides 64K-byte RAM with 12K-byte
EPROM capacity, 4 onboard series interface ports, and a parallel interface port.
Designed for a CP/M operating system, the board features simultaneous and
mixed control of 5 1/4" and 8" floppy drives. BIOS uses 4K-byte RAM for auto-
board rate detect and high speed sector skew for operating software control.
Single unit sells for $595; OEM quantity pricing is available. James Electronics,
Inc, Computer Div, 4050 N Rockwell St, Chicago, IL 60618. Circle 367

Multitasking microcomputer
A dual-processor unit brings the power of the 16/32-bit MC68000 to Z80A based
series 8S-3A microcomputers, while maintaining compatibility with CP/M and exist-
ing 8-bit software. Other sid features include up to 4M-byte main memory,
2.4M-byte dual floppy drives, and 21 backplane expansion slots. Optional
built-in hard disk stores another 21M bytes. The 2-processor configuration
runs Cromix-D, multi-user, multitasking operating system whose features and
user interface are similar to UNIX. Dual-
processor system with 256K RAM costs
$7995. Cromemco, Inc, 280 Bernando
Ave, PO Box 7400, Mountain View,
CA 94039. Circle 368

Single-chip microcomputer
HMOS II processed 8050A achieves video
speed, low power, and high reliability in a
general purpose single-chip microcomputer. The 8-bit 3050AH is compatible
with the software and architecture of the
8048 and 8040. The unit contains 4K bytes
of program ROM, 256 bytes of data RAM,
27 1/0 lines, and an 8-bit counter timer.
It has an 11-MHz clock and can be ex-
panded with MCS-80 and MCS-85 periph-
erals. Two versions, 1 without ROM and 1
with EPROM, will be available soon, as
will the ICE-49A 11-MHz in-circuit emu-
lator. Intel Corp, 3065 Bowers Ave,
Santa Clara, CA 95051. Circle 369

16-bit micro with 1024K RAM
Black Box 3/60S is based on a high speed
16-bit 8088 microprocessor. The micro-
computer features 256K bytes of RAM,
expandable to 1024K bytes. RS-232 serial
ports operating up to 19.2k baud inter-
face the computer to 16 peripherals. In
addition, the unit includes an IEEE 488
interface operating at 800K bytes/s. An
integral 5 1/4 " Winchester disk provides
19M-byte unformatted data storage; a
5 1/4 " floppy stores another 1M byte. The
3/60S runs under MP/M-86 and supports
BASIC, COBOL, and Pascal, as well as
word processing, spread sheet, and data-
based application programs. Rair Micro-
computer Corp, 4101 Burton Dr, Santa
Clara, CA 95050. Circle 370

High speed process controller
The TM990 103, a 16-bit CPU in the TM990
series of microcomputer modules, allows
onboard expansion of 1/0 via 2 sockets.
Additional modules can provide such I/O
capabilities as speech synthesis, floppy
disk control, or EPROM programming.
Memory provides up to 80K bytes of
RAM and 32K bytes of EPROM. Memory
expansion platforms supply additional
memory in various combinations. Other
features are an 87-member instruction
set, onboard fault indicator, and hard-
ware debug panel interface. Prices range
from $1660 to $1830. Texas Instruments
Inc, Semiconductor Group, PO Box
401560, Dallas, TX 75240. Circle 371
Bit-slice/micro development system

The DS370 development system features 16 levels of trigger/trace control, symbolic debugging with user defined mnemonics, and time measurements for performance analysis. System uses an internally bit-sliced processor and an 80-bit wide, 4K-byte deep trace memory that offers 64k breakpoints. Controllable from user’s host system, it provides automatic test equipment capability. Downloading allows setup features like complex formats and mnemonic tables. Prices start at $11,000. Hilevel Technology, Inc, 18902 Bardeen Way, Irvine, CA 92715.

Circle 372

Touch-sensitive development system

Digitized CRT touch development system TK-1000 detects touch with an X-Y coordinate method. Features include transparent screen for installation on a CRT screen, LED position display, RS-232 communication port, and power supply. Screens are available in 12", 15", and 19" sizes. The system is microprocessor based and provides tools for application software such as word processing and graphics. Interaction Systems, Inc, 24 Munroe St, Newtonville, MA 02160.

Circle 373

Microcode development station

STEP-7/FITS firmware integration and test station supports all bit slices, high speed controllers, and digital signal processing circuits. Microprocessor designs receive realtime support (to 36-ns access times) from the station’s memory and ROM emulation. System emulates high speed memory, controls target system clock, and analyzes target’s logic state. The single-unit station has a full-sized CRT terminal, 3 serial 110 ports, and 6 slots (expandable to 10) for memory emulation and logic state analyzers. Two floppy drives and CP/M OS provide over 1.5M-byte storage. Prices range from $8500 to $60,000. STEP Engineering, 757 N Pastoria Ave, PO Box 61166, Sunnyvale, CA 94086.

Circle 374
Today's measure of a printer's performance goes beyond line speed and purchase price. The true test is print quality and cost-per-character operating expense. Porelon ink rolls, designed specifically for impact printer ribbon cartridges, will dramatically improve the number of quality impressions and greatly increase the life of every ribbon.

Better impressions, increased ribbon life. At less cost. That's what you'll get every time you design a ribbon cartridge featuring Porelon ink rolls.

Find out how simple it is to add this performance feature to your impact printers. For further information, call 615/432-4134, or write: Porelon, Inc., 1480 Gould Drive, Cookeville, Tennessee 38501.
Replacement for IBM 327X terminals

Scat X is plug compatible with IBM's bisync communications lines and can operate as an IBM 3278 terminal in either a standalone or cluster environment. The unit supports copy and addressable printers. It features a standard IBM 3278 typewriter-style keyboard, a 14" (36-cm) diagonal, high resolution, nonglare screen with tilt and swivel adjustments, and RS-232/RS-422 interfaces. One terminal costs $1995; versions for cluster use, which requires a terminal controller, cost $1295 each. Peripheral Technology, Inc, 14784 NE 95th, Redmond, WA 98052.

Circle 375

LOGMARS bar-code verifier

Designed to read bar codes complying with the Logistics Application of Automated Marking and Reading Symbols (LOGMARS) established by the U.S. Department of Defense, the Bar Code Verifier ensures that labels are bar-code readable and accurate. The handheld battery operated unit displays 16 chars at a time and scrolls up to 30 chars. Unit price is $595; rechargeable battery is optional. Digitronics, Div of Comtec Information Systems, Inc, 53 John St, Cumberland, RI 02864.

Circle 376

Improved screen speed display

An RS-232 version of The Genius display completes a full page, 57-line x 80-char screen in less than 3 s. The high resolution, flicker free monitor's interface functions up to 19.2k baud with all interface functions controlled by a Z80 microprocessor. Internal memory is 16K and provides buffering and an internal screen memory. The display operates at 100/120 V, 60 Hz or 220/240 V, 50 Hz. It is available with white, green, or amber phosphors and provides reverse video and flashing attributes. A 128-char interchangeable ASCII char generator is used; foreign language char sets are optionally available. Micro Display Systems, Inc, PO Box 455, Hastings, MN 55033.

Circle 377

Alphanumeric thermal printer

MAP-20SL series microprocessor compatible 20-col thermal printers operate over a -40 to 50 °C temperature range. One model operates on 110 or 220 Vac; another operates on 11 to 40 Vdc. Both feature RS-232-C and 20-mA current loop interfaces, logic-selectable baud rates from 75 to 9600, a 2-line/s print rate, a 96-char print set, programmable controls, a built-in self-test program, and electronic end-of-paper sensing. Both models measure 4.44" x 2.75" x 7" (11.28 x 7 x 17.8 cm). Memodyne Corp, 220 Reservoir St, Needham Heights, MA 02194.

Circle 379

Low cost OCR system

Optical character recognition (OCR) system, series 500, employs LSI for data recapture. System applications include remittance processing and inventory control by reading characters printed on inventory tags and computer generated invoices. Data, in a string of up to 80 characters, are entered with either a wand or slot reader and include a variety of fonts with programmable data formats. Standard model is priced at $1295. Caere Corp, 100 Cooper Ct, Los Gatos, CA 95030.

Circle 380

Touch-sensitive screens

Touch-sensitive monitor, compatible with Apple II, IBM PC, and others, features a screen divided into multiple transparent touch-sensitive areas. Monitor is available with a choice of 3 screens: green, composite color, and RGB. For use where fast data entry and response is required, such as data retrieval, building directories, and teaching aids, system provides 12" monitor, cables, cards, and Program-That Writes-a-Program software. Basic system sells for $1450; different configurations are $1550 and $1950. Touch Technology, Inc, 3 Church Cir, Annapolis, MD 21401.

Circle 378
Why is ROLM first to deliver the complete Ada® solution?

Because only ROLM delivers...
- a full 1982 ANSI Standard
  Ada compiler
- a complete Ada Development
  Environment
- a fully configured Ada Work Center
- a complete family of target
  Mil-Spec processors
- extensive hardware and software
  support
...And it's all available TODAY!

With ROLM's ADA/82 you start programming now using a compiler which fully implements the 1982 ANSI Standard and Mil-Spec 1815 (A).

ROLM's Ada Development Environment (ADE®) is an integrated set of software tools that provides configuration controls, user-friendly programming utilities, and general purpose application libraries. ADE also supports the creation of reusable application packages that preserve your long term software investment.

Powerful hardware to increase throughput. ROLM delivers a complete hardware configuration that will immediately support your application software development. The system centers on the powerful MSE/800, a 32-bit super-mini-computer with 2 MB of main memory (expandable to 8 MB) and 8 ports for interactive Ada development terminals (extendable to 128).

Target processors to meet any application. Ada application programs developed on the ROLM Ada Work Center are easily transported to a wide range of ROLM 16-bit and 32-bit Mil-Spec processors.

Now, it's your turn to be first. Ada is happening now...and now is the time to gain a competitive edge by becoming immediately productive in Ada. If you want to lead the market in Ada Program Development, there is only one complete solution. The ROLM Ada Work Center. Don't wait, call or write:

One River Oaks Place, MIS 110
San Jose, CA 95134 (408) 942-8000

ROLM GmbH, 6052 Muehheim/Main, Muehheimer Strasse 54, West Germany. (06108) 60935

ROLM U.K. Limited, Catherine House, 63 Guildford Road, Lightwater, Surrey GU18 5SA, England. (0276) 76363

®Ada is a registered trademark of U.S. Department of Defense
ADE is a trademark of ROLM Corporation.

CIRCLE 127
20 major capabilities together for the first time on a single SMD controller!

- TRUE DEC implementation and media compatibility
- Switch selectable auto-configuration
- Data capacity up to 1,024 gigabytes (formatted)
- TRUE SMD interface (standard drivers and receivers)
- Emulates RM02, RM03, RM05, RK06, RK07
- Mixes emulation modes on a single Unibus controller
- Compatible with all major Operating Systems—DEC and others (uses standard drivers—no patches required)
- DEC diagnostic compatible
- Disk sector buffering (no “data lates”)
- Automatic self-test upon power up
- Built-in bootstrap loader
- DMA throttle - no inter-leaving required
- 16, 18, 22-bit addressing
- TRUE media compatibility
- TRUE DEC ECC/CRC implementation
- Multiple word size block transfer
- Up to four physical drives per controller
- Up to eight logical drives per controller
- Standard DEC media defect flagging
- Standard DEC device addressing, interrupt priority and interrupt vectoring—others can be user selectable
- Maximizes disk data transfer rate for any bus bandwidth (grows with technology)

Sometime a picture isn’t as good as 10,000 words.
New Dimensions In Time & Frequency

Now a Unique concept in benchtop/portable instruments
Global Specialties' New Handheld Model
5000 COUNTER-TIMER

Designed for both laboratory and field operation, the Model 5000 is sophisticated enough to handle virtually all your Time and Frequency measurement needs.

BIG ON VALUE...FEATURES & PERFORMANCE. The only things small about the Model 5000 are its SIZE (7.60 x 3.75 x 1.72 inches) and PRICE...at only $349.95 can you afford not to have one? In stock now and ready for delivery...call us TOLL FREE to find out how to get your Model 5000 today!

- Measure Frequency, Period and Pulse Width
- Full input signal conditioning
- Battery or Charger/Adapter operation
- Unique automatic master reset logic
- High contrast 0.43 inch, 8 digit LCD display
- LCD indicators: Overflow, Gate Open, Low Battery
- Display storage function maintains last reading

SPECIFICATIONS

Input: BNC
Impedance: 1MΩ @ 25pF in all modes
Sensitivity: 30 mVRMS — 1 kHz to 30 MHz
50 mVRMS — DC to 50 MHz

Modes:
Frequency: .1 Hz to 50 MHz (gate times 0.01, 0.1, 1.0, 10 s)
Period: 50 ns to 10 s (1, 10, 100, 1000 cycle averages)
Pulse Width: 25 ns to 10 s (1, 10, 100, 1000 cycle averages)

Full Signal Conditioning:
Coupling: AC or DC switch selectable
Attenuation: x1, x10, x100 switch selectable
Polarity: +/− edge Freq. & Period; >/< trigger level, Pulse Width

Trigger Level: variable 0 ± 500 mV x attenuator setting

Time Base: 10 MHz crystal oscillator (± 4 ppm, -40°C.)

Controls:
Power / Test/On, Mode, Gate
Time/Cycles Averaged
Display-Norm/Hold, Trigger Level, Polarity, Coupling, Attenuation

Power: 6AA Cells (Nicad or Alkaline) 10 hrs continuous operation Optional AC Charger/Adapter

Dimensions: 7.60 x 3.75 x 1.72 inches, (193 x 95 x 44 mm)
Weight: 14 oz., (397g), without batteries
Alphanumeric impact printer

The NAP-16-I line of panel mounted printers provides hardcopy output for test equipment, data loggers, multiplexer station message repeaters, and other industrial and laboratory applications. Operating at one 16-col line/s, the printer achieves a speed of 500k-operation mean cycle before failure. Wire-impact printing mechanism forms 5 x 7 dot matrix chars on plain paper using a single-color (purple) ribbon cassette. Stepper mechanism provides 7-line/in spacing. Prices start at $395. Keltron Corp, 225 Crescent St, Waltham, MA 02154.

Circle 381

Terminal conversion system

Microprocessor based terminal converter, TC3278, allows IBM 3278/3278 terminals to retain all regular features while adding local computing. Local system offers development and application software, data storage devices, and communication operating system and utilities. Single-board microprocessor provides 64K RAM, 3 async serial ports, and 2 coaxial interfaces for the 3278 and 3274/3276 cluster controllers. Storage is available in single or dual floppy drives for 1.6M bytes or in a diskette and Winchester combination for 5M, 10M, or 20M bytes. The system is priced from $1995 with quantity discounts available.

3R Computers Inc, 18 Lyman St, Westboro, MA 01581.

Circle 382

15" monochrome CRT

Complementing its manufacturer's line of 5", 7", 9", 12", and 14" diagonal models, a 15" diagonal monochrome CRT display extends horizontal operating frequencies to 24 kHz, compared to a 19.2-kHz max rating for the manufacturer's similar units. Offered in portrait or landscape versions, the CRT offers an optional range of switching power supplies and custom designed, injection-molded cabinets to accommodate a variety of customer logic board designs; users can also choose from several phosphors and face treatments. Zenith Radio Corp, 1000 Milwaukee Ave, Glenview, IL 60025.

Circle 383

Dual BIFET switch

The SW05 is a dual single-pole, single-throw monolithic BIFET analog switch that enhances the DG200 CMOS device by providing improved performance and a lower max VERROR = 10 uV (IDON x RON) at 125 °C. With fast switching speed guaranteed for 25 to 125 °C, SW05 can operate from dual- or single-power supply systems. TTL input compatibility with 400-mV noise immunity is guaranteed. In 100-piece quantities, the SW05BK (military) is $8.20, SW05FK (industrial) is $2.75, SW05CP (commercial plastic) is $2.50, and SW05BK 883 (improved military grade) is $11.05. Precision Monolithics, Inc, 1500 Space Park Dr, Santa Clara, CA 95050.

Circle 387

DC motor driven blowers

Series WBM-570 includes integral brushless dc motor drives and a 1-, 2-, or 3-stage backward-curved centrifugal fan configuration in a 5.7" (14.5-cm) diameter package. The blowers are designed to equal or surpass performance of 9.5" (24.1-cm) diameter blowers. Units achieve vacuum performance to 28" (71 cm) of water at 0 cfm. A variable 12- to 42-Vdc voltage controls speed. Blowers come with an 8-conductor ribbon cable lead and can be face-mounted in any position via 3 tapped mounting holes on a 4" (10-cm) circle. Double ball bearings provide quiet operation and long life. Ametek, Inc, Lamb Electric Div, 627 Lake St, Kent, OH 44240.

Circle 388

Mini slide switches

Instrumentation grade slide-actuated miniature switches, the k series features a potted/sealed base and terminals that allow the switches to be PCB mounted at the same time as other components for wave soldering processes. The switches are rated from 10 mA/5 Vdc through 2 A/250 Vac, depending on specified contact. Options include actuator location and size, contact type, terminal spacing, single and double circuitry, and several switch functions. An optional clear plastic cover inhibits accidental operation and provides dust protection.

Crouse-Hinds® Co, Arrow Hart Div, 103 Hawthorne St, Hartford, CT 06101.

Circle 389
Now you can build in seconds what used to take forever.

If you have been waiting to view your solid models, your waiting days (or even minutes) are over. Now there's SOLIDVIEW™. A revolutionary, new display technology for viewing solid models that significantly increases system speed. And significantly decreases host overhead, software development time, and total system cost.

By processing tasks like hidden surface removal, visible surface shading, sectional views, contouring, and even piercing objects, SOLIDVIEW slashes image construction time from minutes to seconds. The host is then free to handle viewing transformations and clipping concurrently; system throughput is greatly improved.

What's more, SOLIDVIEW constructs images using polygons instead of pixels. These images are built piece by piece, instead of line by line. So you not only get more speed; but more information.

You can also do more with SOLIDVIEW. You can add new parts without redrawing the entire screen. You can manipulate objects with a minimum of recalculating. You can make exploded or sectional views in seconds. You can even use translucent shading to see behind surfaces.

SOLIDVIEW is available in two models, with a wide array of features. Both offer you 12 x 24 color lookup table, 19" monitor, and the power required to view your images interactively for the first time. Options include pan/zoom, four overlays, hardware cursor, serial interface, and a selection of peripherals.

SOLIDVIEW from Lexidata. It's so fast, it will completely change the way you view your solid images. For fast and interactive response to all your questions, just call us at (800) 472-4747. Or write to us at 755 Middlesex Turnpike, Billerica, MA 01865. TWX 710-347-1574.

LEXIDATA
The clear choice in raster graphics.
Low noise amplifier
Four-channel monolithic Model TRA403 amplifier achieves a 330-mV/µA gain and a 7-ns response time. The device operates on less than 25 mW/channel and maintains noise levels under 25 nA rms. Amplifier comes in 20-pin DIP or 18-pin LCC configurations; PCB-mounted version facilitates evaluation and prototyping. The unit suits amplification of small current pulses obtained from low capacitance devices (20 pF or less) and can be used with solid state radiation and light detectors. Price is $35. LeCroy Research Systems Corp, 700 S Main St, Spring Valley, NY 10977. Circle 390

Axial Schottky rectifiers
USD120, USD130, and USD140 Schottky devices come in the same axial-leaded plastic packages as IN5817, IN5818, and IN5819 rectifiers. Compared with IN5817 devices, however, the USD models offer 250-mV lower forward-voltage drops, higher op temps (150 vs 125 °C), and a higher surge current rating (50 vs 25 A). Among other applications, the rectifiers can serve as freewheeling or polarity-protection diodes in low voltage, high frequency inverters. 1000-piece prices range from $0.59 to $0.74. Unitrode Corp, 5 Forbes Rd, Lexington, MA 02173. Circle 391

Pressure transducer
Model 1518 comes in 13 pressure ranges from 0 to 300 psi (gauge, differential, or absolute). Std features include infinite resolution, low power consumption, ±0.5% static error band (BSL), and long-term stability. Unit operates from choice of 4 regulated dc supplies with 3 options for high level dc output. Robinson-Haipera, One Apollo Rd, PO Box 248, Plymouth Meeting, PA 19462. Circle 392

Low cogging dc motors
Low cost size 20 motor series features highly permeable 11-slot laminations to minimize cogging and electrical noise. High torque to inertia ratio and low self-inductance ensure quick response. Diamond turned commutators, lubricated double-shielded ball bearings, die-cast aluminum end bells, and totally enclosed carbon steel housings are used. Motors are 100% run-in and tested to ensure proper brush/commutator seating and use UL recognized materials. Twenty std size 20 models, with several stack lengths and choice of replaceable or nonreplaceable brushes, are available. Harowe Servo Controls Inc, a sub of Bowman Instrument Corp, PO Box 547, West Chester, PA 19380. Circle 393

Compact transformers/inductors
A series of compact single-hybrid transformers and feed-bridge inductors includes models in two configurations. Larger transformer versions feature an above-board height of 0.8" (2 cm) and handle 120-mA max loop currents, with a balance of 28 to 31 dB at 1 kHz. Smaller transformer versions are 0.52" (1.32 cm) high and handle 0.5-mA maximum loop currents, with a 27-dB balance at 1 kHz. Std feed-bridge inductors are available in both sizes. Prem Magnetics, Inc, 3521 N Chapel Hill Rd, McHenry, IL 60050. Circle 394

INTEGRATED CIRCUITS

Printer-controller chip
Designed to work with Matsushita/National/Panasonic E140-10 series electro-sensitive dot matrix printer mechanisms, Model A10EC printer-controller chip accepts Centronics-type parallel and RS-232-C serial TTL-level data inputs. It provides motor and head control for any E140-10 unit and can control printing of 24 cols. Chip includes inputs for paper-feed control and self-test. The manufacturer also offers a single-board configuration, the A10EB, that includes the A10EC chip. Able Systems Ltd, Unit 3, Kingfisher Ct, Northwich, Cheshire CW9 7TU, England. Circle 395

Octal logic circuits
Five circuits have been added to the line of locally oxidized CMOS (LOCMOS/isoplanar) devices: an inverting (HEF40242B) and a noninverting (HEF40244B) buffer chip, an asynchronous bus transmitter/receiver for 8-bit parallel 2-way communication between buses (HEF40245B), a transparent latch chip (HEF40373B), and a D-type flipflop for use with an 8-bit positive-edge-triggered storage register (HEF40374B). They are pin and function compatible with their TTL equivalents, with TTL compatible 3-state outputs. Circuits tolerate a 3- to 18-V operating voltage range and typically dissipate less than 400 mW. Propagation delays range from 30 to 85 ns, depending on supply voltage. Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Circle 396

Batteryless nonvolatile RAM
Combining CMOS semiconductor technology with std bus compatibility, the NVR8020 nonvolatile RAM memory board contains 1K to 4K bytes of memory. Board applications include industrial control, data acquisition, instrumentation, and security access systems; maintenance-free, no-battery design provides reliability. Suited for systems where online data need to be stored, accessed, and changed, the memory board is priced at $250 in 100-unit quantities with additional discounts available. Styntec Systems Inc, Flowerfield Bldg 1, St James, NY 11780. Circle 397

Switched-mode power supply ICs
Series 8160 ICs can be voltage sourced (18 Vdc max) or current sourced (30 mA max). They contain temperature-compensated reference, sawtooth-waveform generator, pulse-width modulator, and output driver. Housekeeping functions include low and high voltage protection, loop-fault protection, and current limiting and double-pulse protection. Other features are maximum duty cycle adjustment, feed-forward control (duty cycle is inversely proportional to input voltage), and remote on/off switching. Sprague Electric Co, sub of GK Technologies, 555 Marshall St, North Adams, MA 01247. Circle 398

Nonvolatile EPROM
Electrical programmability, UV erasability, and 256k-bit capacity describe the 27256 EPROM. Device is designed for use in industrial control, telecommunications, and other applications where occasional program changes are needed. EPROM programming is accomplished through a fast algorithm that checks each bit in sequence. Memory is organized into 32k bytes, allowing the programming voltage to be reduced to 12.5 V. EPROM sells for $131.10 in 10k quantities. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Circle 399
Run Intel’s Software on the IBM Personal Computer

If you use Intel’s Series-III MDSs to develop software for 8086, 8087, 8088, 8089, 80186 or 80286, you will be excited to hear about ACCESS. ACCESS is a software package that allows the IBM PC to run Series-III software. This includes PLM86, ASM86, PASCAL-86, FORTRAN-86, LINK86, LOC86 and LIB86.

ACCESS combined with an IBM PC and a hard disk gives you additional development systems for one fourth the price of a Series-III MDS—WHAT SAVINGS!

ACCESS will also run on other IBM compatible computers such as the COMPAQ portable computer. It is available for both MS-DOS and CP/M-86 operating systems.

ACCESS combined with your Intel software and the IBM PC provides a complete development package. ACCESS provides you with a Series-III operating system simulator (UDI) and a data link program for transferring files between the IBM and Intel systems. Our optional APXLOD software controls Intel’s SBC-957 debugger from the IBM PC.

ACCESS and the IBM PC with a hard disk are also faster than a Series-III with a hard disk.

Call Genesis Microsystems today to order your ACCESS software.

Genesis Microsystems
(415) 964-9001
P.O. Box 70280 • Sunnyvale, CA 94086
TELEX NO. 171618 MSG SNDR SNJ

IBM is a trademark of IBM Corp.
Intel is a trademark of Intel Corp.
Tell me how to drive bipolar stepper motors in less space, at half the cost.

The L297 and L298 monolithic ICs from SGS may be the total solution to your bipolar stepper motor drive requirements. In fact, the L297/L298 combination provides all necessary interfacing functions between microprocessors and fractional horsepower bipolar stepper motors without additional active components. Applications include carriage control and daisy wheel positioning in printers and head positioning in disk drives.

The L297 Stepper Motor Controller
The L297 needs only clock and direction input signals to generate the four phases required to drive the motor. The L297 features full or half-step modes, with 2 steps per clock pulse possible in the full step mode. The device accepts input commands for clockwise or counter-clockwise operation. In addition, a home signal is generated to detect when the motor is in the home position.

The L298 Multiwatt® Dual H Driver
The L298 is a dual full-bridge driver in SGS' popular Multiwatt® packaging. It effectively replaces 8 power transistors (2.5A each), inverter stages, resistors and other level-shifting components. The four phase signals necessary to drive the L298 can be provided by the microprocessor or the L297.

Cut Constant Current Drive Costs in Half
The L297/L298 combination can also be used with external sensing resistors to provide constant current drive to the motor. Normally, this requires a minimum of two additional ICs (gate and comparator packages). This function is also implemented in the L297 along with the four phase drive signals. By using the L297 and L298 instead of discrete devices, it is possible to cut installed circuit costs by as much as 50 percent.

L293 Dual H Driver
The L293 power amplifier can be used in place of the L298 for lower current, lower power motor drive applications.

Multiwatt® is a registered trademark of SGS-ATES Semiconductor Corporation.
Auto power-down ROMs
SY23128A and SY23256A ROMs are characterized by auto power-down controlled by a chip enable input (for power savings) and an output enable function to eliminate bus contention. Data are accessible in less than 200 ns. SY23128 and SY23256 are nonpower-down models with 3 programmable chip selects allowing multiple ROMs to be or-tied without external decoding. In 1k quantities, prices range from $6 for the 128K nonpower-down to $12 for 256K power-down version. Synertek Inc, 3001 Stender Way, Santa Clara, CA 95054. Circle 400

Fast 64K EEPROM
X2864A EEPROM writes 1 byte or a 16-byte page in 5 ms and operates from a 5-V supply. By internally latching addresses and data, the host system is free for a 5-ms write period. Write speed is 25.6k bps; read access time is 300 ns. Data-polling feature enables device to signal processor when write is finished, eliminating need for ready/busy signal and all write timing/verification hardware. Two-line control architecture ends system bus contention. Xicor Inc, 851 Buckeye Ct, Milpitas, CA 95035. Circle 401

Isolated feedback generator
UC1901 series features an amplitude modulation system that allows a loop error signal to be coupled with a small rf transformer. Diode demodulation achieves accurate, stable transfer characteristics, while the programmable, 5-MHz oscillator permits the use of smaller, less expensive transformers. Performance features include an internal 1.5-V reference accurate to within 1%, 4.5- to 40-V supply operation, and a high gain error amplifier. Unitrode Corp, 5 Forbes Rd, Lexington, MA 02173. Circle 402

High speed multiplier/accumulator
Sixteen-bit, 100-ns multiplier/accumulator (MAC) employs LSI technology for faster processing with less power. TDC1043 provides 35-bit double-precision internal accumulator and 19-bit extended precision output. Packaged in a standard 64-pin DIP, chip applications include array and image processors and interactive graphics. In 100-piece quantities, the MAC is $190. TRW, LSI Products Div, PO Box 2472, La Jolla, CA 92038. Circle 403

Voltage symmetry in DAC
Monolithic 11-bit (10 plus sign) DAC-210S provides ±10-V output, precision voltage reference, logic controlled polarity switch, and output amp. DAC offers sign magnitude coding, which gives an analog output of 0 V for a digital input of all zeros, and is unaffected by offset of gain drift. Chip operating temps for full-range analog values are within ±10 mV (±1 LSB) at 25 °C and within ±2 LSB at extreme temperatures. In 100-piece quantities, the DAC is $27.75. Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050. Circle 404

Fast Service On
Magnetic Tape Heads
For your design, Vikron tape heads offer superior performance with critical parameters such as crosstalk rejection, wear life and low core losses. Work with us on your design, prototype and production of heads for plastic cards, paper cards, magnetic strips and tape.

- CARD READER HEADS
- DIGITAL READ/RECORD HEADS
- GENERAL DIGITAL HEAD

Call (715) 483-3233

FREE HEAD SELECTION GUIDE

Name __________________________ Title __________________________
Company __________________________
Address __________________________
City __________ State __________ Zip __________
P.O. Box 737
520 Blanding Woods Rd. So.
St. Croix Falls, WI 54024
Phone (715) 483-3233
Telex 291099

VIKRON

CIRCLE 131
Technical applications computer

Model 36C, an MC68000 based computer, offers 4 graphics memory planes, gray scale, and a software accessible color map. Available with Pascal and BASIC, graphics language extensions enable users to program single lines for graphic images. Interfaces include HP-IB, RS-232-C, and 16-bit parallel, among others. Unit has 128K-byte RAM expandable to 640K bytes and is software compatible with other Series 200 products. Base price is $15,140; a configured system sells for $17,660. Hewlett-Packard Co., 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 405

Low cost multi-user minis

Series S Naked Mini 4/85 supports 32 users with access to 8M bytes of memory when paired with UNIX System III; with CARTOS, it supports 64 users. Memory cycle time is 650 ns; write access is 270 ns. Model 4-85 has 1M-byte virtual memory (expandable to 8M bytes), cache support, and 2 power supplies. NM4/85 costs $11,600. NM4/95 has been reduced over 50% to $13,690. Computer Automation Inc, 18651 Von Karman, Irvine, CA 92713. Circle 406

Voice recognition on single board

PVRT-100 voice recognition unit, in conjunction with host computer's mass storage, can recognize an unlimited vocabulary kept offline and downloaded. Online capacity is 100 words or phrases with a maximum utterance duration of 1.25 s. Data are entered by keyboard command or by voice instructions via headset or microphone. With applications in inventory control, robotics, password security, and CAD, the system is priced below $1300. Plessey Peripheral Systems, Distributor Products Div., 2632 Du Bridge Ave, Irvine, CA 92714. Circle 407

CAE workstations

A graphics workstation for CAE, the Idea 1200, offers a set of logic design, analysis, and documentation tools. System combines processing, simulation, and timing verification with a local network and distributed data base. With the system, users can design and document digital logic used in PCBs, VLSI, gate arrays, and standard cells. Consisting of 32-bit architecture, graphics display, 1.5M-byte program memory, and 34M-byte Winchester storage, the system, with applications software, is priced at $49,000 in quantities of 4 or more. Mentor Graphics Corp, 10200 SW Nimbus Ave, Suite G7, Portland, OR 97223. Circle 408

SOFTWARE

Graphics software

PLOT II Easy Graphing II is a graphing command language with interfaces for 2 user types. A conversational interface is designed for users performing iterative graphics tasks that require alterations. A second interface aids users with occasional graphics support requirements. Supporting both monochrome and color displays, software is available in FORTRAN source code for host mainframes, or in object code for Tektronix programmable terminals. Host version is priced at $2600 and can be used by an unlimited number of users, while the local version is priced at $310/copy. Tektronix, Inc, PO Box 1700, Beaverton, OR 97007. Circle 409

LISP version available

Using artificial intelligence techniques, Cromemco LISP is designed for robotics, CAD, and design automation. LISP features include fixed and floating point arithmetic, error-trapping capabilities, 150 utilities, Macro facilities, and a table-driven, user modifiable parser. Priced at $595, this version includes full documentation and choice of 5½" or 8" diskettes. Cromemco Inc., 280 Bernardo Ave, Mountain View, CA 94043. Circle 491

Monitoring and control software

With a modular set of standard and optional software, Maxpac is designed to monitor and control realtime industrial processes. The software uses preformatted tables that can define system parameters such as process variables, conversion factors, alarm thresholds, control loops, and digital inputs and outputs. Modular Computer Systems Inc (MODCOMP), PO Box 6099, 1650 W McNab Rd, Ft Lauderdale, FL 33310. Circle 492

C compilers for logic development

C compilers for HP 64000 logic development system support the 8086/8088, 68000, Z8001/Z8002, 6800/6802, and 6809 microprocessors. C programming permits closer interaction with the processor than with Pascal without sacrificing Pascal's language structure, readability, or ease of maintenance. The HP 64000 system linker enables the C compiler to pass key information into the emulator analyzer to speed debugging. The linker also brings together relocatable object modules from assembly language or brings compiled C and Pascal into an executable program. Hewlett-Packard Co., 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 493

Macro assembler for 8086/8088

With performance level between that of a conventional assembler and a compiler, the ASMM7 relocatable macro assembler and linking loader processes the full structured assembly language specified by Intel for its 8086/8088 processors; the assembler also supports Intel's 8087 chip. The ASMM7L package adds a librarian utility program, and the assembler allows user-specified segment names, symbolic and relative addressing, forward references, and a disk-paged large capacity symbol table. Microtec, PO Box 60337, Sunnyvale, CA 94088. Circle 494

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.
A Switching Regulated Power Supply Catalog Designed For Designers.

We're designers, too. We know how time-consuming and confusing it is to jump from section to section in search of features, diagrams and specifications. That's why we designed this new 8 page catalog just for you – the design engineer. It's an ideal reference showing general information, specifications and dimensions, all in an easy-to-use format. No flipping pages back and forth. Now, each section contains all the information you need on one spread.

This brand new catalog is packed with information on the EVS, EVD and EVQ series of single and multiple output switching regulated power supplies from Power/Mate. These series are the top of the line, meeting or exceeding specifications according to UL, VDE, FCC, CSA and IEC. It's quality you can count on from a leader in the industry.

In this convenient catalog, you'll find the answer to your power supply needs. No searching. No time wasted. No questions left unanswered. Get your free copy today. Just call or write – our representatives are at your service.

POWER/MATE
THE PACESETTER IN SWITCHING POWER SUPPLIES
514 S. River Street, Hackensack, New Jersey 07601
(201) 440-3100

FINALLY!
Database management software
A database management and application development system for UNIX and IBM PC, Contel Tools includes programs for various business applications. Four modules within the system handle data storage and entry, and supply report writer and menu system functions. Included are utilities for updating and modifying files. Available separately are a set of accounting modules. The data entry forms allow flexible design and automatic editing. Contel Computer Corp, 4204 Meridian St, Bellingham, WA 98226.
Circle 495

X.29 software support
Using a single-sync communication line, the X.29 networking facility ties remote terminals to host computers. A dial-up line per terminal sends traffic to appropriate host in a single message stream. Terminals can also be concentrated locally in a packet assembler/disassembler with either public or private connections. Network conforms to CCITT X.3/X.29 standards. X.29 software license is $1000 with an X.25 license as a prerequisite. Stratus Computer, Inc, 17 Strathmore Rd, Natick, MA 01760.
Circle 496

Software integrates proNET and DECnet systems
Ringway software unites DECnet software with multi-access local area network proNET. System provides networking capabilities including file transfer, remote file access, remote job submission, and remote log-in. Hardware and software combination offers 10M-bps throughput, less delay, and decreased memory requirements as packets are sent directly to their destination host. Fiber optic links are available for long distance use. Proteon Associates, Inc, 24 Crescent St, Waltham, MA 02154.
Circle 497

July Preview—Watch for a major staff-written review on workstations for computer aided engineering.

CONTROL & AUTOMATION

Programmable robotic system
Industrial tasks can be automated with the 7540 manufacturing system, which includes a microprocessor based controller and a servo-controlled jointed arm. Control unit stores 5 multiple point routines. The arm is capable of 4-direction movement—horizontal arc of 200° and 160° for X-Y axes motion, 100-mm Z-axis motion, and 180° wrist-like motion for the gripper/tool. System is programmed with an IBM PC using AMI/Entry version 2 which features a menu system, editor, and compiler. Price for the 7540 is $37,000 with quantity discounts available. IBM, Advanced Manufacturing Systems, 1000 NW 51st St, Boca Raton, FL 33432.
Circle 498

16-output programmable controller
Self-contained model 2020 features branching, counting, and timing capabilities. It executes up to 256 steps, each step having an output status and 1 or more instructions for leaving the step. The sequential program has a 1-to-1 correspondence with the machine it controls. Other features include 24 general purpose inputs, 4 dedicated inputs, full opto-isolation, and internal switching power supply. Control Technology Corp, 82 Turnpike Rd, Westboro, MA 01581.
Circle 443

INTERCONNECTION & PACKAGING

Fiber optic connector
Eliminating the grinding and polishing associated with conventional connectors, Simplex fiber optic connectors assemble without special tools. The all-aluminium units screw in to achieve fiber-to-fiber attenuation less than 2 dB. Compatible with 100- and 140-μm fiber cables, the connectors suit point to point or fiber to fiber splicing terminations. Per-unit cost is $7.50. Mohawk Cable Co, Optical Group, 9 Mohawk Dr, Leominster, MA 01453.
Circle 444

Multibus-compatible extender card
Version R includes 14 AWG vertical steel rails to support extended cards during system testing and troubleshooting. A stiffener bar allows 0.5" (1.3-cm) component heights on extended boards; nylon card guides enable smooth insertion and extraction. A solid groundplane on the board's backside reduces crosstalk; all system bus signals are distributed on the front. Solder mask on both board sides helps prevent shorts. Prototek, Inc, PO Box 46512, Cincinnati, OH 45246.
Circle 445
How to get a lot more color for your money.

Introducing the HP 2627A Color Graphics Terminal.
Now you can have a bright, sharp image that's easy to read. For only $5,975. Which means our compact new color graphics terminal is setting completely new price/performance standards.

You get 8 basic colors, plus hundreds of additional user-defined ones. Including colors that match our plotter pens. On a black screen with 512 x 390 line resolution. You get raster display technology for fast, selective screen updates. You get vector graphics and polygonal area fills, a combination that makes it easy to create complex shapes, symbols, and even typestyles. In a lot less time. With a lot more precision.

Of course, it's also software-compatible. In addition to HP's DSG/3000 and Graphics/1000-II software, the 2627A runs PLOT 10 from Tektronix, SAS's SAS/GRAPH, Precision Visual's DI-3000 and GRAFMAKER, ISSCO'S DISSPLA and TELL-A-GRAF.

But that's not all; the 2627A has user-definable softkeys and graphics edit keys that make this one of the easiest-to-use terminals on the market. It even gives you complete alphanumeric capability. In a separate memory. So whether you're interested in business or technical applications, just return this coupon and we'll send you more information. Or call your local HP sales office. We're listed in the white pages.
TOSHIBA
BREAK THROUGH

OUR NEW 2Kx8 STATIC RAM
IS TWICE AS FAST AS ANY OTHER BYTE-WIDE.
HITTING SPEEDS TO 45ns.

Toshiba has the world's fastest
2K x 8 Static RAM. With speeds as fast as
45ns and other byte-wide units with power
consumption as low as 1µA, your range
of design options just got twice as wide as
before.

Our new TMM2018D provides
both high-speed and low-power features
with an access time of 45ns. This, along
with high density, explains why they’re
rapidly displacing bipolar devices.

All our high-speed NMOS and
CMOS 2K x 8's are designed for maximum
compatibility with microprocessor bus
structures.

In fact, ours were the first 16K
CMOS RAMs on the market. We designed
them for a maximum 1µA standby current.
Operating from a single 5V power
supply, our byte-wide RAMs are available in
a 24-pin package, DIP (.300” or .600”), flat
pack and a variety of other configurations.


If you’re designing cache memory, high-speed storage, hand-helds and other high-density memory applications, write for more information to Toshiba America, Inc., 2441 Michelle Drive, Tustin, CA 92680, (714) 730-5000. Or call your local distributor or sales representative.

Toshiba America broke the speed limit so there’ll be fewer design limitations for you.
Right-angle female headers
Double-row headers mate with 0.025 in² (0.161-cm²) posts on a 0.1" x 0.1" (0.3-x 0.3-cm) grid, and come in 2- to 126-contact configurations. Contacts are selectively gold plated or solder plated. Each header's dielectric body is made of glass-filled polyester and is unaffected by flow soldering or board cleaning solvents. Twin-beam redundant contacts furnish reliable performance, and the headers' solder tails are positioned by a notched insulator for easy insertion onto PCBs. AMP Inc, Harrisburg, PA 17105. Circle 446

Wrappable logic board
Multibus compatible Series 2200 board features a universal layout for 0.300", 0.400", 0.600", and 0.900" (0.762-, 1.016-, 1.524-, and 2.286-cm) spaced devices; it also includes a 68-pin JEDEC type A LCC socket with wrappable pins. Board capacity is 28 cols of 53 pins each. Edge connectors include one 86-pin model [two rows of 43 pins each on 0.156" (0.396-cm) centers] and one 60-pin model [two rows of 30 each on 0.100" (0.254-cm) centers]. Methodo Electronics, Inc, 7447 W Wilson Ave, Chicago, IL 60656. Circle 447

PCB connectors
A 2-piece PCB connector consisting of a receptacle assembly and a perpendicularly mounted pin assembly provides high density interconnection. Receptacle assembly employs box-type contacts with 4 areas of contact/connection; pin assembly is available with flow solder or compliant pins. Contacts are arranged in 2, 3, or 4 rows with 60 to 684 rows per connector. AMP Inc, Harrisburg, PA 17105. Circle 448

Tell us what you like
Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Batteries back up memories
Lithium batteries can be soldered directly into PCBs and deliver a rated 3 V for memory backup. Three flat types have rated capacities from 120 to 200 mA, continuous discharge current of 0.1 to 0.2 mA, and pulse discharge current from 3 to 5 mA. Two cylindrical batteries have rated capacities of 160 to 1k mA, continuous discharge current of 1 and 2.5 mA, and pulse discharge current of 30 and 70 mA. Sanyo Electric Inc, Battery Div, 200 Riser Rd, Little Ferry, NJ 07643. Circle 451

Voltage surge suppressor
Model DPC-Plus Spike-Spiker has 8 individually switched, 120-V, 15-A outlets divided into 2 banks of 4 outlets each. Six-stage common- and differential-mode voltage spike suppression starts at 131 V and responds within 1 ps; absorption capacity equals 174.5 J. A 5-stage inductive/capacitive series/parallel low pass network furnishes noise filtering in both common and differential modes. Kalglo Electronics Co, Inc, 6584 Ruch Rd, Bethlehem, PA 18017. Circle 452

Triple-output power supply
The ET30-3601 power supply, designed for microprocessor and CRT applications, can power 5" disks, small printers, and cassettes. The supply uses a 15-pin DIN41612 connector and provides 5 V at 5 A, 12 V at 0.7 A, and REI filter, and VDE 0871 level B noise specs. Standard features include input surge, short circuit and overvoltage protection, and a power fail detect circuit. With triple output, the power supply sells for $91 in 100-piece quantities. Bosichert Inc, 384 Santa Trinita Ave, Sunnyvale, CA 94086. Circle 453

50- and 100-W switches
ESP series switching power supplies include five models each at 50- and 100-W rating. They feature 100-kHz switching and input rfi filters to keep conducted interference within FCC specified limits. Std features include automatic current limiting, overvoltage protection, remote sensing, reverse voltage protection, soft starting, remote shutdown, and inrush current limiting. Input voltage is 95 to 130 Vac or 180 to 260 Vac; outputs include 5, 12, 15, 24, and 28 Vdc. Ripple and noise are 50 mV peak to peak; op temp range is 0 to 70 °C. Power Pac Inc, 32 Meadow St, South Norwalk, CT 06854.

POWER SOURCES & PROTECTION

Linear power for disk memory

Model CP687 open frame dc power supply can drive any std 8" or 5" floppy, Priam or Seagate 506 hard disk, Shugart SA1000 series and QIC tape streamer. Output voltages and currents are 5 Vdc at 8 A avg, 9 A peak; —5 Vdc at 2 A; 12 Vdc at 3.5 A; —12 V dc at 0.7 A; and 24 Vdc at 5.5 A avg, 7 A peak. Unit measures 10.88" x 3.88" x 5.5" (27.64 x 9.86 x 14.0 cm). Input voltages include 100/120/220/230/240 Vac, ±10%, 47 to 63 Hz. Power supply is designed for operation where adequate moving air is available. Unit price is $230. Condor Inc, 4880 Adohr Ln, Camarillo, CA 93010. Circle 449

Transient suppressor board
Transient suppressor board HT-1301-B, for OEM and industrial control applications, provides dissipating capacity of 300 kW/ms, response time of 5-ns rise/10-ns recovery, and an alpha factor greater than 60. Board features auto ranging for line voltage variations and auto adjust to clamp at 20% greater than line voltage peak. Unit operates on a standby current of less than 3 mA at 130 V and requires 2 power leads—a 110 to 130 Vac or Vdc and a 5-A external fuse. Available from stock, the board is priced at $172. Hi-Tech Systems, Inc, 3985 N State Rd 39, Lebanon, IN 46052. Circle 450

Tell us what you like
Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Circle 454
The ultimate tool for software debugging your real-time operating system! Loral Instrumentation's act® 1 with its unique interface eliminates diagnostic software while allowing the user to monitor the operating program execution in real-time.

Breakpoints, Stack, Trace, Disassemble, Change, Insert, Move, Save, Load, Display and even Memory Substitution are all features and commands that make the act 1 the most versatile computer analysis tool on the market.

And, it's easy to use! Loral's friendly man-machine interface is unsurpassed for speed and ease of operation. No accident or afterthought, this menu prompted English language control method has been developed through several generations of Loral Instrumentation's equipment.

Loral's act 1 gives you a real-time window into your computer.
Switchers for low voltage ICs

Model PM2496A type 33D100 switching power supply is a single-output offline switcher that provides 3.3 V ±10% at 100 A, making it suitable for 3.3-V (nominal) logic level devices. Regulation is ±100 mV over the full ac input range, load variations, 0 to 50 °C op temp range, and initial warmup. Overload, overvoltage, overtemp, and reverse voltage protections are featured. Std features are remote sensing, ac input fuse, and power loss holdup that maintains regulation for 30 ms after ac input loss. The supply meets UL478 and CSA safety standards and radiated emi according to VDE 0871B. With an external filter, it also meets VDE 0871B specs for conducted emi. Price is $508. Pioneer Magnetics Inc, 1745 Berkeley St, Santa Monica, CA 90404.

EEPROM power source

Compatible with EEPROM requiring 21 Vdc bias and operation, the VA 10.5-10.5 power source converts 5 V input to ±10.5 or 21 V with max current of 40 mA. Specs include noise of 50 mV ±10% at 23 °C, the instrument offers 10 Ms of 10 MHz or -55 to 85 °C. NEMA 12, water-tight, and meets European safety standards. Fully tested with 100% thermal performance is optional. Op temp range is 0 to 70 °C or -55 to 85 °C. NEMA 12, water-tight, and initial warmup. Overload, overvoltage, overtemp, and reverse voltage protections are featured. Std features are remote sensing, ac input fuse, and power loss holdup that maintains regulation for 30 ms after ac input loss. The supply meets UL478 and CSA safety standards and radiated emi according to VDE 0871B. With an external filter, it also meets VDE 0871B specs for conducted emi. Price is $508. Pioneer Magnetics Inc, 1745 Berkeley St, Santa Monica, CA 90404.

Switching power on open PCB

The AC8254 50-W multi-output switching power supply is suited for small microprocessor based systems running mixed logic applications that call for a multi-output supply to the Boschert XL53-350I. It meets regulation and transient response on the 5- and 12-V outputs. Series meets VDE, UL, and CSA requirements with outputs of 5 V at 6 A; -5 V at 0.6 A; 12 V at 2.5 A; and -12 V at 0.6 A. Unit size is 7.75" x 4.25" x 2" (19.69 x 10.80 x 5 cm). Features include short circuit and overvoltage protection, soft start, input emi filtering, 20-ms holdup, brownout rating, and user selectable 120/240 Vac. Price is $60. Summit Electronics, Inc, 750 S Sherman, Richardson, TX 75081.

65-W switching power

SX53-3501 is a fit, form, and function multi-output supply to the Boschert XL53-350I. It meets regulation and transient response on the 5- and 12-V outputs. Series meets VDE, UL, and CSA requirements with outputs of 5 V at 6 A; -5 V at 0.6 A; 12 V at 2.5 A; and -12 V at 0.6 A. Unit size is 7.75" x 4.25" x 2" (19.69 x 10.80 x 5 cm). Features include short circuit and overvoltage protection, soft start, input emi filtering, 20-ms holdup, brownout rating, and user selectable 120/240 Vac. Price is $60. Summit Electronics, Inc, 750 S Sherman, Richardson, TX 75081.

DATA CONVERSION

Differential absolute encoders

Scalable Series DDS90 encoders indicate the absolute difference between two rotating shafts with accuracies to 1 part in 3600. The devices convert any 2 shaft inputs to bcd or binary data, and -4-, 4-, and 5-digit, 0.5° (1.3-cm) high LEDs are available. Data outputs are TTL compatible; data transfer and data hold lines simplify computer interface. The basic data update rate is 2.5 ms; 600-μs performance is optional. Op temp range is 0 to 70 °C or -55 to 85 °C. NEMA 12, water-proof, and explosion-proof transducer housings are optional. Prices start at $595 per axis in unit quantities. Computer Conversions Corp, 6 Dunton Ct, East Northport, NY 11731.

Inductosyn-to-digital converters

Series SDC-19100 converts the slider outputs of Farrand Industries's Inductosyn devices to digital codes. With an lsi chip and hybrid construction, the units achieve 10-, 12-, or 14-bit resolution at ±21-, ±8.5-, or ±5.3-min accuracies, respectively. A Type II tracking loop design eliminates velocity lag when operating at or below the specified tracking rate (960 rpm for the 14-bit unit to 15,000 rpm for the 10-bit unit). Three-state latched outputs facilitate microprocessor interfacing. Other features include direction and count outputs and 1-LSB repeatability. ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Data acquisition system

The ANDS440 is a close-coupled, coprocessing multiloop system for regulating temp, pressure, voltage, and current in industrial environments. Compatible with RS-232-C or 2-mA serial port, the system provides fully isolated analog and digital i/o. There are 3 versions: prompt proportional/digital controller, prompt PID/digital controller, and basic PID/sequencing coprocessing controller. Plug-in cards are available to extend the system for both processing and programming. Analogic Corp, 14 Electronics Ave, Danvers, MA 01923.

Color-mapped video DACs

Compact RGB DAC 4T, 8T, and 8E units combine 3 complete sets of video frequency DACs with color lookup table RAMS and associated logic and control circuitry. The 4-bit DAC displays up to 4096 colors and provides update rates to 40 MHz with a 5-ns settling time to 1 LSB. Eight-bit models have over 16.7M possible colors. The 8T operates at 70 MHz and the 8E at 135 MHz; both have an 8-ns settling time to 1 LSB. The 4T and 8T are TTL compatible; 8E is ECL compatible. Intech, Inc, Microcircuits Div, 2270 Martin Ave, Santa Clara, CA 95050.

High accuracy DAS

ICE-108A data acquisition and control system operates as a computer peripheral on the IEEE 488 bus. Accurate to 0.005% at 23 °C, the instrument offers 39,999-count resolution and a voltage range of 399.99 mV to 300 V. Floating bipolar differential input, 140-dB CMRR, ±300-Vdc CMV, and 90-dB NMRR are also featured. ADC performs 10 samples/s and 9.7 scans/s. Main chassis provides an integrating DVM and 8 plug-in boards, as well as addressing and data/control interfaces. Advanced Technology Research Laboratories Ltd, 5645K General Washington Dr, Alexandria, VA 22312.
Dataram has acquired Charles River Data Systems' DEC-compatible product line. We will continue to offer their popular FD-311 dual floppy subsystems and have added an exciting new floppy-based system, Dataram's A21.

Q-bus and UNIBUS compatible versions of the FD-311 provide dual RX02-compatible 8" floppy drives for $2,400. Our new 7" high A21 combines dual RX02-compatible 8" slimline floppies with an 8-quad slot Q-bus card cage for only $3,500. Both products are supported by the industry's widest range of LSI-11 compatible products. Call or write for details.
CONFERENCES

JULY 11-13—Computer Simulation Conf, Hyatt Regency Vancouver, Vancouver, BC, Canada. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 714/459-3888


AUG 9-11—World Congress on the Human Aspects of Automation, Univ of Michigan, Ann Arbor, Mich. INFORMATION: Pat Van Doren, Technical Activities Dept, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1060 X369

AUG 23-26—Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 13-15—Autofact Europe, Palexpo Conf and Exhibition Ctr, Geneva, Switzerland. INFORMATION: Automated Systems Assoc, Society of Manufacturing Engineers, One SME Dr, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500


SEPT 13-15—Midcon, O'Hare Expo Ctr and Hyatt Regency O'Hare, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Mini/Micro-Midwest, O'Hare Expo Ctr, Rosemont, Ill. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 13-15—Peripherals, Moscone Ctr, San Francisco, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, 355 E Touhy Ave, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

SEPT 13-15—WPOE (Word Processing and Office Environment Show and Conf), San Jose Conv Ctr, San Jose, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 19-21—Advanced Control Conf, Purdue Univ, West Lafayette, Ind. INFORMATION: Henry Morris, Control Engineering, 1301 S Grove Ave, PO Box 1030, Barrington, IL 60010. Tel: 312/381-1840


SEPT 20-21—Data Storage, Marriott Hotel, Santa Clara, Calif. INFORMATION: Cartlidge & Assocs, Inc, 4030 Moorpark Ave, Suite 205, San Jose, CA 95117. Tel: 408/554-6644

SEPT 26-28—Compcon Fall, Marriott Gateway, Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 26-28—Maecon, Kansas City Conv Ctr, Kansas City, Mo. INFORMATION: Jerry Fossler, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 29-30—CAD/CAM and Simulation Conf, Westin Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 619/459-3888

OCT 2-5—Robotech (Internat'l Conf and Exhibit for the Application of Automated Manufacturing Technology), Curtis Hixon Convention Hall, Tampa, Fla. INFORMATION: Tom Will, Latcom Inc, 4135 Laguna, Coral Gables, FL 33146. Tel: 305/667-5150

OCT 3-6—Data Communications Symposium, Cape Cod, Mass. INFORMATION: Kenneth J. Thurber, Architecture Technology Corp, PO Box 24344, Minneapolis, MN 55424. Tel: 612/935-2035

OCT 8-10—PC (Internat'l Exposition and Conf Featuring IBM Personal Computers and Compatabiles), Bayside Exposition Ctr, Boston, Mass. INFORMATION: Gerald A. Milden, Northeast Expositions, 826 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

OCT 10-13—ISA (Instrument Society of America) Internat'l Conf and Exhibit, Astrohall, Houston, Tex. INFORMATION: Philip Meade, ISA, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

OCT 12-14—Fiber Optic Communications Local Area Network Applications, Atlantic City, NJ. INFORMATION: Tom Coggleshall, IGI, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

OCT 18-20—Internat'l Test Conf, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Doris Thomas, PO Box 371, Cedar Knolls, NJ 07927. Tel: 201/267-7120

WORKSHOPS


AUG 8-18—Data Communications, Iowa State Univ, Ames, Iowa. INFORMATION: Paul Bond, 131K Cooper Hall, Iowa State Univ, Ames, IA 50011. Tel: 515/294-1526

July Preview—Watch for a major staff-written review on workstations for computer aided engineering.

If you've outstripped your 256 kbyte addressing capability, if you want a reliable solution to your memory expansion needs, and if budget is a concern, we have the answer. We have made life on the Q-Bus a lot easier. QNIMAP, another outstanding Q-Bus product from Able Computer, allows for full memory expansion up to 4 megabytes of main memory and the use of existing Q-Bus DMA devices. With QNIMAP, you get system performance you never thought possible along with complete support from Able. The QNIMAP consists of two easy to install dual width boards and is software compatible with RSTS/E, RSX-11 and UNIX.

If you have other Q-Bus needs, Able has many exciting products:

- **QNIVERTER** – Bi-directional Q-Bus to Unibus/Unibus to Q-Bus signal converter for memory and peripheral devices.
- **UNIMAP** – Memory expansion to 4 megabytes on the PDP-11/23. Allows use of 18 bit Unibus devices.
- **INTERLINK** – DMA interprocessor link between two Unibus, two Q-Bus, or one Q-Bus and one Unibus system.

Find out more about QNIMAP and the rest of our Q-Bus products. Write or call for details. Able Computer, 1732 Reynolds Avenue, Irvine, California 92714. National offices: Irvine CA (714) 979-7030, Burlington MA (617) 272-1330, Rumson NJ (201) 842-2009. International offices: Canada (Toronto) (416) 270-8086, England (Newbury) (0635) 32125, W. Germany (Munich) (089) 463080. For immediate, toll-free information, dial (800) 332-ABLE.

Q-Bus, Unibus, RSTS/E, RSX/11 and PDP are trademarks of Digital Equipment Corporation. UNIX is a trademark of Bell Laboratories.
Thermocouple connectors
Handbook presents over 50 temperature measurement and panel connector systems. Omega Engineering, Inc, an Omega Group Co, Stamford, Conn. Circle 410

RF emission regulations
Booklet gives overview of standards for acceptable rf emission from electronic products in various countries; address and telephone numbers of 26 regulatory agencies around the world are listed. Sierracin/Power Systems, Chatsworth, Calif. Circle 411

LSI-11 data acquisition
Bus interface products for A-D, D-A, and digital data conversion are illustrated and specified in catalog that includes product selection tables. ADAC Corp, Woburn, Mass. Circle 412

Quality assurance
Manual documents basic procedures for manufacture and reliability monitoring of standard and custom-contract products; cross reference of MIL-Q-9858 and MIL-M-38510 requirements, in addition to flowcharts for MIL-STD-883 method 5004 class S, B/JAN 38510, and c qualifications, are included. Precision Monolithics, Inc, Santa Clara, Calif. Circle 413

Printer selection
Guide profiles a variety of 27- and 40-column models, outlining printer specs as well as controller, power supply, and mechanical subsystems for custom assemblies. Printer Products, div of Capitol Circuits Corp, Boston, Mass. Circle 414

Elastomeric keyboards
Wild Rover® KB series 3 x 4 keyboards are examined in spec sheet that sets forth features and applications as well as circuit and dimensional diagrams. Refac Electronics Corp, Winsted, Conn. Circle 415

Motor reference
Catalog gives complete specs and application data for off-the-shelf motors, gearmotors, and electronic motion controls. Photos and selection information tables complement dimensional drawings and text. Bodine Electric Co, Chicago, Ill. Circle 416

Small programmable controllers
Brochure details processor capacities, applications, specs, and diagnostics for EPTAK 210, 220, and 240 microprocessor based PCs; portable PLUG-A-PROM memory module is also described. Eagle Signal Controls, a Gulf + Western Co, Austin, Tex. Circle 417

Computer interference control
Booklet outlines typical applications for equipment isolators, ac power line filters/suppressors, line voltage regulators, and ac power interrupters. Electronic Specialists, Inc, Natick, Mass. Circle 418

Computer printers
Brochure introduces principal features and options of 9 models ranging from basic dot-matrix to 4-color multipurpose printers. Facit, Inc, Dataroyal Div, Nashua, NH. Circle 419

International telecomm support
Booklet describes features and operation of 300- to 16k-bps modems; time division, statistical, and data/voice muxes; local network products; and network management systems. General DataComm Industries, Inc, Danbury, Conn. Circle 420

Nonvolatile memory
Handbook provides detailed data sheets and application notes for electrically alterable memory ranging from an 82-bit EAROM to a 16K-bit word-alterable EEPROM and a 4K-bit nonvolatile static RAM. General Instrument Corp, Microelectronics Div, H Hicksville, NY. Circle 421

Surge protection and test
Introductory guide outlines circuit design and test techniques for countering transient voltage spikes and current surges, and examines IEEE 587 standard for ac power lines. KeyTek Instrument Corp, Burlington, Mass. Circle 422

Micro miniature D connectors
High density metal- and plastic-shell MIL-C-83513 connectors are specified in book that lists performance data/materials, cutout dimensions/contact arrangements, and mounting/coupling hardware. Malco, div of Microdot Connector Group, Montgomeryville, Pa. Circle 423

Switching power supplies
Booklet reviews state of the art design, along with measurement techniques, paralleling, load sharing, and switching supply applications. CEAG Electric Corp, Power Supply Div, Hauppauge, NY. Circle 424

Illuminated push buttons
Catalog describes switches, specifies electrical/mechanical ratings, and lists materials and finishes for 554 series; schematics, tables, charts, and selection guide are included. Dialight, a North American Philips Co, Brooklyn, NY. Circle 425

Semicustom Linear/digital ICs
Application note APN-30 describes how a high speed logic configuration can be implemented on bipolar semicustom chips primarily used for linear applications; APN-32 explains how to stretch the limited linear design capability available on metal gate CMOS digital array chips by using an MLA CMOS monochip. Interdesign, Inc, a Ferrari Co, Scotts Valley, Calif. Circle 426

Minicomputer DCE
Data communications equipment including data concentrators, data PBXs, local networking equipment, modems, multiplexers, and data sets are described in short-form ordering catalog. Micom Systems, Inc, Chatsworth, Calif. Circle 427

High density Euro connectors

Private communication networks
Tutorial brochure explains networking economics and technologies in available systems. Request on company letterhead from: Judith Allen, Harris Corp, Telecommunication Networks Div, PO Box 1040, Melbourne, FL 32901.

Fiber optic data cables
Brochure describes cables with 4 to 6 graded index fiber channels, as well as general purpose simplex and heavy duty duplex versions, tabulating performance/installation specs and attenuation ranges. Valtec, West Boylston, Mass. Circle 429
Bar-coded or alphanumeric labels, tickets, and tags...

1, 2, or 200 at a time.

The new Zebra™ Demand Printer offers unmatched flexibility. Unlike general-purpose printers, it delivers labels, tickets, or tags when and where you need them—in a form that's easy to use. It dispenses pressure-sensitive labels, either in strips or individually with the backing removed. It's ideal for tag and ticket printing, since it handles multipart forms and card stock up to .016" (16 point). And the Zebra saves you money because it doesn't require expensive thermal or pin-fed papers. There is no waste—you print only what you need.

The Zebra is a high-speed, bidirectional, dot-matrix printer that offers the complete flexibility to print nine different bar code symbologies (including LOGMARS) in 37 different sizes—all in specification—plus OCR and four sizes of alphanumerics. And you're free to change printing format with each printout, so the Zebra can meet a variety of printing needs.

The Zebra is a "smart" printer, too. Interface the Zebra with a basic ASCII keyboard or CRT and you'll have a complete label preparation system. Or input data from your computer via a standard RS-232C port.

The Zebra is built to last and is "ruggedized" to withstand industrial environments. Its unique harmonic drive motion significantly reduces vibration, giving you more accurate printing, with a print-head life rated at 300 million characters. You may have thought you couldn't cost-justify a bar code printer. But the Zebra is priced at less than half that of comparable printers, so you can conveniently set up one or more in your operation.

Find out how the Zebra can improve your information handling—call or write today.

Data Specialties, Inc.
3455 Commercial Ave.
Northbrook, Illinois 60062
(312) 564-1800
Telex 206230

CIRCLE 138
COMPUTER DESIGN ANNOUNCES . . .

the

GRAND PRIZE WINNER!

Stan Nackdymon wins the HP-85 in our Designer Preference survey prize drawing.

What about your chance to be a winner?

You can enter the prize drawing by finding, filling out, and returning the Designer Preference Survey questionnaire bound into your copy of Computer Design every month. Your entry goes into a monthly drawing for an HP 41C calculator. Winners are announced monthly. In addition, all entries are eligible for the Grand Prize annual drawing. The Grand Prize is an HP-85 desk top computer. See our monthly announcements for the features and details on the prizes.

Here's what you should look for

COMPUTER DESIGN

The only computer magazine that concentrates on design. The only design magazine that concentrates on computers.

Best of Luck!
The Premier Computer Graphics Conference

August 24-29
Detroit, Michigan

The 20th Annual Conference on Computer Graphics and Interactive Techniques

SIGGRAPH '83 is sponsored by the Association for Computing Machinery's Special Interest Group on Computer Graphics in cooperation with the Engineering Society of Detroit, the IEEE Technical Committee on Computer Graphics and Eurographics.

Plan now to attend SIGGRAPH '83.

SIGGRAPH '83 pulls together industry experts to present the year's most comprehensive computer graphics conference. There will be ample opportunity to see the latest software and hardware.

The full spectrum of graphics professionals is attracted to SIGGRAPH '83. Attendees are mandatory for professionals striving to keep their computer graphics knowledge up to date. For registration information, contact the SIGGRAPH '83 Conference Office, 111 East Wacker Drive, Chicago, Illinois 60601. If you plan to register on site in Detroit on Sunday, July 24, between 1 p.m. and 11 p.m., a public showing of computer-generated art will be made available.

A complete technical conference.

SIGGRAPH '83 offers a broad range of state-of-the-art courses on graphics and computer science. A technical exhibition will be held. The conference will also provide a forum for professionals to exchange ideas and experiences with their peers.

An equipment exhibition displaying the latest in research and innovative uses of computer graphics in industry.

A public showing of computer-generated art.

ACM/SIGGRAPH '83
**LITERATURE**

**Line printer maintenance**
Booklet examines major aspects of operation, summarizing how to keep units functioning well in an applications environment. Digital Associates Corp, Stamford, Conn. Circle 430

**Monitor/control systems**
Leaflet specifies Digistrip® IV and DigiLink IV, showing process diagrams of control features and applications. Kaye Instruments Inc, Bedford, Mass. Circle 431

**3-output dc-dc converters**
Technical data sheet gives electrical/mechanical specs for c series 9-W units, with application information, photos, and dimensional drawings. Stevens-Arnold, sub of Computer Products, Inc, South Boston, Mass. Circle 432

**Office automation planning**
Brochure reviews office automation strategy, from architecture and selection to implementation. McQuillan Consulting, Cambridge, Mass. Circle 433

**Motor controllers**
Brochure covers series 5600 programmable controllers, discussing capabilities as well as relay, timing, arithmetic, and sequencing functions. Gould Inc, Industrial Controls Div, Westminster, Md. Circle 434

**Network management**
Data sheets for remote sense/control and automatic calling units examine features, benefits, and technical specs; sample configuration diagram of each is included. Paradyne Corp, Largo, Fla. Circle 435

**Time dimension multiplexer**
Line drawings and photos illustrate brochure that describes applications and system operating principles of bit synchronous processors. Seipec Corp, Middletown, RI. Circle 436

**Factory automation**
Brochure reviews Loginet system, highlighting programmable controller networks designed to improve productivity; several applications examples are included. Logicon, Process Systems Div, Fairfax, Va. Circle 437

**6502/6522 measurement system**
Application note describes TSC7135 A-D converter interface to microprocessor based data acquisition and process control, including circuit schematics and hardware/software examples. Teledyne Semiconductor, Mountain View, Calif. Circle 438

**Miniature power supplies**
Single-, dual-, and triple-output models are examined with detailed specs and outline drawings for screw connections as well as logic/op amp pc board mounts. Acopian Corp, Easton, Pa. Circle 439

**Proving computer/controller**
Folder covers operating features, interfaces, and specs, in addition to system and application diagrams, for model 1010. Waugh Controls Corp, Chatsworth, Calif. Circle 440

**MIL-C-5015 connectors**
Catalog gives insert arrangements, conversion tables, dimensional drawings, and photos of connectors and assemblies. Crown Connector, Inc, San Fernando, Calif. Circle 441

---

**Memory Mapped Process Interfaces... The Missing VME Link.**

Monitek has found the missing link between today's microcomputers and industrial processes: M²π Memory Mapped Process Interface Subsystems. M²π places the system/process interface where it's always belonged: between processes and programs.

So for the very first time, programs "see" industrial processes as automatically mapped blocks of memory. And communications between programs and processes are handled by simple read and write operations.

With M²π, you'll free the CPU from database update chores. Simplify programming. End hassles with hardware. And have a stand-alone process interface subsystem that offers you single-point modularity, Eurocard design, and VME synergy. For full details, call or write us today. Monitek, Inc., Digital Systems Division, 1495 Zephyr Avenue, Hayward, CA 94544. Phone:(415)471-8300. © 1983, Monitek, Inc.

---

**Low Cost Subminiature Ball Slides**

LOW FRICTION, LOW INERTIA, PRECISION BALL SLIDES—preloaded to eliminate backlash and side play in head carriages and other reciprocating mechanisms in disk drives, printers, plotters, and copiers.

Hardened stainless steel balls roll on hardened way rods for long life without lubrication. Anodized aluminum bodies ground top and bottom. Stackable for XY positioning. Custom and special designs available.

Sizes start .23" high x .38" wide x .50" travel, capacity 2 lb. Linear accuracy .0005 inch/ inch. Repeatability .0001 inch most models.

COMPARE OUR PRICES —
Call (203) 775-4041 for 12 page catalog and price list. Popular sizes in stock.

**Del-Tron Precision, Inc.**

934 Federal Road, Route 7
Brookfield, CT 06804 (203) 775-4041

---

**Low Cost Subminiature Ball Slides**

LOW FRICTION, LOW INERTIA, PRECISION BALL SLIDES—preloaded to eliminate backlash and side play in head carriages and other reciprocating mechanisms in disk drives, printers, plotters, and copiers.

Hardened stainless steel balls roll on hardened way rods for long life without lubrication. Anodized aluminum bodies ground top and bottom. Stackable for XY positioning. Custom and special designs available.

Sizes start .23" high x .38" wide x .50" travel, capacity 2 lb. Linear accuracy .0005 inch/ inch. Repeatability .0001 inch most models.

COMPARE OUR PRICES —
Call (203) 775-4041 for 12 page catalog and price list. Popular sizes in stock.

**Del-Tron Precision, Inc.**

934 Federal Road, Route 7
Brookfield, CT 06804 (203) 775-4041
Join the innovators of electronic banking.

TTI, the company that introduced customer activated terminals to the banking industry, is leading the research and design of the electronic financial systems of tomorrow.

At Transaction Technology Inc., a research and development subsidiary of Citicorp, we've built a unique technical resource for systems design and implementation. This includes the industry's most sophisticated on-line financial transactions delivery system. We're developing new interactive network technology that promises to revolutionize global financial services as we know them. We continue to develop the most advanced information hardware/software projects anywhere in the country.

We need Talented Technical Individuals to work in the following areas in support of on-line interactive delivery systems.

- On-line Interactive Financial Applications
- Communication Hardware Development
- Communications — Networking, Protocols, Local Area Networks, Network Control
- Operating Systems, Tools, Data Bases
- Data Base Processor, Hardware Development
- Specialized Intelligent Terminal Systems Development
- Personal Computers Software
- Advanced Product Research & Development including symbolic manipulations and inference

Languages and Operating Systems currently in use include: Assembly, C, PASCAL, COBOL, COBOL, TAL, our own specialized operating system, UNIX, 0/532, Tandem, various IBM operating systems, CP/M and TOPS 20. These run on Tandem, various micro-computers, personal computers, Perkin-Elmer, IBM, VAX, DEC 2060 and Quotron equipment.

Ours is a special environment, reflecting our standard of commitment. Our project group orientation provides unusually flexible and attractive working conditions. Benefit packages befitting a financial giant. Financial services at reduced rates. Tuition reimbursement. As a fast-paced, expanding company, we offer fast-paced advancement with commensurate salaries. In short, we do everything to ensure that the most gifted and experienced innovators will find no better career opportunity anywhere in the electronic world.

To learn more about TTI and our career opportunities, send your resume to:

Professional Employment, Department 047
3100 Ocean Park Blvd.
Santa Monica, CA 90405

or: Professional Employment
477 Madison Ave., 8th Floor
New York, NY 10022

Equal Opportunity Employer
SOFTWARE PROJECT ENGINEERS

Build your career at General DataComm!

Dynamic growth and the addition of new projects have created the need for talented, innovative Software Engineers. Overall project responsibility will include the start-up design of real-time microprocessor firmware for state-of-the-art data communications equipment through product release to manufacturing.

You must have hands-on experience in interrupt driven and multi-tasking software written in assembler language. You must also be familiar with hardware and networking concepts. BSEE or BSCS required.

Grow professionally with an established leader in the data communications industry! We offer competitive starting salaries and excellent benefits including stock purchase and profit sharing. Please call, send resume or letter of interest to:

Michael Bleazczak
(203) 797-0711 Ext. 950

One Kennedy Avenue, Danbury, CT 06810
An Equal Opportunity Employer M/F/H/V

CIRCLE 140

Data Processing Hardware & Software Market Research Reports

Frost & Sullivan has recently published analyses and forecasts of the following data processing industry segments:

- **1160 Non-Intelligent Terminals (U.S.)**
  - Price $1,275

- **1092 Automation Systems (U.S.)**
  - Price $1,275

For free descriptive literature, including a detailed table of contents, check the above reports of interest.

- **Please call me I have questions about these reports**

Name & Title: ________________________________

Company: ________________________________

Address: ________________________________

City: __________________ State: __________

Zip: ________ Phone #: ________

Frost & Sullivan 106 Fulton Street
New York, New York 10038 (212) 233-1080

AD INDEX

Able Computer .............................................................. 245
James Brunton Advertising
ADAC ................................................................. 203
Blackwood Associates Inc
Advanced Micro Devices ............................................ 18, 19
Keye/Donnal/Pearlstein
Alps Electric (USA) .................................................... 24, 25
Industrial Marketing Associates
Altek Corp ............................................................ 81
Amdek Corp ............................................................ 35
George M Drake & Associates Inc
AMP ................................................................. 86, 87
Lewis & Gilman Inc
Ampex, Memory Products Div ................................... 148
Amphenol, an Allied Company ............................... 38, 39
Marstellar Inc
Andromeda Systems .................................................. 198
Aptec Computer Systems .......................................... 46
Jack Ramsey Agency
Aydin Corp ........................................................... 71
Gain Advertising
Bail Electronic Display Div ......................................... 31
Red Barron Inc
Bunker Ramo Corp .................................................. 214
James A Ford Advertising
Burr-Brown Corp .................................................... 107, 109, 111
Curt Anderson Corporate Adv Mgmt
Calcomp ............................................................... 45, 47, 49
Carroll Touch Technology ......................................... 256
Richard Newman Associates Inc
Central Data Corp ..................................................... 183
Fillman Advertising
Centronics .................................................................. 210
Cooper G/K
Cermekt ................................................................. 83
Schein ignorant & Associates
Chabin Corp ............................................................ 66
Marken Communications
Charles River Data Systems ....................................... Cover III
Chrislin Industries ..................................................... 14
Chrono-log Corp ..................................................... 220
Cipher Data Products ................................................ 69
Richter & Carr Communications
Columbia Data Products ............................................. 52, 53
g Hastings Advertising
Connor-Winfield Corp ............................................... 256
Control Data Corp ..................................................... 180
E H Brown Advertising Agency Inc
Dataram Corp .......................................................... 5, 243
Louis Zimmer Communications Inc
Data Specialties ......................................................... 247
Juhl Advertising Agency
Data Systems Design ................................................ 62, 63
Tycer • Fultz • Bellack
Data Technology Corp ............................................. 120
Peter Chope & Associates
Datavue Corp, an Intelligent Systems Co .................... 12, 13
The Marcus Group Inc
Del-Tron Precision Inc ............................................. 250
Technell Inc
Devry Institute, Bell & Howell Education Group .......... 58
Cunningham & Walsh Chicago Inc
Digital Equipment Corp ............................................. 88, 89
Schneider Parker Jakuc
Digital Equipment ..................................................... 163
Television Engineering
Digital Marketing Associates ................................... 213
Odiorne Industrial Advertising
Diversified Technology ............................................. 207
Electronic Solutions ................................................... 14, 30
Bowen & Associates Inc
<table>
<thead>
<tr>
<th>Company Name</th>
<th>Page Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fairchild Digital</td>
<td>118, 119</td>
</tr>
<tr>
<td>Abert Newhoff &amp; Burr Inc</td>
<td></td>
</tr>
<tr>
<td>Farrand Controls</td>
<td>208</td>
</tr>
<tr>
<td>Technell Inc</td>
<td></td>
</tr>
<tr>
<td>Frost &amp; Sullivan</td>
<td>252</td>
</tr>
<tr>
<td>Fujitsu Microelectronics Inc</td>
<td>152</td>
</tr>
<tr>
<td>Austin Associates</td>
<td></td>
</tr>
<tr>
<td>Futurenet</td>
<td>75</td>
</tr>
<tr>
<td>Courtney/Wilson Advertising</td>
<td></td>
</tr>
<tr>
<td>General Datacomm</td>
<td>252</td>
</tr>
<tr>
<td>Bernard Schank Associates</td>
<td></td>
</tr>
<tr>
<td>General Electric — DCPBD</td>
<td>150</td>
</tr>
<tr>
<td>Cabell Eanes Advertising</td>
<td></td>
</tr>
<tr>
<td>Genesis Microsystems</td>
<td>231</td>
</tr>
<tr>
<td>Genstar REI Sales Co Inc</td>
<td>257</td>
</tr>
<tr>
<td>Warr Foote &amp; Rose</td>
<td></td>
</tr>
<tr>
<td>Global Specialties</td>
<td>227</td>
</tr>
<tr>
<td>RPR Advertising</td>
<td></td>
</tr>
<tr>
<td>Gould, SEL Computer Systems Div</td>
<td>15</td>
</tr>
<tr>
<td>Group Shree Advertising Corp</td>
<td>193</td>
</tr>
<tr>
<td>GTGO Corp</td>
<td></td>
</tr>
<tr>
<td>Business Marketing Inc</td>
<td></td>
</tr>
<tr>
<td>Heavyside Industries Ltd</td>
<td>257</td>
</tr>
<tr>
<td>Hewlett Packard</td>
<td>237</td>
</tr>
<tr>
<td>Wilton Coombs &amp; Collett Inc Advertising</td>
<td></td>
</tr>
<tr>
<td>Hewlett Packard</td>
<td>50, 51, 59, 134, 135, 146, 147</td>
</tr>
<tr>
<td>Taliant/Yates Advertising Inc</td>
<td></td>
</tr>
<tr>
<td>Hitachi America Ltd</td>
<td>129</td>
</tr>
<tr>
<td>Broder &amp; Gazdag Inc</td>
<td></td>
</tr>
<tr>
<td>IBM</td>
<td>10</td>
</tr>
<tr>
<td>Geer, DuBois Inc Advertising</td>
<td></td>
</tr>
<tr>
<td>Ikegami Electronics USA</td>
<td>67</td>
</tr>
<tr>
<td>Bon Advertising Agency Inc</td>
<td></td>
</tr>
<tr>
<td>Ikier Technology</td>
<td>74</td>
</tr>
<tr>
<td>TECOM</td>
<td></td>
</tr>
<tr>
<td>Industrial Development Association of Cheyenne</td>
<td>257</td>
</tr>
<tr>
<td>Ray Lansing Advertising</td>
<td></td>
</tr>
<tr>
<td>Industrial Programming</td>
<td>33</td>
</tr>
<tr>
<td>Cooper-Cameron Inc</td>
<td></td>
</tr>
<tr>
<td>INMOS Corp</td>
<td>36, 37</td>
</tr>
<tr>
<td>Taliant/Yates Advertising Inc</td>
<td></td>
</tr>
<tr>
<td>Intel</td>
<td>98, 99, 141, 142, 143, 196</td>
</tr>
<tr>
<td>Chitai/Day Inc Advertising</td>
<td></td>
</tr>
<tr>
<td>Intecolor, an Intelligent Systems Co</td>
<td>123</td>
</tr>
<tr>
<td>The Marcus Group Inc</td>
<td></td>
</tr>
<tr>
<td>Kennedy Co</td>
<td>1</td>
</tr>
<tr>
<td>R L Thompson Advertising</td>
<td></td>
</tr>
<tr>
<td>Kontron Electronics</td>
<td>139</td>
</tr>
<tr>
<td>Galusha &amp; Associates</td>
<td></td>
</tr>
<tr>
<td>Kratos Display Systems</td>
<td>218</td>
</tr>
<tr>
<td>Lone Lord &amp; Schon</td>
<td></td>
</tr>
<tr>
<td>Lexidata</td>
<td>229</td>
</tr>
<tr>
<td>Humphrey Browning MacDougall Inc</td>
<td></td>
</tr>
<tr>
<td>Liebert Programmed Power</td>
<td>76</td>
</tr>
<tr>
<td>Marken Communications</td>
<td></td>
</tr>
<tr>
<td>Logical Devices</td>
<td>256</td>
</tr>
<tr>
<td>Loral Instrumentation</td>
<td>241</td>
</tr>
<tr>
<td>Bowen and Associates Inc</td>
<td></td>
</tr>
<tr>
<td>Lundy Electronics</td>
<td>55</td>
</tr>
<tr>
<td>Lundy House Advertising Agency</td>
<td></td>
</tr>
<tr>
<td>M/A Com Linkabit</td>
<td>253</td>
</tr>
<tr>
<td>Knott &amp; Meads Co</td>
<td></td>
</tr>
<tr>
<td>Matrix Electronic Systems Ltd</td>
<td>201</td>
</tr>
<tr>
<td>MDB Systems</td>
<td>224</td>
</tr>
<tr>
<td>Memorex OEM Group (a Burroughs Co)</td>
<td>185</td>
</tr>
<tr>
<td>The Advertising Co of Offfield &amp; Brower</td>
<td></td>
</tr>
<tr>
<td>Memory Protection Devices</td>
<td>220</td>
</tr>
</tbody>
</table>

We’re looking for people who don’t think straight.

If you’re the kind of person who is able to look around the corner instead of straight ahead, consider a career with Linkabit.

Linkabit is a leader in the design, development and manufacture of satellite and terrestrial communications equipment specializing in local communication networks, encryption, forward error correction and high speed modulation.

And the reason we are is that our people are very creative, free-thinking individuals who look beyond the obvious to find innovative solutions to the demanding problems of this industry.

To help keep new ideas flowing, we’ve made sure that all career paths at Linkabit are flexible. Our engineers, for instance, are assigned to projects depending on their interests and abilities. As one assignment is completed, new opportunities are made available in a variety of areas.

Utilizing the most advanced equipment available, we work on a number of diverse and complex projects which include MILSTAR terminals, video scrambling equipment, domestic satellite systems, modems, codecs, advanced processors and fault-tolerant systems.

We are currently seeking skilled individuals who possess applicable experience in the following areas:

- Software Design & Development
- Digital Circuit Design
- VLSI
- Communications System Design
- Software Support/Tools Development
- Thermal & Package Engineering
- Microprocessor-Based Systems
- Components Engineering
- Project Engineering/Program Management

Positions are available in San Diego, Washington, D.C. and Boston. Send your resume to: Dennis Vincent, M/A-COM LINKABIT, 3033 Science Park Road, Drawer 40138, San Diego, CA 92121.
AD INDEX

Microcomputer Systems ...................................................... 256
Micro Products .................................................................. 16
Quantum Communications ................................................. 12, 133
Micro Switch ..................................................................... 161
Momentum Computer Systems ..............................................
    The Advertising Co of Offield & Brower...........................
Monolithic Systems ........................................................... 90
    Dan Meinerz Graphics....................................................
Montek ................................................................................. 250
Imahara & Keep ..................................................................
Motorola Semiconductor Pdts ............................................. 100, 101
    Comm Ad......................................................................
Multiwire ................................................................. 57, 214
    Greenstone & Rabasca Advertising Inc..........................
NCR OEM Marketing Div .................................................... 77
    Reiser Williams DeYong................................................
NEC Electronic Arrays ....................................................... 157
    Ty Anderson Advertising .............................................
NEC Electronics ................................................................. 116, 127
    Giardini/Russell Inc....................................................
NEC Information Systems................................................... 29
    The Stratton Corp....................................................... 127
Nicolet Paratronics ............................................................. 65
    Nova Tran Corp............................................................
    Dewey Advertising Inc..................................................
Oliver Advanced Engineering .............................................. 256
Omnitech ........................................................................... 206
    Ad Mark.....................................................................
Oregon Software ................................................................. 44
    Dall and Dall Advertising............................................
Ozalid .................................................................................. 189
    Warner Bicking & Fenwick Inc...................................
Panasonic ........................................................................... 179, 215, 256
    Sommer Inc.................................................................
Phone I ............................................................................... 257
Plessey Microsystems ......................................................... 205
    Abert Newhoff & Burr Inc...........................................
Plessey Peripherals ............................................................. 167, 168, 173
    Abert Newhoff & Burr Inc...........................................
Porelon .............................................................................. 221
    Campbell-Mithun Inc..................................................
Power/Mate Co .................................................................. 235
    Spectrum Marketing Associates...................................
Qantex ................................................................................ 197
    Richard H Margulis/Marketing Comm...........................
Quadrex Corp ..................................................................... 102
    Cover IV.....................................................................
Ramtek .............................................................................. 102
    Pinné Garvin & Hock Inc.............................................
Raster Technologies .............................................................. 79
    Ketchum Advertising..................................................
Raymond Engineering ......................................................... 185
    Keiler Advertising....................................................... 185
Real-Time Computer Science Corp .................................... 211
    Recognition Concepts................................................
    RGMS Advertising.....................................................
    Rockwell International................................................
    Rolm...........................................................................
    NW Ayer Inc..............................................................
    McArthur & Associates..............................................
    Rosscomp Corp..........................................................
    LeAnce and Herbert....................................................
Scion ................................................................................... 97
    Business Marketing Inc...............................................
Seagate Technology ............................................................. 42, 43
    Lutal Battey & Associates.........................................
    Doug Gottshofer & Co Advertising.............................
Seiko Instruments USA ....................................................... 159
    Doug Gottshofer & Co Advertising.............................
Selenar .............................................................................. 125
    The Advertising Co of Offield & Brower...................
SGS ................................................................................. 232
    The Advertising Co of Offield & Brower...................
Shugart Associates ............................................................. 20, 21
    Chiat/Day Inc Advertising...........................................
Siggraph '83 .................................................................... 249
SofTech Microsystems .......................................................... 85
    LeAnce and Herbert...................................................
    Spectron Software......................................................
    Spectrum Control....................................................... 34
    Barickman Advertising Inc......................................
    Sprague Electric Co.................................................... 177
        The Harry P Bridge Co...........................................
Systems Research Laboratories ........................................... 190
    Tandon Corp............................................................. 26, 27
    TEAC................................................................. 115
    TVC Ads..................................................................
Tektronic ................................................................. 2, 8, 9, 40, 41
    Tektronic Advertising................................................
Teledyne Relays ................................................................. 257
    Michelson Advertising................................................
Toshiba America ............................................................... 238, 239
    Michelson Advertising................................................
    Transaction Technology............................................ 251
    Knott & Meads Co.....................................................
Unitronix ........................................................................... 219
    Advertising/Marketing Associates Inc....................... 219
    Universal Data Systems............................................. 127
    Dayner/Hall Advertising Inc....................................... 127
Vector Automation ............................................................. 131
    Versatron................................................................. 136
    Pallace Inc............................................................... 136
Vicom Systems ................................................................. 217
    Vikron of Northland Aluminum............................... 233
    M R Bolin Inc Advertising...........................................
    Visual Technology..................................................... 73
    Blackwood Associates Inc......................................... 73
    Western Digital.......................................................... 144, 145
        Larry Pao Design...................................................
    Western Peripherals.................................................... Cover II
        Darryl Lloyd Inc.....................................................
    Whitesmiths Ltd.......................................................... 209
        Industrial Marketing Associates................................
Wintek Corp .................................................................... 257
    Wyse Technology....................................................... 60, 61
    Ebey Utley & McManus Advertising...........................
ZAX Corp ......................................................................... 113
    Sales Management International Inc......................... 113
    Zilog................................................................. 95
        Pinné Garvin & Hock Inc........................................

254 COMPUTER DESIGN June 1983
LASER FOCUS 1983
BUYERS' GUIDE

The all-inclusive reference source for laser and fiberoptic products and services. The 18th annual edition includes hundreds of listings for equipment and components along with their technical specifications. Vendors and information sources are clearly indexed. Other features: vendor catalogs, general technical information, a reader information service system.

544 pages; $35. pp. CIRCLE 455

HOW TO ORDER:

15-DAY FREE EXAMINATION
(U.S. AND CANADA ONLY)
Simply circle the appropriate number(s) on the Reader Inquiry Card at the back of this magazine. Your book will be sent to you for your 15-day free trial. If you are satisfied, keep the book and an invoice will follow. Otherwise return the book by the end of the 15-day period, and owe nothing.

CIRCLE 455

TALKING COMPUTERS AND TELECOMMUNICATIONS
By John A. Kuecken

Turn here for the latest methods on speech digitization and reproduction. Talking Computers and Telecommunications covers fundamental engineering requirements for producing intelligible synthesized speech and shows how to produce computer-synthesized speech using Moser synthesis and Linear Predictive Coding techniques. You find invaluable data on telephony, tone detectors, the DTMF detector, and much more.

$26.50 CIRCLE 456

REAL-TIME COMPUTING
With Applications to Process Data Acquisition and Control
By Duncan A. Mellichamp

Become expert at controlling and monitoring a wide variety of EDP processes. Real-Time Computing shows you how to design the best system for specific applications, effectively manage each system, and use sampled-data mathematics to design and analyze computer-controlled processes. It explains the use of multitask programming, multiple computer systems, and hierarchical configurations.

$39.50 CIRCLE 458

A GUIDE TO STRUCTURED COBOL WITH EFFICIENCY TECHNIQUES AND SPECIAL ALGORITHMS
By Pacifico A. Lim

Improve the readability and efficiency of your COBOL programs. Pacifico A. Lim explains how to use coding techniques to produce programs that are easy to understand and inexpensive to maintain. He thoroughly examines the basics of structured programming, coordinated use of all four COBOL divisions, and utilization of ANS COBOL features.

$18.95 CIRCLE 459

ENCYCLOPEDIA OF COMPUTER SCIENCE AND ENGINEERING
Edited by Anthony Ralston

This one-volume library of technical data gives you a storehouse of information in areas ranging from computer systems to the mathematics of computers, modern computer applications, and much more. Its fully revised chapters provide state-of-the-art data on such topics as artificial intelligence, digital computer systems, image processing, and data base technology. "Impressive, comprehensive, well-done."

Datamation $87.50 CIRCLE 460
NEW HIGH PRODUCTION EPROM PROGRAMMER

OAE's new Model 28000 offers:
- Fast 10 MHz Processor.
- More thorough testing than any programmer to screen defective or marginal parts.
- Diagnostic Label Printer option.
- Handles all 5V parts thru 27256.
- Highest throughput capability available.

1973-1983: 10 Years of Excellence

OLIVER ADVANCED ENGINEERING, 676 W Wilson Ave, Glendale, CA 91203. Tel: (213) 240-0080. CIRCLE 476

THE LIFE LINE

Pinpoint the source of your problem fast with the Line Tester from Carroll Touch Technology.

- No battery required.
- 24 lines accessible.
- True 3-state indication

$195 (includes shipping)

For orders or information, call: 217/351-1700
Or send check: Carroll Touch Technology
2902 Farber Drive
Champaign, IL 61821

CIRCLE 477

NEW ECL DIP NEW Crystal Controlled Oscillators
NEW MODELS

ECLA & ECLB

FREQUENCY: 25MHz to 200MHz
OUTPUT: 100K or 10K ECL
SUPPLY: -4.5V or -5.2V
STABILITY: ± .01% or ± .005%
over -25°C to +75°C
DUTY CYCLE: 50 ± 10%
SIZE: 0.5" x 0.8" x 0.25"

THE CONNOR-WINFIELD CORP, West Chicago, IL 60185. PO Box L. Tel: (312) 231-5270, TWX (910) 230-3231

All metal welded package. CIRCLE 480

NEW ECL DIP NEW Crystal Controlled Oscillators
NEW MODELS

ECLA & ECLB

FREQUENCY: 25MHz to 200MHz
OUTPUT: 100K or 10K ECL
SUPPLY: -4.5V or -5.2V
STABILITY: ± .01% or ± .005%
over -25°C to +75°C
DUTY CYCLE: 50 ± 10%
SIZE: 0.5" x 0.8" x 0.25"

THE CONNOR-WINFIELD CORP, West Chicago, IL 60185. PO Box L. Tel: (312) 231-5270, TWX (910) 230-3231

All metal welded package. CIRCLE 480

THE BALANCED STD LINE

MSI-7000 STD Series features 8088 and 8080A CPU cards and memory, I/O, and speech synthesis cards for Z-80, 8088, 8085, and 8080A µP's.
MSI-C000 STD CMOS Series features economical NSC800 µC card and memory and analog I/O cards.
MSI-CR STD Series card racks feature 0.7" card spacing.

MICROCOMPUTER SYSTEMS, INC, 1814 Ryder Drive, Baton Rouge, LA 70808. Tel: (504) 769-2154. CIRCLE 479


OPTICAL & MAGNETIC CARD READERS CIRCLE 478

UV EPROM ERASER

$49.95

INTELLIGENT PROGRAMMER STAND ALONE RS-232

CIRCLE 481

SHIRLEY LESSARD
(800)225-0556
in MA 486-9501
3276 PROTOCOL CONVERTER
CLEO allows up to eight asynchronous ASCII terminals to communicate with a BSC port and may be multi-dropped with other cluster controllers from one port. CLEO may be local or remote over leased-line modems. ASCII terminals may be on-site or remote, over dedicated lines or dial-up. PHONE 1, INC., 461 N Mulford Rd, Rockford, Illinois 61107. Tel: (815) 397-8110.

CIRCLE 482

SOLID STATE POWER FET AC/DC Relay
Teledyne's C46/C47 series are pin-compatible replacements for DIP reed relays where low EMI switching, high reliability and long life are required. Switches AC or DC up to 400V. On-resistance as low as 7 ohms. Control voltage range is 3.8 to 32VDC. Optical coupling provides 1500VDC isolation. Features no offset voltage, low off-state leakage, and high switching speed. $5.80 ea for 5000 pcs.

TELEDYNE RELAYS, 12525 Daphne Ave, Hawthorne, CA 90250. Tel: (213) 777-0077.

CIRCLE 485

6801 MICRO CONTROL SYSTEM
Analog and Power Control I/O...in a Single Board Computer. 6801 or 68701 MPU with 2K ROM or EROM, 128 RAM, timer. 8 12-bit analog inputs, 8-bit analog output, 8 AC or DC inputs or outputs, serial I/O, digital I/O, watchdog timer, power supply. WINTEK CORPORATION, 1201 South St, Lafayette, IN 47904. Tel: (317) 742-8428.

CIRCLE 489

OUR REAL TIME LOGIC ANALYZER
could become your most valuable accessory. Easily attaches to any oscilloscope to compare 8 ± 15 volt signals simultaneously. Make accurate timing and phase relation measurements from DC to 8 MHz. Low power design takes power directly from circuit under test. Complete with 30 inch E-Z-Microhook probe set, manual and full 1 year warranty for only $119.95. Send Check or money order to HEAVISIDE INDUSTRIES, PO Box 2742, Westport, CT 06880-0742.

CIRCLE 484

DISCOVER CHEYENNE!
NO—Corporate Income Tax
NO—Personal Income Tax
NO—Inventory Tax
NO—Tax on In-transit Goods
NO—Tax on Intangibles
NO—Problems!

Locate your corporate HQ, master distribution warehouse, or manufacturing plant in CHEYENNE, WYOMING

HAROLD M. MILLER, Ex-Director
Industrial Development Assn of Cheyenne Municipal Building, 2101 O'Neil Ave
Cheyenne, WY 82001 - 307-637-6385

CIRCLE 486

LIKE NEW PRODUCTS
For free catalog, phone toll-free (800)225-1008
In Massachusetts (617)938-0900
GENSTAR REI SALES COMPANY
6307 DeSoto Ave, Suite J, Woodland Hills, CA 91367.

CIRCLE 487

6801 MICRO LOGIC TIMING SIMULATION
Tired of trial & error circuit design? Analyze and debug your designs before you build them. With MICRO-LOGIC you simply sketch a logic diagram on the CRT screen and run a timing simulation. Your logic network may contain AND, OR, NAND, NOR, EX-OR, D, T, JK FLIP FLOPS and powerful USER-DEFINED 16 PIN MACRO FUNCTIONS, includes on-screen editors for NETWORKS-MACROS, GATES, CLOCK WAVEFORMS and DATA CHANNELS. MICRO-LOGIC is available for the IBM PC and APPLE II computers. A non-graphics version is available for MICRO-LOGIC instruction manual and demo diskette is $50.00. Write for free brochure. SPECTRUM SOFTWARE, 690 W. FREMONT AVENUE, SUITE C, SUNNYVALE, CALIFORNIA, 94087. (408) 738-4387

CIRCLE 483

CIRCUIT CHECKER
MICRO-LOGIC DIAGRAM

CIRCUIT 482

CIRCUIT 483

CIRCUIT 484

CIRCUIT 486

CIRCUIT 487

CIRCUIT 489

CIRCUIT 490

MATRIXED DIRECT MAIL LIST

The most Precise, most Versatile, Cross-Matrixed list of computer Based Systems Designers ever offered for bulk or custom selection. You can rent the entire list, or pinpoint the exact engineers you want to reach. NEW 48-HOUR EXPRESS PROCESSING.

For details, contact Bob Dromgoole at COMPUTER DESIGN, 119 Russell St, Littleton, MA 01460. Tel: (800)225-0556. In MA: (617)486-9501.

CIRCLE 488

6801 MICRO CONTROL SYSTEM
Analog and Power Control I/O...in a Single Board Computer. 6801 or 68701 MPU with 2K ROM or EROM, 128 RAM, timer. 8 12-bit analog inputs, 8-bit analog output, 8 AC or DC inputs or outputs, serial I/O, digital I/O, watchdog timer, power supply. WINTEK CORPORATION, 1201 South St, Lafayette, IN 47904. Tel: (317) 742-8428

CIRCLE 489

CIRCUIT 489

CIRCUIT 490

COMPUTER DESIGN/June 1983 257
Every year, *Computer Design*‘s 90,000 subscribers fill in the most detailed qualification form required by any magazine in the world. Why? Because this form tells us who you are, where you are, what your functions are, what your company does and what you do. It tells us the kinds of projects you are working on, the kind of products you deal with, and where they are used. It becomes the starting point in planning our editorial program.

The information you provide helps us to select the kinds of features, special reports and surveys that will be of immediate, practical use to designers of computer based systems.

The other side of the coin is the value advertisers place on circulation as a major criterion in media selection. As everyone knows, the more advertising pages we carry, the more editorial pages we can provide to you without cost. The bottom line is a better magazine that can speak your special kind of technical language, page after page, issue after issue.
32-Bit Computer Breaks $10K!

Universe 68/05 First to Smash Price Barrier
The new Universe 68/05 is the first true 32-bit computer priced under $10,000 (OEM quantity one). "True" because, unlike other 68000-based systems, the Universe 68/05 handles 32 bits in parallel on its VERSAbus.

Outperforms VAX*
Its price is even more impressive when you look at Universe 68/05

<table>
<thead>
<tr>
<th>MIPS</th>
<th>Cycle time</th>
<th>Bus rate</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>$10K</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$60K</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Universe 68/05</th>
<th>VAX-11/750</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.25</td>
<td>0.75</td>
</tr>
<tr>
<td>390ns</td>
<td>400ns</td>
</tr>
<tr>
<td>20 Mb/sec</td>
<td>13.5 Mb/sec</td>
</tr>
<tr>
<td>$10K</td>
<td>$60K</td>
</tr>
</tbody>
</table>

UNOS, our UNIX* Rev7-compatible operating system with real-time features, runs Pascal, Fortran, C, BASIC, DBMS, and third party application programs.

For more information, just attach your business card to this ad and mail to Charles River Data Systems, 4 Tech Circle, Natick, MA 01760. Or call us at (617) 655-1800. We'll send you a copy of "The Insider's Guide to the Universe," a detailed discussion of the technical concepts behind this remarkable new computer.

CHARLES RIVER DATA SYSTEMS

*VAX is a trademark of Digital Equipment Corporation. UNIX is a trademark of Bell Laboratories. UNOS is a trademark of Charles River Data Systems.
THE BEST HAS JUST BECOME THE BEST DEAL.

Ramtek's popular 6211 Colorgraphic Terminal is now just $4995.* This versatile desk-top unit is ideally suited for the majority of color graphic applications in CAD, science, business, and control systems. Rack mounted (without monitor), it's even more of a value at just $3995.

Need data terminal functions, too? The companion 6221 with full VT 100™ compatibility is priced at just $5995. Plus, a discount is available on 6211 and 6221 systems when both a color printer and 35 mm slide camera are purchased.

The price of quality has never been lower. Volume discounts are also available. For details, call our office nearest you. Or, contact us at 2211 Lawson Lane, Santa Clara, CA 95050. (408) 988-1044.

OUR EXPERIENCE SHOWS.

Ramtek

World Headquarters — Santa Clara, CA (408)-988-2211 European Offices — Amsterdam (31) 2968-5056; London (8936) 76211; Cologne (2234) 78021 U.S. Offices — Dallas, TX (214) 422-2200; Los Angeles, CA (714) 979-5351; Seattle, WA (206) 575-1600; Chicago, IL (312) 397-2279; Houston, TX (713) 774-2233; McLean, VA (703) 893-2020.

Denver CO (303) 694-0758; Cleveland, OH (216) 524-1882; Upper New York/Canada (716) 425-1742; New Jersey (201) 238-2090; Florida (305) 645-0780; Boston, MA (617) 273-4590; Atlanta, GA (404) 252-5066.

*Light pen sold separately.

VT 100 is a registered trademark of Digital Equipment Corporation.