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1979 NATIONAL COMPUTER CONFERENCE 88

With 150 technical program sessions covering the latest developments in computer applications, science and technology, management, and social implications, plus exhibits by more than 400 organizations, this year's NCC promises to be the largest and most diverse ever. Special events will include the Personal Computing Festival and personal development seminars.
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11. BULK SEMI main memory ADD-ON for
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12. 256KB sem ADD-IN for DECSYSTEM 2020
13. 256KB sem ADD-IN for Nova 3
14. 256KB sem ADD-IN for Eclipse
15. ADS and RDOS-compatible BULK CORE
    disk emulation system for Nova and
    Eclipse
16. BULK SEMI Nova/plus-compatible disk
    emulation system for Nova and Eclipse
17. BULK SEMI ADS and RDOS-compatible
    disk emulation system for Nova and
    Eclipse
18. Dual port for Data General-Compatible
    BULK CORE disk emulation system
19. Dual port for Data General-compatible
    BULK SEMI disk emulation system
20. BULK SEMI Interdata-compatible disk
    emulation system
21. Core ADD-ON for Univac (Vario) V77-400

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CIRCLE 5 ON INQUIRY CARD
**LETTERS TO THE EDITOR**

To the Editor:

The Application Note on pp 122-126 in the Feb 1979 issue of *Computer Design* ("Software Error Checking Procedures For Data Communication Protocols," J. Wong, W. Kolofa, and J. Krause) is a reasonable examination of the generation of a crc (cyclic redundancy check). But, the final result in the form of a computer program leaves a lot to be desired. First, it is not fast because it operates in a bit serial fashion. Second, there are better ways.

If one assumes that a table driven crc algorithm which is the fastest nonhardware method is not used because the size of the table would be prohibitive, then a byte parallel algorithm should be found. It seems that *Computer Design* had a previous Application Note which adequately described not only how to generate a crc, but also gave a listing of a program that did a byte parallel crc.

The May 1976 issue of *Computer Design* on pages 190 and 192 (notice how short it can be when you really know what you are doing) had such an article ("Calculating an Error Checking Character in Software"). The author, Suresh Vasa, explained the crc generating algorithm for an F8 and explained the method used to find it. The example given was only for sdlc, but with a little work, it can be converted for other crc polynomials. This was done by myself and others where I work and is now a part of software and firmware routines in many products where the size of a crc table would have been too costly. Both sdlc and bisync algorithms have been generated, checked, and used in the marketplace for over a year. This algorithm is fast (38 \(\mu s\) on an F8 as compared to 512 \(\mu s\) on the 6800), linear (no jumping or looping), and the one drawback in the article (msb, lsb swapping) is easily resolved with still an order of magnitude speed improvement.

I have not programmed the 6800 itself, but as an exercise, I attempted an implementation of Vasa’s algorithm on it (see *SDLC CRC Generating Algorithm for a 6800*). I cannot guarantee its accuracy, but I do not think anything is wrong with it.

Finally, I feel that the editors of *Computer Design* should check back across older issues to find the applicability of new articles or Application Notes. The fact that an article on crcs was redone is good because many engineers do not have the older references, but before the article is accepted it should be shown to at least match (if not exceed) the quality and capability of previous articles or explain why it did not and have a reference to the other articles.

Henry Socha
San Antonio, Texas

**The Authors Reply:**

The purpose of our article ("Software Error Checking Procedures For Data Communication Protocols," *Computer Design*, Feb 1979, pp 122-126) was to communicate the basic concept of evaluating crc software versus hardware. While the byte parallel approach is admittedly faster, we are convinced that the bit serial routine provides better insight and understanding into the crc problem for both bsc and sdlc protocols.

Since Mr Vasa’s article ("Calculating an Error Checking Character in Software," *Computer Design*, May 1976, pp 190-192) dealt exclusively

---

**SDLC CRC Generating Algorithm for a 6800**

<table>
<thead>
<tr>
<th>ENTER:</th>
<th>A = NEW DATA BYTE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CRC = 2-BYTE CRC ACCUMULATION (IN MEMORY)</td>
</tr>
<tr>
<td></td>
<td>B = WORK REGISTER</td>
</tr>
<tr>
<td>EOR A CRCH (3.2) (LEAVE OUT IF DATA ARE KNOWN ZERO)</td>
<td></td>
</tr>
<tr>
<td>STA A CRCH (4.2)</td>
<td></td>
</tr>
</tbody>
</table>

**NOW, GENERATE SDLC CRC FOR COMBINED DATA/CRC**

| LSR A (2.1) |
| LSR A (2.1) |
| LSR A (2.1) |
| LSR A (2.1) |
| EOR A CRCH (3.2) GENERATE I J K L M N O P |
| LDA B CRCL (3.2) |
| STA B CRCH (4.2) SWAP CRCS AROUND (CORRECTING VASA'S FAULT) |

**STA A CRCL (4.2) | ROL A (2.1) | ROL A (2.1) | ROL A (2.1) | ROL A (2.1) | TAB (2.1) SAVE M N O P X I J K | ROL A (2.1) | ROL A (2.1) HAVE 0 P X I J K L M | AND A #037 (2.2) SELECT 0 0 0 0 1 I J K L M | EOR A CRCH (3.2) | STA A CRCH (4.2) | TBA (2.1) | AND A #360 (2.2) SELECT M N O P 0 0 0 0 | EOR A CRCH (3.2) | STA A CRCH (4.2) CRCH DONE | ROL B (2.1) | AND B #0340 (2.2) SELECT N O P 0 0 0 0 0 | EOR B CRCL (3.2) | STA B CRCL (4.2) CRCL DONE |

**END (74 CYCLES, 43 BYTES)**

**Note:** Numbers starting with 0 are in octal.
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Fairchild's MICROFLAME Development System is an enhanceable system designed to develop prototype hardware and software for a broad range of microprocessor applications. From PROM resident code for MICROFLAME-based controllers to realtime multitasking software for distributed processing or control applications using the FOCVS XVI computer.
For the record, our development system combines the FOCVS XVI, a powerful computer offering 64KB of RAM, with a dual-double-density IBM-compatible floppy-disk subsystem (1 megabyte capacity expandable to 4 megabytes). A free-standing video display terminal and a 150-CPS bidirectional dot matrix printer complete the basic system.

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FIRELINK has the additional capability of communicating with remote target systems or other MICROFLAME Development Systems via a modem/acoustic coupler over telephone lines if necessary.

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The system includes, as standard, system processors such as FIRE-EDIT (text editor), FIRE-MACRO (macroassembler), FIRE-SYMBUG (symbolic debugger), FIRE-LIBE (relocatable library), FIRE-LIBEDIT (relocatable library editor), FIRE-OEDIT (octal editor) and FIRE-TYPESET (typesetting program).

The software for PROM formatting and burning is standard on our system using either an attached user-supplied PROM programmer or a detached paper tape.

Optional high-level languages under the development system software include BASIC, FORTRAN and PASCAL.

The system is delivered complete with documentation and an automatic installation and system-test diskette to assist user setup and checkout of the system. For more information, write the FIRE Microcomputer Group, Fairchild Camera and Instrument Corporation, P.O. Box 880A, Mountain View, California 94042.

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with SDLC protocol for an F8, we did not feel it was relevant to our presentation. In fact, we agree with Mr Socha that there is a “drawback” in Mr Vasa’s article, namely, that the incoming data byte should be shifted, with MSB first, into the CRC accumulator. We believe our article made a contribution by pointing out that (1) the incoming data byte should be shifted, with LSB first, into the CRC accumulator, and (2) embedded sync codes are not to be included in CRC accumulations.

By presenting the academic bit serial approach, we feel that we have contributed some understanding of CRC software procedures for both BSC and SDLC protocols that will be of use to the general engineering community.

There appears to be an error in our CRC Subroutine for SDLC Protocol (Subroutine 2, page 126):

LDA A #$40 should be LDA A #$08.

John Wong, Bill Kolofa, and Jim Krause
Motorola Inc, Data Products
West Chicago, Illinois

To the Editor:

I read with interest the article “Software Error Checking Procedure For Data Communication Protocols” (J. Wong, W. Kolofa, and J. Krause) which appeared in your Feb 1979 issue (pp 122-126). This article describes a relatively straightforward software emulation of the hardware feedback register approach to computing cyclic redundancy checksums. As a direct software emulation of a process intended for hardware implementation, the suggested procedure is rather expensive in terms of processor cycles. This is in contrast to more efficient software procedures that may be developed based on table driven approaches.

For example, one such approach was described in your own magazine several years ago. This was in the article by Joseph S. Whiting, “An Efficient Software Method for Implementing Polynomial Error Detection Codes” that appeared in Computer Design in Mar 1975 (pp 73-77). The earliest reference to this technique that I have been able to find, and actually the most lucid explanation as well, was in the article by Martin and Frambs, “A Cyclic Redundancy Checking Algorithm,” that appeared in the Honeywell Computer Journal, Vol 5, No 3, 1971, pp 140-142. Each of these two articles describes procedures whereby storage may be traded off against processor cycles in the calculation of cyclic redundancy checksums. It is shown that the use of relatively small size tables, up to 256 bytes in length, result in quite dramatic decreases in the number of processor cycles required to compute a cnc.

I would be interested in knowing if the present authors were familiar with this work, and if so, why they chose to ignore it.

Ira W. Cotton
National Bureau of Standards
Institute for Computer Sciences and Technology
Washington, DC

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CIRCLE 9 ON INQUIRY CARD
CONFERENCES


JUNE 17-20—Joint Automatic Control Conf, Hilton Hotel, Denver, Colo. INFORMATION: Prof T. F. Edgar, Program Chm, 1979 JACC, Dept of Chemical Engineering, U of Texas, Austin, TX 78712. Tel: 512/471-3080

JUNE 20-22—International Symposium on Fault-Tolerant Computing, Concourse Hotel, Madison, Wis. INFORMATION: Prof Charles R. Kime, Prof T. F. Edger, Program Chm, 1979 JACC, University of Wisconsin, Madison, WI 53705. Tel: 608/262-0206

JUNE 25-27—Design Automation Conf, Town and Country Hotel, San Diego, Calif. INFORMATION: Robert J. Smith, III, Electrical Engineering Dept, U of Texas, PO Box 7728, Austin, TX 78712. Tel: 512/471-4540

JUNE 28—IEEE Indy Microcomputer Show, Sheraton Motor Inn E, Indianapolis, Ind. INFORMATION: Harry D. Bostic, Naval Avionics Ctr, D/810, 6000 E 21st St, Indianapolis, IN 46218. Tel: 317/353-3047

JULY 16-18—Summer Computer Simulation Conf, Toronto, Canada. INFORMATION: Dr A. J. Schieve, Chm '79 SCSC, c/o The Aerospace Corp, PO Box 92957, Los Angeles, CA 90009

JULY 17-20—Joint Intermag/Magnetism and Magnetic Materials Conf, Statler Hilton, New York, NY. INFORMATION: Dr E. F. Luborsky, Conf Chm, Conf Chm, General Electric R&D Ctr, PO Box 8, Schenectady, NY 12301

AUG 6-8—Pattern Recognition and Image Processing, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: PRIP '79, PO Box 639, Silver Spring, MD 20901

SEPT 4-7—COMPCON, Washington, DC. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEPT 5-8—INFO/ASIA, Ryutsu Ctr, Tokyo, Japan. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10012

SEPT 7-9—International Microcomputer Exposition, Dallas, Tex. INFORMATION: IME, 413 Corinth Tower, 13601 Preston Rd, Dallas, TX 75240.

SEPT 17-19—Fourth Internat'l Conf on Software Engineering, Munich, Germany. INFORMATION: Prof Fritz Bauer, Institut fur Informatik der Technischen Universität, D-8 Munich 2, Anzistrasse 21, Postfach 90 94 90, Germany


SEPT 26-29—Mini and Microcomputers Internat'l Sym and Exhibition, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: The Secretary, MIMI '79, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

SEPT 28-30—Northeast Personal and Business Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: Northeast Expositions, PO Box 678, Brookline Village, MA 02147. Tel: 617/522-4467

SEPT 4-7 and JUNE 4-7—Automated Testing for Electronics Manufacturing, ATE Seminar/Exhibit, Radisson Ferncroft Hotel, Danvers, Mass, and Northeast Trade Ctr, Woburn, Mass. INFORMATION: Kote Fitzgerald, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JUNE 11-15—Testing Microprocessor Based Systems, The Colonial Hilton Inn, Wakefield, Mass. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: 617/964-1412

SEPT 3-4—Fourth Annual Workshop on Microprocessor Applications, U of Liverpool, England. INFORMATION: Dr Malcolm J. Taylor, The Computer Laboratory, The University of Liverpool, Brownlow Hill and Crown St, PO Box 147, Liverpool L69 3BX, England

SHORT COURSES


JUNE 18-19—Minicomputer Interface Design: Examples from the Nova Computer; JULY 23-27—Mini and Microcomputers: Their Structures, Characteristics, and Applications; JULY 30-AUG 3—Microcomputer System Design and Applications; and AUG 13-17—Data Network Planning and Design; U of Michigan, Ann Arbor, Mich. INFORMATION: Viole E. Miller, Engineering Summer Conf, 300 Chrysler Ctr, N Campus, Ann Arbor, MI 48109. Tel: 313/764-8490


JUNE 19-22—Modern Digital Communications, National University, San Diego, Calif. INFORMATION: Dr Donald J. Rauch, Evolving Technology Seminars, 3520 Jennings St, San Diego, CA 92106. Tel: 714/224-3788

JULY 16-27—Intro to Digital Electronics and Microcomputer Interfacing, Virginia Military Institute, Lexington, Va. INFORMATION: Prof Philip Peters, Dept of Physics, Virginia Military Institute, Lexington, VA 24450


SEMINARS

JUNE 4-7 and JUNE 5-7—Automated Testing for Electronics Manufacturing, ATE Seminar/Exhibit, Radisson Ferncroft Hotel, Danvers, Mass, and Northeast Trade Ctr, Woburn, Mass. INFORMATION: Kote Fitzgerald, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JUNE 11-15—Testing Microprocessor Based Systems, The Colonial Hilton Inn, Wakefield, Mass. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: 617/964-1412

Announcements intended for publication in this department of Computer Design must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.
The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

More
A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the “Hyperdiagnostics” that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

Faster
The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

For Less
The DSD 440 is the RX02 compatible flexible disk system that combines high performance and advanced features with fast delivery...at a lower price. For further information, call or write Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

Data Systems Design, Inc.
3130 Coronado Drive,
Santa Clara, CA 95051
(408) 249-9353
TWX 910-338-0249

Eastern Regional Sales:
(617) 329-5730
TWX 710-348-0563

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New Breed of MOS.

Intel introduces HMOS II* and a new family of static RAMs that cross the finish line in 20 ns.

Intel just set a new pace for high performance memory with HMOS II. It's our patented next generation MOS technology so advanced it delivers speeds faster than bipolar and even our own first generation HMOS process. HMOS II gives designers the fastest, lowest power static RAMs ever—plus traditional MOS economy and reliability. Our new 215H/2125H 1K RAMs ideal. For new designs, two versions deliver record access speeds of 20 ns and 25 ns, with a speed/power product twice as good as slower bipolar RAMs.

Our 35 ns and low power 30 ns models can be used as direct plug-in replacements for 93415A and 93425A bipolar RAMs. They'll cut power dissipation up to 36%. And, best of all, they're available now.

New, faster 4K with no power increase

Intel's new 2147H gives you all the advantages of our 18-pin 4K x 1 industry standard 2147, with twice the speed and no increase in power. With access times as fast as most 1K RAMs, it's important news for anyone designing buffer, cache, control store and main memory systems. If you're presently working with 1K RAMs, you can increase density or reduce board space by a factor of four. In a 4K format, the 2147H makes possible a new dimension of higher performance systems.

The 2147H's low active power dissipation and automatic power down on deselection also mean dramatically reduced power consumption compared to constant current static RAMs. In fact, because most devices are deselected at any given time, the larger your system, the lower your power dissipation per bit. It all adds up to simplified designs and major savings in cooling and power supplies.

All HMOS II components are fully static and can be used in clocked and unclocked systems. They are directly TTL compatible in all respects: inputs, outputs and operation from a single +5V supply.

Order 2115H/2125H and 2147H RAMs from your Intel distributor. Or, for more information, contact your local Intel sales office or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

1K and 4K RAMs are fully compatible, higher speed upgrades of Intel's time-tested 2115A/2125A and 2147 devices.

1K fast statics that leave bipolar s behind

Designers building cache, writeable control store or buffer memories will find our 16-pin

| HMOS II fast static RAMs |  |
|--------------------------|-----------------|-----------------|
| Part No. | Maximum Access Time (ns)* | Power Consumption (mA)* | |
| 4096x1 | 35 | 180 | 30 |
| 2147H-1 | 35 | 180 | 30 |
| 2147H-2 | 45 | 180 | 30 |
| 1024x1 | 20 | 125 |  |
| 2125H-1 | 20 | 125 |  |
| 2115H-2 | 25 | 125 |  |
| 2125H-2 | 25 | 125 |  |
| 2115H-3 | 30 | 100 |  |
| 2125H-3 | 30 | 100 |  |
| 2115H-4 | 35 | 125 |  |
| 2125H-4 | 35 | 125 |  |

*Over full 0° to 75°C operating temperature range.
**All 2115H versions have open-collector outputs, all 2125H versions have tri-state outputs.

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For the past decade, the field of data communications has been rapidly changing, with important innovations emerging all the time. One recent development of wide ranging significance is the introduction of several new techniques for short distance high speed data communications. These techniques may transform communications within offices, laboratories, factories, and universities.1

It is appropriate to begin with an examination of why a local network is different from other, long distance, networks. By definition, a local network is a data communications system designed to interconnect computers and terminals over a restricted geographical area, typically less than 2 km in diameter. A number of implications follow from this definition.

At a technical level, the problems involved in designing local networks are not very different from those relating to long distance networks (see Panel, “A Hierarchy of Communications Network Problems.”) However, the parameters are different. Since the communication network and transmission medium are not bottlenecks, transmission rates are higher. Delivery delays are shorter and message lifetimes, ie, maximum delivery delays, are shorter. Error rates are lower compared with typical long distance transmission media. Cost of interconnecting terminal and computer equipment is lower. There is greater use of broadcast or multiaddress communications.

From an organizational point of view, a local network is likely to be designed and implemented by a single organization which, in all probability, will also be responsible for its operation. The result is a much higher degree of control than can be expected in a long distance or “global” network. This organizational approach also eliminates such problems as coordinating changes among several different groups, and the “finger pointing” problem of fault diagnosis involving many components.

Local Network Technology
From the premise that communication is required over a local region only, one can trace the line of reasoning to the conclusion that a new type of network technology can be used.

(1) A more expensive communications medium, in terms of cost per meter, can be used in a local network because the total cost of the medium is likely to be insignificant compared to installation and other hardware and software costs.

(2) Since a more expensive communications medium can be used, a more powerful medium is possible, especially in terms of its speed and error performance.

(3) Local interface hardware and communications protocols can be considerably simplified because there is less need to optimize available communications bandwidth—the inherent traffic handling capacity of the network is so much greater than in a global network.

(4) The cost to interconnect a device to a local network can (and must) be reduced significantly by the process of simplification, standardization, and eventually by large scale integration (LSI) manufacture.

(5) As a result, local networks open the possibility for connecting much lower cost devices, eg, small computers

John M. McQuillan
Bolt Beranek and Newman Incorporated
Cambridge, Massachusetts
There's no drum in Centronics' band.

Centronics' 6000 Series Band Printers have banished the drum. Forever. That means important savings and simpler operation for you.

An inexpensive changeable band lets you change character sets or type in seconds without disturbing paper or ribbon. No special tools. No expensive drum. No special service calls.

Centronics' horizontally moving print band means crisper print quality and perfect vertical alignment. You get uniform density control regardless of paper stock.

Band printers are faster and less expensive to service too. A single motor drives both the print band and cassette-enclosed ribbon. Modular construction combined with simplified design minimize downtime. And service is available at more than 100 locations throughout the world.

But that's not all. Centronics' band printers cost less. In fact, thousands of dollars less than comparable drum printers.

Operating flexibility. Easier servicing. Crisper print. Lower cost. Centronics' band printers beat the drum everytime. For information write or call your local authorized Centronics' distributor or Centronics Data Computer Corporation, Hudson, New Hampshire 03051, (603) 883-0111.

CENTRONICS
The Band Leader

CIRCLE 12 ON INQUIRY CARD
"...And for higher performance, we’ll specify Harris Data Acquisition components."
Harris high performance components assure superior speed and accuracy.

Now Harris can provide you with a complete selection of data acquisition products—from op amps to digital-to-analog converters—with the highest performance available anywhere.

It’s what you expect from Harris—the leading supplier of monolithic sample-and-hold, high performance multiplexers and switches. And producer of the first 12-bit monolithic D/A converter... which has led to the most advanced family of DACs in the industry.

HARRIS DATA ACQUISITION PRODUCTS

DIGITAL-TO-ANALOG CONVERTERS
The fastest, most accurate monolithic DACs available. Monotonic over temperature. Designed for minimum glitches.

HI-562 - 12-bit, 200 ns to 0.01%
HI-5612 - 12-bit, 150 ns to 0.01%
HI-5610 - 10-bit, 85 ns to 0.05%
HI-5608 - 8-bit, 50 ns to 0.19%

ANALOG-TO-DIGITAL CONVERTERS
12-bit ADCs soon to be introduced will offer precision and conversion speeds in microprocessor-compatible versions.

HI-5712 - 12-bit, 6 µs conversion
HI-5812 - 12-bit, precision

CMOS ANALOG MULTIPLEXERS
Latch-proof, Single/Differential, 8/16 channel. Overvoltage protected versions can withstand transients up to 1000 volts and inputs of ±20 volts greater than either supply.

HI-506A/7A - 16-channel, overvoltage protected
HI-506/7 - 16-channel
HI-508A/9A - 8-channel, overvoltage protected
HI-181/28A - 8-channel
HI-1840 - 16-channel, high Z, overvoltage protected

CMOS ANALOG SWITCHES
Two popular series feature several latch-proof configurations with high-speed, low-on-resistance, and low-power versions.

HI-200/301 - Dual/Quad, 180 ns, 55 ohms, 15 mW
HI-5040 series - 370 ns, 25 ohms, 1.5 mW

MONOLITHIC SAMPLE-AND-HOLD
Low droop rate coupled with fast acquisition time furnishes the speed and precision needed for 12-bit systems.

HA-2420 - 4 µs to 0.01% acquisition, 5 pA drift current

VOLTAGE REFERENCES
Two new laser trimmed ±10 volt references offer industry milestones in precision and stability.

HA-1600 - ±10 volt, ±1 ppm/°C
HA-1610 - ±10 volt, ±5 ppm/°C

SIGNAL CONDITIONERS
New precision BIFET op amps to complement the Harris high-performance line. Laser trimmed for low offset voltage.

HA-5100/5110 - Wide band BIFET
HA-5150/5160 - High slew BIFET

FAST-SETTLING OP AMP
The fastest monolithic true op amp in the world has superior settling times for voltage output DACs.

HA-5190 - 100 ns to 0.01%, 200 V/µs Slew

COMPARATORS
A family of fast quad comparators is coupled with a soon-to-be-introduced, high-speed precision single comparator for use in ADCs. The 4950 will give true 12-bit accuracy with no sacrifice in throughput.

HA-4950 - 35 ns response, with 100 µV resolution

*To be introduced

HARRIS HOT LINE!
1-800-528-6050, Ext. 455
Call toll-free (except Hawaii & Alaska) for phone number of your nearby Harris sales office. Authorized distributor or expedited literature service.
Local Networking Problems

(1) The central computer facility problem: organization of the several mainframe computers and large peripheral devices operated by a particular organization into a coherent set of commonly accessible resources.

(2) The "satellite" or remote computing problem: interconnection of a wide variety of minicomputer based equipment and associated peripheral devices, located over a limited geographical area up to several km in diameter, to the central computing facility. This is usually termed "distributed data processing" or local intelligence.

(3) The terminal access problem: general interconnection of any terminal device, intelligent or non-intelligent, to any computer system, usually a satellite computer, but also to a mainframe in the central computing facility. These terminals may include traditional keyboard terminals, as well as office automation devices, digital voice terminals, and other microcomputer based equipment.

Long Distance Networking Problems

(4) The standard computer network problem: interconnecting the computing equipment of one organization, typically its central computing facility, through a single transparent, application-independent computer network to some set of other computing resources. This can be accomplished through a public data network, through a private or dedicated packet switching network, through the use of one of the network architectures offered by computer vendors such as SNA or DECNET, or by various other strategies.

(5) The internetwork communications problem: linking together a number of separate and independent computer networks by means of gateway computers, so that messages can be exchanged from one network (possibly through several intermediate networks), to the destination network.

Technical Design Issues

Topological structure is the central design decision in selecting the appropriate local network for a particular situation. Connecting each computer to all of the other computers is impractical in all but the smallest configurations. The figure shows four other basic possibilities in local network structure: star (or more generally, tree), ring, bus, and general distributed topology.

Next important question in designing a local network is the protocol that governs communications between the basic network elements. Conventional star networks have often operated by a polling principle in which the central controller indicates to each of the peripheral devices when they can transmit. A related type of control technique used in star networks is to configure the central controller as a message switching system. In this case, each of the devices connected to the star can transmit whenever it has information. The data are stored by the central switch until the intended destination can accept the traffic.

A common means of controlling the use of a ring network is some form of multiplexing, since each of the devices can remember when its turn to send will come and thus avoid collisions when attempting to use the shared transmission facilities. Contention is an alternative to polling and time division multiplexing. Devices are free to transmit over the network whenever they have information to send, and they are prepared to deal with the possibility that some other device may send at the same time, and perhaps render both transmissions ineffective. Contention has been used most often in bus networks but could be used in any of the other topologies as well.

One important protocol feature that can be designed into a contention system or other control strategy is the

and even intelligent terminals, directly to the local network without the use of terminal concentrators or device controllers.

(6) In turn, this implies that a local network may evolve into a collection of a large number of small, slow devices and a relatively smaller number of high speed computers and peripheral devices.

It is clear from this line of reasoning that there is no sharp division between global and local networks; there is, rather, a continuum in which smaller geographical areas are served with higher speed, lower cost interfaces.

The illustration depicts these networks schematically, and Refs 2 and 3 provide an overview of available vendor network architectures, and a comparison of the IBM approach with new industry standards, respectively.
YOU CAN
ELIMINATE 93% OF YOUR
INTERCONNECTING CABLES!

With Dynamics' System 7700
high speed
analog to digital multiplexer.

System 7700 Sixteen Channel Differential Amplifier Signal Conditioner and MUX has the unique capability to transmit all 16 channels at a data rate of 2500 samples per second per channel over one mile of RG-58U coax cable with an overall system accuracy of ±.04%.

Its features include an amplifier per channel, with gain adjustable from 1 to 12,500, transducer excitation, remote or local calibration, monitoring, bridge balance, and low pass active filters.

Only one interconnecting cable is required between the signal source, and the control center or data center, therefore eliminating 93% of the normal interconnecting cabling required. Circle the number below.

DYNAMICS
Division of Waugh Controls Corp.,
9001 Fullbright Avenue, Chatsworth
California 91311 Telephone 213-998-0121
No one portable everyone's needs.
So we built 21.

Everyone's needs are different. Some want the same versatility in the field they get from a bench model in the lab. Others are more concerned about weight. Some require basic performance models at an economical price. Tektronix offers a selection of 21 portable scopes — 15 real-time and 6 storage models — to satisfy just about everyone.

Take your pick. You can't beat our 400 Series when it comes to high performance. Choose from 9 models ranging in bandwidth from 50 MHz to 350 MHz. All under 26 pounds (11.8 kg). Five with an optional DMM and delta time read out.

If you're looking for a battery-powered model that fits into a briefcase or toolbox, there's our 200 Series. Bandwidths to 5 MHz. Weights less than 3.7 pounds (1.7 kg).

In between, there's the compact 300 Series, with bandwidths to 35 MHz. Each scope weighs less than 11 pounds (5.0 kg). And finally, we offer the low cost T900 Series, priced from just $795.00.

Our worldwide service team goes where you go. We're with you all the way, with more than 500 service personnel at 46 Tektronix centers in the U.S.A. and hundreds of Tektronix-supported service engineers in over 50 other countries to calibrate and maintain your Tektronix scope.

So let us show you the model that's right for you. Simply contact your Tektronix Sales Engineer. He'll arrange for a demonstration of our portable or laboratory oscilloscopes. And for our latest portable oscilloscopes brochure, write: Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe: Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

We're going places
## Product Specifications

<table>
<thead>
<tr>
<th></th>
<th>Storage Models</th>
<th>Nonstorage Models</th>
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<td>465 250 MHz @ 5 mV/div</td>
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<td><strong>Other Special Features</strong></td>
<td>3000 div/us stored writing speed</td>
<td>Widest bw in a portable</td>
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<td><strong>Price</strong></td>
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<td>475A 250 MHz @ 5 mV/div</td>
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<td>High-performance 250-MHz portable</td>
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<td>521 5 MHz @ 2 mV/div</td>
<td>460M 100 MHz @ 10 mV/div</td>
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<td>Tri-service standard 100-MHz scope</td>
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<td>$2620</td>
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<td>5 ns/div</td>
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<td>Cost effective for 50-MHz bw</td>
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<td>0.1 µs/div</td>
<td>5 ns/div</td>
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<tr>
<td><strong>Other Special Features</strong></td>
<td>Autoranging DMM</td>
<td>Only 5.6 lbs (4.9 kg)</td>
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<tr>
<td><strong>Price</strong></td>
<td>$1725</td>
<td>$1725</td>
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<td>213 1 MHz @ 20 mV/div</td>
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<td><strong>Fastest Sweep Rate</strong></td>
<td>400 ns/div</td>
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<td><strong>Other Special Features</strong></td>
<td>DMM/Discroscope @ 3.7 lbs (1.7 kg)</td>
<td>Low cost for dual trace &amp; battery</td>
<td></td>
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<tr>
<td><strong>Price</strong></td>
<td>$1895</td>
<td>$190</td>
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<td><strong>Storage Models</strong></td>
<td>212 200 kHz @ 10 mV/div</td>
<td>T934A 25 MHz @ 2 mV/div</td>
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<td><strong>Delayed Sweep</strong></td>
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<td>10 ns/div</td>
<td>10 ns/div</td>
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<tr>
<td><strong>Other Special Features</strong></td>
<td>Delivered sweep and differential</td>
<td>Variable trigger-holdoff and differential</td>
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<td><strong>Price</strong></td>
<td>$1555</td>
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<td>T933 5 MHz @ 5 mV/div</td>
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<tr>
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<td><strong>Fastest Sweep Rate</strong></td>
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<td>20 ns/div</td>
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<td><strong>Other Special Features</strong></td>
<td>Low-cost dual-trace scope</td>
<td>Recalibrated version of TR22</td>
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<td><strong>Price</strong></td>
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<td></td>
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<tr>
<td><strong>Delayed Sweep</strong></td>
<td>yes</td>
<td>yes</td>
<td></td>
</tr>
<tr>
<td><strong>Fastest Sweep Rate</strong></td>
<td>20 ns/div</td>
<td>20 ns/div</td>
<td></td>
</tr>
<tr>
<td><strong>Other Special Features</strong></td>
<td>Low-cost TEKTRONIX Portable</td>
<td>Only 10.6 lbs (4.8 kg)</td>
<td></td>
</tr>
<tr>
<td><strong>Price</strong></td>
<td>$795</td>
<td>$795</td>
<td></td>
</tr>
</tbody>
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### Time Interval Readout DM44
- Optional, factory-installed, direct numerical readout of time intervals and DMM functions for the 464, 465, 466, 475 and 475A.

### Other Special Features
- **Storage Models**: 3000 div/us stored writing speed.
- **Nonstorage Models**: Widest bw in a portable.

### Prices
- **Storage Models**: $2350, $2795, $1645, $2620, $2665, $1725.
- **Nonstorage Models**: $1895, $190, $1555, $975, $795.

### Additional Information
- **Time Interval Readout DM44**: For the 464, 465, 466, 475 and 475A.
- **Price**: $795.

**U.S. sales prices are F.O.B. Beaverton, OR.** For price and availability outside the United States, please contact the nearest Tektronix Field Office, Distributor or Representative. Prices are subject to change without notice.

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**For immediate action, dial our toll free number**: (800) 547-1512 (In Oregon, collect 694-9051)

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**For demonstration please circle # 16**

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**For literature please circle # 15**
communicated by the store-and-forward method through
is, prior to transmitting, each station can continuously
puters on the one hand, and between satellite computers
explicit detection of collisions among transmissions. That
is, prior to transmitting, each station can continuously
monitor the communications medium to insure that no
other station is transmitting. In the case that a collision is
detected after a transmission has begun, both stations can
detected after a transmission has begun, both stations can
Each gateway computer also has an important role to play with regard to resource
management, in resolving such questions as fair allocation
of resources among users, optimal distribution and schedul­ing of network use, and the like. Since the gateway
controls access to one network from the other, it acts as
a sort of scheduler. Therefore the algorithm it uses for
determining which of several competing users to serve
next is of critical importance to overall performance of
the network system.

Local Network Interface Standards—One of the most
attractive possibilities for standardization is the prospect
for a standard interface to ring or bus type networks.
These interfaces are so simple that even in experimental
form they have been implemented in microcomputers.
This suggests that in operational form they could be
implemented by means of LSI chips. If this step is taken,
and several manufacturers are persuaded that the produc­tion of such standard interfaces is in their interest, it might
be possible to foresee the introduction of local network
interfaces which are so cheap, say $100 each, that even
rudimentary terminals could be directly connected to such
networks.

High Level Protocols—One of the topics often ignored
when considering the design of a local network is that
many levels of function-oriented protocols are necessary in
order to accomplish useful work on the network. For in­stance, the local network may make it possible for the
first time to connect mainframe computers constructed by
different vendors, or to connect several different terminals
with several different mainframes. In addition to being a
solution to a particular problem, however, this intercon­nection also raises the much more general problem of
higher level protocols. In order to be useful, the local
network must support some form of data transport proto­col, file transfer protocol, and virtual terminal protocol.
These protocols are necessary so that a computer which
was designed with one data and file format, and one
particular terminal type in mind, can transfer data and
files to other computers in other formats, and accept in­formation from foreign terminal types.

It has been our experience in network implementation
that these higher level protocols are often the last element
of the network to be completed and the most difficult to
specify with regard to efficiency and generality.

References
1. J. M. McQuillan, "Understanding the New Local Network
Technologies," BBN Report No 3927, Sept 1978, $75
2. J. M. McQuillan, "Evaluating the Vendors' Network Archi­
tectures," BBN Report No 3950, Oct 1978, $75
3. I. Richer and M. Steiner, "Choosing Between X.25-Based
Networks and IBM's SNA," BBN Report No 3948, Oct 1978,
$75

Four possible network topologies. Star network is organized around
single controller. In ring config­uration data flow is sequential
around single transmission loop
connecting communicating de­
ices. In bus network, data are
broadcast to all devices; there is
no closed loop in the transmission
facilities. In general distributed
topology there are several paths
between communicating nodes,
but not all nodes are connected
directly to each other.
If you've been waiting, waiting, waiting for DEC's VT 100, you know what a heavy burden that places on your operations. Now there's hope, because Datamedia just beat DEC to the punch with its new DT 80/1 terminal.

The DT 80/1 not only matches the VT 100 feature for feature, but also takes a big step ahead, by adding full printer control.

Here's another jab: The DT 80/1 gives you the freedom to key in a split screen, double-size characters, and even limited graphics.

In white-on-black or black-on-white.

The CRT screen has other special moves, too, like underline, blink, protect and dual intensity.

The DT 80/1 carries all these features in a very compact frame. It measures just 14" x 14" x 14", so it fits anywhere the VT 100 would fit. And the space flexibility of a detached keyboard is standard.

Like all Datamedia terminals, the DT 80/1 is engineered to run cooler and last longer, without the need for a noisy fan. In fact, we're so confident of its reliability, we've even given the DT 80/1 a full one-year warranty. Just what you'd expect from the company whose products have been Datapro-rated #1 for performance for the past two consecutive years.

Lighten up the burden of waiting. Get the DT 80/1 now. The coupon below will help you get started.

Please send me more information on your new DEC-compatible DT 80/1.
Name_____________________
Company_________________
Address__________________
City______________________
State____________________ 
Zip______________________

Datamedia Corporation
7300 N. Crescent Blvd., Pennsauken, N.J. 08110
Tel: (609) 665-2382 TWX: 710-892-1693

CIRCLE 17 ON INQUIRY CARD
6545 CRT Controller. The designer’s choice.

DESIGN FLEXIBILITY.

That’s what the SY6545 CRT Controller delivers, giving you an unlimited range of system design configurations—all programmable with the SY6545. You can design all your terminals with the same controller. It’s easy. And it’s all the result of the programmability and flexibility of the SY6545.

ROW AND COLUMN ADDRESSING.

In addition to the conventional binary sequential memory addressing modes, the SY6545 gives you the option of addressing the refresh memory by row and column. There’s no need to perform special algorithms for address conversions. Because we’ve made the memory location one-to-one correspondent to the screen location.

TRANSPARENT RAM ADDRESSING.

Transparent RAM addressing allows the CRTC to address the refresh memory “transparent” to the MPU—the refresh memory can be configured to be a slave to the CRTC instead of being shared with the MPU. The SY6545 does all the work of generating memory addresses for display refresh and memory updates. The memory can be updated either during horizontal and vertical blanking periods or interleaved with screen refresh during the display period.

HIGH PERFORMANCE AT LOW COST.

The SY6545 allows maximum hardware/software design trade-offs. With its multiple mode operation, minimum component systems can be achieved without sacrificing performance. With fewer components, you get higher reliability. And lower systems cost. Add to this the fact that a second source is readily available for the proprietary SY6545 CRTC and you’ve got an unbeatable combination.

Our 6545 CRT Controller offers these standard features:
- Alphanumeric and semi-graphic capabilities
- Fully programmable display formats
- Interlaced or non-interlaced scan
- Fully programmable cursor
- External light pen capability
- Up to 16K RAM addressability
- Binary and row/column memory addressing
- Refresh memory can be slaved to CRTC
- Transparent RAM addressing allowing memory updates during horizontal/vertical blanking periods; interleaved during display period; and other modes
- Scrolling capability
- Internal status register to simplify system designs

UPWARD COMPATIBLE TO MC6845.

The SY6545 is plug-in replaceable with Motorola’s MC6845, working in all systems designed for the MC6845—without the need for system modifications of any kind. That’s compatibility. And more, too. Because the SY6545 does even more than the MC6845, operating in more modes and possessing additional features above and beyond the MC6845. That’s upward compatibility.
ACIA and Baud Rate Generator. A choice like no other.

WE'VE MADE IT SIMPLE.

Our 6551 Asynchronous Communications Interface Adapter is the world's most comprehensive ACIA. We made it that way by designing-in simplicity. It interfaces directly with 6500/6800 microprocessor families. And we've kept it small by eliminating unneeded synchronous protocols and conventions.

BENEFITS, PLUS SOME.

It all adds up to higher reliability, lower manufacturing cost and lower system cost. Among the 6551's features are:
- Single +5 V power supply
- Requires only a standard 1.8432 MHz external crystal
- Non-standard user-provided baud rates at 16X external clock frequency (up to 125 kilobaud)
- Stop bits: 1, 1.5 (5-bit word) or 2
- Independently selectable transmit and receive baud rates
- Parity (odd, even, none, mark parity, space parity)
- Double-buffered transmitter and receiver
- Half or full-duplex operation
- Serial echo mode
- Interrupt feature and status register

ON-BOARD BAUD RATE GENERATOR.

The 6551's on-chip programmable baud rate generator eliminates the need for external components and features 15 programmable rates up to 19.2 kilobaud. For non-standard baud rates (up to 125 kilobaud) the 6551 allows the use of an external 16X clock. This wide-ranging programmability allows accommodation of a variety of applications—from point-of-sale, financial and intelligent terminals to front end processors, remote data concentrators, computer-to-computer links and more. Whatever your communications application, the 6551's built-in versatility delivers.

The 6545 CRT Controller and the 6551 ACIA can do the job for you in terminal applications. Put them to work with Synertek's high performance 6500 series microprocessors and memory products, and a high performance intelligent terminal for your needs is only a designer's inspiration away.

Find out how we can help you meet your needs. For information on the 6545 CRT Controller and/or the SY6551 ACIA, fill out the coupon or contact Clement Lee, Microprocessor Group, Synertek, Inc. 3001 Stender Way, Santa Clara, CA 95051. (408) 988-5614. TWX: 910-338-0135.

We've made it in production. We're making it in high technology.
Interactive design of device package and cable connector for coupling solid state light sources and detectors to optical fiber cables is said to result in greatly improved light transfer between active device and fiber, a rugged semiconductor package well suited to high volume production, and a simple efficient interconnection. The new system is the result of a joint design effort by Motorola Semiconductor Products, Inc., PO Box 20912, Phoenix, AZ 85036, and AMP, Inc., Harrisburg, PA 17105.

Light emitting or detecting semiconductor chips are packaged in a resilient plastic ferrule which becomes an integral part of the optical interconnecting system. An optical fiber strand contained in the ferrule package, and pigtailed to the active area of the semiconductor die, extends to the highly polished surface of the ferrule for optimum light transfer. An Optimate fiber optic connector mates directly with the semiconductor package to provide efficient coupling to all major commercially available fiber cables. An increase of device-to-fiber coupling efficiency of up to 50 times that of some current systems is claimed. Measured performance includes speeds to 30M bits/s and operation on systems of 1-km length.

Light-coupling aperture of the semiconductors is an 0.008" (204-μm) diameter core with a numerical aperture (NA) of 0.48. Connector coupling losses to a like fiber are typically 2 dB. Coupling losses due to mismatched diameters or NAS are easily calculated and the amount of light coupled into the cable from the emitter or into the detector from the cable can be readily determined. The devices will be available in the second quarter of 1979 and include one light emitting diode and four detectors.

The Optimate connector compatible with these devices can be bulkhead or PCB board mounted and is less than 0.3" (7.6-mm) high for use between PCB boards located on 0.5" (12.7-mm) centers typical of computer applications. The metal connector provides effective electrical shielding; snap-on shields afford further EMI/RFI protection for critical receiver circuitry. The connector accepts all-glass and plastic clad silica fibers down to 125 μm diameter.

Circle 380 on Inquiry Card

Hybrid Switching System Adapts to Variety of Communications Modes

System EDX, a fully electronic computer controlled switching system for digital communications, handles such data switching applications as time-division circuit, packet, and store and forward. The system has been designed by Siemens Corp., 186 Wood Ave S, Iselin, NJ 08830, to meet CCITT and U.S. Telex, telegram, data, and packet switching standards for public and private data networks.

Hardware for the system basically consists of line terminators, communications controller, a central processor (CPU) from the DEC PDP-11 family to control the communications hardware and peripherals, and the peripherals themselves. A system status panel provides visual indication of system condition, plus visible and audible alarm signals.

Software comprises an operating, and a maintenance system. Operating system includes a control system and switching programs to run the EDX, and language processors and utility programs based on individual requirements of specific EDX systems. Maintenance system is used to commission and maintain an exchange, and consists of test and diagnostic programs to monitor all of the hardware.

As a circuit switch, EDX can be used as a concentrator, terminal exchange, tandem or transit exchange, international gateway, a combination of all four, as well as a PABX. In the circuit switching mode the system can switch asynchronous and synchronous data at speeds to 9.6k bits/s. Manual switching positions are available as required primarily for operator-assisted international traffic.

A data transfer technique that does not load the CPU during the call connect phase assures a high call setup rate, as well as a data throughput of about 400k char/s per switching block, a rate equivalent to about 1500 simultaneous duplex connect...
Pack 10 to 120 megabytes in a unit one-third the size of conventional disk drives.

For OEMs and system builders, the D100 family of compact disk drives offers a surprising list of advantages. Two new models, D140 and D160 add capacity and flexibility to the proven performance of the D120. The D140 includes a 10MB fixed platter in addition to the 1OMB removable cartridge as used with the D120. The D160 uses a sealed (non-removable) module which includes low pressure heads and carriage.

Small Size: Occupying approximately one-third the volume of conventional drives, models D120 and D160 measure 5.6" x 12.2" x 21.8". Model D140 is slightly taller at 6.7".

Innovative Cartridge: Both D120 and D140 models use a flat, thin (1" square by .9") self-ventilated cartridge weighing only 2.8 pounds.

Common Interface: The same controller handles D120, D140, D160, or any combination of the three models. One or more D160's in conjunction with a D120 provide a fixed data base with a high-throughput-10MB load-dump yielding twice the operating flexibility at half the size of conventional single-spindle drives.

High Density/Speed: Up to 7300 BPI, 600 TPI; 920 kilobytes/sec transfer rate.

Accuracy: Data-imbedded servo-tracking techniques assure accurate head positioning and full cartridge interchangeability.

Low Power Consumption: From 100 to 130 watts depending on model.

Reliability: Simplified mechanisms rule out any need for preventive maintenance. The spindle-mounted dc motor is brushless. There are no belts or pulleys, no blower, no transducer, no thermal compensation device. And no head alignment is required. MTBF is 5000 hours for models D120 and D140, 8000 hours for the D160.

Look us up at NCC.

CIRCLE 19 ON INQUIRY CARD
Hardware structure of EDX switching block. Each block can terminate up to 4032 subscriber and trunk lines in any combination. Basic block structure consists of communications hardware, central processors, and peripheral devices. Modular system concept permits several switching blocks to be interconnected through communications bus so that exchanges of as few as 100, to more than 20,000 line terminations can be implemented.

Multimode Tester Checks Data Systems Parameters

An 11-lb (5-kg) portable test instrument for comprehensive onsite checking of data communications systems, the 832 data comm tester operates in four modes: monitor, simulate, echo, and repeat.

In monitor mode, the set will record both data terminal equipment (DTE) and data communications equipment (DCE) either synchronously, asynchronously, or, with proper option, HDLC, as well as record status of key interface lines. In simulate mode, the 832 simulates modem operation, and can send a message.
"100% packaging from AMP allows us to utilize virtually any cable our design requires. Without need for board redesign."

"100¢ packaging from AMP equals unlimited flexibility of cables and headers."

**COAXIAL RIBBON CABLE**
AMP Connectors/Assemblies—
the world’s only mass terminated coax cable.

**DISCRETE WIRE**
AMPMODU Connectors—
The industry’s most versatile packaging system.

**WEBBED CABLE**
AMPMODU Connectors—
Both standard and high pressure contacts assure reliable contact with .025² posts.

**TWISTED PAIR CABLE**
AMP Latch Connectors—
Make termination quick, easy and reliable with the AMP shuttle tool.

**ROUND CONDUCTOR RIBBON CABLE**
AMP Latch Connectors—
Precision tooling makes daisy-chain assemblies in minutes.

**FLEXIBLE CIRCUITRY**
AMP Flexible Flat Cable Connectors—
For transmission cables and custom flexible circuits.

**RECTANGULAR CONDUCTOR FLEXIBLE CABLE**
AMP Flexible Flat Cable Connectors—
Ideal for applications requiring 3 amp current capability.

**ROUND CONDUCTOR BONDED CABLE**
AMP Latch Connectors—
For all standard cables on .050" centers.
"Compatibility with the industry’s broadest line of headers is the reason why."

Headers
- The Industry’s most complete selection—more than 4,000 different variations.
- Barrier inserts allow mixing several connector styles and sizes in one header.
- Accept polarized and detent connectors.
- Panel feed-thru headers for connecting two cable types.

AMP Latch Connectors
- Mass terminates round conductor ribbon cable.
- Redundant duplex-plated contacts and heavy duty strain relief/cover for reliable electrical and mechanical performance.
- Polarization and positive latching for accurate mating to headers.
- Cable-to-cable, edge card, DIP, and receptacle connectors available.
- Mate with AMPMODU headers.

Flat Cable Connectors
- Terminates flat rectangular conductor cable and flexible circuitry.
- Rated for 3 amp current capacity.
- Crimp-on, snap-in contacts are automatically machine applied.
- Housings accept both flat cable and discrete wire.
- Reliable solution for repeated cable flexing applications.
- Mate with AMPMODU headers.

Coaxial Ribbon Cable/Connectors
- Upgrades signal integrity without requiring board redesign.
- Unique AMP cable/connector system allows mass stripping and mass termination for low applied cost.
- 50, 75 and 93 ohm cable on .100" centers.
- Mate with AMPMODU headers.

AMPMODU Connectors
- For discrete wire and webbed cables.
- Complete system for board-to-board and wire-to-board interconnects.
- Polarized housings with strain relief and detent.
- Mate with AMPMODU headers.

Check Reader Service Number 89
“AMP termination equipment and technical service bring out the best in .100¢ packaging.”

Both the AMP Latch and AMPMODU product families include a broad range of application tooling that helps to lower applied costs in today’s .025" technology.

AMP Latch tooling, for example, includes universal bench mounted applicators as well as simple hand tools. They all have the capability of terminating virtually all popular types of round conductor flexible cable.

AMPMODU tooling includes manual and automatic printed circuit board insertion machines and terminating equipment. Each provides production efficiencies and uniformities that increase the value of a wide range of end products.

AMP technical assistance can also help increase product value and we urge you to take advantage of it. It’s available without obligation.

For more information on AMP Latch, AMPMODU, Coaxial Ribbon, and Flat Cable Connectors, call Customer Service at (717) 564-0100 or write AMP Incorporated, Harrisburg, PA 17105.

AMP has a better way.
to the DTE and record its response. In echo mode the unit will accept and record data directly from the DTE and record the same data for display. In repeat mode the instrument will send data repeatedly to the DTE or can be programmed to repeat the transmission only on receipt of a preselected trigger character from the terminal.

In any mode the set operates on either full or half duplex lines with characters from five to eight bits long, with odd, even, or no parity. Baud rates are switch selectable at 13 popular rates between 50 and 9600 bits/s, or can be synchronized to either the DTE or DCE system clocks. An optional self-test adapter allows diagnostic routines to be run beyond the standard routines to assure proper instrument operation.

The instrument was designed by Tektronix, Inc, PO Box 500, Beaverton, OR 97077, to fill the gap between sophisticated analyzers priced from $6k to $12k and the simple status monitors priced at $50 to $200. Basic price for the 832 is $1595.

Software Package Enables Packet Network Access

RDOS X.25 protocol permits ECLIPSE®, NOVA®, and micronova™ computers to access national and international public packet-switched networks, and also supports point-to-point communications between these computers. Availability of the package was recently announced by Data General Corp, Route 9, Westboro, MA 01581. The protocol operates under the real-time disc operating system (RDOS®), realtime operating system (RTOS®), and disc operating system (DOS®). It supports all three levels of CCITT Recommendation X.25, the internationally accepted packet switching protocol.

Public packet-switched networks include Telnet in the U.S., Datapac in Canada, and Transpac in France.

Telnet and Transpac have certified rdos X.25, and certification is in process for Datapac.

RDOS X.25 is supported by DC/CS communications subsystems including synchronous line multiplexers and the DCC/200 data communications controller. Data link control is supported by the link access procedure (LAP), a level of X.25 that specifies the software interface to enable the user's data terminal equipment (DTE) to exchange data with the network's data circuit-terminating equipment (DCE). Physical and electrical interface between DTE and DCE is defined by CCITT Recommendation X.21 bis, the standard EIA RS-232-C interface. The interface is full duplex, character level connecting the DTE to packet-switched networks via high speed synchronous lines up to 56k bits/s.

Nobody else has LSI-11 and LSI-11/2 cards like these.

Our digital cards are loaded with unique features such as the ability to use I/O lines as either inputs or outputs in increments of eight, up to 64 TTL inputs or outputs interfaced directly to the LSI-11 bus, the ability to detect contact closures on discrete input lines, and discrete latched outputs with the capability to drive high current incandescent lamps.

The Bus Repeater Card accommodates more devices than the basic bus can handle. The Bus Translator Card allows LSI-11 peripherals to operate with a Unibus CPU.

Both high level and low level analog cards are available with features like direct thermocouple digitizing, 250V CM isolation, six gain codes, up to 64 channels, and program control interface to mention just a few.

ADAC Corporation, 15 Cummings Park, Woburn, MA 01801 (617) 935-6668.
Design of an electronic technology involves selection of components and design of interconnect, packaging, and power systems. All of these elements interact, and choices made in one area affect the others. Exploration of tradeoffs centered around the power system, and specifically the choice of component power, and of linear regulated versus switching power supplies provides designers with useful insights into packaging problems and potentials.

Relationships between components, power, and volume are described by two equations.

\[
\text{Power required by components} = \text{Power supplied by supply} \quad (1)
\]

\[
\text{No of components} = \frac{\text{Available Cabinet Volume}}{\text{Volume/Component} + \text{Power Supply Volume/Component}} \quad (2)
\]

If parameters are assigned these symbols:

- \( V \): Cabinet volume—the product of outside cabinet dimensions
- \( f \): Fraction of cabinet volume usable for components, fans, and power supplies
- \( n \): No of components
- \( p \): Power/component (W)
- \( d \): Component density on PC boards (components/in² or/cm²)
- \( s \): PC board spacing in cabinet (in or cm)

\( V_p \): Power supply volumetric efficiency (in³/W or cm³/W)

\( V_c \): Cooling fan volumetric efficiency (in³/W or cm³/W)

then Eq (1) becomes

\[
\frac{d \cdot p \cdot f \cdot V_c}{s} = \frac{f(V - V_c)}{V_p + V_c} \quad (3)
\]

where \( f \cdot V_c \) is the volume occupied by components and \( f(V - V_c) \) is that occupied by the power supply and cooling system.

Using these same parameters Eq (2) becomes

\[
\frac{n}{s} \cdot \frac{f \cdot V}{d + p(V_p + V_c)} \quad (4)
\]

A graphical solution to Eq (3) is given in Fig 1, using the parameters described in the illustration. The line sloping up from the left demonstrates how component power requirements increase as the cabinet volume occupied by components increases. That sloping up from the right shows how supplied power increases as cabinet volume occupied by the power-cooling system increases. These lines intersect at a point where 6363 components occupy 5.85 ft³ (0.165 m³) of cabinet volume and dissipate 827 W of power.

Switching power supplies have \( V_p = 1 \) in³/W (16.4 cm³/W). Fig 2 illustrates that the use of such a supply increases the cabinet's component capacity by 21%.
The NEC Static Withstand.

It keeps man-made lightning from knocking out our printers.

People walking on nylon carpet can easily generate thousands of volts of static electricity—enough to knock out mainframes, cause head crashes and create costly printer failures.

Most electronic operations in computer products use only 5 to 10 volts of energy. When someone with high static energy touches such a product, equipment failure can occur unless that energy is siphoned off quickly and safely.

That's why NEC designed and built into its Spinwriter™ character printers and Trimliner™ band printers the industry's most complete static electricity withstand system. Some standard NEC printers have been independently tested with 20,000-volt jolts of static electricity and not missed a single print cycle.

The NEC withstand system starts with an aluminum frame and die-cast cover set—a massive electrical ground. It puts large protective ground planes on all circuit boards and it installs more than 25 ground cables and straps throughout each printer.

The result: a man-made lightning bolt can be dissipated in thousandths of a second, while Trimliner and Spinwriter operations continue uninterrupted.

NEC goes to greater lengths to build better grounding systems into its printer products. But then, NEC wants to build perfect printers. Send for our new printer brochures.

NEC. Going after the perfect printer.

NEC Information Systems, Inc.

Eastern Office: 5 Millis Drive; Lexington, MA. 02173. (617) 862-3120
Central Office: 3400 South Dixie Drive, Dayton, OH. 45439. (513) 294-6254
West Coast Office: 8509 S. Sepulveda Blvd., Los Angeles, CA. 90045. (213) 670-7346
Southern Office: 2965 Flowers Rd. South, Atlanta, GA. 30341. (404) 458-7014

CIRCLE 21 ON INQUIRY CARD
Now, there's a minicomputer tape system with the ability to handle NRZI (800 bpi), PE (1600 bpi), and GCR (6250 bpi) with just one drive and one formatter: The STC 1950. But it's a lot more than a tri-density subsystem. The microprogrammed drive and formatter are designed to give you total flexibility for matching your architecture, and for meeting your customer's price-performance requirements.

For example, you can order the 1950 in lower-cost PE/NRZI or PE/GCR configurations, then field up-grade to tri-density whenever your customer desires. The 1950 also gives you a choice of 50, 75, or 125 ips. And again, the system can be field converted to any other speed.

Up to four tape drives can be radially attached to the 1950's formatter. In a multiple-drive subsystem, the formatter can handle a mixture of speeds and densities. What this means is the flexibility to offer customers the precise configuration they need. Yet, at the same time, the 1950 keeps your design costs, training requirements, and parts inventories to an absolute minimum.

Read/write reliability you can bank on.

To assure the most accurate read/write technology, STC has incorporated into the 1950 all the experience accumulated while becoming the world's leading manufacturer of high-performance tape subsystems.

For example, a unique, two-phase digital tachometer in the capstan motor provides precise tape positioning and stop-lock control. As illustrated, two sensors discriminate the position of leading and trailing edges of each of 1000 tach lines to establish a capstan accuracy of 5650 millionths of an inch. The stop-lock feature prevents the capstan from moving more than one tach line when the drive is stopped. So no tape creep can ever occur.

For speed control, tach pulses are compared to a crystal clock pulse. This approach dispenses with potentiometers, making the system adjustment-free.

The gentlest possible tape handling.

The STC 1950 is equipped with automatic thread/load, for both open reels and easy-load cartridges. This feature, combined with a minimum length, straight-shot, gravity-assisted tape path, assures extraordinarily accurate tape loading. Tape acceleration is kept to a minimum by a microsequencer-controlled linear reel...
The new STC 1950: Three densities and any of three speeds in one state-of-the-art tape subsystem.

servo system. Tape drag and tape edge damage is minimized by the use of hydrostatic air bearings at all critical points. A hydrostatic rewind foot prevents tape and head wear during high speed rewind. And a unique STC tape footage counter, in conjunction with the digital tach and microsequencer, smooths tape acceleration and deceleration for faster and gentler rewind.

New standards of maintainability.
When you specify the 1950 you benefit from all the cost-effective maintenance features developed to service STC's mainframe tape systems.
As an OEM customer, you'll receive, at no charge, a host-independent, on-line diagnostic program that performs over 700 tests. This includes not just functional and reliability tests, but artificial stress testing and fault isolation to uncover potential problems that are often masked by GCR's inherent fail-soft characteristics.

For off-line diagnosis, your service people can use the STC Subsystem Analyzer. This microcomputer-controlled analyzer runs the same test routines as the on-line program, and includes a remote communication capability to facilitate diagnostic assistance from a central point.

On-line or off-line, this diagnostic approach keeps labor costs to a minimum. Typically, it takes less than an hour to find the problem, swap the components, and verify the fix.

To get the full story, get in touch with us today.

For full details, please contact: OEM marketing, Storage Technology Corporation, P.O. Box 6, Louisville, Colorado 80027. Or phone (800) 525-2940; in Colorado 497-5151. In Canada: STC Ltd., 272 Galaxy Blvd., Rexdale/Toronto, Ontario M9W. Phone (416) 675-3350.
When it comes to flat, we've been around.

We make more different kinds of planar cables for more different kinds of interconnect systems than anyone on the planet Earth. And, in this world of planar-come-lately's, Spectra-Strip has been around since the cable world turned flat.

For all your interconnect needs from planar cables to IDC connectors to complete custom assemblies, just check us out. We'll take total responsibility for solving your interconnect problems, and you won't need to call anyone else.

For the name and number of our nearest distributor or rep, write Spectra-Strip, an Eltra Company, 7100 Lampson Avenue, Garden Grove, CA 92642. Or call (714) 892-3361 today.

When you're down to the wire

CIRCLE 23 ON INQUIRY CARD
Use of low power ssr and msi Schottky components may reduce average component power requirements from 0.13 to 0.035 W/component. The graph also shows that the use of such components with a linear supply increases cabinet capacity to 10,178 components; their use with a switching supply increases capacity to 10,987 components, a 73% increase over the initial design.

From these graphs much useful information can be gained, and can be applied to individual design problems. The gains in real component density that may be achieved in a system by the use of low power components or switching power supplies, either (or both) of which increase density by reducing power supply volume is particularly dramatic. With the assumptions given here, the use of low power components is more effective than the use of switching supplies in improving effective component density. However, this result is attained in part because of the assumed cooling fan requirement of 2 in$^3$/W (32.78 cc/W).

The proportion of cabinet volume occupied by the power/cooling system ranges from 15 to 50% of the total. It can be shown that this proportion is solely a function of the ratio $(V_p + V_c)/(s/dp)$—of power/cooling to component dissipation volume requirements.

The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—Ed.
There's a lot of noise out there about the 8086. A lot of noise. And all of it's coming from Intel.

But even with all the pages of advertising, all the claims, all the chest-beating, there's one little fact Intel forgot to mention.
The 8086 isn't the best 16-bit CPU. The AmZ8000 is.
The AmZ8000 is the beginning of a product line. The 8086 is the end. It's nothing but a souped-up version of the 8080 and 8085.
The AmZ8000 has a more powerful, more advanced, much more flexible architecture than the 8086. It also has more addressing modes, more general-purpose registers, larger addressing spaces, better I/O capability and more powerful instructions. It can even accommodate more data types. And the AmZ8000 has a lot higher throughput using standard NMOS than the 8086 using HMOS.

Worried about software? Don't be.
The AmZ8000 is cheaper and easier to program than the 8086.
But it won't just save you money; it'll save you time. You'll be able to develop new
programs faster than ever before. That means you'll be able to get new products to market faster than ever before.

And to speed things up even more, we designed a software development system especially for the AmZ8000. It combines versatile hardware with powerful software. And it’s got a real catchy name: the System 8/8.

One last thing: we know it hurts to drop Intel for somebody else. We’ve just been through it ourselves. But it’s going to hurt a lot more next year and the year after that. By then your competitors could be so far ahead of you, you might never catch up.

Call Advanced Micro Devices and we’ll send you all the facts on the AmZ8000.

Then quietly and calmly, in the privacy of your own office, compare the AmZ8000 with the 8086.

We think you’ll agree with us: Intel may make a lot of noise. But the AmZ8000 makes a lot of sense.
Micromodular Architecture Upgrades Performance Of Medium Scale Computers

'900' series systems provide five times the performance of their predecessors, occupy half the space, and use 50% less power. Burroughs Corp., Detroit, Mich. 48232 has enhanced performance of the machines through use of dense logic and memory circuits coupled with a micromodular concurrent central system architecture.

Providing twice the processing power of the B 2800, the entry level B 2930 uses a fast asynchronously operating modular processor. Its 524k-byte memory expands to 1M bytes using 16k mos chips. This system includes a separate data communications processor, and a microprocessor based, integrated disc controller. Equipped with from 2M to 5M bytes of main memory and up to 32 data link processors, the B 3950 provides up to five times the throughput of the B 2800.

Data link processors control flow of data to and from peripheral units. These independent microprocessors are each programmed to service a specific category of peripheral devices. By assuming overhead associated with 1/o functions the processors free the cpu for more efficient operation.

Memory in both systems is formed of 16k-bit memory chips with error correcting capability. Wide bandwidth enables the processor to fetch four bytes of information simultaneously, providing fast access to programs and data. Logic circuits are advanced Ttl bipolar microcircuits, containing as many as 800 gates each. Logic speed is augmented by high speed control devices that make instruction codes available to the processor in 45 ns.

Micromodular concurrent architecture of the systems provides a central system made up of independent processing elements or modules, each dedicated to specified steps in the overall task. Functions for each respective task are stored in micrologic circuits. The modules run concurrently, each at its own maximum rate. As a result the computer can use all resources at peak efficiency to maintain a consistently high throughput rate.

Functional units of the central processor include program, control, memory access, execution, and memory control modules, and data buffer, i/o processor, data link processors, memory, and logic units. The program module prefetches program instructions, analyzes operations, calculates data addresses, and passes the translated instruction information to the address buffer. The buffer holds the instruction until the control module accepts and processes it, and then passes addresses, size, and formats of the operation to the memory access module.

All data or memory accesses required by the execution module are performed by the memory access module, which stores or retrieves data in the data buffer. Specified arithmetic, logic, and special operations are handled by the execution module with the data buffer acting as a temporary store and work area for data that have been processed or are waiting to be processed by the execution unit.

Memory requests from the memory access module and i/o processor are coordinated at the memory control module. The i/o processor independently moves data between main memory and peripheral devices. It uses an i/o descriptor to manage the entire i/o operation.

The systems are fully compatible with the company's other medium scale computers. Software products required for system operation are packaged together and are available for a license fee. A basic package includes Master Control Program vi, an enhanced version of Burroughs Network Definition Language, a Generalized Message Control System, and a compiler for RPG II, ANSI COBOL, FORTRAN, or BASIC.

Additional software available for this class of computer includes a workflow management system and a data management inquiry system. The workflow system permits the user to control execution of jobs consisting of interrelated tasks, and assign system resources to jobs for execution concurrently, based on classification and priorities. The inquiry system allows users to access information stored in the dbs 11 database.

Vector Graphic Systems Reduce Host Overhead Through Use of Technology

Ease of interfacing, software, modularity, and multiterminal and remote capabilities are emphasized in the Whizzard 7000 and 5000 vector refresh graphic systems. Developed by Megatek Corp, 3931 Sorrento Valley Blvd, San Diego, CA 92121, the families encompass graphic peripherals, graphic terminals, and stand-alone graphic processing systems, and are based on building block modularity.

A self contained system, the 7000 is based on the dual bus architecture of the company's Megraphic 7000 terminal (see Computer Design June 1978, pp 39, 42). A proprietary vector generator and an Adaptive Timing" technique produce fine vector control and capacity for 20,000 short vectors, increased throughput, quality, and repeatability. The vectors have constant intensity; precise endpoint matching is ensured by a patented vector closure feature. Readability down to very small character sizes is provided by the use of stroke generated characters, which can be rotated, scaled, or translated at any angle with full precision of the rotate-translate circuitry.

An internal 32-bit bipolar microprocessor provides the high data processing rates necessary for interactive graphics applications, processing both X and Y information simultaneously. The 3-state 32-bit graphics bus insures that data transfer occurs at optimum rates. Peripheral i/o devices occupy a separate 16-bit bus.

The system's parallel interface uses programmed i/o or dma control, connecting to DEC PDP-11 or Data General NOVA or ECLIPSE. A Universal Interface module allows connection with IBM Series/1, Hewlett-Packard, VAX 11/780, Interdata, and Prime computers.

An intelligent peripheral control unit (IPCU) updates location counters, recording cursor location and making the data available to the cpu only when necessary, thus reducing the overhead loading needed to service peripheral interrupts. The IPCU serves to interface joystick, data tablet or digitizer, and keyboard to the system.

Three-dimensional graphics capability includes rotation, 2D and 3D can be obtained simultaneously on the same display. An optional color
The WHIZZARD™ will amaze you.

Graphics magic you never had before.


Buy a WHIZZARD refresh terminal. Connect it to your computer. Buy a WHIZZARD intelligent terminal. With built-in computing power. Or, buy a stand-alone graphics processing system. With the WHIZZARD's powerful FORTRAN-based graphics software, you're up and running fast.

Add an RS-232-C interface for remote or distributed processing. Up to four monitors for shared graphics processing. Plus all the graphics peripherals you may need.

Two WHIZZARD families. It's your choice.

Choose the WHIZZARD 7000 for unmatched graphics throughput and versatility. With features like hardware rotate, zoom, and multiple viewports. And easy interfacing to any 16-bit or 32-bit computer. Or, the WHIZZARD 5000 for the lowest-cost, high-performance graphics possible. Every 5000 system includes its own NOVA/ECLIPSE computer.

Plus, TEKTRONIX™ users can get complete 4014™ compatibility with our Emutek™ software. It's the easy, economical way to upgrade from storage tube graphics.

For the whole WHIZZARD story, write or call Pat Burke, MEGATEK, 3931 Sorrento Valley Blvd., San Diego, CA 92121. (714) 455-5590. TWX: 910-337-1270. (European office: 14, rue de l'Ancien Port, 1201 Geneva, Switzerland. Phone: (022) 32.97.20. Telex: 23343.)

The Visible Difference

MEGATEK CORPORATION

CIRCLE 25 ON INQUIRY CARD

See the WHIZZARD at NCC, booth 3319-27.
If you’re building an application-specific workstation, start with a Beaver. This new intelligent terminal supplies all the hardware and software you need to get your workstation up and running in record time. For as little as $2995 in quantity.

**Optimize your workstation layout.**

The Beaver comes in three hardware modules: CRT display, detachable keyboard, and mass storage. These independent modules let you human engineer your workstation for peak efficiency.

Put the CRT in front of the operator or to the side. Place the keyboard near the display or away from it. Make the optional floppy disks accessible or lock them up. If space is at a premium, the Beaver modules can be stacked in a compact, single unit.

The Beaver gives you the flexibility to optimize your workstation to fit your needs.

**Fast program development.**

The Beaver comes with plenty of sophisticated software, to help you write your application system quickly.


And communications software for the Beaver is outstanding. You get sophisticated emulators for TTY, 3275, 2780/3780, and more.

**Unbeatable I/O performance.**

I/O throughput is not a problem with the Beaver. Each floppy disk has its own DMA channel and controller.

An optional I/O processor makes it easy to add special devices. Two slots, complete with power, are ready for you to add interfaces to OCR wands, bar code readers, or whatever extra peripherals your workstation application requires.

Need graphics? A special hardware module gives the Beaver 720-by-256-point resolution graphics capability.

**Special terms for system builders.**

At Perkin-Elmer, we designed the Beaver with the features that system builders need. But we didn’t stop there.

We’re offering comprehensive terms and conditions, generous quantity discounts, service warranties, international service coverage, and the kind of support that volume buyers have come to expect from the industry leader.

Our new Beaver joins more than 300,000 other Perkin-Elmer peripherals that are working right now in systems around the world.

**Free brochure.**

To find out more, just give us a call or write. Perkin-Elmer, Randolph Park West, Route 10 & Emery Avenue, Randolph, NJ 07801. (201) 366-5550. We’ll send you our free brochure about the Beaver. The workstation builder.
IT TOOK POWER-ONE TO DO IT...

a switching power supply as dependable as a linear.

When Power-One decided to build a switching power supply, we issued one simple mandate: it must be as dependable as our linears. Well, we did it. A direct drive 5-volt 40-amp switching power supply that's smaller, lighter, simpler, more reliable and less expensive than the rest.

Direct Drive Switching

By using a self-driven switching stage, we've done away with the starting bias, drive and the current sensing transformers. A big reduction in weight plus lower cost, more precise drive control and fewer input to output noise paths. To assure maximum protection against AC line transients and fluctuations, a unique "volt-second" regulation circuit is employed.

Safeguard Design

We've built in a number of safeguards. Like our digital feedback system which yields exceptional loop stability while maintaining positive control of critical switching parameters. And a unique anti-saturation circuit to protect the power transistors from the dire effects of transformer saturation. Plus, by putting inputs at one end of the supply and outputs at the other, we've eliminated inter-circuit cross talk. And speaking of inputs, our dual range design permits either 115 or 230 VAC operation without changing jumpers.

The Bottom Line

Switching frequency: 28KHz — stable as a rock.
Size: a mere 4.88 x 13 x 2 inches — more watts to the inch and more power for the buck. The price: $250 for single units.

Send for complete details. Or better yet, contact your local Power-One representative for immediate action.
With Minicomputers
Adapts GCR To Use
Magnetic Tape Formatter

The
ries out magnetic tape drive
was able to simplify the system suf-
9600
ers. By incorporating this formatter,
cording to be used with
decoding, enabling group coded

Terminal configurations are
ic system,
ible with Data General

monitor provides up to five colors in
16 bits of user definable, user pro-
grammable line texture. Any line
texture may be blanked, doubling
the total line texturing capacity of
the system.

Hardcopy output is facilitated by
a vector to raster converter imple-
mented in hardware. The Raster-
zier™ processes vectors, randomly
converting from an unordered vector
list into raster bit data for the plot-
er, eliminating the need for the host
to order vectors prior to printing.

An interactive total refresh graph-
ic system, 5000 series standalone and
terminal configurations are compat-
ible with Data General ndos, DOS,
and RTOS operating systems. The
system has a self contained NOVA
or ECLIPSE with 32k-words memory,
dual floppy disc drive, and RS-232
interface.

The dual board mc552 graphic
display unit uses hardware routines
to speed vector processing and mini-

ize host processing time. As a DMA
device the graphic display unit re-
ceives coordinates directly from the
computer's memory. Precise analog
stroke writing offers typical endpoint
matching and closure of 0.005"
(0.0127 cm), 16 levels of intensity
control, and constant vector intensity.

Three-level self-diagnostics allow
troubleshooting without outside test
equipment. Subsystem operation can
be verified at the formatter panel
keyboard in offline mode independent
of external test equipment. First
level diagnostic operation supplies
the cpu with a continuous perfor-
man ce report and alerts it in the
event of fault. A second level, off-
line mode, allows self test routines
to be called by the technician to
verify individual module integrity.

The formatter's microprocessor ex-
cutes these test routines stored in
internal memory, polling individual
microsequences associated with each
module as test patterns are routed
through the module to verify proper
handling. The third level uses the
cpu in a dedicated diagnostic mode
and provides approximately 50 in-
terface test messages. The first part
of this diagnostic verifies the csm bus/
cas memory interface and formatter
control path. The second part checks
the various modules, submodules,
and individual circuits of the for-
matter.

Circle 402 on Inquiry Card

3-Terminal Module
Reduces Current Drain
For Standard Keyboard

A 3-terminal Hall effect keyboard
module combined with an integral
microcomputer reduces current drain
for a standard 64-module keyboard
by 140 mA. Replacing the customary
4-terminal module to achieve the
60% reduction in current, the 3T
module was developed by Micro
Switch Div, Honeywell, Inc, 11 W
Spring St, Freeport, IL 61032, as a
logical outgrowth of the keyboard's
microcomputer capabilities.

In the 3T module the input termi-
nal also serves as a minus supply
connection. The module integrates
with the onboard microcomputer's
scan capabilities permitting applica-
tion of power to only eight key mod-
ules at a time during a scan cycle.

Additional production economies
are offered by the reduced size of
the 3T Hall effect chips, helping to
hold the line on prices without af-
fec ting traditional features and per-
formance. The modules use the same
variety of keytops provided since the
Hall effect keyboards were intro-
duced. Yet power requirements are
reduced from the 1 A specified for
a typical 64-key device to the 140
mA specified for keyboards using the
3T modules.

Other economies that are incorpo-
rated in the keyboards are material's
that permit use of a punchable single

Circle 401 on Inquiry Card

Magnetic Tape Formatter
Adapts GCR To Use
With Minicomputers

The F6250 intelligent formatter car-
rries out magnetic tape drive man-
agement and GCR/PE encoding and
decoding, enabling group coded re-
cording to be used with minicompu-
ters. By incorporating this formatter,
Pertec Computer Corp, Pertec Div,
9600 Irondale, Chatsworth, CA 91311,
as was able to simplify the system suf-

Southwest

23 61 61 7

Digit al Te chno lo gy Review

ficiently to meet use and service
needs of the minicomputer market.

An important feature of the main-
tenance concept is the simplicity of
the t/o structure. Most tape depen-
dent functions have been built into
the formatter, relieving the host cpu
and magnetic tape controller of con-
siderable demands. The formatter
interface communicates with the host
cpu over a 28-line bus: a 16-bit
control/status/data bidirectional bus,
five common address space address
lines, and six handshake control lines.

Constant vector intensity of Megatek's Whizzard
graphic system is produced by turning off beam
precisely as it passes through B. Beam continues
on in undefined manner (a) and finally settles at
point B'. After appropriate setup time, beam be-
gins from B' and moves toward C. As it passes
precisely through B, beam is unblanked and vector
is drawn toward C where cycle repeats. Stroke
generated characters (b) take advantage of pre-
cision of vector generator, producing readable
characters even at sizes below 0.1 in
The S2114H 4K at 70ns it'll help you your competition.

With 70, 90 and 120 nanosecond access times, our S2114H VRAM family will give you the speed you're looking for in the 1024 x 4 organization you need. (For those really fast applications, there's a 55 ns version on the way.)

So, if your application requires small cache or buffer memories, you're in for a quick boost in performance. With a sharp reduction in cost and board space.

You'll no longer have to overbuild your system with 4K x 1 memories or fill up four times as many boards with 1K x 1 parts.

This 18-pin VRAM is fully TTL compatible on all inputs and outputs. It has a single +5V power supply. It's completely static. And the chip select function makes it easier to expand your memory system by allowing the I/O pins to be OR-tied to other devices.

High speed runs in the family.

Our entire family of 4K Static VRAMs is geared toward high speed and low power dissipation. That's the beauty of VMOS.
Static VRAM: run away from

And it extends to our 16K and 64K VROMs, too. (As well as the S2147 and S4017 4K x 1 parts which are coming soon.)

So check out our family tree. Then call your local AMI salesman or one of these authorized distributors for fast delivery: Arrow Electronics; Bowtek Electric Co., Ltd.; Century Electronics; Cesco Electronics, Ltd.; Future Electronics; Intermark Electronics; Kierulff Electronics; Parrott Electronics, Inc., Resistacap; R/M Electronics; R. V. Weatherford; Schweber Electronics; Sterling Electronics; Western Microtechnology. Or get in touch with us at AMI Memory Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330.

A lot of people have been waiting for the S2114H. So put in your order fast.
Satellite processors models 8660 and 8661, optional peripheral processing units, increase the processing capabilities of ECLIPSE S/250 processors (see Computer Design, Oct 1978, p 30) from Data General Corp, Rt 9, Westboro, MA 01581. The units operate as frontend or independent processors significantly offloading the CPU. Both include two circuit boards of independent processor logic, memory and I/O buses, and implement the standard ECLIPSE instruction set with powerful extensions.

General purpose satellite processor model 8660 consists of 64k bytes of parity MOS with memory allocation and protection (MAP) capability, a microprogrammed processor with 200-ns cycle time, an independent CPU compatible I/O bus, software controllable console, and interface for bidirectional data transfer between S/250 and satellite processor. The satellite's instruction set consists of the basic ECLIPSE set plus character instruction set that facilitates bit, byte, and data string manipulation and translation.

Model 8661 with a fast hardware array processing extension consists of 56k bytes of parity MOS memory and MAP, 8k bytes of high speed bipolar array processing memory, processor logic, I/O bus, and S/250 interface. Array processing instructions common to the HP/130 and the CPU's integral array processor option are added to the basic ECLIPSE instruction set.

Configured on the S/250 high speed data channel, the satellite processors act as I/O devices. Each has its own independent I/O bus for programmed I/O and data channel transfers. Both support a cross interrupt facility with the S/250 for interprocessor synchronization.

Using MAP software control, the satellites direct memory reference instructions in the satellite program to local memory or to the host S/250 main memory. This facility also exists for data channel DMA references from devices on the satellite's private I/O bus, permitting both high speed interprocessor data transfer as well as enabling data sharing and routing.

Software supports the enhanced system for realtime event-driven and interactive environments. Tasks running under VTOS in the S/250 can bidirectionally communicate and transfer data with tasks running under VTOS in the satellite processor. Programs can be written in global
Guaranteed Compatible!
S-100 Bus OEM Boards
From SD Systems at reasonable prices

Single Board Computer (SBC-100)
Video Display Board (VDB-8024)
Flexible Disk Drive Controller (Versafloppy)
64K Random Access Memory (ExpandoRAM)

ASSEMBLED TESTED AND FULLY BURNED IN

The search is over for the convenience of S-100 Bus Computer boards that are really compatible and dependable. State-of-the-Art engineering, outstanding flexibility, rapid delivery, and low costs make the SD Systems computer boards the best OEM buy. The SBC-100 Single Board Computer is based on the Z80 microprocessor. Up to 8K of 2716 PROM, Serial RS-232 Port, Parallel Input/Output Ports, Software programmable baud rate generator, Four channel counter/timer, and 1K of RAM, all on-board. VDB-8024 Video Display Board features an on-board Z80 microprocessor for maximum flexibility in video control. 80 characters by 24 lines, displayed with high resolution on a 7 x 10 dot matrix. On-board Keyboard power and interface, 2K memory and a glitch-free display by use of I/O mapped interface make this board the most superior board on the market.

The ExpandoRAM is available in 16, 32, 48, or 64K versions using 4116 RAMS. The population can be increased in the field at a future point if requirements change. Featuring Switch selectable boundaries, Bank Selectable Write Protect and using less than 5 watts, the ExpandoRAM is more reliable memory for the money than any other OEM board. Versafloppy, Flexible Disk Drive Controller with IBM 3740 soft sector-ed format compatibility controls up to four single or double sided disk drives either mini or standard size. Full Line Software includes Editor, Z80 Assembler, Linker, C-Basic, Complete Business Packages, System Diagnostic and Control Software and Disk Operating System. PROM Programming Software and Hardware also available. Circle the reader service number for full Technical Data... or call toll free to our Customer Service Department: 800-527-3460.

POST BOX 28610 — DALLAS, TEXAS 75228

CIRCLE 28 ON INQUIRY CARD
Should you specify solid state or hard contact?

ASK CHERRY.

We make both.

When you ask Cherry about keyboards, we'll tell you about our solid state (capacitive) style—a simple switch idea with no bounce constraints that enables a 110 key matrix to be scanned every millisecond. We'll also tell you about our hard contact (gold crosspoint) style that has proven so reliable in so many different applications for over a decade.

We'll also tell you which approach will best meet the unique requirements of your application. Such factors as encoded or non-encoded, number of keys, lighted positions... and more. This is particularly important since keyboard applications vary so greatly in complexity and use that there really isn't any one style of keyboard or one technology that's best for all.

Which keyboard technology is best for you? Ask Cherry. Since we make both, we won't try to talk you out of either one.

Hard contact or solid state? Standard or custom design? Sloped, stepped or sculptured keys? Cherry makes 'em all.

Send for our colorful new 36-page catalog that lets you see 'em all. Includes details, data, output codes and specs on both solid state and hard contact keyboards... plus keyboard switches... keycaps... and more.

See Us At
NATIONAL COMPUTER CONFERENCE
June 4-7, 1979
New York Coliseum
CHERRY BOOTHS 1022-1024
DO WE HAVE A LOT OF MEMORIES TO REMEMBER?

SURE THING!

In fact, we have a Hitachi memory device available for almost every application need. Just look at the next page for proof.

We manufacture everything from 1K CMOS all the way through our million-bit bubble memories. The list goes on and on. And so does our commitment to new and future product development.

But our wide choice of part types isn't the only thing that should keep us memorable.

It's the added value you get with every Hitachi order. Value in proven quality and reliability. In availability. In competitive pricing. In total customer service and attention.

Hitachi value. That's what makes our memories so hard to forget!

Call your local Hitachi representative or distributor for more information. Or call (800) 323-6713.

(Samples, detailed data sheets and catalog are available on written request on your company letterhead.)
# Memories to Remember

## MOS RAM

<table>
<thead>
<tr>
<th>Type</th>
<th>Operation</th>
<th>Process</th>
<th>Organization</th>
<th>Access Time (ns max.)</th>
<th>Cycle Time (ns min.)</th>
<th>Supply Voltage (V)</th>
<th>Power Dissipation (mW)</th>
<th>Pins</th>
<th>Package</th>
<th>Replacement</th>
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<tbody>
<tr>
<td>HM4627-2</td>
<td>Dynamic</td>
<td>NMOS</td>
<td>4096 x 1</td>
<td>150</td>
<td>375</td>
<td>+12, +5, -5</td>
<td>462 max.</td>
<td>24</td>
<td>*</td>
<td>MK427-2</td>
</tr>
<tr>
<td>HM4627-3</td>
<td>Dynamic</td>
<td>NMOS</td>
<td>4096 x 1</td>
<td>200</td>
<td>375</td>
<td>+12, +5, -5</td>
<td>392 max.</td>
<td>16</td>
<td>*</td>
<td>MK427-3</td>
</tr>
<tr>
<td>HM4704-4</td>
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<td>NMOS</td>
<td>4096 x 1</td>
<td>200</td>
<td>375</td>
<td>+12, +5, -5</td>
<td>392 max.</td>
<td>16</td>
<td>*</td>
<td>MK427-4</td>
</tr>
<tr>
<td>HM4716A-1*</td>
<td>Dynamic</td>
<td>NMOS</td>
<td>16384 x 1</td>
<td>120</td>
<td>375</td>
<td>+12, +5, -5</td>
<td>462 max.</td>
<td>16</td>
<td>*</td>
<td>MK4115-2</td>
</tr>
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<td>NMOS</td>
<td>16384 x 1</td>
<td>150</td>
<td>375</td>
<td>+12, +5, -5</td>
<td>392 max.</td>
<td>16</td>
<td>*</td>
<td>MK4115-3</td>
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<td>NMOS</td>
<td>16384 x 1</td>
<td>200</td>
<td>375</td>
<td>+12, +5, -5</td>
<td>392 max.</td>
<td>16</td>
<td>*</td>
<td>MK4115-4</td>
</tr>
<tr>
<td>HM4816*</td>
<td>Dynamic</td>
<td>NMOS</td>
<td>16384 x 1</td>
<td>100</td>
<td>200</td>
<td>+5</td>
<td>440 max.</td>
<td>16</td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>HM46810</td>
<td>Static</td>
<td>NMOS</td>
<td>128 x 8</td>
<td>450</td>
<td>450</td>
<td>+5</td>
<td>370 max.</td>
<td>24</td>
<td>*</td>
<td>MCM6810</td>
</tr>
<tr>
<td>HM4668A10</td>
<td>Static</td>
<td>NMOS</td>
<td>128 x 8</td>
<td>360</td>
<td>360</td>
<td>+5</td>
<td>420 max.</td>
<td>16</td>
<td>*</td>
<td>MCM 68A10</td>
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<tr>
<td>HM4687-2*</td>
<td>Dynamic</td>
<td>NMOS</td>
<td>4096 x 1</td>
<td>45</td>
<td>45</td>
<td>+5</td>
<td>700 max.</td>
<td>18</td>
<td>*</td>
<td>2147-3</td>
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<tr>
<td>HM4687-3*</td>
<td>Dynamic</td>
<td>NMOS</td>
<td>4096 x 1</td>
<td>50</td>
<td>50</td>
<td>+5</td>
<td>840 max.</td>
<td>18</td>
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<tr>
<td>HM47124AF-2</td>
<td>Static</td>
<td>NMOS</td>
<td>1024 x 4</td>
<td>100</td>
<td>100</td>
<td>+5</td>
<td>330 max.</td>
<td>18</td>
<td>*</td>
<td>2114-3</td>
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<tr>
<td>HM47124AF-3</td>
<td>Static</td>
<td>NMOS</td>
<td>1024 x 4</td>
<td>200</td>
<td>200</td>
<td>+5</td>
<td>893 max.</td>
<td>18</td>
<td>*</td>
<td>2114-4</td>
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<tr>
<td>HM483101</td>
<td>Static</td>
<td>CMOS</td>
<td>256 x 4</td>
<td>550</td>
<td>650</td>
<td>+5</td>
<td>142 max.</td>
<td>18</td>
<td>*</td>
<td>5105-1</td>
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<tr>
<td>HM483101V</td>
<td>Static</td>
<td>CMOS</td>
<td>256 x 4</td>
<td>650</td>
<td>650</td>
<td>+5</td>
<td>160 max.</td>
<td>18</td>
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<tr>
<td>HM48345P</td>
<td>Static</td>
<td>CMOS</td>
<td>4096 x 1</td>
<td>550</td>
<td>630</td>
<td>+5</td>
<td>83 max.</td>
<td>18</td>
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<tr>
<td>HM48147P-3</td>
<td>Static</td>
<td>CMOS</td>
<td>4096 x 1</td>
<td>70</td>
<td>70</td>
<td>+5</td>
<td>184 max.</td>
<td>18</td>
<td>*</td>
<td>2147</td>
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<tr>
<td>HM483103</td>
<td>Static</td>
<td>CMOS</td>
<td>4096 x 1</td>
<td>70</td>
<td>70</td>
<td>+5</td>
<td>184 max.</td>
<td>18</td>
<td>*</td>
<td>2147</td>
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<tr>
<td>HM483103P</td>
<td>Static</td>
<td>CMOS</td>
<td>4096 x 1</td>
<td>55</td>
<td>55</td>
<td>+5</td>
<td>184 max.</td>
<td>18</td>
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## Bipolar RAM

<table>
<thead>
<tr>
<th>Type</th>
<th>Level</th>
<th>Organization</th>
<th>Output</th>
<th>Access Time (ns max.)</th>
<th>Cycle Time (ns min.)</th>
<th>Supply Voltage (V)</th>
<th>Power Dissipation (mW/bit)</th>
<th>Pins</th>
<th>Package</th>
<th>Replacement</th>
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<tbody>
<tr>
<td>HM2106</td>
<td>ECL</td>
<td>256 x 1</td>
<td>Open Emitter</td>
<td>15</td>
<td>16</td>
<td>5.2</td>
<td>1.6</td>
<td>16</td>
<td>*</td>
<td>F0415A</td>
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<tr>
<td>HM2110</td>
<td>ECL</td>
<td>1024 x 1</td>
<td>Open Emitter</td>
<td>35</td>
<td>16</td>
<td>5.2</td>
<td>0.5</td>
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<td>*</td>
<td>F0415A</td>
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<tr>
<td>HM2110-1</td>
<td>ECL</td>
<td>1024 x 1</td>
<td>7</td>
<td>8</td>
<td>8</td>
<td>5.2</td>
<td>0.8</td>
<td>16</td>
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<td>F0415</td>
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<tr>
<td>HM2112</td>
<td>ECL</td>
<td>1024 x 1</td>
<td>Open Collector</td>
<td>70</td>
<td>70</td>
<td>+5</td>
<td>0.5</td>
<td>16</td>
<td>*</td>
<td>90415</td>
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<td>HM2111</td>
<td>TTL</td>
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<td>Open Collector</td>
<td>70</td>
<td>70</td>
<td>+5</td>
<td>0.5</td>
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<td>3-state</td>
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<td>45</td>
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## MOS ROM

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<th>Type</th>
<th>Program</th>
<th>Organization</th>
<th>Access Time (ns max.)</th>
<th>Supply Voltage (V)</th>
<th>Power Dissipation (mW)</th>
<th>Pins</th>
<th>Package</th>
<th>Replacement</th>
</tr>
</thead>
<tbody>
<tr>
<td>HM462716</td>
<td>Erasable &amp; Electrically</td>
<td>NMOS</td>
<td>2048 x 8</td>
<td>450</td>
<td>+5</td>
<td>385 max.</td>
<td>24</td>
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<tr>
<td>HM46830</td>
<td>Mask</td>
<td>NMOS</td>
<td>1024 x 8</td>
<td>500</td>
<td>+5</td>
<td>683 max.</td>
<td>24</td>
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<tr>
<td>HM46532-3</td>
<td>Mask</td>
<td>NMOS</td>
<td>4096 x 8</td>
<td>600</td>
<td>+5</td>
<td>440 max.</td>
<td>28</td>
<td>*</td>
</tr>
</tbody>
</table>

*Preliminary

* C: Side brazed ceramic

G: Ceramic

P: Plastic

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CIRCLE 30 ON INQUIRY CARD
optimizing FORTRAN S/1, DCL, or assembler.

Both models include an 8-slot system module that accommodates processor, memory, internal cables, and up to six (8660), or three (8661) I/O device controllers. Each unit can be expanded to support up to 10 I/O device controllers with an 8-slot I/O system module 8652. Four satellites in any mix can be supported by an S/250.

Circle 404 on Inquiry Card

Performance of Expandable CPU Doubled in Intermediate Range

By boosting the performance of the CPU used in the M80 series, Magnuson Computers, 2500 Augustine Dr, Santa Clara, CA 95051, has provided the capability to upgrade a single computer throughout IBM's intermediate computer performance range. The M80 series (see Computer Design, Aug 1978, pp 47-48) is based on the strategic architecture concept, giving it its open ended expandability. Performance, memory capacity, and data channel capacity are extended through addition of PC modules and modifications to firmware control programs.

Extensions to the series provide two models that are claimed to be higher in performance than the 4331 and one that lies between the 4331 and 4341. All are remotely maintainable, include diagnostic processors, and have main memory expandable.

Graph illustrates areas where company feels systems' relative performance and costs are competitive with IBM units.
Bells and whistles standard.

When you buy our 300 Series Ballistic™ Printer, there's one thing we won't offer you much of. Options. Because we made most of them standard on the 300. And lowered its price, too.

**NOT MANY OPTIONS. BUT A LOT OF STANDARDS.**

The new 300 Series Ballistic Printer is a low-cost, 180 cps matrix printer with a built-in microprocessor. It gives you 15 switch selectable form lengths, 15 perforation skips over formats, and full horizontal and vertical tabulation control. Space and blank character compression. Interface control for serial, parallel, or polling and addressing operation. X-ON, X-OFF, capability. Plus a non-volatile forms retention system that retains these programmable settings when power to the printer is turned off.

The 300's character buffer is optionally expandable to 2048 characters. With it, the printer can fully buffer a 1920 character CRT screen of data without waiting for the screen to transfer to the printer on a line-by-line basis.

**THE 300 HAS A GOOD HEAD ON ITS SHOULDERS.**

Like all our Ballistic Printers, the 300's dependability originates with its ingeniously simple, patented Ballistic Print head. Instead of moving cores attached to the wires, it uses small armatures that propel its matrix wires in free flight to the platen.

This revolutionary principle greatly reduces drag. Minimizes wire tip wear. Eliminates clogging with inks, dust, and paper fibers. And most importantly, significantly increases head life. When the head finally does wear out, you can replace it yourself. In minutes. Without a single service call.

**IT HAS PRACTICALLY EVERYTHING. EXCEPT A BIG PRICE TAG.**

The 300 Series has a full 96 ASCII character set, with up to 128 printables optionally expandable to two sets of 128. Which makes it great for bilingual applications. It's even got an elongated character capability, and 10 or 12 pitch standard, with a 10/16.5 dual pitch option. Not to mention 100% duty cycle operation.

On top of that, you get the whole package for a measly $1995. Honest.

After all, we couldn't print it if it wasn't true.

**300 SERIES Ballistic Printer**

**Tougher in the long run.**

Lear Siegler, Inc./Data Products Division, 714 Brookhurst Street, Anaheim, CA 92803; (800) 854-3805. In California (714) 774-1010. TWX 910-591-1157. Telex: 65-5444

CIRCLE 31 ON INQUIRY CARD
to 16M bytes. Existing M80/3 and /4 processors join with the /32, /42, and /43 in competing with IBM's recently announced 4300 and existing System/360 and /370 systems. All five of these units are upgradable.

Model M80/32 provides performance said to be three times better than that of a 4331; and models /42 and /43 offer performances cited to recently announced respectively. Existing /4 converts to performance said to be three times better power line are elements; additional channels are than that of a 4331; and models /42 to 16M bytes. Existing M80 /3 and /43 in competing with IBM's re-

Circle 405

Intelligent CRT Terminal Combines Modularity With Program Development Aids

Introducing the concept of the Data Station, the 3500 is a modular intelligent CRT terminal designed for incorporation into OEM designed workstations. Embodied in the terminal are a range of communications emulators, interactive processing capability, fast access local mass storage, friendly operating system software, and CRT display and keyboard for operator I/O.

The unit, called the Beaver by Perkin-Elmer Corp, Terminals Div, Randolph Fk W, Rt 10 Emery Ave, Randolph, NJ 07801, provides powerful program development aids and I/O performance features. Designed for use in distributed and standalone dedicated data processing, the station can include 12" (30.5-cm) CRT display, detachable keyboard, up to 2 floppy disc units with 160k bytes of online storage, 48k bytes of RAM in 16k-byte increments, 30k bytes of ROM, and provides overlapped I/O, device independence, and shareable I/O devices. Downline loading facilities are available without floppy disc.

System software comprises multitasking disc operating system; extended BASIC interpreter with commercial and scientific extensions including string manipulators, double precision arithmetic, and array and matrix operations; macroassembler; line editor; and 3275, 2780/3780, and TTY communications emulators. Utility and file management programs include automatic file expansion; and a powerful command substitution facility is provided.

A significant functional feature of the unit is inclusion of two fully powered extra PC board slots. The task of interfacing additional hardware to the operating system is simplified by the provision of a high performance SMART DMA interface which can be used to connect to any workstation related hardware such as bar code readers or OCR wands. Overlapped I/O is obtained by having each floppy disc on a separate DMA channel.

Device independent I/O answers the need for changing peripheral devices. Device assignment and task establishment from the keyboard or from within tasks allow the development of a 3780 terminal for interactive application packages. The PETOS multiprogramming operating system for the microprocessor based unit is stored in a 30k-byte ROM, eliminating the need for startup and reload procedures. A 25th line on the 24-line CRT screen area functions as the system console, eliminating the need to interrupt the display with operator messages.

The unit can be programmed in BASIC, assembly language, or using a macroassembler. Program development is further aided by source statement and task generation, a complete file management system that offers automatic file expansion, generalized copy, disc verify and dump, directory, and backup utilities. A DEBUG allows setting of multiple breakpoints, facilitates snapshot dumps, and permits examination and alteration of memory and register contents. An optional hardware debugger provides for stop-on-address capability and produces a map of the 128 most recently executed instructions.

Communications software includes an asynchronous TTY emulator, bi-synchronous terminal manager, bi-synchronous downline loader, 3275 emulation of commands, and a 3270 emulator in both single and multidrop versions. A set of FORTRAN IV routines is available that can cross assemble any Motorola 6800 S-format output into a format compatible with the data station; or generate code on one of the company's 32-bit minicomputers and load it directly.

A standard unit with dual floppies is priced at $3995 in quantities of 50. A down loading version without disc storage is priced at $2995 (same quantity). Units are currently available for delivery.

Circle 406 on Inquiry Card

The end is near.

See page 215
XEROX
INTRODUCES
THE
BEGINNING
OF
A NEW CENTURY.

Century Data Systems (formerly CalComp's Memory Products Division).
Emerging again as a most respected name in mass storage. Now as a subsidiary company of Xerox.
The new Century is beginning with the hottest team in the business.
People who have made Trident the industry's most reliable, maintainable storage module disk drive.
People who have brought low-cost Winchester technology into the OEM world with the Marksman.

And people who, with the Hunter, bring big disk economy, performance and reliability to cartridge users.
Clearly, this Century will bring you a lot to look forward to.

See us at NCC, Morgan Suite, New York Hilton Hotel.
Simple doesn't have to mean unsophisticated. The proof is in our new CRT terminal, the HP 2621. Before building it, we took a long, hard look at the way you use a simple terminal. Then we took the knowledge gained in more than 10 years designing computer products and applied it to engineering an interactive character-mode CRT terminal from the user's point of view.

The outcome was actually two models. The HP 2621A, which sells for $1450. And the HP 2621P, which has a built-in printer, costs $2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.

Try this on your favorite CRT! With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

To make numeric data entry faster and easier, we put the 2621's numeric keypad right in the middle of the keyboard. And the 2621's familiar 68-key keyboard is almost as easy to use as a typewriter.

☐ I'd like to know more about HP's new 2621A and 2621P with built-in hard copy.
☐ I'd like to see HP's new 2621A and 2621P with built-in hard copy.
☐ I'd like to know more about HP's complete family of terminals.

Name ____________________________
Title ____________________________
Company _________________________
Address __________________________
Phone ____________________________

Mail to Hewlett-Packard, Attn: Ed Hayes, Marketing Manager, Data Terminals Division, Dept. 1247, 19400 Homestead Road, Cupertino CA 95014.
iple sophistication.

**DISPLAY**
- High resolution CRT
- Character per-pixel character underline
- Insertion and deletion control

**NGC**
- Full page (40 lines)

**HIGH RESOLUTION**
- 120 character per-second thermal printing
- Uppercase/lowercase letters, control codes, underlining
- Automatic word wrapping

**CASE OF USE**
- A screen-based control system
- Sort configuration

**EDITING**
- Character mode editing (Modify Mode Line Mode)
- Character and line-insert and delete
- Clear line display
The new Intecolor 3621.

Desk top computing will never be the same.

From Intelligent Systems Corporation, the company that developed color graphics at black and white prices, comes a sophisticated new design that will put dynamic, efficient color at the fingertips of everyone who uses a desk top computer. The Intecolor 3621.

It's an advanced concept that combines all the features one could want in a microcomputer. Color. Graphics. Power.

Reliability. Performance. Style. All in a sleek, compact package. At a price that's irresistible.

Eight brilliant colors speed comprehension and communication on an ample 13” screen. The unit has the capability of displaying 32 lines of 64 ASCII characters, as well as plotting graphics on a 128 x 128 grid. Vector software is built in. As is a 51K mini-disk drive, 16K of user RAM expandable to 32K and 16K of Extended Disk BASIC ROM. And a Standard RS-232C Terminal Mode allows interfacing with time sharing units.

That's a lot of flexibility. And it's only the beginning.

In fact, the 3621 is just the prelude of the possibilities that will explode into reality when Intecolor's new 300 series is introduced at the National Computer Conference. Be there when the fireworks go off.

See us at Booth 4806 at the NCC Show in June.
Midrange Computer Family Includes Multiprocessor Configurations

Up to 67% higher performance and lower prices are offered by additions to the 8500 series from NCR Corp., Dayton, Ohio 45479. In addition to multiprocessoring machines that provide the power and reliability necessary in transaction processing environments, the company has reduced prices on memory, provided further unbundling of software, and extended customer software services.

All systems use the virtual resource executive (VRX) operating system that provides full dynamic resource allocation as well as virtual memory without rigid memory partitioning. V-8500M systems accommodate VRX-MP which offers multiprocessing capabilities. Multiprocessing versions of the systems feature up to four tightly coupled processors that share all system resources. The VRX-MP system provides the ability to link different processor models in a single multiprocessing complex, allowing implementation of multiprocessing involving processors with different performance characteristics.

Improved transaction processing is obtained through the use of parallel multitasking techniques in VRX. This provides more parallel operations of critical software segments. The MP version can be implemented with no operator retraining. It incorporates concurrent online diagnostics, multiple remote job entry, and enhanced online program development features.

By conforming to the Migration Path Engineering design philosophy, the systems allow programs, files, and peripherals to be moved from current 8400 and 8500 series units without time consuming conversion effort. Internal bus architecture provides a flexible high speed data path to which all components attach. Extensive use of ECL circuits, 370-ns read/440-ns write RAM, and bit serial link 1/0 capable of transferring data in a serial bit stream at 16M bits/s further extend performance.

Largest member of the family, the V-8585M is a 56-ns mainframe with from 2M to 6M bytes of main memory. It offers 65% greater performance than the 8580 at a price about 20% lower—$375,000. Consisting of two -8585Ms and offering about 1.7 times the throughput of a single processor system, the V-8585M is available at $810,000.

With 2M to 4M bytes of memory and 56-ns processor, the V-8575M has 24% more processing power than the V-8570 at 37% less cost. Two tightly coupled V-8575M processors make up the V-8575MP and provide 70% more processing power.

Offering 45% more power than the V-8560, the V-8565M has from 1M to 3M bytes of main memory, and sells for $140,000 in a 1M-byte version. In a multiprocessor configuration with two tightly coupled processors and from 2M to 6M bytes of memory, the 8565MP has a price of $340,000.

Also offered are V-8555M and MP versions with from 0.5M to 4M bytes of memory, and an -8400 series machine, the V-8455 which supplements the current V-8400 family. This machine operates under VRX with 0.5M to 1M bytes of main memory and offers 90% of the power of a -4331 at 73% of the price.

Circle 407 on Inquiry Card

English-Like Language For Data Base Management On Small Computers

An application development foundation system, SIMILE (Software Intensive Micro-Processing System) fully integrates OODASYL-like database management with query and reporting facilities. Developed by Small Business Machines, Inc., 527 Madison Ave, New York, NY 10022, the system is effective both standalone and as a node on a network.

Based on English-like commands, the conversational system runs on 64k and larger machines. Commands enable the user to define, create, access, maintain, and query a data base. Easy on-and-offloading between system data bases and disc files combine with communication routines to allow interface between mini/micro and mainframe.

Heart of an application is a set of data bases and their subsystems with cross-referencing keys. Each data base is a file of individual records in a standardized format. Complementing this database structure is the command system. Responses to the original prompt allow the user to create or modify the schema file which establishes the database structure; to enter, change, or delete information in the database, or to query or produce reports; to erase a data base; or to exit the system. Each of these actions initiates a dialog in which the system accepts commands, specific information, and alternatives or parameters.

For the system builder, the software provides a general solution to a large number of common situations and problems. By identifying the elements of the structure as they apply to the particular situation, providing detailed descriptions of the character, and supplying organization of the particular items and reports, the builder creates a solution to his problem through the system.

Circle 408 on Inquiry Card

Graphic Processing Systems Speed Design and Manufacturing Cycles

Graphic processing systems HITAC G-710 and -730 increase efficiency of design and manufacturing by providing speedy response and easy operation. Hitachi, Ltd, No. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100, Japan, developed the systems specifically for shortening the design and manufacturing processes using CAD and CAM systems. The G-710 intelligent graphic terminal system is used as a remote terminal, forming part of a centralized large scale processing system. It operates a CAD system requiring large volume interactive computation and is particularly suited for improving efficiency in the design process. Easy operation is provided through use of input methods such as menu command and symbolic command based on a graphic tablet. A distributed computer graphic system, the G-730 uses its own small computer for application programming, and operates a CAD system in interactive mode. Suited for automation of machine parts drafting, the system is capable of graphic 1/0 and interactive modifications without user programs.

Substantial graphic processing programs as well as basic and extended support programs are supplied for the system. These provide capabilities for processing graphic 1/0, modifications, and additions and deletions, without program changes or modifications. Operation is through the graphic tablet as well as programmed function keys and macrocommands.

Circle 409 on Inquiry Card
Computer Mainframe Extends Memory Capacity to 8M Bytes

Extending performance of the OMEGA 480 line into the range of the IBM 3031, the model III, announced by Control Data Corp., Box O, Minneapolis, MN 55440, uses 16k MOS memory chips and ECL circuitry to pack 8M bytes of memory in a cabinet one-half the size of a System 370/158 with 1M bytes. Prices for the systems range from $360,000 for a 2M-byte unit to $540,000 for a machine equipped with 8M-byte memory.

Memory used in the systems is made up of 16k n-channel MOS chips and is expandable in 2M-byte increments to maximum capacity of 8M bytes. Existing models I and II can be field upgraded, providing current users with greater flexibility.

Standard input and output of data are accomplished through the use of one byte multiplexer and five block multiplexer channels. In byte mode maximum data transfer rate on the byte multiplexer channel is 50k bytes/s. Each block multiplexer channel transfers data at a rate of more than 1.85M bytes/s to provide a maximum data transfer rate on all channels of 7.5M bytes/s.

Deliveries of the model III are scheduled to begin in third quarter of this year. The systems are manufactured by IBM Systems, Inc, Bedford, Mass.

Circle 410 on Inquiry Card

IC Packaging Technology Raises Reliability While Lowering Costs

A premolded plastic chip carrier package not only satisfies the need for increased packaging density but also brings the economies of backend operations to the semiconductor packaging houses. Designed by AMP Inc, Harrisburg, PA 17105, as an integral part of a complete process, the technology includes machinery and equipment necessary to operate on a cost applied basis.

Allowing completely automated packaging of bipolar and MOS chips from die attach through marking and testing, the series of strip fed devices are designed to reduce manufacturing cost while substantially improving onboard density, termination reliability, and ease of diagnostics and repair. Population densities include 24-, 44-, and 68-position square packs. A floating outer lead structure provides reliable package to board termination.

The premolded package (PMP)² is a composite metal/dielectric assembly that includes a conductor lead frame and molded insulating body with one or more apertures for mounting microelectronic elements. All necessary plating operations are performed by the package manufacturer to eliminate plating or tinning by the user. Without a specific form factor, the PMP may be fabricated in forms that include conventional DIP, chip carrier types, and multi-component modules.

The encapsulation technique uses silicone gel encapsulation compounds that remain soft after full polymerization, assuring internal compliance and minimal stress build-up inside the package. Prior to application of silicone the area to be protected is cleaned and covered with a monomolecular layer of water. When the compounds are applied to the prepared surface the silicone molecules displace water molecules to form a chemical bond to the chip surface, preventing further bonding or mobility of water and ions across the surface and preventing corrosion.

Assembly options allow direct attachment of the semiconductor device to an external package element facilitating outward thermal transfer. Nominal power handling capabilities range from 350 mW to 10 W for various options.

A complete system of assembly, encapsulation, and finishing equipment incorporates features that include reel to reel stock handling, modularity, and adaptability to assembly options within the technology. Chip assembly and interconnection are based on existing industry techniques.

Circle 411 on Inquiry Card

Computer Series Adds High Performance, Large Capacity CPU

The AS/3-5, an extension to the Advanced System² family of processors from Itel Corp, Data Products Group, San Francisco, CA, has a processor cycle time of 115 ns and claims to offer 22% more performance than IBM's 4341. Functionally compatible with the IBM 4341, System/370 model 158-3, and with all of the company's Advanced Systems, the AS/3-5 is available with 2M bytes of processor storage and can be upgraded to 8M bytes in 1M-byte increments.

The combination of high performance 16k cache buffer and large memory capacity permits users to run the MVS operating system comfortably in addition to DOS/VS, DOS/VSE, OS/VS, svs, and VM/370. Other features include a microcoded processor with many of the assist features of the 3033 as well as IBM 1400/1700 compatibility, and hardware and firmware diagnostics used in the 370/158-3 and 1/188 as well as diagnostics developed exclusively for Advanced System processors.

Purchase price of the system is $800,000. Each additional megabyte of memory costs $75,000. The system is currently available for customer shipment.

Circle 412 on Inquiry Card
Xylogics Technology Produces the Quality Family of Disk Controllers and Subsystems

When you choose any member of the Xylogics family, you get performance for your most demanding application and reliability that sets a new standard for the industry. In a word, you get quality.

You also get flexibility, which has made Xylogics a leader in intelligent disk controllers. Xylogics broad range of disk controllers is continuously expanding to meet the growing list of popular mini and microcomputers being offered.

The Xylogics quality family includes:
- Model 410 SBC/Multibus Cartridge Disk Controller
- Model 510 DEC LSI-11® Cartridge Disk Controller
- Model 610 DEC PDP-11® Cartridge Disk Controller
- Model 810 Data General Nova/Eclipse Cartridge Disk Controller
- Model 211 DEC PDP-11 Storage Module Disk Controller
- Model 850 Data General Nova/Eclipse Storage Module Disk Controller

Systems designers know that the latest microprocessor technology goes into Xylogics controllers, insuring superior performance. Users of Hewlett-Packard, Varian, Interdata, Honeywell and many other mini/microprocessors may also find Xylogics technology applicable to their systems needs.

Regardless of your application, Xylogics technology delivers controllers and subsystems to match your exact specifications. For details, contact our Applications Department. Today.

® LSI-11/PDP-11 are registered trademarks of Digital Equipment Corporation.
Computers Control and Test Processes in Entire Pharmaceutical Tablet Manufacturing Facility

Automation can serve many purposes, many of which directly or indirectly benefit either workers or the public. In a munitions plant, it eliminates the need for humans in a potentially hazardous environment; in an engine fabrication facility, it enables heavy blocks of metal to be maneuvered without physical strain on people. However, in pharmaceutical fabrication facilities—in addition to providing desired precision—it minimizes the handling of chemicals and materials in areas where strict sanitary standards must be maintained in order to prevent contamination or reduction in quality.

The Elkton, Va, Pharmaceutical Laboratories facility of Merck & Co's Merc Sharp & Dohme Div is a prime example. Although similar but smaller plants are in operation in the U.S. and in Europe, when the Elkton facility was dedicated in October 1977 it was the first large scale computer controlled tablet manufacturing operation in the U.S.

Computer control is maintained on all steps in the production of one of the company's major prescription pharmaceutical products. With virtually no human handling of chemicals or processing materials during or between processing steps, the system automates movement of all necessary materials through the process; controls weighing, mixing, grinding, drying, lubricating, and blending of bulk pharmaceutical ingredients; compresses code-identified tablets; coats tablets with a water based solution; and provides partially computerized control of quality control testing of both raw materials and finished tablets.

The computer controlled tablet manufacturing process fills 21,600 ft² (2000 m²) in an 80-ft (24-m) high, 3-story (equivalent to an average 6-story) building area, with what is described as a "labyrinth" of equipment: sophisticated pharmaceutical manufacturing, material handling, and computer process control equipment. Included are machines for blending, granulating, drying, tablet compressing, and tablet film coating plus hoppers, tanks, bins, pipes, columns, vacuum and bucket conveyors, belts, coils, cables, valves, dampers, sensing devices, and alarms. An additional 113,000-ft² (10,500-m²) area in the 154,000-ft² (14,300-m²) facility is used for packaging, quality control, warehousing, receiving, shipping, maintenance, and mechanical operations.

The Production Process

Controlling element for the process is a Control Data Corp System 17 computer. Integrated within the system are approximately 240 sensing, regulating, and controlling devices; a communications system that includes visual display terminals and printers; and an 8 x 14' (2.5 x 4.3-m) backup panel that can become a manual control center if required. Hundreds of miles of wiring interconnect system components.

The computer regulates valves, dampers, motors, and belts to maintain flow and processing of materials and to control processing conditions within specified limits and ranges. Weights and rates of flow of chemicals, liquids, and tablets are checked by the computer via sensing devices at various stages of the process. In addition, the computer monitors temperatures, humidity levels, and pressures in both manufacturing and conveying equipment.

Movement of all solid and liquid chemicals, processing fluids, and, at later stages of the process, compressed and film coated tablets, is totally automated. For greater efficiency, the custom designed automated materials handling system incorporates vertical drops through pipes and columns to utilize gravity flow where possible, but uses pumps, vacuums, and bucket conveyors to accomplish upward and horizontal flow when necessary.

Chemicals flow by vertical drop from a third floor bulk loading station through a series of holding and feeding hoppers into blending equipment and finally to continuous granulating and drying equipment on the first floor (see simplified flow diagram). A vacuum system draws granulated powder from a first floor dryer through an 80' (24-m) high stainless steel column to the third floor for grinding and sizing.

Again by vertical drop, the components move through lubricating hoppers and blenders that add and blend chemicals to ease compressing, and into first floor compressing machines. As tablets are compressed to proper specifications for thickness, weight, and hardness, a code identification is added to each.

Bucket conveyors then carry the tablets up into hoppers that feed second floor coating columns. Finally, the finished tablets are placed in stainless steel tote bins for storing prior to packaging.

(Continued on page 74)
WHY PUZZLE OVER PIECES?

See the whole picture on Sanders' Graphic 7

Sanders' Graphic 7 provides the whole picture by drawing bright, crisp vectors and symbols so rapidly that you see all the data you want. Benchmark tests with actual time measurements have proven Graphic 7 to be the refreshed cost-performance leader. This performance spells results for your application.

Convenience? Chances are the Graphic 7 will interface directly to your minicomputer's parallel DMA channel or connect to your mainframe via an RS-232 time-share link. The Graphic 7 dual microprocessors will handle the graphics and let your computer do its job more efficiently.

At Sanders we build graphic displays to tough standards and we support them. The reliability of a solid product backed by a solid organization helps keep your job on track.

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Sanders Associates, Inc., Information Products Division, Daniel Webster Highway South, Nashua, NH 03061. (603) 885-5280; TWX: 710-298-1894.

CIRCLE 36 ON INQUIRY CARD
The SA4000 Fixed Disk Drive.
The SA4000 Series of rigid disk drives are the newest line of low cost mass storage products from Shugart. Our floppy disk drives have been the industry standard for years, and now our fixed disk drives are setting new standards of their own. Like the lowest cost per megabyte in their capacity range so you can have up-to-date Winchester storage at a price that won't bite into your system profits. That means real dollars and cents savings to help keep your system competitive. SA4000 drives are available in capacity ranges that are just right for most systems too—14.5 and 29 megabytes (unformatted). And when you design our drives into your system, you can be sure you've got a system architecture that's compatible with IBM S/32, S/34 and System 1 fixed/floppy architecture.

The head in cost per

Winchester Technology and Two Configurations.
Shugart fixed disk drives use industry-proven Winchester head and media technology to preserve your data in its own safe, sealed environment. The model SA4004, with 14.5 megabyte capacity, utilizes one disk and four heads. The SA4008, 29 mbyte version, has two disks and eight heads. Eight optional fixed heads are available to give you an additional 144 kbytes (unformatted) of head-per-track storage for applications such as indexed files or table look-up. The SA4000 Series offers an easy upgrade too. Keep your floppys for I/O and system back-up. Add our rigid disk drives for the additional capacity and throughput you need to upgrade your operating systems and mass storage.
When You Think Actuators, Think Fasflex II™. Shugart's new, proprietary Fasflex II™ is another result of Shugart's headstrong commitment to R&D. This open loop band actuator is virtually wear-proof, and it doesn't require any adjustments in the field. Heat dissipation? With Fasflex II it's extremely low—only 200 watts is typical. But the Fasflex II actuator is only one of the benefits you get with the SA4000 series. The drives weigh a mere 35 pounds—that's about half the weight of comparable units. They're compact. They use only 5.25 inches of panel space, they can be easily mounted in a 19-inch RETMA rack. The drives are rugged, yet easy to maintain. The PCB and spindle drive motor are open and accessible on the underside of the drive. No preventive maintenance is required.

of its class megabyte.

And if you're looking at the bottom line, SA4000 drives are easy to integrate into your system. The drives utilize a simplified interface which can be easily designed into your system. In addition, you can use the same power supply for both the SA4000 drives and floppy drives, since they have the same voltage requirements. Want to get on-line quick? Our new SA4600 controller handles up to four SA4000 drives with an option to control up to four single or double density floppy disk drives. Bottom line? Lower overall system cost. So now's the time to design a classy system with the head of its class—the compact, reliable, low cost SA4000. Shugart Associates, Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; West Coast Sales/Service: (408) 252-6860; Midwest Sales/Service: (612) 574-9750; East Coast Sales/Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 17-60-06.
Operators at stations in the "field" within the building monitor critical steps and communicate via 2-way radios with a process operator in the central control room. The field operators initiate the loading of bulk materials at the beginning of the process and conduct tests of the tablets at compressing and film coating stages. Materials are not permitted to pass these stages of the process until the computer has checked the in-
Simplified process flow diagram of materials handling steps in Merck Sharp & Dohme's computer-controlled pharmaceutical tablet fabrication plant in Elkton, Va. Multiple stages of process are shown here singly and some transfer lines have been deleted.

formation relayed from the field operators and determined that the overall process is functioning within bounds. Then signals from the computer initiate the next procedural steps.

Computer directed application of a Merck developed aqueous (water based) film coating solution takes place in massive plexiglass columns, rather than in traditionally used cylindrical coating pans. Each of four
Simplified process flow diagram of materials blending and tablet compressing and handling stages
Computer control room. 14' long panel at top of backup panel is complete flow diagram shown in simplified form earlier in this article. Merck designed backup panel can be used for manual control of process if necessary.

Closeup of control room console and CRT terminals. "Field" operators communicate via 2-way radio with process operator who interfaces with computer.

Quality control facility. Chemist uses Digital Equipment Corp PDP-11 minicomputer to control automated weighing and potency testing of finished tablets produced in automated process. Prior tests check incoming materials and production procedures.

film coating installations consists of a 6' (1.8-m) diameter plexiglass column positioned several feet off the floor. Compressed tablets are automatically conveyed and dropped into the column from the tablet feeding hoppers above.

Channeled air streams carry the tablets through a guide baffle and up through the center of the column to meet a computer directed spray of coating solution. Coated tablets emerge over the top of the baffle and cascade down, drying as they fall. This cycle is continuous over a specified process time.

The aqueous film coating solution is prepared in advance by computer control in an area directly beneath the film coating columns and is automatically delivered and sprayed into the columns during the coating process under computer direction. Washing and cleaning of pumps, lines, and tanks also is accomplished automatically under computer control.

Quality control procedures are automated under control of a Digital Equipment Corp PDP-11 minicomputer system. Incoming raw materials are subjected to both physical examinations and analytical tests for identity, purity, and quality before use in the manufacturing process. Then, all production operations are audited and inspected to assure compliance with procedures and controls. Finally, finished tablets must pass a battery of tests for weight, potency, purity, and stability as well as uniformity, disintegration, and dissolution.

In an automated packaging operation, bottles are filled with the proper number of tablets, cotton is added, and caps and labels are attached. Bottles of 100 are inserted in cartons, cartons are shrink wrapped with polyethylene and packed in cases, and cases are conveyed to a warehouse area—again all automatically. Bottles of 1000 are processed by a machine that automatically applies labels and thermoplastic pockets to the bottles, folds product circulars, and inserts the circulars into the pockets. These bottles are then individually shrink wrapped, case packed, and moved to the warehouse.

Software

In cooperation with Control Data Corp, Merck & Co's automation and control department developed AUTRAN, a FORTRAN like language that allows the plant engineer to write his program in a familiar form—such as start pump, stop motor, and open valve. Traditionally, pharmaceutical industry logic that specifies production sequence steps and control loop setpoints has been organized on sets of operator instructions called batch sheets. AUTRAN programs can be read almost as readily as the former batch sheets. This eases program and computer system checkout procedures. Currently, approximately 250 separate applications programs handle 22 simultaneous batches, run by the plant in 6 separate processes. However, for possible future expansion, the computer system is designed to accept up to 60 simultaneous batches in 30 processes.
The Maxi-Mini.
5¼" double-sided, double-density industry compatible mini-disk drive.

Maximum storage capacity in minimum space. Siemens offers a 500K byte capacity in a compact drive half the size of a standard 8-inch. And our plug-to-plug compatible Maxi-Mini disk drives are available for immediate delivery.

Siemens Maxi-Mini disk drives utilize Wangco technology which has been proven in over 20,000 installations. Available with either single or double head, these mini-disk drives also provide many other important features. Such as a true anti-crunch mechanism which prevents cover closure until the diskette is fully in place. This helps avoid data loss and provides a very real dollars and cents savings on disk replacement. There’s also a wide mouth which permits easier, more convenient insertion of media, shortening load/unload time.

Also available from Siemens are single- and double-sided 8" floppy disk drives and mini-disk controllers. For immediate delivery of the Maxi-Mini or information about other OEM products from Siemens, contact us at:

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CIRCLE 40 ON INQUIRY CARD
**Digital Control and Automation Systems**

**DC&AS Briefs**

Data Acquisition System Performs Several Additional Functions

A hardware and software programmable data acquisition system, the DataloggerPlus 6200 series also monitors, processes, computes, and performs interfacing functions. It is based on an M6800 microprocessor, handles both analog and digital inputs, and provides RS-232 and parallel outputs. The system provides 16 channels, expandable in 16- or 32-channel increments up to 128 in the basic unit, and 256 additional in each remote unit. Other features include 4k memory expandable to 32k, gain programmable inputs for each channel, digital calendar clock, high/low alarm capability for each channel, and 20-col alphanumeric printer. Dynatech R/D Co, 99 Erie St, Cambridge, MA 02139 provides turnkey configurations to individual customer requirements.

Circle 294 on Inquiry Card

Servo Drive/Digital Control Package Designed for Use with Programmable Controllers

Commander I, a closed loop positioning module, is claimed to be the first servo drive/digital control package for use with programmable controllers. It also can be used with dc motors and open loop numerical control systems. Introduced by Hyper-Loop Inc, 7459 W 79th St, Bridgeview, IL 60455, the 7 x 5 x 11.5" (18 x 13 x 29-cm) unit has resolution ranges of from 0.001" (0.0254 mm) to 0.00001" (0.000254 mm). Pulse frequency is up to 100k pulses/s and guaranteed closed loop control accuracy is ±2 pulses. A fault detector prevents runaway conditions that might be caused by loss of resolver feedback or stored command position.

Circle 295 on Inquiry Card

Peak Power Demand Control Systems Lower Energy Costs

Data on present and foreseeable utility rate structures as well as metering methods are maintained by microprocessors in two power demand control systems introduced by Dynapar Corp, 1675 Delaney Rd, Gurnee, IL 60031. These microprocessors permit control over a variety and mix of electrical loads for a wide range of industrial and commercial facilities to reduce peak power demand and thereby lower energy costs.

PDC-1100/1150 series systems can control from 8 to 32 separate loads in groups of eight. Each unit provides eight priority levels and each level can accommodated with 232 inputs and parallel outputs. The system provides 16 channels, expandable in 16- or 32-channel increments up to 128 in the basic unit, and 256 additional in each remote unit. Other features include 4k memory expandable to 32k, gain programmable inputs for each channel, digital calendar clock, high/low alarm capability for each channel, and 20-col alphanumeric printer. Dynatech R/D Co, 99 Erie St, Cambridge, MA 02139 provides turnkey configurations to individual customer requirements.

Circle 294 on Inquiry Card

From PERCOM - for Your Mini-Disk Drives...

Low Cost, Ready-to-Use Power Supply - 1-, 2- and 3-Drive Enclosures

the PS-401

Used on Percom's LFD and TFD series of 5½-inch mini-disk drives, the PS-401 power supply comes complete with ac power cord, dc connector, on-off switch and fuse. Install, plug into ac and your drive is ready.

The +5-volt and +12-volt outputs of the PS-401 are conservatively rated for most mini disk drives including Shugart's SA-400 and SA-450 models, Pertec models FD-200 and FD-250, Wangco models 82 and 282, MPI's model B51 and the MOD I and MOD II units manufactured by Micropolis.

The PS-401 features thermal overload protection and short-circuit current limiting. Operating ambient temperature is from 0°C through 40°C. Storage is from -22°C to 50°C.

Input for the domestic version is 117 Vac, 50-60 Hz, 0.5 ampere (max). Foreign country version operates on 230 Vac, 50-60 Hz at ¼ ampere (max).

Order PS-401 power supplies by calling Percom's toll-free number: 1-800-527-1592.

Drive Enclosures

These pre-drilled metal drive enclosures may be ordered in standard blue, silver or brown enamel finish. Other colors are optional. Rubber bumpers for desk-top operation are permanently attached.

Order 1-, 2- or 3-drive enclosures by calling Percom's toll-free number: 1-800-527-1592.

* Price is for 100 quantity. Unit price is $55.00 for domestic version, $70.00 for foreign version. Call for foreign version OEM prices.

† Price is for 100 quantity. Unit price is $29.95. Call or write for 2- and 3-drive enclosure prices or price of optional finish colors.

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Dataproducts


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date up to eight loads. Each priority level can be assigned one of four priority types.

Access to operational data is provided by a CRT alphanumeric display and keyboard. Each keyboard interacts with four operational and four data entry displays. Options include printers, chart recorders, digital and analog 1/0 modules, remote CRT displays, and remote input keyboards.

Circle 296 on Inquiry Card

**Error Status Indicator Troubleshoots Programmable Controller Systems**

An error status indicator module that instantly troubleshoots any system controlled by its programmable controllers has been introduced by Cincinnati Milacron, Electronic Systems Div, Lebanon, OH 45036. A 3-digit numerical display immediately identifies online failures within the system. The module can be programmed to show 512 cycle interruption alerts and 64 noncycle related alerts.

Each application designer generates a diagnostic manual tailored to particular application and documents the specific online device for each alert. Whenever an un-programmed interruption occurs in the system, the indicator flashes a 3-digit alert and the user references the diagnostic manual to identify the source of trouble. Other lighted indicators show the proper operation of the 12-, 5-, and -18-V power supplies; a fourth indicator flashes if there is ever a failure of the programmable controller contact bus.

Circle 297 on Inquiry Card

**Handheld Input Unit for Industrial Control Retains Long Messages**

A large display buffer that stores up to 960 characters is a key feature of the HT/7 control/display unit. The handheld unit, made by Termiflex Corp, 17 Airport Rd, Nashua, NH 03060, displays two 20-char lines of 0.15" (0.38-cm) high char. Control messages are scrolled in a selectable format as they are accessed from the buffer memory. The 7 x 4.25 x 2.25" (17.8 x 10.8 x 5.7-cm) unit operates on 5 Vdc and internally develops the ±12 Vdc necessary for the Rs-232-C interface. Operation can be either full or half duplex and all 128 ASCII characters and codes can be transmitted or displayed.

Circle 298 on Inquiry Card

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CIRCLE 44 ON INQUIRY CARD
The latest trends in the use of computers for business and professional applications will highlight the 1979 National Computer Conference. According to conference chairman Merlin G. Smith, T. J. Watson Research Center of IBM, the NCC '79 program will present recent developments in computer science and technology and will provide attendees with a better understanding of the total industry, including a greater consciousness of the social implications of the expanding use of computers.

Organized by program chairman Richard E. Merwin, George Washington University, approximately 150 technical program sessions will cover the latest developments in computer applications, science and technology, management, and social implications. Twelve parallel groups of sessions run all four days of the conference at the New York Hilton and Sheraton Centre (formerly the Americana). Included in the technical program are three "mini-conferences"—application areas that will receive in-depth coverage. Augmenting the technical sessions are 15 1-day professional seminars plus 1 all-day workshop.

John R. Opel, president of IBM, will deliver the keynote address Monday June 4 at 10 am. The all-conference reception Monday evening, the third annual Personal Computing Festival, plus the finals of the Amazing Micro-Mouse Maze Contest, a Science Film Theater, Pioneer Day, and a morning TV program will be special attractions of NCC '79.

Technical Program

Technical program sessions feature expanded coverage of management and user requirements, while
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Introducing a ruggedized version of Intel's iSBC* 80/10A Single Board Computer

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Our ruggedized SECS 80/10A likes it hot — or cold. It shrugs off shock, vibration, moisture. And thrives on dust, dirt and grime.
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Functional counterpart of Intel iSBC 80/10A
Exclusively licensed by Intel, our SECS (Severe Environment Computer System) is a functional counterpart of the standard iSBC 80/10A board. Even uses the same development system software.

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Our SECS 80/10A, which uses rugged Intel 883B chips, is mounted on a 9" by 6" shock and vibration resistant, full ATR compatible board. Conduction cooled, it operates from −55°C to +85°C. Add our numerous support modules and you end up with a versatile severe environment microcomputer system at a fraction of the development cost.

Other SESCO products
We also have a complete line of MIL SPEC core and semiconductor memories. New products include D-DAS, a digital data acquisition system for the 1553 bus, and SETS, a compact digital tape recorder with 23 megabit capacity.

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WAY OUT IN FRONT.
providing in-depth treatment of the latest technical developments. Fourteen sessions throughout the conference constitute the mini-conference devoted to Computers, Law, and Public Policy. These sessions will address legal and social issues relevant to data processing including the Federal Communication Commission's Second Computer Inquiry, the rewrite of the Communications Act, a software tax, recommendations for expanded copyright protection, anti-trust enforcement by promoting competition in data processing and communications industries, and the difficulty of obtaining criminal prosecution or civil action against perpetrators of computer crime and fraud.

Rounding out the concentrated focus on the "mini-conferences," the remainder of the program sessions cover recent strides in computer applications, science and technology, management, and social implications. Those sessions under the heading science and technology give major emphasis to data base technology, computer architecture, networking, software reliability, distributed operating systems, and modeling of program behavior. The social implications sessions are devoted to problems of computer security and privacy including data base security, data encryption, security enforcement in programming languages, operating systems security, and information flow and leakage. Receiving particular attention among the computer applications will be computer simulation with sessions planned on emulation laboratories and their use by industry, government, and universities; plus the future of simulation languages, and state of the art of biological simulation.

**Personal Computing Festival**

Technical sessions, applications demonstrations, and commercial displays will be offered in the NCC '79 Personal Computing Festival under the direction of chairman Richard A. Kuzmack, Mathematica, Inc, to answer the questions most frequently heard by those who use or own personal computers: "What do you do with it?" and "Is a personal computing system worth the investment in time, money, and effort?"

Utility will be the watchword throughout this year's program. Session topics include small computer maintenance, personal computer simulation, modeling, personal investment analysis, communications between computers, home and school computer aided education, speech synthesis and recognition, recreational mathematics, and interactive intelligent games including chess. This year, for the first time, prizes will be awarded for the best papers accepted for publication in the NCC '79 Personal Computing Proceedings, and for the best applications demonstrations.

**Personal Development Seminars**

Covering topics designed to stimulate personal, managerial, and technical growth, each full-day Personal Development Seminar will be limited to 100 attendees, with the exception of the hands-on microcomputer workshop that will be held twice and limited to 60 attendees per day. The seminars, held at the New York Sheraton, each require a separate $50 fee that includes course material plus admission to NCC and Personal Computing exhibits. Following are abstracts of selected seminars.

**Special Activities**

An International Visitors Center, located in the Canada room on the second mezzanine level of the New York Coliseum will be staffed from 8:30 am until 6:00 pm throughout the conference. Translation assistance will be available for Spanish, Japanese, French, and German. Also provided will be telephones and limited copier service.

At 7 and 8 am each day a special 1-hour TV program will be aired at most conference hotels. Each "Today at NCC" will spotlight that day's events and
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The speed and performance you get in the NOVA 4/C, for $3500* (complete), is the best deal ever offered a customer needing a basic computer to integrate in his terminals, test instruments or business applications. And it includes a unique self-diagnostic capability that lets the computer trouble-shoot itself to cut service time and cost.

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preview upcoming events. The special program will also be shown throughout the day on TV monitors at the New York Coliseum and New York Hilton.

Pioneer Day will honor a milestone in the history of computing—the development of COBOL. Two special sessions will mark the twentieth anniversary of the creation of COBOL—Common Business Oriented Language. The first will discuss the origins of COBOL, focusing on the programming environment in the late 1950s and emphasizing the rationale behind committee decisions. Topics will include the use of English language and separation of the data description from executable statements, as well as some of the administrative and political factors that were involved in achieving acceptance by users and manufacturers. The second session will provide a retrospective view of COBOL, including establishment of initial standards, comparisons between the original language and COBOL’s present form, and prevailing attitudes of the computing community towards COBOL.

The Science Film Theater will screen a sampling of films and videotapes from universities, industry, private filmmakers, and distributors to show how a computer can be used as an artistic creator, an industrial aid, and an educational instrument.

Exhibits

With regular exhibits occupying the four floors of the New York Coliseum plus the second floor and suites of the New York Hilton Hotel, NCC’79 promises to be the largest and most diverse display of state-of-the-art computer products and services. Exhibit hours are 11 am to 7 pm Monday, June 4; 10 am to 6 pm Tuesday and Wednesday June 5 and 6; and 10 am to 4 pm Thursday, June 7. In addition, the Personal Computing Festival exhibit at the Sheraton Centre Hotel will be open Tuesday and Wednesday, June 5 and 6 from 10 am to 6 pm and Thursday June 7 from 10 am to 4 pm.

Registration

Complete onsite conference registration fee including technical and professional program, conference exhibits, Personal Computing Festival, and conference Proceedings is $75. One-day conference program and exhibits, including the corresponding Personal Computing Festival activities, is $25; four and one days of exhibits are $25 and $10, respectively. Personal Computing Festival fees are $15 for the complete festival including NCC ’79 Personal Computing Proceedings; excluding the Proceedings, registrations are available at $5 for one day and $9 for all four days. Registration begins from 4-8 pm Sunday June 3 at the New York Hilton, and continues beginning 7:45 am on Monday, June 4, at the New York Hilton and Sheraton Centre (formerly the Americana). Shuttle buses will run at regular intervals between the Coliseum, the Hilton, and the Sheraton Centre.

Conference Proceedings may be ordered at $30 for members of any of the 13 AFIPS constituent societies, and $60 for nonmembers; Personal Computing Proceedings are $6. Please send payment with order to AFIPS Press, 210 Summit Ave, Montvale, NJ 07645.

Excerpts from the Technical Program contain sessions of particular interest to Computer Design readers. Information is limited to that available at press time.
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<table>
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<th>Feature</th>
<th>Printer</th>
<th>Integral Data 440</th>
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Monday Afternoon

Session 3 2:30-4 pm Sheraton Centre Imperial A
Software Performance Modeling and Analysis
Chairman: Amrit L. Goel, Syracuse University
Focusing on the models and measures for software system performance, this session will present results of applications to actual software projects.

Session 4 2:30-4 pm Sheraton Centre Imperial B
Impact of Future Technologies on the Computer Industry
Chairman: Robert Colten, Gnostic Concepts
Two-thirds of the products sold by the computer industry today did not exist five years ago. New technologies are the driving forces behind the growth of the computer industry, and this session will provide data processing professionals with an understanding of these forces, together with insights into emerging data processing, mass memory system, distributed computing, and mainframe technologies, and their impacts.

Session 5 2:30-4 pm Sheraton Centre Georgian A
An Assessment of Future Computer System Needs for Large-Scale Computation
Chairman: Peter Lykos, Illinois Institute of Technology
The number of degrees of freedom available to the computer designer is increasing rapidly, but there is a communications gap between users and designers of large scale scientific computers. It is no longer sufficient for users to express their growing needs with the simplistic statement "bigger and faster." Users must organize in order to determine to what extent there are classes of problems and corresponding algorithms generic to several disciplines, together with some measure of their importance, so that the computer vendors can reduce the uncertainty in estimating user needs and reduce the corresponding risk of entering that marketplace.

Session 7 2:30-4 pm Sheraton Centre Royal B
State of Art of Minicomputer Hardware/Software and Distributing Processing
Chairman: Marvin Golland, Peat, Marwick, Mitchell & Co
A panel of hardware/software vendors will present their organization's products, how they perceive the marketplace, and how their organization is attempting to fulfill the need. An overview of minicomputer hardware today and realistic expectations over the next few years will introduce the panel.

Session 9 2:30-4 pm Sheraton Centre Georgian B
Networks and Data: An Interim Report by the CODASYL Systems Committee
Chairman: Bernard K. Plagman, DBS Systems, Inc
The distributed database environment is a logical outgrowth of two major trends in the data processing industry. The CODASYL Systems Committee's analysis of the relationship between database technology and distributed processing serves managers interested in incorporating one or more data bases into a distributed processing environment. Design choices available will be discussed as well as network and database oriented components and their relationships.

Session 10 2:30-4 pm Hilton Sutton
Developing Professional Standards
Chairman: William P. LaPlant, Jr
(Information not available at press time)
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Session 11 2:30-4 pm Sheraton Centre Royal A

Practical Applications of Data Encryption
Chairman: Durrell Hillis, Motorola Government Electronics Div
Two users, from different organizations in the financial world, will relate experiences in implementing data security and discuss their cost tradeoff analysis leading to their implementation. An electronic surveillance expert will review the current threats associated with wiretapping and other electronic surveillance techniques, and two suppliers of standard data encryption equipment will discuss capabilities and limitations of current state of the art encryption systems.

Session 13 4:15-5:45 pm Sheraton Centre Imperial A

Measurement of Software Reliability
Chairman: T. C. Wesselkamper, Virginia Tech
Presenting recent research results in measuring and predicting software reliability, this session will focus on methods that take into account the differences between hardware and software. The work done in verifying the validity of the theory will be carefully considered in the two papers to be followed by a panel discussion.

Session 14 4:15-5:45 pm Sheraton Centre Imperial B

Mass Storage System Technology
Chairman: George A. Michael, Lawrence Livermore Laboratory
(Information not available at press time)

Session 15 4:15-5:45 pm Sheraton Centre Georgian A

Array Processing: An Innovative Approach to Scientific Computing
Chairman: Roy D. Gwin, Floating Point Systems
Discussions of history, philosophy, and implementation of array processors will emphasize problem solving environments. Two environments to be detailed are computer tomography which has allowed the medical profession to have a greater diagnostic capability, and cockpit flight simulators where advances made will allow full simulation of aircraft for pilot training. Also discussed will be the basic mathematical requirements of such environments and their adaptation to array processing through the mathematical solutions of sparse matrices.

Session 17 4:15-5:45 pm Hilton Grand Ballroom West

Database Machines
Chairman: T. H. Bonn, Sperry Research Center
Database machines are commanding wide-spread interest. Users are concerned over increasing database computational loads, and yet they need new functionality. A number of different approaches to database machine architecture have been reported in technical literature and in product announcements. With the rapid advances in VLSI technology, even some of the exotic ideas soon may be cost-effective. These trends need to be put into perspective both from short and long term, and from the user and designer.

Session 20 4:15-5:45 pm Sheraton Centre Georgian B

The ANSI Reference Model for Network Protocols
Chairman: Helen M. Wood, National Bureau of Standards
A provisional reference model, intended to guide subsequent standardization activities, is being developed under the auspices of the American National Standards Institute (ANSI). The model currently consists of seven layers, each of which supports specific data transmission and/or data processing oriented functions, protocols, and interfaces. In this session, the ANSI provisional reference model and its relationship to existing and future, national and international standards will be examined.

Tuesday Morning
Session 25 8:30-10 am Sheraton Centre Imperial A

Designing Distributed Systems
Chairman: Dennis J. Frailey
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To deliver the Future, we designed the 8086 with a totally new architecture, super-efficient for implementing high-level, block-structured languages such as Pascal and PL/M-86.

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We're committed to delivering the industry's highest performance, today and into the future. The 8086's architecture maximizes system throughput today by delivering ten times the processing power of its 8-bit predecessors. Planned expansion promises another order of magnitude increase in performance through the addition of I/O processors, special instruction set extension processors, memory management and distributed intelligence configurations.

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- Bulk Fuel Dispensing Terminals
- Data Input for CRT Terminals
- Computer Access Devices
- Fare Collection Systems
- Identification & Badges
- POS Terminals
- Self-Service Gas Stations

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Topics relating to design issues ranging from tools for analysing potential designs to experience with existing systems will be explored, with emphasis on directly coupled physically distributed multicomputer systems.

Session 29 8:30-10 am Hilton Grand Ballroom West
Distributed Database Systems
Chairman: S. Bing Yao, New York University
(Information not available at press time)

Session 32 8:30-10 am Sheraton Centre Georgian B
An Overview of Network Technology
Chairman: Dixon Doll, IBM Telecommunications
(Information not available at press time)

Session 35 10:15-11:45 am Hilton Mercury
Evolution of the Computer Communications Market in a New Technological Era
Chairman: L. Dan O'Neil, National Telecommunications and Information Administration
Domestic communications issues which are affecting the data processing industry, including the FCC's Second Computer Inquiry, the rewrite of the Communications Act, and the impact of new technology upon the development of this law will be addressed.

Session 37 10:15-11:45 am Sheraton Centre Imperial A
The Interface Between Database Management Systems and Operating Systems
Chairman: Eduardo B. Fernandez, IBM Corp
This session will bring into focus some of the problems faced by designers of database systems to adapt to the environment provided by the operating system.

Session 40 10:15-11:45 am Hilton Grand Ballroom West
Relational Database Systems
Chairman: P. Bruce Berr, Syracuse University
This session will deal with several current issues in relational database systems. Specifically, the authors will address query operations that require means of finding efficient procedures for creating new relations; performance enhancement through query compilation, update problems and solutions to problems; and finally, a new design procedure for relational data base.

Session 41 10:15-11:45 am Sheraton Centre Royal B
Benchmark Selection of Teleprocessing Systems
Chairman: Gerald W. Findley, GCA/ADPS
The advent of plug-compatible mainframes, distributed processing, and falling hardware prices has raised new questions about the technical validity and cost-effectiveness of benchmarking during the selection of teleprocessing systems. The use of teleprocessing benchmarks, however, has been increasing. Leading CPE and benchmarking experts will discuss these developments and issues including the advantages of benchmarking, technical approaches and pitfalls, the cost for both vendors and users, benchmarking goals, remote terminal emulation, and the future of benchmarking.

Session 43 10:15-11:45 am Sheraton Centre Georgian B
Measurement Phases of Computer Selection
Chairman: Sandra A. Mamran, Ohio State University
This session will address the feasibility of executing measurement phases in a comparison study of interactive services available through a computer network. Theoretical, technical, and economic aspects of measuring interactive services will be discussed,
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both in relation to generating test workloads and doing statistically sound data collection and analysis. The emphasis will be on special problems present in the comparison of interactive (as opposed to batch) systems.

Tuesday Afternoon

Session 46 2:30-4 pm Hilton Mercury Computer Communications and the International Marketplace
Chairman: L. Dan O'Neil, National Telecommunications and Information Administration
A status report of international negotiations relating to communications facilities, planning, and ownership will be presented, with attention given to the impact of these disputes and agreements upon the worldwide data processing industry.

Session 48 2:30-4 pm Sheraton Centre Imperial A Computer Systems Analysis and Evaluation
Chairman: Victor L. Wallace, University of Kansas
(Information not available at press time)

Session 49 2:30-4 pm Sheraton Centre Imperial B Dynamic and Reconfigurable Architectures
Chairmen: Svetlana P. Kartashev, University of Nebraska; C. V. Ramamoorthy, University of California; and Steven I. Kartashev, Dynamic Computer Architecture, Inc
Adaptable architectures change their structure via software to adapt to computational peculiarities of a program and are divided into three classes: dynamic, reconfigurable, and microprogrammable. This session will make a survey of dynamic and reconfigurable architectures, specify new architectural adaptations of future computer systems, and outline program analysis techniques aimed at finding these adaptations.

Session 50 2:30-4 pm Sheraton Centre Georgian A Impact of Security and Protection on Computer Architectures
Chairman: Virgil D. Gligor, University of Maryland
Recent advances in protection architectures for both centralized systems and networks will be reviewed. The relevance of these advances to the users' security needs in various environments such as military security, banking, industry, and personal computing will be delimited. Focus will be on the ease (or lack thereof) of integrating protection mechanisms into existing architectures, with some practical limitations of security and of the corresponding protection mechanisms that may restrict the impact of such mechanisms on commercially available systems.

Session 52 2:30-4 pm Hilton Grand Ballroom West Database Evolution
Chairman: Dennis McLeod, University of Southern California
The structure of a computerized data base must adapt with time, as the needs and requirements of an organization change. This evolution must accommodate changes in the user views of a data base as new information must be incorporated. Changes in data base usage and performance requirements must also be handled. This panel will discuss current techniques, approaches, and search directions in addressing the problem of database evolution.

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Session 53 2:30-4 pm Sheraton Centre Royal B
Planning, Acquisition, and Implementation of Minicomputer Based Business Systems
Chairman: Marvin Golland, Peat, Marwick, Mitchell & Co
Data processing consultants and experienced users who are thoroughly familiar with implementing minicomputer business systems will comprise this panel, the focus of which is non-technical. An overview of the minicomputer field, basic definitions, and opportunities will be provided, intending to identify and describe the various steps such as requirements definition, hardware/software selection, contractual arrangements, and implementation of minicomputer systems.

Session 60 4:15-5:45 pm Sheraton Centre Imperial A
Modeling of Program Behavior
Chairman: David Kuck
Concerned with two very different models of program structure, one paper will analyze the way in which references to array elements are contained within iterative loops, and restructure the program to improve performance on virtual memory systems; the second will explain behavior, and describe the relationships between their primitive operators.

Session 61 4:15-5:45 pm Sheraton Centre Imperial B
Dynamic and Reconfigurable Architectures: Problems, Evolution, and Applications
Chairmen: Svetlana P. Kartashev, University of Nebraska, and Steven I. Kartashev, Dynamic Computer Architecture, Inc
Under discussion will be software and hardware problems of designing powerful systems with adaptable architectures (involving dynamic, reconfigurable, and microprogrammable adaptations). Such architectures increase a system's throughput using the same resource, augment the area of effective applications, and simplify the process of creating a system's prototype. Panelists will discuss the problems of supersystems of the 1980s, computation of program(s) by a sequence of computers, new requirements to operating systems, and finding the best system architectures through analysis of an algorithm.

Session 62 4:15-5:45 pm Sheraton Centre Georgian A
Distributed System Control Architecture
Chairman: Daniel Schutzer, Naval Electronics Systems Command
There has been much study in recent years concerning the advantages and disadvantages of distributed processing architectures and networks. This session will describe three representative applications of distributed processing, and some specific analyses performed in support of these applications. It is believed that these analyses will provide general insight as to some major issues associated with the management and control of distributed processing architectures and networks.

Session 64 4:15-5:45 pm Hilton Grand Ballroom West
Database Management Systems Architecture
Chairman: John Berg, National Bureau of Standards
What makes a complete database environment from a user viewpoint? A discussion of components, interfaces, and interactions is necessary to make a database environment useful and acceptable to potential users. Of the many ways which an entire database...
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CIRCLE 62 ON INQUIRY CARD
system might be viewed, which views are better, and what criteria should be used to judge or measure "better"?

**Wednesday Morning**

**Session 72 8:30-11:45 am Sheraton Centre Imperial A**

**Quantitative Measures of the Quality of Programs and Systems**

Chairman: Ned Chapin, InfoSci Inc.

Easy, inexpensive, and controllable maintainability characterizes most high-quality systems and programs. The focus of the first half of this double session will be on quantitative factors affecting maintainability. These include design, management, and statistical factors with some ideas for quantitative measurement and control. The second session will focus on solidly grounded measures useful in program and system design, development, debugging, and maintenance as complexity in design and implementation has long been pointed to as degrading the quality of systems and programs. Recent advances now make it possible to measure the complexity present in quantitative and reliable ways.

**Session 74 8:30-10 am Sheraton Centre Georgian A**

**Fault Tolerant and Maintainable Systems**

Chairman: Jacob A. Abraham, University of Illinois

Focusing on techniques to tolerate hardware or software failures in systems, or to effectively manage them in order to reduce down time, this session will feature papers on a highly reliable, fault-tolerant multiprocessor for aircraft control and on a low-cost, easily maintainable business computer. The question is whether the additional cost of fault-tolerance or maintainability is justified in terms of the improvement in overall throughput.

**Session 78 8:30-10 am Hilton Regent**

**Simulation for Predicting Computer System Performance**

Chairman: Brian W. Unger, University of Calgary, Canada

This session will present recent work in discrete-event and hybrid simulation models for predicting the performance of computer systems.

**Session 80 8:30-10 am Hilton Sutton**

**Advances in Secure Operating Systems Technology in the Department of Defense**

Chairman: Stephen T. Walker, Department of Defense

The day of trusted ADP systems is at hand. After eight years of computer security research, operating systems with sufficient integrity for DOD multilevel secure use will be available during 1979. These systems serve as existing proof to the computer industry that trusted ADP systems can be built, with profound implications on all sensitive information handling applications. This session will describe the design of their secure operating systems.

**Session 84 10:15-11:45 am Sheraton Centre Imperial B**

**The Impact of New A-D LSI Technology on Systems**

Chairman: Rob Walker, Intel Corp.

Examples of a recently available class of semiconductor devices combining linear and complex digital functions on the same chip include microprocessors with A-D converters, telecommunication CODECs and filters, and analog microcomputers. The combination of linear and complex digital circuitry on a single chip constitutes a fundamental advance in semiconductor technology, inferring both lower cost and higher performance. A variety of technologies

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CIRCLE 66 ON INQUIRY CARD
such as bipolar processors, NMOS, and CMOS are being proposed in the search for optimum price/performance.

Session 85 10:15-11:45 am Sheraton Centre Georgian A
Testing and Fault-Tolerance in Digital Systems
Chairman: Stephen Y. H. Su, State University of New York
Since the technology has moved into VLSI, testing has become more important than ever. Intermittent faults are the major cause of failure. The first paper will survey the techniques for modeling, testing and reliability evaluation, and fault-tolerant design of digital systems with intermittent faults. Testing schemes for computer architecture are essentially ad hoc. The second paper will identify the likely errors in implementing an architecture and provide tests for improving the error coverage.

Session 86 10:15-11:45 am Hilton Grand Ballroom East
How to Sell New Technology to Management
Chairman: Herbert B. Safford, GTE Data Services, Inc.
(Information not available at press time)

Wednesday Afternoon
Session 95 2:30-5:45 pm Sheraton Centre Imperial A
Case Studies in Software Development Techniques
Chairman: Julie E. K. Landstein, IBM Corp
In this session the participants will discuss their experiences, tools, and methods used in the various phases of the software development process, the importance of project planning which involves problem and requirement definition, and the necessity of control throughout the life of the project. Next, the technical issues of software implementation and software validation will be addressed; and finally, the inevitable phase of all software projects, that of enhancements and modifications.

Session 96 2:30-4 pm Sheraton Centre Imperial B
High End Microprocessor Architecture
Chairman: Bernard Peuto, Zilog Corp
High end microprocessors are competing with top of the line 16-bit minicomputers and have many of the architectural features of 32-bit minicomputers. The panel will assess the market for this new product and speculate about the impact on computing.

Session 97 2:30-4 pm Sheraton Centre Georgian A
Advanced Industrial Robotics
Chairman: John Albus, National Bureau of Standards
Current and near-future applications of industrial robots to materials handling, tool manipulation, assembly, and inspection will be discussed. Issues of modeling, simulation, high level programming languages, and interfaces to external data bases such as CAD/CAM CL data files will be addressed. Methods by which robots can be programmed to respond to sensory input so as to cope with uncertainties and recover from errors will also be considered.

Session 100 2:30-4 pm Sheraton Centre Royal B
Special Computer Applications
Chairman: Daniel Van Belleghem
(Information not available at press time)

Session 101 2:30-5:45 pm Hilton Regent
Simulation Results
Chairman: John McLeod, Society for Computer Simulation
Panelists in the field of computer simulation will address the question of how simulationists can contribute more effectively to the solution of problems of our time.

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So Much LSI-11 & PDP-11 Analog I/O...
Session 107 4:15-5:45 pm Sheraton Centre Imperial B

**Database Design**

Chairman: Sham Navathe, New York University

Addressing itself to the problems of designing and implementing data bases in business, industry, and government, this session will discuss design decisions, issues, and strategies for each of the following phases: requirements analysis, collection of application needs in information structuring and processing, integration of user/application needs into a logical database design, transformation of logical database design into a DBMS schema, schema implementation and physical design, operational considerations, administration, and control.

Session 108 4:15-5:45 pm Sheraton Centre Georgian A

**Advances in Computer Graphics**

Chairman: Bertram Herzog, University of Colorado

(Information not available at press time)

Thursday Morning

Session 117 8:30-10 am Sheraton Centre Imperial A

**Communications Technologies: Their Impact on Computing**

Chairman: David L. Mills, Communications Satellite Corp

The panelists will discuss a number of technology related issues upon which the development of large scale information networks pivot. Of particular interest is the rapid growth of packet switching technology for the integration of multimedia traffic, including speech, facsimile, and record data. Facilitating the growth of this technology is the emerging use of dynamically shared satellite and radio channels accessible by large user populations. This technology is bound to current and proposed networks by the development of sophisticated protocols uniquely suited for high reliability and efficient utilization of resources, even under adverse operational conditions.

Session 119 8:30-10 am Sheraton Centre Georgian A

**New Directions in Distributive Architectures**

Chairman: Frank Westervelt, Wayne State University

(Information not available at press time)

Session 124 8:30-10 am Sheraton Centre Georgian B

**Network Performance Modeling**

Chairman: Vijay Ahuja, IBM

(Information not available at press time)

Session 130 10:15-11:45 am Sheraton Centre Royal B

**Computation Problems in Pattern Recognition and Image Processing**

Chairman: King Sun Fu, Purdue University

Discussing various computation problems involved in pattern recognition and image processing applications, this session will present special computation algorithms, computer architectures, and software considerations for pattern recognition and image processing.

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118  CIRCLE 68 ON INQUIRY CARD  COMPUTER DESIGN/MAY 1979
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DISTRIBUTORS: Almo Electronics Corp., Philadelphia, PA; Baltimore, MD; Bell Industries, Bellevue, WA; Century Electronics, Albuquerque, NM; Wheatbridge, CO; Salt Lake City, UT; Noram Davis Electronics, South Euclid, OH; Diplomat/Westland, Inc., Sunnyvale, CA; Diplomat/Southland, Inc., Clearwater, FL; Diplomat/Lakeland, Inc., Elk Grove Village, IL; Diplomat/IPC of Mass., Chicopee Falls, MA; Diplomat, Holliston, MA; Diplomat/Northland, Inc., Farmington, MI; Diplomat/Electro-Com Corp., Minneapolis, MN; Diplomat/St. Louis, Inc., St. Louis, MO; Diplomat/IPC Corp., Totowa, NJ; Mt. Laurel, NJ; Diplomat Electronics Corp., Woodbury, NY; Diplomat/Asta-Land, Inc., Salt Lake City, UT; Future Electronics Corp., Montreal, Quebec, Downsview, Ontario, Ottawa, Ontario, Natick, MA; Hughes-Peters, Inc., Cincinnati, OH; Columbus, OH; Intermark Electronics, Sunnyvale, CA; Santa Ana, CA; San Diego, CA; KA Electronics, Dallas, TX; Kent Electronics, Houston, TX; G.S. Marshall, Sunnyvale, CA; Carcoga Park, CA; El Monte, CA; San Diego, CA; Phoenix, AZ; Midway Electronics, Inc., Freepport, NY; Orange, CT; Reptron Electronics, Inc., Livonia, MI; Columbus, OH; Resco/Raleigh, Raleigh, NC; Semiconductor Specialists, Inc., Chicago, IL; Burlington, MA; Farmington, Mi, Minneapolis, MN; Hazelwood, MO; Pittsburgh, PA; Dallas, TX; Milwaukee, WI; Sterling Electronics, Phoenix, AZ; Santa Clara, CA; San Diego, CA; N. Hollywood, CA; Baton Rouge, LA; Waltham, MA; Albuquerque, NM; Dallas, TX; Houston, TX; Tukwila, WA; Summit Distributors, Inc., Buffalo, NY; Summit Elec. of Roch., Inc., Rochester, NY; Technico, Inc., Columbia, MD; Roanoke, VA; Western Microtechnology Sales, Cupertino, CA; Western Region office in Orange, CA at (714) 633-2980; or our Eastern Region office in Melville, NY at (516) 293-5660; or our Midwestern Region office in Des Plaines, IL at (312) 298-7081.

CD-1
The solid name in disk controllers introduces two smart new single boards. For DEC and Data General.

They’re ready for delivery now. Intelligent storage module disk controllers with multi-drive capability, multiple sector transfer, and hardware error correction. They come complete with cables and manuals. For $3580, quantity one.

These controllers are substantial achievements. But then we’ve been making single board disk controllers for DEC, Data General, and Interdata systems for over four years. And more than three thousand trouble-free units are out there working now.

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2470 Embarcadero Way, Palo Alto, California 94303, (415) 856-7400

While you’re at the NCC show, see our newest products at our hospitality suite in the New York Hilton.
Session 132 10:15-11:45 am Sheraton Centre Georgian B
**AUTODIN II—Data Communication System**
Chairman: Sydney Gordon
(Information not available at press time)

Session 133 10:15-11:45 am Hilton Sutton
**Microcomputers in Technical Professional Development**
Chairman: Raymond G. Fox, Learning Technology Institute
Continuing personnel development in the field of science and engineering is critical in maintaining technical competence in an era of rapid technological change and obsolescence. This session will look at solutions to these problems which employ the use of microcomputers in the technical professional development process. Panelists will describe methods of microcomputer uses, applications, and results achieved, and will identify the future potential of this technology.

**Thursday Afternoon**
Session 136 2:30-4 pm Sheraton Centre Imperial B
**Associative Processors—Why Are They Needed? What Can We Expect in the Future?**
Chairman: Tadao Ichikawa, Hiroshima University
Considering the rapidly developing LSI technology of recent years, there is now a need to work toward the economical implementation of application oriented, high performance associative processors to meet social requirements. Session participants with theoretical and physical backgrounds of implementing the systems will discuss practical applicability of associative processors to database management and image processing problems in terms of cost-effectiveness.

Session 137 2:30-4 pm Sheraton Centre Georgian A
**High Level Language and Direct Execution Machines**
Chairman: Edward Feustel
(Information not available at press time)

Session 142 2:30-4 pm Sheraton Centre Royal A
**Computerized Control Systems for Automated Production Facilities**
Chairman: Leonard B. Gardner, u.s. Army Armament Research and Development Command
Different types of control systems for automated production facilities will be discussed, beginning with relay type logic and analog controls, and progressing to computers and digital controls. Included will be programmable controllers, microprocessors, and minicomputers. Procedures for system design and equipment specification will be presented. The production line is treated as a continuous process. A control strategy for optimization will be discussed, along with methodology used to develop functional guidelines and process control standards, and requirements for interfacing hardware and software.

Session 148 4:15-5:45 pm Sheraton Centre Royal B
**Error Correcting Codes: Applications to Memory Systems**
Chairman: Raymond S. Lim, NASA—Ames Research Ctr
(Information not available at press time)

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- For program loading, diagnostics, PROM emulation
- Over 1 megabits, 2.4K Baud rate, 4.8K optional
- Includes all read/write and motion electronics
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*1K Qty. Avail. N. Amer. only.*
### Professional Development Seminars

**Tuesday 8:30 A.M.-4:30 P.M.**

<table>
<thead>
<tr>
<th>Time</th>
<th>Seminar</th>
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| 2:30-4:00  | Regulation or Antitrust — Competition in the Computer/Communication Marketplace  
Edwin B. Spievack |
| 4:15-5:45  | Insurance Industry Automation  
Peter B. Walker  
Trust & Securities Industry Automation  
Junius W. Peake |
|           | Software Performance Modeling & Analysis  
Amrit L. Goel  
Measurement of Software Reliability  
T.C. Weseikamper |
|           | Impact of Future Technologies on the Computer/Industry  
Roy D. Ryan  
Mass Storage System Technology  
George A. Michael |
|           | An Assessment of Future Computer System Needs for Large-Scale Computation  
Peter Lykos  
Array Processing: An Innovative Approach to Scientific Computing  
Roy D. Ryan |
|           | Unions in Data Processing  
Richard Herzholtz  
Business & Entrepreneurial Opportunities in Computers  
Stanley Klein |

**Wednesday 8:30 A.M.-4:30 P.M.**

<table>
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<tr>
<th>Time</th>
<th>Seminar</th>
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| 2:30-4:00  | Database Machines  
T.H. Bojin  
Database Machines  
T.H. Bojin |
| 4:15-5:45  | State of Art of Minicomputer Hardware / Software & Distributive Processing  
Marvin Golland  
Computer Page Printing  
Jenice Cartun |
|           | User Assistance in On-Line Systems  
Richard L. Wexelblat  
Computers in Biological & Medical Simulation  
Thomas G. Coleman |
|           | Networks & Data: An Interim Report by the CODASYL Systems Committee  
Bernard K. Plugman  
The ANSI Reference Model for Network Protocols  
Helen M. Wolf |
|           | Developing Professional Standards  
William P. LaPlant, Jr.  
Technical Aspects of Privacy Protection in Transnational Data Systems  
Rein Turn |
|           | Practical Applications of Data Encryption  
Durrell Hils  
Determining the Value of Computer Applications  
Edward O. Joslin |

**Thursday 8:30 A.M.-4:30 P.M.**

<table>
<thead>
<tr>
<th>Time</th>
<th>Seminar</th>
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| 2:30-4:00  | Human Engineering in Teleprocessing Systems  
Thomas R. Bailey, TRB Systems  
Personal Computing Pioneers  
Sol Libes  
The Coming Small Computer Earthquake  
Burchenal Green |
| 4:15-5:45  | Recent Developments in Minicomputer Technology  
John H. Carson, Carson Associates  
Managing Structured Methodologies  
Edward Yourdon, Yourdon, Inc.  
Computer Systems Performance  
Jeffrey P. Buzen, BGS Systems, Inc. |

Separate registration required for each seminar.
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<th>10:15-11:45</th>
<th>2:30-4:00</th>
<th>Tuesday P.M.</th>
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<td></td>
<td>Commercial Banking Automation William J. Deane</td>
<td>EFT &amp; Consumer Banking Automation Robert V. Sabieck</td>
<td>International Banking Automation Derek G. Hall</td>
<td>The Automation of Check Processing Wayne B. Lewin</td>
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<tr>
<td></td>
<td>Emulation Laboratories &amp; Experience Ingrid A. Eldridge</td>
<td>Simulation Development Tools</td>
<td>Simulation of Industrial Processes J. Talaverge</td>
<td>Simulation Languages Tuncer Oren</td>
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**Personal Computing Festival**

8:30
- Personal Robotics
  - Ralph Holls

10:30-12:30
- Small Business Systems: What Can I Get For $?
  - Dan Ring & Bob Redmond

2:30-4:30
- Meeting of Computer Retailers
  - Asan

(Continued on p 126)
PerSci delivers the Dual-Headed Diskette Drive that works and the Double Density IBM Compatible Controller to back it up.

While everyone else was waiting and promising—PerSci did it! Designed the industry's first fully reliable, field proven, dual-head design—now available in a high technology dual diskette drive, the PerSci Model 299. The 299 has a total of four heads handling two double-sided diskettes—providing up to 3.2 Mbytes of data in a drive the size of a standard floppy. And because the Model 299 has voice coil positioning, this dual diskette drive can seek data four to six times faster than possible on two independent stepper motor drives. All offered by PerSci at a highly competitive OEM price.

To save time and money in systems design, PerSci backs up the 299 with the first available double density, dual-head flexible disk controller—the Model 1170—for all applications requiring IBM 2D, IBM 3740 or S-100 bus compatibility. The PerSci 1170 is Z-80 based, the smallest, most intelligent floppy disk controller on the market.

The PerSci 299 and 1170 controller are designed with the same advanced technology that has made PerSci number three in diskette product shipments (and moving up). Don't wait around for more talk and more promises. Call PerSci for full information.

PerSci, Inc., 12210 Nebraska Avenue, West Los Angeles, California 90025. (213) 820-3764.

CIRCLE 72 ON INQUIRY CARD
Introducing the Sperry
Designed exclusively for three

The Sperry Univac V77-800 Miniframe is the newest and most powerful mini we've ever built—a high performance, multi-use, general-purpose minicomputer system designed for both commercial and scientific data processing. It has a memory range from 128K bytes to 2 megabytes (with error correcting memory) and a 150 nanosecond CPU with integrated cache of 1024 bytes. Plus 12K bytes of user programmable writable control store.

There's an optional new high speed 64-bit floating point processor that works in conjunction with a new globally optimized ANS '77 FORTRAN.

No wonder our three most important customers think so highly of it.

OUR OEM CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

The Miniframe is customer microprogrammable. So an OEM can implement his own firmware packages. And with the many software packages we offer, the OEM can add all the bells and whistles he wants.

The Miniframe comes with our largest instruction set ever. So OEM's with their own software have much more flexibility in design.

The Miniframe speaks PASCAL, the powerful new language for scientific, commercial, and system programming that most competitive systems still can't speak. And of course, it also speaks COBOL, FORTRAN and RPGII.

More good news is that the Miniframe is compatible with the rest of the V77 product line.

OUR SYSTEM HOUSE CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Naturally, system houses want all the features OEM's do. And more.

So we gave them more.

More operating systems, for example. Choose from VORTEX or our new SUMMIT—an interactive, multi-terminal system with transaction processing and data base management. It gives you easy editing, screen formatting, and documentation aids. Plus speedy, comprehensive program development.

System houses also think PASCAL is important. Because it's more efficient, easier to maintain, expand, and modify.

The Miniframe brings systems builders a new query language called QL-77. It features inquire and report facilities. And interfaces...
Univac V77-800 Miniframe.
of our very best customers.

directly to TOTAL*, the data base management system. So preprocessing and intermediate handling are a thing of the past. Finally, TOTAL also gives you complete data base access and file access security.

OUR END USER CUSTOMERS KNOW WE DESIGNED IT JUST FOR THEM.

Take all the features we designed in for OEM's and system houses and say ditto for the end user.

But we didn't stop there. We also pressed a few special hot buttons just for end users.

Consider QL-77, for example. End users will love our new query language because it reduces the amount of application programming. By storing query language procedures right in the data base file. Where they can be easily and quickly recalled and executed at any time.

Once again, SUMMIT, our new operating system, helps the end user handle transaction processing. Without any additional, expensive software. It's also the right answer for a multi-tasking, "fully-implemented" distributed processing system.

Finally, the Miniframe supports DCA and conventional protocols. So you can talk to both SPERRY UNIVAC and IBM hosts.

YOU'LL KNOW WE DESIGNED THE MINIFRAME JUST FOR YOU.

No matter what your application, no matter what your need, the Miniframe may just be the answer.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, ext. 536.


In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

We're Sperry Univac.
And our new Miniframe is going to solve some very big problems.

*TOTAL is a registered trademark of Cincom, Inc.
TEKTRONIX thinks your logic analyzer should be as versatile as you are

So ours let you sample synchronously and asynchronously.

As a digital designer you must be versatile enough to do the entire design job. Logic and timing. Software and hardware analysis. Activity on and off the bus.

And so you need a logic analyzer that lets you synchronously verify logic and trace program flow on the bus; then asynchronously verify timing sequences and examine chip to chip transactions off the bus. A logic analyzer, in short, as versatile as you are.

Tektronix Logic Analyzers are versatile. In the synchronous mode, examine software flow using the clock of the system under test—up to 20 ns sampling rate. Switch to asynchronous and sample with the Logic Analyzer's own clock—up to 10 ns sampling rate. Pulse anomalies and timing problems are out in the open, where you can see them. With one logic analyzer.

Synchronous and asynchronous sampling: it helps make our Logic Analyzers versatile. So you can do today's job and tomorrow's. So you can change applications without changing your logic analyzer.

Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix, Ltd., P.O. Box 36, St. Peter Port Guernsey, Channel Islands.

For technical data, circle 74 on Inquiry Card. For a demonstration, circle 75 on Inquiry Card.

For immediate action, dial our toll free automatic answering service: 1-800-547-1512
### Preliminary Conference at a Glance (Continued)

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<td>8:30-10:00</td>
<td><strong>Thursday A.M.</strong></td>
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<td>Information Privacy: Public Policy &amp; Recordkeepers' Responsibilities Francis M. Gregory, Jr.</td>
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<td>Implementation Factors in Hospital Information Systems David J. Mischelewich</td>
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<td>Communications Technologies: Their Impact on Computing David L. Mills</td>
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<td>Performance Modeling &amp; Evaluation of Database Management Systems Larry Kirschberg</td>
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<td>New Directions in Distributive Architectures Frank Westervelt</td>
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<td>The Expanding World of Service George O. Harmon</td>
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<td>Computer Chess — The Next Decade Dennis W. Cooper</td>
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<td>What Can Pattern Recognition &amp; Image Processing Do for the Society King Sun Fu</td>
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<td>Computing in Developing Countries K. Varvian</td>
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<td>Network Performance Modeling Vijay Ahuja</td>
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<td>Computer Fraud Donn B. Parker</td>
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<td>10:15-11:45</td>
<td><strong>Thursday A.M.</strong></td>
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<td>The International Privacy Debate: Laws, Licenses &amp; Limitations Alexander D. Roth</td>
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<td>Data Dictionary Systems Henry C. Leikovits</td>
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<td>2:30-4:00</td>
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<td>Data Processing &amp; the Provision of Legal Services in the Private Law Office Helley Fromholz</td>
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<td>Computer-Based Consultation and Ambulatory Patient Care: How Should It Be Implemented? John Lackmann</td>
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<td>Associative Processors — Why Are They Needed? What Can We Expect in the Future? Tadashi Ichikawa</td>
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<td>4:15-5:45</td>
<td><strong>Thursday P.M.</strong></td>
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<td>High-Level Language &amp; Direct Execution Machines Edward Feustler</td>
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<td>Time Management for the Professional Hudson E. Henry</td>
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<td>Finding Value in Used Computers William S. Grinker &amp; Marvin Lurie</td>
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<td>User Microprogramming of Minicomputers Joseph M. Austin</td>
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<td>Error-Correcting Codes: Application to Memory Systems Raymond S. Lin</td>
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<td>Applications of Computers in Criminal Justice Systems Arthur B. Carroll</td>
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<td>The Military Message Experiment Duane Adams</td>
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<td>Current Topics on Information Retrieval Carolyn J. Crouch</td>
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<td>Management of Computer Centers by Contract William P. LaPlante, Jr.</td>
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<td>Personal Career Planning for the Information Systems Professional Peter McGregor</td>
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<td>Personalized Control Systems for Automated Production Facilities Leonard B. Gardner</td>
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<tr>
<td>8:30</td>
<td><strong>Personal Computing Festival</strong></td>
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<td>10:30-12:30</td>
<td>Simulation, Modeling &amp; Games Stephen Smith</td>
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<td>Computer Retailing Alan Haid &amp; Craig Tenney</td>
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<td></td>
<td>Computer Fraud Donn B. Parker</td>
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<tr>
<td>2:30-4:00</td>
<td>Personal Computer Maintenance William Godbout &amp; William Schenker</td>
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<td>Personal Computing in Other Hobbies Harold Buchanan</td>
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<tr>
<td></td>
<td>Recreational Mathematics Abraham Waksman</td>
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Plus other Personal Computing Topics.
Computer Design asked most NCC '79 exhibitors to supply advance information on truly new products to be introduced to attendees at the Conference. To the best of our knowledge, the following 72 are such products. However, because of the early copy deadline for this issue in respect to the dates of the Conference, some companies will display products on which they could not supply preview information.

MICROPROCESSOR CONTROLLED READER/SPOOLER

Reel motors of model 661C9 reader/spooler combination are microprocessor controlled, allowing each reel to operate independently and wind or read punched tape in both directions asynchronously. Low maintenance read head handles 5-, 6-, or 8-level tapes, center feed, and advanced feed without adjustments. Unit has single nonfocused, derated, 25,000-h light source, with fiber optics light distribution system. Decitek, 129 Flanders Rd, Westboro, MA 01581.

See at Booth 435
Circle 415 on Inquiry Card

WINCHESTER DISC DRIVES

FD 130 and FD 65 drives have an unformatted capacity of 132.4M and 66.3M bytes/drive, respectively. Specs for both include an access time of 6 ms track to track and rotational speed of 3900 r/min. Also available is the M2202 front loading cartridge drive with 83.3M-byte unformatted capacity. All 3 units have a transfer rate of 819k bytes/s. Fujitsu America Inc, 2945 Oakmead Village Ct, Santa Clara, CA 95051.

See at Madison Suite
Circle 416 on Inquiry Card

DESKTOP COMPUTERS

The 3000 series with 13" (33-cm) CRTs and the 9000 series with 19" (48-cm) screen, offering a variety of configurations, feature a 1-piece molded cabinet with built-in keyboard and 8-color display. Both support high level languages. Options include built-in floppy or hard disc, graphics capabilities, lightpens, and asynchronous/synchronous communications. Intelligent Systems Corp, 5965 Peachtree Corners E, Norcross, GA 30071.

See at Booth 4806

Circle 417 on Inquiry Card

SEMICONDUCTOR RAM MODULE

Pin compatible with DEC PDP-11/70 computers, PINCOMM 70S installs in the MK-11 memory chassis, which holds up to 16 modules and DEC memory cards without modification. Memory card capacity is 256k bytes. Also featured are sockets for RAM ICs and 2 onboard spare RAMs. Trendata Corp, 3400 W Segerstrom, Santa Ana, CA 92704.

See at Booth 1312
Circle 418 on Inquiry Card

LARGE DISC CONTROLLER FOR LSI-11

Three models of the microprocessor based SC01 controller family are compatible with DEC software and allow users to add as much as 0.5G bytes of hard disc storage capacity to LSI-11 systems. SC01/A emulates DEC RP11/RP02/RP03 subsystems; SC01/B emulates RH11/RM02/RP04/RP05/RP06 subsystems; and SC01/C emulates RK61/RK06/RK07 subsystems. Incorporated are an automatic self-test capability plus extensive subsystem diagnostics in onboard firmware, and special operating functions. Two PC boards plug into any pair of std Q Bus quad slots. High speed bipolar technology and std SMD interfacing are included. Any 2 industry compatible drives may be integrated into a single subsystem, all operating at serial data rates up to 100Mhz. Fully buffered disc I/O circuitry permits operation at radial cable distances of 50 ft (15 m) and Daisy chain cable distances of 100 ft (30 m). Micro-programmed error control functions allow std ECC/CRC operations to be performed at full data rates under all interface methods. Emulex Corp, 17785 O Sky Park Cir, Irvine, CA 92714.

See at Booth 344
Circle 419 on Inquiry Card

INTERACTIVE EDITING TERMINAL

A 46-line (2 pages) up/down scrolling machine with editing capabilities including margin wrap on character insert and delete, the model 12 will accommodate 32 user programmed functions in a 2000-char nonvolatile function buffer. Variable I/O parameters are also programmable and nonvolatile. By displaying 5 or more field modifiers (pro-

tect, dim, blink, inverse video, and under) in any combination, the unit provides a full 80 characters of data per line. Primarily an editing terminal, it doubles as an online interactive terminal and will be available in an emulator version. Telearay Div, Research Inc, PO Box 24084, Minneapolis, MN 55424.

See at Booth 2006
Circle 420 on Inquiry Card

NOTE

Booths numbered 1000, 2000, 3000, and 4000 are located in the NY Coliseum on floors corresponding to the first digit; booths 300 to 999 plus suites are in the NY Hilton Hotel; and booths from 1 to 150 are in the Sheraton Centre Hotel at the Personal Computing Festival.
Defend your PDP-11. Don’t feed it to the dumb beasts. Get a UMC-Z80 and let it handle those serial-line protocols. Liberate your PDP-11 for the tasks it’s best at.

What’s a UMC-Z80? It’s a complete microprocessor system that plugs into your UNIBUS. The Processor Board handles two full-duplex serial lines. They’ll run asynchronous, or synchronous byte or bit oriented protocols. At speeds up to 880 Kbaud. Or over 56 Kbaud for greedy ones like HDLC or ADCCP.

Population explosion? No problem. Add a Serial Line Expansion Board. Or two. Or more. Each one gives you 8 independent microprocessor systems. Each system has dedicated memory plus independent interrupts. And serves two full-duplex serial lines. That’s 16 hungry lines per board.

For software, the choice is yours. You can cook up your own with the UMC-Z80 Software Development System. Or pick up some carry-outs like HDLC, ADCCP, IBM BiSync protocols (like 2770, 2780 or 3780), and even X.25 level IV. Available now or available soon.

Now if all that doesn’t keep the beasts at bay, nothing will.

Want to know more? Contact ACC today.

ASSOCIATED COMPUTER CONSULTANTS
228 EAST COTA STREET, SANTA BARBARA, CALIFORNIA 93101.
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STANDALONE IMAGE PROCESSOR

A self-contained microprocessor combined with full resolution display makes picture analysis possible within the EyeCom II as a standalone system. Image processing software has been expanded to provide turnkey image processing systems. The system contains an alphanumeric terminal, high speed picture digitizer, high resolution display, joystick cursor, and microprocessor. Picture digitizer offers 640 x 480 resolution with true 8-bit digitization in <5s with up to SX video contrast enhancement prior to digitization. Display has 640 x 480 resolution with 8-bit gray scale and white graphics overlay. Hardware scroll and zoom up to SX and hardware window transfers to processor are provided. Full typewriter keyboard allows for 4-level ASCII codes, 256 in all. Screen can display the 128-char ASCII set on 24 lines of 80 chars. Spatial Data Systems, PO Box 249, Goleta, CA 93017.

See at Booth 4036
Circle 421 on Inquiry Card

VIDEO DISPLAY TERMINALS

D304 is equipped with a sophisticated electronic package, designed for use in serially transmitting information to and receiving information from an interconnected data source at speeds up to 19,200 baud. Screen displays 60 x 24, 64 x 16, 40 x 12, or 32 x 16 lines of characters selectable from the keyboard. Memory stores 80 x 24—1 page, 64 x 16 or 40 x 12—2 pages, or 32 x 16—4 pages. Keyboard has standard layout plus 12-key numeric pad, and 14 function keys. Parity, number of character/line, and number of lines are switch selectable at keyboard. Used as interactive terminal in full duplex, each character including control characters is transmitted without affecting cursor location. In polled block mode terminal is assigned address that must be included in sequence to receive or transmit data. Informer, 8332 Osage Ave, Los Angeles, CA 90045.

See at Booth 2005
Circle 422 on Inquiry Card

VIDEO TERMINALS

Minimizing operator fatigue through typewriter oriented keyboard and clear display of outgoing and incoming data, InterTube displays 1920 char arranged in 24 lines with 80 char each. A 25th line (half intensity) displays terminal operating modes. Control section of the terminal is based on the Z80 microprocessor. Display module and driver circuitry consists of 12” (30.48-cm), high resolution, wide bandwidth CRT mounted in steel frame. Power supply is a solid state switching design. Transmission mode is half- or full-duplex, keyboard selectable. Keyboard has a std teletypewriter compatible layout, 18-key numeric pad, keyboard lock/unlock under program control, and special function keys. Self-diagnostic firmware testing routine provides a continuous display of data on the screen. Intertec Data Systems Corp, 2300 Broad River Rd, Columbia, SC 29210.

See at Booth 1237
Circle 423 on Inquiry Card

DISPLAY TERMINALS

Regent® series 20, 40, 60, and 300 range from simple display terminal to a clustered intelligent terminal. For use as a basic computer conversational device, model 20 has EIA and current loop interfaces, with u/lc on 12” (30.48-cm) CRT and control code display in a 24-line x 80-char format. Full incremental cursor movement and addressability and a std unidirectional auxiliary port are provided. Conversational model 40 also has extensive visual highlighting features, status line, numeric pad, function keys, and bidirectional auxiliary port, plus insert and delete line feature. Model 60, a smart, buffered display terminal, adds buffered transmission with editing capability to features of the 20 and 40. It can send a character, line, or page at a time, and offers bidirectional, serial, auxiliary interfaces with independent speed setting. Low cost clustered intelligent terminal model 300 includes 52k bytes of RAM, 2 diskette drives, up to 4 smart display terminals, printer interface, and asynchronous and synchronous (software selectable) communications interfaces. Applied Digital Data Systems, Inc, 100 Marcus Blvd, Hauppauge, NY 11787.

See at Booth 1322
Circle 424 on Inquiry Card
Many engineers are resisting fiber optics. We know why.

Most good engineers can't resist a good idea. (And fiber optics is a compelling idea, after all: optical communication cables carry more information in less space with less weight, and eliminate electrical interference, just for starters.)

Some very good engineers see fiber optics in a different light. They point out that a good idea must also be a proven product. Their job is not to get trapped into testing new products, it's to take advantage of proven ones.

Quite right.
Which is why it may come as a surprise that there are more than 2,000,000,000 feet of our fiber optics in use today. Galileo has been manufacturing fiber optic products for nearly 20 years.

We offer the most complete line of optical communication cable in a range of attenuations, mechanical strengths and cost to meet your application requirements. In fact, you can probably find whatever Galileo Galite® fiber optic cable configurations you need from stock (not just our highly versatile Galite 3000).

You see, we make it all ourselves, from raw materials to finished cables. Which is why we can tell you and show you more about fiber optics than anybody else today. Including how to take advantage of it as a proven technology. (You'll find a complete line of connectors and electronic components available from Galileo, which makes application and installation very simple indeed.)

You can write to Galileo for a detailed information package that will give you a good idea of what fiber optics can do for you today. Or you can call Galileo's applications engineers at (617) 347-9191 for specific personal help on how... and where... fiber optics could fit into what you're doing today.

You'll find we offer more than fiber optics. We also offer know-how.
Socket Connectors—IDS Series
For pluggable termination of cable to header mounted on PCB. Single piece body for easy assembly, fewer parts to inventory. Cover latch and optional strain relief for operational reliability.

Transition Connectors—IDT Series
Used to attach cable permanently to PCB. Has rugged single piece design for fast assembly and high reliability. Cover latch swivels for easy cable insertion.

Cable Plugs—IDP Series
Offer fast, easy plugging of cable to PCB directly or into DIP sockets. Tapered pins assure quick, easy insertion into DIP sockets. One unit design speeds handling and assembly. Cover latch swivels for easy cable insertion.

Headers—IDH Series
Mounts permanently to PCB and accepts socket connectors. In straight or right angle mounting—for solder or wrap/pin termination. Handy ejector/latch available—when closed it locks socket into place and serves as ejector when open.

Laminated Flat Cable
RN offers both cable and connectors—your assurance of "single source" reliability. Available in white or color coded 100 foot rolls in 10 thru 50 conductor sizes.
has it now...a truly economical

- flat cable system

for high speed assembly
using tooling you already have

This RN IDC System delivers what engineers want ...

- Advanced automated manufacturing facilities enable RN to cut costs — pass the savings on to you
- Fewer pieces for faster assembly, reduced inventory
- Can be assembled with IDC tooling already in place
- Each connector made more rugged, more resistant to shock, vibration and cable strain
- Assured reliability and compatibility of cable and connectors — RN supplies both

Economical, easy to use — once properly adjusted, all RN IDC connectors can be assembled with a simple base plate change

Hand Held crimp tool for assembling IDP series Cable Plugs and IDT series Transition Connectors

Bench mounted crimp tool for assembly of all RN IDC connectors.

WRITE TODAY for new Robinson-Nugent Insulation Displacement Connector catalog with complete specifications and dimensions on the entire IDC product line.
Designers of military and high reliability systems can depend on Intel for the latest in LSI technology. We deliver more advanced mil-spec microcomputers and semiconductor memory than anyone.

Here's our strategy. The fiercely competitive pressures of the industrial marketplace have driven us to push for higher and higher performance with greater and greater reliability. Last year alone Intel spent $41 million on research and development. That investment strengthened our decade of leadership in microelectronics. And it enables us to keep our commitment of bringing the world's most advanced LSI microcircuits to the military.

JAN-approved 8080A: leading edge of military LSI

Intel invented the microcomputer, and it's no surprise our 8080A was the first microprocessor to qualify for JAN approval and first for QPL Part I listing (M38510/42001 BQB). Now military designers can also take advantage of Intel's M8085A, military version of the most powerful 8-bit microprocessor ever. Or design with our recently militarized single-chip microcomputer, the M8048.

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To expand your design capability even further, Intel is currently working with government agencies and military equipment manufacturers to upgrade more devices to military specifications. We stand ready to support your programs with additional JAN-approved components as slash sheets are issued.

For more information on Intel's complete family of military devices contact your local Intel distributor or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.
BUSINESS MINICOMPUTER

Up to 3 flexible diskettes with 615k bytes of storage and 32k bytes of MOS memory characterize the self-contained desk model configuration. Its full 24-line x 80-char video display terminal has a std typewriter and 10-key pad; the 150-char/s matrix printer features vertical forms control, tractor feed, and compressed print. The upward expandable Centurion Series 100 also contains multitasking and communications capabilities. Warrex Computer Corp, 1780 Jay E11 Dr, Richardson, TX 75081.

See at Booth 4111
Circle 425 on Inquiry Card

RANDOM VECTOR PROCESSOR

Accepting random vectors and symbols from a host mainframe, processor reduces the information to raster form, and outputs it to a variety of popular electrostatic and matrix plotters, including Versatec, Gould, Houston Instruments, and Trilog models. System design incorporates LSI technology, with MOS memory for vector and symbol storage. Microprocessor controlled ROM storage provides system logic, with high speed arithmetic implemented in TTL. Data input options include mag tape, serial asynchronous RS-232, IBM BISync, and 8-bit parallel; system also accepts data in line printer format. Random vector and symbol output from mainframe is produced by machine independent FORTRAN drive program integrated into user's graphics application software. KMW Systems Corp, 8307 Hwy 71 W, Austin, TX 78735.

See at Booth 436
Circle 427 on Inquiry Card

HEAVY STOCK, BOTTOM FEED PRINTER

Designed for printing on tough surfaces such as steel, plastic, and cardboard, IDS-7440 features a 7 x 7 dot matrix and bar code 39, an alphanumeric code used in government applications. It can also be used with multiple and variable sized forms. Two stainless steel rollers maintain registration and permit steel forms to be pulled up for alignment. An optical sensor determines presence of end cuts or indentions and perfectly positions the next label. Dataroyal, Inc, 235 Main Dunstable Rd, Nashua, NH 03061.

See at Booth 1316
Circle 428 on Inquiry Card

400-Hz SOLID STATE POWER SYSTEM

Power interface for computers meets most 400-Hz central processor requirements, including IBM 3032 and 3033 specs. Four configurations with increasing capability for upgrading are a frequency converter, UPS with storage battery, redundant UPS, and combination 400-Hz/utility frequency UPS. Cyberex, Inc, 7171 Industrial Park Blvd, Mentor, OH 44060.

See at Booth 4112
Circle 429 on Inquiry Card

INTERACTIVE ANSI COBOL COMPILER

Implementing Nucleus; Table Handling; Sequential, Relative, and Indexed I/O; Inter-Program Communication, and Library modules, enhanced version of CIS COBOL Compiler meets ANSI level 1 requirements for a COBOL compiler. Version 4 of the software package is designed to support interactive applications, is able to exploit features of a microcomputer, is oriented toward rapid program development, and is supported by intelligent utility programs. Designed to run on 8080 and Z80 based systems, compiler is supplied with full internal and interfacing documentation. Also shown will be Version 3. Supplied on both standard and mini-floppy diskettes, this version will run on any microcomputer with 32K or more bytes RAM that supports the CP/M operating system. Micro Focus Ltd, 58 Acacia Rd, St John's Wood, London NW8 6AG, England.

See at Booth 323
Circle 430 on Inquiry Card
NCC PRODUCT REVIEW

SMALL BUSINESS COMPUTER

Z80 based Microsystem features dual 5" (12.7-cm) minifloppy drives with 320-byte capacity and internal 56k user RAM and 8k reserved RAM and ROM. Desktop sized cabinet also includes two RS-232-C asynchronous and synchronous serial I/O ports, 4-MHz clock, and 12" (30.5-cm) CRT. 94-key keyboard has number pad and 16 special function keys. Software includes business accounting package plus FORTRAN, COBOL, and E-BASIC. Billings Computer Corp, 2000 E Billings Ave, Provo, UT 84601.

See at Booth 3223
Circle 431 on Inquiry Card

50-MHz MINI-SCOPE

Weighing <15 lb (6.75 kg), PS950A measures 4.2 x 8.5 x 15.4" deep (10.67 x 21.6 x 29.1 cm). Bright trace is attained by 7-kV acceleration potential on a mesh CRT with metallized screen. Internal graticule and small spot size give sharply defined trace. Mesh tube affords superior deflection sensitivities, eliminating dynamic range problems in vertical and horizontal amps. Trigger range is well above the 50-MHz vertical bandwidth. 7-ns risetime, bright trace, and trigger assure stable presentation of narrow low repetition rate pulses. Front panel controls are grouped by function with CRT separating vertical and display section from horizontal controls. Scope has 8 x 10-div display [0.25" (0.653 cm) /div]. Horizontal and vertical modules can be detached from scope by removing screws and unplug­ping PC connector. Power requirement is <35 W. Vu-Data Corp, 7170 Convoy Ct, San Diego, CA 92111.

See at Booth 2001
Circle 432 on Inquiry Card

POWER INPUT ISOLATION/REGULATOR

MicroPower™ series computer power interfaces isolate, regulate, and filter power output between std wall outlets and terminals, mini, or microcomputers. Interface reduces downtime due to power line fluctuation, disturbances, and transients. Brownout protection against all forms of low line voltage up to -20% of nominal line voltage is provided. Series will also protect against high line voltages to +20% of nominal. Additional features incorporated include Soft/Start™ capability which eases turn on/off stress in the connected equipment and common mode noise reduction. Power input to unit is by cord and plug connected to a suitable source of building power. Portable unit outputs 1k VA, single-phase with 120 Vac, 60 Hz. Computer Power Systems Corp, 3398 E 70th St, Long Beach, CA 90805.

See at Booth 304
Circle 433 on Inquiry Card

0.5" MAGNETIC TAPE HEADS

Streamer heads incorporate LTC® for long life, high reliability operation, and are capable of storing data from 1 IBM model 3370 disc drive (570M bytes) on 1500 ft (457 m) of 0.5" (1.27-cm) magnetic tape at a data transfer rate of 1.66M bytes/s. Low cost model DQ-91 is a 9-channel, 0.250" (0.635-cm) streamer head that is capable of recording at 10,000 fc/in (2937/cm). When used with GCR it provides a capacity of 32M bytes on 3M's DC-300A cartridge. Also shown will be the FFD-DST double-sided floppy disc head that reliably reads and writes on both sides of the disc maintaining precise alignment and compliance through use of an optical/mechanical alignment technique. Compatible with ANSI stds for flexible disc operation, the head extends data capacity of a single disc to 1M byte. Nortronics Co, Inc, 8101-10th Ave N, Minneapolis, MN 55427.

See at Booth 1110
Circle 434 on Inquiry Card
The fastest, most reliable alternative to fixed-head disk.

IMPERIAL TECHNOLOGY'S
MAXRAM
STORAGE SYSTEM

- RANDOM ACCESS
- HIGH SPEED
- ZERO LATENCY
- SOLID STATE RELIABILITY

Here's the best alternative to fixed-head disk for cost-conscious users of PDP-11 & Nova computers.

- High speed random access.
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- Pluggable modules of 0.524 megabytes each; expansion capability to 8.388 megabytes.
- 1.5 microseconds access time.
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- No data loss in event of power failure.
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The MaxiRAM System is also available for use with other computer types.

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Order your FREE copy today! Find out how the MaxiRAM Storage System offers unmatched economy and performance for your memory requirements.

Imperial Technology, Inc.
831 S. Douglas Street
El Segundo, California 90245
(213) 679-9501
NONIMPACT PRINTER

Printing on electrosensitive paper 8.5" (21.6-cm) wide at 225 char/s, model 912 draws each letter and number from a 9 x 12 matrix using a precision print-head designed for service. The unit has minimum moving parts and reduced components count and is tools for easy assembly in high volume production. Character set is std 96 ASCII set with upper and true lower case. Controls and indicators include power on light, power on/off switch, online/off-line/no print switch, self test/paper advance switch, and out of paper sensor with audio alarm. Programmable controls include paginate and continuous print mode. Unit has 256 bytes of buffer memory std (2048 bytes are optional). Computer Printers International, Inc, 280 Polaris St, Mountain View, CA 94043.

See at Booth 60
Circle 435 on Inquiry Card

BUSINESS COMPUTER WITH BUBBLE MEMORY

General purpose microcomputers include a BASIC language operating system, bubble memory mass storage, alphanumeric plasma display, and integral printer in a compact portable unit weighing <20 lb (9 kg). System 128 has 128k-bytes magnetic bubble memory for mass storage, expandable in increments of 128k. System 100 offers 90k bytes (expandable to 400k) of mass storage in a minifloppy disc housed inside the case. Built-in memory is the same as in the 128, and includes 48k bytes of dynamic RAM and 1k bytes of static RAM, expandable to >2M bytes, plus 8k bytes of ROM, expandable to 32k. External disc drives can be interfaced to provide additional storage. Serial, parallel I/O, and S-100 capabilities allow interfacing with a range of peripheral units. Findex Inc, 1625 W Olympic Blvd, Suite 707, Los Angeles, CA 90015.

See at Booth 39
Circle 436 on Inquiry Card

STREAMING TAPE DRIVE

Low profile 0.5" (1.3-cm) tape moving drive supplies disc backup for small business systems. Operating in a high speed streaming mode without frequent stops and starts, the drive takes data on-the-fly in large blocks (up to a full disc) at 100 in (254 cm)/s, automatically inserting industry std interrecord gaps. In conventional stop/start mode, the drive performs at 12.5 in (31.8 cm)/s. The IBM and ANSI compatible device reads and writes data in 1600 bits/in (630/cm), phase encoded format. Up to 30M bytes (nom) of data can be accommodated on a 10.5" (26.7-cm) reel; total capacity of many disc files can be dumped into the tape drive in a single continuous operation. The drive includes formatting electronics. It occupies 8.75" (22.2 cm) of vertical rack space, or can be housed with a disc file and CPU in a desk cabinet. Up to 8 drives can be daisy chained on the company's industry std formatted interface. General specs include low speed variation that is ±1% of nom and instantaneous speed variation that is ±3% of long term. Cipher Data Products, 5630 Kearny Mesa Rd, San Diego, CA 92111.

See at Booth 3311
Circle 437 on Inquiry Card

TRACTOR FEED IMPACT PRINTER

Low cost printer has software selectable character sizes, full u/lc 96-char ASCII set, and 80- and 132-col formats. Model 440 Paper Tiger™ combines microprocessor, controls, indicators, and electronics on a single PC board. Std features include adjustable form width, forms control with 8 std form lengths, choice of 6 or 8 lines/in (2.3 or 3.1/ cm) vertical spacing, software selectable character density, automatic multil ine buffering, and both RS-232-C serial and Centronics compatible parallel interfaces. Multiple transmission rates from 110 to 1200 baud are switch selectable. A stepper motor paper feed insures fast reliable paper movement, and an automatic reinking mechanism extends ribbon life. Integral Data Systems, Inc, 14 Tech Circle, Natick, MA 01760.

See at Booth 4440
Circle 438 on Inquiry Card
DEC PDP-11 TAPE USERS
NO WAITING . . .

For the first embedded single board
Magnetic Tape System Controller

Datum's new PDP-11 software compatible single board design, Model 1520 Embedded NRZI Tape Controller offers you more for less. And we're delivering them right now.

More versatility, occupies a single HEX SPC slot or comes with its own chassis, 16 bit microprocessor controlled, word and or byte memory transfers with odd or even starting addresses and byte counts, TM-11 or IBM data compatibility is available. The 1520 interfaces to the Datum D450 tape drive or any industry standard tape drive (up to four can be attached). Dual Density is achieved simply by adding a second board to accommodate the Phase Encoded function. Additionally, Datum offers you Phase Encoded ID data burst detection.

And we offer you less, less initial cost*, less preventative maintenance. And you use less space thanks to Datum's advanced embedded controller design.

If you're a PDP-11 tape user and need delivery now, owe it to yourself to learn more about Datum's more for less tape program. For early delivery contact your local Datum representative today.

PDP-11 SOFTWARE COMPATIBLE

*Single board NRZI design, $3,000 Qty-1

PDP 103

Systems (tape drive and controller) pricing begins at $6,900 Qty-1

And, there's no waiting to see Datum at the NCC, Booth 1220
Because even engineers

When was the last time you had the "perfect" hardware design only to learn it now needs three serial I/O ports?

Our new Micro Design Series minimizes these problems and lets you quickly respond to changing product definition and market conditions. Here's how:


First, decide what functions your system needs. Match the Z80-based, MDX functional modules to your design. Plug those modules into an MDX card cage. Then start writing your software.

Need to modify your system? Simply exchange, add or delete MDX modules at any time. The small 4.5" x 6.5" board size makes system packaging easier. And both 2.5 and 4.0 MHz versions are available.

You get this versatility because all MDX modules are STD-Z80 BUS compatible. This second-sourced, motherboard
interconnect system lowers system cost two ways: you buy only what you need, and you reduce hardware development time.

A Wide Choice of Z80-Based Systems.
Need a small but powerful single-board computer? In addition to the broad family of MDX modules, Mostek's MD Series includes a separate family of stand-alone boards designated MD. The MD single-board computers are also Mostek Z80-based and the same small size as the MDX modules.

More Coming in '79.
For even greater design flexibility, the MD Series will expand to include a hardware single-step module, 2-channel programmable serial I/O module, 32-bit programmable parallel I/O module, floppy-disk controller module, plus more MD single-board computers.

Start designing your MDX system with the MDX-PROTO kit. This powerful evaluation/prototyping kit is available now for only $1095.

Call or write us today for more information. Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; phone 214/242-0444. In Europe, contact Mostek Brussels; phone (32)02/660.25.68.
Computer-aided design, Management information systems, Medical/tomography, Command and control, Earth resource/land mapping, Reconnaissance photography, Training/simulation systems, Process control, Micrographics.

Aydin Controls, since 1967 the pioneer in computer graphics and imaging, can help you more efficiently, effectively, and creatively structure your man/machine interface with the 5216 Color Graphic/Image System.

Versatile, modular hardware – You can configure the 5216 for requirements from simple alphanumeric or graphic displays to sophisticated image-processing and analysis applications.

Flexible, easy-to-use software – The 5216 is available with the most comprehensive software package in the industry, including a highly efficient operating system, two- and three-dimensional packages, image analysis program, and interactive list processing software.

Extensive peripherals and accessories – Keyboards, joysticks, track balls, graphic tablets, graphic printers, cartridge and floppy disk drives, and much more to come.

See us at NCC, Booths 3056 and 3058.

We make it easy to add Aydin IMAGE-ination

Our application engineers can help you add Aydin IMAGE-ination. Call or write for a demonstration or for more information.

414 Commerce Drive Ft. Washington, PA 19034 (215) 542-7800 TWX: 510-661-0518
8M-BYTE SEMICONDUCTOR MEMORY SYSTEM

Packaged in a 15.75" (40.0-cm) chassis, basic Bulk Semi system unit is 2-board DR-128S system consisting of controller (BSC) and array (BSA) boards. BSC supports up to 16 BSA boards and has capability of configuring available memory in 2- or 4-byte words. BSA is 128k x 43 (36 data and 7 ECC bits), or 512k bytes. Cycle and access times for a 36-bit word are 500 and 350 ns, respectively. In addition to normal control functions and error correcting, controller provides error logging. Controllers allow systems to be used as disc emulation systems for DEC, Data General, and Interdata minicomputers, and can be used for large capacity main memory expansions. Dataram Corp, Princeton-Hightstown Rd, Cranbury, NJ 08512.

See at Booth 1506
Circle 439 on Inquiry Card

COMPUTER GRAPHICS SOFTWARE SYSTEM

Contouring and business graphics options are available for DISSPLA® system. Extended device interfacing feature permits users to set up intimate relationship between system software and graphics hardware wherein software queries hardware to see what tasks it can perform, then shifts workload between the two accordingly. The device independent, integrated software system of FORTRAN subroutines are called up by the user's program to produce publication quality 2- and 3-dimensional graphics. Output is via plotters, CRTs, computer output microfilm units, flatbed plotters, or art generators. Integrated Software Systems Corp, 4186 Sorrento Valley Blvd, San Diego, CA 92121.

See at Booth 3102
Circle 440 on Inquiry Card

NOTE

Booths numbered 1000, 2000, 3000, and 4000 are located in the NY Coliseum on floors corresponding to the first digit; booths 300 to 999 plus suites are in the NY Hilton Hotel; and booths from 1 to 150 are in the Sheraton Centre Hotel at the Personal Computing Festival.

16-CHANNEL LOGIC STATE ANALYZER

PM3500 can operate with external clock from the system to acquire data in a synchronous manner or with its internal clock. A synchronous mode increases clock rate, allowing detailed study of timing relationships. A 20-position internal clock allows data to be sampled at speeds from 20 ms to 10 ns. A high speed circuit in each input channel monitors between-clock pulses, capturing high speed glitches. The unit will trigger on glitches, or can be triggered externally. State displays are presented in binary, octal, or hex; a mapping facility shows entire contents of captured block of 505 serial bits on up to 16 channels, displaying each stored parallel word as single dot. Philips Test and Measuring Instruments, Inc, 400 Crossways Pk Dr, Woodbury, NJ 11797.

See at Booth 3042
Circle 441 on Inquiry Card

MICROPROGRAMMED VIDEO DISPLAY TERMINAL

Designed for multidrop communications networks that incorporate Burroughs computers and displays, model 2830 offers enhanced emulation of TD331 and TD333 terminals. Std features include concatenation with auto bypass, TTY mode, integral numeric keypad, 7 x 9 char matrix, printer output, and data communications buffer operation. Also shown are 4050H and 4050U display terminals which emulate Honeywell and Univac terminals and computers. Delta Data Systems Corp, Woodhaven Industrial Pk, Cornwells Heights, PA 19020.

See at Booth 4107
Circle 442 on Inquiry Card

MINIFLOPPY DOUBLE-HEAD DISC DRIVES

Model 52 with 70 tracks has a track to track access time of 5 ms. Pulley-band design offers high temp stability, on-track repeatability, and accurate positioning. Single- and double-density (unformatted) units feature 218.8 x 10³ and 437.5 x 10³ bytes/disc, respectively. Rotational speed is 300 r/min ±1.5%; avg latency is 100 ms. Micro Peripherals Inc, 21201 Oxnard St, Woodland Hills, CA 91367.

See at Booth 370
Circle 443 on Inquiry Card
80-COLUMN THERMAL PRINTER

Thermal RO printer model PPS-80E uses 5 x 7 dot matrix characters to provide 10 char/in (3.9/cm) at 6 lines/in (2.3/cm) on friction feed or perforated 8.5" (21.6-cm) paper. Signaling rates offered are serial mode up to 9600 baud (with option), and parallel mode up to 960 char/s; average throughput is 30 char/s. Unit interfaces with parallel format (TTL), or serial RS-232-C or 20-mA loop using a mass termination connection. Special functions include odd, even, or no parity, pulse to generate audible signal if desired, vector generator graphics, special status chars, and APL, Hebrew, Arabic, or custom character sets. Answer-back is an option. The unit measures 12.2 x 5.2 x 9" deep (30.9 x 13.2 x 22.9 cm), weighs 5.375 lb (2.419 kg), and operates at from 0 to 50°C. Telpar, Inc, 4132 Billy Mitchell Rd, Addison, TX 75001.

See at Booth 110
Circle 444 on Inquiry Card

STORAGE MODULE AND DATA CARTRIDGE CONTROLLERS

DC-233 storage module disc controller for DEC PDP-11 computers contains a miniature distributed processing architecture for handling up to 8 nonremovable and removable media multiplexer disc drives ranging from 50M to 300M bytes. It is software compatible to DEC operating systems having RM03 or RP05/06 support. The embedded processor houses the controller and 1 to 8 drive adapters together in the CPU or expansion chassis. Radial configuration isolates each drive; the drive adapter controls its drive's commands and status. The controller portion handles communications to CPU and implements data transfers and error correction coding and decoding. TC-170 0.25" (0.635-cm) data cartridge tape controller for Data General Nova computers and emulators controls up to 8 drives, emulates 0.5" (1.27-cm) mag tape systems, and is IRIS and RDOS compatible. The embedded unit uses 6400-bit/in (2520/cm) serial MFM, 1600-bit/in (630/cm) PE serial, or 1600-bit/in (630/cm) PE parallel formats. Weispecorp, Western Peripherals Div, 1100 Claudina Pl, Anaheim, CA 92805.

See at Booth 3046
Circle 445 on Inquiry Card

CRT MONITOR FOR CRITICAL DISPLAY APPLICATIONS

All solid state except for CRT; model DC 949 has a 15" (38-cm) diag, 100-in² (650-cm²) display area, 110° deflection angle, and implosion protection. P4 phosphor is std; others are available. All electronic circuitry is mounted on one PC board, TTL input only, with separate horizontal and vertical drives. All inputs are 2.5 V to 5.0 V pk-pk. Logic 1 initiates black display. Power inputs required are 55 Vdc at 700 mA max, and 5 Vdc at 50 mA max. Video response is within 3 dB from 10 Hz to 25 MHz. Resolution is 900 lines center, 800 lines corners, with geometric distortion of 2% max. Scan frequencies are 34.2 kHz horizontal, 50/60 Hz vertical. The unit is 10.5" (26.6 cm) high, 12.38" (31.4 cm) deep, and 13.12" (33.3 cm) wide. Weight is 14.5 lb (6.5 kg). Audiotronics, Video Display Div, 530 Fifth Ave, New Brighton, MN 55112.

See at Booth 3107
Circle 446 on Inquiry Card

300-LINE/MIN DEMAND DOCUMENT PRINTER

Innovator 250 is designed for multiform applications where printed form is required immediately after printing. Immediate access to printed form is offered in addition to clear legibility of the fully formed char. Printer uses a tear bar located 0.250" (0.647 cm) from center of printed line so that paper is not wasted. Tractor feed mechanism is capable of printing 80 char/line on variable width and length multipart forms. Intelligent controller board mounted and accessible within cabinet provides for field selectable configuration via switch strapping. Centronics, Dataproducts, 20/60-mA current loop, and RS-232 compatibility are offered as std. Interfaces provide hardware and software transparency with existing host computer or terminal operating systems. Innovative Electronics Inc, 15200 Northwest 60 Ave, Miami Lakes, FL 33014.

See at Booth 1236
Circle 447 on Inquiry Card
A Beautiful Way To Interface

SOROC's first and foremost concern, in designing outstanding remote video displays, has resulted in the development of the IQ 140. This unit reflects exquisite appearance and performance capabilities unequaled by others on the market.

With the IQ 140, the operator is given full command over data being processed by means of a wide variety of edit, video, and mode control keys, etc.

The detachable keyboard, with its complement of 117 keys, is logically arranged into 6 sections plus main keyboard to aid in the overall convenience of operation. For example, a group of 8 keys for cursor control / 14 keys accommodate numeric entry / 16 special function keys allow access to 32 pre-programmed commands / 8 keys make up the extensive edit and clear section / 8 keys for video setup and mode control / and 8 keys control message and print.

Two Polling options available: 1) Polling compatible with Lear Siegler's ADM-2. 2) Polling discipline compatible with Burroughs.

The IQ 120 is the result of an industry-wide demand for a capable remote video display terminal which provides a multiple of features at a low affordable price. The IQ 120 terminal is a simple self-contained operator / computer unit.

The IQ 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IQ 120 terminal incorporates a 12-inch CRT formatted to display 24 lines with 80 characters per line.

CIRCLE 84 ON INQUIRY CARD
COMMUNICATIONS MULTIPLEXER

80-COL BIDIRECTIONAL MATRIX PRINTER

The parallel interface bidirectional dot matrix printer with modifiable char set operates with any system having at least 1 parallel TTL input and 2 parallel TTL output ports, and a power supply capable of 3 A at ±16 Vdc and approx 0.5 A at 8 Vdc. Throughput speed is 84 lines/min. The printer draws its power from the mainframe. It is completely software driven, including char generation. The optional software driver comes on 2708 P/Rom. Since the driver is written in Z80 code, implementation of the printer can involve no programming in Z80 systems. A source listing is included in order to rewrite it or alter the char set. S-100 compatible products to be shown include a 12k P/ROM-1k RAM board with P/ROM programmer; fast scan TV digitizer that converts output from std TV cameras into 8-bit gray scale digital information and transfers it to RAM; and Bitstreamer II board featuring 3 serial I/O ports, interrupt request capability, realtime clock, and 2 parallel ports to interface terminals, printers, readers, and punches. Vector Graphic, Inc, 31364 Via Colinas, Westlake Village, CA 91361.

See at Booth 340
Circle 448 on Inquiry Card

COMMUNICATIONS MULTIPLEXER FOR PDP-11

Microprocessor derived design of DV/16™ enables mixing synchronous and asynchronous lines in any combination of 4 or 8 while maintaining modem control and compatibility with DV11 related software. Line configuration can be changed as often as needed. Word transfer instead of byte DMA is used to gain speed of 76,800 char/s or to let user operate in one-half bandwidth required by DV11 data transfers. Four boards contain 16 channels; expansion to 32 channels takes up 7 standard SPC slots. Also shown, model 10047 Emuloader™, fixed console emulator (ODT), and bootstrap loader combined on single board for several PDP-11 computers. Able Computer Technology, Inc, 1751 Langley Ave, Irvine, CA 92714.

See at Booth 411
Circle 449 on Inquiry Card

LINE BUFFERED SERIAL IMPACT PRINTER

Featuring an integrated cutting device for handling special forms such as airline tickets, statements, ledgers, checks, and labels, M78 service printer uses a continuous roll paper supply and automatically cuts off the completed form immediately after printing. The 80-col bidirectional unit prints at 200 char/s. A 7 x 7 matrix font is std, with 9 x 9, 9 x 7, and 12 x 9 available as options. Optional fonts allow the printer to produce negative print, OCR A and B, bar code, ulc with desenders, elongated chars, and double width chars. The unit can accommodate 64-, 96-, and 128-char sets. The buffer can store a complete line of text. For forms compatibility or best readability, operator can switch from 6 to 8 lines/in (2.3 to 3.1/cm) spacing or switch character spacing from 0 to 12, 14, or 16.5/in (0 to 4.7, 5.5, or 6.4/cm). Tally Corp, 8301 S 180th St, Kent, WA 98031.

See at Booth 2021
Circle 450 on Inquiry Card

VOICE INPUT DATA ENTRY TERMINAL

Model 1800 allows users to send to or retrieve data from a computer by talking to it over any telephone line. System need not be trained to user's voice before calling. It can accommodate 8 users simultaneously and validates data entry by voice response and error correction procedures. The terminal operates by changing the received word into digitized form understandable to a computer. Standard vocabularies include approx 21 words, including 10 digits, and command words specific to the application. Voice response subsystem verifies input by repeating back to user at any point before initiating any action. Response vocabulary consists of approx 128 words. Interface is standard RS-232, asynchronous full-duplex up to 4800 baud or 20-mA serial current loop. Terminal can also emulate standard computer interfaces such as IBM 3271. Dialog Systems, Inc, 32 Locust St, Belmont, MA 02178.

See at Booth 381
Circle 451 on Inquiry Card
Behind the panel of the 5½-inch high Ampex 8MS5 Minicomputer, there's an 800 nanosecond CPU and as much as 64K words (128K bytes) of memory. All on a single board.

Leaving four big slots for your own cards. 15 x 15 inch boards, with whatever you need to realize the goals of your system. Insert controllers for disk, tape, printers or terminals. As long as the controller is compatible with NOVA*, it'll be compatible with the Ampex 8MS.

That's because Ampex designed this minicomputer to take full advantage of the environment that has grown up around NOVA computers. But this mini has some extras you never expected to see in a mini.

Like front access to all components. And a programmer's console with octal pad input, octal readout and LED indicators. Plus a single bus structure.

Charley Penrose has some suggestions about achieving big system capability in the little 8MS cabinet. Call him at 213/640-0150. Or write to him at Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245.

*NOVA is a trademark of Data General Corporation.

AMPEX MAKES IT EASY.

See the complete line of Ampex Products for Data Processing in Booth 2208 at NCC.

CIRCLE 85 ON INQUIRY CARD
600-CHAR/s MATRIX PRINTER
Proprietary magnetic, stored energy print head prints 600 char/s with no duty cycle or page density restrictions. Open binary interface gives a 128-dot/in (50/cm) vertical and horizontal resolution for graphics and plotting. Available as the BNY-M mechanism only or model BNY, printer stores up to 4 print fonts, including a 2-pass high quality font, under program control. 7 x 8 matrix yields 230 lines/min with full 132-char lines; 15 x 16 matrix prints at 150 char/s. 96-char u/lo ASCII fonts have true underlining and elongated characters. Expanded characters for labeling are 2, 4, and 8 times normal character size. Other features include an OCR font, 990-char buffer, and multiple copies of 1- to 6-part forms. Florida Data Corp, 3308 New Haven Ave, West Melbourne, FL 32901.
See at Booth 507
Circle 452 on Inquiry Card

COLOR GRAPHICS DISPLAY SYSTEM
Featuring max resolution up to 1024 scan lines of 1280 elements and 128 bits/element, RM-9400 display generator has vector writing speeds of >16k vectors/s, based on an avg vector length of 50 pixels. Microprocessor based unit offers choice of 5 resolutions. An expanded internal display user memory and upgraded internal display processor, addition of 1 to 8 special purpose 16-bit bipolar microprocessors, and reduction of refresh memory access time increase performance. Each processing element performs specific functions, permitting overlap of functions to increase vector throughput. System decodes and processes a high level binary formatted instruction set. Instructions, transmitted and received via 16-bit parallel interface can be executed immediately or stored as subpictures in user memory for deferred execution. Ramtek Corp, 585 N Mary Ave, Sunnyvale, CA 94086.
See at Booth 4328
Circle 453 on Inquiry Card

INTERACTIVE TERMINAL WORKSTATION
Standalone system provides dual buffering, allowing terminal and printer to be independently addressed, and permitting data entry and retrieval while printout is in progress. Built-in diagnostic features allow operators to detect both hardware and software related problems without interrupting normal operations. Microprocessor based terminal consists of CRT, keyboard, and logic module. Using IBM Bisync 3275/3271 emulation, it communicates at speeds to 9600 bits/s over dedicated lines and 4800 bits/s over dial-up lines. Extended editing, highlighting, horizontal and vertical cursor controls, and other convenience features are offered. Freestanding CRT tilts and swivels and keyboard may be positioned to suit operator. Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166.
See at Booth 2200
Circle 454 on Inquiry Card

FIBER OPTIC ASYNCHRONOUS DIGITAL DATA LINKS
Data links perform serial transmission in simplex or duplex mode over transmission paths of up to 1.5 km. Serial data transfer is from 0 to 6M bits/s with bit error rates better than 10^-7. With TTL compatible I/O, std units are supplied with connectorized fiber optic cable. Connector is BNC or 25-pin miniature. Within the optical interface, the transmitter features an LED as optical source, operating wavelength of 820 nm nom, and output of -15 dBm typ; the receiver has a PIN diode as optical detector and a typical sensitivity of -40 dBm (at 300k bits/s) and -30 dBm (at 6M bits/s). Operating temp range is 0 to 40 °C. For standard models, measuring 8.9 x 20.3 x 25.4 cm, power requirements are 115/220 Vac, 50/60 Hz. Two types of fiber optic cable offered are graded index single (D1G-062) and twin (D2G-062) core for high data rate computer and industrial control applications. Fiber attenuation is to 12 dB/km max, and impact strength is 1.5 N*m with 8.5-mm radius hammer, 10 cycles without fiber breakage. Core diameter measures 0.0625 mm and fiber diameter is 0.125 mm. Canstar Communications, 1240 Ellesmere Rd, Scarborough, Ontario M1P 2X4, Canada.
See at Booth 4116
Circle 455 on Inquiry Card
The Operating System for Business

Educational Data System's New Supermini

The Unbeatable Combination

A new approach to system building . . .

IRIS is used throughout the world for multi-terminal, real-time applications in business and database management. Combined with the POINT 4, IRIS supports up to 32 terminals.


The POINT 4 is the perfect complement to IRIS: 400 nanosecond instruction execution; 128K bytes of directly addressable RAM; means for extending the instruction set; intercomputer communication; virtual control panel and built-in diagnostics — all on the CPU board.

The POINT 4 is compatible with a wide range of commercially available peripheral devices, including our Mighty Mux DMA channel multiplexer and Micro-N microprogrammable processor.

Get IRIS, the application software and POINT 4 from the people who created all three and support them best. Or, since they come unbundled, buy only the components you need.

For the whole story on the Unbeatable Combination, send in the coupon or call TODAY . . .

(714) 556-4242

Educational Data Systems
1682 Langley Avenue
Irvine, California 92714

CIRCLE 86 ON INQUIRY CARD

Name ____________________________ Title ______________

Phone __________________________

Company _________________________

Street __________________________

City ____________________________ State ______ Zip ______________
NCC PRODUCT REVIEW

TAPE PUNCH STATION
Self-contained station punches paper or Mylar tape with either 5- and 6-channel ISO or 6-channel TTS data according to the die block. Model 3601, a tabletop station, has 75- and 50-char/s versions. Microprocessor based TTL compatible interface accepts parallel data; RS-232 V.24 serial input is optional. Interface includes parity check, motor check, motor speed regulation, and automatic motor start/stop. Tape is perforated by punching needles, which are electromagnetically selected according to the input data. Data and feed signals are synchronized by a photoelectric timing generator. Two built-in test programs check function of the company's model 36 punch mechanism. GNT Automatic, Inc, 1560 Trapelo Rd, Waltham, MA 02154.
See at Booth 2004
Circle 456 on Inquiry Card

BAND TYPE LINE PRINTERS
ChainTrain® series 3001 printers feature high speeds with low noise. Models 3151, 3301, 3601, and 3901 have speeds of 150, 300, 600, and 900 lines/min, respectively, and offer a 10-char/in (3.9/cm) format as a std feature; 3151 and 3301 offer 15 char/in (5.9/cm) as a customer option. Larger in size to provide better cooling and equipped with a power supply of increased capacity to accommodate the faster line speeds the printers can be utilized to advantage in either a main computer room or a remote location. A 1200-line/min machine with high reliability construction the ChainTrain model 1200 is a horizontal moving font printer utilizing a carrier with interchangeable 8-char links riding on a monorail track. Unit accepts 6-part forms ranging in size from 3.5 to 19.5" (8.9 to 49.5 cm) in width. Data Printer Corp, 99 Middle­ sex St, Malden, MA 02148.
See at Booth 2017
Circle 457 on Inquiry Card

NOTE
Booths numbered 1000, 2000, 3000, and 4000 are located in the NY Coliseum on floors corre­ sponding to the first digit; booths 300 to 999 plus suites are in the NY Hilton Hotel; and booths from 1 to 150 are in the Sheraton Centre Hotel at the Personal Computing Festival.

MONOCHROME DISPLAY MONITOR
Black-on-white, high density, high reso­ lution raster display monitor is human engineered for daily use without eye­ strain. The HRD-15 displays 6200 7 x 9 dot matrix characters on an 8 x 10.5" (20- x 26.6-cm) screen. High speed model H scans 60k horizontal lines/s, generating 1024 visible lines. Dot reso­ lution is rated at 0.01" (0.254 mm). Monitor has a rise/fall rate less than 2 ns. Fast scanning and rise/fall rates improve clarity and density, eliminate "smear" at dot edges and create a dot with more edge contrast. Flicker-free performance is insured by the 60k non­ interlaced scans/s. Horizontal and verti­ cal sync are separate TTL signals; video is ECL. CPT Corp, 1001 S Second St, Hopkins, MN 55343.
See at Booth 362
Circle 458 on Inquiry Card

WIREWRAPPING TOOL
"Just WrapTM" is a wiring process and series of tools that produce wirewrapped connections without prior stripping or slitting of the wire insulation. Designed to wrap on 0.025" (0.63-mm) sq posts, each tool carries a 50-ft (15-m) spool of 30 AWG (0.25-mm) wire. It wires continuously through any number of pins (daisy chain); OK Machine and Tool Corp, 3455 Conner St, Bronx, NY 10475.
See at Booth 108
Circle 459 on Inquiry Card

INTELLIGENT HIGH SPEED READER/PUNCH
Dual ported serial RS-232 SRP-750 system is designed to reduce line and operating costs by functioning as a high speed peripheral or standalone device. Features include 4K RAM buf­ fer, auto diagnostics, full- or half-du­plex, high speed edit or duplication capabilities, with selectable operating speeds up to 3000 baud, send or re­ ceive. Mechanism uses Mylar or paper tape interchangeably without needing registration readjustment. Data Special­ ties, Inc, 3455 Commercial, Northbrook, IL 60062.
See at Booth 1528
Circle 460 on Inquiry Card

154
COMPUTER DESIGN/MAY 1979
Everything you need to know about flat cable/connector systems.

To save space. To increase circuit flexibility and reliability. To lower total installed cost. To profit from the state-of-the-art in mass termination.

T&B/Ansley offers you the industry’s broadest line of flat cable/connector systems. That’s because we’ve been flat cable specialists for decades, and we were pioneers in the development of cost effective mass-termination techniques for volume production and ease of assembly.

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That includes connectors, headers, mounting hardware. It includes round and flat conductor flat cable, as well as jacketed and shielded jacketed cable. It includes our MICRO-PITCH line, which is ideal for mass termination in high density, controlled impedance applications. And our FLEXSTRIP® Jumpers, the most flexible, reliable components available for interconnecting one circuit board to another.

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CIRCLE 87 ON INQUIRY CARD

Send for your free copy today!
How Litronix' opens a new world

Now designers have a communications peripheral perfectly matched in size and cost to the world of microcomputers. Litronix invented the Intelligent Display* to give microcomputers a new way of "talking" to users in words, numbers or even sentences. And not surprisingly, these displays are already beginning to create a new class of microcomputer-based products.

The Intelligent Display is an alphanumeric LED readout that incorporates ASCII decoder, multiplexer, memory and LED driver in a built-in CMOS IC. It interfaces simply and directly to any microprocessor bus, much like a RAM. Power is from a single +5V supply, and operating current is low enough for any battery powered device.

**Litronix puts intelligent communications in the palm of your hand** or anywhere panel space is limited. Three versions of the Intelligent Display are already available to fit a wide variety of applications. The smallest lets you fit 20 characters side by side in a space of only 3.5 inches.

Litronix' Intelligent Displays are already being used in the portable terminal, the low cost microcomputer and electronic translator above. They're also ideally suited for applications like control panel readouts. Handheld computer

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*Intelligent Display is a trademark of Litronix, Inc.*

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<table>
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<th>Part Number</th>
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<th>Character Height</th>
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<td>4</td>
<td>17</td>
</tr>
</tbody>
</table>
Intelligent Display™
of microcomputer applications.

Intelligent Displays™ of microcomputer applications. "Smart" games and appliances. Educational products, and more.

Use Intelligent Displays in any product that calls for alphanumerics. They'll reduce component count and cut costs dramatically. Since everything is encapsulated in a single package, design and production costs are minimal. And because no display interface PC board is needed, component costs are typically reduced by 25%. Typical OEM volume pricing will range from $2 to $5 per digit, depending on display type. For easy breadboarding with Intelligent Displays, ask about our inexpensive, prewired Evaluation Kit. To get data sheets and a copy of our applications note on Intelligent Displays, or for a demonstration, phone or write Litronix, Inc., 19000 Homestead Road, Cupertino, CA 95014. Telephone (408) 257-7910.
MAKE YOUR NOVA
PERFORM LIKE A FERRARI

...with the first Lifetime-Guaranteed Disc Controller

At Quentin Research, we don’t call our revolutionary new Model N6010 Nova Compatible Disc Controller “The Cadillac of the Industry”: it comes without “bells and whistles”… the luxury accessories you probably won’t need and don’t want to pay for.

Instead, Quentin’s crack team of Advanced Technology Specialists has created a low cost, ultra-high speed controller that brings out the “Ferrari” in your basic Nova; permitting the computer to handle information at maximum disc speed: 9.67 MHz or 1.2 MBytes per second.

But in designing the N6010 as the fastest controller on the market, we haven’t left off the important features: overlap seek, compatibility with RDOS, IRIS and BLIS/COBOL operating systems, and the capability to interface up to four CDC or other storage module disc drives with any Nova or Eclipse computer.

Unprecedented reliability? How else could we sell it with the industry’s only “no strings” Lifetime Guarantee? And at a price that gives you a lot more byte for the buck.

Call us for more information, or make a date to visit our modern new Research Center and take the N6010 for a spin. Find out how we’re putting tomorrow’s technology into today’s computers.
MULTISTATION BAR CODE READ SYSTEM

Allowing up to 10 remote scanning wands to operate from a single reader, Satellite Wand System model 9171 has LED status indicators for interaction with host computer; 9170 is a nonstatus indicator version that can be interconnected in a daisy chain or star configuration (9171 can be daisy chain connected only). Up to 500 ft (152 m) of cable can be used in the system. System operates on party line basis; when wand is removed from its receptacle, all other wand stations are disabled and their busy lights come on. Each wand station is equipped with speaker which emits audible beep for each valid label scan by the light pen. 9170 version is compatible with all of the company’s readers; the 9171 with all status indicator readers. Unit mounts to wall or bench. Interface Mechanisms, Inc, PO Box N, Lynnwood, WA 98036.

See at Booth 3202
Circle 461 on Inquiry Card

HIGH SPEED ARITHMETIC PROCESSOR

Multiple accumulators, registers, and data paths along with high speed, high accuracy floating point arithmetic suit the FPS-100 to performing extended reiterative multiplication and addition algorithms. 38-bit floating point processor has 28-bit 2’s complement mantissa, 10-bit biased binary exponent, and a dynamic range of $0.5 \times 2^{-30}$ to $(1 - 2^{-m}) \times 2^{31}$. Registers consist of 64 36-bit floating point accumulators, 16 16-bit integer data registers, and 16 12-bit subroutine return stacks. 8k-, 16k-, 32k-, or 64k 38-bit words of MOS main data memory; 1k or 4k 64-bit words of program source RAM; 2.5k or 4.5k 38-bit table ROM plus 1 word RAM; and optional 4k or 8k table RAM constitute the processor's memory. Floating Point Systems, Inc, PO Box 23489, Portland, OR 97223.

See at Booth 2231
Circle 462 on Inquiry Card

ECLIPSE DATA SYSTEMS ENHANCEMENTS

Software additions to the Eclipse® C/150 family provide improved compatbility and greater system performance. Included are Advanced Operating System (AOS) support; INFOS QUERY, a general purpose online inquiry utility easing access to AOS INFOS files; AOS text entry and editing system, an optional utility for text processing applications, featuring extensive cursor positioning, flexible text manipulation, search, and replace; a virtual data capability for COBOL under AOS, permitting arbitrarily large data elements to be defined in a COBOL program; and availability of the X.25 protocol on all RDOS/RDOS/DOS computer systems to access public packet switched networks. AOS COBOL's screen management extensions for screen definition, display, and field I/O improve compatibility between Eclipse and Commercial Systems families; a common development system can be used with both families. Hardware is enhanced with the announcement of models C/150 and C/350, providing memory of up to 1M and 2M bytes, respectively. Data General Corp, Rt 9, Westboro, MA 01581.

See at Booth 2117
Circle 463 on Inquiry Card

MULTIUSER SMALL BUSINESS COMPUTER SYSTEMS

Designed for large scale programming in BASIC and COBOL, 1000/4 and /8 data systems consist of 16-bit CPU; 32k to 64k 16-bit words of dynamic RAM; 4 to 8 ADM-3A Dumb™ terminal consoles, respectively; bidirectional 180-char/8 Ballistic™ printer, and 10M-byte cartridge disc memory. All electronics, CPU, memory, and disc are housed in a single desk. Multiuser capability allows up to 8 users at the same time. Operating system and application program are maintained on disc and automatically brought into main memory in segments as required, reserving memory for data in-process and resulting in high throughput. Educational Data Systems' IRIS and Information Processing Inc's BLIS/COBOL operating systems provide communications and multiuser capability to as many as 16 separate terminals. Lear-Siegler Inc, Data Products Div, 714 N Brookhurst St, Anaheim, CA 92803.

See at Booth 2526
Circle 464 on Inquiry Card
COMMERCIAL/MILITARY ARRAY PROCESSORS

MAP-200 and -300 series 32-bit programmable, floating point array processors for use with 16- and 32-bit minicomputers reduce time needed to do strings of iterative arithmetic by several orders of magnitude. ATR and rack-mountable militarized units conform to MIL-E-5400 and MIL-E-16400, and are compatible with AN/AYK-14, /UYK-20, -41, and -42 minicomputers. All software developed for the commercial unit is transferrable to the militarized versions. Each MAP contains its own programmable CPU along with supervisory control software. Intelligent programmable interfaces and independent asynchronous bus structure permit host independent data I/O at transfer rates to 40M bytes/s. Processors provide 3 independent banks of memory and can be field expanded. CSP Inc, 209 Middlesex Tpk, Burlington, MA 01803.

See at Booth 421
Circle 465 on Inquiry Card

INTELLIGENT DISC DRIVE

Functioning as a disc drive, subsystem, or data management facility, the STC 2700 family features a microcomputer, Winchester disc technology with formatted capacities of 39M, 93M, and 200M bytes of fixed storage; dual ports; high speed, byte parallel data transfer; and bidirectional, full handshake communication protocol. Specs include track to track seek of 10 ms (worst case), and transfer rates of 0 to 2M bytes/s to user and 0.768M bytes/s to media. Avg seek and max seek, both including ontrack settling, are 25 ms (typ) and 60 ms (worst case), respectively. The traditional drive function replaces most hardwired servo logic for seek and head positioning, R/W circuitry, and speed control. At the subsystem level, the MC6801 based microcomputer performs device dependent functions, absolute address translation from relative address, error check and correction, and media defect handling. The integrated data management facility includes software tools—operating system, limited PL/1 compiler, editor, assembler, linker, loader, and batch command processor—for system programming. Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027.

See at Booth 3614
Circle 466 on Inquiry Card

1200-BIT/s FULL-DUPLEX ACOUSTIC COUPLER

VA3434 designed around the VA3400 modem, replaces present 300-bit/s couplers to increase data transmission by a factor of four, literally converting any telephone handset into an acoustic connection for a 1200-bit/s full-duplex data terminal utilizing 103-type modem protocol. Acoustic cups have a double flange seal to provide noise isolation.

See at Booth 1000
Circle 467 on Inquiry Card

VECTOR INFORMATION PROCESSOR

V.I.P. offline Plotmaster™ system consists of microprogrammed, multiple microprocessor based vector information processor and up to 8 5000 series electrostatic plotters and printer/plotter of the same or mixed types. Inputs may be vector plot, raster plot, or print information, all of which can be stored on the same 9-track multilife tape and plotted or printed under system control. Standard IBM tape formats, labeled or unlabeled, are accepted. Double buffered memories (15k bytes/buffer std, expandable to 64k bytes/buffer) allow overlapped data input, processing, and plotter data transfer for max hardcopy output speed. PLOT 5000 graphics software can be used on IBM System 360/270 with DOS, DOS/VS, MFT, MTV, VS1, SVS, or MVS operating systems. Plot vector information can be spooled using std IBM output writers. Gould Inc, Instruments Div, 3631 Perkins Ave, Cleveland, OH 44114.

See at Booth 3015
Circle 468 on Inquiry Card
9 big reasons why OEM's choose GTCO Digitizers & X-Y Tablets

Performance
GTCO DATATIZER X-Y tablets or digitizers give the best overall performance at the lowest overall cost.

Technology
Electromagnetic Absolute Ranging Digitizing (the superior operating principle) offers high performance digitizing through non-metallic material with up to a 1.0" thickness.

Simplicity
Only three items—tablet or digitizer work surface, cursor and a controller—represents a complete system.

Interfacing
Serial pulse or parallel data interface is standard. RS-232 and Micro/Firmware options available. Require ±5V and ±12V to ±15V.

Options
Eight standard tablet sizes from 6" x 6" to 42" x 60" (all sizes compatible with any cursor and controller) Resolution 0.001" (0.025 mm, 0.1 mm) and 0.010" (0.25 mm, 1.00 mm) Accuracy ±0.005". Optional ±0.003" (10 = 1 mil). Backlighting Rear Projection Crosswire and Pen Cursors Micro/Firmware Stand Alone Systems

Reliability
Tablets feature precision printed circuit grid for a lifetime of rugged, stable performance backed by an exclusive 2-year warranty. Cursors feature rugged, high-impact case and operate at high signal levels without preamps. Cursor switches field replaceable. Controller contains all active DATATIZER circuits and uses common 7400LS IC's located on one small plug-in controller board.

Interchangability
All tablet sizes, cursors and controllers may be interchanged without requiring adjustment.

Trouble Free
No adjustments, no preventive maintenance and no detrimental environmental effects. UL and CSA approval pending.

The Company
GTCO is an established graphic technology company with a better idea. We challenge you to evaluate and compare our technology and products and then join our Fortune 500 List of OEM users who are purchasing the new patented GTCO DATATIZER.
HARD DISC FOR SINGLE BOARD COMPUTER

Contained in separate unit attaching to single-board 8000-6 series computer, Shugart Winchester technology hard disc provides 15M or 30M bytes of online storage. Z80 computer, double-density disc controller, hard disc controller, 2 Shugart 8" (20.3-cm) floppy discs, and control electronics are contained in computer chassis. Both units are mountable. Altos Computer Systems Inc, 2338A Walsh Ave, Santa Clara, CA 95050.

See at Booth 52
Circle 469 on Inquiry Card

TAPE STORAGE SYSTEMS

Model 1200 stores up to 2M bytes unformatted data using 3 model 200 2-track Minidrives™. System records 1600 phase encoded bits/in (650/cm) at a 30" (76-cm)/s write/read speed and transfers data at 6k bytes/s. Built in ANSI/ECMA formatter provides phase encoding and decoding, automatic error checking on write and read using 16-bit CRC, bidirectional 30" (76-cm)/s read, and bidirectional 90" (226-cm)/s search. Modular design of 5.25 x 19 x 19.5" (13.3 x 48 x 49.5 cm) system allows mounting of from 1 to 3 drives and simplifies maintenance and service. System interfaces with RS-232, PDP-11, LSI-11, NOVA, SBC 80/10 or /20, and ROLM. Meeting MIL-T-21200 and MIL-E-16400, model 5100 also transfers 6k bytes/s. 5100 interfaces with same systems as 1200, but stores up to 4.2M bytes. Qantex, 60 Plant Ave, Hauppauge, NY 11787.

See at Booth 1607
Circle 470 on Inquiry Card

STATISTICAL NETWORK PROCESSOR

Microprocessor controlled data communications device functions as an intelligent concentrator and statistical time division multiplexer. The SNP-100 features multipoint option allowing the user to poll a number of remote sites along a single transmission line. Available in 2-, 4-, and 8-channel models, the processor maximizes operating efficiency by concentrating asynchronous inputs into a single high speed output.

Features include error checking routines, downline loading that permits changes in remote site operation to be made from a central location, and continuous self-testing. Optional command and diagnostics port monitors all important system functions and can alter most system operation parameters. Prentice Corp, 795 San Antonio Rd, Palo Alto, CA 94303.

See at Booth 404
Circle 471 on Inquiry Card

NOTE
Booths numbered 1000, 2000, 3000, and 4000 are located in the NY Coliseum on floors corresponding to the first digit; booths 300 to 999 plus suites are in the NY Hilton Hotel; and booths from 1 to 150 are in the Sheraton Centre Hotel at the Personal Computing Festival.

VIRTUAL MEMORY COMPUTER SYSTEMS

The communications oriented 3200 series offers 5 32-bit, virtual memory models that are IBM/360 and /370 compatible, using the VPS operating system; 3 simultaneous operating modes are online interactive, remote job entry, and batch. The systems handle COBOL, FORTRAN, PL/1, APL, BASIC, and assembler language. National CSS, Inc, 187 Danbury Rd, Wilton, CT 06890.

See at Booth 514
Circle 472 on Inquiry Card

MEMORY ENHANCEMENT UNIT FOR NOVA 3

A 15 x 15" (38 x 38-cm) memory expansion and hardware multiply/divide controller board for the Data General Nova™ 3 line of minicomputers extends the memory capacity of 64k bytes up to a max capacity of 256k bytes. Memory protect, memory parity, and hardware multiply/divide features are also available as options. Custom Systems Inc, 2415 Annapolis Ln, Suite 170, Minneapolis, MN 55441.

Circle 473 on Inquiry Card

SINGLE-BOARD MAGNETIC TAPE CONTROLLER

DU120 couples up to four 7- or 9-track 0.5" (1.27-cm) magnetic tape drives to PDP-11 computers. Completely contained on one quad module that occupies one SPC slot in computer chassis, unit emulates DEC TM11 controller and is completely software compatible with RT-11, RSX-11, RSTS, IAS, and MUMPS software systems. Single board design incorporates proprietary microprocessor that enables an automatic self-test feature to be used in isolating system malfunction. Automatic self-test constantly monitors controller for proper operation. Tape format is compatible with 7- or 9-track IBM and ANSI standards for DEC or IBM compatibility. Selectable tape speeds from 12.5 to 112.5 in (31.75 to 285.75 cm)/s are offered. Distributed Logic Corp, 12800-G Garden Grove Blvd, Garden Grove, CA 92643.

See at Booth 351
Circle 474 on Inquiry Card
Sorry Joe. It's custom MOS/LSI.

Chances are that in the fifties you were into custom cars too—who wasn't? But today you're designing systems, and custom means MOS/LSI.

If you're presently in production or breadboarding a system with discrete components and a batch of SSI and MSI integrated circuits, our high-density MOS processes will usually enable us to put your whole system on ONE CHIP at great cost savings. We've got high-voltage P-MOS technologies, as well as C-MOS capability. But, where we really shine is in our high-density n-channel silicon-gate COPLAMOS® technology, which virtually all our customers are now specifying for their high-performance, low-cost custom requirements. If you also need quick turn-around on mask-programmable options and patterns, we can combine COPLAMOS® with our most recent technological breakthrough CLASP™ (which stands for COPLAMOS Last Stage Programmability) to provide the solution.

Standard Microsystems is a total-capability supplier—all design engineering, wafer processing, assembly, and test is performed in our modern, Hauppauge, New York facilities. Our processes are usually compatible with current state-of-the-art processes used throughout the industry. Not only can we start your design from scratch, but we can enter the custom cycle at any point. If you have masks, we can process wafers, generate test procedures, assemble devices and final test.

So, the next time you have a need in the custom area, just peel out to Standard Microsystems and tell 'em Joe sent ya.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Boulevard, Hauppauge, New York 11787 (516) 273-3100 TWX: 510-227-8998
The largest manufacturer of MOS/LSI data communication circuits
CIRCLE 92 ON INQUIRY CARD
INTRODUCING THE PERKIN-ELMER 3220

The Highest Performance Mini.
Full 32-bit architecture. DMA bandwidth of 8MBytes. MOS memory in 256KB modules with error correction as standard. Memory error logging down to the chip level, if you want. Memory expansion to 4MBytes. Cache memory, 128 32-bit registers, number-crunching features no 16-bit mini can match. And, all for less than a PDP-11/60.

The Lowest Cost Supermini.
Outstanding run-time speed and accuracy. Fast, responsive program development. Easy, cost-effective program conversion. Check the comparison chart.

Either Way, We’ve Got Them Beat.

<table>
<thead>
<tr>
<th></th>
<th>DEC 11/34</th>
<th>DEC 11/60</th>
<th>P-E 3220</th>
<th>SEL 32/57</th>
<th>PRIME 550</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>16-bit</td>
<td>16-bit</td>
<td>32-bit</td>
<td>32-bit</td>
<td>32-bit</td>
</tr>
<tr>
<td>DMA Bandwidth</td>
<td>2MB</td>
<td>6MB</td>
<td>8MB</td>
<td>26MB</td>
<td>2.5MB</td>
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<tr>
<td>Maximum Memory</td>
<td>256KB</td>
<td>256KB</td>
<td>4MB</td>
<td>1.67MB</td>
<td>2MB</td>
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<tr>
<td>Number of Registers</td>
<td>8</td>
<td>16</td>
<td>128</td>
<td>8</td>
<td>128</td>
</tr>
<tr>
<td>Direct Addressing</td>
<td>56KB</td>
<td>56KB</td>
<td>4MB</td>
<td>.5MB</td>
<td>32MB (virtual)</td>
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<tr>
<td>Writable Control Store</td>
<td>No</td>
<td>Yes (opt.)</td>
<td>Yes (opt.)</td>
<td>Yes (opt.)</td>
<td>No</td>
</tr>
<tr>
<td>Shared Memory Support</td>
<td>No</td>
<td>No</td>
<td>Yes (opt.)</td>
<td>Yes (opt.)</td>
<td>No</td>
</tr>
<tr>
<td>Pricing – Processor</td>
<td>256KB, PF/AR, Systems Console, Chassis and Cabinet</td>
<td>$29,700</td>
<td>$41,900</td>
<td>$33,500</td>
<td>$41,600</td>
</tr>
<tr>
<td>256KB Expansion Memory</td>
<td>N/A</td>
<td>N/A</td>
<td>$10,000</td>
<td>$12,500</td>
<td>$15,000</td>
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<tr>
<th></th>
<th>Optimizer Technology</th>
<th>Average Compile Time</th>
<th>Whetstone Benchmark</th>
<th>Matrix Inversion Program</th>
<th>Binary Search</th>
<th>Price *</th>
</tr>
</thead>
<tbody>
<tr>
<td>3220 FORTRAN VII</td>
<td>Global</td>
<td>2000 LPM</td>
<td>2.25 Sec.†</td>
<td>3300 Sec.†</td>
<td>39 Sec.†</td>
<td>$ 88,600</td>
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<tr>
<td>VAX FORTRAN IV Plus</td>
<td>Block</td>
<td>1300 LPM</td>
<td>.85 Sec.</td>
<td>3700 Sec.</td>
<td>109 Sec.</td>
<td>$167,200</td>
</tr>
</tbody>
</table>

*Both 3220 and VAX configured with: 512KB, Floating Point, 10MB Disk, Dual Density Tape, OS, FORTRAN.
†Without cache memory option.

Visit Perkin-Elmer at the NCC, June 4-7, in New York.
Dynamic 32-Bit Software, Perkin-Elmer Quality.

The software available for the Model 3220 is exactly what you expect from Perkin-Elmer, a company whose reputation was built on quality products. It's true 32-bit software, tuned and proven where it counts: in the field. And not just for months. For years.

From the Inventors of the 32-bit Supermini.

When we introduced the first 32-bit supermini five years ago, we were known as Interdata. Now we are the Computer Systems Division of Perkin-Elmer, with over 2000 successful 32-bit installations worldwide.

The Model 3220 is the first member of our new Series 3200 family, with more to come. Advanced systems and software that will keep Perkin-Elmer the undisputed leader in 32-bit performance and price.

Find out how we've got them beat any way you look at it. Call or write for a demonstration today. Perkin-Elmer, 2 Crescent Place, Oceanport, NJ 07757. (800) 631-2154, Or, in New Jersey, (201) 229-6800.

CIRCLE 93 ON INQUIRY CARD

PERKIN-ELMER
A REAL TIME CLOCK FOR OUR 10th ANNIVERSARY

The 1845A Real Time Of Day Module features software selectable interrupts, sockets for up to 4K of optional EPROM memory (with the ability to jumper-select 4 EPROM types). Memory can be enabled or disabled, and the base starting address selected, by simply using the appropriate “on-board” switches. In addition to these features, counter output may be read in either hexadecimal or BCD code.

TIME CONTROL: The 1845A module gives you time control of software execution and processor operation. It provides timing for applications such as the real time monitor, executive software support, time-scheduled instrumentation programs, high resolution A/D support, process control monitoring and effective real time software development.

BATTERY BACK-UP: The battery back-up designed into our module can keep it running, even if power fails, for up to 30 days. The back-up power system features automatic recharging.

PCS/INDUSTRIAL MICROCOMPUTERS: The 10th anniversary of PCS celebrates 10 years of dynamic design and manufacturing experience that has led to one of the most complete lines of industrial microcomputers in the industry. So, whatever your industrial microcomputer requirements demand - complete systems, industrial microcomputer packages, or a broad line of modules, including super intelligent microprocessor modules, memory modules and a wide assortment of interfaces, the PCS standard product line is the solution.

For complete information contact your local PCS representative or call the PCS HOTLINE (313) 429-4971.

Process Computer Systems Inc.
750 North Maple Road, Saline, Michigan 48176
(313)429-4971 TWX:810-223-8153

CIRCLE 94 ON INQUIRY CARD
MICROPROCESSOR PRODUCTS FOR CONTROL SYSTEMS

The iCS™ family includes iCS 80™ chassis to aid in design and assembly of industrial control systems, and 3 signal conditioning/termination panels to ease interfacing signals to and from controller. Chassis is mechanical and electrical framework on which user can assemble a single or multiple card 8- or 16-bit microcomputer system. Termination panels iCS 910, 920, and 930 provide analog, digital, and ac-dc signal conditioning, respectively, per user requirements, and interface the system to external signal wiring. Of key importance, iCS 80 is built around the MULTIBUS™ backplane allowing designers to use an array of 5 CPU products including ISBC 86/12™, using the 16-bit 8086 microcomputer, and all ISBC 80™ series SBC products. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051.

See at Booth 1420
Circle 479 on Inquiry Card

PAPER MOTION MONITORS

Two monitors immediately signal a paper jam (or paper out condition) to avoid loss of data and eliminate retrieval time. Devices are mounted on the inboard side of XACTRON® tractors. Model PMP processor insures that paper actually responds to a line advance command; model PMD detector responds to every 0.080" (0.203 cm) of linear paper travel. Precision Handling Devices, 65 S Main St, Assonet, MA 02702.

See at Booth 4000
Circle 476 on Inquiry Card

SMART TERMINALS WITH PAGING OPTION

Independent paging added to the "Editor 1" line allows data to be input to a specific page rather than scrolled to another page of local storage. Data received from the host computer may be addressed from either page of the 2-page option without disturbing data contained on the unaddressed page. Data transmission to the host computer is also performed on an independent page basis, or both pages may be transmitted. EECO, Computer Terminal Products Group, 1601 E Chestnut Ave, Santa Ana, CA 92701.

See at Booth 1112
Circle 477 on Inquiry Card

FIXED MEDIA DISC DRIVE

Based on Winchester technology, model D800 has a max capacity of 20M bytes. Dimensions are 8.5" (21.6 cm) wide and 14.25" (36.2 cm) long. Mechanically interchangeable with 8.25" (20.96-cm) floppy disc drives, the unit can be mounted in most small business or multiterminal systems without changes. Pertec Computer Corp, Peripherals Div, PO Box 2198, Chatsworth, CA 91311.

See at Booth 3300
Circle 478 on Inquiry Card

DOT MATRIX IMPACT PRINTERS

Models 830 and 8300 are 7-wire, 80-col bidirectional dot matrix printers. The 830 prints 125 char/s and 70 lines/min. Available as printer mechanism or self-contained printer, unit’s sprocket paper feed accepts multi-ply pin feed paper from 3.5 to 8.5" (8.9 to 21.5 cm) wide. Paper can be loaded from bottom or from rear, and print line position is readily adjustable. The 8300 also prints 125 char/s but at 60 lines/min. 5 x 7 or optional 7 x 9 dot matrices form 96 ASCII characters in normal and double width. 8300 has 8-bit parallel interface and 1 line (80 normal width characters) buffer. Both print heads have a life expectancy of 100M char. C. Itoh Electronics, Inc., 5301 Beethoven St, Los Angeles, CA 90066.

See at Booth 358
Circle 479 on Inquiry Card

MICROPROCESSOR CONTROLLED COMMUNICATIONS PROCESSOR

Software programmable CM 9100 processor concentrates from 4 to 32 synchronous and asynchronous data streams into one high speed link using statistical multiplexing. X.25 level 2 link protocol employs GO BACK N ARQ for error free transmission between units. 50- to 19.2k-bit/s port speeds with ASCII, Correspondence code, and EBCD; CTS/XON-XOFF buffer overflow protection; built-in self-diagnostics; per line status displays; and downline loaded line characteristics are std. Compatible with the CP 9000 multi- microprocessor, basic unit includes 4 asynchronous/synchronous ports, 1 SDL/HDLC line, 16k-bytes buffer RAM, 12k-bytes RAM for application software, microprocessor, power supply, and chassis. Digital Communications Corp, 19 Firstfield Rd, Gaithersburg, MD 20760.

See at Booth 500
Circle 480 on Inquiry Card
FIXED DISC DRIVE

D160, fixed disc member of the D100 family, has 2, 3, or 4 discs, and stores up to 120M bytes in a volume of 5.6 x 12.2 x 21.9" (14.2 x 31 x 55.4 cm). Three drives can be vertically mounted in a standard 19" (48.3-cm) rack. The three versions provide 60M bytes on 2, 90M bytes on 3, or 120M bytes on 4 nonremovable discs, with 4, 6, or 8 low pressure heads contained in a sealed module. Head positioning is performed by reading servo data interlaced in each track. Heads automatically position themselves on required track. Densities exceed 7k bits/in (2.75k/cm) and 600 tracks/in (236/cm). MTBF is 8k h, and operating power consumption is 130 W. Drives are compatible with other D100 series units and can be intermixed on the same controller. Cir-Honeywell Bull, 200 Smith St, Waltham, MA 02154.

See at Booth 347
Circle 481 on Inquiry Card

MICROPROCESSOR BASED RS-232 CASSETTE SYSTEM

Storage system is composed of a master and from 1 to 3 slave drives. An 8035 microprocessor in the master handles all communication, data buffering, formatting, and drive control functions. Interfaces are RS-232-C or 20-mA current loop, with 8-bit parallel optional. Storage is up to 2M bytes/system. Search speed is 100" (254 cm)/s, with less than 10-s avg access time. 256 bytes of RAM buffer store is provided. Operation is totally asynchronous. Analog & Digital Peripherals, Inc, 815 Diana Dr, Troy, OH 45373.

See at Booth 3111
Circle 482 on Inquiry Card

SOLID STATE CAPACITIVE KEYBOARD

Featuring low profile contactless keys, this keyboard is enabled by custom designed NMOS encoder chip. Virtually any customer requirement can be custom built. Encoder requires 5 Vdc and provides encoding capability up to 10 bits for 110 keys, 4 modes/key. Any code, including ASCII, Baudot, and EBCDIC, may be selected. Estimated life is more than 300M operations. Externally adjustable scan time range is from 10 to 80 µs/key. Noise immunity circuit distinguishes between valid key depression and noise, and hysteresis circuit eliminates keyswitch "teasing." Burst rate speed capability is 1k char/s. Options include N-key rollover or lockout, repeat for all, no, or selected keys with repeat rate up to 900 Hz, and pulse or level strobes. Cherry Electrical Products Corp, 3630 Sunset Ave, Waukegan, IL 60085.

See at Booth 1022
Circle 484 on Inquiry Card

6800 FLOATING POINT ARITHMETIC

The floating point arithmetic/scientific function package for the Motorola 6800 family operates on 9-digit BCD values. It is written in 6800 assembly language and is supplied on either 7- or 9-track tape in both source and relocatable object form. Argument passing and calling protocol allow use with PL/W or assembly language programs. Wintek Corp, 902 N 9th St, Lafayette, IN 47904.

See at Booth 4022
Circle 485 on Inquiry Card

BAND PRINTERS

300-, 630-, and 900-line/min B-Series band printers each offer a variety of 69 easily interchangeable print bands in 22 languages. 48- and 96-char ASCII sets are optional. Units print 132 char/line; 300- and 600-line/min models offer optional 15-char/in (6/cm) density. Features include operator control and fault indicator panel, 6-part forms capability, swing out yoke and inline paper tractors for easy forms loading, paper status detecting sensors, and automatic turn-off of print band drive motor following any 30-s nonprint period. Printers are plug-compatible with DEC. Data General, Hewlett-Packard, IBM Series/1, Interdata, and RS-232-C interfaces. Digital Associates Corp, 1039 E Main St, Stamford, CT 06902.

See at Booth 1106
Circle 486 on Inquiry Card

COMPUTER DESIGN/MAY 1979
FOR MAXIMUM PERFORMANCE... IN A MINIMUM PACKAGE... EVERYONE AGREES... IT'S THE

DSR-100
BADGE READER

★ Completely solid state—maximum reliability and long-life.
★ Models for all standard punched badges.
★ Reads complete alpha-numeric code.
★ Complete validity check.
★ Absolute column count—regardless of punched data.
★ Low cost, small size.

This is the 100% punched badge reader. Provides complete read-out of all punched data with 100% reliability. Simple, compact unique design provides maximum interfacing capabilities.

Write for complete technical data

PROGRAMMING DEVICES DIVISION
SEALECTRO CORPORATION
MAMARONECK, N.Y. 10543
PHONE: 914 698-5900  TWX: 710-566-1110

Sealec product model:
1401 Ventura Blvd., Suite 215, Sherman Oaks, Ca. 91403, (213) 998-8157
1901 Old Middlefield Way, Suite 10, Mountain View, Ca. 94043 (408) 965-1212
Sealec Ltd., Portsmawth, Hants, England
Sealec S.A., Zone Industrielle Tallois Est, 83087 Tallois CEDEX, France

CIRCUIT COMPONENTS  R.F. COMPONENTS  PROGRAMMING DEVICES

CIRCLE 95 ON INQUIRY CARD

169
Many companies exhibiting at NCC '79 are showing products that have been announced previously or which were described in recent issues of Computer Design; still others supplied information that was too late or too little for processing as “first time shown” products. The following briefs are a sampling of the products that NCC '79 attendees can expect to be exhibited by some of those companies.

Applied Magnetics Corp (Booth 1312):
Printed circuit boards, interconnection devices, precision magnetic heads, and specialized test equipment

Astrocom Corp (Booth 363):
Microprocessor based tabletop keyboard/display terminal with ROM and various increments of RAM plus a single- or dual-floppy disc drive and matrix printer

Atlantic Research Corp (Booth 1129):
Intershake diagnostic test system, Interview II standalone data monitor, portable data test sets, and patching and switching equipment for data communications maintenance

BASF Systems (Booth 4630):
Single- and double-sided minifloppy disc drives and media, standard floppy disc media, rigid disc media, and 40M- and 80M-byte capacity storage modules

Boschert, Inc (Booth 4232):
OL 153E self-contained power module for 115- and 230-V input Qume printers and line of switching power supplies from 25 to 400 W

Centronics Data Computer Corp (Booth 1121):
High density dot matrix word processing printer plus serial dot matrix and fully formed character line printers and nonimpact micro-printers

Chromatics, Inc (Booth 4060):
of 8-color graphic and alphanumeric readout systems based on Z80 CPU plus full memory and I/O structure

Compucorp (Booth 113):
625 Mark II business computer with extended BASIC language operating system and up to 64k bytes of internal memory; can also be used for data acquisition and scientific realtime applications

For a limited time, Computer Interface Technology is offering the PENSEE Computer System, complete with 64KB RAM, floppy disk controller, two serial and a parallel I/O ports, CRT terminal, double density floppy disk drives, and 90 LPM printer for only $6995.

What is PENSEE™? It is the first mini system designed for direct high-level language execution. It executes PASCAL statements up to 10 times faster than comparable 16-bit systems available today.

See the PENSEE at the NCC Show N.Y.C. June 4-7, Booth #346

FEATURES:
- 64KB of high speed RAM memory
- Floating point hardware (proposed IEEE std)
- High speed 16-bit integer arithmetic
- DMA floppy disk controller
- Two RS232 async/sync ports
- Two 8-bit parallel ports
- System self-test microdiagnostics
- UCSD PASCAL language, operating system & utilities
- PASCAL MICROENGINE™ processor

TAKE ADVANTAGE OF THIS OUTSTANDING OFFER. WRITE OF CALL:

PENSÉE is a trademark of Computer Interface Technology

PENSÉE™ COMPUTER SYSTEM FOR ONLY $6995.00

See the PENSÉE at the NCC Show N.Y.C. June 4-7, Booth #346

PASCAL MICROENGINE is a trademark of Western Digital Corporation

PENSÉE is a trademark of Computer Interface Technology

CIRCLE 96 ON INQUIRY CARD
The best way to solve computer graphics hardcopy problems today.

And tomorrow.

Electrostatic printer/plotters from Gould.

Go ahead, be choosy. Because our 5000 series of electrostatic printer/plotters gives you easy solutions for even your toughest problems. And we're also working right now to satisfy your needs for the future.

Whichever model you choose, you can count on reliability, clear and crisp graphics, high contrast and high resolution. Most models are also UL 478 listed. And even at our high plotting speeds, hardcopy is dry thanks to our exclusive, patented closed loop toning system.

We also make it easy for you in other ways.

With software, intelligent and DMA interfaces, on-line, off-line and remote configurations. As well as support of popular computers such as IBM 360/370, PDP-11, HP-2100 and Data General NOVA/ECLIPSE series.

Let us tell you more about our patented designs, exclusive techniques and competitive features that can help solve your problems. For immediate help, call the toll-free number below. Or write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, Ohio 44114.

Call toll free for brochure: (800) 325-6400, ext. 77. In Missouri (800) 342-6600.

CIRCLE 97 ON INQUIRY CARD
Shortcut to Success.

Introducing iSBC 86/12™, the single board computer that brings the power of the 8086 to the Multibus™ standard.

There's no quicker way to implement designs with the new 8086 16-bit microprocessor than our new iSBC 86/12. It's dramatic evidence of the architectural capability of the 8086, with unprecedented computing power, memory and I/O capacity on a single board.

Multibus™ architecture ensures success.

The Multibus standard is your path to success with the iSBC 86/12 board. Since we introduced it in 1976 it has become the industry standard microcomputer bus. Even then we were looking forward to the 8086 and designed the Multibus architecture to support both 8- and 16-bit computers in single or multimaster systems, and a full megabyte of directly addressable memory.

That gives you unlimited design flexibility, with immediate access to the complete iSBC family of 8-bit computers, memory boards, and analog and digital I/O, peripheral control and communications boards.

Plus over 100 additional expansion boards from more than 40 independent suppliers. And Multibus compatibility means you can preserve your design investment as your application requirements grow from 8 to 16 bits.

iSBC 86/12™ designed from experience.

We drew upon all our design experience to make the iSBC 86/12 board the most advanced 16-bit single board computer available.

At its heart is our 8086 CPU that gives the iSBC 86/12 board ten times the processing power of our 8-bit single board computers. We added 32K bytes of dual port RAM, fully accessible by all Multibus masters in shared memory designs. There are sockets for up to 16K bytes of EPROM. And the advanced architecture of the 8086 addresses up to a full megabyte of system memory.

The iSBC 86/12 board has a flexible I/O structure, with 24 programmable parallel I/O lines and a programmable synchronous/asynchronous communications channel with RS232C interface and programmable baud rate generator. In addition, the iSBC 86/12 architecture provides nine levels of vectored interrupt control and two programmable interval timers.

And, with Intel, there's no penalty for success. When volume makes it more economical for you to build instead of buy your boards, we'll provide manufacturing drawings, pc artwork and a volume source for all the essential LSI components.

The same Intellec® Microcomputer Development System used with all Intel® microcomputers supports the iSBC 86/12 board with features such as ASM 86 assembler and PL/M 86 block-structured high level system programming language. You can debug your software right on your prototype system with ICE-86™ In Circuit Emulator or with the iSBC 957™ Interface and Execution package.

Attend an iSBC™ seminar in your area.

The best way to get started with this new-generation Single Board Computer is to attend the Intel iSBC seminar in your area. You'll learn about the iSBC 86/12 board and the rest of the iSBC product line. And we'll take you through the configuration and design cycle for several applications. For a seminar schedule and detailed information contact one of the Intel regional offices listed below.

And, for a free copy of our iSBC Configuration Planning Kit, or for on-site configuration or pricing assistance, write: Intel Corporation, Dept. 4-903, 3065 Bowers Avenue, Santa Clara, CA 95051.

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CIRCLE NO. 98 FOR CONFIGURATION PLANNING KIT
CIRCLE NO. 99 FOR CONFIGURATION AND PLANNING ASSISTANCE
The Anadex 80 Column Printer.

First check the specs. Then check the price.

Our new 80-column dot matrix line printer – the DP-8000 – combines high performance and operating convenience with a low price that's worth checking into.

☐ Check Performance
The DP-8000 features a precision engineered, heavy duty printing mechanism that can print the complete 96 ASCII character set, bi-directionally, at 84 LPM.

☐ Check the Interface
Included at no extra cost, are two input connectors (see photo) that provide three basic ASCII compatible interfaces: EIA Std. RS232C, for interfacing at up to 96000 Baud with most mini-computers and modems; the 20/60 mA current drive mode required by Teletype® ASR33-35 printers; and the parallel-bit, serial character synchronous Centronics compatible interface.

The DP-8000 includes 12 lines of internal FIFO buffer storage and can accept data continuously or in bursts. Optionally, increased buffer storage of 2048 characters can be supplied for CRT dump and similar applications.

☐ Check Printer Quality
A 9 × 7 character font provides virtually half-dot resolution for clean crisp print quality on the original plus three copies.

Precise paper positioning is ensured by a sprocket-feed paper advance, user-programmable Top of Form control, and up to 8 vertical tab positions.

☐ Check Convenience
For operating ease, the DP-8000 accepts paper through the rear or bottom of the unit, provides programmable Skip Over Perforation control, and Out of Paper indication and logic signal.

☐ Check the low Price
The best news is the price. A complete DP-8000 is unit-priced at under $1000, with substantial discounts in larger quantities.

Once you've checked out the performance and price, we think you'll agree that the DP-8000 is definitely worth checking into.

ANADEX, INC. • 9825 DeSoto Avenue • Chatsworth, CA 91311, U.S.A. • Tel: 213/998-8010 • TWX 910-494-2761
ANADEX, LTD. • Dorma House, Guildford Road • West End, Woking, Surrey GU24 9PW, England • Tel: Chobham (09905) 6333 • Telex: 858762 ANADEX G

CIRCLE 100 ON INQUIRY CARD
Computer Devices, Inc (Booth 1550): Model 1206 Miniterm® portable computer that also operates as automatic send/receive terminal; integral, alphanumeric bar code reader; and double-density minifloppy disc drives.

Computer Interface Technology (Booth 346): PASCAL Microengine™ computer system with stack oriented 16-bit processor, 64k-byte RAM, floating point hardware, and DMA floppy disc controller.

Computer Link Corp (Booth 3500): Magnetic tape and disc cleaners, testers, and degaussers.

Computer Transceiver Systems (Booth 1026): Variations of Executerm 4000 and 4080 terminals.

Conrac (Booth 1019): Model 480 microprocessor based CRT terminal and high performance color and monochrome video displays.

Cortron Div of Illinois Tool Works (Booth 2618): Series III solid state keyboard using linear ferrite core design, for large computer, interactive terminal, and microcomputer applications.

Cullinane Corp (Booth 2702): OLG 2.0 English language query facility, IDMS/DC teleprocessing monitor integrated with database management systems, and IDMS 5.0 integrated database management system.

Cutler-Hammer (Booth 416): Directrol® multiplexer system for up to 4096 signals in industrial control communications; functions alone or with DEC, Data General, or IBM computers.

Data Electronics, Inc (Booth 368): 34M-byte Microtape™ 7-track digital cartridge tape drive using group code recording for 7200-bit/in (2835/cm) density.

Data Processing Power Corp (Booth 379): MNIC series Powermobile, a self-contained movable power system with flexible shielded cables to conduct power to various computer components.

Data Products Corp (Booth 3224): 80-char/s thermal and 340-char/s impact matrix printers; and 300- and 600-line/min shaped character band and 300- to 1250-line/min shaped character drum printers.

Data/switch Corp (Booth 434): CPS-1000 computer/peripheral switch system, DCS-2000 data communications switch, CTS-3000 coaxial terminal switch, and DACS-4000 direct access control system.
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Megatek Corp (Booth 3319): Whizzard 7000 and 5000 vector refresh graphic systems (see pp 46, 51)

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Micro-Term Inc (Booth 320): Mime-I and -II computer terminals have switch selectable software compatibility with company's ACT-IVB, Lear Siegler ADM-3A, DEC VT52, and Hazeltine 1500 terminals

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STANDARD MODULES OFFER FLEXIBLE MULTIPROCESSOR SYSTEM DESIGN

Configuration of a variety of simple to complex systems, including closely coupled multiprocessors and loosely coupled networks is simplified by use of standard hardware modules which communicate over an asynchronous bus.

Alan D. Hirschman and Gamil Ali
Compunetics, Incorporated, Monroeville, Pennsylvania
Richard Swan
Carnegie-Mellon University, Pittsburgh, Pennsylvania

Designers have recognized that the microcomputer’s attractiveness as a low cost source of processing power is often outweighed by its low speed and limited addressing capability. For complex applications that have some inherent parallel structure, however, a distributed system of microprocessors can result in exceptionally effective design solutions which circumvent these limitations. There is debate over the best implementation of distributed microprocessor systems since almost all designs implemented to date are highly application dependent. Some applications, for example, favor loosely coupled networks in which independent processors send and receive limited commands or data from a central processor, usually over long distance, low bandwidth channels. Memory sharing is neither essential nor practical in such systems. Distributed systems of this type, which generally incorporate several microprocessors as satellite controllers for a central processor, have been used commercially. Other systems require much closer coupling among processors in which interprocessor communication takes place over one or more high bandwidth channels to shared memory, usually without the aid of a central controller. This configuration characterizes a true multiprocessor as opposed to a network. A structural approach to multimicroprocessor system design uses computer modules based on the Texas Instruments TMS 9900 microprocessor as building blocks to configure systems ranging from limited standalone controllers, through loosely coupled networks, to closely coupled multiprocessors with up to 128M words of memory shareable among all processors. Modularity and expandability, the primary goals in the hardware design, are ultimately aimed at drastic reductions in design time and cost for customized systems of varying degrees of complexity.

An application in which five processor modules are put to work in a closely coupled multimicroprocessor to perform a realtime communications and control task uses four microprocessors, each servicing an independent synchronous communication channel that receives and transmits data over full-duplex serial lines at 4800 baud. The four microprocessors format data, check for errors, and initiate certain control functions. Communication among processors is done largely through memory sharing. A fifth microprocessor receives data from the other four microprocessors, maintains a direct memory access (DMA) channel to and from an external computer, and provides an asynchronous interface for operator monitoring and intervention through a front
panel and a terminal. While this particular application could have been performed by one fast minicomputer with real-time multitasking capability, the modular multimicroprocessor approach results in considerable cost reduction and software simplification. Although the microprocessor is a relatively slow device, the parallelism obtained in closely coupled multiprocessors greatly enhances system speed and throughput. In addition, future expansion of the system is accomplished easily by adding more microprocessors, and without significant increase in overall cost.

Another attractive capability of the multimicroprocessor approach over the single multitasking minicomputer is the potential for increased system reliability. Reliability can be increased by allowing more than one microprocessor to perform the same critical tasks in parallel. The increased hardware redundancy is not cost-prohibitive because processor modules are relatively inexpensive. In this application, reliability is achieved by having a duplicate multiprocessor system ready to take over if the online system fails or must be shut down for maintenance.

**System Capabilities**

Several capabilities that are highly desirable in a multimicroprocessor architecture are implemented in the microprocessor based modules. Fundamental to the design of a closely coupled multiprocessor system is the ability of all processors to share portions of physical memory. The design allows a processor access to a local physical memory that while reserved primarily for its own use may also be shared among other processors. This use of shared local memory is similar to the structure used in CM*, a multiprocessor developed at Carnegie-Mellon University. Arbitration logic resolves competition for use of each processor’s memory bus. The principle of “circuit switching,” whereby a direct signal path is established between a source processor and a destination memory, is used instead of the “packet switching” technique in which data can be held at convenient nodes in the system while segments of the data path are established. Although packet switching makes more efficient use of system resources, such as the interprocessor bus, the circuit switched design simplifies the hardware structure.

A memory map facility expands shareable address space from 32k to 128M words. Each processor requiring access to a large shared memory space has a map module. The map is implemented as a fast 16-word register which can be loaded under program control to translate a 2k page anywhere within the 128M word shareable address space. (Note that total system address space, which includes private as well as shareable memory, can be considerably larger than 128M words and is, in fact, proportional to the number of processors in the system.)

Processors are linked together by a single interprocessor bus (IBUS) which carries address, data, and control lines. The use of a single bus shared by more than one processor places some constraints on the designer. The most important constraint requires that most of a processor’s memory references should be to its local memory and that use of the IBUS should be minimized. Requests for IBUS are initiated by the need to access shared physical memory that is associated with another processor.

Contention for the IBUS is resolved by an asynchronous rotating priority technique. In this method, processors are organized in a closed ring, and bus control passes around the ring in one direction. The processor currently in control of the IBUS must wait until all other intervening requests have been serviced before it can gain control again. By giving all members of the system an equal chance to control the IBUS, this technique prevents “starvation” of low priority processors, which would otherwise occur in a fixed priority scheme. Also, unlike synchronous bus arbitration schemes, which allow a processor to access the IBUS only during a specific time slice, the asynchronous system ensures that the processor currently controlling the IBUS immediately conditions the logic for transfer of bus control to another requesting processor. Control is actually transferred when the current IBUS transaction is completed.

Additional hardware implements a lock function and a powerful method for initiating interprocessor control functions. A lock signal prevents simultaneous access by two or more processors to certain critical data structures in shared memory, such as stacks or queues. The hardware provides an indivisible test-and-set instruction which sets or resets the lock. Interprocessor hardware interrupts are initiated by writing into specific addresses in the physical memory associated with the destination processor. In the same way, certain control functions can be initiated so that a source processor can force the destination processor to go through an initialization sequence or to relinquish control of its address and data buses. The latter function is useful as a hardware diagnostic.

**Basic Computer Modules**

Fundamental building blocks for the modular system are the TMS 9900 16-bit microprocessor and a 2k memory, which may consist of some combination of random access and programmable read-only memory (2114 RAM and 93453 P/R/ROM) (or their equivalents, respectively). The microprocessor architecture lends itself to the realtime processing environment. Transfer of program control between realtime tasks (context switching) is done efficiently by maintaining most of the machine’s working registers in memory. When a context switch is made, only three additional registers need to be stored to preserve machine state. The basic processor/memory module can be expanded by adding more memory [2708 or 2716 electrically programmable read-only memory (EPROM)], synchronous and asynchronous communications controllers (TMS 9903 and TMS 9902), and 4-channel DMA controllers (Intel 8257 or TMS 9911). Each of these functional modules (Fig 1) is physically implemented on a 4.5 x 5" (11.4 x 12.7-cm) double-sided printed circuit (PC) board, which is tied into the system through a wire-wrapped backplane. Address, data, and control lines
Fig 1 Basic modular system. Simplest system consists of two modules implemented on double-sided PC boards. First module contains microprocessor and support circuitry; second module contains up to 2k of 16-bit RAM and/or EPROM. Programmable I/O interfaces, DMA controller, and additional memory (maximum 32k) expand system capability. Address and data lines are buffered for expansion module which supports more memory, control, or special device interfaces.

Fig 2 Memory sharing methods. Independent processors transfer data through common or shared memory (a) in some systems. Allowing a processor direct access to shared memory local to any other processor, system (b) requires one access to interprocessor bus (IBUS), while system (a) requires one bus access to transfer into common memory and second access to transfer out to destination processor.
are buffered so that additional memory, communications controllers, DMA channels, and other specially designed interfaces can be added to the system in a modular fashion.

**Interprocessor Communication**

In many applications it is necessary that more than one processor have rapid access to data or executable code anywhere in the system. Closely coupled multiprocessors, which require much more rapid access to information than most networks, need to share memory over at least one high capacity channel. One method of memory sharing provides a common area which is accessible to all processors [Fig 2(a)]. Arbitration hardware, centrally located at the common memory, controls the use of the common system memory bus. An alternative design associates shared memory with each processor module in a decentralized fashion [Fig 2(b)]. In this system, hardware associated with each processor module determines which regions of its memory space are shared, which are private, and which are accessible by reference to another processor's physical memory. The latter design is preferred, first, because only one access to the IBUS is required to transfer a data word to or from shared memory and, second, because its symmetry makes highly modular hardware possible.

Fig 3 illustrates how the address space of two processors can be apportioned. Some areas of physical memory are private, that is, accessible only by one processor module; shared memory is physically associated with one processor but is accessible to all modules; and remote memory is accessed by transfer over the IBUS to shared physical memory in another module. Since system performance is limited by the bandwidth of the single IBUS, the design is most effective if each processor makes reference primarily to its local memory and uses shared memory in other modules sparingly.

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In this system design, 32k 16-bit words of memory are shareable, although the addition of private memory in each module implies that total system memory is proportional to the number of modules. To obtain a much larger memory space, a memory map module that is capable of translating any 2k page of memory into a 128M-word address space (Fig 4) is implemented on a single printed circuit (PC) card. Four page bits are used to address a 16-word register which appends 16 page bits to the processor's 11 low order address bits. During system initialization, each processor loads the map registers from a private 1k ROM; any time afterward, the map can be loaded under program control. The map can also be read by its associated processor for diagnostic purposes.

**Modular Multimicroprocessor Architecture**

Basic computer modules can be easily linked together to form a multimicroprocessor (Fig 5). Address, data, and control signals are carried over the single IBUS. A path to the local memory bus is established by a memory bus allocation module. This module's task is to determine upon every clock cycle whether the local processor or an external processor has access to shared local memory. Address, data, and control transceivers are normally disabled until a decision is made to allow a local or an external memory reference, after which the appropriate signal path is enabled. Remote references to physical memory in another module initiate action by the interprocessor bus arbiter module. If there is no activity on the IBUS, the processor module requesting a remote reference receives bus mastership. Only then is a path enabled for data, address, and control from the local memory bus to the IBUS. The destination processor sees the memory cycle carried on the IBUS as an external memory reference, then completes its current local memory cycle, if any, and establishes a path to the local memory bus for the source processor.

These arbitration procedures eliminate the possibility of a deadlock, which occurs when two or more processor modules simultaneously allocate a single resource for themselves, effectively blocking the system. Consider the case in which module A makes a remote reference to local memory in module B and gains control of the IBUS. Suppose that module B now decides to make a remote reference to local memory in A and also establishes a path to the IBUS. Neither memory reference will complete under these conditions.
since deadlock will occur. The memory bus allocation module prevents deadlock during remote references by allowing a path from processor bus to IBUS only after IBUS mastership is obtained.

An important capability of this design is that memory control signals MEMEN (memory enable), WE (write enable), DBIN (data bus input/output), and READY (memory is ready) are carried over the IBUS between source and destination modules to control data flow to and from memory. The design also allows for the possibility of burst mode DMA transfers over the IBUS between devices and memories in different modules; in this case, memory bus allocation logic overrides the normal procedure that allows local memory cycles to resume after the external memory reference completes. In general, burst mode DMA over the IBUS is used infrequently because it blocks all other processors from the IBUS.

To achieve orderly allocation of the local memory bus, each processor uses its own system clock to synchronize local and external references. The timing diagram, Fig 6, illustrates how local memory is allocated when local and external references compete. An external processor has obtained mastership of the IBUS
and seeks to obtain a path to the local memory by placing its MEMEN signal on the IBUS as IMEMEN. At the trailing edge of clock $\phi_1$, a local memory reference begins (MEMEN active), and the external reference (IMEMEN active) is synchronized. At $\phi_3$, the allocation logic allows the local reference to proceed. The external reference waits until the local reference completes. While the external reference proceeds, another local memory reference is attempted by the destination processor, but it must wait until the external reference completes.

Interprocessor Bus Arbitration

An asynchronous rotating priority scheme (Fig 7) arbitrates the use of the IBUS among contending processors seeking remote memory references. Processors are organized in a ring which is linked by a daisy-chained GRANT line. This structure is particularly suitable in multiprocessors without a centralized controller. The GRANT signal is passed around the ring from the current master to the processor with the earliest request. In the event of simultaneous requests, the processor physically closest to the current master will have its request latched and then will receive GRANT, thereby becoming the potential "next master." The GRANT signal passes directly through a processor which has no latched request, but goes no further than the "next master." When the current master relinquishes control of the IBUS, the next master immediately takes control. A processor can request use of the IBUS from itself if no other processor is actively requesting. The minimum time for transfer of mastership is dependent upon the greatest physical distance between two processors. In the present system, a minimum of 500 ns is required between a request for the IBUS and receipt of bus mastership.

At power up, a special module asserts initial bus mastership, although it is incapable of requesting the bus itself. The interprocessor termination/control module (Fig 5) provides resistor termination networks for the interprocessor bus, but it also monitors IBUS activity. If bus mastership is lost in the system due to noise or component failure in one or more processor modules, the interprocessor termination/control module asserts mastership after a switch-selectable timeout period and reinitializes the IBUS arbitration logic throughout the multiprocessor system. Without this capability, all IBUS activity could be blocked by a failure in one module.

Control Structure

System design makes use of the IBUS to transmit and receive control commands as well as data. As shown in Fig 8, by writing into a few user-specified remote memory locations, one processor can control the destination processor through hardware initiation of the following three actions:

Interrupt on two hardware priority levels—This process is useful for "handshaking" in which one processor must notify another that some action has been taken. The TMS 9901 on the communications controller module contains a network capable of prioritizing up to 16 hardware interrupt levels and generating 16 software programmable outputs that assert hardware interrupts or other controls. In an application where each processor must be able to interrupt any other, the number of direct hardwired connections will increase as the square of the number of processors. These connections are all eliminated, however, with the control structure shown.

Reset/load function—By the same method, the source processor causes the destination processor to go through one of two possible initialization sequences.

Hold function—Any processor can cause another to
Fig 9 Multimicroprocessor application. In communications application data must be manipulated, formatted, and transferred to and from external computer and four independent full-duplex serial channels. Each of four slave communication microprocessors reformats data from serial channel and writes into shared memory of master microprocessor. Master sends data to external computer over DMA channel. Commands and data from external computer are written into shared memory of appropriate communications processor. Operator can inspect and modify activity anywhere in system through terminal maintained by master.

Multimicroprocessor Application

A complete communication system has been designed and built (Fig 9) based on the modular architecture described. The application is ideal for a multiprocessor system because of its highly parallel structure.

Hardware Structure

Four slave processor modules communicate independently with an external system through 4800-baud modems which are each interfaced through a TMS 9903 synchronous controller. The controller transfers data to and from its associated processor over a special serial line called the CRU bus. Each slave communicates over the IBUS with a master microprocessor, which supervises activity of the slaves and provides a DMA channel to an external computer. The master uses shared memory in the slaves for two principal purposes: to write data from the external computer, which the slave then reformatst and transmits to the modems; and to issue commands and data for use by diagnostic programs (memory and instruction tests) executed by each slave. Slaves, in turn, use shared memory in the master to write reformatted data received from the modems, as well as status words generated by slave diagnostic programs. Each slave operates primarily within its local memory; only 5 to 10% of all memory references require access to the IBUS. Total physical memory in this system (less than 32k) is partitioned among the five microprocessors. With the exception of the top and bottom 1k pages required for initialization of each processor, all memory is shared.

The master microprocessor maintains an asynchronous controller (the TMS 9902) to load executable code from an FS 990 minicomputer on which all assembly level software is developed. Code that has been partially debugged on the disc based development system is loaded by the TMS 9902 over an EIA standard serial channel and distributed to RAM throughout the system for final checkout. Although fully debugged software
resides on EPROMs in the operational multimicroprocessor, field changes to the software are necessary occasionally. Since the development system is unavailable in the field, a cassette tape unit is used to load programs into RAM, which is substituted for EPROM during software modification in the field.

A DMA controller based on the Intel 8257 is also maintained by the master microprocessor. The DMA controller services both an input and an output channel to an external processor. The 8257 controller transfers data only between shared local memory in the master microprocessor and the external computer's input/output channels; thus use of the IBUS for DMA transfers is avoided.

Software Structure

Modularity of the multiprocessor is reflected in the application software. Each communications slave microprocessor executes local code that is duplicated in each slave module. All slaves operate independently of one another but are allowed to receive and to issue commands, status words, and data during infrequent communication with the master. The beginning and end of important events are signaled by interprocessor interrupts. Master and slave microprocessors maintain very simple monitors which handle interrupts and take action upon receipt of status or command words. Processed data blocks from the slaves are queued by the master for transmission over a DMA channel to an external computer. In addition, the host maintains a debug monitor that runs concurrently with the real-time task. Through a terminal, an operator may examine activity anywhere in the system and intervene in the operation of any slave.

At system initialization, extensive checks are performed on system memory, instruction set, and integrity of the IBUS. A front panel alphanumeric display presents diagnostic information in the event of failure, permitting fault localization to the module level.

Summary

With system architecture that allows modular development of flexible designs from off-the-shelf PC cards, the multiprocessor system concept greatly extends the power of the individual microprocessor in those applications with inherent parallel structure. Principal benefits of this approach to system design are modularity, expandability, software simplification, and low cost. Circuit switched hardware provides functional capabilities that include memory in each processor that is accessible by any other processor in a system. Physical memory associated with a processor can be private (accessible only by the associated processor) or shareable by all processors in the system. The memory mapping facility expands shareable address space from 32k to 128M words. Total system memory, consisting of both shared and private areas, is proportional to the number of processors. Bus arbitration hardware uses an asynchronous rotating priority technique to allocate use of the interprocessor data, address, and control buses. Hardware achieves multilevel priority interrupts and other control functions among processors by decoding unique addresses on the interprocessor bus, eliminating the need for direct wire connections of interrupt and control lines.

One important limitation of this design approach is the use of the single interprocessor bus, which imposes constraints on the volume of communication traffic that can be supported. To prevent impaired system performance, each processor's executable code must have a high degree of "locality," requiring infrequent access to the interprocessor bus.

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Alan D. Hirschman received his undergraduate degree in physics from New York University and his Ph.D. in electrical engineering from Carnegie-Mellon University where his research interest was in the area of optimal algorithms for waveform compression. He is presently employed by Compunetics where he is involved in research and development for multiprocessor systems.

Gamil M. Ali is a project manager at Compunetics. He holds a BSEE degree from the University of Cairo, Egypt and an MSEE degree from the University of Pittsburgh. He is a member of the IEEE.

Richard Swan holds a BS degree in computer science from the University of Essex, England, and has completed his Ph.D. in computer science at Carnegie-Mellon University where he was principal designer of hardware implementation and architecture of CM+. Currently holding the position of assistant professor at CMU, his research interests include parallel architectures, addressing structure design, hardware support for operating systems, and performance evaluation.
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AN OVERVIEW OF MILITARY TACTICAL DISPLAY TERMINALS

Examination of an idealized modern military tactical display terminal and trends for the future are covered as well as objectives, applications, inputs, hardware, software, and display operation in a command and control environment.

Edward W. Gennetten  
Naval Ocean Systems Center, San Diego, California

Basic functions of a tactical display terminal are to improve military decision making and to expedite human reaction time—key elements in a command and control environment. The increasing speed and sophistication of offensive weapons systems have substantially narrowed the time available to diagnose a threat and to take appropriate countermeasures. The military tactical display terminal must present complex data in a format that can be quickly, clearly, and correctly comprehended.

Fig 1 illustrates the general appearance of a model tactical display terminal. For purposes of perspective, a model of a simple command and control system configuration is shown in Fig 2, in which each system display terminal can be assigned a different mode of operation. For example, terminal 1 may be dedicated...
to an air/surface tracker mode of operation, where
the operator uses sensor returns (eg, radar), for track-
ing targets. Display terminal 2 may be dedicated to
a target identification mode, where the operator anal-
yzes input data and identifies target types. Display
terminal 3 may be dedicated to an air intercept con-
troller mode, where the operator dispatches
friendly interceptor type aircraft toward unidentified
targets. Display terminal 4 may be dedicated to a fire
control coordinator mode, where the operator imple-
m ents the selecting, loading, arming, and firing of a
weapon.

Commonality between the system display terminals
facilitates casualty backup procedures and system ex-
pansion, simplifies training programs, and reduces
maintenance, acquisition, and other support costs. Sig-
nificant differences in the system display terminals
may reside only in software, but differences may also
exist in hardware because of modular construction
providing substitute capabilities. By interchanging read-
only memories (ROMS), data entry devices, or computer
and sensor interface modules, a display terminal can
be adapted for different modes of operation within a
single system display configuration. Currently, tactical
systems predominantly utilize random scan cathode ray
tube (CRT) displays.

**Display Terminal Inputs and Outputs**

Two primary sources of input information transformed
into meaningful imagery by tactical display terminals
are sensor data and computer data. Common examples
of sensor data are radar, sonar, and television signals.
Common examples of computer data are range, bear-
ing, speed, and target course information.

To select sensor information (Fig 2), the display
terminal operator initiates a request to a host computer
for a sensor presentation. The host sends a switching
message via the computer select and data distribution
unit to the sensor select and sensor data distribution
unit, which in turn couples the selected sensor signals
to the requesting display terminal. Sensor inputs may
be digital, analog, or a mixture of both.

Two-dimensional radar is a common sensor with in-
puts consisting of at least three component signals:
video, main trigger, and azimuth. Radar video is usually
analog, main trigger is a binary pulse, and azimuth
is in one of three common formats: 5-wire synchro,
azimuth change pulses (ACP)/azimuth reference pulse
(ARP), and in recent systems a digital word of typi-
cally 12 bits. Three-dimensional or height finding radar
has more complex video, trigger, and azimuth signals,
as well as elevation signals.

Sonar signals, like radar signals, vary in complexity
and nature from system to system. Typically, a set
of sonar signals includes sonar video, bearing informa-
tion in the form of ramp modulated sine and cosine
functions, an unblanking signal, and a sound reference
in the form of a sine wave with frequency variable
over a small range.

Television video includes camera, video tape, and
synthetically generated signals. In some systems, televi-
sion video is redirected to an ancillary raster scan
display mounted above the tactical display terminal
for displaying alphanumeric messages relating to
status information and alerts.

Computer data consist of serial and/or parallel
words that usually range between 16 and 36 bits.
There are four types of computer words in use. Two
types, output data words and external function words,
are employed to transmit information from the host
computer to the display terminal. (The word "output"
is referenced here with respect to the host computer
and not to the display terminal to be consistent with
the input/output (I/O) interface standard MIL-STD-
1397.)
Output data words transmitted to the display terminal consist of instruction, data, and control words. Only instruction and data words are loaded into the display terminal memory, and a set of these is referred to as a message. Control words are not loaded into the display terminal memory, but perform functions such as determining which messages will be accepted by a certain display in a series of displays, perhaps where a certain message will be loaded in memory, and which legends will be illuminated on display control pushbuttons.

External function words from the host computer are used either to control or initiate the interrogation (polling) of a peripheral device. Control over a display terminal includes such actions as setting the refresh rate, selecting range scale, extinguishing a cursor, and enabling blocks of memory. Control over the computer select and data distribution unit includes requesting, forcing, and releasing control of various interconnections between computer and terminal.

Interrogation of a display terminal by the host computer involves gathering status information, such as the contents of selected registers, particularly those associated with data entry devices, eg, trackball registers. To start interrogation, an external function word alerts the display as to the nature of the request; the display terminal responds by transmitting status information back to the host computer, using input words, the third type of computer words. The fourth type of computer word, interrupt word, is also used to transmit status information from the display terminal to the host computer except that interrupt words are initiated within the terminal.

**Display Terminal Architecture**

A representative block diagram of a tactical display terminal is shown in Fig 3. In actual military displays the relationship between the blocks may be modified, and other blocks may be deleted or added.

**Computer Interface**

Host computer data enters the display terminal via the computer interface, which may contain one or more I/O ports. The most widely used computer interface employed in Navy tactical display terminals, as described in MIL-STD-1397, consists of four interface types:

1. NTDs fast parallel -3 V 250k words/s max
2. NTDs slow parallel -15 V 40k words/s max
3. ANEW parallel 3.5 V 250k words/s max
4. NTDs serial ±3.5 V 10M bits/s max

NTDS is an acronym for “Naval Tactical Display System,” while ANEW is a designation. Voltage levels for logic 0 and 1 differ among these interfaces. Fig 4 illustrates input and output data lines and associated handshaking signals for the first three interface types. Before transfer from the host computer to the display terminal, a message and associated control words define a buffer within the host computer memory. The sequence of events occurring in the transfer of buffer contents to display terminal is given below for the output channel (Fig 4(a)):

1. Program control in host computer initiates output buffer for a given channel.
2. Display terminal sets output data request signal when it is ready to accept data.
3. Host computer detects an output data request signal.
4. At convenience of host computer, first output word in buffer is placed on output data lines.
5. Host computer sets output data acknowledge line, indicating that output word is ready for sampling.
The display terminal is the controlled device or slave. The external interrupt enable line permits the display terminal to transmit interrupt words. In general, the input channel (Fig 4a) also follows a similar description for the output word buffer. All the steps in this sequence, except the first, are repeated for every output word until the number of words specified in the output buffer have been transferred. The host computer has the option of forcing any output word from the output buffer regardless of the state of the output data request line. A description of the sequence of events for transfers of an external function word buffer parallels the above description for the output word buffer.

Transfer of an input buffer or interrupt word over the input channel (Fig 4b) also follows a similar sequence except that the input data flow is from display terminal to host computer. The input data acknowledge line is common to both input transfer operations. The external interrupt enable line permits the display terminal to transmit interrupt words. In general, the host computer is the controlling device or master, while the display terminal is the controlled device or slave.

The external function request and external interrupt enable lines are not available on all Navy systems. The serial computer interface consists of one coaxial cable for an input, and one for an output channel. Serial transfers are accomplished by using two types of pulse trains. The first, called a control frame, consists of three bits—a sync bit followed by two control or handshaking bits (request and acknowledge type information). The second pulse train consists of $2n$ bits—a sync bit followed by a word identifier bit and, then, $n$ information bits. The transmitting device sets the identifier bit as follows:

Display terminal: 0 input word
1 external interrupt word
Host computer: 0 output word
1 external function word

After the incoming computer data has crossed the interface boundary, it is level shifted and subjected to interface processing, which generally includes error detection, retiming, and distribution.

**Display Terminal Processing**

Instruction and data words transferred from the host computer are stored in the display terminal memory (Fig 3). Memory size in modern tactical display terminals ranges from 65k to 130k bytes. These large memories allow greater amounts of software resident in the display terminals, increase the processing capabilities of the terminals, and reduce the load on host computers.

Display terminal memory contains data words and two types of instruction words. The first type of instruction words consists of macroinstructions such as ADD, JUMP, SHIFT, and COMPARE. These instructions make up resident programs such as loader, debug, diagnostic, and operational programs. The data words contain information such as a missile's velocity and altitude, and are used by the operational program. This program generates a second type of instruction word called a display instruction. Display instructions determine the nature of the display imagery, which consists of alphanumeric and graphic data. Representative display instructions in terms of simple labels are TEXT, VECTOR, CIRCLE, and ELLIPSE. A set of display instructions is commonly referred to as a display file, or list, and is modified frequently in an operational environment. Operational programs in both host computers and display terminals process input information to create the display file.

The display processor (Fig 3) handles conventional processing operations such as those dictated by the operational program, eg, creating display instructions. This processor employs a bit slice bipolar microprocessor configured to give a 16- to 36-bit machine with a nominal instruction execution time of around 1 µs. Microinstructions stored in partially filled ROMs define the aforementioned macroinstructions and offer the capability to input additional macroinstructions.

The display controller (Fig 3) retrieves display instructions from the display file in a sequential manner, processes them, and couples the resulting data to the function generator, which generates the display.
imagery. This controller may be implemented with a microprocessor or microcontroller having general purpose working registers and an arithmetic logic unit. The controller may retrieve a subset of conventional instructions, such as JUMP, CONDITIONAL BRANCH, WAIT, and SUBROUTINE CALL, which increase the capability of the display in certain applications. In any case, the number of these instructions in a display file is limited, relative to the display instructions used by the display controller.

Periodic retrieval of the display file by the display controller involves display refreshing. If the refresh frequency is too low, the imagery will flicker. If the refresh frequency is programmable, the time per picture frame may range from 15 to 250 ms. Minimum refresh frequency to avoid flicker depends on phosphor persistence, ambient light level, electron beam intensity, writing rate(s), size of display file, and amount of timesharing with realtime sensor data.

Processing by the display controller includes manipulation and modification of the display file to increase display effectiveness. Examples of display file processing are translating, scaling, and scissoring. Translation involves the movement of the display presentation in the X, Y plane, scaling is the magnification or contracting of the display presentation, and scissoring is the filtering of the display instructions into two instruction sets. One set includes display instructions that create the display presentation seen on the physical screen. Depending on application, the number of picture elements (pixels) on the screen usually ranges from 512 × 512 to 2048 × 2048, with 1024 × 1024 the most common size. The second set represents those instructions that define imagery off the physical screen, that is, imagery in the virtual screen less the physical screen imagery. The virtual screen is usually four to eight times larger, depending on the number of range scales required. For example, the virtual screen may be defined by a field of 17 bits for both X and Y, which relate to a 128 × 128 mile area. If the physical screen is defined by 10 bits in X and Y, the range scale setting will determine which 10 adjacent bits out of 17 will be selected. The 10 most significant bits will define maximum range scale. Each successive shift of 10 adjacent bits, towards the least significant bits in the 17-bit fields, results in a 50% reduction in range scale.

**Function Generator**

The function generator consists of three component generators: character, vector, and conic. The character generator can produce numeric, alphanumeric, and special symbols with a typical repertoire ranging from 128 to 256 characters. Some characters may be RAM programmable with the remainder reprogrammable only by ROM modification. RAM programmable characters or symbols are created by a set of special display instruction words.

Numerous character generation techniques have been developed for random scan displays. The most common technique, the stroke writing method (Fig 5), involves sequentially coupling various X and Y deflection waveforms to their respective deflection circuits. Each stroke is contained within a clock time interval. Beam intensity is also blanked or unblanked by Z-intensity modulation of the CRT grid within a clock interval. The number of strokes used in producing a character typically ranges from 8 to 32. Character generators usually have the capability under computer/operator control to rotate characters by 90°, blink, change sizes (usually 2 to 4 sizes), and change brightness levels (usually 2 to 4 levels). The ratio of X to Y sweep (width to height) amplitude per stroke may also be programmable; this ratio in Fig 5 is 2:1.

Vector generators can also be implemented by several methods. All methods end up with positive or negative ramps applied to the X- and Y-axis deflection systems to produce a vector on the display screen. The two most common types of vector generators produce either a single vector having a wide range of possible lengths and orientation, or produce a chain of short vectors connected end to end. The latter type of vector is identified by names such as delta, augment, or contiguous. Vector generators normally are provided with the capability to dash, dot, blink, and change vector brightness levels.
Conic generators produce open or closed curves that are members of the conic family, such as circles, ellipses, and arcs. As with other function generators, numerous techniques exist for implementing conic generators. In some display terminals, a conic generator is not installed, and circles, ellipses, or arcs are developed on the screen using contiguous vectors. The main disadvantage of this technique is that a large number of display instruction words are employed relative to more conventional conic generators. As with vector generators, conic generators usually have the capability, under computer control, to dash, blink, and change conic brightness levels.

Some function generators incorporate automatic brightness compensation by modulating the z-axis as writing speed varies. For example, a vector generator may produce any length vector within a definite time interval; without brightness compensation, shorter vectors are brighter than longer vectors. In the design of some vector generators, no z-intensity modulation is required because the time to generate a vector is proportional to its length.

Sensor Interface and Conversion

The sensor interface receives sensor signals. After appropriately terminating the different signals associated with a sensor, the signals are conditioned before coupling them to the sensor converter. Signal conditioning includes clamping, filtering, level shifting, and amplitude changing.

The sensor converter operates on the signals to produce scanning signals that are coupled to the deflection amplifiers and control the movement of the electron beam over the viewing screen in a structured pattern. A conventional radar presentation employing a radial scan is shown in Fig 6(a). Several techniques are available for generating a radial scan; the net result is negative and positive ramps that are amplitude modulated by a sine function on the x-axis and a similar function phase shifted on the y-axis by 90°. A conventional sonar presentation employing a spiral scan is shown in Fig 6(b). This scan mode is produced by a pair of phase shifted sine functions that are ramp modulated.

A horizontal raster scan is produced by a set of high frequency ramps and a set of low frequency ramps applied to the x and y axes, respectively. A common raster scan pattern is shown in Fig 6(c). A low frequency ramp and an associated high frequency ramp define a field, and two fields define a frame. The two fields, shown as solid and dotted lines in Fig 6(c), are interlaced to prevent flicker and smearing of the associated display imagery. The human eye integrates consecutive fields of interlaced imagery so that motion appears to be continuous while using lower persistence phosphor to reduce motion smearing. Interlacing may not be necessary if the associated imagery is relatively static. A variety of other structured scan formats exists to enhance the presentation of imagery derived from advanced sonar and radar systems.

Timeshared Deflection

The timeshared deflection unit receives three basic inputs: structured scan patterns from the sensor converter; function generator scanning patterns for the generation of conics, vectors, and characters; and an unstructured or random scan [Fig 6(d)].

In random scan, the electron beam is positioned at any point on the viewing screen by applying a signal of constant level to both the x and y axes. "0" levels of the x and y deflection waveforms in Fig 6(d) correspond to the center of the associated CRT presentation. Transient time is the time interval between changes in successive positions on the screen. At a particular random scan position, such as a, b, c, or d in Fig 6(d), a character or vector may be written.

Random scan waveforms are the outputs of two digital to analog converters (DACs). These are located between the display controller and the timeshare deflection module. Digital inputs to the DACs originate from bit fields that define x and y positions in the display instruction words (Fig 7). If the display imagery on the physical screen represents a translation on the
Fig 6 Scanning waveforms. Radial (a), spiral (b), and raster (c) are structured scans providing familiar display presentations for radar, sonar, and television, respectively. Variety of other structured scans exists for display of advanced sensor information. Random scan (d) is used to locate alphanumeric and graphic information on display screen; waveforms (d) represent D-A converted X, Y position bits (Fig 7) after adjustment for transformations, such as range scale change and offset.

virtual screen, the display controller adds a fixed offset to each position bit field as the display instruction words are retrieved from memory. The 15 bits in each X-Y position bit field define a virtual screen; the physical screen may be defined by only 10 bits. Again, which of the 10 adjacent bits are used is determined by the range scale setting. Also, when a display instruction word is retrieved from the display file, the word identification (ID) bit field is used to direct the remaining part of the instruction word to the character, vector, or conic generator.

The function of the timesharing block is to multiplex and sum the various scanning signals. For example, within a refresh cycle, the random scan of Fig 6(d), along with a fraction of the radial scan of Fig 6(a), are time division multiplexed. During that portion of the refresh cycle when the random scan is activated, the function generator sums its inputs [see Fig 5(b)].

Data Entry Devices

Data entry devices enable the operator to rapidly enter data into the display terminal, where they are acted upon by the operational program, resulting in modification or manipulation of the display imagery.

Data entry devices can generally be classified in two categories. First are those that transmit information to the host computer or display processor, such as function and keyboard switches. The second category contains devices, such as a joystick or a trackball, that can be used to point to and select alternatives listed on the display screen for subsequent processing; in some modes of operation, these devices are used in conjunction with function switches. A light pen and
a graphic input tablet can be placed in either category, depending on their mode of operation.

Function switches are usually grouped together. The output of a function switch is a code that is interpreted by software to initiate a logical operational sequence. Function switches range from the simple pushbutton to complex switches containing multimeasure readouts under host computer or display processor control. A matrix of the latter is commonly called an action entry panel; functionally, it is a 3-dimensional matrix of switches. For example, consider a representative hardware/software implementation of an m x n x h size matrix. Let m x n represent the physical array of multilegend illuminated pushbutton switches. Each individual switch in the array can take the place of up to 48 switches. Within each switch is a film chip containing 48 different brief messages. A particular message is selected by activating a miniature back-lighted lamp. Each switch has a single code associated with it which is used to select a message. The third dimension (h) is defined by the software of the operational program. Let level h, define m x n classes of information where each class is differentiated by a brief message. Depressing a function switch results in examination by the operational program of the function switch code and the software description of level h. Responding to operational program instructions, the display processor changes all n x m readout messages. The new messages represent level h1 designating subclasses of the selected class of information. If a function switch is again depressed, another examination by the operational program is initiated. The function switch code and the software description of level h1 are translated as a jump to a service routine. This routine dictates an alphanumeric message to be printed on the CRT containing information pertinent to the selected class/subclass.

The keyboard, generally similar to a typewriter keyboard, has extra keys that enable the operator to perform functions such as edit, backspace, and delete. Adjacent to the keyboard, when emplaced, the joystick is an upright handle, and the trackball a rotatable ball mounted in a hemispherical socket. Movement of either device generates a changing set of x, y coordinates for the operational software. The resulting coordinates are also used to generate an electronic marker or cursor. A light pen, when placed against a bright spot on the CRT screen, detects a pulse of light as the scanning electron beam passes. The resulting pulse can be translated into x, y coordinates at the pen tip. A graphic input tablet consists of a flat area and a stylus. The stylus, which interacts with the tablet to specify x, y coordinates, may function as a passive or active instrument depending on the technology employed in the design of the graphic input tablet.

Display Device

CRT capabilities typically include variable persistence, color, background generation, storage, and symbol generation. Other display devices, such as flat panels, presently lack capabilities and are expensive. Currently, the CRT offers superior capability in displaying a gray scale, color, high quality graphics, background information, and a large number and type of symbols.

Some displays employ penetration CRTs that have multicharacteristic phosphors. These tubes offer either dual persistence or 4-color capability. Both types have different phosphors deposited on the CRT faceplate in thin layers or in an onion skin manner. To excite the various phosphors, the impacting electrons must have different energies, as controlled by the accelerating voltages applied to the anode. Therefore, depending on the particular CRT construction, switching anode voltages provide a single persistence or up to four distinct colors for the second tube type.

With the first or dual-persistence tube type, two colors are present, green for short, and orange for long persistence; however, such displays are not classified as color displays. For example, if all alphanumeric and graphic information appears as a steady green color and radar targets appear as flashes of orange, the display presentation does not have the appearance of a color display.

Both penetration CRT types have significant limitations that have hindered their wide acceptance. Brightness suffers because of inefficient phosphors. To increase brightness, refresh frequency can be increased and writing speed decreased, but this technique reduces the amount of information that can be displayed. If the grid voltage is increased to brighten the display, the spot size grows and degrades the resolution. Other problems include anode power supplies in the kilovolt range that are physically large and power consuming.

A compromise approach to dual persistence with a monochrome CRT involves a phosphor mix that offers a measure of persistence but provides some smearing of moving graphic and alphanumeric information. For example, consider a block of alphanumeric data defining an aircraft in terms of identification, airspeed, and altitude. As the aircraft target and associated block of alphanumeric data move across the screen, the data block leaves a smeared trail while the radar target eventually fades out. Sometimes, radar targets are synthetically generated to render a solid appearing image.

Conventional TV color CRTs with mask structures cannot be used in a tactical display terminal that requires a variety of possible scan modes because of alignment problems between the mask holes and the scanning path of the electron beam.

Display Software

In general, system display terminal software consists of three programs: operating system, language proces-
The operating system is a collection of programs that enables system programmers to efficiently create operational programs. These programs may include monitor, editor, file maintenance, and debugging programs. With the monitor program, the programmer can interface to system hardware and software from a keyboard, using a comprehensive set of English-type commands. An editor allows a programmer to create and modify text or programs. A file maintenance program provides a means to manipulate and maintain programs and data as files. A debugging program assists a programmer in uncovering and correcting program errors.

The language processor relates to high level and/or assembly language programs for translating a source program into machine code. The Navy currently makes extensive use of a high level language called Compiler Monitor System 2 (CMS-2) to perform data processing in tactical display systems. CMS-2, consisting of a blend of languages such as JOVIAL, CS-1, and FORTRAN, is a problem-oriented machine-independent language; yet the programmer can include segments of symbolic machine language, at the sacrifice of some machine independence.

An operational program written for a display terminal dictates the mission of that terminal, and enables the operator to interact with the display system using data entry devices. Hence, display instructions that make up the terminal display file are created by the operational program in response to operator manipulation of the various data entry devices. Other display instructions are created by the operational program in response to other computer or sensor inputs beyond the operator's control.

In an operational ship environment, system software may consist basically of a set of operational programs, each of which is responsive to the specific task assigned to the display terminal. The operating system and language processor components of the system software may be found only at a few display system sites where operational programs are developed. The operation programs in a display system may be resident in the display terminal, host computer, or both, depending on the complexity of the display terminals and display system.

**Future Trends**

There is a trend towards the adoption of displays using a raster scan monitor as in conventional TV. These monitors are reliable, inexpensive, and ideal for changing display information such as TV signals which do not require refreshing. However, part of the information in a tactical display is static and requires refreshing. Combining the monitor with solid state memories provides a fundamental structure for a low cost display terminal. The increase in capability and falling prices of monitors and memories is the principle motivation supporting this combination.

Basic memory is organized as a 2-dimensional matrix of pixels, and is referred to as bit map memory. All but the simplest of these include a third characteristic: a number of bit map levels for encoded gray scale, color, and other information. The conventional display file may no longer exist; all characters and vectors are distributed in bit map memory and are sequentially read out line by line during refresh. Some raster displays may employ memory saving techniques such as a virtual bit map memory, in which the screen is partitioned into a grid of graphic cells, with each made up of a matrix of pixels. A display file contains a list of addresses of those graphic cells that carry information. In a typical picture many graphic cells are empty, thereby permitting a small memory capacity. Graphic cells are accessed much like conventional raster scan character generators.

Future raster display terminals may use dual bit map memories to enhance system capability. Primary use for the second bit map memory is to accept a picture from another source within the display system without destroying the contents of the first bit map memory. The operator can then select contents of the second memory for review. Further uses include casualty backup, auxiliary information storage, scratch pad function, and temporary storage during generation of a hard copy.

Other than memory, increasing interest in raster displays can be credited to advances in microprocessors and LSI character generation. An increasing application of microprocessors in raster displays is in the generation of graphics. Given input parameters, a succession of pixels defining a graphic structure is calculated and loaded into the bit map memory. Input parameters include such things as vector end points, center and radius of circle, and so on. LSI character generator circuitry like that used in commercial alphanumeric displays may be adapted for a text mode of operation; depending on the system philosophy for processing alphanumeric data, there may be no need to provide a separate buffer for alphanumeric information. A line of characters can be processed directly and the resulting video inserted into the bit map memory with other information.

A significant advantage of the raster scan display, relative to the random scan display, is availability of a wide variety of colors and solid area shading or coloring. Color coding of tactical data has long been favored by the military. The additional information furnished by color coding can reduce decision times when a large number of targets is being displayed. Recent progress in the development of the beam-indexing CRT offers the potential for providing high resolution color and less susceptibility to shock and vibration. This CRT uses a single electron gun controlled by electro-optical feedback.

At this time the principle limitation of raster scan versus random scan displays is resolution. The latter
typically operates within a $1024 \times 1024$ matrix. To approach such resolution with a raster scan display means that the number of horizontal lines per frame must be increased beyond the TV standard of 525 to a little over 1024 lines per frame. So, the frequency of the horizontal raster line must be increased from 15 kHz to around 34 kHz. The active horizontal line time is partitioned into 1024 time intervals, each one pixel in "width." To accommodate such high horizontal resolution, some monitors have a video bandwidth up to 40 MHz.

At the system level, the raster scan approach offers capabilities far too complex or expensive to undertake in a random scan system. Some of these capabilities include video recording, frame capture, time compression, and hard copy. Raster scan display information, recorded by conventional video tape machines, is valuable for making measurements of display quality, maintaining display equipment, conducting postmission analyses, evaluating operator performances, and conducting training. Frame capture offers interesting capabilities. For example, a bulk memory of selected captured frames for distribution to remote terminals is of value in managing large amounts of critical information. Time compression of sensor information makes moving target identification easier. Such a system sequentially plays back in real-time the last 30 or so stored scan converted frames, where each frame represents one cycle time of a sensor. (An example of sensor cycle time is the time it takes for a radar antenna to make a complete revolution.) There are more advanced time compression techniques but they are currently proprietary. Hard copies of a selected video frame are possible using various types of hard copy devices. All that is required is connection of a single video cable and a stationary picture source. A selected picture (frame) in a dynamic display presentation can be captured, previewed, and copied from the second of the dual-bit map memories.

Sensor information can still be integrated with alphanumeric and graphic data by generating sensor information in a raster format using solid state scan converters, which overcome problems of calibration, reliability, and conversion time lost during the read mode of single ended tube scan converters. Scan converted sensor video is independent of sensor cycle time. Combining it with the computer generated video in the bit map memory poses no loading problems, i.e., no flicker. Moreover, a multipersistence capability is available if desired. This is accomplished by decrementing pixel intensity periodically at a preset rate throughout the cycle time of the sensor. By changing the preset rate, the persistence can be made variable out to infinity if so desired. Reducing the need for long persistence phosphors for sensor data in raster displays enables the use of brighter and longer life phosphors. Command and control rooms can maintain a higher ambient light.

Conventional TV equipment can be integrated in with a raster scan system with appropriate A-D and D-A conversion as required. Video tape recorder and TV camera video can provide background information in a video presentation. Background video, long sought after by the military, can be mixed with output video from bit map memory. Typical background video might be a map having meteorological patterns, topographical contours, or roads. Background video can also be obtained from film and slides using conventional equipment. Special effect, remote video switching, timebase correctors, processing amplifiers, distribution amplifiers, and TV test equipment are further examples of conventional equipment that can be incorporated into a raster scan display system when appropriate. The use of some of this conventional TV equipment would, however, be incompatible with high resolution ($1024 \times 1024$ lines) raster systems.

Current raster display systems do not employ all of the above capabilities. However, complete integration is highly probable because of increased capability and cost reductions.

**Summary**

This article has discussed the state of the art in military tactical display terminal design. The terminal described must be understood to be an idealized model. Tactical display terminals currently in use are not as complete in every respect as the characterized model, which, in general, portrays what the industry is presently offering to meet military requirements.

For the future, it appears that technological improvements in raster scan display techniques, and cost reductions in the associated hardware, particularly microprocessors and solid state memories, are making raster scan display technology increasingly attractive.

**References**


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Edward Gennettten has had nine years' military display experience including five years at the Naval Ocean Systems Center, two years at Stromberg Data-graphics, and two years at Norden Div United Technologies. He holds BSEE and MSEE degrees from the University of California at Davis.
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CIRCLE 113 ON INQUIRY CARD
LOGIC VARIABLE FORMAT
TECHNIQUES FOR EFFICIENT
PROCESS CONTROL I/O

Software coding schemes to process digital input/output variables minimize program memory and execution time requirements, achieving efficient throughput of a process control system.

Rajiv Bhargava and Anil K. Chandra
Bhabha Atomic Research Centre, Bombay, India

When used for process control, a computer acquires information about the state of process and delivers control signals to alter the state in a desired manner. The composite job to be performed by software comprises scanning the process inputs, generating command outputs based on an analysis of the inputs (performing logic operations), and delivering outputs to the process. Since the process under control runs continuously, the computer has to repeat this operation regularly. Software programs are thus structured to be executed completely in periodic cycles. The duration of these cycles is determined by the maximum period in which the control system must respond to any change in the process parameters.

Hardware/software designs have to be optimized to ensure that control system operations are completed within the allotted time. The time required to process digital inputs and outputs (I/Os) is determined by the format used to represent digital I/O variables. Conventionally, each logic variable is represented by one bit. This method speeds up input acquisition and output delivery, but slows down the software processing of logic inputs as microcomputers seldom provide proper bit manipulation instructions.

An alternative data formatting scheme allocs each logic variable a full byte. Since most microcomputers provide extensive byte processing instructions, this scheme reduces program length and execution time, although larger data memory is required.

A microcomputer acquires signal inputs from a process through a digital input unit (DIU) and delivers control outputs through a digital output unit (DOU). Signal inputs from, and control outputs to, the operator console are routed similarly. Digital I/O data may comprise arithmetic variables, such as shaft encoder outputs, or logic variables, such as relay closures. In most process control systems, the time taken to read inputs and dispatch outputs is much less than the time taken to solve logic equations. The time required for solving logic equations is minimized by choosing a proper format to represent the logic variables.

In the logic equation \( L_K = L_A \cdot L_B \cdot L_C \), the logic variables \( L_A, L_B, \) and \( L_C \) represent the status of process components. Logic variable \( L_K \) represents a control output. Obviously, the hardware solution for this equation requires a 3-input AND gate. In software, either of two algorithms—direct code or branch code—can be used to write a program to solve this equation.

**Direct and Branch Code Schemes**

The branch code scheme, on the other hand, is implemented as:

```
LOAD LA
AND LB
AND LC
STORE LK
```

 `/Fetch LA into accumulator`

`/AND accumulator with LB`

`/AND partial result with LC`

`/Store result in LK`
In this scheme, program execution time is independent of the actual logic state of any operand.

The branch code scheme, on the other hand, is implemented as

\[
\begin{align*}
\text{TEST} & \quad \text{LA} & \quad / \text{Check status of LA} \\
\text{BRZ} & \quad \text{RESET} & \quad / \text{Branch to reset if LA = 0} \\
\text{TEST} & \quad \text{LP} & \quad / \text{Check status of LB} \\
\text{BRZ} & \quad \text{RESET} & \quad / \text{Branch to reset if LB = 0} \\
\text{TEST} & \quad \text{LC} & \quad / \text{Check status of LC} \\
\text{BRZ} & \quad \text{RESET} & \quad / \text{Branch to reset if LC = 0} \\
\text{SET} & \quad \text{LK} & \quad / \text{Make LK = 1} \\
\text{BR} & \quad \text{FURTHER} & \quad / \text{Continue further processing} \\
\text{RESET} & \quad \text{RESET} & \quad / \text{Make LK = 0} \\
\text{FURTHER} & \quad --- & \quad / \text{Code for further processing}
\end{align*}
\]

Here, the state of each input variable is checked in turn. If any variable is false (ie, logic 0 state), output variable LK is reset to false without checking the states of the remaining variables. Output variable LK is set to true (ie, logic 1 state), if none of the input variables is false. Program execution time, in this scheme, depends on the logic states of the operands. The solution of the logic equation is obtained quickly if the first operand tested is false, but it is slow if all the operands have to be tested before effecting the state of the output variable.

Direct code implementation requires the use of LOAD, STORE, AND, OR, NOT, and XOR operations. Most microcomputers provide these as regular instructions for byte length operands, although possibly not for single-bit operands.

Branch code implementation requires the use of TEST LV, SET LV, and RESET LV operations, which are generally not provided in available microcomputers. These operations must be implemented in terms of the instructions available in a given microcomputer.

Eight Variables/Byte Format Scheme

This formatting scheme stores eight logic variables in a byte; ie, one bit is allotted to each logic variable. The true state of a variable is represented by 1 and the false state by 0. This scheme minimizes the time required for data transfers between the microcomputer and the process since it utilizes the entire microcomputer data bus width.

To solve a given equation, it may be necessary to use only a few of the logic variables stored in a particular byte. Most microcomputers, however, do not provide instructions to specify and operate on a particular bit of a word. Thus, the software program has to identify and extract variables relevant to the solution of an equation.

For example, to implement the SET LK operation in an 8085 based microcomputer system, output variable LK must be set to true. LK is stored in a memory location with byte address BA(LK), along with seven other variables. The contents of this location are XXXX LKXXX, the states of the remaining stored variables being immaterial. To identify LK, it is necessary to use a mask—BM(LK)—which in this case is 0000 1000. Thus, the specification of a variable requires a byte address and a byte mask. Operation SET LK is now implemented as

\[
\begin{align*}
\text{LDA} & \quad \text{BA(LK)} & \quad / \text{Load into accumulator the byte} \\
& \quad / \text{containing LK} \\
\text{ORI} & \quad \text{BM(LK)} & \quad / \text{Set to 1 the bit representing LK} \\
\text{STA} & \quad \text{BA(LK)} & \quad / \text{Store modified byte}
\end{align*}
\]

This piece of code occupies eight bytes in memory and takes 33 clock cycles for the 8085 based microcomputer to execute.

Using the branch code scheme, equation \( LK = LA \cdot LB \cdot LC \) is programmed as

\[
\begin{align*}
\text{LDA} & \quad \text{BA(LA)} & \quad / \text{Fetch byte containing} \\
& \quad / \text{LA into accumulator} \\
\text{ANI} & \quad \text{BM(LA)} & \quad / \text{Extract bit representing LA} \\
\text{JZ} & \quad \text{RESET} & \quad / \text{If LA = 0, reset LK} \\
\text{LDA} & \quad \text{BA(LB)} & \quad / \text{Fetch byte containing} \\
& \quad / \text{LB into accumulator} \\
\text{ANI} & \quad \text{BM(LB)} & \quad / \text{Extract bit representing LB} \\
\text{JZ} & \quad \text{RESET} & \quad / \text{If LB = 0, reset LK} \\
\text{LDA} & \quad \text{BA(LC)} & \quad / \text{Fetch byte containing} \\
& \quad / \text{LC into accumulator} \\
\text{ANI} & \quad \text{BM(LC)} & \quad / \text{Extract bit representing LC} \\
\text{JZ} & \quad \text{RESET} & \quad / \text{If LC = 0, reset LK} \\
\text{SET} & \quad \text{LDA} & \quad / \text{If LA = LB = LC = 1,} \\
& \quad / \text{fetch byte containing LK} \\
\text{ORI} & \quad \text{BM(LK)} & \quad / \text{or with mask and set} \\
& \quad / \text{bit representing LK} \\
\text{RESET} & \quad \text{JMP} & \quad / \text{Branch to STORE} \\
\text{LDA} & \quad \text{BA(LK)} & \quad / \text{If LA or LB or LC is false,} \\
& \quad / \text{fetch byte containing LK} \\
& \quad / \text{into accumulator} \\
\text{ANI} & \quad \text{BM(LK)} & \quad / \text{Clear bit representing LK} \\
\text{STORE} & \quad \text{STA} & \quad / \text{Store modified byte} \\
\text{FURTHER} & \quad --- & \quad / \text{Code for further processing}
\end{align*}
\]

In each case, the program extracts the relevant input variable by proper masking, and resets LK if any input variable is false. It sets LK to true if none of the input variables is false. The code for this program occupies 40 bytes in memory. The minimum time for solution of this equation (63 cycles) is achieved if LA is false. The program executes in a maximum time (124 cycles) when all three variables (LA, LB, and LC) are true. On the average, the program executes in 84.2 clock cycles (Table 1). The time taken to solve the logic equation depends on the states of the operands. Assuming a random distribution, the average execution time is obtained as the weighted sum of the execution times for various input combinations. Weight W for an input combination is the probability of that combination’s occurrence. When using the eight variables/byte format, it is not feasible to use the direct code scheme for solving logic equations, as bit-manipulation instructions are not available.

One Variable/Byte Format Scheme

Only one logic variable is stored in each byte of data. In general, any two distinct 8-bit patterns may be chosen to represent true and false states. If the patterns use more than one bit out of the eight for coding the state of the logic variable, the hardware for generating the pattern in DIU and detecting it in DOU...
becomes complex. However, from hardware and software points of view it is immaterial which of the eight bits is chosen for coding and whether true is represented by a logic 1 or 0. For example, the two states may be represented as

True = 0000 0001
False = 0000 0000

The choice of hexadecimal 00 code to represent false leads to easier coding and more understandable programs. However, the use of this format increases the time required for data transfers between the microcomputer and the process. It also requires increased data memory space to store all the variables.

Since each data byte stored in the microcomputer memory now represents only one logic variable, it is not necessary to extract a variable before utilizing it. Thus, a variable is completely specified by a byte address. Operation SET L.K is now implemented as

\[
\text{MVI A,01H} \quad / \text{Load accumulator with code for true}
\]

\[
\text{STA BA(LK)} \quad / \text{Store accumulator in L.K}
\]

This piece of code occupies five bytes in memory and takes 20 clock cycles for the computer to execute.

Using the branch code scheme, the equation \( L.K = L.A \cdot L.B \cdot L.C \) is programmed as

\[
\begin{align*}
\text{LDA BA(LA)} & \quad / \text{Load LA into accumulator} \\
\text{ANA A} & \quad / \text{Set condition codes} \\
\text{JZ STORE} & \quad / \text{Result = LA, if LA = false} \\
\text{LDA BA(LB)} & \quad / \text{If LA = true, then} \\
\text{ANA A} & \quad / \text{Test LB} \\
\text{JZ STORE} & \quad / \text{Result = LB, if LB = false} \\
\text{LDA BA(LC)} & \quad / \text{If LA = LB = true, then} \\
& \quad / \text{result = LC} \\
\text{STORE STA BA(LK)} & \quad / \text{Store result in L.K}
\end{align*}
\]

\text{FURTHER --- ---} \quad / \text{Code for further processing}

In each case, the program obtains the relevant input variable and tests its state. It sets output variable L.K to false if any input variable (L.A, L.B, or L.C) is false. It sets L.K to true if all the input variables are true. The program executes in a minimum time (40 cycles) if L.A is false and a maximum time (74 cycles) if L.A and L.B are both true. On the average, the program executes in 55 cycles. The program occupies 20 bytes in memory.

Using the direct code scheme, the same equation is programmed as

\[
\begin{align*}
\text{LDA BA(LA)} & \quad / \text{Load LA into accumulator} \\
\text{MOV B,A} & \quad / \text{Move contents of accumulator to B register}
\end{align*}
\]

The equation \( L.K = L.A \cdot L.B \cdot L.C \) is programmed as

\[
\begin{align*}
\text{LDA BA(LA)} & \quad / \text{Load LA into accumulator} \\
\text{ANA A} & \quad / \text{Perform AND operation} \\
& \quad / \text{between LA and LB} \\
\text{MOV B,A} & \quad / \text{Move result into B register} \\
\text{LDA BA(LC)} & \quad / \text{Load LC into accumulator} \\
\text{ANA A} & \quad / \text{Perform AND operation} \\
& \quad / \text{between LC and partial result} \\
\text{STA BA(LK)} & \quad / \text{Store result in L.K}
\end{align*}
\]

\text{FURTHER --- ---} \quad / \text{Code for further processing}

In this implementation, the program fetches each variable in turn and performs the desired logic operations directly. The program occupies 16 bytes in memory and executes in 68 cycles regardless of the actual logic states of the input variables.

**Software Comparison**

Table 2 contains a representative list of logic equations encountered in typical process control applications. In this table, LA, LB, LC, LD, LE, and LF are operands, and LK is the result of a logic equation. Variable LK may be fed directly to the process or may be treated as an intermediate variable to be used as an operand in other equations. Similarly, operands LA through LF may be logic inputs representing the states of process

<table>
<thead>
<tr>
<th>TABLE 2</th>
<th>Representative Logic Equations For Process Control System</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) SET L.K</td>
<td>(2) RESET L.K</td>
</tr>
<tr>
<td>(3) TEST L.K</td>
<td>(4) L.K = LA</td>
</tr>
<tr>
<td>(5) L.K = LA</td>
<td>(6) L.K = LA • LB</td>
</tr>
<tr>
<td>(7) L.K = LA • LB • LC</td>
<td>(8) L.K = LA • LB • LC • LD</td>
</tr>
<tr>
<td>(9) L.K = LA + LB • LC</td>
<td>(10) L.K = LA + LB • LC • LD</td>
</tr>
<tr>
<td>(11) L.K = LA • LB + LC</td>
<td>(12) L.K = LA • LB + LC • LD • LE</td>
</tr>
<tr>
<td>(13) L.K = LA • LB + LC • LD • LE</td>
<td>(14) L.K = LA • LB + LC • LD • LE • LF</td>
</tr>
<tr>
<td>(15) L.K = LA + LB • LC + LD • LE • LF</td>
<td>(16) L.K = LA • LB + LC • LD • LE • LF</td>
</tr>
<tr>
<td>(17) L.K = LA • LB + LC • LD • LE • LF</td>
<td>(18) L.K = LA • LB • LC + LD • LE • LF</td>
</tr>
</tbody>
</table>
TABLE 3
Comparison of Three Processing Schemes

<table>
<thead>
<tr>
<th>Equation Number</th>
<th>Eight Variables/Byte (Branch Code)</th>
<th>One Variable/Byte (Direct Code)</th>
<th>One Variable/Byte (Branch Code)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Length</td>
<td>Time in Clock Cycles</td>
<td>Length</td>
</tr>
<tr>
<td></td>
<td>Avg</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>1</td>
<td>8</td>
<td>33</td>
<td>—</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
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</tr>
<tr>
<td>18</td>
<td>64</td>
<td>129</td>
<td>93</td>
</tr>
</tbody>
</table>
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Both parameters—program length and program execution time—are better for the one variable/byte scheme for all equations. Using one variable/byte, the branch code scheme, compared with the direct code scheme, provides faster average execution times (17% less) at the cost of extra program length (21.2% more).

**Hardware Comparison**

The DIU can be implemented to accommodate each of the two format schemes (Fig 1). In this control system, 32 process input signals (I_{31} to I_{0}) are to be multiplexed onto the 8-bit data bus. In the one variable/byte scheme [Fig 1(a)], the 11 most significant bits (MSBs) of the address bus (A_{15} to A_{5}) are decoded to identify the module. The remaining five bits (A_{4} to A_{0}) are decoded to choose a particular process signal and to place its status on the data bus. Consider the case when it is necessary to acquire the status of signal I_{15}. Signal I_{15} is wired to address 1111 0000 0000 1111. The microcomputer places this address on the address bus and also forces the IO/M line to zero, indicating that this is a memory address. The status of signal I_{15} appears at the output of multiplexer block A. After a proper delay, the microcomputer issues a read pulse (RD) which causes the status of I_{15} to appear at line D_{0} of the data bus; the microcomputer reads this status into the accumulator.

In the eight variables/byte scheme [Fig 1(b)], 14 address bits (A_{15} to A_{2}) are decoded to identify the module. The remaining two bits (A_{1} and A_{0}) are decoded to choose a particular group of eight process signals and to place their status on the data bus. For example,
if it is necessary to acquire signal I₁₅ in this design scheme, the microcomputer sends out the relevant address (1111 0000 0000 0011) on the address bus and forces the IO/Ӣ line to zero. After a delay, the microcomputer sends the WR pulse. The byte containing I₁₅ is read into the microcomputer, and the software program can then extract I₁₅ to examine its status.

The DOU can be similarly implemented (Fig 2). In this control system, the state of any of 32 process outputs (O₀ to O₃) is to be controlled. In the one variable/byte scheme [Fig 2(a)], the 11 most significant address bits (A₁₅ to A₅) are decoded to identify the module. The remaining five bits (A₄ to A₀) are decoded to enable the relevant gate input (Gₙ) according to the particular output intended to be controlled. The status of the selected output is effected corresponding to the data on the least significant bit (LSB) — D₀ — of the microcomputer data bus. Consider an example where it is necessary to set output O₃ to a logic 1 state. Output O₃ is wired to address 1111 0000 0000 1111. The microcomputer places this address on the address bus and places a one on the D₀ line of the data bus. It forces the IO/Ӣ line to zero, and after a proper delay, issues a write (WR) pulse. This pulse is routed to the clock inputs of all DM 8613 latches. However, only gate input G₃ corresponding to output O₃—in block A—is enabled because of the decoding function performed by 74154. Accordingly, O₃ is set to one, without any of the remaining outputs being affected.

In the eight variables/byte scheme [Fig 2(b)], the WR pulse effects the status of eight outputs at a time according to the data on the data bus. Fourteen address bits (A₁₅ to A₂) are decoded to identify the
module. The remaining two bits ($A_1$ and $A_0$) are demultiplexed into four outputs and these outputs are used to route the WR pulse to the relevant eight outputs being controlled. Consider, for example, that outputs $O_7$ through $O_0$ are to be controlled according to pattern 1100 1010. Outputs $O_7$ through $O_0$ are wired to address 1111 0000 0000 0000. The microcomputer places this address on the address bus and the control pattern on the data bus ($D_7$ to $D_0$). Next, it enables the IO/MI line and then issues a WR pulse after a delay. The WR pulse causes outputs $O_7$ through $O_0$ to be set according to the data pattern on the data bus. No significant difference exists in the extent of hardware required to implement DIU and DOU in either formatting scheme.

**Additional Considerations**

Before commencement of processing logic equations, the software program has to first acquire input variables from the process. After completion of logic processing, the program has to dispatch the output variables to the process. This necessitates consideration of several additional system design factors, such as mapping mode, frozen I/O, and change based inputs schemes.

Acquisition and delivery of I/O variables can be conducted by mapping the relevant hardware units.
in either 1/0 space or memory space. Memory mapped 1/0 transactions are faster, and relevant programs occupy less space in memory.

An input variable may often be required in the solution of more than one equation. During the course of a particular cycle, an input variable should present the same status to each relevant equation. It is thus necessary for the software program to freeze (hold) the status of the process inputs at the start of a computation cycle. This holding is done by scanning the inputs and storing them in memory. However, it is seldom necessary to synchronize the dispatch of outputs to the process. The resulting solution of a logic equation can thus be delivered directly to the process, eliminating the necessity of a separate program for dispatching outputs. Dispatching is incorporated in a distributed manner in the logic equation solution programs.

A controlled process generally demands attention only when any of its parameters undergo a change. Typically, the number of inputs changing per cycle is small. In such cases, it is much faster to check for a change in a group of inputs and update only the changed inputs in one variable/byte format than to scan each input individually in this format.

In change based inputs scheme, the status of inputs is stored in both one variable/byte and eight variables/byte formats. In a particular computation cycle, the inputs from the process are scanned in groups of eight and compared against their status of the previous cycle stored in eight variables/byte format. If a change is detected, the state of corresponding variables in both formats is changed. Variables stored in one variable/byte format are utilized in solution of logic equations. Thus, this scheme exploits both formatting schemes in an advantageous way.

Application Example

As a typical application example, Table 4 shows the distribution of each type of equation in an actual process control application. A total of 216 output variables are determined by the solution of 258 equations containing 185 input variables. These variables also include the 1/0 and processing for the operator console. It is necessary to freeze the input status at the commencement of the computation cycle. The output delivery, however, does not need to be synchronized and the digital 1/0 units are memory mapped. Average number of inputs changing state in one computation cycle is less than one.

Tables 5 and 6 compare the total memory—sum of all program lengths and data memory—and execution time requirements, respectively, for various implementations of this application example. The processing schemes considered are eight variables/byte format with branch code, one variable/byte format with direct code, and one variable/byte format with branch code. Input scanning schemes are straight inputs and change based inputs. Choice of input scanning scheme has little effect on memory requirements, but the change based input scheme requires much less time to execute than the straight input scheme. Using one variable/

byte instead of eight variables/byte format reduces overall memory requirements by 50 to 60% and, in conjunction with change based inputs scheme, reduces total time for one computation cycle by 25 to 37%.

Summary

A process control system must be designed to respond promptly to any changes in process parameters. If only logic parameters are considered, the required processing time depends on which of two possible formats is chosen to represent the logic variables. If only one variable instead of eight is stored in a full byte, there is an increase in the length of data memory as well as the time required to acquire the state of all variables from the process. However, there is a significant saving in the length of program memory and the time of program execution—sufficient to compensate for the larger data memory needed and the longer time required for scanning inputs.

Often, a large number of process parameters are represented by arithmetic variables. It is desirable that identical digital 1/0 units be used for transfers of arithmetic as well as logic variables. It is wasteful, however, to read an 8-bit arithmetic number one bit at a time; this number is best read as an integral byte. One solution is to read all digital variables as bytes; i.e., arithmetic variables are read as a full 8-bit number/byte and logic variables as eight/byte. Software programs utilize arithmetic variables directly, and convert and store the logic variables as one/byte in memory.

This strategy also works well when systems are based on the change based inputs scheme. In this scheme, the software program reads logic variables as eight/byte, checks for a change against the previous stored status, and effects change in the one variable/byte table only if a change is detected. The latter scheme is the most efficient.

Acknowledgements

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Working as a scientific officer in the Reactor Control Div of the Bhabha Atomic Research Centre, Rajiv Bhargava has handled system design and software development of both computer based data logger systems and an operator training simulator for nuclear power plants. He holds a BS degree in physics from Meerut University and an MS degree in mathematics from Bombay University.

Anil Chandra also serves as a scientific officer in Bhabha Atomic Research Centre's Reactor Control Div. He has performed system design and hardware development for nuclear power plant computer based control systems. His Bachelor of Technology in electrical engineering is from the Indian Institute of Technology, Delhi.
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Programmable Timer Provides Accurate Interval Measurements

With minimal hardware parts and software overhead, monitor design measures each time interval of recurring beat-to-beat event sequences independently, rather than as average of longer time interval.

Fred H. Carlin and James A. Howard  
University of California, Santa Barbara, California

A common equipment approach for monitoring repetitive events uses a counter that accumulates the number of events over a known time or base period. The advantages of this approach are simplified hardware and straightforward software, but since the total number of counts received during the base period is usually specified as ±1 count for most available systems, measurement accuracy, as well as hidden abnormalities detection, may compromise critical applications.

This 8253 programmable interval timer\textsuperscript{1,2} is designed into a double buffer counter system. The highly accurate monitor system requires only two chips, exclusive of address selection logic. Software overhead is minimized since this counting system executes an interrupt service routine prior to the occurrence of each event. The counting system is readily assigned tasks of counting events with both slow and fast repetition rates. Applications include monitoring of cardiac and respiratory rates and other frequency encoded data such as neurological activities.

**Hardware Principles**

In the Figure the 8253 timer, comprising three independent 16-bit counter/dividers,\textsuperscript{3,4} data buffer, control word register, read/write logic, and internal bus, is interfaced to an 8080/8085 microcomputer bus by a 7474 flipflop. The control word register stores the constants used to specify the operation of each counter/divider. The data buffer links the internal bus and the microcomputer 8-bit data bus. Read/write logic supervises the flow of data on the internal bus and through the data buffer.

Not shown in the Figure is the address selection logic since, in small systems, a bit selection scheme may be employed, thus eliminating the need for this logic. Bit selection is accomplished by assigning each chip select (CS) line to its own bit in the address selection byte. In the Figure, CS would be tied to an address line, e.g., AB3. To select the timer chip, the address would be 111101xx. The lower two address bits (xx) specify inputs to the read/write logic. Bit 3 (marked by a 0) specifies the timer. Bits 7 through 4 and bit 2 are filled with 1s since each of these may specify another device or chip.

Used as a divider, timer A pro-
vides a primary count frequency to timers B and C. The frequency source to timer A is typically the system clock. If a system clock frequency of 3.072 MHz is used (e.g., in an 8085 microcomputer system), frequencies as low as 25 Hz may be obtained by division. The external divide-by-two 7474 flipflop is required because the maximum counting rate of the 8253 timer is about 2.6 MHz.

Timers B and C utilize the output from timer A to accumulate counts between events. Timer A may be programmed to provide a wide range of frequency outputs, hence a corresponding range of resolving power. If, for example, timer A is programmed to provide a frequency of 1 MHz, events with a period of up to 65,536 µs could be measured with ±1-µs accuracy. If, on the other hand, timer A is programmed to provide a frequency of 25 Hz, events with a base period of up to about 43 min (65,536 x 0.04 s) could be measured with an accuracy of ±40 ms.

The counting system is designed so that either the B or C timer is active, at any one time. The event input line toggles the 7474 flipflop which, in turn, stops the currently active timer and activates the currently dormant timer. The latter begins counting the frequency provided by timer A. Simultaneously, the counter that has just been stopped generates an interrupt. The interrupt is the signal for the microprocessor to read the timer and reset it to zero, thus reinitializing it for the next count interval.

Spurious signals that may be encountered could grossly upset any

---

**PROGRAM 1**

**Initialization Routine**

| INIT:   | MVI A,36H | :GET MODE CONTROL WORD  
|---------|-----------| :FOR TIMER A  
| OUT     | OF7H      | :OUTPUT TO TIMER A  
| MVI A,70H | :GET MODE CONTROL WORD  
| OUT     | OF7H      | :OUTPUT TO TIMER B  
| MVI A,0BOH | :GET MODE CONTROL WORD  
| OUT     | OF7H      | :OUTPUT TO TIMER C  
| MVI A,0 | :LOAD DIVISION CONSTANT  
| OUT     | OF4H      | :LSB TO TIMER A  
| MVI A,8 | :GET MSB OF DIVISION  
| OUT     | OF4H      | :MSB TO TIMER A  
| MVI A,0 | :GET A ZERO  
| OUT     | OF5H      | :ZERO COUNTERS B AND C  
| OUT     | OF5H      |  
| OUT     | OF6H      |  
| RET     | :RETURN TO CALLING ROUTINE  

**PROGRAM 2**

**Interrupt Service Routine**

| INTO:   | PUSH H | :SAVE H.L. REGISTERS  
|---------|--------| :SAVE ACCUMULATOR AND  
|         | PUSH PSW | :FLAGS  
|         | LHLD .TBL | :GET ADDRESS OF TABLE  
|         |         | :INTO H.L  
| MVI A,70H | :GET MODE WORD  
| INX     | OF7H | :OUTPUT TO TIMER  
| INX     |  
| IN     | OF5H | :GET FIRST BYTE OF COUNT  
| MOV M,A | :STORE IN MEMORY  
| INX     | H | :BUMP H.L  
| IN     | OF5H | :GET SECOND BYTE  
| MOV M,A | :STORE IN MEMORY  
| SHLD .TBL | :PUT POINTER TO TABLE  
|         |         | :BACK  
| MVI A,0 | :GET A ZERO  
| OUT     | OF5H | :ZERO COUNTER  
| OUT     | OF5H |  
| POP H | :RESTORE H.L  
| POP PSW | :RESTORE ACCUMULATOR  
|         |         | :AND FLAGS  
| EI     | :RENEABLE INTERRUPTS  
| RET     | :RETURN  

Note: Calling routine must enable interrupts
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accumulated counts. In practice, these signals are optimally filtered out by the transducer and related electronics. If, however, only the majority of disturbances is eliminated, sufficient capability remains in the counting system design to discern these abnormal counts by software means. The system design described allows more microprocessor time to be devoted to detection and correction. Schemes using the measurement of the total number of counts over a given time period (eg, 10 s) are disadvantageous since an extra count or two during the collection period would be detected simply as an increased rather than an abnormal rate.

Software Principles
Basic software requirements that must be accomplished are (a) initialization of the timer chip, whereby the chip is specified as a divider and two counters, (b) loading of the divider with a division constant, and (c) collection of beat-to-beat data under interrupt control. Initialization is accomplished by a short sequence that sets up timer A as a simple frequency divider and timers B and C as simple counters. Divider A is loaded with an appropriate divisor to obtain a frequency that has a period equal to or less than the resolution desired. Upon the enabling of interrupts, beat-to-beat data are collected.

At reception of each interrupt, the corresponding counter is read and the contents are reset to zero, thus readying the counter for the next count period. Time available for servicing the interrupt is up to the full period of the incoming waveform. Data outputs are direct measures of the length of the intrabeat periods.

Program 1 gets and stores control words and initialization constants for each of the three timers. The 16-bit division constant for timer A is also loaded, and the B and C timers are set to zero. The calling routine is expected to set up and enable interrupts.

The interrupt service routine reads timer B and places the result in table TBL. Pointer to table is updated and timer B is reset to zero. A similar routine is required for timer C. The technique of placing collected data in a table is not mandatory. The resulting short routine enables the microprocessor to service the beat-to-beat timer in about 100 µs; the processor is then free to perform other processing chores during the remaining time. The resulting numbers stored in table TBL are a measure of the beat-to-beat intervals. With a system clock frequency of 3.072 MHz, the sample program produces counts in 1-ms increments for each beat period. Since the maximum count of the B or C timer is 65,536, the maximum interval that may be measured is 65.536 s which is sufficient to cover all heart rates.

Summary
The monitor design gathers event-to-event timing data with minimal hardware and software overhead. Hardware minimization saves cost and space, especially if several such counters are to be included in a packaged system. Minimal software requirements are paramount in applications where repetitive events occur rapidly, for example, in the investigation of neural activity. Time intervals are measured separately and independently, giving accurate measurements even if events have a wide variation from beat-to-beat.

References
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Optical Link Design and Component Selection

Careful selection of light source, detector, optical modems, couplers, and optical cable enable single-fiber half-duplex link between remote and local coaxial connected key station systems

Norman Goldberg and J. A. Eibner
Sperry Univac, Blue Bell, Pennsylvania

An optical data link for connecting five computer-aided data entry key stations to a processor has been designed, built, and tested (Fig 1). The resulting system accepts keyboard-entered source data from a maximum of 32 operator keystations and produces validated data records for mainframe processing. System requirements included a data link length of up to 1.6 km, operation at $10^6$ baud, a signal-to-noise ratio corresponding to a bit error rate of less than $10^{-15}$, and half-duplex data transmission. A single fiber optic cable was selected for the link interface because it offered many advantages over coaxial cable, i.e., low transmission losses, immunity to electromagnetic interference, and freedom from noise and pickup problems associated with ground loops.

Moreover, an optical cable is smaller, weighs less, and is more secure. Various combinations of optical, mechanical, and electronic components were investigated to achieve the desired performance level.

Component Selection

Lens System
Since the data link for computer-aided data entry (CADE) operates in a half-duplex mode, data terminals can be interconnected by a single

Fig 1 Block diagram of CADE system installation. Optical modem connects optical cable to previously installed coax cable, which connects four key stations to processor. Five additional key stations are connected at other end of optical cable via second optical modem.
fiber cable. This adds the complication of a T-coupler at each end of the optical cable, but the significant cost saving of 1.6 km of fiber made the complication acceptable. Each T-coupler couples light from a light emitting diode (LED) source into the cable and from the cable to a detector (Fig 2). A dielectric beam splitter divides the incident light into a reflected and a transmitted beam. Lenses project the LED radiation onto the cable end and radiation from the cable end onto the detector.

Focal length of the source lens had to be on the order of 5 mm to keep the T-coupler compact and still have space enough to insert a beam splitter between the lens and the cable. An f-number as low as 0.5 was desirable so that a large fraction of radiation from the LED source would be projected onto the cable end. Low cost aspheric lenses, which also have little spherical aberration, are ideally suited for this application. They are somewhat astigmatic, but this does not significantly affect the radiant power inserted into the cable. A pair of identical aspherical lenses with their aspheric surfaces in contact is used for the source lens. The individual lenses each have a focal length of 8.5 mm and a diameter of 12 mm.

The combination (or symmetric doublet) has a focal length of 5.0 mm and an f-number of 0.5.

In the fiber input coupler (Fig 3), the radiation emitted by the LED source of diameter d₁ at an angle θ₁ is focused to an image of diameter d₂ = M₀ d₁ and makes an angle θ₂ = θ₁/M₀ at the image position. M₀ is the magnification and the angles are assumed to be small, i.e., θ = sin θ. If the f-number of the lens is small enough to collect all radiation emitted up to the angle θ₀, the lens increases the acceptance angle by a factor of M₀, and therefore the solid angle coupled into the fiber, which is proportional to the square of the acceptance angle, is increased by a factor of M₀². If source and image diameters are both larger than fiber diameter, which is true in this application, the fraction of the source radiation projected onto the fiber is reduced by a factor of M₀². As a result, the radiation coupled with the lens is the same as the radiation coupled by direct butting of the LED against the fiber, except for losses due to reflections at the four surfaces of the lens doublet.

In testing the lens doublet operation, 175 µW were coupled into the fiber, and 205 µW were coupled by butting the same LED source directly to the fiber. The reduction in power is in agreement with the losses expected by reflections from the lens. In the source lens system, magnification is 1.7 and the image of the source is appreciably larger than the fiber core. This arrangement is relatively insensitive to small displacement of LED, lens, or fiber. Up to 100-µm displacement of the fiber in any direction reduces the power coupled into it by less than 10%.

The detector lens system focuses the fiber core onto the detector, whose active area diameter is 0.76 mm — three times larger than the fiber core. A pair of identical plano-convex lenses with the convex vertices in contact are used for this lens system. The individual lenses have a focal length of 8.1 mm and a diameter of 4.3 mm. The combination has a focal length of 4.1 mm, and an f-number of 1.0. In the detector lens system, magnification of the lens is 2.2, and the numerical aperture (NA, the sine of one-half the acceptance angle) of the lens is 0.4. Since this NA is larger than the NA of the cable (see Optical Cable section) and the image of the fiber core is smaller than the active area of the detector, all the light from the fiber reaches the detector except for reflection losses at the lens and detector surfaces.

**LED vs Injection Laser**

It was determined that system requirements could be met with an LED source or an injection laser. The LED was chosen because injection lasers are expensive, require either precise temperature control or a feedback system to keep the power level constant, and have shorter lifetimes.

**Optical Cable**

Power that can be coupled into a fiber from an LED source is on the order of −10 dBm (power in dB relative to 1 mW). A minimum loss of 6 dB is introduced by the beam splitters used in the T-coupler. Average power required to achieve a signal-to-noise ratio corresponding to a bit error rate (BER) of 10⁻¹⁵ at 1 MHz with an avalanche photodiode (APD) and the system preamplifier is about −60 dBm. Therefore, loss in the fiber cable must
be less than 44 dB (60 - 10 - 6 dB), or 27 dB/km for a 1.6-km link length. Thus, a relatively low loss cable is required. A plastic covered silica fiber (PC-10), which costs less than glass-on-glass fiber, meets this requirement. Its specifications are optical attenuation of <20 dB/km at a wavelength of 800 nm, steady-state 3-dB numerical aperture of 0.22, and core diameter of 250 μm. Actual measurements determined that the attenuation of the 1.6-km cable is 16.8 dB/km at 800 nm and the steady-state 3-dB NA is 0.12. NA is below specification, which adds about 5 dB power loss. This loss is almost recovered in the 1.6-km cable by the lower than specified attenuation.

Several tradeoffs were considered in selecting PC-10 fiber. Important positive factors were its low cost and large core diameter. The latter increases the insertion power of low cost LEDs, which are all large. When low cost small LEDs become available, large core area will be of less importance.

Negative tradeoffs concerned the effect of a humid environment and the difficulty of bonding a connector to the silicone cladding. No degradation of optical properties was observed in a 60-m test length after being submerged in water for 38 days, nor in a 900-m test length after six months in a usually flooded underground duct. Similar results have been reported for longer test periods. The bonding problem is still not completely solved, but bonding is satisfactory for long cable lengths where the stress at the fiber connector bond is not as large as it is in short cables.

**LED Source**
The selected radiation source is an HP-20 LED with a wavelength of 800 nm, which is close to the minimum attenuation wavelength of PC-10. Optical power of the diode with a current of 200 mA is 20 mW. The hemispherically-shaped LED source has a diameter of 460 μm. Intensity of radiation is essentially constant over an angle of ±40° from the optical axis.

**Optical Detector**
The selected TIED 38 optical detector circuit consists of a silicon APD and a reference diode. Breakdown voltages and temperature coefficients of the diodes are closely matched. The reference diode is used in a temperature compensating bias circuit that holds the avalanche gain of 100 constant over wide temperature variations. Active area of the APD has a diameter of 750 μm.

**Data Recovery**
Format for the transmitted data was determined by the existing data entry system in which the optical link is used. Data are transmitted in asynchronous start-stop nonreturn to zero (NRZ) format in half-duplex mode at a modulation rate of 10⁸ baud. The system uses a polling protocol, ie, the central processor sequentially polls the key stations, and a key station can transmit only after it has been polled. System design allows for a response to be generated as early as 2 μs after an incoming signal is completed. Because the optical link will be used only for distances greater than 2000 ft (610 m), it will take at least 8 μs for a response to be received after a transmission is completed.

These system considerations imposed restrictions on the data recovery scheme. First, the receiver must function with arbitrary data patterns, including long strings of Os and 1s. Second, transients caused by saturation of the receiver due to scattered light from the transmitter at the same end had to decay in less than 8 μs. Finally, decision-making logic was required to determine the direction of transmission and disable the transmitter or receiver to prevent interference.

The preamplifier is a simple 2-stage, bipolar transimpedance circuit. Predominant noise contributors are shot noise in the first transistor’s base junction, which is proportional to the base current, and thermal noise in the feedback resistor (Rf). Base current is inversely proportional to the collector resistor (Rc). Thermal noise is inversely proportional to Rf; thus, by increasing Rc and Rf, noise spectral density can be reduced. Bandwidth (BW) is limited by the detector’s capacitance and the amplifier’s input resistance, which is proportional to Rf. Similarly, the first transistor’s collector capacitance and Rc can also limit bandwidth. Therefore, by increasing Rc and Rf, bandwidth is reduced. By careful design, noise can be reduced in direct proportion to BW rather than by √BW, which might have been expected. Measured results for the preamplifier with PIN detectors over the range of 0.3 to 30 MHz show the predicted linearity. The noise equivalent power (NEP) at 1 MHz is 1 nW (−60 dBm). An additional 10-dB improvement is obtainable with an APD.

The NEP of the APD and amplifier is 0.11 nW (−70 dBm). To achieve a BER of 10⁻¹⁵, the peak-
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to-peak signal to rms noise ratio must be 15.9 if the noise is assumed to be Gaussian. Therefore, required power is 1.7 nW or -58 dBm. A more sophisticated amplifier circuit could result in even lower input power requirement. Data recovery is accomplished by differentiating the preamplifier output, amplifying the differentiated signal, detecting positive and negative pulses, and using them to set and reset a flip-flop (Fig 4). This scheme allows for recovery of all NRZ data patterns with ac coupling between gain stages. The ac coupling time constant can be very short, preventing long recovery times when the receiver is overdriven.

System Results
In a prototype system, the LED source with drive current of 100 mA emitted 10 dBm. Coupling loss into the fiber was 21.5 dB. Loss in 1.6 km of cable was 26.9 dB (16.8 dB/km); the two beam splitters added another 6.2 dB loss, and detector coupler loss was 1.4 dB, with resulting input power to detector of -46 dBm (25 nW). Allowing for a time degradation of 3 dB and an additional 3 dB for degradation of LED and receiver sensitivity by temperature variation, the system was estimated to have an excess power of 6 dB.

After a successful system checkout with a fiber cable on a reel, the cable was installed on site. The fiber optic cable length was actually 3200 ft (975 m) and was connected by an optical modem to a previously installed 3300 ft (1006 m) of coaxial cable, which runs to the Cade processor. Coaxial cable also connects four local Cade key stations to the processor. The other end of the fiber optic cable is connected via a second optical modem to five remote Cade key stations (Fig 1). The optical cable runs through manholes, under a bridge, and through a subway tunnel. New cable procured for this installation had an attenuation of 9 dB/km. Two cable breaks occurred, one during the pulling of the cable and the second a month later. In both cases, unplanned splices were made by terminating the broken ends with available connectors and joining the connectors with coupling fittings. These splices introduced an excess loss of 12.5 dB. However, this loss was offset by the lower loss of the new cable. The total cable loss is 24 dB, which is less than the 26.9 dB loss of the cable in the prototype system. Except for fiber breaks because the cabling is not tough enough for the harsh manhole environment, the system has operated reliably. Preliminary results with a more rugged replacement cable promise to correct the breakage problem.

Acknowledgement
The assistance of Mr Richard Lawrence in the design and construction of the electronic portion of the system is gratefully acknowledged.

References
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CIRCLE 120 ON INQUIRY CARD
Microcomputers can be interfaced to 7-segment displays by a number of means. Two methods, discussed in Part 1 (Computer Design, Apr 1979, p 128), are latching and multiplexing—usually used only with multi-digit displays. Alternatives to these are provided by software techniques.

When the microprocessor constantly updates the light emitting diode (LED) display (with digit enable codes and data values output to the display every millisecond), the microcomputer is unfortunately tied up so that it cannot perform any other tasks. The Program For 10-Digit Number Displayed on Multiplexed LED (contained in Part 1, Apr 1979, p 136) could, of course, be converted to a subroutine. If it is called every 15 or 20 ms, the 10-digit number will still be displayed at a reasonably fast rate. However, it may be difficult to program the microcomputer so that the DISPLAY subroutine is called this often.

An interrupt can solve this problem. Whenever the 8080 microprocessor is interrupted, it outputs a numeric value to the next consecutive digit in the display. The microcomputer has to be interrupted at least 400 times every second for the display not to “flicker.” Therefore, the 10-digit number will be displayed 40 times every second. To interrupt the microprocessor so that it “services” the display this often, a low frequency oscillator (400 Hz) can be wired to one of the interrupt interfaces previously discussed. 1,2

The program that services the interrupt and outputs a new 8-bit value to the display interface is similar to the software used in Fig 2 (see Part 1, Apr 1979, p 132); however, because of its length, the listing has not been included. The difference between the two programs is that the microprocessor has to store the digit enable code and the address of the memory location that contains the next digit to be displayed. These values must be stored in memory, because register pair H and register D may be used by the interrupted program. Therefore, each time the oscillator interrupts the microcomputer, it has to read from memory the address for the next digit to be displayed and its corresponding digit enable code. After the number is displayed, the digit enable code and memory address are incremented and stored back in memory. To simplify this software, the 10-digit number can be stored in 10 memory locations, one digit per memory location, rather than “packing” the binary coded decimal (BCD) data.

This interface, however, is limited by the ns8857 to display the numbers 0 through 9; it cannot display the letters A through F, which are needed for hexadecimal numbers or message codes such as HELP or Error. To do this, the ns8857 must be replaced by a device that can drive any combination of individual segments. The UDN-2981A (Sprague Electric Co) contains eight individual drivers for use in the display interface. This device has eight inputs and eight outputs, with each input interfaced to an individual data bus line by means of a latch circuit and each output wired through a current-limiting resistor to one segment input of the display (A to G). If desired, the last driver in the integrated circuit (IC) can drive the decimal point in the display. Since the UDN-2981A has eight inputs, an 8-bit output

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CIRCLE 121 ON INQUIRY CARD
Lookup Table For Multiplexed LED Display

/This program drives a 10-digit, multiplexed, 7-segment display. A lookup table is used to convert BCD numbers to appropriate 7-segment code.

DISPLA, LXIH /Load register pair H with memory
120 /address where BCD digits are stored
004 /004 120 = hex 0450
MVID /Load D with first digit
000 /that will be enabled

DISPL1, CALL /Display first two packed
DIGIT /BCD digits
0
INXH /Increment memory address
MOVAD /Get digit enable word into A
CPI /Compare it to
012 /eleventh digit enable count
JNZ /Haven't displayed all 10
DISPL1 /digits yet, so do two more
0
JMP /Have displayed all 10 digits,
DISPLA /so display them all again
0

DIGIT, MOVAM /Get packed BCD word into A
CALL /Then use lookup table to
OUTIT /determine proper sequence
0 /of ones and zeroes
MOVAM /Get same word again
RLC /Rotate four MSBs into
RLC /four LSBs
RLC

OUTIT, ANI /Save only four LSBs
017 /(017 = hex 0F)
PUSHH /Save register pair H on stack
LXIH /Load register pair H with
BINSS /base address of lookup table
0
ADDL /Add LO address to the number in A
MOVLA /Save the result in register L

JNC /There is no carry, so leave the
OKASIS /content of register H alone
INR /Increment register H by one
OKASIS, MVIA /Output an invalid digit enable code
377 /so that display is blanked
OUT
125
MOVAM
POPH /POP register pair H off of stack
OUT
128
MOVAD
OUT
125
INRD
INTENS, MVIE /Increment digit enable
200 /Load E with a number
200 = hex 80 = decimal 128
INTEN1, DCRE /Decrement the number
JNZ /If it is nonzero, execute
INRD
INTEN1
0
RET /When E = 0, return

008 /7-segment code for 0
009 /7-segment code for 1
133 /7-segment code for 2
117 /7-segment code for 3
146 /7-segment code for 4
155 /7-segment code for 5
174 /7-segment code for 6
007 /7-segment code for 7
177 /7-segment code for 8
147 /7-segment code for 9
000 /7-segment code for 10
000 /7-segment code for 11
000 /7-segment code for 12
000 /7-segment code for 13
000 /7-segment code for 14
000 /7-segment code for 15

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port (latch) will have to be used to interface it to the microcomputer. This means that one output port will be used to output the sequence of ones and zeroes that specify the sequence of segments to be turned on or off. A 4-bit output port allows the digit enable code to be output and stored in the interface.

A recent column discussed lookup tables and their application in converting BCD numbers to 7-segment codes. The Lookup Table For Multiplexed LED Display (see program listing) accomplishes this. The first difference between this program and the one displayed in Part 1 can be seen at `DIGIT`. After the packed BCD word is moved from memory to register A, the `OUTIT` subroutine is called. This means that the first BCD digit to be displayed is in bits D3 through D0 of the A register. At `OUTIT`, bits D7 through D4 of the A register are set to zero. The content of register pair H is then saved on the stack and the pair is loaded with the base address of the lookup table. The BCD number in the A register is added to this address. MVIA and OUT instructions at `OKASIS` cause the display to be blanked by writing an invalid digit enable code out to the display interface. While the display is blanked, the microprocessor moves the bit pattern for the number to be displayed from memory to the A register (MOVAM). Register pair H is then popped off of the stack and the 7-segment bit pattern is output to port 126. Register A is then loaded with the digit enable code, which is output to port 125. Execution of the `OUT125` instruction turns on the specified digit in the display. The microprocessor executes an intensifying time delay loop before returning to the MOVAM instruction just after `DIGIT`. `MOVAM` loads the A register with the same packed BCD word that contained the previously displayed digit.

However, the BCD digit in bits D7 through D4 must now be displayed. Therefore, bits D7 through D4 are rotated into bits D3 through D0 of register A before the 8080 executes the instructions at `OUTIT` that cause the required bit pattern for the 7-segment display to be fetched from the lookup table. The bit pattern, followed by a digit enable code, is then output to the interface. The remaining instructions in the two programs are the same.

An additional display method is the use of an external display controller IC with the multiplexed display. Intel Corp manufactures a number of these ICs—compatible with the 4004/4040, 8080, and 8085. These are the 4269, 8279, and 8279-5. National Semiconductor Corp also has two display controller ICs for use with 8-digit displays. One of the devices (MM74C912) displays 0 to 9 and the other (MM74C917) displays hexadecimal numbers. Ref 4 suggests additional hardware and software information on multiplexed LED displays.

References

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To complement the MP/100 and MP/200, Data General Corp, Rt 9, Westboro, MA 01581, has introduced an array of packaging comprised of a 4-slot card cage for OEM mounting, half-bay cabinets, and a 5.25 x 14” (13.34 x 36-cm) 8-slot chassis. Packaging accessories include card frames, extender cards, power supplies, and cables.

Software support for the families under DOS and RTOS are Extended BASIC, Business BASIC, FORTRAN IV, and DG/L structured programming language. Communications and sensor I/O utilities, communications software emulation packages, and support utilities are supplied.

A line of communications, sensor I/O, and terminal interfaces, as well as micronova peripherals are compatible with the family. The microprocessor is priced at $56.10 (100 quantity). For packaged systems with 64k bytes of memory, the MP/100 costs $2800 and the MP/200 is $3700 in single quantity. Various priced configurations are offered.

Circle 330 on Inquiry Card

**Powerful Microcomputers Offer Functionality of Minicomputers**

Small board size and high component density of the LSI-11/23 microcomputers allow their use as building blocks for complex instrument builders or as central elements of special business oriented systems. With the hardware functionality and software compatibility of a midrange minicomputer, the microcomputer consists of only two 5.2 x 8.9” (13.2 x 22.6-cm) boards and backplane.

The fourth generation member of the PDP-11 family from Digital Equipment Corp, Maynard, MA 01754, features 256k bytes of memory—four times greater than that of the low end LSI-11/2. It uses the full instruction set of the PDP-11/34 minicomputer, as well as the software supported memory segmentation and protection features of the RSX-11M and -11S multitasing, multitasking, user operating systems. Employing the LSI-11 bus structure with asynchronous operation, the family has a cycle time of 290 ns (CPU) and 500 ns (memory); memory access time is 210 ns. A multifunction board option includes ROM, RAM, serial I/O, and crystal clock functions. An optional floating point processor chip executes from 5 to 10 times faster.

In addition to RSX-11M and -11S software, the microcomputers run all LSI-11 family software without modification including the RT-11 operating system and high level languages such as BASIC, FORTRAN IV, and FOCAL. Software debugging aids include hardware implemented ODT function (microcoded). Software also permits protected program space and multiuser operations.

In 100-unit quantities, the unit is priced at $1758. A rack mountable, packaged PDP-11/23 version, priced at $4500 in 100 quantity ($6800 for single units), measures 19 x 5.19 x 22.7” (48.3 x 13.2 x 57.8 cm). Customer evaluation shipments are scheduled for late summer. A P/ROM board for $300 and P/ROM programmer for $1975 support P/ROM intensive LSI-11 applications.

Circle 331 on Inquiry Card

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**Diagram**

LSI-11/23 CPU module (model KDF11-AA) consists of MMU chip with 11/34 compatible memory management, floating point accumulators, and scratchpad and working registers; fast access control chip with 552 words of micromemory; and data chip with registers, 16-bit data path, and ALU. KEF11 option provides single/double-precision, FP-11 compatible, floating point instructions.
Rugged Microprocessors Are Produced for Military Uses

Meeting MIL-STD-883C requirements, the military version of the Am8085A rugged microprocessors are produced for military uses. Meeting MIL-STD-883C requirements, the military version of the Am8085A single-board houses communications computer for OEMs.

The S-100 board computer, Micro-Slice, contains a 4-MHz Z80 module with power-on jump to any 256-byte boundary, eight software prioritized interrupt inputs, and realtime clock. Its communication capabilities are enhanced by its support of the IBM Bisync protocol; it also features X.25 or X.75 level one compatibility. Memory handles up to 8k of ROM and 2k of static RAM.

Other features that enable the board's use for OEM, business, and hobby applications are an asynchronous/synchronous serial port with 16 software selectable baud rates (50 to 19.2k), two fully buffered bidirectional parallel ports, common output buffer, four bidirectional USART control ports, two realtime clock control ports, two single-bit status ports, and fully buffered bus drivers. Slave mode operation permits multiple Micro-Slices to run on the same bus under one CPU. Micro Diversions, Inc, 8455-D Tyco Rd, Vienna, VA 22180, supplies front panel software either as a listing or pre-programmed on EPROM.

Logic diagram portrays Micro-Slice™ single-board communications computer. Z80 based system from Micro Diversions features software selectable parity, stop bits, and number of data bits; break detection and generation; local or remote maintenance loopback; transparent or nontransparent mode; and full- or half-duplex operation.

Circle 332 on Inquiry Card

Circle 333 on Inquiry Card
BATTERY SUPPORTED CALENDAR CLOCKS

PDP-11*
TCU-100 • $495
- Provides month, day, hour, minute and second.
- Can interrupt on date/time, or periodic intervals.
TCU-150 • $430
- Provides year, month, day, hour, minute and second.
- Automatic leap year.
- Patches for RSX-11M, RT-11 FB/SJ VO2, VO3 and UNIX.

LSI-11/2*
TCU-50D • $295
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- Dual size board.
- Patches for RT-11 SJ/FB VO2, VO3B.

Lockheed SUE
TCU-200 • $550
- Provides year, month, day, hour, minute, second and milli-second.
- Interval interrupts between 1/1024 seconds and 64 seconds.

Computer Automation (Naked Mini)
TCU-310 • $385
- Provides year, month, day, hour, minute and second.

Multi-Bus**
TCU-410 • $325
- Provides year, month, day, hour, minute and second.
- SBC/BLC compatible.

HP 2100
TCU-2100 • $395
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Serial Clock (RS 232 or 20 mA)
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- Connects between any terminal and host computer.
- Provides date, time and more!

All Digital Pathways TCUs have on board NICAD batteries to maintain time and date during power down. Timing is provided by a crystal controlled oscillator. Prices are U.S. domestic single piece. Quantity discounts available.

For more information on these products, contact:
Digital Pathways Inc.
4151 Middlefield Road
Palo Alto, CA 94306
Phone: (415) 493-5544

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<th><strong>NCC Show</strong></th>
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<th><strong>LSI-11</strong></th>
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<tr>
<td>Visit us in booth 2631 to see our full line of MULTIBUS® compatible microcomputer products and DEC compatible, multi-purpose and custom memories.</td>
<td>We’ve priced these memories to be the best values ever, consistent with full spec. memory elements and our rigid quality assurance programs. Listed prices are single quantity, U.S. only. Substantial OEM discounts available.</td>
<td>We’ll pay the airfreight on any of these memories, anywhere in the U.S.</td>
<td>For high density LSI-11 memory expansion the dual height MSC 4601 gives you 32K to 64K bytes, with on-board distributed refresh, in a single option slot. Provision for battery backup. Addressable in 2K byte increments. Only $935 for the 64K byte version.</td>
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<td><strong>48 hour delivery</strong></td>
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<td>MSC 4601</td>
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<td>We’ll ship all single quantity orders within 24 hours of receiving your written purchase order. And we’ll ship airfreight. With many models, OEM quantity orders (25 or more) can be filled just as fast. Check with us for details.</td>
<td>These offers apply only to the specific models shown and may be withdrawn without notice.</td>
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<td>The MSC 4501 gives you up to 32K bytes in 8K increments in a single quad slot. Distributed or burst refresh modes are on-board switch selectable. $450 for 32K bytes is our best price ever.</td>
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<td><strong>MSC 4501</strong></td>
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IS THE BEST TIME TO BUY OUR LSI-11, PDP-11 & PDP-8 MEMORIES.
HERE’S WHY:

**PDP-11**
For expanding PDP-11/04 to 55 memory, the MSC 3302, with built in power supply, provides 32K to 248K bytes, with or without parity. Can operate with two CPU's, either singly or simultaneously. $7,370 for 248K bytes with parity.

**MSC 3302**
The MSC 3303 fits 24K bytes into any single DD-11 small peripheral slot. Works with PDP-11/04 to 55. A special version provides clearance for use with PDP-11/15's and 20's. Lower power and low price of $995.

**MSC 3303**

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CIRCLE 134 ON INQUIRY CARD
Single-Chip µComputers Are Configured With Bus Oriented Architecture

System designs requiring single-chip economy, flexibility of multiprocessing bus architecture, and power of a comprehensive set of 16-bit arithmetic operations are fulfilled by the 70-series of single-chip microcomputer devices. First members of the ins8070 family are the ins8070a, a minimum system containing 64 bytes of RAM and no onchip ROM; ins8072 with 64 bytes of RAM and 2.5k bytes of ROM; and ins8074 with 64 bytes of RAM and 4k bytes (32k bits) of ROM. The 16-bit instruction set with stack operation is suited to control system applications, as well as high level language execution.

Fabricated by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, using n-channel MOS technology, the devices are housed in a standard 40-pin dip and require only 5 V. Communications between the devices and external memory or peripherals are effected via a 16-bit dedicated address bus and 8-bit bidirectional data bus. Handshake bus access control on the chip handles multiprocessing and DMA operations. Separate strobe inputs indicate when valid I/O memory or peripheral data are present on the 8-bit bus. The remaining I/O signals are dedicated to general purpose control and status functions.

Other features are simplified programming with multiple addressing modes, ASCII to BCD conversion in one instruction, character search instruction, onchip generation, two interrupt/sense inputs, and three user accessible control-flag outputs.

ins8070 is MICROBUS™ compatible. All voltage levels, drive capability, and timing are fully defined, thus any compatible microprocessor or peripheral may be interfaced and those that are not entirely compatible may be adapted.

INS8072 is National Semiconductor's single-chip microcomputer system containing 64 bytes of RAM and 2.5k bytes of ROM. 70-Series features bus oriented architecture for ease of implementation in standalone, direct memory access and multiprocessing applications.
RX02-Compatible Double Density Floppies for the LSI-11/2

And Have it Your Way

With the LSI-11/2 built-in: The MF-211 Dual Floppy/LSI-11/2 does everything the 11V03-L will do...

To go with your LSI-11/2: The FD-211 Dual Floppy System is the perfect plug replacement for your RX02...

The MF-211 Dual Floppy/LSI-11/2 System, using the CRDS Double Density Controller, is functionally identical to the DEC 11V03-L, but using only 10½” rack space. The MF-211 is the perfect low-cost answer to your 11V03-L requirement.

Check These Additional Features:
- Functionally identical to DEC’s 11V03-L
- Double and Single Density Operation
- Complete Software/Media Compatibility with LSI-11/2
- Over One Megabyte Storage Per System
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- DEC Software and Interface Cards available as options
- 30K Addressable Memory
- Considerable Dollar Savings

The FD-211 Double Density Floppy Disk System, using the CRDS Double-Density Controller, is totally software/media compatible with the Digital Equipment RX02 Floppy Disk System. It provides a compact, low-cost and highly reliable solution for all RX02 applications.

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- 5¼” Low Profile Chassis
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Why CRDS Products Give You So Much:
In addition to providing complete RX02 instruction set compatibility, the CRDS floppy disk controller card offers DMA data transfer by sector, bootstrap loader (eliminating need for DEC’s REV-11 or BDV-11), IBM 3740 formatter, self-diagnostic, and interface electronics, all contained on a single dual-height card which plugs directly into the H9270 backplane. To design and package sophisticated controller electronics on a single dual-height card is a unique CRDS achievement, unmatched by any other controller supplier in the industry.
- RX02 Double Density and Single Density Operation
- Complete RX02 Software/Media Compatibility with LSI-11/2
- Integral Bootstrap Loader
- Built-In Self-Diagnostic, Formatter
- Dual-Height Controller for LSI-11 or LSI-11/2 Backplane

For more info on our FD-211 and MF-211 Double-Density Floppy Disk Systems, just call or write:

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4 Tech Circle, Natick, MA 01760  Tel. 617 655-1800  TWX 710 386 0523

CIRCLE 135 ON INQUIRY CARD
Boards Operate at 4 MHz
In OEM Subassemblies
and Industrial Control

A family of four microcomputer boards introduced by Zilog, Inc., 10340 Bubb Rd, Cupertino, CA 95014, can be incorporated by OEMs into computer subassemblies and high performance industrial control systems. The main board in the series is the Z80 microprocessor based MPB. It contains four I/O peripheral components configured to support a line printer interface, DMA control, and two independent full-duplex serial communication channels implemented with the Z80A serial I/O and buffered for RS-422 or -423, interface.

The other boards include memory, floppy disc controller, and I/O. The Z80A ROM/RAM board has either 16k or 64k bytes of dynamic RAM, with sockets for up to 8k bytes of nonvolatile F/ROM or EPROM. The single-board Z80A FDC directly controls up to eight single-density floppy or mini floppy disc drives; double-sided drives are also supported. Although interfacing to Shugart’s 400, 450, 800, and 850 series, the controller’s control and data port bits are I/O programmable.

The Z80A I/D provides the 4-MHz boards with programmable I/O port capability. Four uncommitted PIO circuits support 64 bidirectional I/O lines; unused board space contains plated holes for insertion of wire-wrap devices.

In-Circuit Emulation and Signature Analysis Locate Faults At All Levels

Faults at the system, module, and component levels in 6800 microprocessor based products are located by the portable, standalone Microcomputer Analyzer (µCA) which combines the power of two diagnostic techniques—in-circuit emulation and signature analysis. Test points or data generation does not have to be built into the product under test, because the test instrument uses a microprocessor within the analyzer as the data generator, and the microprocessor socket of the system under test as the standard common test point for system analysis.

Using 110 V, 60 Hz, M68UCANA1 is enclosed in an attaché style case, measuring 19 x 10.5 x 7.5” (48 x 26.7 x 19.1 cm) and weighing 21 lb (9.5 kg). Both the alphanumeric display and keyboard are under software control and can be modified through program changes. Additional memory, communications interface, or other microprocessor emulator modules can be added to the multiple position card cage. Motorola Microsystem, PO Box 29012, Phoenix, AZ 85036, has priced the unit at $3750 each in quantities of 1 to 5.

In-circuit emulation is implemented by connecting the system under test to the analyzer through an umbilical cord and a 40-pin connector that plugs into the microprocessor socket. Customer supplied test programs thoroughly exercise all system components and provide data used to locate faults—at the module or functional level—in circuits, memory, and interfaces to the microprocessor.

At the component level, signature analysis locates faults by probing test nodes. The technique detects bit streams generated by the in-circuit emulator, compresses them, and displays hexadecimal representations of their values. The emulator cycles through its test program generating identical bit streams and the same hexadecimal values appear at nodes. Hexadecimal values obtained are compared against known good values to locate faults.

Total Hardware/Software Concept Forms Universal Development System

AMDS-AFD offers development tools for 8080, 8085, 6800, 6802, or Z80 microcomputer systems for design and testing. The station integrates the CPU processor and 48k bytes of static RAM, universal logic analyzer, CRT, and keyboard.

Hardware development capabilities are realtime in-circuit emulation to 5 MHz; 48-channel logic analyzer with 256-state trace buffer, three hardware break registers, loop counters, and delay counters; dual, double-density disc drives with 1M-byte storage capacity; and over 20k-Char/s, 24 x 80 CRT display. With 256 x 48 bits of storage, the logic analyzer traces realtime systems, using complex or simple break conditions.

Relocatable macro assembler, object program linker, screen based editor, interactive debugger, and command control language are the software development set on diskette.

Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045, has priced the system at $16,500.

In-Circuit Emulation

Motorola’s Microcomputer Analyzer (µCA)—M68UCANA1—is packaged in portable attaché type case. At left is signature analysis and time domain test probes, as well as control pod with test leads, and at right is emulation pod and cables to microprocessor

Chip Set and Development Computer Execute

PASCAL Object Programs

A 16-bit computer chip set, developed by Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663, is claimed to directly execute PASCAL object programs at least five times faster than is possible with conventional system software and eliminates the need for the host operating system and interpreter. The PASCAL MICROENGINE™ line includes both the chip set and a software development system for OEMs and personal computing stores.

The chip set standardizes the University of California at San Diego version of PASCAL. The software system includes a PASCAL operating system: PASCAL compiler, BASIC compiler, file manager, screen oriented editor, debug program, and graphics package, all written in PASCAL.

Key to the system is the pseudo machine (P-machine) implemented
If you don't see it here, ask!

M1000/M2000 series 5-inch and 9-inch display modules. These highly reliable displays testify to the effectiveness of measured rather than calculated MTBF. Samples of every complete Motorola CRT display module are life-tested for a minimum of 10,000 hours at 55°C. Customers report some of our displays logging more than 40,000 hours and still going strong.

M3500 series 12-inch display modules in chassis or kit form (shown). Cost saving, plus no metal boundaries to inhibit your own layout.

MD3000 series 12-inch display modules. Between the MD3000 and M3500 series, you can have your 12-inch display in any of several ways: chassis or kit, separate sync TTL level, composite video or direct drive inputs, choice of standard EIA phosphors, choice of scan frequencies, with or without anti-reflective faceplate.

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The M4408 15-inch module displays a full page horizontally (132 x 46) or vertically (96 x 66, shown). High character density and low cost, too—raster scan technique with standard TTL logic interface gives you economy twice: once in purchase price and again in design costs. A technology leader.

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Shrewsbury, New Jersey (201) 544-9541
Baltimore, Maryland (301) 821-0062
Overseas, ask for International Sales Manager, Carol Stream, Illinois (312) 690-1400.
WD9000 16-bit microprocessor from Western Digital is designated PASCAL MICROENGINE. Chip set consists of five LSI components. Arithmetic component contains ALU, microinstruction decode, register file, and processor control path. Control processor holds macroinstruction decode, portions of control circuitry, microinstruction counters, and I/O control logic. Three high speed 512 x 22-bit custom MICROM components implement P-code instructions.

Four MOS LSI components comprise the chip set. The arithmetic chip contains microinstruction decode, ALU, and register file. A microsequencer chip contains macro instruction decode, portions of control circuitry, microinstruction counters, and I/O control logic. The two MICROM chips (each 22 x 512) contain the microinstruction ROMS along with microdiagnostics.

Additional features are user defined bus configuration, four levels of interrupts, single- and multibyte instructions, hardware floating point, stack architecture, 3.0-MHz 4-phase clock (75 ns/phase), and TTL compatible 3-state interface. Basic desktop computer WD9000 features the MICROENGINE processor, 64k bytes of RAM, DMA control functions, floppy disc controller, two RS-232 asynchronous ports, and two 8-bit parallel ports on a single board, with...
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Pin compatibility on our 16K, 32K and 64K ROMs gives you built-in future memory expansion capability. All it takes to upgrade your system's ROM capacity for new applications is to replace our 16K ROMs with our 32K ROMs or replace our 32K ROMs with 64K ROMs. And you can usually do it with no hardware changes.

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Static Read Only Memories.

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<th>Part Number</th>
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<th>Speed</th>
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<tr>
<td>SY4600</td>
<td>2048x8 or 4096x4</td>
<td>550nsec</td>
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<tr>
<td>SY2316A</td>
<td>2048x8, 550nsec</td>
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<td>SY2316B</td>
<td>2048x8, 450nsec</td>
<td>(2716 compatible)</td>
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<tr>
<td>SY2316B-3</td>
<td>2048x8, 300nsec</td>
<td>(2716 compatible)</td>
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<tr>
<td>SY2332</td>
<td>4096x8, 450nsec</td>
<td>(2716 compatible)</td>
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</tr>
<tr>
<td>SY2364</td>
<td>8192x8, 450nsec, 24 pin</td>
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three power supplies in a 5.25 x 16.25 x 13.5" (13.3 x 41.3 x 34.3-cm) enclosure. The WD/90 PASCAL MICROENGINE computer for program development and OEM applications is comprised of the single-board computer, power supply, system enclosure, documentation, and floppy diskette containing UCSD PASCAL operating system.

The chip set is priced at $195 for a single set, $97.50 each at 10,000 quantity. The single-board computer costs $1995. The system retails at $2995; OEM single-quantity price is $2495.

Circle 337 on Inquiry Card

Microcomputer Speaks Through Use of Speech Synthesizer Modules

Voice response is now possible using either of two speech synthesizers that have been designed to interface to Radio Shack's TRS-80 microcomputer. One of the modules utilizes phonemes, while the other operates in either phonetic or direct parameter control modes.

Phoneme Module

Votrax, a div of Federal Screw Works, 500 Stephenson Hwy, Troy, MI 48084, has designed the electronic voice response synthesizer as a plug-in peripheral to the microcomputer, providing speech in English and limited foreign languages. The package is complete with an audio amplifier and speaker. A ribbon cable, emerging from the back of the 12 x 6.2 x 4" (30.5 x 15.6 x 10.2-cm) cabinet, is long enough to allow the cabinet to rest on top of the video display.

The synthesizer converts the computer output into electronically synthesized speech, using the 62 phonemes to produce words and phrases. To produce a phoneme, the user supplies the synthesizer with the ASCII character corresponding to the phoneme symbol. Integrating these phonemes creates smooth, intelligible speech.

Both Level I and II BASIC can be used. BASIC programs can be created or modified to include computer voice response using a specialized print statement as an output command. The last 32 print locations on the video display, into which the interface has been address mapped, is the window. After opening the window, the user should first send a pause (which is silent) to synchronize the module when it has been idle. While the window is open, any character printed into it is copied into the synthesizer's input buffer. After the transmission, a pause should be sent as the last phoneme before closing the window; the window then is closed to prevent accidental outputting.

The synthesizer produces the sound and the LED goes off. The voice module's input buffer is 32 phonemes deep; duration of a phoneme varies from 40 to 160 ms. Power requirements are 120 Vac, 60 Hz, 0.10 A.

Circle 338 on Inquiry Card

Direct Parameter Control Phonetic Mode Synthesizer

Model CT-1T is an S-100 bus compatible speech synthesizer packaged by Computalker Consultants, 1730 21st St, Suite A, Santa Monica, CA 90404, in a 6 x 4 x 12" (15 x 10 x 30-cm) chassis with a 110-Vac power supply. The interface circuit board contains a 2-W audio amplifier, an S-100 connector for the CT-1 speech synthesizer board, and a Radio Shack compatible edge connector. A cable connects the unit to the TRS-80 bus connector on either keyboard or expansion interface. Standard phone jacks connect to external speakers, headphones, or external amplifier (not provided).

The high quality voice generator operates with a microcomputer which has Level II BASIC and a min of 16k RAM (32k is recommended). Control of perceptually and physiologically fundamental aspects of speech is via nine acoustic/phonetic parameter data frames transmitted on the computer's bus.

Direct parameter control mode sends data to the synthesizer's nine output ports at the rate of 900 bytes/s from a predetermined speech parameter file to give intelligible and natural sounding speech. This requires a rate of approx 100 frames/s. Characteristics and language variations of the speaker are retained in the output. A parameter data frame consists of a sequence of nine output instructions which update each of the nine parameter values. After addressing any of the ports, a min of 20 µs must be allowed before addressing another port.

In phonetic mode, the CSR1 Synthesis-by-Rule software converts ASCII phonetic text strings into speech parameter data, which are sent to the synthesizer to produce speech. The GENPRM subroutine uses tables of parameter values for each English phoneme.

Software supports both modes. The basic set consists of CREDEIT parameter data editor, speech parameter data files (HELLO, LETTERS, DIGITS), and CSR1. They are available on 5.25" (13.34-cm) diskettes or standard cassettes.

Circle 339 on Inquiry Card

Extended Systems Span Range of Low Cost to Intensive Graphics

Two desktop graphic computing systems added to the 4050 series create a 3-member family with language, storage, and software compatibility. Tektronix, Inc, PO Box 500, Beaverton, OR 97077, extended the 4051 system with models 4052 and 4054, featuring a new processor and special memory architecture for speed. BASIC and Plot 50 software, allowing system expandability to multisuser configurations, operate on the systems. The 4052 is directed at areas of research and management reporting. For engineering and design areas, the 4054 handles complex diagrams and high density interactive graphics.

Features that are standard among all three units are a direct view storage tube, internal magnetic tape drive with 300k bytes, and an IEEE Std-498 (CPM) interface. A 16-bit microprogrammed processor with microcoded floating point instructions

Extended series of Tektronix graphic computing systems add 4052 (pictured) and 4054 to model 4051. Two new systems have 32k bytes of memory, processor for high performance computing and graphics, and data sharing with host computer at up to 9600 baud. Model 4054 offers 19" (48-cm) display along with other graphics enhancements.
A Cut Above the Other

Able comes up with a 16-line DV11 replacement that puts the PDP-11 user back in control.

You don't have to be stuck again with fixed sync/async line controller configurations in your PDP-11. Our DV/16 puts you back in control with a unique microprocessor-derived flexibility that lets you mix sync and async lines in any combination of four or eight while maintaining modem control and compatibility with established DV11-related software. You get 16 channels on only four boards compared to a filled up nine-slot mounting module required by the DEC equivalent. Expansion to 32 lines takes up only 7 standard SPC slots in your PDP-11 compared to the addition of two full 9-slot backplanes for the DV11's.

We use word transfer instead of byte DMA to either gain a two to one speed advantage (76,800 characters per second) or let you operate in one half the bandwidth required by DV11 data transfers. Power requirements are more than fifty percent lower, too. The DV/16 is a cut above the other all right, but the price doesn't show it. Ours is a very cost effective alternative, delivered off the shelf as usual. We've made the cut. Now it's your deal! Write for details. We'll show you why our customers call us the leader among manufacturers of DEC enhancements.

Able, the computer experts.

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Graphic computing system. Block diagram highlights model 4052, consisting of four board sections. Solid black lines are data and address, darker shaded lines are address, and lightest areas are data lines. All 4050 series products are compatible in language, software, storage, and GPIB peripheral devices.

has been used in the 4052 and 4054 to increase throughput over the 4054 for generation of dense, mixed graphic and alphanumeric displays. Memory is 32k bytes, expandable to 56k bytes. Data processing and communications speeds also are increased; the Option 1 interface offers rates up to 9600 baud.

Graphics enhancements to the 4054, not offered in the other systems, are a vector character generator (as opposed to dot matrix); four character sizes; constant-rate vector generator to draw dotted, dashed, and solid vectors; and thumbwheel controlled crosshair cursor. The 19" (48.3-cm) screen has over 13M addressable points to support 133 character lines of text.

Binary loading and matrix commands, standard on the 4052 and 4054, can be accessed on the 4051 by inserting the respective ROM packs. Added ROM packs for the two systems are the 4052 R06 editor, 4052 R07 signal processing ROM pack, option 10 printer interface, and ROM pack for the 4907 file manager.

Options and peripherals are a joystick, matrix printers, hardcopy unit, interactive digital plotters, file manager, digital cartridge tape drive, and graphic tablet. Prices are $5995 for the 11" (28-cm) 4051, $9800 for the 11" (28-cm) 4052, and $16,500 for the 19" (48-cm) 4054.
The Software Solution

Microsoft holds a unique position in the microcomputer OEM marketplace – we’re the ONLY company with a complete line of microcomputer system software. That’s our specialty... and we’re very good at it. Not just one or two products for one or two computers, but an integrated line of system software that supports all the popular 8-bit processors and the new 16-bit processors.

**BASIC Interpreter**
for 8086

Get the most popular microcomputer BASIC in the world for the most available 16-bit microprocessor, the 8086.

**BASIC-80 Interpreter**
for CP/M, ISIS-II, TEKDOS

If you need BASIC for an 8-bit machine, you’ll want Microsoft BASIC. It’s the world’s most powerful BASIC, supporting both industrial and commercial use.

**FORTRAN-80 Compiler**
for CP/M, ISIS-II, TEKDOS

FORTRAN, enhanced for microcomputer use, comes with macro assembler and linking loader. Generates optimized machine code at 300 lines per minute and easily links to assembly language subprograms.

**COBOL-80 Compiler**
for CP/M and ISIS-II

ANSI ’74 COBOL with fully tested ISAM and many advanced features such as ACCEPT/DISPLAY, COPY, EXTEND, SEARCH, COMPUTE, STRING. Packed decimal data representation conserves memory.

**MACRO-80 Assembler**
for CP/M, ISIS-II, TEKDOS

No question about it — MACRO-80 is the fastest, most powerful 8080/280 assembler on the market. Full Intel-standard macro facility and an assembly rate of over 1000 lines per minute. Accepts 8080 and 280 opcodes.

Reliable, proven, tested software. Microsoft's software is already in use in thousands of microcomputer systems. Buy it from stock, or talk to us about custom versions. OEM licensing and purchase agreements are available. If there's a "software void" somewhere in your microcomputer product line get the solution. At Microsoft.
4-MHz 16-Bit Family of Microprocessors Increases Throughput

Separate address and data buses maximize performance of the TMS9900-40 microprocessor by avoiding multiplexing delays. The 16-bit MPU features a minicomputer instruction set and memory to memory architecture. Texas Instruments, Inc., PO Box 1443, Houston, TX 77001, supports three I/O techniques—DMA, memory mapped, and CRU (for optimum control line manipulation without using memory space). CRU provides single-command page switching for memories larger than 65k bytes.

The current family includes the 9900-40 CRU ($41.25/100 units), 9904-40 clock generator/driver ($7.20), 9901-40 peripheral systems interface ($7.06), and 9902-40 asynchronous communications controller ($5.63). A universal emulator for the Advanced Microprocessor Prototyping Laboratory supports the microprocessor. Floppy and hard disc based systems with high level language development options are available.

Circle 341 on Inquiry Card

General Purpose Module Connects Logic Analyzer To Most Microcomputers

Realtime viewing of system operation is obtained when the model 1611A logic state analyzer when model 10264A general purpose module (diagrammed) is attached. Address field uses 16 bits; data field is set for 8-bit bus; with 8-bit external and 4-bit auxiliary fields for other buses or control lines.

Activity on most microprocessors is monitored by Hewlett-Packard's model 1611A logic state analyzer when model 10264A general purpose module (diagrammed) is attached. Address field uses 16 bits; data field is set for 8-bit bus; with 8-bit external and 4-bit auxiliary fields for other buses or control lines.

Each 8-bit half of a multiplexed 16-bit address bus and a 16-bit data bus are clocked separately into the analyzer. A separate clock interro­ gates an added 4-bit auxiliary bus at another time.

A listing shows absolute code being executed with respect to established trace parameters. Display formats for address and data fields are in hexadecimal or octal. External and auxiliary fields may be in binary, or the base chosen for the data and address fields.

With the general purpose module installed, the analyzer's mnemonic key is inhibited since mnemonic code is microprocessor defined and therefore cannot be displayed. Connection to the system under test is universal, with two pods, individual leads, and miniature probes for each of the data, clock, and qualifier inputs.

Circle 342 on Inquiry Card

µProcessor Analyzer and Clip-on Probe Broaden In-Circuit Testing

Microprocessor analyzer capabilities have been extended from 8080 and 8085 systems to include the Z80. One instrument, using three separate clip­ on probes, offers direct user inter­ action with all memory locations and internal microprocessor registers, and compatibility with all 8080, 8085, and Z80 system configurations. Current AO8080 analyzers (see Computer Design, June 1978, p 161 and Sept 1978, p 154) can be factory updated by AO Systems Inc, 1736 Front St, Yorktown Heights, NY 10598, to include the Z80 edition capabilities. The analyzer costs $2795.

Interactive register access functions include the Z80's background (alternate) register set, and index registers IX and IY. The operator accesses the foreground or background register set, independently of the register set in use by the program.

Programs may be single-stepped by machine cycle or instruction set, or run at an adjustable speed of 1 to 4000 steps/s while examining memory or registers. The program trace recorder stores 128 instructions. Debugging features include breakpoint and realtime monitor functions.

Circle 343 on Inquiry Card
Almost perfect.

Our new ADM-42 doesn't have quite everything. But it comes so close, you might never notice.

Because it's a complete, semi-intelligent terminal for just about any application you can name. And it does just what you want it to do, just when you want it done.

The ADM-42 is completely self-contained, and provides you with flexibility of format, security, editing, interface, and transmission. It also features a full two-page display as standard equipment. Not as an option. And it comes with a truly staggering array of options.

THE MORE YOU USE IT, THE SMARTER IT SEEMS.

We gave the ADM-42 a bright, easy-to-read 2000 character display. A full 128 ASCII character set. 16 function keys for 32 separate commands. And five separate cursor control keys.

The 42's behavior modification gives you a factory installed personality for an alternative ESC sequence lead-in—in addition to the standard ESC. And End Block character. A New Line character sequence. A field separator. And even a function sequence preamble.

Its status displays on the screen give you a conveniently wide range of information at a glance. While its special symbols indicate the entry of control characters in memory. Also, all control characters can be stored using the escape sequence or program mode. And the Field Protect Mode allows rapid data entry into forms or instruction pages.

THE ADM-42 WILL HAND YOU ANOTHER LINE.

The terminal's displayed data is formatted in 24 lines per page, 80 characters per line. And, to top it off, it comes with a 25th line established and reserved exclusively for status indicators and messages of up to 79 characters.

As if all this weren't enough, the ADM-42 has an impressive list of options. Like synchronous transmission with various line protocols. An extended memory capable of adding data space up to a maximum of 8 pages. And programmable function keys, to name but a few.

THE ADM-42 IS ONE TOUGH ACT TO FOLLOW.

The ADM-42 has just about everything. Including a microprocessor that increases reliability and ease of operation. Any way you look at it, in fact, it's one pretty smart buy.

So if you're thinking of upgrading to a more intelligent terminal, at a more than reasonable price, call us today. Or better yet, contact your local distributor.

We'll show you how easy it is to move up to the ADM-42. The terminal that's so smart, you'll swear it's got a mind of its own.

AD42
Getting smarter all the time.

Computer/Terminal Combination Produces Business Microsystem

Configuration of the System B microcomputer manufactured by Vector Graphic, Inc, 31364 Via Colinas, Westlake Village, CA 91361, uses the Z80 based Vector mz and 12" (30.5-cm) diagonal Mindless Terminal. The mz has 158 instructions, two quad-density Micropolis floppy discs, disc controller board, bit streamer I/O board, 32k RAM, and 12k 2708 P-ROM-RAM board with extended monitor. The terminal incorporates the keyboard and monitor.

Other features are the Flashwriter II video board displaying 80 characters x 24 lines with an 8 x 10-character matrix. The 48k dynamic RAM board contained in the business system uses 16k-bit chips.

Software includes MDOS with Micropolis BASIC and the company's MZOS disc operating system (see Computer Design, Dec 1978, p 142), as well as cp/x. A Z80 assembler zsm facilitates interactive program customization. Suggested retail price is $4750.

CIRCLE 344 on Inquiry Card

\[\text{\textcopyright Computer System's Power Accomplishes Small Business Applications}\]

The self-contained sds 420 desktop system consists of a 2-MHz 6502A 8-bit microprocessor; 32k bytes of memory expandable to 56k; from 1.25M to 10M bytes of floppy disc storage on PerSci dual-diskette, single/double-density drives; and a Ball Brothers 12" (30.5-cm) CRT display with 25 lines of 80 characters/line and 2k bytes of refresh memory. A 71-key alphanumeric detachable keyboard has a decimal pad, cursor control, reset and interrupt keys, and three user programmable keys. Memory cycle time is 250 ns. Dual-head drives are optional; up to four drives are supported by the system. A single 9 x 13" (23 x 30-cm) board, mounted beside the memory board, houses the processor chip (with instruction times of 1 µs Min and 3.5 µs max), two LSI chips for logical interface with subroutines, 1k bytes of ROM for bootstrap program storage, 2k bytes of RAM containing the CRT's current display, controllers, and two RS-232 I/O ports. A communications interface and parallel interface are optional. Single-unit price is $7700.

Scientific Data Systems, Inc, 12640 Beatrice St, Los Angeles, CA 90066, has equipped the system with an extended 12k BASIC interpreter—an advantage for performing business applications. Features of standard BASIC are improved upon with the addition of commands for formatted printing; input and manipulation of commands; file interface to random, sequential, and keyed files; I/O device handling; error handling; screen window management; and source file editing. Users can write database manipulation programs with the keyed file interface.

The operating system, modeled on large computer systems, controls the system through simple unambiguous commands. It supports program segment overlays, dynamic disc space allocation, flexible file size and organization, and device independent I/O. Utility programs handle file directory listing, diskette initialization and copying, handling of sequential files, and a resident assembler.

CIRCLE 345 on Inquiry Card
In 1975, Printronix introduced the first printer designed to fill the need for medium speed impact printing at practical prices. The unique concept and design of this matrix impact line printer brought unequalled print quality to impact printing. Its elegant simplicity, with up to 50% fewer parts than band, drum or chain printers, also established proportionately higher levels of reliability. Today, they are available in 150, 300 and 600 line-per-minute models priced about the same or less than medium speed band, drum or chain printers. They're warranted for one full year while 90 days is typical for others. And they all offer you one feature band, drum or chain printers can't provide: full graphics plotting capability. Get acquainted with our family. You might be captivated by their cost/performance and cost of ownership attributes. They're all up for adoption. Printronix, Inc., 17421 Derian Ave., P.O. Box 19559, Irvine, CA 92713. (714) 549-8272. TWX: (910) 595-2535.

PRINTRONIX
CIRCLE 142 ON INQUIRY CARD
To see or not to see? That is the question.

And Polaroid has the answer: circular polarizer contrast-enhancement filters let you see your display under a variety of lighting conditions.

Circular polarizers kill reflections from CRT's by acting as a light trap. Ambient light can go through the circular polarizer, but after it is reflected from the tube face, it can't get out again. And circular polarizers can suppress up to 99% of reflected room light. They are far more effective than absorption-type filters for improving contrast.

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We offer the widest selection of off-the-shelf contrast-enhancement filters. Or—we'll make up precisely the filter you need: Choose glass or plastic filters with polished or nonglare surfaces. They can be flat or shaped to your specifications. They can have anti-reflective, RFI or abrasion-resistant coatings. Colors can be computer-matched to your display to provide maximum visibility.

We sell circular polarizers and offer technical assistance worldwide. For a free sample, just fill out and mail the coupon below. Or call Dick Adams collect at 617-864-6000, ext. 3315. He'll recommend the contrast-enhancing filter that best meets your needs.

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The double-headed 5-1/4" floppy with a big difference.

PCC has them. In quantity. Ready for shipment.
Double-headed floppies that are compatible with Shugart down to the last screw hole.
It’s the PCC FD-250, the double-headed version of our own FD-200. It can replace the Shugart SA 400 and quadruple your capacity (to as high as 437.5K Bytes).
What the FD-250 means is that right now you can fill up those empty boxes in your systems that are waiting for floppy drives. And you can upgrade from single- to double-sided immediately.
All without re-machining a single screw hole.
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Why wait? Your competition won’t.
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New York-(716) 271-2710
Florida-(305) 647-6150
England-(0) 734-582115
Headquarters-(213) 999-2020

CIRCLE 143 ON INQUIRY CARD
SOFTWARE

Program Development System Capabilities Operate Simultaneously

Text editor, assembler, link loader, and simulator facilities comprise the MicroSim program development system for Intel 8080/8085 or Zilog Z80 target microprocessors. It reduces debugging time for assembly language programs since it assembles a program as it is entered.

Features that the Digital Products Group, 350 Sharon Pk Dr, Q23, Menlo Park, CA 94025, has incorporated are byte segregation and an internal clock. Thus, the system can distinguish bytes of storage containing data, instructions, and addresses. The counting of machine cycles allows the user to determine the real-time duration of target program execution.

If an error is discovered during execution of the program, it is corrected immediately using editing commands within the simulator that modify the source program text. Each line of text that is entered is also checked for syntax errors and is assembled into machine code. Once corrections are complete, a single command reloads all program segments into memory and restarts program execution.

Circle 346 on Inquiry Card

OEMs Can Build High Level Language Into Microcomputer Systems

OEMs can supply BASIC-80 as part of their software for the isbc 80 single-board computer systems with the isbc™ 802 BASIC-80 interpreter package. The software is tailored to the actual system configuration by the OEM, by the service organization in the field, or by the customer. Meeting minimal BASIC standards of ANSI X3.60-1978 and ECMA-55, the language is documented and interpretative, serving commercial, control, and industrial applications. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, designed the software to run under the RMX/80™ Realtime Multitasking Executive.

Two forms are a relocatable version and predefined version. The relocatable version operates with an isbc 80/10A, 80/20, 80/20-4 or 80/30 system equipped with an I/O terminal, 48k of RAM, and normally including a disc drive (the BASIC, alternatively, could be stored in ROM-P/BOM).

An Intellec® Microcomputer Development System can store the BASIC-80 interpreter as a library of routines on a discette. To add the language, the designer specifies the end-use system parameters. The development system retrieves the applicable components and produces a minimum size, full feature BASIC-80 configured to the specific OEM system. The development system also houses FORTRAN-80, PL/M-80, and/or macro assembler languages.

Routines can be selected from other user supplied discette files of the FORTRAN runtime library and RMX/80 realtime multitasking executive library. The development system links and relocates these routines with other software components into a complete software solution in machine level code. It is then loaded into the isbc system and stored on disc or on P/BOMs.

Automatically loading BASIC-80 and the needed RMX/80 components, the predefined version operates with a specific hardware system configuration that includes the isbc 80/30, 32k bytes of additional RAM, the isbc 204 disc controller board, a disc drive, and compatible terminal. Two P/BOMs are plugged into the computer board to provide the bootstrap loader.

A software package contains both a single- and double-density diskette, each containing the configurable and preconfigured versions. BASIC-80 configurable RMX/80 disc based interpreter is copyrighted and licensed by Intel. The one-time price is $4995.

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672,000 BYTE TAPE DRIVE FOR 3M DC100A DATA CARTRIDGE

MODEL 200 MINIDRIVE™...
The most compact tape drive ever...
Large, up to 672,000 bytes capacity...
Recording on one or two tracks...
Read-after-write capability...
3M DC100A or ITC TC-150 Data Cartridge...
High transfer rate, up to 48,000 bits-per-second...
Low power requirements, +5 and +12 Volts DC only...
High electrical and mechanical reliability...
Flexible configurations range from basic OEM building blocks to complete tape memory systems...
Optional electronics and mounting hardware...
From $250 in single unit quantities...
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CORE MEMORIES

LSI-11, SBC 80, 6800

S-100, IMP, PACE

- Non-volatile. No battery back-up
- Pin to pin compatibility.
- Power monitoring for data protection.*
- Write protect.
- One year warranty on parts and labor.
- All units temperature cycled and burned in.

Software Support
Enhances Debug/Development System

To speed and ease the software development cycle, an array of software supports the Z80, floppy disc based Z80F™ development system. This device (see Computer Design, Apr 1978, p 174) develops and debugs the microcomputer product line produced by Mostek Corp, 1215 W Crosby Rd, Carrolton, TX 75006

FLP-80dOS (version 2.0) is the operating software. Augmenting the operating software and system capabilities are two macro assemblers, BASIC, FORTRAN IV, and a software library. The Mostek Z80 macro assembler, MACRO-80, is an upgrade of the FLP-80dOS assembler (ASM). MACRO-70 has advanced from the FLP-80dOS assembler for the 3870 microcomputer (FZCASM). Fully upward compatible, both assemblers provide for nested conditional assembly and symbol lengths of any number of characters in addition to macro capabilities. They support global symbols, relocatable programs, a symbol cross reference listing, and unused symbol reference table.

The company's BASIC, an implementation of Microsoft BASIC for the Z80 microprocessor, acts as an interpreter and is suitable for user interactive processing. Features include long variable names, substring assignments, and hexadecimal and octal constants. Arrays have up to 255 dimensions, with runtime allocation and deallocation. Editing, error trapping, and trace facilities simplify program debugging.

Comparable to mainframe and minicomputer FORTRAN compilers, FORTRAN IV provides a microprocessor FORTRAN and assembly language development package that generates relocatable object modules. Subroutines may be compiled separately and stored in a system library. Also featured are calling Z80 assembly language subprograms from FORTRAN programs and compiling several hundred statements/min in a single pass.

The final enhancement is the FLP-80dOS software library (volume 1) containing 23 programs designed to run on the operating system. It is supplied on two diskettes, with both source and object code. □

Circle 348 on Inquiry Card - MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

Software Support
Enhances Debug/Development System
FRANKLY, WE DON'T KNOW WHY ALL FLOPPY DRIVES AREN'T MADE THIS WAY.

Sure, MegaFloppy™ disk drives may cost more than other 5¼-inch floppies. But they give you so much more. For example, MegaFloppy disk drives give you all the storage capacity of an 8-inch floppy in the body of a 5¼-inch floppy. Up to 1 million bytes. More than ten times the capacity of other 5¼-inch floppies.

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No wonder we're already Number 2 in the marketplace. With over 20,000 units shipped.

So if you've always used 8-inch drives, and thought you always would, consider our MegaFloppy disk drives. They'll make you wonder why people build them any other way.

MICROPOLIS™
Where the 5¼-inch drive grew up.

For a descriptive brochure, in the U.S. call or write Micropolis Corporation, 7959 Deering Avenue, Canoga Park, California 91304. Phone (213) 703-1121. Or, better yet, see your local representative.

CIRCLE 146 ON INQUIRY CARD
See the Micropolis drive on display at their Marriott Essex House suite...
HEY DISK JOCKEY, WE'RE CELEBRATING SOMETHING NEW TO BACKUP YOUR WINCHESTER DISKS.
If you’ve been trying to backup Winchester disks with floppies and your file is beginning to look like this week’s top 40, lend us your ears.

DEI’s new 34 M Byte High Density Microtape™ Cartridge Drive is the latest development in the Funnel Series. It has as much capacity as 34 double density, double sided floppy disks, and 48% more capacity than an 800 bpi ½-inch reel-to-reel drive with 2,400 ft. of tape.

The 7,200 bpi, ¼-inch cartridge tape drive accomplishes this remarkable technical breakthrough by recording 7-tracks in GCR or MFM code at up to 10,000 FRPI and can transfer at the rate of 216 Kilobits/second.

Put Microtape Drive performance together with small size (it’s just 7-inches wide, 5¾-inches deep, 4¼-inches high and weighs 4 lbs.) and you’ll have another reason to specify.

To top it all, there’s DEI’s experience with over 6,000 High Density cartridge tape drives in the field. In fact, our 17.28 MB Microtape drive has become an industry standard for Winchester disk save and restore.

So join the celebration and try our new High Density Microtape drive with your minicomputer system. Your customers will be tooting a tune that’s music to your ears.

Write Data Electronics, Inc.
370 N. Halstead St., Pasadena
California 91107
Or call (213) 351-8991, Telex 67-5327.
Three basic approaches to logic design have been developed by the semiconductor industry to satisfy the demand for large scale digital integrated circuits: standard off-the-shelf circuits, custom circuits, and gate arrays. Since each of these has characteristic advantages and liabilities, the approaches are frequently mixed in system designs.

The off-the-shelf approach represents the lowest cost option for the MSI/LSI user because such circuits are normally sold in relatively large quantities throughout the industry as part of a circuit family for use in implementing logic, thereby supplying cost advantages of large volume semiconductor manufacture. However, the high risk factor that is involved in the probability that the industry will adopt a particular LSI circuit or family as a standard (thereby permitting large volume sales), limits the line of standard LSI circuit families. This is particularly true in high technology fields, such as ECL, where potential volume (even if a circuit is adopted as a standard) is much smaller than that of the more generalized, less critical applications.

Custom design provides each customer with exactly the circuits he needs (usually on a proprietary basis), but the cost per circuit is high unless volume requirements are large enough to amortize the relatively high development costs. Moreover, development time of complex custom circuits can be on the order of 1 to 2 years. A custom design approach to logic design of systems usually involves a mixture of standard MSI/LSI circuits coupled with custom LSI circuits.

The third approach involves a standard array of a large number of gate circuits diffused into a silicon chip. An interconnecting metallization pattern is provided by the circuit designer to allow the manufacturer to convert these basic gates into functional custom circuits. This gate-array approach represents a tradeoff between development cost and time on the one hand, and performance on the other. Performance is compromised because of the necessity for using a gate as the basic building block for LSI circuits. This results in longer propagation delays, compared with similar functions using ECL series-gating techniques (for example), and usually involves a relatively inefficient use of chip area.

The Macrocell approach to custom LSI, developed at Motorola, supplements the three techniques described. This design strategy circumvents the cost and time factors of custom circuits, and reduces the deficiencies of the conventional gate arrays.

**Macrocell Array Concept**

Extending the gate-array concept, the Macrocell Array, instead of gates, contains a number of unconnected transistors and resistors within each cell in the array. Specifi-
The Raycorder Cassette Terminal Model 6801

The Model 6801 Raycorder Cassette Terminal is a dual-cassette operating system capable of reading, writing, and copying data at switch selectable rates from 110 to 9,600 baud through a full duplex, asynchronous RS232C interface.

Operating under the control of a microprocessor with up to 4K of firmware, the Model 6801 has designed-in versatility never before available in a system of this type.

Connected to a serial port of a DEC PDP8 or PDP11 and given the proper address, it will emulate the typical paper tape reader/punch and perform the functions of program load, data logging, assembly, edit or duplication. Select one of two Texas Instruments Silent 700® modes, and tapes can be written, read, or copied that are completely compatible with the 733ASR but at much higher data rates.

With its extension connector, the Model 6801 can be connected to any RS232C port without disturbing the device formerly connected there. With this feature, for example, tape storage can be added where only hard copy print out or CRT display had previously existed.

Utilizing two of Raymond’s time-proven 6406 Raycorder cassette drives, the Model 6801 provides the ultimate in a reliable, flexible data storage and handling device for a multitude of applications. Detailed specifications will be provided on request.

For the OEM
Raymond’s small tape drives, long the standard of the industry, are now available with all new electronics that make interfacing a cinch.

Model 6406 for Philips Cassettes, redesigned with many new features at a lower cost.

Model 6409 for Mini-Data Cassettes, now has a parallel interface and other changes you’ll appreciate.

Model 6413 for ¼-inch Data Cartridges, the newest member of the team is catching on fast.
functions. All macros incorporate series-gated ECL structures, full adders, quad latches, and many other predefined structures for optimized performance. Presently 85 different macros take the form of standard logic elements such as dual type D flipflops, dual full adders, quad latches, and many other predefined functions. All macros incorporate series-gated ECL structures for optimized performance. Presently 85 different logic functions make up the library.

To generate an LSI design, the designer need only select the appropriate macros from the library, assigning these to the desired cell locations, and creating the necessary cell interconnecting pattern. The computer itself generates the proper interconnecting pattern within each cell. This computer aided design approach, operated via standard timesharing terminals, greatly speeds up the circuit development while simplifying the designer/manufactuer interface. It serves to design the interconnects, to check out the performance of the designs, and to generate the custom metal patterns that complete the IC processing sequence.

Compared with the conventional approach to custom LSI circuits, the concept offers a considerable reduction in delivery time. With a stockpile of fully diffused and tested wafers, turnaround time (from the time the customer gives the go-ahead signal for generating the metal mask until finished parts are delivered) is an anticipated 12 weeks. In comparison with gate arrays, the use of higher component density and more efficiently designed subcircuits (macros) yields a substantial improvement in performance (circuit speed), while a greater utilization of onchip components reduces potential system costs. Compared with equivalent systems developed with discrete logic (separately packaged MSI/LSI logic functions), the high packing density of the array chip offers up to a 50 to 1 reduction in system component count, with a power dissipation reduction of as much as 5 to 1.

Important features of a Microcell array are listed in the Table. The basic chip consists of 106 individual cells: there are 48 major cells, 32 interface cells, and 26 output cells. A half-cell schematic of a major cell shows the unconnected transistors and resistors (Fig 1). Cells within each of these three basic classifications contain identical fixed arrays of resistors and transistors, and all chips are built from a standard diffusion set; i.e., all chips are identical and can be prefabricated, up to the metallization step.

Applications
One of the most important features of the design is the logic flexibility provided by the function library. The system value of the array can be shown by examining possible circuit options.

Fig 2 shows a block diagram of an 8-bit binary/BCD ALU that was designed using more than 96% of all cells in the array. The ALU operations include binary and BCD addition and subtraction, shift left, shift right, increment, transfer, invert, and various logic operations.

Macrocell Array Characteristics

<table>
<thead>
<tr>
<th>Cells</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Major</td>
<td>48</td>
</tr>
<tr>
<td>Interface</td>
<td>32</td>
</tr>
<tr>
<td>Output</td>
<td>26</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Equivalent Gates</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1192</td>
<td>if full adders and latches used in all cells</td>
</tr>
<tr>
<td>904</td>
<td>if flipflops and latches used in all cells</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Dissipation</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>4 W typical for 904 gates</td>
<td></td>
</tr>
<tr>
<td>4.4 mW/equivalent gate</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cell Delays</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface</td>
<td>0.9 ns typ (1.3 ns max)</td>
</tr>
<tr>
<td>Major</td>
<td>0.9 to 1.3 ns typ (1.3 to 1.8 ns max)</td>
</tr>
<tr>
<td>Output</td>
<td>1.5 ns typ (2.2 ns max)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Drive</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>25-0 load on any output cell (to total of 8)</td>
<td></td>
</tr>
<tr>
<td>50-0 loads on all output cells</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Edge Speed</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5 ns typ 20 to 80% (1 ns min)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Macros</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Major cells</td>
<td>54</td>
</tr>
<tr>
<td>Interface cells</td>
<td>14</td>
</tr>
<tr>
<td>Output cells</td>
<td>17</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ambient Temperature Range</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to 70 °C with heat sink and 1000 lpm (linear feet/min) air flow</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thermal Resistance</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>15 °C/W with heat sink and 1000 lpm air flow</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Absolute Maximum Junction Temperature</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tj = 165 °C</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage Compensated</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ES} = -5.2 V \pm 10%$</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MECL 10K Compatible</th>
<th></th>
</tr>
</thead>
</table>

Fig 1 Half cell schematic (one-half of major cell). Major cells in array comprise internal area on the chip and are used for majority of logic capability. Each major cell contains 52 transistors and 48 resistors. Components are connected together on first layer metal to form logic functions with 4 series-gated structures operating on MECL 10K logic levels.
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(214) 661-0300 (405) 528-6071 (602) 968-5962 (808) 523-1326
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CIRCLE 149 ON INQUIRY CARD
MSB sign protection results on arithmetic shift right, and the overflow output checks for a sign bit change on arithmetic shift left. Three 8-bit independently controlled latches can be used to hold data on any input. The propagation delay for any function from input to output is only 13 ns (max). A 32-bit ALU can be built from four of these arrays, using ripple carry, with a propagation delay from input to output of less than 20 ns.

For larger word lengths, lookahead carry circuits such as the 1C10179 can be used to minimize propagation delays. Typical power of the chip is 4.1 W total, which includes the power of the output transistors driving a 50-Ω load. The total number of equivalent gates using the gate equivalent in the library is 528, for a power dissipation of 7.8 mW/gate (avg).

A 16 x 4 multiport register file is diagrammed in Fig 3. The circuit has two independent address and output ports for reading the contents of the memory. Address access time is only 6.5 ns (max).

**Fig 2** Eight-bit binary/BCD ALU utilizing Macrocell Array. Five function select inputs select 32 ALU operations on three 8-bit input ports, with result sent to output bus either directly or through accumulator for pipelining.
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CIRCULAR 152 ON INQUIRY CARD
Four ICs Execute Data Encryption Algorithm to Safeguard Information

A 4-circuit set of data encryption circuits, based on the FELT™ technology, execute the National Bureau of Standards encryption algorithm, meeting functional requirements specified in the Federal Information Processing Standard publication 46. The devices protect information (links or circuits, based on files) in data transmission systems and high performance peripherals through a virtually unbreakable encryption system.

A pair of data registers, four 8-bit shift registers, control logic, and two 64 x 4-bit ROMs comprise each 9414-1, -2, -3, and -4 circuit. The circuits are available as a set of components or as board level components. Pricing for the 4-piece set of circuits is $100 in 100 to 999 quantities.

A 56-bit key word enciphers or deciphers a 64-bit data word stored in eight 8-bit bytes. Two bits of each byte are distributed to each of the four chips. The 56-bit key word, combined with eight parity bits is also broken down into eight 8-bit bytes. Bits 1 through 4 of each byte go to both chips 1 and 2; and bits 4 through 7 go to chips 3 and 4, with the parity bit fed to one of four chips. Thus, the set stores a 64-bit plain text or cipher text word, as well as the key word.

During data loading, the chip set performs an initial permutation of the input word. The loaded data are split into two blocks, and each byte encounters further permutations through a series of 16 iterations/block of cipher data. There are 72 x 10^13 key variations possible between the permutations of the 64-bit data word and 56-bit key. Deciphering uses the same key word. Access to a file is useless without the key.

Separate data I/Os allow simultaneous input of the data block to be processed with the previous block's output. The system can be implemented within existing data link protocols without modifying word size, since I/O blocks are both 64 bits. Processing of a 64-bit data block in 24 clock pulses makes the chip set potentially the fastest of its kind available, according to the Microcomputer Group of Fairchild Camera and Instrument Corp, 464 Ellis St, Mountain View, CA 94042. Throughput rates range up to 13.3 MHz (75 ns)/bit or 200 kHz (4.8 µs)/64-bit word.

Circle 360 on Inquiry Card

High Performance CMOS Amplifiers Employ Unique Circuit Design

A commutating autozeroing technique (CAZ) is utilized in the design of an operational amplifier, which provides a near zero initial offset voltage of 5 µV, 0.1 µV/°C offset drift with temperature, input leakage current of 5 pA, and open loop gain >100 dB. These parameters also characterize an instrumentation amplifier that is based on the same design technique.

Each device consists of two op amps, a set of analog switches, and a digital timing section, all included on a single CMOS chip. Autozeroing capacitors are required to complete the functions—two capacitors in the case of the 14-pin ICL7600 op amp, and four in the case of the 18-pin ICL7605 instrumentation amplifier. These two devices, produced by Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014, are priced respectively at $6.50 and $15.00 each in 100-unit quantities.

The analog switches in one of these CAZ amplifiers are used to connect each internal op amp alternately into either a signal processing mode or into an autozero mode. If one amplifier is in the autozero mode, the other is automatically in the signal processing mode. In autozero, the amplifier stores on a capacitor a voltage value that is equivalent to its noise voltage. Some time later, the amplifier's output and its non-inverting and inverting inputs are reconnected through the analog switches, so that the error voltage stored on the capacitor is added to the noninverting (plus) input, canceling the internal input error voltage of the op amp. The result is that the input signal is continuously processed, while low frequency noise and offset errors of both op amps are monitored, updated, and corrected at the commutation frequency. Offset voltage drift with respect to time and temperature is considerably less than similar effects observed in conventional chopper-stabilized op amps.

According to the manufacturer, the CAZ technique gives the user a...
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CIRCLE 153 ON INQUIRY CARD
designs. Those conventional designs require a fairly complex gain network of external resistors, which must match and track one another for good common-mode rejection. The CAZ instrumentation amp requires only two external resistors to set gain (as is also true of the CAZ op amp), and the common mode rejection ratio (CMRR) of 110 dB is independent of the resistor values. No adjustments other than full scale are necessary to achieve high performance.

Control of device operation is accomplished via the digital section of the chip, which contains an RC oscillator, a frequency divider, a level translator, and an output buffer. The level translator allows use of an RC oscillator, which operates from a low, stabilized supply voltage. Power consumption is low and only minimal supply current transients are present for potential feedback into the analog section. The oscillator provides an output of about 10 kHz, and through addition of external capacitance, can be programmed to operate at any lower frequency. A ratio terminal permits the user to change the divider ratio to produce several options, from freerunning at any reasonable commutation frequency (10 to 500 Hz) to full lock to an external clock such as the master clock of an integrating ADC.

"virtually ideal" amplifier. There are no requirements for trimming or selection during manufacture, as compared to currently available devices, which require either special processing and/or careful selection to achieve comparable performance.

Other characteristics include a low noise voltage (3 µV pk-pk over a 0.1- to 10-Hz frequency range) and low noise current (1 pA pk-pk over the same frequency range). Low frequency temperature effects are correctable by the commutation circuitry. Long-term drift is fully compensated and, at ~0.1 µV/yr, is negligible.

The instrumentation amplifier is intended to replace the classic 3- or 2-op amp instrumentation amplifier

Fast Monolithic 10-Bit D-A Converter Features ±1/2 LSB Linearity

Bipolar monolithic technology and TTL/CMOS compatibility are features of a D-A converter that is characterized by a 10-bit resolution and ±1/2 LSB worst case linearity error. DAC-IC10B, produced by Datel Systems, Inc, 11 Cabot Blvd, Mansfield, MA 02048, requires only an external reference and operational amplifier for voltage output operation. A full-scale change in output current settles in 250 ns, and with a fast ic op amp (such as AM-452 by the same manufacturer), a 10-V output change can settle within 1 µs. Digital input coding is straight binary for unipolar operation and offset binary for bipolar operation.

This circuit incorporates 10 fast switching current sources which drive a diffused resistor R-2R network. 

DAC-IC10B (BM) from Datel is 10-bit monolithic DAC. Featuring ±1/2 LSB linearity, device settles in 250 ns. Fast current switches drive diffused resistor R-2R ladder network, which is laser trimmed through cutting aluminum links.
Other people make them, of course. But you can't get them in volume. Unless you're willing to wait a very long time. And in this business a printer you can't get is about as useful as all those wonderful products that haven't been invented yet.

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The ladder network is laser trimmed by cutting aluminum links. A reference control amplifier and a bias circuit are also included in the converter. An external reference current of 2 mA is required at the positive reference input terminal; this is accomplished by an external voltage reference and a metal film resistor.

Additional characteristics include ±18 ppm/°C gain tempco, with monotonicity guaranteed at room temperature (25 °C). The gain tempco is 20 ppm/°C. Output current is 0 to 4 mA and output voltage compliance is −2.5 to 20 V, permitting direct driving of a 625-Ω resistor for a voltage output. The reference input current can be varied from 0.5 to 2 mA to give monotonic operation as a one or two quadrant multiplier. Other applications include digitally controlled attenuators, display systems, computational circuits, and automatic test circuits.

These converters combine operating flexibility and speed with low cost. They are available in both a commercial version (operating over 0 to 70 °C and priced at $14.50 in 1 to 24 quantities) and a military version (operating over −55 to 125 °C and priced at $27.50 in 1 to 24 quantities). Both are monotonic over the operating temperature range. Power supply requirement is 5 V at 18 mA and −15 V at 20 mA.

Maximum ratings limit V\text{CC} to 7.0 V, V\text{EE} to −18 V, and digital input voltage to 15 V. The output voltage (pin 3) must lie between 0.7 and −5.0 V. Reference current must not exceed 2.5 mA nor reference differential input exceed 0.7 V.

Circle 362 on Inquiry Card

Schottky ECL RAM/Register File
Has Dual Output Ports

A 16-word by 4-bit monolithic random access memory/register file utilizing Schottky emitter coupled logic features two separate output ports, enabling any two 4-bit words to be read simultaneously from the outputs. Each output port contains a 4-bit latch, and a common latch enable (LE) input is used to control all eight latches. This device, which has two write enable (WE) inputs, is designed so that LE and either WE can be wired together to make the operation of the RAM appear edge triggered.

IDM29705A is a selected high-speed device having an access time of 25 ns, in contrast to a 53-ns access time for the standard 29705. National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051, which provides the standard device on a second-source basis, is the sole source for the A version.

Having fully decoded A address and B address fields, the device can address any of the 16 memory words for the A output port and simultaneously select any of the 16 words for presentation at the B output port, with incoming data written into the 4-bit RAM word selected by the B address. Data accessed at the A address port appear at the A output port, and data accessed at the B address port appear at the B output port. The D inputs are used to load the new data into the device (see Diagram).

Several of these devices can be cascaded to increase the total number of memory words in the system. Tri-State™ outputs are provided, and when OE-A is high, the A output port is in the high impedance mode. OE-B, when high, forces the B output port to the high impedance state.

Writing of new data into the RAM is controlled by the WE inputs. With both of these inputs low, data are written into the word selected by the B address field. The memory outputs follow the data inputs during writing, if LE is high. With either WE high, no data are written into the RAM.

Absolute maximum ratings require that supply voltage (relative to ground) lie between −0.5 and 6.3 V, that dc voltage applied to outputs for high output state lie between −0.5 V and V\text{CC} max, and that dc input voltage fall no lower than −0.5 V and no higher than 5.5 V. The dc output current (into outputs) is limited to 30 mA or less, while dc input current must remain between −30 and 5.0 mA. Storage temperature is constrained to the −65 to 150 °C range, and ambient temperature under bias must stay between −55 and 125 °C.

Hybrid V-F Converters Are Guaranteed Over Wide Temperature Range

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quad op amp operates from single supply voltage

quad operational amplifier lm3900 features current-mirror inputs with noninverting operation. it provides a large output-voltage swing and operates over a supply voltage range of from 4 to 36 v; with a balanced supply, it operates with voltages from ±2 to ±18 v. specs include a low bias current of 30 na, open loop gain of 70 db, 2.5-mhz bandwidth, and output voltage swing of v+ - 1 v. internal frequency compensation and output short circuit protection are included.

texas instruments inc, po box 225012, dallas, tx 75265, intends it as a second-source part for the national semiconductor device with the same designation. suitable applications for the 14-pin plastic or ceramic ddrps include ac amplifiers, ac active filters, and low speed, high voltage logic gates.

circle 364 on inquiry card

lsi optical transceiver utilizes ill technology in detection devices

utilizing linear ill technology, an lsi optical transceiver is designed for use as a proximity detector or small particle sensor in security, industrial, or environmental applications. produced by cherry electrical products corp, 3600 sunset ave, waunakee, wi 60085, the cs-258 has the capability of strobed detection for high ambient light operation plus combined analog and digital noise filtering to eliminate false triggering. onchip features include a 0.5-a led driver, 140-mv receiver, and an output driver. the unit is provided in a standard 16-pin dip.

with addition of an ir led, photodiode, and several noncritical resisters and capacitors, the device becomes a complete optical transceiver system. it includes a 3-pole filtering network on the receiver amplifier, which reduces the response to 120-hz ambient light. this filtering, combined with strobed detection of incoming pulses and multiple pulse integration requiring consecutive pulses for triggering, allows the system to be relatively open to ambient conditions without false alerts.

circle 365 on inquiry card

models 4731/4733 v-f converters from teledyne philbrick are freerunning (astable) voltage controlled multivibrators. effective currents from inputs (a, b, c, and d) are summed at op amp a1. a1 and q1 form precision current pump, producing current i from collector of q1 to charge capacitor c at rate which is precise linear function of input signal. when voltage on c reaches fixed precision threshold, schmitt-trigger output changes state and triggers one-shot (monostable) multivibrator, which produces constant width output pulse. amplified by o2, pulse functionally activates precision charge dispenser (pcd), which discharges c to same zero level every time output pulse is produced and makes operation possible with full-scale input voltages from less than 10 mv to 20 v. its current pin (the summing point of an op amp) resolves currents as low as 1000 pa, which makes operation possible with full-scale input voltages from less than 250 mv to greater than 100 v. nonlinearity is 0.005%, equivalent to 16-bit end-point linearity, while differential nonlinearity and dynamic range approach 20 bits.

guaranteed tempcos for the devices in ppm/°c are 15 (hot) and 25 (cold) for the 4731 and 20 (hot) and 30 (cold) for the 4733. both are offered with 100% screening similar to mil-std-883, method 5008. this screening includes internal visual, stabilization bake, constant acceleration, seal, fine and gross leak, external visual, and, for -83 versions of both models, burn-in and temperature cycling are also included.

circle 363 on inquiry card
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This system is completely compatible with DEC disk-pack media and software such as RT-11, RSX-11, RSTS, MUMPS, etc... but it costs thousands of dollars less. In fact, add-on drives for this system cost half of the DEC equivalents.

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**16-Bit DAC Provides Short Settling Time**
Offering 16-bit, 4-digit resolution, ±0.003% nonlinearity (max), and a gain drift of ±15 ppm/°C or less over a temperature range of 0 to 70 °C, a hybrid d-a converter incorporates fast settling switches, low drift voltage reference, and stable, laser trimmed, thin film resistors. Settling time is 10 µs to ±0.003% FSR. Six models provide a choice of three codes (unipolar, bipolar, bcd), and voltage or current output.

**DAC71 from Burr-Brown**
DAC71 from Burr-Brown, PO Box 11400, Tucson, AZ 85734, provides output voltages of 0 to 10 V (cas and cco) or ±10 V (cas) as well as output currents of ±1 mA or 0 to ±2 mA. Input power is ±15 Vdc (no load) and 5 Vdc (logic supply).

As a current output device, it will drive the summing junction of an op amp to produce an output voltage. The op amp output voltage is the product of the dac's output current and the feedback resistance. Use of an internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

All models are supplied with an internal 6.3-V reference voltage supply. This reference voltage has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a gain drift of ±3 ppm/°C and is burned in for a total of 168 h for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200 µA. An external buffer amplifier is recommended if the dac's internal reference is used externally in order to provide a constant load to the reference supply output.

Digital input specifications for TTL compatible levels call for 2.4 V (min) and 5.5 V (max) for logic 1 at 40 µA. Corresponding values for logic 0 at ~1.0 mA are 0 and 0.4 V. The 24-pin ceramic package measures 1.375 x 0.75 x 0.25" (35 x 19 x 6 mm). It is priced from $39 in 100s.

**Circle 366 on Inquiry Card**

---

**Voltage model of 16-bit DAC71 from Burr-Brown. Hybrid converter features ±0.003% nonlinearity (typ), gain drift of ±15 ppm/°C, and settles in 10 µs (max)**
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You'll find the flexibility you need for virtually any digital data handling requirement. Features like 30 ips read/write, 90 ips search and rewind, read-after-write checking, 800/1600 bpi recording density, and phase or biphase encoding on 1, 2, or 4 tracks. Storage capacity per cartridge is up to 23 million bits. But there's more to this drive's wide acceptance than meets the eye. Features like interchangeable printed circuit boards, long-life motor, and initial low cost have made this unit particularly suitable for small system integration where cost/performance, reliability and serviceability are of utmost concern.

Applications like remote data collection, data communications, word processing, POS, and data entry are just a few ways that these drives are handling data in thousands of systems today.

To get all the facts on the MDS 2021/2022 Cartridge Tape Drive, mail the attached coupon, or call us collect today.

*3M DC300A Data Cartridge

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OEM Division
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Herkimer, N.Y. 13350
East Coast-Contact: H. Johnson (315) 866-5300
West Coast-Contact: J. Engstrom (714) 772-0803

Please send me information on the MDS 2021/22 Cartridge Tape Drive.
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Title
Company
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City ______ State ______ Zip ______
☐ I'm in a hurry. Have a representative call me at: (___) ______

CIRCLE 161 ON INQUIRY CARD
DESTROYING A CIRCUIT IS AS EASY AS WALKING ACROSS A CARPET

Acrylics, wools, silks and moving nyons in a computer room increase susceptibility to static charges. A few steps and a spark from body to computer cabinet is all it takes to produce a charge as high as 30,000 volts. And, if the cabinet and/or components are poorly grounded, the charge can be transmitted to components causing overloading and circuit malfunction.

Metex Shielding Provides Ideal Protection from Low Signal IC Overload

Metex shielding products such as Combo Strip® Gasketing, Xecote® Conductive Coating and Xecon® Conductive Elastomer protect your equipment by shielding it from this predatory energy...keeping it away from digital IC’s and other vulnerable components.

Metex Products Protect Against Unwanted EMI/RFI Too

Viewing screens, air vents, cabinet slots and any other enclosure openings are access points for EMI/RFI energy. Easily picked up by sensitive components by induction, EMI/RFI radiation can cause distortion of low power signals and overloading of subsequent circuits. This may lead to IC degradation, or catastrophic failure.

Metex provides Shield-Vu® Shielded Windows of any size or shape, constructed of finely knitted wire fused between panes of acrylic or glass, that offer effective attenuation with over 90% visibility. We also make air intake and exhaust vents that permit free airflow but are almost totally opaque to EMI/RFI.

Available in configurations to meet your needs, Metex shielding products are produced to the most exacting demands, including France’s CISPR, the German VDE and U.S. IEEE.

Protect your digital IC circuitry. Our staff of applications engineers will assist you now in finding solutions to your present and potential shielding problems. In the East call 201-287-0800, west of the Rockies call 213-320-8910. To write: 970 New Durham Road, Edison, N.J. 08817 or 20437 S. Western Avenue, Torrance, CA 90501

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CIRCLE 221 ON INQUIRY CARD
Ampex disk storage modules are both interface and media compatible with CDC's 9760 and 9762. And Ampex 40 and 80 megabyte SMDs offer a unique advantage over the CDC equivalents—they both can grow to a capacity of 160 megabytes with a simple field modification.

You'll find a lot more than CDC-compatibility when you look into the Ampex storage module family. Ampex can package your drive in rack, console or "Tempest" configuration, and can deliver such desirable features as variable sector format, address mark capability and on-track head servoing. The transfer rate is 1.209 megabytes per second, and access time average is 28 milliseconds.

Other Ampex disk storage modules provide capacities of 100, 200 and 300 megabytes, and within a given family, you can begin with the minimum storage and upgrade to a higher capacity right in your own facility. For those with super special data needs, Ampex even has a 300 megabyte module with a parallel transfer rate of 10.88 megabytes per second.

Larry Russell has the information. Call him at 213/640-0150, and he’ll prove that now there are twice as many ways to get the SMD capacity you need when you need it. Technical information and performance data is complete, and free. Write to Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Immediate delivery is only a P.O. away.
Course 142 — Five days
**Troubleshooting Microprocessor-Based Systems**

**TORONTO**
June 25-29

**SAN FRANCISCO**
July 9-13

**SAN DIEGO**
July 23-27

**MINNEAPOLIS**
July 30-August 3

Nearly all manufacturers, OEMs and end users are suffering from microprocessor bottlenecks and customer service problems directly caused by the unavailability of trained personnel to test and troubleshoot microprocessor systems. This unique course is specifically designed for engineers and senior technicians involved in production testing, field service and design of microprocessor-based systems. The course provides these personnel with the practical knowledge they require, including in-depth understanding of:

- a) microprocessor software and hardware
- b) how to apply the most powerful microprocessor debugging techniques
- c) how to use microprocessor troubleshooting equipment.

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphics systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

- Display Hardware
- Software Structures
- Color Display Techniques
- The Hidden Line Problem
- Two Dimensional Graphics
- The Hidden Surface Problem
- Three Dimensional Graphics
- Software 'Build or Buy'
- Transformations
- Selection Methodology

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensible manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

- An Overview of Applications
- Design Techniques
- Digital vs. Analog Signals
- Computer Aided Design
- Operations on Digital Signals
- Statistical Approaches
- Recursive Filters
- Spectral Estimation
- Nonrecursive Filters
- Application Case Study

---

**Course Hours:**

Orientation (First Day): 8:15 – 9:00 A.M.
Lecture Sequence: 9:30 A.M. – 12:15 P.M.
Informal Discussion Session with Instructor: 1:15 – 2:30 P.M.

**Course Fees:**

**Four-Day Courses:**
365, 350, 320 or 160 $695.00 (U.S.)
142 or 412 $795.00 (U.S.)

**Course Fees Include:**

- Lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
- Team/Group Discount: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

**CONFIRMATION:**

Upon receipt of your course Order Coupon or enrollment by telephone, a complete confirmation package will be forwarded, including course location details and an invoice.

**DIPLOMA/CONTINUING EDUCATION UNITS**

Each attendee receives a Course Completion Certificate awarding one Continuing Education Unit (CEU) for each ten hours of class participation. The CEU is a nationally recognized unit awarded by universities and educational organizations for participation in continuing educational programs.
Course 350 — Four days

**Distributed Processing and Computer Networks**

- **TORONTO**
  - June 5-8
- **HARTFORD**
  - June 12-15
- **WASHINGTON D.C.**
  - June 19-22
- **SAN DIEGO**
  - July 10-13
- **OTTAWA**
  - July 17-20
- **MINNEAPOLIS**
  - July 24-27

This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of the concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

- What is to be Distributed?
- Data Communication Concepts
- The Computation Continuum
- Computer Networks
- Network Protocols
- Database Structures
- Database Requirements
- Security Considerations
- Evaluation and Selection
- Management and Control

Course 320 — Four days

**Structured Programming**

- **CHICAGO**
  - June 5-8
- **TORONTO**
  - June 12-15
- **HARTFORD**
  - June 19-22
- **SAN FRANCISCO**
  - July 10-13
- **MINNEAPOLIS**
  - July 17-20
- **OTTAWA**
  - July 24-27

This course is designed for programmers, software engineers, systems analysts and their managers who are charged with the responsibility of creating and maintaining reliable, complex program structures. Participants will develop a clear understanding of the concepts and applications of structured methodology, and will learn to evaluate various types of structured programming techniques. The course will provide in depth exposure to structured design and structured programming tools and procedures. The underlying theme of the course is the development of skills which will enable the production of structured programs at minimum cost, while planning for program changes, modifications and reducing maintenance costs.

- Analyzing the Programming Function
- Principles of Structured Program Design
- Tools and Aids for Structured Program Design
- Case Study Workshop
- Implementing Structured Coding
- Verification Using Structured Walk-Through
- Developing Structured Systems
- Productivity Management and Project Control
- Organizing the Programming Team

Course 160 — Four days

**Microprocessor Hands-On Workshop**

- **WASHINGTON D.C.**
  - June 4-7
- **BOSTON**
  - June 11-14
- **SAN FRANCISCO**
  - June 19-22
- **HONOLULU**
  - June 26-29
- **SAN DIEGO**
  - July 16-19
- **MINNEAPOLIS**
  - July 24-27
- **OTTAWA**
  - July 30-August 2

This course is intended for engineers, programmers, systems analysts and their managers. It has been found extremely useful by attendees both with or without prior experience in either computers or electronics. In fact, managers who have attended report the course provides a level of familiarity, awareness, and confidence which enables them to better manage their staff in applying microprocessors.

**EACH STUDENT RECEIVES A COMPLETE 8080 MICROCOMPUTER AND INTERFACING SYSTEM FOR HIS PERSONAL USE THROUGHOUT THE COURSE.**

- Microprocessor Concepts and Terminology
- Analysis of Potential Applications
- Microcomputer Hardware Design
- Hands-On Programming Exercises
- Hands-On Interfacing Exercises
- Development Equipment and Software
- Selecting the Correct Microprocessor
- Managing a Microcomputer Project
- How to Get Started
- Future HW and SW Developments

**□ PLEASE ENROLL ME IN COURSE:**

**CITY:**

**DATE(s):**

**MAIL TO:**
Integrated Computer Systems, Inc.
3304 Pico Blvd., P.O. Box 5339
Santa Monica, CA 90405

**OR CALL:**
(213) 450-2060
LOS ANGELES

**OR:**
(703) 548-1333
WASHINGTON, D.C.

A confirmation letter with complete details will be forwarded to you.

Company ____________________________
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Mail Stop ____________________________

Address ____________________________
City ____________________________
State/Province ____________________________
Postal Code/Zip ____________________________
Telephone ____________________________

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Please put me on your mail list to receive future course schedules.

**CIRCLE 160 ON INQUIRY CARD**
FOR OFFICES THAT WANT TO KEEP IT QUIET, THE NEW TALLY HUSH-TONE KEEPS THE LID ON NOISE.

If printer noise disturbs your office serenity, you'll appreciate the mel-low decibels of the whisper-quiet Tally Hush-Tone. Our special acoustically designed enclosure attenuates printing noise level down to an unheard of quiet level. When not printing, the Hush-Tone is totally quiescent.

Available at 125 and 200 lines per minute, the Tally Hush-Tone is easy to live with, easy to operate. And easy on the pocketbook. It's the newest member of the Tally T-2000 series—the most reliable (and lowest cost of ownership) line printers you can buy. Remember, Tally line printers never need adjustments, lubrication nor preventive maintenance. And you can always count on consistent print quality.

The Tally Hush-Tone. You get more than quiet performance. You get up-time performance.

Call or write today. Tally Corporation, 8301 South 180th Street, Kent, Washington 98031. Phone (206) 251-5500.
### Core & Semiconductor Memories

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STANDARD MEMORIES has grown into a new name.

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3400 West Segerstrom Ave., Santa Ana, CA 92704. (714) 540-3605

CIRCLE 158 ON INQUIRY CARD
Use of a precision ball bearing carriage such as that on large discs provides the model 288 double-density, dual-diskette drive with excellent stability in head positioning on both sides of the diskettes. Claimed by PerSci, Inc to be the industry’s first microprocessor controlled diskette drive as well as the first with a dual-head design that lends itself to high yield volume production, this drive has seek speeds 2.5 to 10 times faster than that of standard drives plus twice the data capacity in the same space, but at a per diskette cost competitive with ordinary drives.

Both the two diskettes and the four read/write/erase heads are housed in a casting designed as a direct replacement for the Shugart 850/851. Except for voice coil, the units are pin for pin identical and physically, electrically, and data interchangeable.

**Design Features**

The head of the 288 differs from that of the company’s other drives both electronically and mechanically. Although fully IBM compatible, the head uses straddle erase rather than tunnel erase. However, primary changes in the read/write head are mechanical.

To improve head compliance greatly and to effect high yield production, the company used a combination button/flexure head, an approach that minimized complexity and improved overall design. First, the gimbal was improved to allow greater freedom of movement in both axes. Then a different material and physical configuration was used for the head’s flex cable. This more flexible cable eliminates interference with proper gimbal action. In addition, the precision head assembly maintains an exact relationship between flexure and media, assuring data reliability. Finally, a mechanism has been implemented within the drive body for holding each diskette in a precise plane, maintaining proper contact between the fixed button head and the media. This mechanism also reduces media and head wear by reducing penetration of the button head into the media.
Beehive's Product Line Offers You a Choice!

Beehive International offers you a product line of flexible capabilities, Plus two new choices:

Detachable Keyboard As a Micro Bee Standard

Our New Multi-Page / Editing Terminal, Model DM30

Family Planning At Its Best

Low Cost/Feature Enhancements

MICRO BEE/MODEL DM10 $995
The DM10 is an 8085A microprocessor controlled terminal offering numerous user oriented features, including a line drawing capability to allow creation of graphic displays. The 25th status line is used extensively by the DM10 system firmware to display modes of operation, error messages, communication protocol data and a time-of-day clock as well as a status message showing optional switch configurations.

Flexible Applications Oriented

MICRO BEE/MODEL DM1S $1345
The DM1S is a completely programmable terminal featuring a new design concept of socketed flexibility. The needs of virtually any application can be met with custom generated software or software purchased from Beehive. Emulation packages include DEC VT52*, Microdata Prism*, Data General Dasher*, ADDS Regent 100* and Beehive's DM1A®.

*These names may be subject to trademark claims

Expanded Function Capabilities

MICRO BEE/MODEL DM1A $1395
The DM1A expands Beehive's product line conversation capability by allowing bidirectional, fully buffered communications to an auxiliary device. Communications between the CPU and the auxiliary peripheral device can be transparent to the terminal. Features include non-displayable character attributes enabling selection of seven video levels, a line drawing capability and the ability to enter or receive data in the unlocked portion of the display.

Editing

MICRO BEE/MODEL DM20 $1695
Beehive's DM20 is a buffered terminal designed to address both interactive and batch mode markets. Standard features include bidirectional serial auxiliary port, fixed tabs, clear entry function, descenders on lower case characters, invisible cursor, CPU message deposit, line monitor mode, CPU line lock and transparent printing. An invisible memory address pointer, sixteen function keys and system mode/control keys are very positive enhancements.

BEEHIVE'S NEWEST!

Multi-Page/Editing

MICRO BEE/MODEL DM30 $1995
In addition to incorporating all DM20 features, Beehive's new DM30 provides two pages of display memory, an auxiliary serial interface, and an optional parallel interface. Next page and previous page key lets the user select page boundaries while Scroll Up and Scroll Down permits the user to go across page boundaries in scanning text and editing.

The answer is BEEHIVE

The choice is yours!

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or contact our sales office nearest you.

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EUROPE: Amsterdam, The Netherlands Phone 020-451522

CIRCLE 162 ON INQUIRY CARD

Mr. Duke DeForest, Vice President of Sales for Beehive, invites you to see the entire Micro Bee product line with new detachable keyboard styling at the NCC . . . Booth 2135
Beat blackouts and noise with Deltec's uninterruptible power systems.

The most advanced UPS systems on the market today. When the inevitable brownouts, blackouts or transient noise interrupt your computer or electronic systems, Deltec delivers. Maximum MTBF, minimum MTTR.

700 VA to 37.5 KVA. Single or 3-phase. Deltec systems have proven to be reliable and cost efficient in hundreds of industrial and government installations.

Call us about your requirements. Deltec has a system that will meet your needs without grossly exceeding them. That's what we mean by cost efficient.

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... gives you hard answers on how to solve AC Power problems. Now available at our cost of $3.00. Write or call for a copy.

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980 Buenos Ave., San Diego, CA 92110. Telephone (714) 275-1331

Through use of large scale integration (LSI), it has been possible to place all electronic elements on a single printed circuit board. Both the positioning system and most major drive functions are controlled through an 8048 microprocessor chip; read/write functions are controlled by a company designed LSI chip.

A "slimming filter," used with large discs but not previously on a diskette drive, effects read compensation in double-density. This eliminates the need to implement write precompensation in the controller to achieve high data reliability. That design feature makes the drive more tolerant of diskette imperfections, dirt, dirty heads, and noise, and results in more reliable data transfer. In addition, a pulse width discrimination technique prevents noise pulses from appearing as flux reversals and provides excellent noise immunity.

**Specifications**

Double-density unformatted capacities are 3.2M bytes/drive, 1.6M bytes/diskette, 10.4k bytes/track, with MFM or M2FM encoding. Bit density is 6536 bits/in (2573/cm) and transfer rate is 500k bits/s. (Single-density figures are one-half those of double-density, but with FM encoding.)

Operating times are 10-ms track to track access, 0 settle, 100-ms 76-track seek, and 35-ms head load.

Physical dimensions are 8.72" H, 4.38" W, 15.4" D (22.15 x 11.13 x 39.12 cm). Weight is 22 lb (10 kg). Operating environment is 40 to 115°F (5 to 45°C).

AC power requirements are 50/60 ±0.5 Hz, 90 to 127 V at 0.4 A typical (in 110/115-V installations) and 180 to 253 V at 0.2 A typical (in 200/230-V installations). DC requirements are 24 V ±5%, 5.0 A average, 8.5 A peak; 5 V ±5%, 2.0 A max; and -5 V ±5%, 0.25 A typical.

Reliability ratings are <1 soft read error in 10⁹ bits, <1 hard read error in 10¹² bits, and <1 seek error in 10⁶ accesses. MTBF is >6000 h.

**Price and Delivery**

OEM quantity price for the model 288 diskette drive is $925. First deliveries will begin in June. PerSci, Inc, 12210 Nebraska Ave., West Los Angeles, CA 90025. Tel: 213/820-3764

For additional information circle 225 on inquiry card.
LET'S PUT OUR HEADS TOGETHER.

The Facit 4540 Serial Matrix Printer has already made a name for itself with its standard 250 characters a second - all crisp, full-bodied and perfect throughout the 500 million character service life of the printhead. Versatility comes from the rare 9×9 dot matrix, and the Facit 4540 offers a genuine 100% duty cycle and entire elimination of adjustment and lubrication.

The whole secret is in the unique printhead and its microprocessor controlled impact printing mechanism.

Integration of mechanics and electronics has made Facit peripheral data products world famous.

Facit 4540 extends this tradition. So let's put our heads together. To make your systems more efficient, more competitive and more in demand.

Facit 4540 Serial Matrix Printer with the unique printhead.

Facit-Addo Inc., 66 Field Point Rd, Greenwich, Conn. 06830. (203) 622-9150. Telex 96-5998.

Visit the Facit Exhibit at NCC Booth #1316.

CIRCLE 164 ON INQUIRY CARD
EASY TO PROGRAM ELECTRONIC CONTROLLER HAS 32 PROGRAMMABLE STEPS

Circle 226 on Inquiry Card

FULLY MILITARIZED ECLIPSE MINICOMPUTER MEETS SEVERE ENVIRONMENT APPLICATIONS

The MSE/30, a military specification version of the Data General Eclipse® commercial minicomputer, supports Data General’s multiprogrammed advanced operating system (AOS), as well as the INFOS® database oriented file management system, ANSI standard COBOL, FORTRAN, and PL/1. Capabilities include word, byte, and bit addressing, string handling, and field editing. For floating point operations, a separate extended arithmetic processor operates in parallel with the central processor. High speed cache memory boosts system throughput. Main memory can be expanded from a minimum of 256k to 1024k bytes. A minimum system includes at least a 67M-byte storage module, and up to 545M bytes of online disc storage are available with large systems. Multiprocessor systems and faster character I/O processing can be accommodated and the manufacturer’s Mil-spec peripherals can be added. Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 227 on Inquiry Card

SUBSYSTEM AUTOMATICALLY LOADS FLOPPY DISC MEDIA FOR DATA PROCESSING OPERATIONS

A self-contained automatic floppy disc loader for systems using either open or closed flap 8” (20-cm) discs in either single- or double-density format, the model 1005-1 allows the operator to process a number of discs sequentially without intervention. Input hopper capacity is 50 discs but as the stack decreases, the operator can add more discs to the hopper without stopping the loader. In automatic mode, the input hopper automatically feeds individual discs to a Shugart model SA801 disc drive. After completion of a read or write operation, an eject mechanism automatically places each disc in the output hopper. In manual mode, the operator may elect to sequence individual discs through load and unload cycles. A halt upon reject feature stops the automatic sequencing of discs and sounds an audible alarm to alert the operator that the last disc in the drive was rejected. Media Systems Technology, Inc, 1616 S Lyon St, Santa Ana, CA 92705

Circle 228 on Inquiry Card

For use in developing products or converting existing products to solid state electronic control systems that can perform jobs such as sequencing, timing, level sensing, flow rate, control valve operation, or automated assembly, standard unit has 32 programmable steps, 11 input functions, and 8 outputs, and is expandable to 40 outputs. All units are protected against switch bounce and emi, and have logic circuitry necessary to establish sequence of operation, and device drivers to interface with equipment under control. Timing range of clock and time delays is from 0.2 to 120 s/step. Outputs are rated 2 Adc at up to 50 V each. Dimensions are 5 x 12.5 x 11.5” (12.7 x 31.75 x 29.2 cm). Power requirements are 120 Vac, 50/60 Hz, 50 W. European models are also available. Control Technology Corp, 82 Turnpike Rd, Westboro, MA 01581

Circle 229 on Inquiry Card
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a new era in video display terminals

A programmable terminal for
OEM's and large system users...

A multifunctional terminal for
applications in distributed data
processing and office environments
of the future...

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terminal that offers an intelligent
choice for your special terminal
requirements.

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which combines the latest 16-bit micro-
processor technology with our own
proven video display technology.
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your interests in mind—from data
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emulation) to specific applications
(Text Processing). Then we built in
many special features, and loaded
the DELTA 7000 with memory to
handle your unique applications
programs—at a most attractive price.

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with the new DELTA 7000. Write or
call for more information today.

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CIRCLE 166 ON INQUIRY CARD

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EAD, Holtzer-Cabot and Janette motors

CIRCLE 167 ON INQUIRY CARD

DOUBLE-SIDED, SINGLE-DENSITY FLOPPY DISC SYSTEM

EXORdisk™ III provides a removable media storage capability for EXORciser™, EXORTerm™, and Micromodule™ products. M68SFD1102 and M68SFDU1102E (expansion unit) systems offer storage for more than 1M bytes with the basic unit and over 2M bytes with the addition of an optional dual-drive expansion unit. Each system consists of 2 double-sided, single-density drives in a compact tabletop cabinet, a controller board, and an interconnecting cable assembly from the controller to the disc drive unit. Circuitry is included for head unload timeout, and a write protect feature protects master diskette programs. Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036.
Circle 229 on Inquiry Card

COMMUNICATIONS PROTOCOL DEVELOPMENT SOFTWARE PACKAGE

The GPD (general protocol driver) software package was developed for the Data General minicomputer product line using AOS, RDOS, and RTOS. It operates in the minicomputer or in the data communications unit (a programmable front end). The systems programmer writes a protocol description program in which logic is coded in a macro language that supports the control features of the asynchronous and synchronous line multiplexer interfaces. Macro language allows coding of IBM 2780 BISync protocol in only 200 instructions. A single processor can support 7000 char/s, and asynchronous and synchronous protocols can be mixed in a variety of combinations. Protocol programs are automatically re-entrant. Systems Strategies, Inc, 1250 Broadway, New York, NY 10001.
Circle 230 on Inquiry Card

MINICOMPUTER BASED LABORATORY SYSTEM

A more powerful TP-50 lab computer system, based on a DEC PDP-11/34 minicomputer with 124k words of memory and supported by the RSX11-M software operating system, provides a full range of capabilities in pulse height analysis, instrument control, and general computation. Multiple users can be supported simultaneously, each performing a different task, and can interact with the system via several industry standard programming languages such as FORTRAN and BASIC. A bus translator allows any standard LSI-11 or PDP-11 compatible peripheral to be added to an existing system.

Tennecomp Systems, Inc, 785 Oak Ridge Tpk, Oak Ridge, TN 37830.
Circle 231 on Inquiry Card

CIRCLE 169 ON INQUIRY CARD

COMPUTER DESIGN/MAY 1979
The read-out is quality.

Quality is what has made Zenith famous for over sixty years and number one in the television industry. It's that quality, that commitment to excellence — that insures the reliability of every product we make.

Our manufacturing facilities, laboratories, equipment, procedures, experience and know-how give you the quality and reliability that you look for in a CRT Display. A CRT Display that will hold up under really tough operating conditions.

And to all this, our people add the personal service and special attention you want from your CRT Display source.

**Exhaustive testing**

Our testing insures that every component operates to exacting Zenith standards. Exhaustive computer analysis, electron microscope and thermograph scan tests are only a sample of what we do.

Our environmental lab tests Zenith CRT Displays for thousands of hours under extreme humidity, vibration, altitude and temperature conditions.

Zenith CRT Displays are designed not only to meet our exhaustive testing requirements, but your demanding specifications as well.

**Application engineering**

Every CRT Display we design has our customers in mind. Before our engineers even begin new circuit layouts, we'll meet with you and find out what your exact needs and specifications are.

**Advanced componentry**

Components in the CRT Display are designed with reserve capacity for low maintenance and continued reliability.

The Zenith CRT Display is equipped with a Zenith designed and built deflection transformer. It not only gives a consistent scan, but it is also embedded in epoxy for long-term reliability and the elimination of high frequency squeal.

**Important Zenith Features**

The Zenith CRT Display is precision engineered. No linearity controls are required and the CRT Display's vertical and horizontal synchronization is automatic.

The Zenith CRT Display frame can be adjusted to virtually any angle you want. This will satisfy many customer requirements without having a frame custom designed.

But we do welcome the opportunity to meet all your special requirements.

**Zenith tradition**

At Zenith we'll make sure you get the same service, quality and reliability in your CRT Display that we've been giving our customers for over sixty years.

For further information and specifications, write CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call 312-773-0074.

National Computer Conference, June 4-7, Booth 314.
CIRCLE 168 ON INQUIRY CARD
Basic Micro-Data Network Modules that Offer Total Flexibility, High Reliability and Low Cost, Too!

compunetics, inc. introduces a complete set of computer modules that save you real time in the design of large or small distributed microprocessor systems. Based on the TMS 9900® 16-bit processor, these modules allow a full range of applications - from simple stand alone controllers to large multi-processors - and are compatible with existing systems. All are fully assembled on 4½ x 3½" cards. Fabulous time and money savers!

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CIRCLE 169 ON INQUIRY CARD

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CIRCLE 174 ON INQUIRY CARD

DISC PACK MAINTENANCE UNIT

Designed for visual and mechanical inspection of magnetic discs, the system 340 tester/cleaner/inspector accommodates 6-high IBM 1316, 11-high 2316, and 12-high 3336 disc packs, or their equivalents, through use of interchangeable spindles. Features include instrumentation for the measurement of axial and radial runout, as well as for the mechanical rejection of deflected discs. An adjustable disc surface mirror assembly provides a clear view of both sides of the disc. Visual inspection functions include the detection of dirt, scratches, edge damage, burned oxide, head crash damage, loading marks, and other unacceptable imperfections. The Texwipe Co, PO Box 278, Hillsdale, NJ 07642.

Circle 232 on Inquiry Card

STANDBYLINE Z80 EMULATOR

Model EZ-80 plugs into the CPU socket of Z80 based products to test and troubleshoot both software and hardware, with no restrictions on memory addressing or programming technique. Basic features include easy access to I/O or memory, realtime run, single-step, and dual breakpoints. A 255-word by 32-bit trace memory captures all target program activity for forward or backward review. Contents of 19 CPU registers are available for examination and may be changed to new values at any time. All memory locations and I/O ports are available for examination or modification. True hexadecimal readout of address, data, and register contents use dot matrix type displays for fast, accurate recognition. General purpose built-in system diagnostics include RAM test and ROM/PROM verification tests. Applied Microsystems, 11064 118th Place NW, Kirkland, WA 98033.

Circle 233 on Inquiry Card

MULTICOLOR VIDEO GRAPHICS TERMINAL

Available as a computer peripheral under direct memory access control or for use as a telecommunications terminal through an RS-232 interface, the AED 512 multicolor terminal has up to 8 memory planes that allow 256 simultaneous colors from a pallette of 256 colors to be displayed on a TV monitor. Byte serial hardware interface is RS-232-C or 20-mA current loop, full- or half-duplex, at up to 19.2k baud (selectable at a backpanel thumbwheel switch or the keyboard). Direct video memory access is 8 or 16 bits parallel, on bidirectional 3-state data lines, at data rates up to 500k baud. Complete image transfer to or from terminal requires 0.5 s. Video memory is 16k x 1 MOS organized in 512 x 512 planes. Advanced Electronics Design, Inc, PO Box 61773, Sunnyvale, CA 94088.

Circle 234 on Inquiry Card

CIRCLE 174 ON INQUIRY CARD

COMPUTER DESIGN/MAY 1979
ANALOG INPUT SYSTEM CARDS FOR MD AND 7000 SERIES BUSES

A family of 12-bit data acquisition systems that are backplane and protocol compatible with Mostek MD and Pro-Log 7000 series microcomputer building blocks consists of isolated and nonisolated single-board analog input systems mounted on a 4.5 x 6.5" (11.4 x 16.5-cm) card and operates from the ±12-Vdc present on the bus. Systems are designed for software effective operation with MK3880 or Z80 microprocessors; oncard interface logic provides all needed circuitry for vectored, daisy chained interrupt operation, and includes provisions for accommodating I/O port expansion. Interrupt prioritization, address selection, and expansion enabling of the I/O ports is achieved by jumpering appropriate points on the card for maximum ease of programming.

Data Translation Inc, 4 Strathmore Rd, Natick, MA 01760.
Circle 239 on Inquiry Card

NOISE IMMUNE STEPPER CONTROLLER

Designed for direct connection to a range of microprocessor systems, MPSD-10 operates on the basis of input channel state transitions instead of the traditional pulse train. This eliminates the possibility of positioning inaccuracies caused by electrical noise. The controller permits full-step operation using only 2 logic signals and half-step operation using only 4 logic signals. Power supply overloads are prevented by a circuit that stops adjacent channels from being energized simultaneously. Each channel of the module, which snap mounts conveniently on standard 3" (7.6-cm) track, can be driven from a single, ordinary gate of any common logic family. Duane Elms Associates, Inc, 341 Alpha Pk, Highland Heights, OH 44143.
Circle 236 on Inquiry Card

MODULAR OPTICAL ENCODER

Because R-1500 and R-2000 encoders use a die-cast black anodized solid aluminum base, optical components cannot change position with time. Light source is a single LED, and sensors are on a monolithic IC, with uniform characteristics to eliminate sensor to sensor tempco differences. Models are available for mounting on shafts preloaded in either direction, thus preventing problems with pattern rub-off during axial shaft loading. Input voltages for both range from 4.76 to 5.25 Vdc at 125 mA. Quadrature is 90° ±3° at 5 Vdc and 75 kHz. Output format is a differential sinewave suitable for input to a comparator. Electro-Craft Corp, 1600 Second St S, Hopkins, MN 55343.
Circle 237 on Inquiry Card

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CIRCLE 171 ON INQUIRY CARD

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While your pen plotter is struggling to make one circuit drawing, they get two, three or more.

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Sample plots courtesy of Calma, Motorola and Micro Mask. Shading patterns courtesy of Calma.

See Versatec at NCC
CIRCLE 175 ON INQUIRY CARD
DIGITAL TEST SYSTEM

Inspector 100, a fully programmable digital IC test system, performs both functional and dc parametric tests on devices having from 14 to 24 pins and operating from 4.5 to 5.5 V. Controlled by a 8085 microcomputer system, tester has 32k bytes of memory, dual floppy discs, and built-in 9" CRT and keyboard. Test head accepts personality modules from 14 to 24 pins to automatically configure it to test corner power pin devices. All pin electronics are actively driven. Pragmatic Designs, Inc, 711 Sterlin Rd, Mountain View, CA 94043.
Circle 241 on Inquiry Card

FLOPPY DISC CONTROLLER

FD-100-STD, physically and electrically compatible with the Pro-Log/Mostek Std Bus concept, supports up to 4 IBM std format soft sectored 8 or 5.25" (20.3- or 13.3-cm) floppy discs. Software control allows intermixing of both types of drives. A motor on/off control circuit for minifloppies is provided as a std feature. All disc drive status lines are available to the host processor. I/O port selection is miniswitch selectable. Applied Micro Technology, Inc, PO Box 3042, Tucson, AZ 85702.
Circle 242 on Inquiry Card

STATIC MEMORY TESTERS

RAM CHEK testers administer pass/fail tests to all locations of device under test in <0.2 s. The 2102 tests 2102 type 1k static memories. Test procedure consists of plugging device into socket on instrument and pushing button. If green LED on the panel lights, all storage locations have passed test; if any location is inoperative, the test cycle stops and a red LED lights. Soft failures may be detected by continuously recycling test procedure. Reliability, Inc, PO Box 37409, Houston, TX 77036.
Circle 243 on Inquiry Card

64k MEMORY FOR H11 MICROCOMPUTER

Designed specifically for Heathkit/Digital Equipment H11 and DEC LSI-11/2 and PDP-11/03 microcomputers, CI-1103 is available as an 8k x 16 dual-width board using 200-ns 4027 4k x 1 dynamic devices, or 32k x 16 dual-width board using 200-ns 4116 16k dynamic devices. Unit plugs directly into computer and offers either onboard distributed refresh or external refresh control logic. Data access time is 300 ns and cycle time is 525 ns. Chrislin Industries, Inc, Computer Products Div, 31312 Via Colinas, #102, Westlake Village, CA 91361.
Circle 244 on Inquiry Card
Model MM-8080B, with 8k bytes of core memory and 8k or 16k bytes of ROM on the same module, is designed for nonvolatile storage with Intel's Intellec MDS and SBC 80/05, /10, /20, and /30 microcomputers. It is plug compatible with Intel's Multibus™ and is a direct replacement for the SBC 406, 416, and 016. It also can be used with computers from other manufacturers that offer SBC 80 compatible products. Internal power monitoring circuits protect data in core from power failure or during on/off conditions. No battery backup or special circuits are required for power supply sequencing. Portions of the core memory may be write protected in 1k increments up to 8k and are switch selectable. Micro Memory, Inc, 9438 Irondale Ave, Chatsworth, CA 91311.

Circle 245 on Inquiry Card

840-W HIGH EFFICIENCY SWITCHING POWER SUPPLY

JF750P series fan cooled switchers for either 208-Vac or 115/230-Vac nom operation at 47 to 63 Hz are available in 2-, 5-, 12-, 15-, and 24-V output (=10% adjustable) in current ranges from 180 to 35 A. Output power is rated up to 840 W, depending upon output voltage and current. Features include overvoltage protection, remote sensing, thermal shutdown, reverse voltage protection, paralleling capability, and an efficiency up to 83%. Options such as SCR crowbar protection, power fail, remote programming, and margin switch are available. Regulation is specified at 0.1% for any combination of line and load conditions, and ripple is 10 mV rms max, 50 mV pk-pk max. Holdover storage is >60 ms after input is removed. ACDC Electronics, Div of Emerson Electric Co, 401 Jones Rd, Oceanside, CA 92054.

Circle 246 on Inquiry Card

ALPHANUMERIC AND GRAPHICS CRT CONTROLLERS

EXO-2480, a single-board video interface between EXOR-ciser bus microcomputers and a standard TV monitor, provides 96 ASCII characters with descendents plus 32 graphic symbols in one 24 x 80 page or two 24 x 40 pages. Features include normal or inverse video, with or without blink, synchronized internally or from an external source. EXO-512, a complete graphics controller, provides a 256 x 512 horizontal display or 2 independent 256 x 256 images; 4-level gray scale is obtained by combining images. Both boards can be used as master or slaves in an alphanumeric/graphics application; by adding a second EXO-512, an image containing 4-bit pixels is produced. Matrox Electronic Systems Ltd, 2795 Bates Rd, Montreal, Quebec H3S 1B5, Canada.

Circle 247 on Inquiry Card
PROGR~MMABLE
PULSE GENERATOR
PX32 is a fully programmable pulse generator featuring repetition rates to 20 MHz and amplitudes to 25 V (with option G). Rise time at min settings is <5 ns. Repetition rate, delay, width, rise and fall times, offset and amplitude are all programmable using an IEEE-488 bus. Trigger mode, gating, pulse pair, and polarities of both output pulse and offset are programmable with the bus. Each function has a unique address allowing the pulse output to be modified without reprogramming all functions. Tri-Phenix Electronics, 15823 S San Pedro St, Gardena, CA 90248. Circle 248 on Inquiry Card

PASCAL COMPILER FOR
ECLIPSE MINICOMPUTERS
A PASCAL compiler for Data General's multiuser, multitasking advanced operating system (AOS) running on the Eclipse line of computers, AOS PASCAL can shorten program development time in production and research facilities, and open possibilities for online programming instruction. Developed from the University of Lancaster's RDOS implementation of the P4 standard of PASCAL, package includes source code and binaries on 9-track, 800-bit/ in. (314/cm) magnetic tape. Gamma Technology, Inc., 2452 Embarcadero Way, Palo Alto, CA 94303. Circle 249 on Inquiry Card

HOSTILE ENVIRONMENT
CARTRIDGE RECORDERS
CR300 is designed to meet requirements of MIL-E-16400/-5400/-4158. The recorder features a sealed environmentally secure Super-Pak cartridge that houses a std completely interchangeable DC-300A cartridge. The unit offers 30-in (76-cm)/s read/write, and 90-in (228-cm)/s search/rewind. Capacity is 23M bits/cartridge. ANSI/ECMA compatibility; 1-, 2-, or 4-track serial or parallel recording; and transfer rates up to 192k bits/s are std. Millipak Corp, 9 Fairchild Ave, Plainview, NY 11803. Circle 250 on Inquiry Card

HIGH PERFORMANCE
CASSETTE TAPE SYSTEM
Model 374 includes an Intel 8085A microprocessor controller and std RS-232-C communications interface with switch selectable rates from 110 to 19.2k baud. Optional I/O ports allow inclusion of low speed peripherals. Using std Philips digital cassettes, the unit reads and writes digital data in both Diphase and ANSI formats. Rugged transport design incorporates 4 separate dc motors that accomplish all tape loading, positioning, and movements. Dicom Industries, Inc, 715 N Pastoria Ave, Sunnyvale, CA 94086. Circle 251 on Inquiry Card

The Most Comprehensive Software System Available for Microcomputers.

Our PANA/BASIC Software is the most comprehensive operating system available for microcomputers. It combines the power of ANSI COBOL file processing with the flexibility of a multiuser interactive operating system enhanced by the programming simplicity of BASIC. The result is a powerful yet simple system, which is ideally suited for handling a variety of functions such as: small business accounting, word processing and text editing, inventory control, media conversion, engineering/scientific analysis and interactive software development. Our PANA/BASIC System offers you microprocessor software:

- Multiuser capability
- Powerful string handling
- Time-shared multi-terminal operation
- Interactive data entry and control
- Quick response times
- COBOL style format edit control and string match
- Multiuser file protection
- File capabilities equivalent to ANSI COBOL
- AND MANY MORE

The system is available for a variety of microprocessors including Intel 8080/8085 and Zilog Z80.
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Decitek Standard Floppy Disk Drive uses 8" removable diskettes single-sided, single or double density recording. 48 TPI, industry compatible formats. Dimensions: 8½" wide x 4¾" high x 14" deep.

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Decitek, 129 Flanders Road, Westboro, Massachusetts 01581.

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CIRCLE 180 ON INQUIRY CARD
**EPROM PRODUCTION TESTER AND DUPLICATOR**

Designed to detect poorly erased or static damaged EPROMs, UPP-2700 evaluates all EPROMs both before and after programming. By pressing a single key, the 8048 processor tests and duplicates 16 2708s in <200 s. Solid state audio beeper informs operator of incorrectly inserted devices or test failures. A 40-pin personality module contains programming and test algorithms for generic EPROM families, including 2704, 2708, 27L08, TMS 2716, I2758, I2716, TMS 2516, TMS 2532. Oliver Advanced Engineering, Inc, 678 W Wilson Ave, Glendale, CA 91203. Circle 252 on Inquiry Card

**SELF-CONTAINED SUBREGULATOR MODULE**

Providing a -5-V at 600-mA regulated output from any -7 to -30-V source, AR5-06/VDP connects to negative output of multiple output power supply to provide additional -5-V output required by microprocessors. Unit mounts within the original outline dimensions of any of the company's open frame supplies; all mounting and interconnecting hardware are provided. Output specs yield regulation characteristics of 1% for line and load, and output ripple of 5 mW. Power-One, Inc, Power-One Dr, Camarillo, CA 93010. Circle 253 on Inquiry Card

**MICROCOMPUTER PROTOTYPING SYSTEM**

A Eurocard width (100-mm) universal prototyping card for microcomputer and other bus oriented designs, LP-12U accommodates a dense mix of DIP ICs of all sizes. Holding 20 16-pin DIPs, the 4 x 6" (10 x 15-cm) board has 60 gold-plated edgeboard connector fingers at each end for up to 120 offboard connections. Cards can be interconnected without chassis wiring using a generalized motherboard. Motherboards are available for openframe mounting or for use with card cages. Cybertek, Inc, PO Box 3467, Seminole, FL 33542. Circle 254 on Inquiry Card

**100-ft³/min AXIAL FLOW FAN**

Model 320, measuring 4.6" sq x 2.3" deep (11.7 x 5.8 cm), delivers 100-ft³ (2.83-m³)/min free air at zero static pressure. Rugged 1-piece metal frame eliminates warpage and breakage; a Celcon plastic fan adapts the unit to high temperature environments. Powered by quiet, impedance protected, UL listed motor, fan weighs 1.25 lb (0.56 kg). Hi-Tech Inc, 3600 16th St, Zion, IL 60099. Circle 255 on Inquiry Card
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THE FIRST REAL TIME IN-CIRCUIT DEVELOPMENT SYSTEM FOR ALL BIPOLAR PROCESSORS.

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P.O. Box 61166, Sunnyvale, CA 94088

STEP-2'S REAL TIME (45 ns) RAM MEMORY simulates the system control store for fast trial of object code. Word widths from 8 to 96 bits can be efficiently achieved and memory reconfiguration can be accomplished in seconds. You can emulate two independent memories simultaneously for multiprocessor or unique architecture systems.

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STEP-2'S WORD ORIENTED EDITOR simplifies locating and patching problems in your code. Features include octal or hex representation, binary readout and easy word/bit modification. Blocks of code can be moved in memory to insert additional lines or save a routine before editing. And our search command can locate all instructions containing a specified field or bit pattern.

STEP-2'S DIAGNOSTIC FACILITY speeds debug. Direct control of processor HALT, RUN, STEP, CYCLE, and RESET is accomplished through the keyboard. Real time break points/triggers can be set without disturbing processor activity. Breakpoint state and processor activity is displayed on the CRT, allowing you to quickly verify processor operation.

STEP-2 IS COMPATIBLE WITH YOUR EXISTING SOFTWARE. A full range of serial communications options makes it simple to connect to any computer system from a large computer, timesharing service or an Intel® Development System. Downloading your existing object code takes only minutes using either STEP-2's generalized PROM I/O routine (GENPROM)™ or word-oriented I/O routine (MICROWORD)™.

STEP-2 HAS COMPLETE SOFTWARE SUPPORT. Our Transportable Meta Assembler, (TMA), is completely compatible with AMDASM and can be installed on an Intel® Development System or 16 bit (or larger) computer with Fortran. The TMA is easy to understand and use — powerful conditional assembly statements and cross reference tables simplify code generation. The assembled code can be downloaded directly into STEP-2 for testing and verification.
Here's low cost, high performance Zilog Z80A emu- lation for your Intel development system

Only RELMS offers you the powerful Z80 in-circuit emulator (SPICE) and the Z80 system adaptor module (SAM) for hardware and software development. And only RELMS gives you such price/performance value. The complete Z80 SPICE is priced as low as $2,695; RELMS Series II is only $1,695.

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RELMS
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CAMAC-GPIB INTERFACE
Model 9001 allows CAMAC instruments to operate as standard listeners and talkers on any IEEE Std 488-1975 bus. Program instructions from any GPIB controller to the interface select an individual instrument module within a CAMAC crate, select any subaddress within that module, and establish the read, write, or control function. A crate of up to 23 individual modules is handled in the same manner as an ordinary single device connected to the bus. LeCroy Research Systems of California, 1800 Embarcadero Rd, Palo Alto, CA 94303.

EXORCISER COMPATIBLE 16k STATIC RAM MODULE
A 16k-byte static random access memory module, the 9627 is configured as 2 independent 8k blocks which can be individually placed at any 8k boundary in the memory map. Std configuration has 480-ns access time; 9627A, a 300-ns version, and 9726B, a partially populated version, are available on special order. Creative Micro Systems, 11642-B Knott Ave, Garden Grove, CA 92641.

ANSWER/ORIGINATE ACoustIC COUPLER
Operating at 300 bits/s, AC-312 coupler is Western Electric 103 compatible and is switch selectable between originate and answer modes. When in answer mode, unit generates answer tone necessary to communicate with 300-baud originate-only couplers and modems. Modulation is phase coherent frequency shift keying. Transmit output level is -18 dBm ±2 dB and receive sensitivity is -45 dBm ±2 dB. Carrier detect delay is 150 ms (on), 50 ms (off). Digicom Data Products, Inc., 1140 Koli Cir, Suite 108, San Jose, CA 95112.

310 CIRCLE 183 ON INQUIRY CARD
by beating their price/performance up to 50% with a complete family of µP Disc & Tape Controllers you slip into ONE SLOT of your PDP* /LSI-11*

Presently, Dilog (Distributed Logic Corp.) is the only firm offering you single board Disc and Tape Controllers for the PDP* & LSI-11*

... either as individual modules or as subsystems, complete with drive.

COMMON FEATURES of Dilog Disc and Tape Controllers: single quad size board fits one slot of your computer—no external power or chassis...just a cable to connect the drive—you don’t need anything else! The low cost simple designs employ proprietary sophisticated bipolar µPs so you benefit with: • increased reliability • automatic self-test including error data entry protect and indicator • data transfer busy LED indicators • running of standard DEC or Dilog supplied diagnostics from computer without tricks or gimmicks of any kind • compatibility with all existing standard software.

TAPE CONTROLLERS supplied by Dilog replace the TM11*, for TU10* /TS03*, and interface all industry standard drives. They support both 7 and 9 track 1/2-inch standard tape drives with 7, 8½ or 10½" reels, at speeds up to 112.5 ips.

PDP-11 µP TAPE CONTROLLER, Model DU120 emulates the TM11* and offers you a 30-50% cost advantage when used with an industry standard drive.

LSI-11 µP TAPE CONTROLLER, Model DQ120 does not currently have a DEC counterpart, so this controller offers every advantage and makes tape drives economically practical.

DISC CONTROLLERS produced by Dilog support all 2.5, 5, and 10 and 20MB drives.
Lots of manufacturers offer vanilla terminals that meet their specifications. And, in lots of applications, that may be all you need. But, if you're a design engineer with a tailored system in mind, why sacrifice it to comply with your CRT's limitations? You do have an alternative. Ann Arbor sells user-defineable terminals.

We take a standard CRT design (ours or one of the vanilla manufacturer's), and add the extra function keys you want...delete the features you don't use...vary the display configuration...match the packaging to your user's environment. In short, we fit our terminal to your systems design.

All at a surprisingly low cost to you!

So if you're in the market for CRT displays, and vanilla isn't your favorite flavor, contact us at 6107 Jackson Road, Ann Arbor MI 48103. Tel: 313-769-0956 or TWX: 810-293-6053.

When An Off-The-Shelf Display Terminal Just Won't Do...

...CALL ANN ARBOR!

Ann Arbor TERMINALS, INC.

CIRCLE 186 ON INQUIRY CARD

An acoustically coupled modem, the 30-32 plugs into a page printer data terminal or CRT and accepts a standard telephone handset in rubber caps mounted on its top. A remote computer can then be linked by a standard telephone line to the terminal. Data are transmitted between computer and temporary telephone hookup via voice frequency tones acoustically coupled to the telephone microphone and earpiece. Units provide Bell System 103/113 compatible, full- or half-duplex, 300-bit/s data communication over conventional dial telephones. Datec, Inc., PO Box 839, Chapel Hill, NC 27514. Circle 260 on Inquiry Card

CIRCLE 185 ON INQUIRY CARD

PORTABLE ACOUSTIC MODEM

Cost Effective ASR For Your Terminal...

...NOW!

DSI's LRP-300 Reader/Punch Combo adds 300 baud ASR storage and edit capability to any RS-232 or TTY current loop terminal. Just plug in between terminal and modem and you're ready to go. Our whisper quiet field-proven MODUPERF system is backed by a one year warranty. At only $1395, the system pays for itself by improved accuracy, data throughput, and reduced line charges in a matter of months. Don't wait to go ASR. Order your LRP-300 and start saving line costs NOW. DEALER INQUIRIES INVITED.

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CIRCLE 187 ON INQUIRY CARD

PRODUCTS

COMPONENT LEVEL VOLTAGE TO CURRENT CONVERTERS

Designed to provide 4- to 20-mA outputs with 0- to 1000-Ω grounded or floating loads, model 2B20, a nonisolated version, accepts a std 0- to 10-V input, and features linearity as low as ±0.005% max (B grade) and ±0.025% max (A grade), span drift of ±0.005%/±C max, and op temp range of -25 to 85 °C. Model 2B22, an isolated version, accepts input ranges of 0 to 1 and 0 to 10 V and is available in J, K, and L grades, featuring a high CMR input to output isolation of 2500 Vdc continuous. Analog Devices, Inc., Rt 1 Industrial Pk, Norwood, MA 02062. Circle 261 on Inquiry Card

HIGH AMPERAGE SUBMINIATURE FUSES

Rated at 20, 25, and 30 A, and for operation at 32 V or less, picofuses measure 0.13" (0.33 cm) in diameter and are 0.31" (0.79 cm) long. They are available with radial or axial leads 1.5" (3.8 cm) long and 0.04" (0.10 cm) in diameter. Devices will withstand vibrations of 10 to 2000 Hz at 20 G per method 204A, test condition D, of MIL-STD-202. Operating ambient temp range is from -55 to 125 °C. At -55 °C current carrying capacity is 110% of rating. Littlefuse, Inc., 800 E Northwest Hwy, Des Plaines, IL 60016. Circle 262 on Inquiry Card
When you integrate hardware and software, "act 1 solves your time problem."

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- Reduced Software Debug Time
- Timely Development and Production

The easy-to-use "act 1" makes short work of that frustrating and costly problem of overall systems analysis. It puts an end to finger pointing by giving both hardware and software designers a fast way of coordinating their work in the system environment, thereby reducing expensive over-design of both equipment and programs. You can inspect, modify, and correlate computer and computer controlled systems in real time... and more importantly your development program will be "on-time."

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Delta handles more over-the-counter shipments of 50 lbs. or less than any other certificated airline. And DASH (Delta Airlines Special Handling) serves 86 U.S. cities plus San Juan. Any package less than any other certificated minutes at cargo terminals. Special Handling) serves 86 acceptable. DASH packages accepted over-the-

Delta is ready when you are


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PRODUCTS

CARD READER FOR LSI-11 MICROCOMPUTER

A 300-card/min, 80-col card reader for the DEC LSI-11 and PDP-11/03. CR 300/21 is compatible with Digital Equipment’s CR 11 hardware and software which operates on medium and large PDP-11 systems. The reader includes a vacuum feed reader mechanism, case work, electronics, interface cable, and a dual size module that mounts in one-half quad slot. Cardamation Co, 9A, Frazer Mall, Frazer, PA 19355.

Circle 263 on Inquiry Card

LED RETRORELECTIVE SCANNER

Designed to sense a retroreflective target and ignore other reflective objects passing between the scanner and target, the S22004 Retro-Skan scanner and retroreflector provides positive detection for objects as reflective as polished metal at distances up to 20” (50.8 cm). Unit consists of invisible-IR LED, silicon photosensor, special lens, and ambient light filter sealed in a piece, machined aluminum body. It operates with steady state dc power or with modulated and pulsed controls.

Skan-A-Matic Corp, Rt 5 West, Elbridge, NY 13060.

Circle 264 on Inquiry Card

PROGRAMMABLE 30-MHz MOS/CCD DRIVER

PI-454, compatible with Tektronix TM-500 series power modules, converts a TTL input signal into a ±15-V, 50-Ω output signal for driving MOS type devices at clock rates of ~30 MHz. Output high and low levels are independently manually adjustable or voltage programmable from 15 to -5 V and from -15 to 5 V, respectively. A digital programming option is available, and output high or low level may be manually set to ground. Pulse Instruments, 1536 W 25th St, San Pedro, CA 90732.

Circle 265 on Inquiry Card
Bill Greene, Staff Engineer  
Process Computer Systems Group  
Chemicals & Plastics Division Engineering  
Union Carbide Corporation

Bill Greene is a staff engineer for the Process Computer Systems Group which is responsible for designing, building, testing and installing process control computer systems in the company's manufacturing plants.

Because of their experience, we gave them our new Classic 7860 super mini to test. Their experience with it was summed up in three words. "We love it."

"It's a reliable machine. And reliability is the name of the game."

"We'll trade performance for reliability anytime," said Bill. "But with the Classic, we don't have to.

"The Classic hardware is very solid. Especially for a new product. "The performance characteristics of the Classic are impressive, too. With its extremely fast floating point processor, the Classic can run through a program more than 3.7 times as fast as a MODCOMP II."

"A working computer with software that doesn't work is useless."

"We've been running the MAX III operating system for five years and the MAXNET III network extension for the past two years. They've performed well under very demanding conditions. In fact, over the past year, we've had more than 99.5% uptime on more than 30 installed MAX III systems.

"However, we're installing larger process computer networks now with more and more satellites. So we need increased host computer hardware and software capabilities.

"Our tests with MODCOMP's enhanced MAX IV operating system in the Classic have been very encouraging.

"MAX IV and the new MAXNET IV will help us relieve bottlenecks so that we can add more links and do more work with the computer. We also expect that File Manager, which can create a new file anywhere on a disc, will be a useful tool.”

"We install 15-20 systems a year, so ease of implementation is important."

"Even though the Classic is a powerful and sophisticated machine, it should be an easy system for our project teams to implement. MODCOMP provides plenty of documentation and they've always been very helpful in working with us to get our systems up and running.

"In fact, we think so highly of MODCOMP and the Classic, we've already ordered two MODCOMP Classic 7860's to be used as host computers in large process control distributed networks."

"It takes a tough computer to satisfy a tough customer."

At MODCOMP, we specialize in building real-time computers. They work in chemical plants. In petroleum refineries. In steel foundries. In jet propulsion labs. In electric power plants. In some of the harshest industrial environments you can imagine. Nevertheless, independent surveys have rated MODCOMP computers the most reliable systems on the market.

If you want reliability, but you don't want to trade performance to get it, do what Union Carbide did. Buy a MODCOMP Classic.
COMPUTER GRAPHICS SYSTEM DESIGNER

Challenging career opportunity for aggressive, "shirt-sleeves" system designer with computer graphics group. We are building capability to support design, documentation, manufacturing and field service graphics requirements. The technical effort includes:

- Development and integration of a local, branching network
- Design and implementation of a distributed operating system to synchronize transaction steps through the many network nodes
- Design and implementation of a very large distributed data base
- Integration of this system with many different turnkey graphics systems
- Integration of this system into the user community

MS in Computer Science, Electrical Engineering or Mathematics (or equivalent) preferred. Experience with digital communications, CAD systems and/or approximately 7 years experience with scientific/real time interactive systems.

Please send resume, including earnings record, to William Crocca, Xerox Corporation, Building 128, 800 Phillips Road, Webster, New York 14580.

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- Accepts SYNC, ASYNC, BISYNC, HDLC, SDLC protocols
- Interfaces TTL, RS232, Current Loop, Telex, TWX
- Modules field replaceable for low MTTR
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- Built-in Modems available up to 2400 BPS
- Lowest cost per port in the industry
- Terminal Cluster Concentrators

More Than 1,400 Systems Installed

CIRCLE 190 ON INQUIRY CARD
Sundstrand’s continued growth through product expansion and market penetration has created these challenging opportunities.

CIRCUIT DESIGN
Digital and analog circuit design for aircraft and industrial control systems.
Advanced circuit design of aerospace power conversion systems.

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Analysis and design of system requirements for 400 cycle power systems. Will be responsible for system characteristics, protective functions, and direction of system testing.

PACKAGING
Packaging of electronic components for aircraft control and secondary power systems for military and commercial requirements. Responsibility runs from schematic through qualification.

ELECTRIC MACHINERY
Design and development opportunities available for engineers with high performance generator design experience. Responsibility encompasses preliminary design through production deliveries.

TEST FACILITY
Analog — Engineers to design test stands and associated electrical electronic controls and data acquisition systems. Experience in solid state closed loop analog control systems is desired.
Digital — Engineers to design the hardware and software of digital computer based equipment used in the testing of high speed rotating machinery and mechanical actuating equipment. Experience in assembly and Fortran programming of minicomputers is required.

MANUFACTURING ENGINEERING
Productivity and value engineering for electronic packaging of control systems. Review new product designs, and coordinate production methods recommendations with manufacturing, assembly and engineering.

ELECTRICAL ASSEMBLY
While experience with rotating electrical equipment is required, specific experience with fractional HP - AC & DC motors and/or aircraft generators is desired.

Sundstrand Corporation’s Advanced Technology Group designs, manufactures, and markets a variety of mechanical and electrical accessory products for advanced military and new generation commercial aircraft.

Sundstrand offers excellent salaries and benefits including an extensive medical and dental plan, a liberal holiday schedule, and educational reimbursement. Both the Advanced Technology Group’s and the Corporation’s headquarters are located in Rockford, Illinois, providing easy access to Chicago and to the recreational areas of southern Wisconsin.

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INTERLOCK LIGHTED PUSHBUTTON ASSEMBLIES
Identical in appearance to other TH series switches, interlock assemblies are available in lighted pushbutton combinations; mushroom caps, key operated, Hall-effect, or oil-tight switches can be obtained on special order. Providing T-1¾ lamp compatibility, devices have double terminals and use metal mounting nuts. Wipe and roll gold-plated-silver self-cleaning contacts enable them to handle loads from low level to full range with min of contact bounce. All types are available 1 to 4-pole, and rated at 5 A, 250 Vac. Unimax Switch Corp, Ives Rd, Wallingford, CT 06492.
Circle 269 on Inquiry Card

TERMINAL CONTROLLER AND DATA CONCENTRATOR
VISTA/80 units use multiple microprocessor architecture and function either as intelligent clustered CRT/keyboards controller or hold and forward data concentrator. Modular design enables changes in network function protocol and terminal devices to be accommodated and expansion to handle network growth. Controller supports up to 18 CRT/keyboards or combination of CRTs and printers. Data concentrator attaches to host computers through 1 or 2 9600-baud lines, and supports 8 9600-baud circuits on downline side. Microform Data Systems, 830 Maude Ave, Mountain View, CA 94043.
Circle 270 on Inquiry Card

HIGH PERFORMANCE BIFET OP AMPS
Internally compensated HA-5100 and uncompensated HA-1010 op amps have laser trimmed thin film resistors to reduce input offset voltage to <1.5 mV. Proprietary design and dielectric isolation process techniques produce wide-gain-bandwidth product to 80 MHz and settling time of <2 µs (0.1%, 10-V output step) at 25 °C. Drift is minimal over the temp range. Military (-55 to 125 °C) and commercial (0 to 75 °C) temp ranges are available. Harris Semiconductor Products Div, PO Box 883, Melbourne, FL 32901.
Circle 271 on Inquiry Card
It's simple. At your request, we send you a design kit that allows you to lay out up to six off-the-shelf-power supplies in our new standard 19" rack. The power supplies you select can be linear or switching supplies of various sizes to give you up to six outputs. And, the racks come in three different RETMA sizes, four front panel configurations and a wide range of features and options for maximum flexibility of design. The kit includes stick-on die cut outlines of all our standard power supply case sizes and a simple method for determining the system's cost...all in just a few minutes. An easy-to-complete order form is also included for your convenience.

Here's what we do...We assemble the power supplies into the rack, completely wired. Using specialized testing equipment, your entire system is checked for every function. And we provide you with the wiring diagram and an outline drawing for each rack assembly we deliver.

Selectable Rack Features
1. Push-button selector switches
2. Lighted circuit breaker
3. Front panel voltage adjustments
4. Digital volt/amp meter
5. LED output indicator
6. Individually fused modules
7. Perforated rack cover
8. Rugged slides
9. AC input barrier strip or optional line cord.

Send for your free design kit on your company stationery now.

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When it comes to LSI-11 interface, MDB has it:

- General Purpose Interfaces
  - Parallel for programmed I/O and DMA
  - Bus foundation modules
  - Dual and quad wire wrap for any DIP design

- Device Controllers for most major manufacturer's
  - Printers
  - Card equipment
  - Paper tape equipment
  - Plotters

- Communications/Terminal Modules
  - Asynchronous
  - Asynchronous with modem/data set control
  - Synchronous

- (P)ROM Memory Modules
  - Read-only modules (without memory)
    - For 2704, 2708 and 1702 UV PROMS
    - For 5623, 5624 and 3625 PROMS and ROMS

- Chassis Assemblies
  - Backplane/Card Guide (8 quad slots)
  - Chassis Enclosure
  - Roll-Around Cabinet

- Power Supplies
  - Single, dual and triple output configurations available

- I/O Cable Assemblies
  - MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 14 days ARO or sooner.

- MDB places an unconditional one year warranty on its controllers and tested products. Replacement boards are shipped by air within twenty-four hours of notification. Our service policy is exchange and return.

- MDB also supplies interface modules for PDP**-11, Data General, Interdata and IBM Series/1 computers. Product literature kits are complete with pricing.

Circle 104 for LSI-11; 105 for PDP-11; 106 for DG; 107 for Interdata; 108 for IBM. See us at NCC, Booth # 2042

Circle 104 for LSI-11; 105 for PDP-11; 106 for DG; 107 for Interdata; 108 for IBM. See us at NCC, Booth # 2042

Changeover from U.S. std 60-Hz, 115-V to 50-Hz, 220-V sources is accomplished by simple internal strap changes in ac to dc power supplies, reducing inventory requirements for OEMs who furnish their equipment to worldwide markets. In 4 std case sizes providing output power up to 650 W, supplies have high MTBF, efficiencies from 65 to 85%, and offer excellent line regulation. Current limiting is inherent. NJE, PO Box 50, Dayton, NJ 08810.

Circle 272 on Inquiry Card

3-STATE LED

XC-5491 provides red and green lighted color from the same T-11½ package. LED is a 0.200" (0.508-cm), 2-leaded package containing a red and green LED chip in inverse parallel. By reversing polarity of applied current, LED will emit red or green light. Chips brightness matched so that red and green light output is uniform at 10 mA, eliminating need for special drive circuits. Xclton Corp, Shaker Pk, 5 Hemlock St, Latham, NY 12110.

Circle 273 on Inquiry Card

LSI-11 COMPATIBLE STATIC SEMICONDUCTOR MEMORY

VML 1116 is hardware and software compatible with DEC LSI-11, -11/2, and -11/03 microcomputers. Memory packs 16k x 16 on a single dual-width PC board. Onboard DIP switch allows memory operation to 124k. The 4096 x 1 NMOS static RAM design eliminates need for refresh. A single 5 V at 2.5 A derived from the bus option slot powers 16k. Access time is 250 ns and cycle time is 350 ns with no refresh. Computer Extension Systems, Inc, 17511 El Camino Real, Houston, TX 77058.

Circle 274 on Inquiry Card

* TM Digital Equipment Corp.
C. Itoh's Model 8300 printer looks superb.

It works even better.

C. Itoh offers you the perfect OEM printer for general purpose computers, communication terminals, data loggers and micro computers: the Model 8300. This quiet and low-cost unit features a straightforward, reliable design and a continuous-duty 7-wire head with a life expectancy of 100 million characters.

Designed with an 8-bit parallel interface, the 80-column, dot matrix Model 8300 prints bi-directionally at 125 CPS. Its sprocket paper feed mechanism accepts multi-ply pin-feed paper in any width from 4.5" to 9.5"; paper can be loaded from the bottom or rear; and print line position is readily adjustable. The Model 8300 works even better than it looks. Would you expect anything less from C. Itoh?

Write today for detailed specifications.
The race for dot-matrix printer sales can be won by a head!

If you're selling dot-matrix printers, chances are you'll win — or lose — by a head. The speed, reliability and versatility of the print-head mechanism can make or break your product.

Florida Data's PB-600M/BNY-M is a heavy-duty matrix printer mechanism designed for high print-volume applications.

Selecting the PB-600M or BNY-M will assure you, as the OEM, of highest performance and maximum value added. FDC supports these products with complete documentation, including all analog and logic circuits, power supply recommendations and packaging. This support enables the OEM, at minimum development expense, to produce a complete, high-performance printer.

The mechanism includes a print-head, rail assembly, timing disc assembly, motors, paper tractor and ribbon assembly. A vertical-forms tape reader is optionally available. The BNY-M uses a high-speed stepper motor and a dual-track timing disk for high resolution characters and 128 dot/" graphics.

The print-head employs magnetic stored-energy wire hammers — a technology developed by FDC. The eight-wire head is capable of hammer rates as high as 3,000 cycles per second, with no duty cycle or page density restrictions. This translates to 600 characters per second for 8 x 7 matrix printing, or 240 lines per minute for 132 character/line format. For shorter lines, the unit is capable of over 1,000 lines per minute.

FDC's PB-600M/BNY-M prints an original plus seven copies and handles forms from 2" to 15" wide. Paper slew is 8"/sec. for the PB-600M and 13"/sec. for the BNY-M. Either unit weighs approximately 20 lbs. and is 21½" wide x 9" high x 12."

The mechanism is bi-directional, fast and almost unbelievably durable. It lets you offer your customers line printer speed with serial printer economy, and it's been field-proved in our own PB-600 printers.

Before you invest another dollar in printer development, find out what Florida Data can do for you. Write for further technical data or call 305/724-6080 to arrange a demonstration.

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West Melbourne, FL 32901
Choice of circuitry.
- XY Matrix
- single pole/common bus
- 2 out of 7 (or 8) coded output
Readily interfaced with logic circuitry.

Outstanding performance characteristics.
Positive tactile and audible feedback, low profile, patented snap-action dome contact, and 3 million operation per button contact system life-rating.

Standard product features.
- 1/2 inch or 1/4 inch button centers. Total button travel of only .015 inch. Standard post or flange mounting; top or sub mounting. Molded of tough ABS plastic; buttons with black on white molded-in legends standard, other options available, including clear snap-on caps for user legending.

Send for complete specifications, truth table, and information about our full line of Keyboard products.
Brawn for your brainchild.

Computer Grade Aluminum Electrolytics. No one needs to tell you how vital capacitors are to the operating competence of a computer. A single surge or cut-back in power can potentially cause an entire system to malfunction. That's why Nichicon makes Computer Grade Capacitors under the strictest quality control procedures. We supply the brawny reliability to make sure that your brainchild works properly.

Nichicon has the right capacitor for every computer design need. These include our NKB Compact Series, NSB Standard Series and NHB High-Ripple Series. Nichicon computer grade capacitors feature top quality pressure sensitive safety vent construction with PVC insulating sleeves.

**Long life reliability** is built into every unit. In an operating temperature range of \(-25^\circ C\) through \(+85^\circ C\), these aluminum electrolytics offer a dependable low-leakage current, high-ripple capabilities and low ESR.

Computer Grade Capacitors are excellent examples of Nichicon's continuing emphasis on reliability as the dominant design criterion. We also manufacture every other type of capacitor including all types of aluminum electrolytics, ceramic discs, film, oil filled—without PCB's, metallized paper and wax paper capacitors for standard or specialized applications.

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CIRCLE 196 ON INQUIRY CARD
COMPUTER DESIGN/MAY 1979
THE "SMART" PRINTER BUY.

Low cost is smart. With Dataroyal's low prices and volume discounts, few printers cost less to buy. With Dataroyal's unique microcomputer design and rugged mechanism, other printer costs less to own.

It's smart to let one printer do the job of many. A wide range of firmware packages allows Dataroyal printers to meet almost every requirement within the 120-200 character-per-second performance range. Upgrade, downgrade or odd new functions - interfaces, communications protocols, buffering, and more - all within seconds.

In the factory or in the field.

It's smart to demand reliability, and Dataroyal has years of experience building printers that work because they have to. Many of the Dataroyal printers now in use operate in hostile environments at 100% duty cycle.

It's smart to choose a vendor who can deliver. Dataroyal can, in 45 days or less. Low purchase prices, applications flexibility and reliability add up to low cost of ownership over a long product life.

IPS 7000 INTELLIGENT PRINTING SYSTEMS

1M1010 programs bipolar P/ROMs, single-chip microcomputers, FPLAs, PGAs, PALs, and PMUXs to manufacturers' specs, provides full editing capability, and has 14-digit alphanumeric gas discharge display and full size keyboard. Capabilities include check sum, insert, delete, and move words or blocks of RAM. The entire P/ROM set may be programmed from RAM; 4k x 8 RAM is standard and 16k x 8 is optional. Two serial I/O ports are included.

International Microsystems, Inc, 11554 C Ave, Auburn, CA 95603.
Circle 278 on Inquiry Card

VHF SYNTHESIZER

With an output frequency variable from 80 to 120 MHz, SI-103C offers 6½-digit resolution with the stability and accuracy of the internal crystal clock. Frequency stability is ±1 x 10⁻⁶ from −10 to 50 °C. BCD programming is available, if thumbwheel frequency control is not desired. Output is 13 dBm with nonharmonic spurious responses down to 70 dB below the carrier. Harmonic outputs are down to <25 dB below the carrier. Power requirements are 115/230 Vac at 50-60 Hz, 20 W max.

Syntest, 169 Millham St, Marlboro, MA 01752.
Circle 279 on Inquiry Card

CARD PUNCH CONTROLLER

DP2029 allows card punching from any std asynchronous RS-232-C communications line equipped with hardware hold-off capability (on lines without this capability, user can delay or transmit nulls for card release, character, or feed delays). Baud rate is selectable from 110 to 9600. Unit buffers up to 2 characters with carriage return configured as std card release (other char may be used as triggers).

Digital Products, PO Box 79438, Houston, TX 77079.
Circle 280 on Inquiry Card

CIRCLE 197 ON INQUIRY CARD

PRODUCTS

P/ROM PROGRAMMER

CIRCLE 198 ON INQUIRY CARD

MFM floppy, 1 head or 2

AED's field-proven 6200 Series floppy disk system has recently been expanded to provide the minicomputer user with a wider choice of disk drive capability. The AED6200 Series now offers double density (MFM) systems in four configurations: 2 drives with single head (5½" and 7" cabinets), 4 drives with single head (10½" cabinet), 2 drives with dual head (7" cabinet) and 4 drives with dual head (two 7" cabinets). All systems come complete with formatter, power supply, drive electronics and CPU interface. Interfaces for LSI-11, PDP-8 and 11, Nova/Eclipse, Varien, Interdata and CAI are all available from AED.

Here is a checklist of the AED6200's outstanding user benefits:

- low cost, fast access storage
- 1.2 megabytes/diskette
- industry standard 8" media
- programmable formatter for ideal record size
- multiple source drives
- 8 computer interfaces available
- expandable to 4 drives
- CRC and IPL for easier loading
- delivery from stock on all popular models

Get all the facts by calling or writing to our Marketing Manager today.

Advanced Electronics Design, Inc.
COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400
Fullerton 714-738-8688, Telex 367498

CIRCLE 198 ON INQUIRY CARD
When it comes to computers, SAMS PUBLISHES THE BOOKS

Introducing...

It has long been the objective of the "Blacksburg Group" to develop timely and effective educational materials and aids that will permit students, engineers, scientists and others to quickly learn how to apply new technologies to their particular needs. The members of the group have long been involved in digital electronics, minicomputers, and microcomputers.

The Blacksburg Continuing Education Series™ is an easy to read format consisting of 16 titles. Subjects range from basic electronics through microcomputers, operational amplifiers and active filters. Each title in the series includes detailed experiments, "hands-on" learning experiences, and examples to reinforce basic concepts. Book Size 5½" x 8½", softbound.

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Indianapolis, Indiana 46206

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Sample outputs, specs, outline drawings, and descriptions of 7-segment numeric, 5 x 7 matrix alphanumeric, and graphics/alphanumeric/analog fixed head, nonimpact thermal printers are featured in brochure. Gulton Industries, Inc, East Greenwich, R.I. Circle 300 on Inquiry Card.

Displays and Connectors

MOS Semicustom IC Design
Schmitt triggers and multivibrators, and logic design for CMOS and NMOS monolithic chips are subjects discussed in two application notes intended to aid in custom MOS IC design. Interdesign, Inc, Sunnyvale, Calif. Circle 302 on Inquiry Card.

Microcomputer Systems
Descriptions, photos, and conceptual diagrams for board level computers, rack mounted and prototyping systems, supporting products, plus STARPLEX™ information are included in databook that is available by letterhead request, attn: Series/80 Databook, to National Semiconductor Corp, CPA Marketing Services, MS/10A190, 2900 Semiconductor Dr, Santa Clara, CA 95051.

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Micro 700 Band Splitter, presented in brochure, allows up to four synchronous data terminals to share a single telephone or EDS link. Micom Systems, Inc, Chatsworth, Calif. Circle 303 on Inquiry Card.

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Guide provides specs and dimensional drawings for bonded, laminated, and color coded flat cable; bulk and prestriped flat jumper cable; and custom assemblies. Bellden Corp, Electronic Div, Richmond, Ind. Circle 305 on Inquiry Card.

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Brochure provides descriptive information and application data for basic, private line, and toll test board versions of 9800 series test board systems. Wiltron Co, Mountain View, Calif. Circle 306 on Inquiry Card.

Replacement Printers
Booklet cites operating features and characteristics of printers that interface to IBM, DEC, Data General, Hewlett-Packard, Univac, and Interdata systems. Decision Data Computer Corp, Horsham, Pa. Circle 307 on Inquiry Card.

Discrete Testing System
60-p brochure contains all information needed to define and configure test system, including photos, illustrations, and descriptions of IMPACT line, software, and accessories. Lorin Industries, Inc, Danbury, Conn. Circle 308 on Inquiry Card.

Low Profile Relays
Catalog supplies specs, dimensional drawings, PCB layouts, and photos for class 63, 64, and 65 relays. Magnecraft Electric Co, Chicago, Ill. Circle 309 on Inquiry Card.

Programmable Intelligent Terminal Systems
Brochure outlines extensive system software support that includes high level languages, forms generation, and utilities and diagnostics. Ontel Corp, Woodbury, NY. Circle 310 on Inquiry Card.

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High power semiconductor coolers and medium power heat dissipators are profiled with technical details, performance curves, and dimensional drawings in catalog. Velamile Products, Div of Ostby & Barton Co, Warwick, R.I. Circle 311 on Inquiry Card.

Programmable Controllers
Primer on programmable controller for those not acquainted with them, and brochure on MaxiMiser programmable controller are available by letterhead request to Cincinnati Milacron, Electronic Systems Div, Mason Rd and Rte #48, Lebanon, OH 45036.
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