GENERAL FEATURES

New AppLINX CD-ROM Released!

The latest AppLINX CD-ROM contains a collection of applications and product information useful for designers working with Xilinx devices...

See Page 9

PRODUCT INFORMATION

XC9500 CPLDs in Volume Production

Four members of the in-system-programmable XC9500 CPLD family are ready for designers looking for the best ISP solution...

See Page 13

5,000,000 and Counting

The world’s most popular FPGA, the XC4000 Series, hits two milestones...5M units shipped and the first production of the XC4000EX family...

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DESIGN TIPS & HINTS

Downloading CPLDs With an Embedded Processor

An embedded processor can be used to control CPLD programming, resulting in considerable flexibility throughout the product life cycle...

See Page 18

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The Programmable Logic CompanySM

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San Jose, CA
Probabilistic Capacity

Every user of programmable logic at some point has to ask the question: "How large a device will I require to fit my design?"

Despite the advent of FPGAs like the Xilinx XC4000 series and the Xilinx Virtex, the process of selecting the right programmable logic device continues to be a complex one, fraught with competing claims of the various vendors and try to sell programmable logic devices, which have been named to reflect that claim. Then came the use of "memory blocks" in addition to "logic gates". Each bit represents a portion of the memory; the total number of bits represents the total memory capacity. Thus, "counting gates" is far from an exact science; different vendors and manufacturers may count different things. The number of 2-input NAND gates that can be represented in a programmable logic device is just one of the many metrics that provide an indication of the amount of logic that can be implemented in that device.

In the same vein, direct competitors and suppliers of FPGA devices may count different things, and for different reasons. There are, for example, the number of configurable logic blocks or macrocells, are not always sufficient. (However, in some instances, the number of 2-input NAND gates, which represent the basic logic resources, direct comparisons, such as the chip to silicon, though the same concept is not necessarily the same.)

It is important to note that what is a problem for one vendor may be an advantage for another. In fact, a look at the density figures provided by different vendors reveals that the same number of gates can be implemented in two different devices in different ways. Some vendors decide what the capacity of their device is, and then design their logic functions. This metric has the advantage of being familiar to ASIC designers and, in general, it is easy to compare one vendor's claims with another's. Furthermore, since each family of devices has a different architecture, the way in which logic resources are represented will vary from one vendor to another. Thus, the density figures provided by different vendors are not directly comparable.

Another problem with comparing gate counts is that different vendors may use different definitions of what constitutes a "gate". For example, a single 4-input look-up table (LUT) can quickly inflate gate counts. For example, if a vendor defines a LUT as a single logic element, then a single 4-input LUT would be counted as four gates. If the vendor defines a LUT as a single logic function, then a single 4-input LUT would be counted as a single logic function. Thus, "counting gates" is far from an exact science; different vendors and manufacturers may count different things.

The number of 2-input NAND gates that can be represented in a programmable logic device is just one of the many metrics that provide an indication of the amount of logic that can be implemented in that device.
One Size Does Not Fit All: Development System Products & Strategies

by KENN PERRY • Director of Software Marketing

One design tool configuration cannot meet the needs of all programmable logic designers. Overall, today’s designers are looking for top-down, language-driven design support that enables system-level integration within their programmable logic design methodologies. However, user requirements and expectations vary considerably, dependent on their design methodologies, cost considerations and time-to-market pressures.

Xilinx is addressing the needs of the low-, mid- and high-density classes of designers with three XACT™ software solutions: the Foundation Series™, Alliance Series™ and System Level Integration (SLI™) options. Thus, Xilinx users can choose between a complete, tightly integrated design system supporting industry-leading HDLs, schematic capture and simulation (the Foundation Series), or the integration of Xilinx implementation tools into their chosen EDA environment, leveraging defacto industry standards (the Alliance Series). Additionally, comprehensive system-level design is supported by SLI options, such as LogiCore™ modules, that enable users to achieve high density and performance while greatly reducing time-to-market. These products are available today.

Foundation Series
Designers of low-density FPGAs and CPLDs, the largest group of users, typically are cost-sensitive and prefer easy-to-use, push-button, integrated software solutions that support both schematic and language-based entry methods. Intolerant of delays, defects or risks, these users desire a complete, “shrink-wrapped” solution. The Foundation Series solutions provide the technological “foundation” upon which support for higher-density Xilinx devices can be built.

Xilinx is the first programmable logic vendor to offer a low-cost, shrink-wrapped solution that integrates schematic entry, HDL synthesis and gate-level simulation for both CPLDs and FPGAs. The goal of the Foundation Series solution is to provide an environment where the user can open the box, install the software, get up-to-speed quickly and complete designs successfully without assistance — although support is readily available if needed. From a single environment, users have access to HDL synthesis (VHDL and ABEL initially), schematic entry, gate simulation and core implementation tools, making PDL development simple and easy without compromising design flexibility or performance. The Xilinx continuum of software functionality and device technology enables users to expand their Foundation Series system capabilities with the changing demands of their design requirements.

Alliance Series and the Alliance Program
The mainstream segment of programmable logic, encompassing mid-range density users (10k to 19k gates), is the fastest growing segment in the programmable logic market. With decreasing market windows and increasing technology demands, main-
stream designers have critical business issues to solve. To remain competitive in today’s marketplace, they have developed their own design methodologies employing tools and technology provided by EDA vendors. They prefer to leverage their previous investments and experiences by using the appropriate combination of tools from their EDA and programmable logic suppliers. Therefore, it is critical that their programmable logic design solutions are tightly-integrated with their established methodologies and support industry standards. The Alliance Series, based on the industry’s most powerful set of third-party EDA integration solutions and partnerships, provides the benefits of an “open system.” Alliance Series products support industry standard design interfaces, such as EDIF, VHDL, Verilog and EPM, and allow designers to create and verify designs in their chosen third-party EDA environment.

Through the Xilinx Alliance Program, integrated design solutions for the design of Xilinx devices are available from a broad array of third-party EDA suppliers. The Alliance Program is structured to ensure that Xilinx users have access to the widest variety of high-quality third-party tools, certified to work with Xilinx products. Currently, the Xilinx Alliance Program includes more than 100 partners, representing over 160 products, who have been selected for their contribution to Xilinx development and their responsiveness to customer needs. The Alliance Program supports these partners with technical information and assistance on an ongoing basis and, in turn, the partners provide Xilinx with input regarding product interfaces and directions.

System Level Integration (SLI)

High-density users, typically the early adopters, require leading-edge technology to help solve their very large, complex and performance-driven design problems. These users focus on advanced functionality and need the newest, most advanced technologies. As programmable logic devices increase in density, designing at the gate level is no longer a realistic approach. SLI tools go far beyond just delivering support for higher-gate-count designs. Xilinx SLI options facilitate the design of system-level functions in high-density, high-performance programmable logic devices. Intended as “add-ons” to the Alliance and Foundation Series products, current SLI tools include the LogiCore modules. LogiCore modules are fully-verified, drop-in system level modules, such as target and initiator PCI bus interfaces. These tools can dramatically shorten design cycles and facilitate complex, system-level integration within programmable logic devices.

Next Generation Core Software Platform

The upcoming upgrade to the XACTstep software platform incorporates our next-generation core software environment, leveraging the industry-leading technologies from the merger between Xilinx and Neocad. This new core technology includes timing-driven optimization, mapping, FPGA placement and routing and CPFD fitting algorithms, and it will be the software platform for all existing and future Xilinx IC product development and support. This new release will still incorporate many aspects of the popular XACTstep version 6 software environment, providing users with an easy migration path and protecting previous tool and training investments.

In summary, upcoming releases of the XACTstep product series are being developed to include the latest technological advancements, including enhanced SLI product offerings, value-added EDA technologies and additional Xilinx device support. These advancements will deliver increased ease-of-use benefits for rapid design implementation flows, enhanced integration and high-quality results. In addition, Xilinx integrated educational tools will round out the technologies being delivered.

Future programmable logic design solutions from Xilinx will place more emphasis on making users of programmable logic better overall system designers, as well as ensuring rapid design implementation into Xilinx silicon.

The upcoming upgrade to the XACTstep software platform incorporates our next-generation core software.

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Items that have changed since the last issue (XCell 22) are in color.

Ruby:

These partners have a high degree of compatibility and have repeatedly shown themselves to be significant contributors to our users’ development solutions.

Emerald:

Proven Xilinx compatibility

For more information, please refer to the previous issue of XCell.
can account for anywhere from one to nine ‘gates’ when used to implement a logic function, depending on the type of function that is implemented. However, when that same look-up table is used as 16 bits of ROM or RAM memory, it now is implementing 16 x 4 = 64 ‘equivalent gates’. Thus, FPGA gate counts rapidly inflate when the capacity metric assumes a significant amount of on-chip memory usage; it’s important to know what assumptions about memory usage apply to a claimed gate density in these devices.

For example, the device names in the XG4000E and XG4000EX families are based on our ‘maximum logic gates’ metric — a measure of logic capacity only that assumes no memory usage. However, a major competitor has named its competing family based on a metric they call “typical gates” that includes both types of gates, and further assumes up to 35% on-chip memory utilization. Superficially, based on the device names alone, it appears that their devices are much larger than ours. However, even a cursory examination of device resources reveals a quite different story. For example, their “20,000-gate” device includes 1,152 4-input look-up tables, 1,344 registers and a maximum memory capacity of 12K bits. In contrast, the Xilinx “33,000-gate” XC4013E includes 1,152 4-input lookup tables, an additional 1,356 registers and a maximum memory capacity of 128K bits. However, even a cursory examination of device resources reveals a quite different story. For example, their “20,000-gate” device includes 1,152 4-input look-up tables, 1,344 registers and a maximum memory capacity of 12K bits. In contrast, the Xilinx “33,000-gate” XC4013E includes 1,152 4-input lookup tables, an additional 1,356 registers and a maximum memory capacity of 128K bits. However, even a cursory examination of device resources reveals a quite different story. For example, their “20,000-gate” device includes 1,152 4-input look-up tables, 1,344 registers and a maximum memory capacity of 12K bits. In contrast, the Xilinx “33,000-gate” XC4013E includes 1,152 4-input lookup tables, an additional 1,356 registers and a maximum memory capacity of 128K bits.

This is not to say that Xilinx has not, at times, been guilty of “gate-inflation.” However, we have been more consistent over the years than most of our competitors. We recently reviewed and slightly revised our methodology for assigning gate counts for XC4000 Series and XC5200 family FPGAs. The results of that effort can be seen in the product specifications included in our latest data book. Xilinx application note #059, “Gate Count Capacity Metrics for FPGAs,” explains our capacity metrics and the methodology used to obtain them; the application note can be viewed at our WebLINX web site (www.xilinx.com).

Besides being subject to statistical manipulation, gate counts used as capacity metrics suffer from another severe drawback – they usually take only logic block and on-chip memory resources into account. Modern FPGAs include a host of other important features. For example, architectural features in the XC4000 Series that are not reflected in our capacity metrics include wide-edge decoders, dedicated arithmetic carry logic, registers and logic in the I/O blocks, global busses and clock distribution networks, and internal three-state buffers. These important features can considerably boost the capacity and system integration capabilities of these devices.

Experienced CPLD and FPGA users realize that there can be considerable variation in the logic capacity of a given device dependent on factors such as how well the application’s logic functions match the target device’s architecture, the efficiency of the development tools, and the knowledge and skill of the designer. So, my advice is to apply a healthy dose of skepticism to CPLD and FPGA manufacturers’ gate count metrics (yes, even ours). Examine the assumptions behind the “gate counting methodology.” Better yet, take the time to examine and compare all the internal resources of the various devices being considered for a design.
Swiss Engineers Use FPGAs to Link the critical communications control logic, they chose the world's leading FPGA family — the XC4000 Series.

Based on the XC4000 Series, the critical communications controller was realized in only two XC4000 FPGAs. All the processing elements (PEs) are connected to a common 72-bit bus. All the special registers and FIFO buffers are controlled by a central communications controller.

This protocol, implemented directly in hardware using the FPGA devices, allows fast, low-latency communications and connected to a common 72-bit bus. All the special registers that control clock, reset, interrupts and similar functions. Each PE is connected to the digital signal processor (DSP), enables the processing power in each PE.

Developed during the project, the new communications protocol called Intelligent Communication was developed to provide fast communications and connected to over 3000 applications.

Changes since last issue printed in color; 1736A, 1765 and 17128 columns eliminated since last issue
### Programmer Support For Xilinx XC7200/7300 CPLDs — November 1996

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### Supercomputing Systems

In the GigaBooster system, the controller was redesigned into three XC4013 FPGAs to allow room for expansion. One FPGA holds several small state machines, an abundance of control registers, and other glue and interface logic; this design uses about half of the available logic blocks, but all of the I/O pins. The other two FPGAs implement the logic directly involved in the gathering and redistribution of data from the processing elements, including a 42-bit counter and a large register/comparator file for each PE. The first of these FPGAs is more than 90% utilized, and connects to five of the processing elements.

About 40% of the second FPGA contains the identical logic for the remaining two PEs. Additional logic is dedicated to monitoring the system's behavior and the values of internal counters, registers, and other glue and timing simulation were used to debug and verify system operation.

The FPGA's readback capability also was exploited during system debug, and is now used to “dump” the state of the communications controller in the event of a communication failure. Using readback, the values of internal counters, registers, and state machines can be extracted and analyzed.

In summary, the use of reconﬁgurable XC4013 FPGAs was key to the implementation of interprocessor communication protocols directly in hardware, as opposed to the more-traditional software approaches. The resulting high-performance communications management allows the system to tap the full processing power of each of its Alpha processors, delivering 1.6 Gigaflops of peak performance in an affordable and compact system.

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**Note:** The XC7200 and XC7300 CPLD charts have been combined since the last issue.

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**Supercomputing Processors**

“The use of reconﬁgurable XC4013 FPGAs was key to the implementation of interprocessor communication protocols directly in the hardware.”
MiroTech Microsystems: Real-Time Reconfigurability for DSP Acceleration

Our congratulations to the development team at MiroTech Microsystems Inc. (Montreal, Canada). MiroTech Microsystems has released a commercial product that uses reconfigurable computing to advance the state-of-the-art for DSP acceleration. At the most recent ICSPAT/DSP World Exposition in Boston, MiroTech Microsystems announced an exclusive North American agreement with Spectrum Signal Processing Inc. to distribute MiroTech’s FPGA-based DSP acceleration module. MiroTech’s X-CIM module complements Spectrum’s extensive PCI, VXI and VME C4x-based DSP product line. Together these products provide substantial acceleration for selected compute-intensive, high-performance applications.

X-CIM is an FPGA-based reconfigurable computer in a TIM form factor that is fully-compliant with Texas Instruments’ TM520C40 DSP processor. The module features 80 Mbytes/s communication port bandwidth, 30 ns on-the-fly reconfigurability, and hardware-implemented parallel processing. It’s a sophisticated, highly portable architecture based on Xilinx reconfigurable FPGAs and banks of high-speed RAM.

As the tendency towards more complex DSP systems continues to grow, designers are constantly seeking new ways to reach higher performance and to unravel bottlenecks while reducing development costs. "What is unique with our X-CIM is its implementation in an IEEE standard and off-the-shelf product packaging," noted MiroTech President and CEO Pierre Popovic. "The X-CIM module can deliver acceleration up to 100 times that of a general-purpose DSP processor for highly repetitive ‘inner loops’ within algorithms.

The marriage of the X-CIM module with Spectrum’s products allows the design of very compute-intensive systems while staying within Spectrum’s C40 environment and DSP development tools. X-CIM modules are supported by a comprehensive suite of software tools referred to as COREKIT. With these tools, developers can transparently accelerate a wide range of DSP functions in applications such as radar, sonar, voice and image processing.

For more information on the X-CIM product line, contact MiroTech Microsystems Inc. at 514-956-0060 or at MiroTech@montreal.com.

The Xilinx Reconfigurable Computing Developer’s Program is promoting the commercial use of FPGAs in reconfigurable computing applications. These systems add significant value by dynamically changing FPGA designs, in real-time, while the system is operating. Applications that can exploit the benefits of the RC concept include graphics and image processing, audio processing, and data communications.

For more information on the Xilinx Developer’s Program and our reconfigurable computing efforts, please visit our web site at www.xilinx.com, or call John Watson at 408-879-6584.
Last September, a group of more than 35 leading electronics firms announced the formation of the Virtual Socket Interface (VSI) alliance. This open alliance is dedicated to promoting the growth of the system-level integration (SLI) chip industry by developing the technical standards required to enable the “mix and match” of system-level modules (SLMs). Xilinx has entered the VSI alliance, and is actively participating in standardization efforts affecting programmable logic technologies. Our participation augments our current programs for the development of a diverse set of high-quality SLMs, called LogiCore™ modules, for the various Xilinx FPGA and CPLD families.

The goal is to establish a set of open SLM design interface and productionization standards. Through use of the developed standards, design engineers will be able to use SLMs from several sources in the design of highly-integrated programmable logic devices. For example, a designer could construct a system combining SLMs supplied by Xilinx (such as the LogiCore PCI master/slave), SLMs from third-party providers (such as the members of the Xilinx LogiCore Alliance), and reusable modules from his/her previous designs.

SLMs from all sources will be designed to common standards, much like physical components that are mixed-and-matched today on a printed circuit board. These VSI-compliant SLMs can be viewed as “virtual components” that, through common interface standards, fit quickly into “virtual sockets.” In order to rapidly provide a solution, the design data standards will be based on open formats commonly supported by all EDA vendors.

High-quality SLMs are a key component for high-performance and high-density programmable logic design. The use of predefined and pre-verified SLMs can dramatically reduce system development cost and time, resulting in faster time-to-market and a greater competitive advantage.

For further information about the VSI Alliance, see their web site at www.ip-net.org. For additional information about the LogiCore products and LogiCore Alliance Program, see the WebLINX web site at www.xilinx.com/products/logicore/logiwire.htm.

New AppLINX CD-ROM Shipped

An updated AppLINX CD-ROM has been shipped to all registered Xilinx users. The CD contains a complete collection of Xilinx applications and product information. Access to the AppLINX CD is another benefit of maintenance support for the Xilinx development system.

The AppLINX CD-ROM includes:

- Presentation notes for the Xilinx 1996 Fall Seminar
- The AppLINX CD merges the best aspects of the Xilinx WebLINX web site and the Xilinx FTP site. Users with access to an HTML browser can navigate the files quickly and easily off-line, while links are available to find the latest information on-line.
- The AppLINX CD will be updated on a regular basis. Make sure you visit the Xilinx WebLINX web site at www.xilinx.com for the latest information.
- Regarding the fall seminar, contact your local Xilinx sales office to inquire about a presentation to your company.
Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative.

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For the first time, Xilinx Inc. quarterly sales revenues declined from both the prior quarter and the year ago period. Revenues for the September-ending quarter were $150.6 million, a decrease of 13.1% from the immediately preceding quarter and 7.5% from the same quarter one year ago.

The September quarter was a difficult quarter for the overall programmable logic industry and Xilinx in particular,” stated CEO Wim Roelandts. “We believe this industry and Xilinx in particular,” stated CEO Wim Roelandts. “We believe this

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How are Boundary Scan components for the XC4000 family instantiated in Verilog-based designs?

To use Boundary Scan components in XC4000 Series devices, instantiate the boundary scan symbol (BSCAN) and the associated dedicated I/O. Use the “dont_touch” attribute; otherwise, BSCAN may be deleted by the Synopsys compiler.

Runscript for compiling the XC4000/XC4000E BSCAN Verilog Example:

```
PART = 4025ehq240-3
TOP = example
read -format verilog "bscan4k.v"
set_port_is_pad "" insert_pads
set_dont_touch u1
set_dont_touch u2
set_dont_touch u3
set_dont_touch u4
compile
replace_fps
set_attribute TOP "part" type string
PART
write -f xnf -h -o "bscan4k.xsnf"
```

What is happening when Quicksim issues this warning of every primitive in a design?

```
Q: Warning: Instance "GIVE_ME_AN_E utility"
Q: Could not find a registered simulation model with label: "xc4000"
Q: NULL model will be inserted. (from: Analysis/Simulation/Utilities/DesignUtils/185)
```

This is caused by an incorrectly-written simulation viewpoint for the design, which may result when a design is retargeted to a new device family. The solution is to delete that default viewpoint, then run PLD_DVE_SIM on the design, specifying the correct part family. If done from the command line: an XC4000 design, for example, might use:

```
delete_object blanking_design/default.pld_dve_sim blanking_design.xc4000
```

Note: If Timsim® -o was used to create the simulation model, be sure to run Timsim® instead of PLD_DVE_SIM. Timsim® -o runs PLD_DVE_SIM, then adds links to timing information into the viewpoint afterwards.

```
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```

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```
module example (a,b,c);
input a, b;
output c;
wire tdo_net;
wire tms_net;
wire tdi_net;
wire tck_net;
reg c;
output c;
input a, b;
module example (a,b,c);
input a, b;
output c;
wire tdo_net;
wire tms_net;
wire tdi_net;
wire tck_net;
reg c;
output c;
input a, b;
module example (a,b,c);
input a, b;
output c;
```

```
Xilinx Inc. stock is traded on NASDAQ under the symbol XLNX.
```

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**Foundation**

Q: Besides the CD-ROM supplied with the product, are there any sources of additional information about using the Xilinx Foundation Series software?

A: The Foundation Documentation Update Pack contains application notes about the Foundation Logic Simulator, Foundation XVHDL compiler, and a new simulation tutorial. Get FND_DOC1.EXE (self-extracting ZIP file) from the Xilinx FTP site (ftp.xilinx.com/pub/swhelp/foundation) or the Xilinx IBIS Software Help. Also:

- EDIF2XNF: targeting an XC4000E device. During the Xilinx Foundation Series software?

Q: In this example, OFD is a primitive associated with the device being targeted. Schematic library with which the design was loaded from the Xilinx FTP site at:


A schematic originally targeted for the XC4000 family is now targeting an XC4000E device. During Men2XNFs, the following error occurs when running EDM2XNF:

**Error: 6 EDIF data "qfd.xds" not found in directory */usr/warc/data/unified/edif4000e"

In this case, the schematic was created using the XC4000 library, but the design is now targeted to an XC4000E device. (Other family combinations may also cause this error.) Certain symbols are primitives in the schematic library with which the design was built (XC4000E), but are macros in the library associated with the device being targeted (XC4000E). In this example, OFD is a primitive in the XC4000E library but is a macro in the XC4000E library (since it has, underneath it, the clock-enabled QFDX symbol).

DELETE TECHNOICAL QUESTIONS & ANSWERS

**Mentor Graphics**

Q: Can XACTstep 5.2.1 be used with Mentor Graphics’. Bx release?

A: Under Mentor B.x, Gen_sch8 and XBLXGS may fail with either “call to undefined procedure” (SunOS) or “unresolved propagate symbol” (HP-UX) error messages due to problems with dynamically linking to Mentor’s Design Data Port (DDP). A patch is available to fix these problems and make XACTstep 5.2.1 interface smoothly with Mentor B.x. The patch may be downloaded from the Xilinx FTP site at:


Q: ENVWrite (Mentor’s EDIF editor) looks at the XC4000 version of OFD in the schematic. This component has attached to it a COMP=OFD property, indicating that this component is a primitive and should be written as such in the EDIF file. EDIF2XNF then takes this primitive description and looks for the corresponding old eds file in the $ICl/data/unified/edif4000e directory, that contains EDIF descriptions for XC4000E primitives. Since OFD is not a primitive in the XC4000E family, the old eds file does not exist in the directory, resulting in the error.

A: The correct OFD from the XC4000E library has no COMP=OFD property attached to it, since the COMP property is reserved for primitives. Therefore, if the correct XC4000E component had been used, ENVWrite would have written out the hierarchy below OFD. Then, EDIF2XNF would have never seen the “primitive” and would have never tried to look for a non-existent old eds file in the XC4000E data directory.

The proper way to retarget the design to a new device family is to use the Convert Design utility in PLD_DA before running the implementation flow. Convert Design replaces the library components in a schematic or set of schematics so that they come from the proper library. For instructions on how to use Convert Design, see Solution 794. “Retargeting a design in Mentor Design Architect (Convert Design),” from the Xilinx Solutions Database:

http://www.xilinx.com/twiki/data/794.htm

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**WebLINX and SmartSearch Agents Keep You Up-To-Date**

That’s it! This will create an agent that will notify you whenever Xilinx posts a new application note to the site. Remember that you can create an agent for anything you can search for, and they are not limited to the Xilinx site.

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The following XAPP application notes and XBRF application briefs have recently been added to WebLINX. You can find these by first going to the application notes page and selecting XAPP application notes or application briefs:

- XAPP051 Synchronous/Asynchronous FIFOs
- XAPP052 Efficient Shift Registers, USR Counters, etc.
- XAPP053 Implementing FIFOs in XC4000 Series RAM
- XAPP054 Constant Coefficient Multipliers for the XC4000E
- XAPP055 Block Adaptive Filter
- XAPP056 System Design with New XC4000EX I/O Features
- XAPP057 Using Select-RAM Memory in XC4000 Series FPGAs
- XAPP058 XC9500 In-System Programming Using an 8051 Microcontroller
- XAPP059 Gen_Sch8 Count Capacity Metrics for FPGAs
- XAPP060 Design Migration from XC4000 to XC5200
- XAPP061 Design Migration from XC4000 to XC4000E
- XAPP062 Design Migration from XC4000 to XC4000E
- XAPP063 Interfacing XC95020 to Microprocessors (TMS320C54 Example)
- XAPP064 Interfacing XC95200 to Microprocessors (TMS280C50 Example)
- XAPP065 XC4000 Series Edge-Triggered and Dual-Port RAM Capability
- XAPP066 XC5200 Select-RAM Flexibility with Speed
- XAPP067 XC4000E Low Power Consumption: At High Speed
- XAPP068 XC4000 Series Select-RAM Maximum Configurability
- XAPP069 XC4000EX Routing: A Comparison with XC4000E and ORCA
- XAPP070 XILINX® FLL Design Techniques and Usage in FPGA Design
- XAPP071 XC4000-Series FPGAs: The Best Choice for Delivering Logic Cores
- XAPP072 XC5200 Far-Locking Capacity and Benchmarks
One-Day VHDL Seminar Now Available

Xilinx is sponsoring a series of one-day introductory VHDL seminars conducted by qualified instructors from Esperan Inc. Esperan specializes in technical training and has educated thousands of VHDL users since 1992. This one-day course, a must for new users, emphasizes the basics of the VHDL language. A full day of lecture and hands-on labs, the seminar uses the VHDL tool offered by Xilinx in the Foundation Series™. The seminar is intended to provide an introduction to VHDL, which is becoming the standard description language for hardware design. Each attendee receives an evaluation kit of the Xilinx software. This provides an opportunity to practice the skills and knowledge obtained at the seminar. The kit includes the Foundation Series software, an integrated tool set of schematic entry, VHDL synthesis, functional and timing simulation and design implementation tools—everything needed to create an entire design. Xilinx, its distributors and representatives, together with Esperan, are sponsoring these seminars. Contact your local Xilinx representative to inquire about VHDL training seminars in your area. In related news, electronics distributors Hamilton Hallmark, Marshall and Insight are in the process of creating VHDL workshops as well. In each case, Xilinx FPGA devices and the Foundation Series tools have been selected for use in the lab exercises.

Updated Training Courses Available

The basic Xilinx technical training courses have been updated to reflect all the features of the latest development software. XACTstep™ version 6.0.1 software is fully incorporated into the schematic-based design course. The course examines a complete design scenario for the Foundation Series software user. The updated synthesis-based design course provides VHDL/Verilog designers with an intimate working knowledge of the XACTstep v5.2.1/6.0.1 synthesis software. Both of these courses are available worldwide. The current schedule of schematic-and synthesis-based courses, as well as course registration information, can be found at the WebLINX web site (www.xilinx.com).

First Hands-On Workshop on Reconfigurable Computing

The Xilinx University Program (XUP) has had an active training schedule with nine recent workshops in four countries. XUP workshops are designed to train university instructors on the basics of using programmable logic for undergraduate courses, graduate courses and research. In addition to the standard workshops, and in response to a growing interest in dynamically-reconfigurable logic, a unique, leading-edge workshop was held at Cornell University (Ithaca, NY).

The Cornell workshop was the first to examine both the hardware and software issues associated with dynamically-reconfigurable computing, including hands-on laboratory exercises. Participating lecturers included representatives from Xilinx, the Virginia Institute of Technology, ETZ Zurich, Cornell University, and Imperial College (UK). Mr. Nick Treddinick, an IEEE Fellow, presented the keynote address. Xilinx is committed to addressing the needs of the reconfigurable logic market, and the Xilinx University Program is committed to further academic support of this exciting area of study. Proceedings from the workshop are available to XUP participants, and further information about this workshop and future XUP workshops can be obtained on the web at www.xilinx.com/programs/univ.htm.

Windows NT Environment

Windows NT 4.0 users will install the newer version of Rainport mentioned in the Windows Setup section. A readme within the ZIP file explains how to install this driver.

Running the tools

You will be running the tools in an MS-DOS session. Take a look at the Reference Guide Volumes 1, 2 and 3 for specific information about using these tools in a DOS environment. You will see that some of the Windows tools will work. Besides the Simulation Utility and the Memory Generator, you can create a new icon for the Timing Analyzer. The Command Line for this tool is C:\xact\timingan.exe and the Working Directory is C:\xact. There have been cases where these Windows tools have had problems, and the workaround is to use the DOS equivalent. Tools that will not work are the Design Manager, Flow Engine, and Floorplanner.

If you have any problems using the Adobe Acrobat reader, you can download a copy of Acrobat 2.1 for Windows 95/NT from their Web site, www.adobe.com/acrobat/windows.html. Hopefully, these hints will get you up and running within your Windows NT environment. There are some differences with different installations of Windows NT, so results may certainly vary.
Running XACTstep™ v5.2.1 in a

XACTstep™ version 6.0.x (the Windows tools) was compiled and tested for Windows 3.x. It was not compiled for Windows NT. Unlike Windows 95, there is no work-around to enable the Windows tools to work. This release does NOT support Windows NT.

However, we have had some success using XACTstep v5.2.1 (the DOS tools) within a DOS session under Windows NT. There are a few things that must be done to set up the environment, as described below.

Please note that the next full release of Xilinx software will support Windows NT 4.0. The solution described here should be considered a tactical work-around for Windows NT 3.51 and a temporary work-around for Windows NT 4.0.

All of the instructions apply to both Windows NT versions 3.51 and 4.0, unless otherwise noted.

Windows Setup

Windows NT 3.51: Make sure that your Windows NT 3.51 is up-to-date with the latest patches and bug fixes, known as Service Pack 4. To check the status of your system, open the Administrative Tools program group and double-click on the Windows NT Diagnostics icon. Select the OS Version button and check the number next to Service Pack. If it is less than 4, you will need to upgrade. This free upgrade can be found at Microsoft’s Web site: www.microsoft.com/ kbd/softlib/winnt.htm. Select “Service Packs” then “Windows NT 3.51 Service Pack 4” to download. Place this self-extracting file in a temporary directory and run it in DOS. It will expand lots of files into this directory. Then, within Windows NT 3.51, choose File ➤ Run Update.exe from within this temporary directory and the update install program will run.

Windows NT 4.0: You will need to download two items from the Rainbow Technologies Web site. (Rainbow Technologies is the manufacturer of the hardware key.) At their site, www.rbt.com/ tech/drivers/drivers.htm, download “Patch for Windows NT 4.0” and “Rainport Driver for Windows NT.” The former is a single executable, NTIOM.EXE. Replace the existing version in your C:\WINNT\SYSTEM32 directory and reboot. This file will be included in Windows NT 4.0 Service Pack 1 when it is built. The latter is the Rainport driver that is explained in the Drivers section.

Installation

The first thing that must be done is the Xilinx install, simply perform a Windows install. Assuming that D:\ is your CD drive, just select File ⚫ Run (or Start ⚫ Run) and type D:\WIN\Install\Wininstall.exe at the prompt. If you are using Viewlogic tools that support Windows NT, (Workview Office, NOT ProSeries), choose the DS-VL-STD-PCI product (not the Stand-alone) from a Custom install. Select the products you would like to install, but keep in mind that you will be using the DOS tools, so programs like the Flooplanner should be deselected.

Change the target path so the interface tools are copied to C:\PROSER instead of C:\XACT and C:\WORKVIEW.

Next, copy the kerm32.dll file from D:\PROSER to both C:\XACT and C:\WORKVIEW.

Then, install the patched version of XNFPREP. This file is located on our FTP server, D:\PROSER to both C:\XACT and C:\WORKVIEW.

The Windows tools will run from D:\PROSER. This directory is included with the Windows tools installation. If the Windows tools are copied to C:\WVOFFICE instead of D:\PROSER, the tools are found in C:\WVOFFICE when the program runs.

Five Million and Counting

Xilinx device #5,000,000 shipped in September. The recipient, Acuson Corporation, a manufacturer of medical electronics systems, was featured at a commencement ceremony.

Since its introduction in the early 1990s, the XC4000 family has quickly grown to become the world’s most successful FPGA product line. The addition of XC4000E devices (and now the XC4000EX versions) to the product family has accelerated the rate of innovation. The XC4000 family reached the million-unit milestone.

As medical technology continues to advance at a phenomenal rate, the success of Acuson more and more depends on our ability to design and deliver the best products possible in the shortest amount of time,” stated Robert Gallagher, Acuson president. “The XC4000 has greatly contributed to our technological vision and has helped us provide cost-effective solutions for the needs of our dynamic marketplace. We are delighted to share in the XC4000’s success.”

New XC9500 ISP Products in Volume Production

Four new XC9500 ISP (In-System Programmable) CPLD devices are now in volume production. The XC9536, XC9572, XC95108 and XC95216 CPLDs are ready for designers looking for the best, most-flexible ISP solution. These 36-, 72-, 108- and 216-macrocell devices, respectively, feature fast, guaranteed performance, the industry’s best pin-locking architecture, a true JTAG-compliant interface, and advanced flash memory technology with up to 10,000 program/erase cycles. The resulting benefits include reduced overall costs, faster time-to-market and the flexibility needed to make design changes anytime during the product life cycle.

New XC9500 ISP Products in Volume Production

Please contact your local Xilinx sales representative for further technical information, price and availability information, or requests for samples of these new ISP CPLD products.

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The XC4000 Series of FPGAs

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The XC4000EX Family Enters Production

The world’s most popular FPGA series just got bigger! Xilinx began shipments of production-qualified XC9500EX devices in November. The XC9500EX offers 6,000,000 logic gates and a typical gate range (logic and memory) of 22,000 to 65,000 gates. Planned devices in the XC9500EX family will range from 26,000 to 128,000 logic gates.

The XC9500EX FPGAs contain all the advanced features of the popular XC4000 and XC9500E architectures. However, several significant enhancements to the architecture address the routing, clock distribution, and I/O needs of higher density devices (See XCell #20, page 21).

Development system software for the XC9500EX family will start shipping in late December. The initial software offering will support Synopsys, Mentor Graphics and Viewlogic EDA environments, as well as workstations from Sun (both SunOS and Solaris) and HP. Please contact your local Xilinx sales representative for the latest availability status.

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X4000 device #5,000,000 shipped in September. The recipient, Acuson Corporation, a manufacturer of medical electronics systems, was featured at a commencement ceremony.

Since its introduction in the early 1990s, the XC4000 family has quickly grown to become the world’s most successful FPGA product line. The addition of XC4000E devices (and now the XC4000EX versions) to the product family has accelerated the rate of innovation. The XC4000 family reached the million-unit milestone.

As medical technology continues to advance at a phenomenal rate, the success of Acuson more and more depends on our ability to design and deliver the best products possible in the shortest amount of time,” stated Robert Gallagher, Acuson president. “The XC4000 has greatly contributed to our technological vision and has helped us provide cost-effective solutions for the needs of our dynamic marketplace. We are delighted to share in the XC4000’s success.”

The XC4000EX Family Enters Production

The world’s most popular FPGA series just got bigger! Xilinx began shipments of production-qualified XC9500EX devices in November. The XC9500EX offers 6,000,000 logic gates and a typical gate range (logic and memory) of 22,000 to 65,000 gates. Planned devices in the XC9500EX family will range from 26,000 to 128,000 logic gates.

The XC9500EX FPGAs contain all the advanced features of the popular XC4000 and XC9500E architectures. However, several significant enhancements to the architecture address the routing, clock distribution, and I/O needs of higher density devices (See XCell #20, page 21).

Development system software for the XC9500EX family will start shipping in late December. The initial software offering will support Synopsys, Mentor Graphics and Viewlogic EDA environments, as well as workstations from Sun (both SunOS and Solaris) and HP. Please contact your local Xilinx sales representative for the latest availability status.
During its first 12 years, Xilinx has continued to maintain every component product line it successfully introduced. We take pride in that. However, as processes migrate to smaller geometries with lower costs, and architectures continue to improve, the economics of overlapping product families dictates that some product life cycles should end.

We are aware that IC users are very wary of product obsolescence. All too often, products are discontinued as a result of business decisions that do not adequately include the customers' perspective. To ensure that we get it right the first time we discontinue a product, Xilinx has taken a different approach and solicited customer input to assist in designing our product obsolescence program.

Our goal is to provide users with ample notification of product discontinuations and ensure adequate supplies of affected products for as long as possible. The program includes "customer advisory" notices as a preview of future product changes and discontinuations, generous last-time-buy periods to allow ample planning and/or redesign time, and relationships with end-of-life suppliers that ensure product availability beyond the Xilinx last-time-buy and last-time-ship periods.

Xilinx Product Discontinuance Policy — The Xilinx Product Discontinuance Policy addresses two situations — where a replacement device exists (PDN1) and where a replacement does not exist (PDN2).

PDN1 — When a form, fit, function replacement exists, the last-time-buy (LTB) period is one year and last-time-ship is 90 days after the LTB period.

PDN2 — When no form fit or function replacement exists, the last-time-buy is two years to allow users the time necessary to completely redesign the board or perform a detailed analysis of LTB requirements.

End-of-Life Supplier — At the end of PDN1 or PDN2, all remaining inventory will be shipped to an end-of-life supplier. The supplier will be able to deliver Xilinx discontinuing products to those users that choose not to exercise the last-time-buy option, or have an unexpected need.

In summary, Xilinx has attempted to take a user-sensitive approach to product obsolescence. Early notification, extended last-time-buy periods and the use of end-of-life suppliers give the user a variety of options to explore and ease any problems resulting from a product discontinuation.

Your comments and suggestions regarding this policy are welcome. Please send all comments to Daniel Chan, Xilinx Marketing, at daniel.chan@xilinx.com.

Embedded Download App Note
Xilinx has developed the tools needed to deliver this powerful capability to designers. The package includes a thoroughly tested, transportable C program, a detailed application note on its use, and the Xilinx EZTAG™ software. The design was initially developed for an 80C51-type microcontroller, but the processor-specific aspects are kept to a minimum, with a simple assembler level call. This keeps all JTAG protocols at the fully transportable ANSI C level, for which there is an abundance of available compilers. The package covers all the necessary details, including the conversion of intermediate files to formats compatible with EPROM programmers.

To obtain the embedded download application note and software, simply access the WebLINX web site at www.xilinx.com and look for the CPLD applications section. Alternately, make your request via e-mail to isp@xilinx.com.

### TECHNICAL SUPPORT RESOURCES

**HOTLINE SUPPORT, U.S.**

Customer Support Hotline: 800-255-7778

Hrs: 8:00 a.m.-5:00 p.m. Pacific time

Customer Support Fax Number: 408-870-4442

E-mail Address: hotline@xilinx.com

Customer Service**: 408-559-7778, ask for customer service

*Call for software updates, authorization codes, documentation updates, etc.

**HOTLINE SUPPORT, INTERNATIONAL**

UK, London Office

telephone: (44) 1932 820281

fax: (44) 1932 820222

Band A Board Service

(44) 1932 333540

E-mail address: abhelp@xilinx.com

France, Paris Office

telephone: (33) 1 346 01 00

fax: (33) 1 346 09 95

E-mail address: frhelp@xilinx.com

Germany, Munich Office

telephone: (81) 3 3297 9163

fax: (49) 89 991 5493

e-mail: dhp@xilinx.com

Japan, Tokyo Office

telephone: (81) 3 3297 9163

e-mail: jhotline@xilinx.com

Germany, Munich Office

telephone: (33) 1 346 01 00

fax: (49) 89 991 5493

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e-mail: jhotline@xilinx.com

**Keeping Up with Changing Standards**

There are many benefits to embedded in-system programming. Products can be updated to the "leading edge" just before shipping and then updated in the field as technology changes, rather than wait to ship until all expected upgrades are complete. For example, this capability could allow a manufacturer to ship products based on new and evolving standards because once a standard has been established, previously shipped systems can be updated in the field to maintain compliance (see Figure 1).

To accommodate potential field upgrades, choose a CPLD device with a robust architecture to ensure that ample speed and capacity are available to tolerate future changes. The XC9500 architecture is specifically designed to tolerate a wide range of changes while retaining the pinouts initially dictated by the PCB design. By choosing the right XC9500 device and including embedded programming capabilities in the system, embedded download success is assured.

### Xilinx Obsolescence Policy

<table>
<thead>
<tr>
<th>Obsolescence Policy</th>
<th>Form, Fit and Function Alternative</th>
<th>Obsolete Ordering Code</th>
<th>Notify to Last Time Buy (LTB)</th>
<th>Last Time Ship (LTS)</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDN1</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>1 year 90 days</td>
<td>XC9500A/H</td>
</tr>
<tr>
<td>PDN2</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>2 years 90 days</td>
<td></td>
</tr>
</tbody>
</table>

*Specification control document (SCD) available to stay with old product for one year.

Xilinx To Discontinue Older XC4000A/H FPGA Devices
Xilinx has announced that it will stop production of two families of field programmable gate array devices in 1997 — the XC4000A and the XC4000H families (older two families of field programmable gate arrays devices in newer devices provide footprint-compatible solutions with substantial cost and performance advantages over the older devices. This marks the first obsolescence of mature Xilinx FPGA devices, and it begins the implementation of one of the industry's most customer-friendly product discontinuation policies. Last-time-orders to buy the XC4000A and XC4000H devices will be accepted until September 30, 1997. Last-time shipments will be made until March 31, 1998.

For more information, contact Daniel Chan, Xilinx Marketing, at daniel.chan@xilinx.com.
Download CPLDs with an Embedded Processor

With its FastFLASH™ technology, supporting access up to 10,000 program/erase cycles, Xilinx XC9500 CPLDs bring all the advantages of in-system programming (ISP) to an advanced CPLD architecture. Embedded processors can be used to control CPLD in-system programming, resulting in considerable benefits throughout the product life cycle, from initial design to field updates.

Why embedded downloading?

Generally, designers download their CPLD patterns through a serial port driven from a PC or workstation during system development and debug. Once the design is stable and high-volume production begins, production-level programming can be switched to third-party programmers (such as those from HP, GenRAD and Teradyne). Increasingly, however, designers need to program parts directly using the onboard microprocessor in an embedded system.

This approach allows changes after field installation with minimal risk to overall system behavior. End users can update their own hardware. For systems with a floppy disk or CD drive, field upgrades can be implemented just like a software update. Remote updating is possible using a modem or other communication link — the embedded controller would capture update information from an external data stream and channel it to the ISP CPLDs on the board, as well as on-board flash memories (or volatile memories).

The non-volatile XC9500 CPLDs do not need reloading with each power cycle. However, because they can coexist in the same JTAG download chain with FPGAs, it may be easier and more convenient to reconfigure CPLDs on the board, as well as on-board flash memories (or volatile memories).

This approach avoids the cost and time normally associated with physical changes to the PC board. Remote updating allows the ability to implement field upgrades to the system, such as modifications to the printed circuit board — perhaps even without opening the system enclosure!

Embedded processors can be used to support in-system programming during design, prototyping, manufacturing or in the field. With sufficient prior planning, extensive design changes can be implemented (if needed) without making external physical changes in the system, such as modifications to the printed circuit board — perhaps even without opening the system enclosure!

Advantages of in-system programming include:

- Faster download time from a PC
- Refined fitter optimization algorithms
- JEDEC programming file generation for improved fitting efficiency
- New CPLD family support and enhancements
- Improved circuit boards and programmers
- Enhanced toolsets and models
- Faster download time from a PC

New CPLD Software Updates

New device support and enhancements have been added to the Xilinx XC9590 CPLD software. Both the core fitter and EZTag™ download software have been enhanced to support XC9500 CPLD family designs.

The latest updates feature:

1. JEDEC programming file generation for the newest member of the XC9500 family, the XC9572-7.
2. Refined fitter optimization algorithms for improved fitting efficiency
3. Newfitter reader improvements to accept Exemplar™ generated netlists
4. ISP algorithm enhancements
5. Faster download time from a PC

HW-130 Device Programmer Update

We work closely with third-party programmer manufacturers to support our products with standard programmer solutions. Our own HW-130 programmer for Xilinx SPROMs and CPLDs supports system development and low-volume programming requirements.

Updated HW-130 interface software is now available for both PC and workstation platforms (DOS, Windows 95, Windows NT, Sun OS, Solaris, HP9000/700 and IBM RS6000 environments). Users can download the files from the bulletin board system, or request the upgrade by contacting a local Xilinx sales representative. The upgrade is free-of-charge to current HW-130 owners.

VITAL Model Support for XC9500 CPLDs

VITAL model support for the XC9500 family is now available from Topdown Design Solutions. These models allow the designer to interface existing gate array VHDL from Xilinx to the SD304 program to simulate and verify the VHDL design. These models are designed, implemented, sold and supported by Topdown Systems.

For additional information, contact Topdown Systems by telephone at 800-435-8435 or by electronic mail at info@topdown.com. Topdown Systems’ web site is located at www.topdown.com.
Implementing Median Filters in XC4000E FPGAs

The median filter is a popular image processing technique for removing salt and pepper (“shot”) noise from images. With this technique, the eight direct neighbors and center point of a sliding 3-by-3 array are examined. The median value of the nine elements replaces the original center pixel. The graph of Figure 1 shows the minimum exchange network required to produce a median from nine input pixels by performing a partial sort.

Figure 1 shows the minimum exchange network required to produce a median from nine input pixels by performing a partial sort. Each node is a two element sort, with the lower input exiting the node on the left, the higher input leaving on the right. The triangular groups of nodes perform a full sort on three elements. The high-speed carry logic of the XC4000E FPGA is used to implement an efficient compare/swap function. The carry logic in each CLB is set up for an A-B subtract function, with CLB is set up for an A-B subtract function, with the carry out of the carry out of the subtractor being controlled by the carry out of the subtraction (Figure 2). Nodes where both outputs are used may be implemented in nine CLBs (eight for the mux, 1/2 for carry out test), nodes where one output is discarded require only five CLBs.

When the circuit is implemented, pipelining can be used so that only three pixels are clocked in at once, eliminating two of the three full sort node groups at the top of the graph (Figure 3). In a system with eight-bit pixels, total CLB usage for this real-time median sort circuit is 85 CLBs.

Figure 2: Using carry logic to perform high-speed compare functions

Figure 3: Pipeline for clocking in three pixels at a time

XC9500 ISP on the HP3070 Tester

With in-system-programming (ISP), programmable logic devices such as XC9500 CPLDs can be programmed and reprogrammed even though they are soldered on a system board. ISP devices can facilitate prototype development, streamline manufacturing flows and enable remote system updates.

The XC9500 family implements ISP functionality using the IEEE 1149.1 (JTAG) Test Access Port (TAP), and without requiring externally applied “supervolatges.” Thus, automatic test equipment (ATE) that supports the JTAG TAP can be used to program XC9500 CPLDs.

HP3070 Configuration and Fixturing

One such ATE platform, the Hewlett Packard HP3070 Board Test System, can perform ISP as an integrated part of the manufacturing test process. The Xilinx EZTag™ software, the Xilinx-supplied vector translation tool (gen_lhp) and an HP3070 ATE system equipped with a Control-Plus card are required in order to integrate XC9500 device programming into the system test flow.

Using EZTag to Generate an SVF file

First, run EZTag to generate a Serial Vector Format (SVF) file from the JEDEC programming file of the target design. The SVF file is in an ASCII format and describes TAP operations. The file encodes the entire programming algorithm for the selected device in the system as a series of TAP instructions. If a readback/verify operation is required after the program step, a separate SVF file with the verification vectors specified should be generated.

Generating an HP 3070 ISP Program

Use the SVF file(s) as input to the “gen_lhp” tool. This tool takes the SVF file(s) and creates a complete HP3070 test program.

This tool runs on the HP workstation that acts as the controller for the HP 3070. The “gen_lhp” program translates the SVF files to the appropriate number of digital Vector Control Language (VCL) files. VCL is the HP9507 stimulus description language.

After generating the VCL file, “gen_lhp” invokes the HP 3070 “dcomp” compiler to generate the “.o” object file from each VCL file. The object file is the executable ATE test program.

Generating an HP 3070 ISP Program

The gen_lhp program also creates a testplan file that drives the test program on the HP 3070. This testplan file can then be incorporated into an existing testplan file to have the in-system programming function executed at the appropriately chosen point in the ATE test flow.

This software and methodology will also work on the following HP testers: the HP3072, HP3073, HP3074, HP3075, HP3079CT, HP3172, HP3973 and HP3975 systems.

Availability

The gen_lhp software and accompanying documentation is available via the Xilinx WebLNX™ (www.xilinx.com) Web site, FTP site (ftp://pub/swhelp/cpld) and BBS (Software Help • CPLD). The SVF to VCL translation tool is currently supported on HP700, SunOS 4.X, Windows NT and Windows 95 platforms.

Procedure used to create an SVF file:

1. Create the design using XABEL-CPLD or any compatible third-party design entry tool.
2. Fit the design and save it to a JEDEC output file.
3. Invoke the EZTag software from the XACT™ command line with the SVF option specified.
4. Generate an SVF file to “program,” “erase” or “verify” the selected part in the boundary-scan chain.
Implementing Median Filters in XC4000E FPGAs

The median filter is a popular image processing technique for removing salt and pepper (“shot”) noise from images. With this technique, the eight direct neighbors and center point of a sliding 3-by-3 array are examined. The median value of the nine elements replaces the original center pixel. The median of the 3-by-3 array is the fifth element in the sorted list of nine elements; thus, the algorithm requires a high-speed sort of the nine pixel values.

The graph of Figure 1 shows the minimum exchange network required to produce a median from nine input pixels by performing a partial sort. Each node is a two element sort, with the lower input exiting the node on the left, the higher input leaving on the right. The triangular groups of nodes perform a full sort on three elements. The high-speed carry logic of the XC4000E FPGA is used to implement an efficient compare/swap function. The carry logic in each CLB is set up for an A-B subtract function, while the function generators are used to implement a 2:1 multiplexer. The multiplexer is controlled by the carry out of the subtraction (Figure 2). Nodes where both outputs are used may be implemented in nine CLBs (eight for the max, 1/2 for carry chain initialization, and 1/2 for carry out test), nodes where one output is discarded require only five CLBs.

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First, run EZTag to generate a Serial Vector Format (SVF) file from the JEDEC programming file of the target design. The SVF file is in an ASCII format and describes TAP operations. The file encodes the entire test program into the system test flow.

Generating an HP 3070 ISP Program

Use the SVF file(s) as input to the “gen_hp” tool. This tool takes the SVF file(s) and creates a complete HP3070 test program. This tool runs on the HP workstation that acts as the controller for the HP 3070. The “gen_hp” program translates the SVF files to the appropriate number of digital Vector Control Language (VCL) files. VCL is the HP3070 stimulus description language.

One such ATE platform, the Hewlett-Packard HP1070 Board Test System, can be used to perform ISP on a XC9500 device on the HP 3070. The “gen_hp” program also creates a testplan file that drives the test program on the HP 3070. This testplan file can then be incorporated into an existing testplan file to have the in-system-programming function executed at the appropriately chosen point in the ATP test flow.

Using VCL to Generate an SVF File

The “gen_hp” program also creates a Vector Control Language (VCL) file. VCL is available via the Xilinx WebLINX™ (www.xilinx.com) web site, FTP site (//pub/swhelp/cpld) and BBS (Software Help • CPLD). The SVF to VCL translation tool is currently supported on HP60, SunOS 4.X, Windows NT and Windows 95 platforms.

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2. Fit the design and save it to a JEDEC output file.
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Downloading CPLDs with an Embedded Processor

With its FastFLASH™ technology supporting up to 10,000 program/erase cycles, Xilinx XC9500 CPLDs bring all the advantages of in-system programming (ISP) to an advanced CPLD architecture. Embedded processors can be used to control CPLD in-system programming, resulting in considerable benefits throughout the product life cycle, from initial design to field updates.

Why embedded downloading?

Generally, designers download their CPLD patterns through a serial port driven from a PC or workstation during system development and debug. Once the design is stable and high-volume production begins, production-level programming can be switched to third-party programmers (such as those from HP, GenRAD and Teradyne). Increasingly, however, design changes on its "own" board fits the embedded system.

This approach allows changes after field installation with minimal risk to overall system behavior. End users can update their own hardware. For systems with a floppy disk or CD drive, field upgrades can be implemented just like a software update. Remote updating is possible using a modem or other communication link — the embedded controller would capture update information from an external data stream and channel it to the ISP CPLDs on the board, as well as on-board flash memories (or volatile memories).

The non-volatile XC9500 CPLDs do not need reloading with each power cycle. However, because they can coexist in the same JTAG download chain with FPGAs, it may be easier and more convenient to reload their configurations during every power-up sequence. The 10,000 reprogramming cycles offered by XC9500 CPLD FastFLASH™ technology makes that strategy possible. By using the advanced JTAG capabilities contained in the XCS9500 devices, the internal UserCode register can maintain a reprogramming counter, if needed.

New CPLD Software Updates

New device support and enhancements have been added to the Xilinx XC9500 CPLD software. Both the core fitter and EZTag™ download software have been enhanced to support XC9500 CPLD family designs.

The latest updates feature:
1. JEDEC programming file generation for the newest member of the XC9500 family, the XC9572-7.
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VITAL Model Support for XC9500 CPLDs

VITAL model support for the XC9500 CPLD family is now available from Topdown Design Solutions. These models allow the designer to generate timing-accurate, gate-level VHDL from Xilinx Virtex and Zynq models. VBAK-VITAL models are designed to work with the Model 2000 simulator. These models are designed, implemented, sold and supported by Topdown Systems.

For additional information, contact Topdown Systems by telephone at 800-438-8435 or by electronic mail at info@topdown.com. Topdown Systems’ website is located at www.topdown.com.
# Product Obsolescence Policy

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**PDN2** — When no form fit or function replacement exists, the last-time-buy is two years to allow users the time necessary to completely redesign the board or perform a detailed analysis of LTB requirements.

### End of Life Supplier

At the end of PDN1 or PDN2, all remaining inventory will be shipped to an end-of-life supplier. The supplier will be able to deliver Xilinx discontinued products to those users that choose not to exercise the last-time-buy option, or have an unexpected need.

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Your comments and suggestions regarding this policy are welcome. Please send all comments to Daniel Chan, Xilinx Marketing, at daniel.chan@xilinx.com.

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## TECHNICAL SUPPORT RESOURCES

### HOTLINE SUPPORT, U.S.

**Customer Support Hotline:** 800-255-7778

Hrs. 8:00 a.m. - 5:00 p.m. Pacific time

**Customer Support Fax Number:** 408-879-4442

**E-mail Address:** hotline@xilinx.com

**Customer Service:** 408-559-7778, ask for customer service

---

### HOTLINE SUPPORT, INTERNATIONAL

**UK, London Office**

telephone: (44) 1932 820821

fax: (44) 1932 820822

**Bulletin Board Service:** telephone: (44) 1932 820822

**E-mail:** ukhelp@xilinx.com

**France, Paris Office**

telephone: (33) 1 3463 0959

fax: (33) 1 3463 0929

**E-mail:** ifrhelp@xilinx.com

**Germany, Munich Office**

telephone: (49) 89 991 54930

fax: (49) 89 940 4748

**E-mail:** dhelp@xilinx.com

**Japan, Tokyo Office**

telephone: (81) 3 3297 9163

fax: (81) 3 3297 0167

**E-mail:** jhelp@xilinx.com

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## Embedded Download App Note

Xilinx has developed the tools needed to deliver this powerful capability to designers. The package includes a thoroughly tested, transportable C program, a detailed application note on its use, and the Xilinx EZTag™ software. The design was initially developed for an 8051-type microcontroller, but the processor-specific aspects are kept to a minimum, with a simple assembler level call. This keeps all JTAG protocols to the fully transportable ANSI C level, for which there is an abundance of available compilers. The package covers all the necessary details, including the conversion of intermediate files to formats compatible with EPROM programmers.

To obtain the embedded download application note and software, simply access the WebLinx web site at www.xilinx.com and look for the CPLD applications section. Alternately, make your request via e-mail to ipx@xilinx.com.

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## Xilinx To Discontinue Older XC4000A/H FPGA Devices

Xilinx has announced that it will stop production of two families of field-programmable gate arrays devices in 1997 — the XC4000A and the XC4000H families (older variations of the XC4000 Series of products). The XC4000E, XC4000EX and XC4000D families will not be affected. Users of these devices can replace them with newer Xilinx XC4000E and XC5200 FPGA family products, these newer devices provide footprint-compatible solutions with substantial cost and performance advantages over the older devices.

This marks the first obsolescence of mature Xilinx FPGA devices, and it begins the implementation of one of the industry’s most customer-friendly product discontinuation policies. Last-time-orders to buy the XC4000A and XC4000H devices will be accepted until September 30, 1997. Last-time shipments will be made until March 31, 1998.

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Xilinx home page on the World Wide Web: www.xilinx.com

Electronic Technical Bulletin Board (U.S.) 408-559-9327

XDOCS E-mail document server: send an E-mail to xdoc@xilinx.com

Embedded Download App Note

E-mail addresses for questions on specific applications:

Digital Signal Processing applications: diap@xilinx.com

PC-based applications: pcb@xilinx.com

Plug and Play ISA applications: ppi@xilinx.com

PCMCIA card applications: pcmcia@xilinx.com

Synchronous Transfer ATA applications: ata@xilinx.com

Reconfigurable Computing applications: recconf@xilinx.com

In System Programmable CPLD applications: isp@xilinx.com

Universal Serial Bus applications: usb@xilinx.com

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## Keepin Up with Changing Standards

There are many benefits to embedded in-system programming. Products can be updated to the “leading edge” just before shipping and then updated in the field as technology changes, rather than wait to ship until all expected upgrades are complete. For example, this capability could allow a manufacturer to ship products based on new and evolving standards because once a standard has been established, previously shipped systems can be updated in the field to maintain compliance (see Figure 1).

To accommodate potential field upgrades, choose a CPLD device with a robust architecture to ensure that ample speed and capacity are available to tolerate future changes. The XC9500 architecture is specifically designed to tolerate a wide range of changes while retaining the pinouts initially dictated by the PCB design. By choosing the right XC9500 device and including embedded programming capabilities in the system, embedded download success is assured.
Running XACTstep™ v5.2.1 in a Windows environment

XACTstep™ version 6.0.x (the Windows tools) was compiled and tested for Windows 3.x. It was not compiled for Windows NT. Unlike Windows 95, there is no work-around to enable the Windows tools to work. This release does NOT support Windows NT.

However, we have had some success using XACTstep v5.2.1 (the DOS tools) within a DOS session under Windows NT. There are a few things that must be done to set up the environment, as described below.

1. Please note that the next full release of Xilinx software will support Windows NT 4.0. The solution described here should be considered a tactical work-around for Windows NT 3.51 and 4.0. All of the instructions apply to both Windows NT versions 3.51 and 4.0, unless otherwise noted.

Windows Setup

Windows NT 3.51: Make sure that your Windows NT 3.51 is up-to-date with the latest set of patches and bug fixes, known as Service Pack 4. To check the status of your system, open the Administrative Tools program group and double-click on the Windows NT Diagnostics icon. Select the OS Version button and check the number next to Service Pack. If it is less than 4, you will need to upgrade. This free upgrade can be found at Microsoft’s Web site: www.microsoft.com/technet/nt/whatisnew/sp4.htm. Select “Service Packs” then “Windows NT 3.51 Service Pack 4 for Intel (x86)” to download. Place this self-extracting file in a temporary directory and run it in DOS. It will expand lots of files into this directory. Then, within Windows NT 3.51, choose File ➤ Run Update.exe from within this temporary directory and the update install program will run.

Windows NT 4.0: You will need to download two items from the Rainbow Technologies Web site. (Rainbow Technologies is the manufacturer of the hardware key.) At their site, www.rnbo.com/tech/drivers/drivers.htm, download “Patch for Windows NT 4.0” and “Rainport Driver for Windows NT.” The former is a single executable, NTVID.MXE. Replace the existing version in your C:\WINNT\SYSTEM32 directory and reboot. This file will be included in Windows NT 4.0 Service Pack 1 when it is built. The latter is the Rainport driver that is explained in the Drivers section.

Installation

The first thing that must be done is the Xilinx install, simply perform a Windows install. Assuming that D: \ is your CD drive, just select File ➤ Run (or Start ➤ Run) and type D:\WIN\Install\Install.exe at the prompt. If you are using Viewlogic tools that support Windows NT, (Workweek Office, NOT PROseries), choose the DS-VL-STD-PCI product (not the Stand-alone) from a Custom install. Select the products you would like to install, but keep in mind that you will be using the DOS tools, so programs like the Floormappler should be de-selected. Change the target path so the interface tools are copied to C:\XACT and C:\WVOFFICE instead of C:\PROSER.

Next, copy the kme3432.dll file from D:\PROSER to both C:\XACT and C:\WVOFFICE.

Then, install the patched version of XNFPREP. This file is located on our FTP site as XNFPREP. This file is located on our FTP site at the prompt. If you are using Viewlogic tools to enable the

New XC9500 ISP Products in Volume Production

Four new XC9500 ISP (In-System Programmable) CPLD devices are now in volume production. The XC9536, XC9572, XC95108 and XC95216 CPLDs are ready for designers looking for the best, most-flexible ISP solution. These 36-, 72-, 108- and 216-macrocell devices, respectively, feature fast, guaranteed performance, the industry’s best pin-locking architecture, a true JTAG-compliant interface, and advanced flash memory technology with up to 10,000 reprogram/erase cycles. The resulting benefits include reduced overall costs, faster time-to-market and the flexibility needed to make design changes anytime during the product life cycle.

THE XC4000 SERIES OF FPGAS:
Five Million and Counting

The world’s most popular FPGA series just got bigger! Xilinx began shipments of production-qualified XC9500EX devices in November. The XC9400EX offers 6,000 maximum logic gates and a typical gate rate (logic and memory) of 22,000 to 65,000 gates. Planned devices in the XC9500EX family will range from 26,000 to 120,000 logic gates.

The XC9500EX FPGAs contain all the advanced features of the popular XC4000 and XC4000E architectures. However, several significant enhancements to the architecture address the routing, clock distribution, and I/O needs of higher density devices than the XC9500EX.

The XC4000EX Family Enters Production

The XC4000 family has quickly grown to become the world’s most successful FPGA product line. The addition of XC4000EX devices (and now the XC4000EX versions) to the product family has accelerated the rate of delivery. The XC4000EX family includes over 100 devices that range from 25,000 to 125,000 logic gates.

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TECHNICAL TRAINING UPDATE

One-Day VHDL Seminar Now Available

Xilinx is sponsoring a series of one-day introductory VHDL seminars conducted by qualified instructors from Esperan Inc. Esperan specializes in technical training and has educated thousands of VHDL users since 1992. This one-day course, a must for new users, emphasizes the basics of the VHDL language.

A full day of lecture and hands-on labs, the seminar uses the VHDL tool offered by Xilinx in the Foundation Series™. The tuition fee is $99. Feedback from participants has been extremely positive; extra seminars have been added to the schedule to meet demand.

Each attendee receives an evaluation kit of the Xilinx software. This provides ample opportunity to practice the skills and knowledge obtained at the seminar. The kit includes the Foundation Series software, an integrated tool set of schematic entry, VHDL synthesis, functional and timing simulation and design implementation tools; everything needed to create an entire design.

Documents accompanying the seminar are available to XUP participants, and further information about this workshop and future XUP workshops can be obtained on the Xilinx web site at www.xilinx.com/programs/univ.htm.

The current schedule of schematic- and synthesis-based courses, as well as course registration information, can be found at the WebLINX web site (www.xilinx.com). ☞

Windows NT Environment

Xilinx is committed to addressing the needs of the reconfigurable logic market, and the Xilinx University Program is committed to further academic support of this exciting area of study. Proceedings from the workshop are available to XUP participants, and further information about this workshop and future XUP workshops can be obtained on the Xilinx Technical Support for assistance. ☞

First Hands-On Workshop on Reconfigurable Computing

The Xilinx University Program (XUP) has had an active training schedule with nine recent workshops in four countries. XUP workshops are designed to train university instructors on the basics of using programmable logic for undergraduate courses, graduate courses and research.

In addition to the standard workshops, and in response to a growing interest in dynamically-reconfigurable logic, a unique, leading-edge workshop was held at Cornell University (Ithaca, NY).

The Cornell workshop was the first to examine both the hardware and software issues associated with dynamically-reconfigurable computing, including hands-on laboratory exercises. Participating lecturers included representatives from Xilinx, the Virginia Institute of Technology, ETH Zurich, Cornell University, and Imperial College (UK). Mr. Nick Treddinick, an IEEE fellow, presented the keynote address.

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Can XACT/step 5.2.1 be used with Mentor Graphics’ Bx release?

As Under Mentor Bx, Gen_sch and XBLXG5 may fail with either “call to undefined procedure” (SunOS) or “ unresolved propagate error messages due to problems with dynamically linking to Mentor’s Design Data Port (DDP). A patch is available to fix these problems and make XACT/step 5.2.1 interface smoothly with Mentor Bx. The patch may be downloaded from the Xilinx FTP site at: http://ftp.xilinx.com/pub/swhelp/mentor/b1_521.tar.Z (SunOS) http://ftp.xilinx.com/pub/swhelp/mentor/b1_521.tar.Z (HPUX).

A schematic originally targeted for the XC4000 family is now targeting an XC4000E device. During Men2XNF, the following error occurs when running EDIF2XNF:

• Targeting an XC4000E device. During the Xilinx Foundation Series software?

A schematic or set of schematics so that they come from the proper library. For example, you can create a SmartSearch Agent that will alert you regarding any new application notes posted to the Xilinx site by following these steps:

2. Click on the “Register Now for Agents!” link at the bottom of the page.
3. Fill in the registration information.
4. Click on the “Register” button.
5. Click on the “Add New Application Note” link.
6. Select the “application notes” check box.
7. Leave the text box blank but select the “summary” check box.
8. Click on the “Save Search Settings” button. On the results page, in the upper right corner is a text box with the label “Agent Name”.
9. Type “Xilinx Application Notes” into the agent name box and click on the Create button.

WEBLINK

WebLINK (www.xilinx.com) has become a popular stopping place on the information superhighway. Based on recent traffic reports, more than 5,000 people visit the Xilinx World Wide Web site each week. Some of the most popular areas of our web include SmartSearch, Product Information pages, Application Notes and the Data Book page.

We’re constantly adding new information to WebLINK. In fact, over the last few months we have added many new application notes and application briefs to the site, as listed here...

If you are interested in keeping up-to-date with new technical information being posted to WebLINK, then SmartSearch Agents are for you. A SmartSearch Agent will automatically notify you via e-mail when a document of interest to you is posted to any of the 50 or so sites that we monitor. A SmartSearch Agent may send you e-mail notification when a certain XAPP or XBRF is posted to WebLINK.

In the following, the XAPP application notes and XBRF application briefs have recently been added to WebLINK. You can find these by first going to the application note page and selecting XAPP application notes or application briefs.

• XAPP031 Synchronous/Asynchronous FIFOs
• XAPP052 Efficient Shift Registers, USB Counters, etc.
• XAPP053 Implementing FIFOs in XC4000 Series RAM
• XAPP054 Constant Coefficient Multipliers for the XC4000E
• XAPP055 Block Adaptive Filter
• XAPP064 Interfacing XC6200 to Microprocessors (TMS320C50 Example)

In addition, the following application notes have been updated:

• XAPP013 Using the Dedicated Carry Logic in XC4000E
• XAPP018 Estimating the Performance of XC4000E Adders and Counters

Xilin Application Briefs are technical papers describing the advantages of Xilinx products, especially versus alternative solutions:

• XBRF001 XC4000E Select-RAM Flexibility with Speed
• XBRF002 XC4000E Lower Power Consumption: At High Speed
• XBRF003 XC4000E Select-RAM Maximum Configurability
• XBRF004 XC4000EX Routing: A Comparison with XC4000E and ORCA
• XBRF005 PLL Design Techniques and Usage in FPGA Design

For more information on the Xilinx Solutions Database, see Solution 798, “Retargeting a design in the XC4000 family is now targeted to an XC4000E device. (Other family combinations may also cause this error) Certain symbols are primitives in the schematic library associated with the device targeted (XC4000E). In this example, OFD is a primitive within the XC4000 library but is a macro in the XC4000E library (since it has, underneath it, the clock-enabled OFDIX symbol).

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Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative.

<table>
<thead>
<tr>
<th>TITLE</th>
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<td>Features &amp; Benefits</td>
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<tr>
<td>Software Solutions Brochure</td>
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Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676).

**UPCOMING EVENTS**

- **Design SuperCon**
  - Jan. 21-25
  - Santa Clara, California

- **ACM/SIGDA 5th International Symposium on FPGAs**
  - Feb. 9-11
  - Monterey, California

- **International Integrated Circuits Conference**
  - March 17-18
  - Shanghai, China

- **European Design and Test Conference**
  - March 17-20
  - Paris, France

- **Intellectual Property in Electronics Seminar**
  - March 17-18
  - Santa Clara, California

- **Semiconductor Solutions Conference**
  - March 18-20
  - Birmingham, United Kingdom

- **Design SuperCon**
  - March 15-14
  - Beijing, China

**FINANCIAL RESULTS**

For the first time, Xilinx Inc. quarterly sales revenues declined from both the prior quarter and the year ago period. Revenues for the September-ending quarter were $150.6 million, a decrease of 13.1% from the immediately preceding quarter and 7.5% from the same quarter one year ago.

“However, we are encouraged by the nearly 1,400 new software seats that we sold this quarter, 70% of which are versions of our new shrink-wrapped, low-cost Foundation™ software,” Roelandts continued. “We are also optimistic that our new XC9500 and XC4000EX families will provide meaningful contributions to revenues before our fiscal year end.”

Xilinx Inc. stock is traded on NASDAQ under the symbol XLNX.

What is happening when Quicksim issues this warning of every primitive in a design:

```plaintext
Warning: Instance "/GIVE_ME_AN_E" Could not find a registered simulation model with label: "xc4000" NULL model will be inserted. (from: Analysis/Digital/Simulation Utilities/MAIN 85)
```

This is caused by an incorrectly-written simulation viewpoint for the design, which may result when a design is retargeted to a new device family. The solution is to delete that default viewpoint, then run PLD_DVE_SIM on the design, specifying the correct part family. If done from the command line, an XC4000 design, for example, might use:

```plaintext
delete_object blanking_design/default pld_dve_sim blanking_design xc4000
```

Note: If Timsim® -o was used to create the simulation model, be sure to run Timsim® instead of PLD_DVE_SIM. Timsim® -o runs PLD_DVE_SIM, then adds links to timing information into the viewpoint afterwards.

How are Boundary Scan components for the XC4000 family instantiated in Verilog-based designs?

To use Boundary Scan components in XC4000 Series devices, instantiate the boundary scan symbol (BSCAN) and the associated dedicated I/O. Use the ‘dont_touch’ attribute, otherwise, BSCAN may be deleted by the Synopsys compiler.

The Verilog code for instantiating BSCAN in the XC4000 is shown below. VHDL and Verilog examples for both the XC4000 and XC5000 can be found on the Xilinx Web site (www.xilinx.com), or can be emailed to users via the Xdocs mail server (email xdocs@xilinx.com).

**Synopsys RUnscript for compiling the XC4000/XC4000E BSCN Verilog Example:**

```plaintext
PART = xc4000
TOP = example
read -format verilog "bscan4k.v"
set_part_is_pad "" insert_pads
set_dont_touch u1
set_dont_touch u2
set_dont_touch u3
set_dont_touch u4
set_dont_touch u5
compile
replace_fps
set_attribute TOP "part" -type string
PART
write -f xnf -h -o "bscan4k.xsnf"
```
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<tr>
<td>240</td>
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**COMPONENT AVAILABILITY CHART**

Xilinx Joins Virtual Socket Interface Alliance

Last September, a group of more than 35 leading electronics firms announced the formation of the Virtual Socket Interface (VSI) alliance. This open alliance is dedicated to promoting the growth of the system-level integration (SLI) chip industry by developing the technical standards required to enable the “mix and match” of system-level modules (SLMs). Xilinx has entered the VSI alliance, and is actively participating in standardization efforts affecting programmable logic technologies. Our participation augments our current programs for the development of a diverse set of high-quality SLMs, called LogiCore™ modules, for the various Xilinx FPGA and CPLD families.

The goal is to establish a set of open SLM design interface and productionization standards. Through use of the developed standards, design engineers will be able to use SLMs from several sources in the design of highly-integrated programmable logic devices. For example, a designer could construct a system combining SLMs supplied by Xilinx (such as the LogiCore PCI master/slave), SLMs from third-party providers (such as the members of the Xilinx LogiCore Alliance), and reusable modules from his/her previous designs.

SLMs from all sources will be designed to common standards, much like physical components that are mixed-and-matched today on a printed circuit board. These VSI-compliant SLMs can be viewed as “virtual components” that, through common interface standards, fit quickly into “virtual sockets.” In order to rapidly provide a solution, the design data standards will be based on open formats commonly supported by all EDA vendors.

High-quality SLMs are a key component for high-performance and high-density programmable logic design. The use of predefined and pre-verified SLMs can dramatically reduce system development cost and time, resulting in faster time-to-market and a greater competitive advantage.

For further information about the VSI Alliance, see their web site at www.ipnet.org. For additional information about the LogiCore products and LogiCore Alliance Program, see the WebLINX web site at www.xilinx.com/products/logicore/logicore.htm.

New AppLINX CD-ROM Shipped

An updated AppLINX CD-ROM has been shipped to all registered Xilinx users. The CD contains a complete collection of Xilinx applications and product information. Access to the AppLINX CD is another benefit of maintenance support for the Xilinx development system.

The AppLINX CD-ROM includes:

- Presentation notes for the Xilinx 1996 Fall Seminar
- The AppLINX CD merges the best aspects of the Xilinx WebLINX web site and the Xilinx FTP site. Users with access to an HTML browser can navigate the files quickly and easily off-line, while links are available to find the latest information on-line.
- The AppLINX CD will be updated on a regular basis. Make sure you visit the Xilinx WebLINX web site at www.xilinx.com for the latest information.
- Regarding the fall seminar, contact your local Xilinx sales office to inquire about a presentation to your company.
MiroTech Microsystems: Real-Time Reconfigurability for DSP Acceleration

Our congratulations to the development team at MiroTech Microsystems Inc. (Montreal, Canada). MiroTech Microsystems has released a commercial product that uses reconfigurable computing to advance the state-of-the-art for DSP acceleration. At the most recent ICSCAT/DSP World Exposition in Boston, MiroTech Microsystems announced an exclusive North American agreement with Spectrum Signal Processing Inc. to distribute MiroTech’s FPGA-based DSP acceleration module.

MiroTech’s X-CIM module complements Spectrum’s extensive PCI, VXI and VME C4x-based DSP product line. Together these products provide substantial acceleration for selected compute-intensive, high-performance applications.

X-CIM is an FPGA-based reconfigurable computer in a TIM form factor that is fully-compliant with Texas Instruments’ TMS320C40 DSP processor. The module features 8 Mbytes/s communication bandwidth, 50 ms on-the-fly reconfigurability, and hardware-implemented parallel processing. It’s a sophisticated, highly portable architecture based on Xilinx reconfigurable FPGAs and banks of high-speed RAM.

As the tendency towards more complex DSP systems continues to grow, designers are constantly seeking new ways to reach higher performance and to unravel bottlenecks while reducing development costs. "What is unique with our X-CIM is its substantial acceleration for very compute-intensive systems while staying within Spectrum’s C40 environment and DSP development tools. X-CIM modules are supported by a comprehensive suite of software tools referred to as COREKIT. With these tools, developers can transparently accelerate a wide range of DSP functions in applications such as radar, sonar, voice and image processing," noted MiroTech President and CEO Pierre Popovic. "The X-CIM module can deliver acceleration up to 100 times that of a general-purpose DSP processor for highly repetitive ‘inner loops’ within algorithms."

The marriage of the X-CIM module with Spectrum’s products allows the design of very compute-intensive systems while staying within Spectrum’s C40 environment and DSP development tools. X-CIM modules are supported by a comprehensive suite of software tools referred to as COREKIT. With these tools, developers can transparently accelerate a wide range of DSP functions in applications such as radar, sonar, voice and image processing.

For more information on the X-CIM product line, contact MiroTech Microsystems Inc. at 514-556-0060 or at MiroTech@montreal.com.

The Xilinx Reconfigurable Computing Developer’s Program is promoting the commercial use of FPGAs in reconfigurable computing applications. This program adds significant value by dynamically changing FPGA designs, in real-time, while the system is operating. Applications that can exploit the benefits of the RC concept include graphics, audio processing, and data communications.

For more information on the Xilinx Developer's Program and our reconfigurable computing efforts, please visit our website at www.xilinx.com, or call John Watson at 408-879-6584.
In the GigaBooster system, the controller was redesigned into three XC4013 FPGAs to allow room for expansion. One FPGA holds several small state machines, an abundance of control registers, and other glue and interconnect logic; this design uses about half of the available logic blocks, but all of the I/O pins. The other two FPGAs implement the logic directly involved in the gathering and redistribution of data from the processing elements, including a 42-bit counter and a large register/comparator file for each PE. The first of these FPGAs is more than 90% utilized, and connects to five of the processing elements.

About 40% of the second FPGA contains logic directly involved in the gathering and redistribution of data from the processing elements, including a 42-bit counter and a large register/comparator file for each PE. The first of these FPGAs is more than 90% utilized, and connects to five of the processing elements.

The FPGA designs were developed on a Sun workstation using Viewlogic's implementation. The design runs at 20 MHz.

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The FPGA designs were developed on a Sun workstation using Viewlogic's implementation. The design runs at 20 MHz.
To implement the critical communications control logic, they chose the world’s leading FPGA family — the XC4000 Series.

Based on the “alpha7” prototype system, they developed a new communications protocol called Intelligent Communication was developed to provide fast communications and communications controller realized within three microseconds. Each PE is dedicated to interprocessor communications and connected to a common 72-bit bus. All the special registers and FIFO buffers are controlled by a central communications controller.

During the development of the “alpha7,” several approaches were tested and compared. This protocol was implemented in Xilinx FPGAs. All the PE’s run the Digital UNIX operating system, providing access to over 3000 applications.

A new communications protocol called Intelligent Communication was developed to provide fast communications and communication controller realized within three microseconds. Each PE is dedicated to interprocessor communications and connected to a common 72-bit bus. All the special registers and FIFO buffers are controlled by a central communications controller.

This protocol, implemented directly in hardware using the FPGA devices, allows fast, low-latency communication control, enabling the system to take full advantage of the FPGA’s parallel processing power. This protocol is implemented in two XC4013 devices.

Changes since last issue printed in color; 1736A, 1765 and 17128 columns eliminated since last issue.
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Stream designers have critical business issues to focus on: high-density, high-performance programmable logic design solutions are providing new possibilities for solving for designs at the gate level is no longer a realistic consideration. However, advanced tools and techniques are required to meet the challenges of the future. New core technology includes timing-driven optimization, mapping, FPGA placement and routing algorithms that allow for higher-gate-count designs. Xilinx SLI options merge between Xilinx and NeoCAD. This merger between Xilinx and NeoCAD is a result of the industry's most tightly-integrated with their established methodologies and support industry standards. The solutions and partnerships provide the appropriate combination of high-levels of performance in programmable logic blocks and enable complex, high-speed, high-performance designs. These tools can support the latest technologies, such as Rapid Prototyping, XACT and Foundation Series products, current SLI designs in their chosen third-party EDA environment.

Through the Xilinx Alliance Program, integrated design solutions and partnerships provide many benefits for the design of Xilinx devices, as well as ensuring rapid and efficient tools, such as automatic test generation and simulation. These tools can dramatically shorten development and testing of the interface to XACT software. The industry-leading technologies from the alliance are based on the Xilinx and NeoCAD solution for these products.

The upcoming next-generation core software platform incorporates our next-generation XACT core software. This new release will still incorporate the latest XACT technology as well as providing new capabilities and features. It will be designed to meet the needs of advanced designers and support advanced technologies. As previous versions of XACT were released, new technologies and design methodologies have been developed, providing new capabilities and features for these products. Future XACT versions will incorporate these changes and provide enhanced capabilities for advanced designers.

**GUEST EDITORIAL**

**The Alliance Program,** the alliance of EDA companies and Xilinx, has been established to provide the highest quality third-party EDA tools for Xilinx products. Currently, the Xilinx Alliance Program includes a number of companies who have been selected for their contributions to Xilinx development and their responses to the widest variety of high-quality third-party EDA suppliers. The Alliance Program is a set of technology partners and tools that are integrated with Xilinx's own tools, providing a seamless interface to Xilinx's design tools. These partners include EDA vendors, who provide tools certified to work with Xilinx products. They prefer to leverage their previous investments and expertise in the design of Xilinx devices, as well as ensuring rapid and efficient tools, such as automatic test generation and simulation, for designs in their chosen third-party EDA environment.

In summary, upcoming releases of the new core software platform will provide many benefits for the design of Xilinx devices, as well as ensuring rapid and efficient tools, such as automatic test generation and simulation, for designs in their chosen third-party EDA environment.
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<tr>
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Inquiries about the Xilinx Alliance Program can be e-mailed to alliance@xilinx.com

Changes since last issue (XCell 22) printed in color. • The following two entries deleted: ITS, The Rockland Group
FROM THE FAWCET

By BRADLY FAWCETT

Every user of programmable logic at one point has the question, "How large a device will I require to fit my design?" At some point, all users have to select the most cost-effective solution for their programmable logic needs, who must sift through the complexity of available programmable logic devices to select the best one (or ones) for their different projects. Since each family of devices offers a unique set of logic functions, designers can end up comparing apples and oranges.

The proliferation of available programmable logic devices presents a unique set of challenges to designers, who must determine the accuracy of the various design methodologies for their particular application. This accuracy is a product of the design methodology chosen and the potential for error in the designer's logic function. It is also a product of the design methodology chosen and the potential for error in the designer's logic function. It is also a product of the design methodology chosen and the potential for error in the designer's logic function.

In the world of programmable logic, there are three types of falsehoods - lies, damned lies and statistics. The first one of these is a lie - the second is damned lies - and the third is statistics. These days reminds me of the old saying about the fox and the grapes.

Most vendors, including Xilinx, describe device capacities in terms of "gate counts," which is the number of gates implemented on the die of the device. But due to the increasing complexity of programmable logic devices, "gate counting" is no longer an accurate indication of the capacity of our devices compared to other manufacturers' competing products. Unfortunately, some vendors describe their devices by "gate counting," which presents a tremendous problem for potential programmable logic users, who must sift through the complexity of available programmable logic devices to select the best one (or ones) for their different projects.

One of the most difficult problems facing those of us who make, market, and sell programmable logic devices is how to accurately indicate the capacity of our devices compared to other manufacturers' competing products. Unfortunately, some vendors describe their devices by "gate counting," which presents a tremendous problem for potential programmable logic users, who must sift through the complexity of available programmable logic devices to select the best one (or ones) for their different projects.

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