



XC9500 ISP on the HP3070 Tester

With in-system-programming (ISP), programmable logic devices such as XC9500 CPLDs can be programmed and reprogrammed even though they are soldered on a system board. ISP devices can facilitate prototype development, streamline manufacturing flows and enable remote system updates.

The XC9500 family implements ISP functionality using the IEEE 1149.1 (JTAG) Test Access Port (TAP), and without requiring externally applied “supervoltages.” Thus, automatic test equipment (ATE) that supports the JTAG TAP can be used to program XC9500 CPLDs.

HP3070 Configuration and Fixturing

One such ATE platform, the Hewlett Packard HP3070 Board Test System, can perform ISP as an integrated part of the manufacturing test process. The Xilinx EZTag™ software, the Xilinx-supplied vector translation tool (gen_hp) and an HP3070 ATE system equipped with a Control-Plus card are required in order to integrate XC9500 device programming into the system test flow.

Using EZTag to Generate an SVF file

First, run EZTag to generate a Serial Vector Format (SVF) file from the JEDEC programming file of the target design. The SVF file is in an ASCII format and describes TAP operations. The file encodes the entire programming algorithm for the selected device in the system as a series of TAP instructions. If a readback/verify operation is required after the program step, a separate SVF file with the verification vectors specified should be generated.

Generating an HP 3070 ISP Program

Use the SVF file(s) as input to the “gen_hp” tool. This tool takes the SVF file(s) and creates a complete HP3070 test program.

This tool runs on the HP workstation that acts as the controller for the HP 3070. The “gen_hp” program translates the SVF files to the appropriate number of digital Vector Control Language (VCL) files. VCL is the HP3070 stimulus description language.

After generating the VCL file, “gen_hp” invokes the HP 3070 “dcomp” compiler to generate the “.o” object file from each VCL file. The object file is the executable ATE used to perform ISP on a XC9500 device on the HP3070.

The “gen_hp” program also creates a testplan file that drives the test program on the HP 3070. This testplan file can then be incorporated into an existing testplan file to have the in-system programming function executed at the appropriately chosen point in the ATE test flow.

This software and methodology will also work on the following HP testers: the HP3072, HP3073, HP3074, HP3075, HP3079CT, HP3172, HP3173 and HP3175 systems.

Availability

The gen_hp software and accompanying documentation is available via the Xilinx WebLINX™ (www.xilinx.com) web site, FTP site (/pub/swhelp/cpld) and BBS (Software Help ➔ CPLD). The SVF to VCL translation tool is currently supported on HP700, SunOS 4.X, Windows NT and Windows 95 platforms. ♦

Procedure used to create an SVF file:

1. Create the design using XABEL-CPLD or any compatible third-party design entry tool.
2. Fit the design and save it to a JEDEC output file.
3. Invoke the EZTag software from the XACT® command line with the SVF option specified.
4. Generate an SVF file to “program,” “erase” or “verify” the selected part in the boundary-scan chain.