

Benchmarks Confirm XC9500 CPLD

The Xilinx XC9500 CPLD family provides the most-advanced, most-reliable pin-locking capability in the industry. This important feature allows designers to maintain pinouts after making design changes, eliminating costly, time-consuming PC board re-work. CPLDs that do not have adequate pin-locking capability often require pinout changes even after minor design changes, leaving no room for error and no possibility for field upgrades or field customization.

Pin-Locking Issues

In most CPLDs, each I/O pin is driven directly by a macrocell through an I/O block, as shown in **Figure 1**. When the

impacting both design performance and resource utilization.

Logic requirements also affect the ability of the fitter to place and route the design when the pinout is locked. Slow speed designs with simple, narrow logic functions requiring few inputs, feedbacks and product terms are inherently easier to pinlock than high speed designs with wide fan-in and product term intensive logic functions.

The Keys to Reliable Pin-Locking

To address these pin-locking issues, Xilinx XC9500 CPLDs feature abundant routing resources, wide function block fan-in and flexible product term allocation. The XC9500 fitter also optimizes the initial placement to maximize the design's pin-locking capability.

Pin-locking restricts the fitter's capability to place design resources; therefore, good routability is crucial. The routing resources of a CPLD determine how much of the logic block resources (inputs, product terms and registers) can be used to accommodate design changes after the pins are locked in a design. In a fully routable CPLD, buried logic can be moved without regards to routing restrictions, freeing function block resources that may be needed by the logic that drives the I/O pins.

The XC9500 family provides the most routing resources of any available CPLD family. All devices in the XC9500 family are 100% routable; if there are enough function block resources to implement the design, it will route.

Wide function block fan-in is another important requirement for pin-locking. Since CPLDs typically are used for high-speed, signal-intensive logic functions, wide function block fan-in is a requirement for implementing functions in a single logic

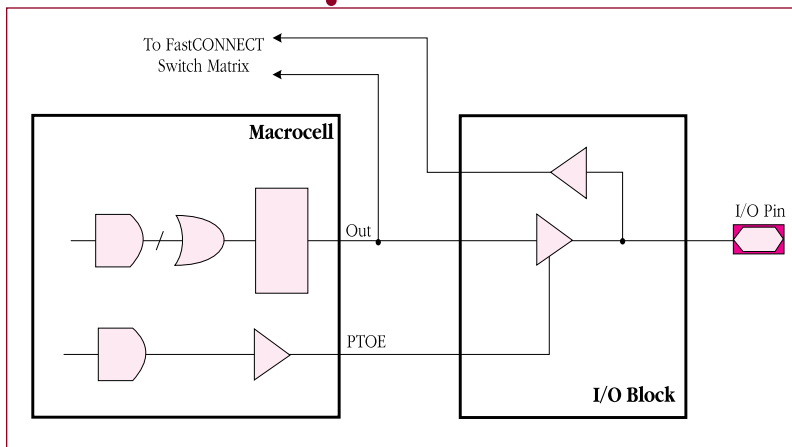


Figure 1: *Simplified XC9500 I/O Architecture*

design is pinlocked, the fitter is forced to map logic into specific macrocells to maintain the pinout. If the device architecture is limited, with inadequate routing in the central switch matrix, the fitter may not be able to place and route the design when the pins are locked.

Some CPLDs use an output routing pool to compensate for their primary routing deficiencies. However, output routing pools introduce additional delays and do not prevent the fitter from having to consume logic resources as routing feedthroughs,



Pin-Locking Capabilities

level. The number of available function block inputs affects the fitter's ability to add more signals to any logic that must remain in that function block (because it drives I/O pins). Wide fan-in capability also helps the fitter implement that logic in a single pass through the device.

Each XC9500 function block has 36 inputs from the switch matrix. Competing in-system programmable CPLDs have as few as 16 inputs.

Product term allocation is important to pin-locking because it allows design changes that increase the product term requirement. All XC9500 devices allocate individual product terms from anywhere in the function block to the macrocell that needs them, accommodating logic changes when the design is pinlocked.

In the XC9500 family, up to 90 product terms can be allocated to any macrocell in the function block. This is in contrast to competing CPLDs that restrict the product term availability (from 5 to 32 pterms) on the basis of macrocell location in the function block.

Fitter software is a key component of any successful CPLD pin-locking solution. The fitter must work in conjunction with the device architecture, spreading the outputs to accommodate design changes when the design is pinlocked.

The XC9500 fitter is optimized to take full advantage of the hardware resources of the XC9500 family. The Xilinx fitter is capable of intelligently utilizing all available device resources to retain pinouts and still maintain the required performance, even after significant design changes.

The Pin-locking Benchmarks

The following three sets of benchmark data show the relative pin-locking perfor-

mance of the XC9500 CPLDs and two competitor's ISP CPLD families. These benchmarks are based on typical applications such as address decoders, datapath designs and address counters. They illustrate the CPLD device's capability to accommodate design changes while maintaining an acceptable level of design performance; not only must the iterated design reroute when the pinout is maintained, it must do so with minimal impact on design performance. Therefore, all of the benchmark data is normalized to the design performance that is achieved when the fitters are free to choose the pinouts without restrictions.



“The benchmark results confirm the superior pin-locking performance of the Xilinx XC9500 family. This performance is consistent across all devices and package types.”

Address Decoder Benchmark

This benchmark design contains two 16-, 32- or 36-bit buses which are decoded to generate two chip select outputs and is intended to measure the effect of routing resources and function block fan-in on the CPLD's pin-locking capability. A typical design change involves the correction of an error in which the outputs are decoded incorrectly.



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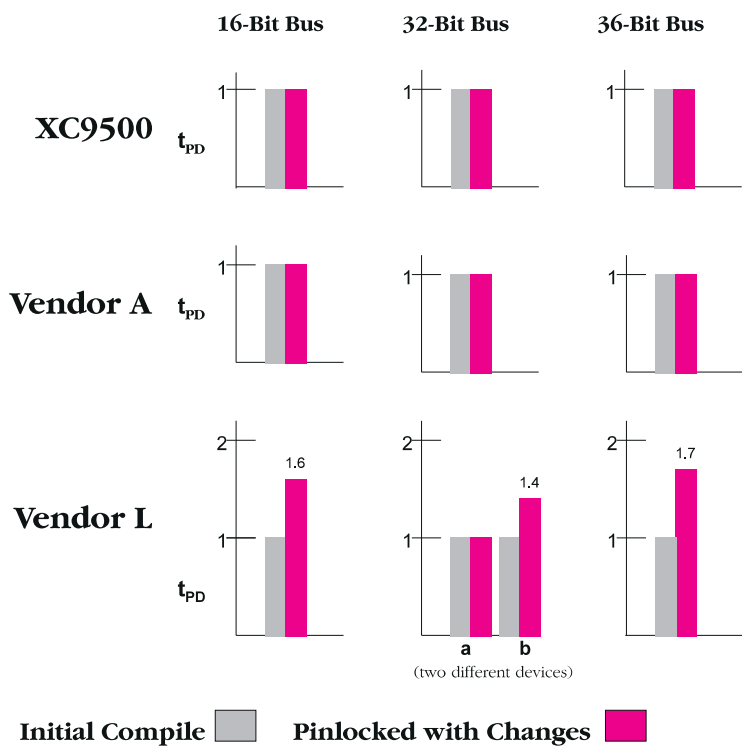


Figure 2: Address Decoder-Normalized Benchmark Results

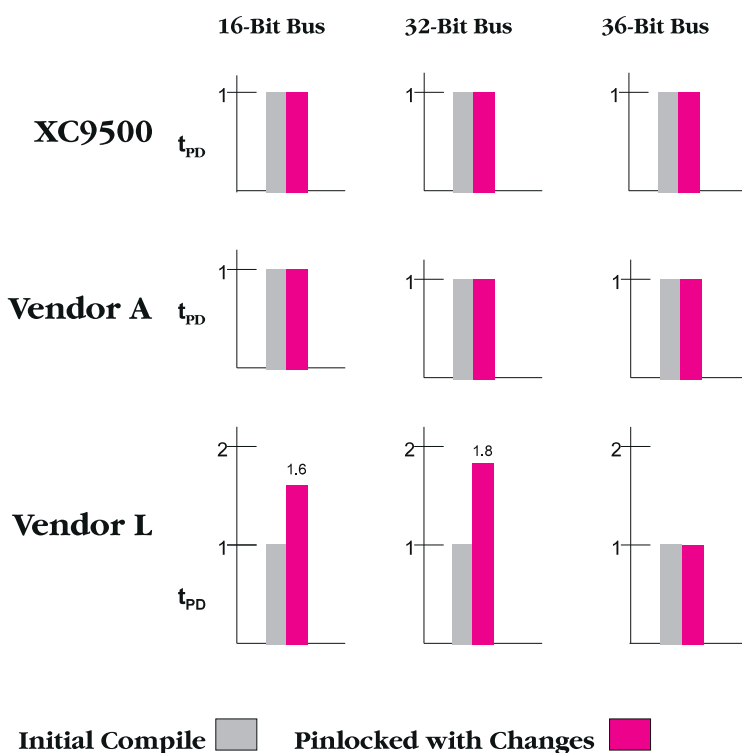


Figure 3: Data Path-Normalized Benchmark Results

XC9500 Benchmarks

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The benchmark results in **Figure 2** demonstrate that both the Xilinx XC9500 family and the Vendor A devices were able to accommodate the design changes without any impact on design performance. Vendor L devices maintained the same pinout, but with a significant (up to 60%) performance penalty. Since the Vendor L devices have 16 input logic blocks, the performance degradation of the 16-bit address decoder can be attributed to poor routing resources while the performance of the 32 and 36-bit decodes is degraded by both poor routing and narrow logic block fan-in.

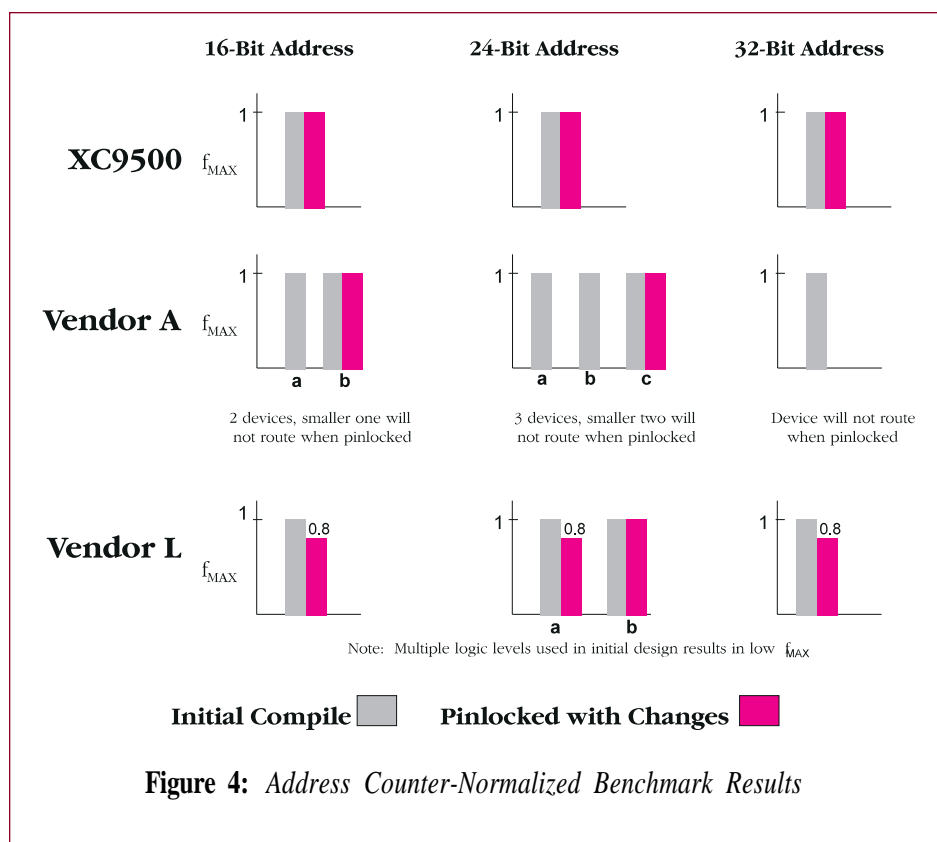
Datapath Benchmark

This benchmark design measures the affect of routing resources on the CPLD's pin-locking capability. This design contains a single 16-, 32- or 36-bit wide data bus. A typical design change involves the reordering of data bits.

The benchmark results shown in **Figure 3** show that both the Xilinx XC9500 family and Vendor A devices were able to accommodate the design changes without any impact on design performance. Vendor L devices sacrificed performance (up to 80%) to reroute the design when pinlocked. Since only one logic block input was required for each output, this performance degradation can be attributed to poor routing resources, or fitter performance, or both, but cannot be attributed to logic block fan-in.

Address Counter Benchmark

This benchmark design contains two 16-, 24- or 32-bit loadable address counters loaded from separate buses but with common clock and hold signals. A typical design change alters the initial count load value. This benchmark measures the effect of routing resources and function block fan-in on the CPLDs pin-locking capability



when macrocell feedbacks and other high fan-out signals are involved.

The benchmark results shown in **Figure 4** demonstrate the superiority of the XC9500 CPLD architecture. All XC9500 devices were able to accommodate the design changes without any impact on design performance. When Vendor A's routing resources were

stressed, performance didn't just degrade, the devices completely failed to route.

Vendor L devices used several layers of logic in the initial design, with correspondingly low f_{MAX} . This enabled the fitter to reroute the design using alternate routing paths, with less performance degradation (20%) than designs initially requiring only one logic level.

Conclusions

The benchmark results confirm the superior pin-locking performance of the Xilinx XC9500 family. This performance is consistent across all devices and package types. The wide function block fan-in enables pin-locking of wide, high-speed logic functions. Furthermore, because feedthroughs are not needed for routing, there is no performance degradation due to routing congestion. This timing consistency is as important as routing ability for maintaining pin-locked designs.

The XC9500 CPLD devices feature the industry's best pin-locking capability, eliminating the need for PCB modifications due to design changes. This feature not only shortens design cycles and decreases design costs but also facilitates the use of in-system programmability to upgrade or modify systems in the field. ♦