

CPLDs

Q When using XABEL-CPLD™, how do I specify fast slew rates for Xilinx CPLDs?

By default, the slew rate is SLOW for all pins. The FAST attribute is used to selectively control the slew rate on a pin-by-pin basis for any output signal. In XABEL-CPLD, use the following syntax:

```
XEPLD PROPERTY 'FAST ON
signal_list';
```

If you omit the signal name list, the FAST property applies to all pins. If you include a signal name list, the listed signals are given the specified setting and all other signals are given the opposite setting.

Q When using schematic capture, how do I specify fast slew rates for Xilinx CPLDs?

To assign individual pins in a schematic to use the faster slew rate, attach a FAST attribute to the output pad.

Q When using the Xilinx Synopsys Interface (XSI), how do I specify fast slew rates for Xilinx CPLDs?

The Synopsys HIGH attribute translates to a SLOW Xilinx slew rate, and the NONE attribute translates to a FAST Xilinx slew rate. As with the other design entry methods, the XSI default for outputs is SLOW. To set all outputs for FAST slew rate, use the following syntax:

```
set_pad_type -slewrates NONE
all_outputs ();
```

Use this command after specifying the set_port_is_pad command and before implementing the insert_pads command. You can set any individual output for fast signal transition by using the following syntax:

```
set_pad_type -slewrates NONE
port_name
```

Mentor Graphics

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Q Running Convert Design to retarget designs (as described in XCELL 20, page 41) loses NET, LOC, and other properties associated with schematic ports and PADs in my design. What's happening?

This is due to a change in Design Architect that occurred between Mentor A.1 and A.4. A fix is available by E-mailing xdocs@xilinx.com with "send 822" in the subject line. The problem also has been fixed in XACT 5.2.1.

Q While running Quicksim II under Solaris, I get the following errors on all of my RAMs and ROMs:

```
/MEMORY/sp_ram32': Problems
loading binary '$LCA/gen_lib/
sp_ram32/sp_ram32.ss5_b'
Could not load object file
"/tools/ds344/gen_lib/sp_ram32/
sp_ram32.ss5_b"
No such file or directory
```

What does this mean and how is it fixed?

Unlike standard QuickPart models, Xilinx RAMs and ROMs are described using "behavioral language models" (BLMs), that have as their core a binary executable file. This file is named differently for each platform: .ss5_b for SunOS, .ss5_b for Solaris, etc. Thus, under Solaris, Quicksim expects to find a .ss5_b file where none exists, since Solaris-native versions of the RAM and ROM models are not part of released XACT 5.x software. However, an unofficial RAM and ROM patch is available on the Xilinx BBS:

```
Category: Software Help
Subcategory: Mentor
Filename: SOLARMEN.ZIP
```

This is a compressed TAR file that needs to be extracted in the \$LCA directory.

Note: Currently, Xilinx does not officially support the Solaris operating system. This is an unofficial patch and, as such, has not been fully tested.

Q While running Fncsim8 under Solaris, Gen_sch8 or XBLXGS generates this error message:

```
crtl:bad [02] open: /tools/
mentor/lib/mgc_ld.so
Abort - core dumped
```

What does this mean and how can I fix it?

Gen_sch8 and XBLXGS are incompatible with Solaris, so their use should be avoided under this operating system. This usually involves avoiding XBLOX or XABEL components on schematics. If the design contains RAM or ROM components, obtain the library patch described in the answer to the previous question.

Q I encountered the following error during EDIF2XNF:

```
Error: 3 port name I1 not
found on external library
primitive for cell OR2
```

What does this mean and how can I fix it?

This error usually occurs from mixing Xilinx libraries (i.e., obsolete and Unified) or having an incorrect library setting in EDIF2XNF. For more information, E-mail xdocs@xilinx.com with "send 396" in the subject line.

Q Will XACTstep v5.2 work with Mentor Graphics' B.1 release?

Xilinx strongly recommends using the Mentor A.x release with XACTstep v5.2, as Xilinx has not tested Mentor B.1 and will not officially support this product until the Merged Release. However, testing by Mentor Graphics found that the implementation flow and most of the simulation flow should work properly. Gen_sch8 and XBLXGS were found not to work properly due to problems associated with dynamic linking to Mentor's Design Data Port (DDP). If you must use Mentor B.1, avoid using XBLOX or XABEL components in your designs, if possible, to eliminate the need to run Gen_sch8 or XBLXGS.

Synopsys

Q How can I initialize my XC4000E RAM module?

The contents of an XC4000E RAM at power up may be specified (initialized) by the user. When RAM modules are instantiated directly in the HDL source code, initialization values for the RAM may be entered using the following command:

```
set_attribute
  "instance_name" xnf_init
  "init_value" type string
```

Replace "instance_name" with the actual instance name of the RAM module that has been instantiated. For 16-location RAMs, specify a 4-digit hexadecimal value for "init_value". For 32-location RAMs, specify an 8-digit hexadecimal value. *NOTE: Although this mechanism permits RAM-initialization information to be carried into the FPGA implementation tools for incorporation into the configuration bitstream, it does not affect behavioral simulation. For behavioral simulation, a RAM's contents remain unknown until they are defined by valid write accesses. However, backannotated functional or timing simulation will reflect this RAM initialization information.*

Q What should my .synopsys_dc.setup and .synopsys_vss.setup files contain to synthesize and simulate XC4000E designs?

.synopsys_dc.setup: The .synopsys_dc.setup file for XC4000E synthesis should be identical to that for XC4000 designs, with the exception of the target- and link-library settings and the reference to the XBLOX DesignWare Library. An example .synopsys_dc.setup file is shown below. The target- and link-library settings were created using the command: synlibs 4005e-3

```
search_path = { . \
<XC4000E_DS401_install_path>/
synopsys/libraries/syn \
```

```
<Synopsys_install_path>/
libraries/syn}
define_design_lib xblox_4000e
-path \
<DS401_install_path>/
synopsys/libraries/dw/lib/
fpga/xc4000e
compile_fix_multiple_port_nets
= true
xlnx_hier_blknm = 1
xnfout_library_version =
"2.0.0"
bus_naming_style = "%s<%d>"
bus_dimension_separator_style
= "><"
bus_inference_style =
"%s<%d>"
link_library = {xprim_4005e-
3.db xprim_4000e-3.db
xgen_4000e.db \
xfpga_4000e-3.db xio_4000e-
3.db}
target_library =
{xprim_4005e-3.db
xprim_4000e-3.db
xgen_4000e.db \
xfpga_4000e-3.db xio_4000e-
3.db}
symbol_library =
{xc4000e.sdb}
synthetic_library =
{xblox_4000e.sldb
standard.sldb}
```

The reference to the XC4000E XBLOX DesignWare library is differentiated from the XC4000 XBLOX library with a new name: xblox_4000e.

.synopsys_vss.setup: The .synopsys_vss.setup file for XC4000E simulation should also be identical to that for XC4000 designs with the exception of the simulation-library reference. An example .synopsys_vss.setup file is shown below.

```
timebase=ns
time_res_factor=0.1
no_hazard_mesg=true
WORK > DEFAULT
DEFAULT : ./WORK
xc4000e:<XC4000E_DS401_install_path>/
synopsys/libraries/sim/lib/
xc4000e
```

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Europe

UK, London Office

telephone: (44) 1932 349402

fax: (44) 1932 333530

BBS: (44) 1932 333540

e-mail: ukhelp@xilinx.com

France, Paris Office

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