

# Using OrCAD Capture and Simulate

The OrCAD interface software provided by Xilinx supports the SDT 386+ schematic editor and VST 386+ simulator. The new Windows-based OrCAD tools, Capture and Simulate, are not directly supported. This article outlines the recommended flow for interfacing Capture and Simulate with the XACTstep tools.

More information on the design flow is also available from OrCAD (*OrCAD Application Note #12, Using OrCAD Capture and Simulate with Xilinx XACT XDM or XACTstep*, and the Simulate for Windows on-line help topic: Xilinx).

## USING CAPTURE

For Xilinx projects, keep each DSN file in a separate directory. Each project directory will contain the Capture DSN file, the INF netlist files, the XNF files used as input to the XACTstep tools, and the XPROJECT subdirectory.

### Translating Xilinx Schematic Libraries

OrCAD Capture can automatically convert the schematic libraries shipped by Xilinx. Simply choose **File⇒Open⇒Library**. In the dialog box, list files of type **SDT Library** and open the desired library (for example, C:\XACT\XC4000\XC4000.LIB). Capture will open another dialog box, asking where you would like to save the translated library. Save the library in the same directory, and do not change the library name. Changing the library name will result in an invalid INF netlist. In the above example, the library should be saved as C:\XACT\XC4000\XC4000.OLB.

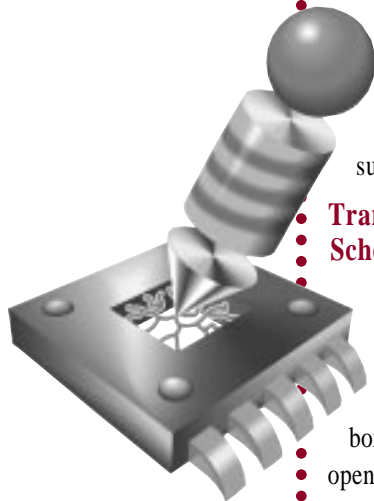
The Xilinx Unified Libraries can also be downloaded from the Xilinx Technical BBS at 408-559-9327 (filename XOLB.ZIP). These libraries already have the default Xilinx part properties added (see the *Adding Xilinx Attributes* section).

### Adding Xilinx Attributes

You can use part properties in Capture schematics to add Xilinx attributes to your design. Unlike SDT, Capture stores default part properties directly in the Xilinx library or your design. You can introduce the default Xilinx part properties (described in Chapter 11 of the *XACTstep OrCAD Interface/Tutorial Guide*) into the Xilinx libraries by using the **Tools⇒Import/Export Properties** commands (described in Chapter 16 of the *OrCAD Capture for Windows User's Guide*), or download the libraries from the BBS.

To add a Xilinx attribute to a part:

1. Double-click on the part.
2. In the **Edit Part** dialog box, click **User Properties**.
3. In the **User Properties** dialog box, select the property you wish to edit (for example, OPTIONS\_1 in an XC4000 design).
4. Enter the attribute in the value field (for example, loc=p11) and press <ENTER>.
5. When you are done editing properties, click OK to return to the **Edit Part** dialog box, then click OK to return to the schematic.



# with XACTstep™ version 6

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## USING CAPTURE(CONTINUED)

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Unlike SDT, Capture allows properties to be placed on hierarchical blocks (formerly known as sheet symbols). Because the Xilinx flow uses the old INF netlist format, properties on hierarchical blocks are not supported.

For Xilinx attributes to be properly written into the INF netlist, select **Options⇒Design Properties** when the **Design Manager** window is active. Select the **SDT Compatibility** tab, and enter the property names that will map into the INF netlist in any order. You do not have to include property names that are not used in the design (for example, if you only use the LOC,OPTIONS property in your XC3000 design, you do not have to enter the BASE, INIT, and other property names in the SDT Compatibility tab). When converting an SDT design, Capture automatically updates the SDT Compatibility table to reflect the property names listed in the SDT.CFG file.

### Migrating Between Xilinx Families

Capture uses a design cache to store the library components that are used in each design. To migrate an existing design from one Xilinx architecture to another, the components in its cache must be replaced. In the Design Manager window, double-click on the **Design Cache** folder to open it (if there is no **Design Cache**, select **View⇒Logical** to switch to logical view). Click on the first part in the cache, then select **Design⇒Replace Cache**. In the dialog box, edit the **Part Library** field or use the Browse button to select the new Xilinx library. Repeat this procedure with each part in the cache.

### Generating an XNF File

Make sure that the **Design Manager** window is the active window. From the menus, select **Tools⇒Update Part References**. In the dialog box, click OK. Then select **File⇒Save** to save the updated design.

Select **Tools⇒Create Netlist**. In the dialog box, select the **VST** tab. You can change the name of the top level INF file, but do not change the destination directory.

Open an MS-DOS session and CD into the project directory. Execute the following command:

```
> sdt2xnf <design>.inf -p  
    <parttype>
```

where <design> is the name of the top-level design and <parttype> is the target Xilinx device (for example, 3120APC84-2)

Exit the DOS session, then open the XACTstep Design Manager. Select **File⇒New Project**. In the **New Project** dialog box, click on the **Browse** button to select an input design. List files of type XNF, and select <design>.XNF as the input file. Click OK. Select the target family and click **Translate**. In the **Translate** dialog box, click OK.

### Known Issues

Unlike SDT, Capture writes a configured library into an INF netlist only if parts from that library are used in the schematic. If the top level schematic contains no parts from a “standard” Xilinx library (XC2000, XC3000, XC4000, XC5200 or XC7000 library), an invalid INF file will be created. For example, if the top level

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## Using Capture

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schematic contains only hierarchical blocks, XBLOX parts, and/or user library parts, SDT2XNF will issue the following error:

```
DS35-SDT-ERROR-033:  
No standard Xilinx XC2000/  
XC3000/XC4000 SDT libraries  
were used in the INF file  
design.inf'.
```

To prevent this error, place a part from the appropriate standard Xilinx library on the top level schematic. If the part is left unconnected, it will be trimmed by the Xilinx tools.

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### USING SIMULATE

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For functional simulation, create an XFF file using the **Design⇒Translate** command in the XACT<sub>step</sub> Design Manager or an XNFBA.XNF file by checking the Flow Engine

**Setup⇒Options⇒Produce Timing Simulation Data** box. For timing simulation, the XNFBA.XNF file must be used.

Create a new simulation project. In the **Edit Simulate Project** dialog box, do not add any netlists to the project. Click **OK**.

Select **Tools⇒Convert XNF to VHDL**. In the dialog box, edit the **XNF Input File** field or use the **Browse** button to select the input file. Specify the name of the output VHDL file and top level entity, and select whether you are performing a functional or timing simulation. Click **OK**.

#### Known Issues

The following is a list of problems that have been encountered while performing Xilinx simulations with Simulate v6.0. These issues have been addressed in Simulate v6.10.

- XFF files containing CLBMAP symbols cannot be simulated. To perform functional simulation on these designs,

create an XNFBA.XNF file and select **Functional Simulation** in the **Convert XNF to VHDL** dialog box.

- There are no models for NAND gates. These models have been added, and a new XVHDL.AUX file is available on the OrCAD BBS (503-671-9401) or on the OrCAD web site ([www.orcad.com/tbbs/SIMULATE/LIBRARY/ORCAD](http://www.orcad.com/tbbs/SIMULATE/LIBRARY/ORCAD)). Look for the file called xvhdl.zip.
- The VHDL model for the T pin of the BUFT component has incorrect polarity in some of the libraries. This affects simulation of the following components: BUFT, BUFT4, BUFT8, BUFT16, BUFE, BUFE4, BUFE8, BUFE16.
- The VHDL model of the FDPE component initializes the flip-flop output to 0 instead of 1.
- Some XBLOX™ designs containing falling-edge-triggered flip-flops cannot be simulated using timing information. Only functional simulation is possible on these designs. ♦

# X<sub>S</sub> A<sub>T</sub> C<sub>E</sub> T<sub>P</sub>