

XC9500 CPLDs:

Managing the “Product Life Cycle”

The XC9500 CPLD family incorporates a unique combination of product features specifically developed to meet all the needs for in-system programming (ISP) throughout the entire “product life cycle.” This product life cycle starts with board-level prototyping and system debug, advances to programming and board-level testing during manufacturing, and finally completes with field upgrades.

The XC9500 product features reduce the total cost of ownership by eliminating many of the traditional problems of product development using PLDs. These features include 5 V in-system programmability,

superior pin-locking capability, support for 10,000 program/erase cycles, and full 1149.1 JTAG support for in-system debug and version control.

Design and Prototyping

ISP-capable CPLDs provide a definite benefit

over devices requiring an external programmer. ISP devices eliminate the handling errors and damage associated with removing the chip from the socket on the circuit board.

Through the multiple design iterations of the debug and prototyping process, the ISP CPLD can be repeatedly reprogrammed with different patterns while soldered on a printed circuit board (PCB). The ability of the architecture and tools to

support pin-locking — that is, the ability to maintain a fixed pinout while making logic changes internal to the device — is crucial to avoid expensive and time-consuming board rework. The XC9500 CPLD, originally architected for in-system programming, offers users the best in pin-locking capability.

Many existing ISP devices are fabricated using traditional EEPROM technology. However, the advanced XC9500 FastFLASH™ technology provides several advantages over EEPROM technology. Foremost among these is programming endurance. EEPROM technology typically allows 100-1000 program/erase cycles. FastFLASH technology has an endurance of 10,000 program/erase cycles. This high programming endurance minimizes or eliminates costly board rework resulting from reprogramming failures.

System Integration

When the entire system is assembled for test and debug, all important logic states should be easily accessible, and internal logic implementations within each device should be capable of being checked. Each XC9500 device supports the IEEE 1149.1 boundary-scan specification, including INTEST and USERCODE instructions used to easily access and debug user logic and track pattern revisions, respectively.

Manufacturing

Concurrent programming of all XC9500 CPLDs in the system with the standard JTAG interface simplifies the manufacturing flow in the production stage. Programming can be done after board assembly. This reduces production inventories, eliminates the need for tracking multiple



devices with multiple codes, and abolishes the stand-alone programming step. The resulting reduction in programming time also results in significant cost savings, especially at high unit volumes. Furthermore, built-in version control and in-system board customization contribute to manufacturing flexibility, saving time and money.

Field Upgrades

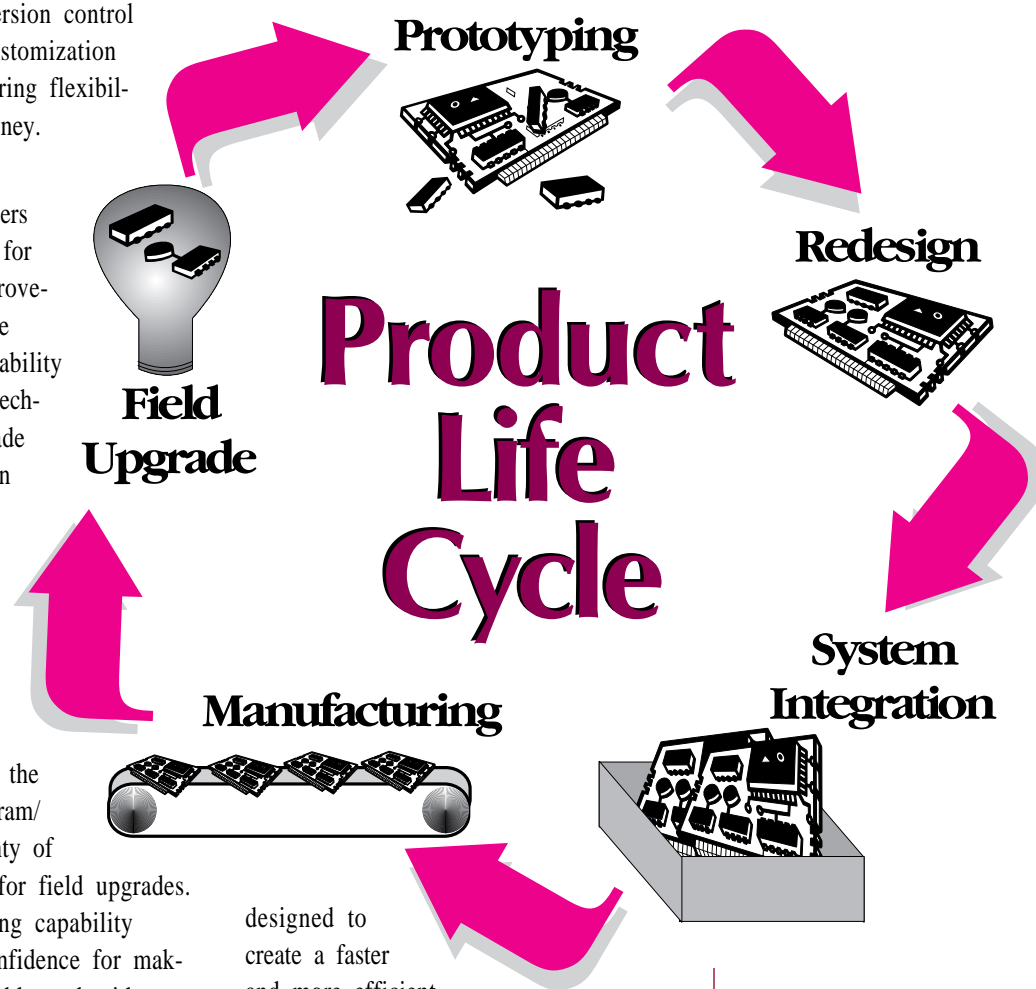
In the past, CPLD users were hesitant to design for field upgrades and improvements because of device reprogramming and reliability fears. With FastFLASH technology, true field upgrade and repair capability can now be designed into the product.

Since the XC9500 family is easily programmed through the JTAG port, any design can be easily prepared for "upgrading in the field." The 10,000 program/erase cycles ensure plenty of "reprogram headroom" for field upgrades. The enhanced pin-locking capability provides the highest confidence for making design changes reliably and without requiring expensive board re-work.

Two more XC9500 JTAG operations enhance field upgrade capability by aiding with system repair strategy. SAMPLE/PRELOAD operations allow output sampling and input stimulus preloading while the device is fully operational. The

HIGHZ command disables bussed lines, facilitating the isolation and diagnosis of interconnect failures.

Xilinx products have always been



designed to create a faster and more efficient product development process. By using the XC9500 in-system-programmable CPLDs, users can now add to those benefits the flexibility, pin-locking capability, performance, reliability and testability necessary for supporting the ever-shorter product life cycle. ♦